USERS MANUAL

f 1625,-

TEAC MT-2

extra: bodig:
f 110,- 12 V-voeding 1,8 A
f 92,- 5 V-voeding 0,75 A
documentatie
f 16,- spec.
f 70,- instructie
ca. f 50,- ? konnektor, kast !/

1. SPECIFICATIONS

DATA FORMAT

Data format complies with ISO-3407, ECMA-34, JIS-C6281 and other similar standards.

Recording Format:	Phase Encoding
Recording Density:	800 bpi(32 bits/mm, nominal)
Number of Tracks:	Single Track

CONSTRUCTION

Exterior Dimensions:	105(H) x 120(W) x 91(D)mm
Weight:	1.2kg, Max.

MECHNICAL CONSTRUCTION

Tape Drive System:	D.C. Motor Direct Reel Drive System
Tape Speed Detection System:	Encoder Detection
Cassette Insertion:	Pocket Holder type
Cassette Eject Mechanism:	Manual Ejection by depressing EJECT Button
BOT/EOT & Clear Leader Detector:	Photoelectric Detector
Magnetic Head:	Single Track, Single Gap Read/Write Head

POWER REQUIREMENTS

	Average Current Consumption	Maximum Current Consumption	Permanent Ripple Voltage
D.C.+12V±5%	1.0 A	1.8 A*	Less than 100mVp-p
D.C.+ 5V±5%	0.7 A	0.75A*	Less than 100mVp-p

* Except for surge current at power-on

GROUND ISOLATION

Insulation resistance between 0V power supply and frame ground: 5 Meg Ohms or more, at 150V D.C.

ENVIRONMENTAL CONDITIONS

Temperature range(Operating):	+5°C ~ +40°C
(Storage):	-15°C ~ +60°C
Relative Humidity Range(non-condensing)	
(Operating):	20% ~ 80%
(Storage):	10% ~ 90%
Vibration(Operating):	Less than 0.5G(less than 120Hz)
(Packaged Condition based on TEAC standard packing):	
Impact:	Less than 40G(less than 30msec)
Continuous:	Less than 3G

OPERATIONAL CHARACTERISTICS

Tape Speed(Slow):	15 ips(38.1cm/s) ± 3%
(Fast):	45 ips(114.3cm/s) ± 4%
IBG:	0.97 ± 0.24 inch(24.64 ± 6.10mm)
Erased Length	2.19 ± 0.27 inch(55.63 ± 6.86mm)
Initial Gap:	2.26 ± 0.40 inch(57.40 ± 10.16mm)
Readable IBG Length	0.7 inch(17.78mm) or more
Required tape length for Long IBG detection:	15.0 ~ 22.2 inch(381.0 ~ 563.9mm)
Start distance for HIGH SPEED SEARCH:	2.4 inch(60.96mm) or less

Stop distance for HIGH SPEED
SEARCH: 1.9 inch(48.26mm) or less
Nominal Data Transfer Rate: 12k birs/sec
Recording Density 800 bpi ± 4%
Treshold Level(at reference read level)
(LOW): 18 ± 3%
(HIGH): 40 ± 5%

INTERCHANGEABILITY

Cassette tapes which comply with the Information Interchange format standardized in ISO-3407, JIS-C6281, and etc. are securely read by the MTU. Also cassette tapes written with the MTU enable the perfect interchangeability with the Information Interchange format standardized in ISO-3407, JIS-C6281, and etc.

MTBF

10,000 hours or more at the 10% rate of operation

MAGNETIC TAPE

Magnetic tape cassette for Information Interchange which comply with ISO, ANSI, ECMA, JIS, and other similar standards. Also the cassette used for the MTU shall be previously approved between TEAC and the customer.
Recommended tape: TEAC CT-300

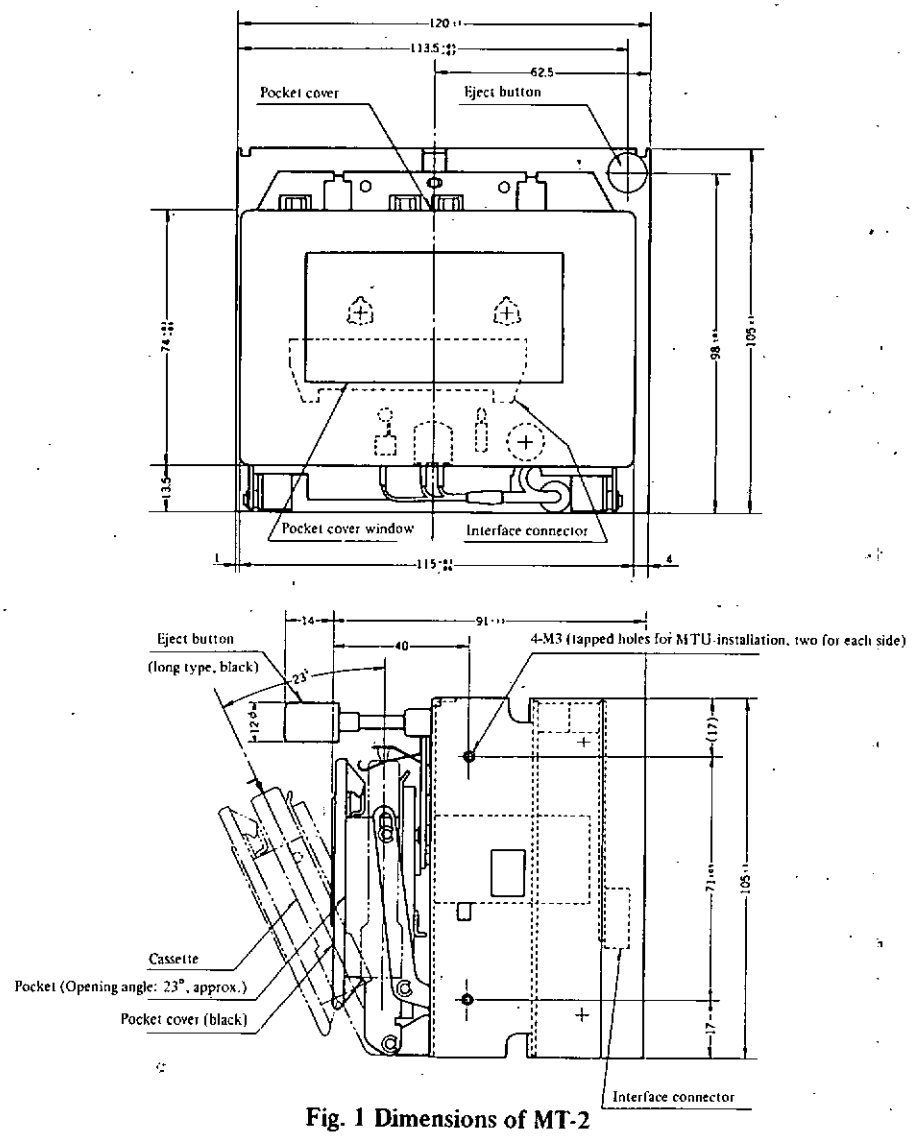


Fig. 1 Dimensions of MT-2
(unit: mm)

2. INTERFACE

2.1. INPUT/OUTPUT SIGNALS(EIGHTEEN SIGNALS OF SIX TYPES)

i)	Bi-directional data lines(DO ~ D7)	8 lines
ii)	Select lines(SEL, RSO ~ RS2)	4 lines
iii)	Data transfer control lines(READ, ECLK)	2 lines
iv)	Interrupt request line(IRQ)	1 line
v)	DMA control lines(DRQ, DACK)	2 lines
vi)	Reset line(RST)	1 line

2.1.1. DO ~ D7(DATAO ~ DATA7) Input/Output signal
Eight bi-directional data lines for the data transfers between the CPU and the MTC. The three-state output drivers remain in the high impedance state except for the output operations of the MTC.

magnetic tape cassette

2.1.2. SEL(SELECT) Input signal
If the ECLK signal is given while this signal is at LOW level, the MTU is selected and the data writing to the internal registers and data reading from the internal registers of the MTC can be performed. The internal registers are selected by RSO ~ RS2 signals and either the writing or the reading is selected by the READ signal.

2.1.3. RSO ~ RS2(REGISTER SELECT 0 ~ 2) Input signal
These signals select one of the eight registers from RO to R7. The same as the SEL signal, these signals shall remain the determined level during the data transfers.

2.1.4. READ Input signal
A signal to determine the data transfer direction of the data lines (DO ~ D7). When the READ signal is at LOW level the data transfer direction is the output direction, while it is the input direction when this signal is at HIGH level. Data are transferred from MTU to CPU at output direction and from CPU to MTU at input direction. If this signal is input with DACK signal, the directions are reversed, i.e., input direction at LOW level and output direction at HIGH level.

2.1.5. ECLK(ENABLE CLOCK) Input signal
Only one timing signal to be supplied from the CPU to the MTC. All the data transfers are performed in synchronization with this signal. When this signal is in LOW level, data transfers are enabled.

2.1.6. IRQ(INTERRUPT REQUEST) Output signal
A signal to request an interrupt to the CPU. If an interrupt request occurs in the MTC, the signal becomes LOW level and the level is held LOW until the CPU reads out the contents of the register ISR(INTERRUPT STATUS REGISTER) in the MTC.

2.1.7. DRQ(DMA REQUEST) Output signal
When the MTU is at the DMA mode and a data transfer request (DA or DBRE) occurs in the MTU, this signal goes LOW level for requesting the data transfers to the DMA controller. The IRQ signal does not output at this time.
An external DMA controller is required for the DMA transfers.

2.1.8. DACK(DMA ACKNOWLEDGE) Input signal

A signal to respond to the DRQ signal. The MTC resets DA or DBRE when this signal becomes LOW level. Accordingly, DRQ signal also returns to HIGH level. At the LOW level of this signal, the external DMA controller controls the data transfers from MEMORY to DBR(DATA BUFFER REGISTER) or from DBR to MEMORY with READ and ECLK signals. The data transfer direction determined by the READ signal is opposite to the normal transfers at this time which is output direction at HIGH level and input direction at LOW level.

2.1.9. RST(RESET) Input signal

When the signal is set to LOW level, all the registers in the MTU are cleared and the MTU returns to the initial condition. This signal shall be supplied until the power supply voltage reaches the stable condition after the power-on to perform the power-reset. MTU can be operated from 1μsec after this signal returns to HIGH level.

2.2. INPUT/OUTPUT CIRCUITS

2.2.1. Electrical Characteristics of Signals

Following specifications apply to the Interface Connector of the MTU.

LOW Level(TRUE):	0 ~ 0.5V(Stable condition)
HIGH Level(FALSE):	2.4 ~ 5V(Stable condition)
Interface Receiver Sink Current:	2.0m A or less(Stable condition)
Interface Driver Sink Current Capacity:	
DATA0 ~ DATA7 Input/Output Signals:	32m A or less
For other Output Signals :	16m A or less

2.2.2. Interface Connector

Number of Pins:	50 pins(25 pins, double)
Pin-Pitch:	0.1 inch(2.54mm)
MTU Side Connector:	FCN-705P050-AU/00 manufactured by FUJITSU Limited., or equivalent.
MTU Side Connector Pin Location:	Fig.4

Cable Side matched connector:

Connector No.3425 manufactured by 3M Co.Ltd., connector No.FCN-705J050-AU/00 manufactured by FUJITSU Limited., 65043 series manufactured by BERG ELECTRONICS,INC., or equivalent.

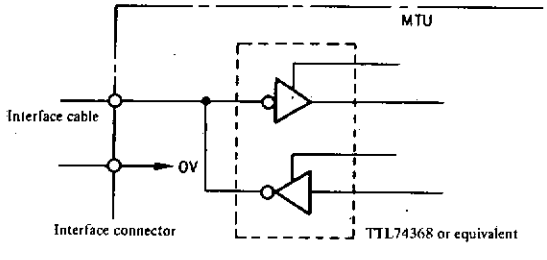


Fig. 2-1 Driver/Receiver (DATA0 ~ DATA7 Input/Output signals)

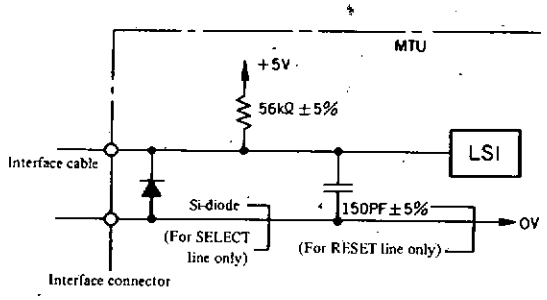


Fig. 2-2 Receiver (RESET, SELECT Input Signals)

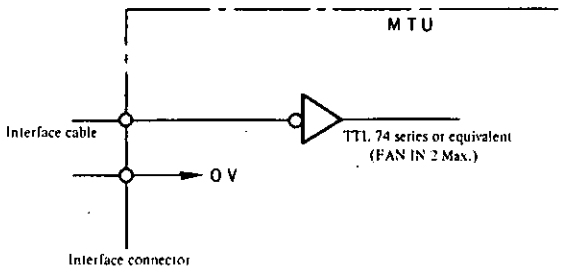


Fig. 2-3 Receiver (other Input Signals)

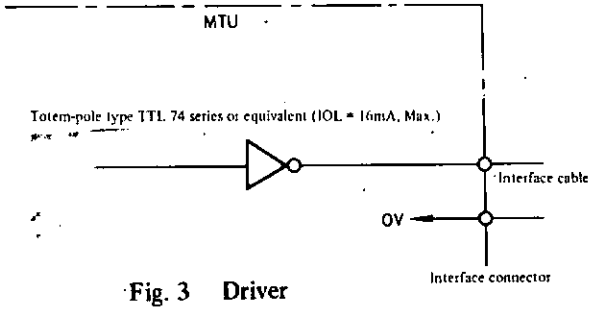


Fig. 3 Driver

SIGNALS	PIN NOS	DIRECTION
RESET	3	MTU ⟵ CPU
ENABLE CLOCK	5	⟵
READ	7	⟵
DATA 7	9	⟷
DATA 6	11	⟷
DATA 5	13	⟷
DATA 4	15	⟷
DATA 3	17	⟷
DATA 2	19	⟷
DATA 1	21	⟷
DATA 0	23	⟷
SELECT	25	⟵
INTERRUPT REQUEST	27	⟶
DMA REQUEST	29	⟶
DMA ACKNOWLEDGE	31	⟵
REGISTER SELECT 2	33	⟵
REGISTER SELECT 1	35	⟵
REGISTER SELECT 0	37	⟵
+12V	46, 47, 48, 49	⟵
+5V	43, 44, 45	⟵
0V	39, 40, 41, 42, 4, 6, 8 10, 12, 14, 16, 18, 20 22, 24, 26, 28, 30, 32 34, 36, 38	⟷
FRAME GROUND	2	⟷
NO CONNECTION	1	
POLARIZING KEY	50	

Table 1 Input/Output Signals and Terminal Nos.

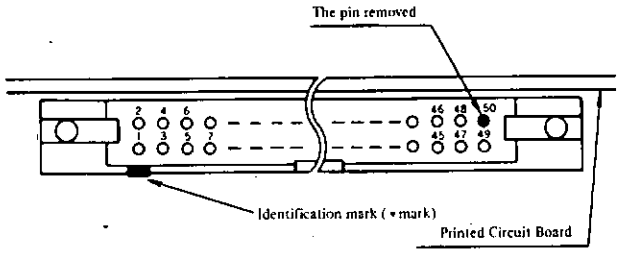


Fig. 4 MTU side connector pin location

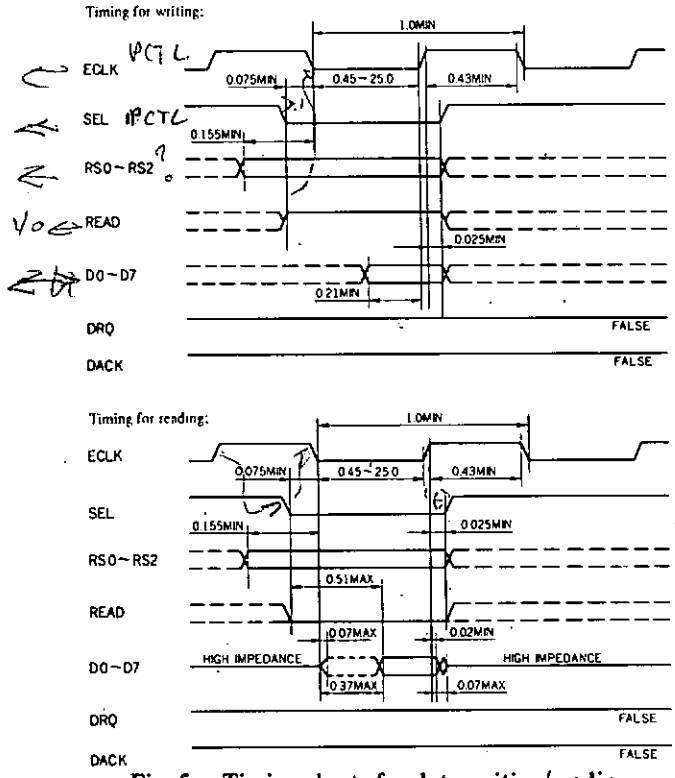


Fig. 5 Timing charts for data writing/reading.
(unit: μ sec)

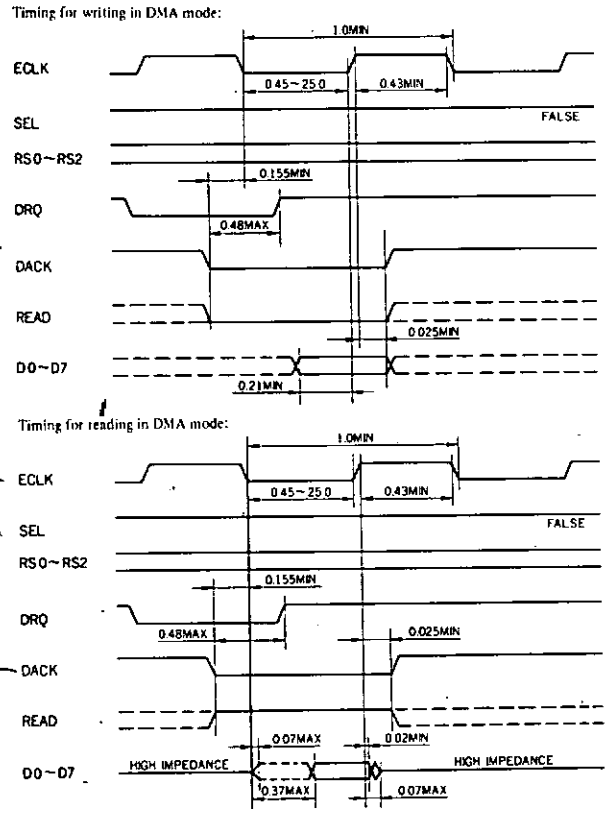


Fig. 6
Timing charts for data writing/reading in DMA mode.
(unit: μ sec)

INTERFACE CABLE

1. Signal lines
   Conductor Resistance: 350 ohms or less/km
   Inter-lines electrostatic capacity: 0.1 μF or less/km
2. Maximum Cable Length
   For AWG #28, 50 lines, flat cable: 2m or less.

3. REGISTERS

Fig.7 shows the internal registers in the MTC. One of these registers is selected by the CPU through three signals RS0 ~ RS2. Data transfers are performed through the lines D0 ~ D7 and the transfer direction (input or output) is determined by the READ signal.

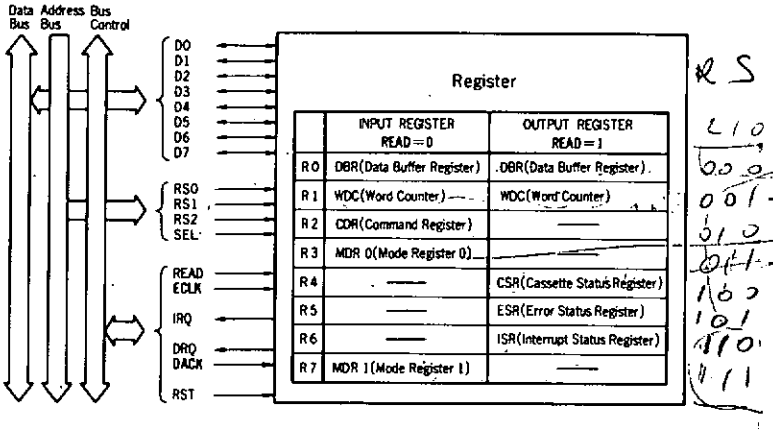


Fig. 7 BUS Interface

3.1. FUNCTION OF INTERNAL REGISTERS

Control commands, status infromation, write or read data, setting of data transfer words between the MTC and the CPU are performed through these registers.

3.1.1. DBR(DATA BUFFER REGISTER) Input/Output, R0

RS		D	
0	0	0	DATA 0(LSB) Least Significant Bit
1	0	1	" 1
2	0	2	" 2
		3	" 3
		4	" 4
		5	" 5
		6	" 6
		7	" 7(MSB) Most Significant Bit

Data are transferred between the CPU and the MTU through this register. At the False state("0") of the READ signal, DBR becomes Input Register and the data can be written into the CMT. At the True state("1"), it becomes Output Register and the data can be read out from the CMT.

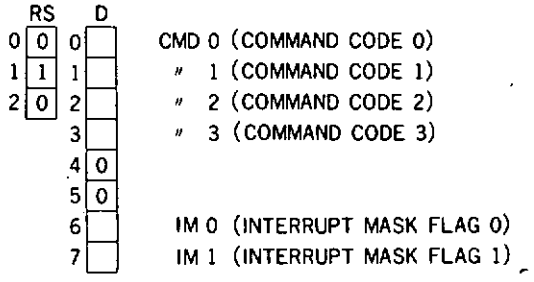
3.1.2. WDC(WORD COUNTER) Input/Output, R1

RS		D	
0	1	0	2^0
1	0	1	2^1
2	0	2	2^2
		3	2^3
		4	2^4
		5	2^5
		6	2^6
		7	2^7

A register to determine the number of data to be transferred between the CPU and the MTC. The number of data to be transferred shall be designated in bytes and expressed in a positive binary notation to this register before the input of a WRT command or RDH/RDL command.

The number of data designated by this register are written into the cassette tape for a WRT command. And as much read data as designated by this register for RDH or RDL command are transferred from the cassette tape to the CPU.
1 through 256 bytes are available for the number of data to be designated.(Write "0" to this register for designating 256 bytes).

3.1.3. CDR(COMMAND REGISTER) Input, R2



1) CMD0 ~ CMD3
By writing a control command code to the bits from CMD0 to CMD3, the MTU starts its operation.
Table 2 shows the control commands and command codes.

MNEMONIC	CMD 3210	HEXA-DECIMAL NOTATION	CONTROL COMMANDS
-	0000	0	NO OPERATION
WRT	0001	1	WRITE ONE BLOCK
WTM	0010	2	WRITE TAPE MARK
ERA	0011	3	ERASE
RDL	0100	4	READ ONE BLOCK (L)
RDH	0101	5	READ ONE BLOCK (H)
SKP	0110	6	SKIP ONE BLOCK
REV	0111	7	REVERSE ONE BLOCK
SLP	1000	8	SET LOAD POINT
SLE	1001	9	SET LOAD POINT WITH ERASE
REW	1010	A	REWIND START
-	1011	B	NO OPERATION
STM	1100	C	SEARCH TAPE MARK
HSS	1101	D	HIGH SPEED SEARCH
-	1110	E	NO OPERATION
-	1111	F	NO OPERATION

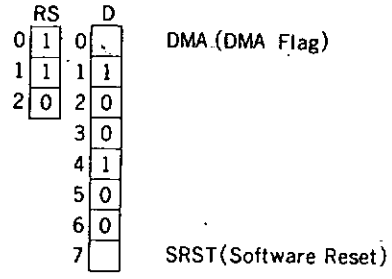
Note: When the command No.0, 12, 15, or 16(No operation) is supplied, MTU performs no operation and waits for the next control commands.

Table 2 Control Commands

2) IM0 ~ IM1
When these bits are written to "1", the contents of the register ISR(later explained) are inhibited to reflect to the IRQ signal. When IM0 is "1", no IRQ signal outputs even if DA and DBRE(flags in the ISR) are set. [Mask of DA, DBRE].
When IM1 is "1", no IRQ signal outputs if CCE(flag in the ISR) is set.[Mask of CCE].

3.1.4. MDR0(MODE REGISTER 0)

Input, R3



Once the register is written, the contents is maintained except for the SRST bit. Rewriting is required for changing the designation.
With the input of RST signal, or writing "1" to the SRST (MDR0, b7), the register is reset and all the bits are cleared to "0".

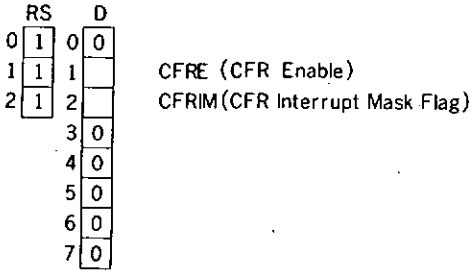
1)DMA(DMA flag)
If this flag is set to "1", DMA transfers are enabled.

2)SRST(SOFTWARE RESET)
If a "1" is transferred to this bit, all the registers in the MTC are cleared and return to the initial condition. This bit has an equivalent function as RST signal. Since the contents of the bit is not maintained, it is not required to write "0" to reset this bit.

Note: You cannot set the SRST bit and the DMA bit at the same time. Accordingly, it is required to write "0" to SRST to reset this register after the power-on, input of the RST signal, or setting the SRST bit to "1". Maximum 8μsec of time is required from the "1" setting to this bit to the completion of resetting. Remember that reading from and writing to the other registers are not enabled during this software reset period.

3.1.5. MDR1(MODE REGISTER 1)

Input, R7



1)CFRE(CFR ENABLE)
If this flag is set to "1", CFR flag in the register is set when the MTU becomes free or the MTU is free. The contents of this flag is reset and returns to "0" when the CFR is set. The condition of MTU free means that no control command is given to the MTU or that the tape completely stops after completing the given control command.

2)CFRIM(CFR INTERRUPT MASK FLAG)
This flag is effective only for the state that CFRE (b1)="1".
If this flag is reset to "0", IRQ signal outputs when CFR="1".

3.1.6. CSR(CASSETTE STATUS REGISTER) Output, R4

RS		D	
0	0	0	EOT (End of Tape)
1	0	1	TM (Tape Mark Detect)
2	1	2	FPT (File Protect)
		3	CSD (Cassette Side)
		4	NRDY (Not Ready)
		5	0
		6	0
		7	ERR (Error Status)

1)EOT(END OF TAPE)

The inserted cassette tape is divided into three states from the areas on the tape as shown in the Fig.8. These states are controlled in the MTC. The state changes when the conditions described in the figure are satisfied. The "C" state in the figure is called EOT state and the EOT flag is set to "1" in the state.

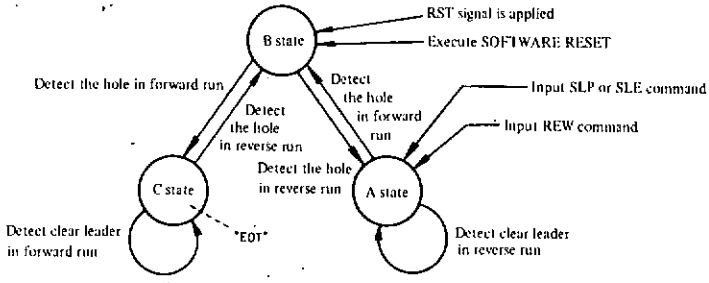


Fig. 8 EOT flag

2)TM(TAPE MARK DETECT)

The flag is set when one of the following conditions is satisfied.

i)WTM command is executed.
ii)Tape mark is detected by RDL or by RDH command.
iii)Tape mark is detected by SKP command.
iv)Tape mark is detected by STM command.

TM flag is reset at the trailing edge of ECLK signal when the contents of register CSR is read out. The flag is also reset by RST signal or by SRST signal.

3)FPT(FILE PROTECT)

The "1" state of this flag indicates that the inserted cassette tape is not in recordable condition. The status is effective when NRDY(CSR, b4) is "0".

4)CSD(CASSETTE SIDE)

This is the status to indicate which side of the inserted cassette is up. "0" indicates that the cassette is inserted with A side up and "1" with B side up. This status is effective when NRDY(CSR, b4) is "0".

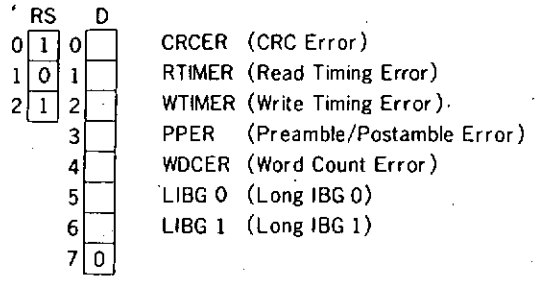
5)NRDY(NOT READY)

The status becomes "0" when the CMT is ready for operation. The MTU can execute the control command immediately. The READY condition means that more than 0.4~1.5sec has passed since the power supplies were turned on and the cassette tape was inserted.

6)ERR(ERROR STATUS)

The inclusive-OR of all the status in the register ESR is indicated on this flag. Only one "1" in the contents of ESR makes ERR "1". The flag is reset when the contents of ESR is read out.

3.1.7. ESR(ERROR STATUS REGISTER) Output, R5



If an error or errors are detected during the execution of a control command the causes of errors are indicated in this register. When the contents of this register is read by the CPU, they are reset to "0". It is also reset by RST signal and SRST signal. Note that ERR(CSR, b7) also becomes "0" at the same time when this register is cleared.

1)CRCER(CRC ERROR)

The CRC checking is performed only during the execution of WRT, RDL, or RDH command. At the execution of WRT command, it is checked whether the CRC code is correctly produced and if an error is detected, the flag is set to "1". At the execution of RDL or RDH command, the CRC code of the read data from the CMT is checked and if an error is detected, the flag is set to "1".

2)RTIMER(READ TIMING ERROR)

Read timing is checked only during the execution of RDL or RDH command. If the service from the CPU for the data transfer request of the MTC(DA flag) is delayed and a next data transfer request(DA flag) occurs before the CPU reads out the contents of the register DBR, this flag is set to "1". Even if an error occurs in a data block, the MTC continues the data transfer request(DA="1") for each byte until the block end is detected.

3)WTIMER(WRITE TIMING ERROR)

Write timing is checked only during the execution of WRT command. If the service from the CPU for the data transfer request(DBRE flag) is delayed and a next data transfer request (DBRE flag) occures befofe the CPU transfers the data to register DBR, this flag is set to "1". Even if the write timing error occurs, the MTC continues to supply data transfer requests(DBRE="1") until the contents of register WDC becomes "0".

4)PPER(PREAMBLE/POSTAMBLE ERROR)

Preamble and postamble are checked only during the execution of WRT, RDL, or RDH command.

At the execution of WRT command, it is checked whether the preamble and the postamble are correctly added and if an error is detected, the flag is set to "1".

At the execution of RDL or RDH command, the preamble and postamble patterns of the read data from the CMT are checked. If an error is detected, the flag is set to "1".

5)WDCER(WORD COUNT ERROR)

Word count error is checked only during the execution of RDL, or RDH command. The MTC compares the number of data from the cassette tape(excluding preamble, postamble and CRC) with the number previously written in the register WDC before the input of RDL or RDH command and if both numbers do not match, the flag is set to "1".

If the number of data actually read is greater than the number written in WDC, data transfer requests equal to the number written in the WDC are supplied to the CPU and the residual data are ignored.

6)LIBGO(LONG IBG 0)

This check is performed during the execution of HSS command. If an IBG longer than 17.0 ~ 22.2 inch(431.8 ~ 563.9mm) is detected during the execution of HSS command, this flag is set to "1" to complete the command.

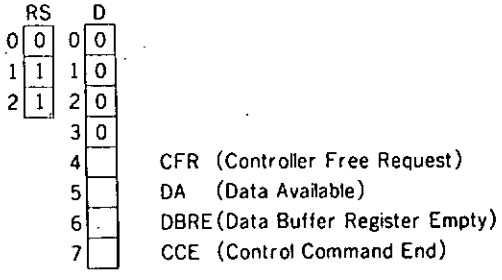
7)LIBG1(LONG IBG 1)

This check is performed during the execution of WRT, WTM, RDL, RDH, SKP, REV, SLP, SLE, or STM command.

Except for SLP and SLE commands, if IBG longer than 15.0 ~ 18.9 inch(381.0 ~ 480.1mm) is detected during the execution of one of the above commands, the flag is set to "1" to complete the command.

For SLP and SLE commands, the flag is set to "1" to complete the command if the BOT hole is not detected after specified length of tape run.

3.1.8. ISR(INTERRUPT STATUS REGISTER) Output, R6



If a request to the CPU's service occurs in the MTC, a flag in the register is set. When the CPU reads out the contents of the register, it is cleared. It is also cleared by RST signal or SRST.

1)CFR(CONTROLLER FREE REQUEST)

When the CFRE(MDR1, b1) is set to "0", this flag is always "0". If CFRE is "1", the flag is set when the MTC becomes free. If CFRIM(MDR1, b2) is also "0" at this time, IRQ signal outputs during "1" state of this flag.

2)DA(DATA AVAILABLE)

This flag is effective only during the execution of RDL or RDH command. The MTC sets this flag to "1" to request the service from the CPU for each writing of read data in the cassette tape to the register DBR. If IMO(CDR, b6) is "0", IRQ signal outputs during "1" state of this flag.

3)DBRE(DATA BUFFER REGISTER EMPTY)

This flag is effective only during the execution of WRT command.

If the register DBR becomes ready for next data writing, the MTC sets this flag to "1" and requests the data transfer to the CPU. If IMO(CDR, b6) is "0", IRQ signal outputs during "1" state of this flag.

4)CCE(CONTROL COMMAND END)

This flag is set when all of the basic operation of each control command is completed and the MTC is ready for receiving the next control command. This flag is set in the above condition once for every control command. If IM1(CDR, b7) is "0" at this time, IRQ signal outputs as long as this flag is set.
When this flag is set, the cassette tape still continues its running, even though the contents of the register ESR for the command has been already determined. When the next command is successively given, the MTU executed the next command without stopping the tape (ON THE FLY operation) as long as the previous command and the new command are both slow mode in the same direction or the new command is only to change the tape speed from slow mode to fast mode. If they are not in the same direction, the next command is executed after a stop of the tape.

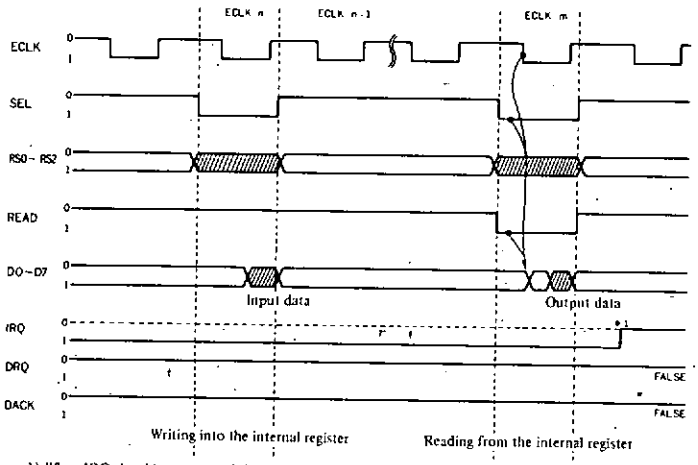
4. CONTROL

4.1. DATA TRANSFERS

Data transfers between the CPU and the registers, and DMA data transfers are explained in this section. Enough consideration is required not to set SEL signal and the DACK signal to "1" at the same time in any case.

4.1.1. Data transfers between the CPU and the Registers

Fig.9 shows the timing chart for the data transfers. The timing chart shows the two direction of transfers, writing into the internal registers and reading from the internal registers.



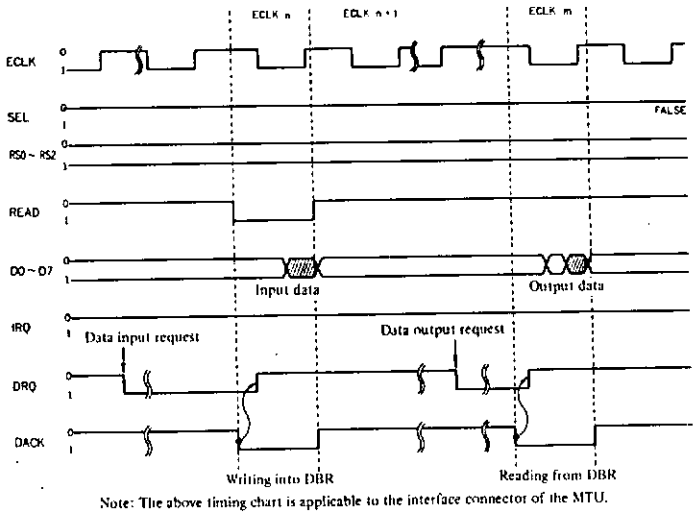
Notes: 1) When IRQ signal is output and the internal register ISR is read by the ECLKm, the IRQ signal returns to "0" with this timing.
2) The above timing chart is applicable to the interface connector of the MTU.

Fig. 9 Timing chart for data transfers between CPU and internal registers

1)Writing data into the internal registers
a)Input the SEL signal and RS0 ~ RS2 signals synchronizing with the ECLK signal(ECLK m)
b)During the input of above signals, keep the READ signal at HIGH level.
c)MTC samples the data on the D0 ~ D7 lines at the trailing edge of the ECLK signal(ECLK n) and writes the data into the registers selected by the RS0 ~ RS7 signals at the leading edge of the next ECLK signal(ECLK n+1).
d)Fot the input of the next ECLK signal(ECLK n+1), maintain the SEL and DACK signals at "0" state.

2)Reading data from the internal registers
a)Input the SEL signal and RS0 ~ RS2 signals synchronizing with the ECLK signal(ECLK m).
b)During the input of above signals, keep the READ signal at LOW level.
c)The output drivers of D0 ~ D7 lines are enabled as long as the ECLK signal(ECLK m) is active and the contents of the internal registers selected by the RS0 ~ RS2 signals are supplied to D0 ~ D7 lines. Except for this period, the output drivers keep high impedance state.

4.1.2. DMA Transfers
Fig.10 shows the timing chart for the data transfers at DMA mode. In the DMA transfers, DACK signal instead of SEL and RS0 ~ RS2 signals controls the data transfers to or from the internal register DBR.



Note: The above timing chart is applicable to the interface connector of the MTU.

Fig. 10 Timing chart for DMA transfers

1)Writing data into DBR
a)Input the DACK signal synchronizing with the ECLK signal (ECLK n). There are no restrictions for the RS0 ~ RS2 signals.
b)During the above operation, keep the READ signal at LOW level.
c)MTC samples the data on the D0 ~ D7 lines at the trailing edge of the ECLK signal(ECLK n)and writes the data into the internal register DBR at the leading edge of the next ECLK signal(ECLK n+1).
d)For the input of the next ECLK signal(ECLK n+1), maintain the

SEL and DACK signals at "0" state.

e)The DRQ signal returns to "0" state at the leading edge of the DACK signal.

2)Reading data from DBR

a)Input the DACK signal synchronizing with the ECLK signal. There are no restrictions for the RS0~RS2 signals.

b)During the above operation, keep the READ signal at HIGH level

c)The output drivers of D0~D7 lines are enabled as long as the ECLK signal(ECLK m) is active and the contents of the register DBR is supplied to the D0~D7 lines. Except for this period, the output drivers keep high impedance state.

d)The DRQ signal returns to "0" state at the leading edge of the DACK signal.

4.2. CONTROL METHOD

The CPU controls the MTU by supplying a series of control commands. This section explains the procedure required for the CPU to execute the control commands.

4.2.1. Control Procedure

1)Writing into the register MDR0

Once the register MDR0 is written, its contents are maintained unless one of the following operations from (a) through (c) is performed. In other word, if you write into this register in the initialized routine, you need not write for every control command.

a)Resetting the MTU by RST signal.

b)Resetting the MTU by SRST.

c)Rewriting to the register MDR0.

2)Check for the status of the cassette tape

Read out the contents of the register CSR to check the status of NRDY(b4), FPT(b2) and CSD(b3). Do not forget to check the status before you start operation at every insertion of a cassette. You may perform this checking every time before the input of each control command.

a)The case of NRDY="1".

The state indicates that no cassette is inserted into the MTU. Accordingly, both status of FPT and CSD are meaningless. Except for special cases, do not input a control command to the MTU when NRDY="1". If a control command is supplied when NRDY="1", the MTU accepts the command and waits for the READY condition of the CMT. The MTU starts operation immediately after a cassette is inserted and the CMT becomes READY. FPT and CSD cannot be checked previously when a control command is supplied at the NRDY="1".

b)The case of NRDY="0"

It indicates that a cassette is already inserted and the MTU is ready for operation. At this time, FPT and CSD show the status of the inserted cassette correctly.

i)FPT="1"

It indicates that the write enable plug is removed from the inserted cassette and the cassette is in unrecordable condition. Never supply write commands (WRT, WTM, ERA, SLE) when the cassette is in above condition. For the input of write commands, no data are written to the tape nor is the tape erased. However, the control command will not be executed correctly.

ii)CSD

It indicates which side(A or B) of the cassette is inserted up. CSD="0" indicates that the A side is up, while CSD="1" indicates B side up. Check CSD anytime you need to.

3)Writing into the WDC

For the execution of WRT, RDL, and RDH control commands, be sure to write the number of words to be transferred into the WDC. Since the contents of WDC is not maintained, write it every time before supplying the above control commands. You need not write WDC for the other commands. Even if you set WDC for one of the other commands, it has no influence on the execution of the command.

a)WRT command

Designate the number of data(in bytes) to be written into the cassette tape in positive bianry notation. Preamble, postamble and CRC are not included in the number.

b)RDL, RDH commands

Designate the number of data(in bytes) to be transferred to the CPU in positive binary notation. After the preamble is removed, data transfer requests occurs as much as designated by WDC.

4)Executing the control command

If IM0(b6) and IM1(b7) are set at the same time as writing into the register CDR, the MTU starts the execution of the control command immediately.

a)IM0

IM0 is effective when the command to be executed is one of WRT, RDL, and RDH. When IM0 is "0", IRQ signal outputs when DA(ISR, b5) or DBRE(ISR, b6) is set. When IM0 is "1", IRQ signal is inhibited.

b)IM1

IM1 is effective for every control command. When IM1 is "0", IRQ signal outputs when CCE(ISR, b7) is set. When IM1 is "1". IRQ signal is inhibited.

5)The data transfer control

Data can be transferred by one of WRT, RDL, and RDH commands. Detailed explanation for the data transfer control is in the item 4.2.2.(Data transfer control).

6)Detecting the end of control command

The MTU sets the CCE(ISR, b7) to "1" when the control command is completed. If IM1(CDR, b7)is "0" at the input of a control command, the CPU can detect it by an interrupt. If IM1(CDR, b7) is "1", IRQ signal is inhibited. Accordingly, it is required to read out the contents of the register ISR during the free time of the CPU to detect that the CCE="1".

Fundamentally, no other commands will be accepted during the execution of a command from its acceptance to its completion.

7)Checking the error status

When the completion of a control command is detected by CCE="1", then read out the register CSR and check the status of EOT(CSR, b0), TM(CSR, b1), and ERR(DSR, b7). When ERR="1", read out the register ESR for detailed examination of errors. The register ESR is reset when the contents are read out. If no error is detected proceed to the next process. Appropriate error treatment is required if an error is detected.

8)Writing into the register MDR1

When you use CFR, write into the register MDR1 after detecting CCE="1". If you set CFRE(MDR1, b1) to "1", CFR(ISR, b4) will be set when the tape stops completely. For usual applications, you need not use CFR. If you do not use CFR, you may give the next command after detecting CCE="1".

4.2.2. Data Transfer Control

The data transfers are performed by WRT, RDL, and RDH commands. There are the following three methods to transfer the data.

1)Polling

Previously reset the DMA flag(b0) of the register MDR0 to "0" and then set IM0(CDR, b6) to "1" at the same time as supplying a control command. By the above settings, the interrupt by DA(ISR, b5) or by DBRE(ISR, b6) is inhibited. Therefore, it is required that the CPU always check for the presence of a data transfer request by reading out the contents of the register ISR after the input of a control command.

When DA="1" is detected, the data shall be read out from the register DBR, and when DBRE="1", the data shall be written into the register DBR.

When the data transfers are performed by polling, CCE="1" shall also be detected by polling.

2)Interrupt

Previously reset the DMA flag(b0) of the register MDR0 to "0" and then reset IM0(CDR, b6) to "0" at the same time as supplying a control command. If these flags are in the above condition, IRQ signal outputs when a data transfer request occurs. The CPU reads out the register ISR in the interrupt service routine and reads out data from the register DBR when DA="1", and writes data to the register DBR when DBRE="1".

When the data transfers are performed by the interrupt, CCE="1" shall also be detected by the interrupt.

3)DMA

For the DMA transfers, an external DMA controller is required. Many types of constructions and control methods for DMA transfers will be disigned for each system you select. In this item basic function to be equipped to the DMA controller, operations of the MTU, and the workings of the CPU are explained. Following shows the steps for DMA transfers. Refer to the Fig.11.

a)Set DMA flag(MDR0, b0) to "1" for setting the register MDR0.

b)Write the initial address of the data area in the memory to the address register in the DMA controller.

c)Designate the data transfer direction in the R/W flag of the DMA controller. It is required that the data transfer direction of the next control command to the MTU matches that of the transfer direction of the R/W flag.

d)Designate the number of data transfers to the register WDC in the MTU.

e)Write the control command code to the register CDR in the MTU. Be sure to reset IM1 to "0" and detect the end of the control command by an interrupt.

f)When a data transfer request occurs in the MTU, the MTU outputs DRQ signal for DMA controller.

g)Receiving the DRQ signal, DMA controller requests the DMA transfer to the CPU.

h)When permission for the MDA transfer is supplied from the CPU, DMA controller starts the DMA transfer control as determined

in the R/W flag of the DMA controller.

i) If a transfer from the memory to the register DBR in the MTU is designated by R/W flag, the contents of address register outputs to the address lines and the read-out data from the memory outputs to the data lines. Synchronizing with the above operation, the DMA controller supplies DACK signal to the MTU to store the data on the data lines to the register DBR.

j) For a transfer from the regisger DBR to the memory, the operations in reverse direction of the above step (i) shall be performed.

k) The data transfer for one byte will be completed by either (i) or (j) items. The DMA controller informs the CPU of the completion of the transfer and increments the number of the address register and then waits for the next DRQ signal.

l) Repeat the steps from (g) to (k) as many times as determined by WDC. When all the steps are repeated as many times as required, no DRQ signal outputs from the MTU.

m) The CPU detects the end of the control command by the interrupt of CCE(ISR, b7).

n) Start the operation from item (b) for the next DMA transfer.

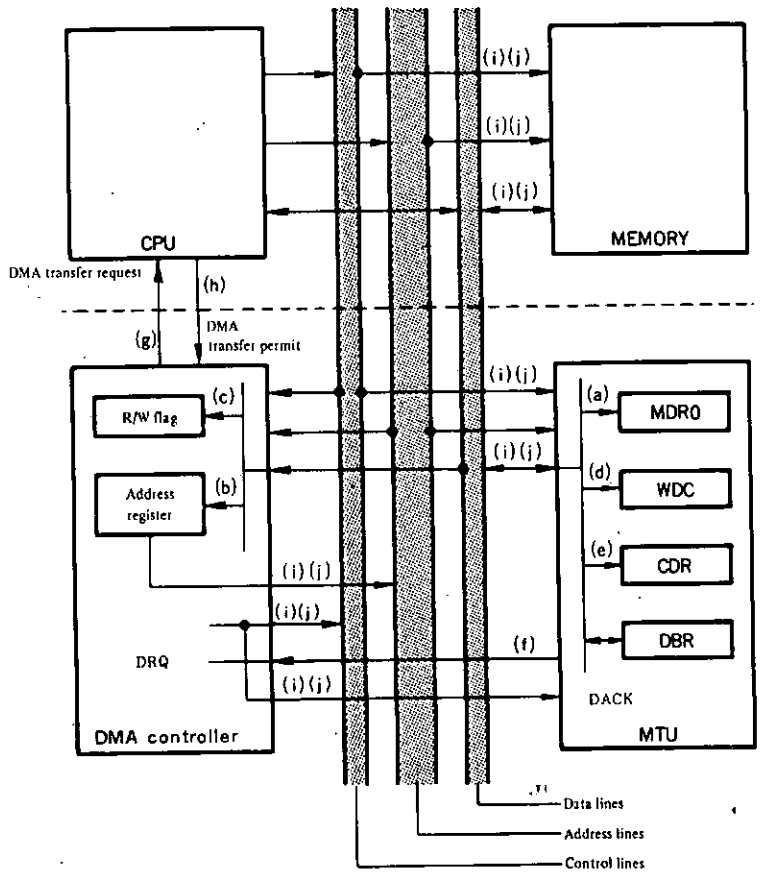


Fig. 11 Diagram for DMA data transfer

5. OPERATION

5.1. WRITE OPERATION

Write operation shall be performed according to the following steps. Also enough cares shall be payed to the precautions.

5.1.1. Write Operation Procedure

1)Turn on the D.C. power supply.

2)Insert a cassette tape.

3)Confirm the cassette status

The CMT will be ready(NRDY="0") within 0.4 ~ 1.5sec after the insertion of a cassette. Confirm that NRDY="0" and check for FPT(CSR, b2) and then check for CSD(CSR, b3). When NRDY="1", never execute a write operation.

4)Execution of REW command

Input a REW command to the MTU. If the command is given at the BOT side clear leader end, 2sec, approx. is required to enable the execution of the next command even if the CCE(ISR, b7) immediately indicates "1". However, you may input the next command immediately after the CCE becomes "1".

5)Execution of SLE command

After confirming the start of the REW command(CCE="1"), input a SLE command. Never input a SLP command by an operation error. An input of a SLP command not only erases the tape but also disturbs the insertion of initial gap.

6)Starting the write operation

Start the write operation when the end of SLE command (CCE="1") is detected. The specified initial gap will be inserted even if a WRT command is supplied immediately after the completion of the SLE command.

7)End of the write operation

At the end of the write operation, execute the after treatment for write operation. Refer to the item 5.4. explained later. Then successively execute a REW command to rewind the tape to the BOT side clear leader end and eject the cassette.

8)Detection of EOT

When the EOT hole is detected, do not write data blocks beyond the hole as a basic rule and perform the after treatment. Successively, execute a REW command to rewind the tape to the BOT side clear leader end. Then remove the cassette and start the next operation from the step 2).

5.1.2. Precautions

1)Never remove the cassette from the MTU during operation. Such removal might cause the tape to slip past the stopped point which might leave an unerased portion of the tape or shorten the IBG length at the next insertion for writing.

2)When the operation is finished, be sure to remove the cassette after rewinding the tape. If it is not done, the magnetic coated area of the tape might be damaged during the transportation or dust might be brought to the coated surface which will cause the errors.

3)When it is necessary to remove the cassette during operation, put a mark on the tape where the operation is stopped.(Usually a tape mark is wtitten there). Then rewind the tape to the BOT side clear leader to remove it. For starting the operation again, search the mark to continue the operation from that point.

4)When the power has been turned on already, the cassette may be inserted after the input of a REW command. The procedure of write operation for this case is 1), 4), 2), 3).

5.2. READ OPERATION

Read operation of a cassette tape shall be performed according to the following procedure:

5.2.1. Read Operation Procedure

1)Turn on the D.C. power supply.

2)Insert a cassette tape.

3)Confirm the cassette status
The CMT will be ready(NRDY="0") within 0.4 ~ 1.5sec after the insertion of a cassette. Confirm that NRDY(CSR, b4)="0" and check for FPT(ISR, b2) and CSD(CSR, b3) if required.

4)Execution of REW command
Input a REW command to the MTU. If the command is given at the BOT side clear leader end , 2sec, approx. is required to enable the execution of the next command even if the CCE(ISR, b7) immediately indicates "1". However, you may input the next command immediately after the CCE becomes "1".

5)Execution of SLP command
After confirming the start of the REW command(CCE="1"), input a SLP command. Never input a SLE command by an operation error.

6)Starting the read operation
Start the read operation when the end of SLP command(CCE="1") is detected. If the initial gap is longer than 33mm, read operation will be started from the first block.

7)End of the read operation
When the read operation is completed, execute a REW command to rewind the tape to the BOT side clear leader end. And then remove the cassette tape from the MTU.

5.2.2. Precautions

1)Never remove the cassette from the MTU during operation, even if the tape stops moving. Such removal might cause tape to slip past the stopped point and the data will not be read out correctly when a block reading(RDL command) is executed.

2)When the operation is finished, be sure to rewind the tape to remove it from the MTU. It is not done, magnetic coated area of the tape might be damaged during transportation or dust might be brought to the coated surface which will cause errors.

3)When the power has been turned on already, the cassette may be inserted after the input of a REW command. The procedure of read operation for this case is 1), 4), 2), and 3).

5.3. ERROR CHECKING IN WRITE OPERATION

Since a single gap head is equipped to the MTU, a read after write check cannot be performed during the execution of a WRT command. If it is possible in your application to have an extra time for checking and if enough reliability is required for the written data on the tape, perform the write back space read check. However, if enough care is payed to the handling and storage of tapes, the special error checking is not always necessary for data writing. Enough consideration to your system design and especially in programming is required to solve the permanent errors in data reading even if the write back space read check is performed. The consideration is of course necessary when the error checking is not performed for data writing.

5.3.1. Write Back Space Read Check

After executing a WRT command, reverse the tape to the beginning of the written block by a REV command and read the block for checking by an RDH command. The one block write operation consists of the combination of these three commands and is called a write back space read check.

1)Contents of error to be checked

a)CRCER(ESR, b3)

Check CRCER after executing an RDH command.

b)PPER(ESR, b3)

Check PPER after executing an RDL command.

c)WDCER(ESR, b4)

Confirm that the WDCER(ESR, b4) is "0" after the execution of an RDH command by making the WDC value for RDH equal to that for WRT command.

d)Data compare

This need not be performed if not required.
Save the written data by a WRT command in the buffer memory. When the block is read by an RDH command, compare the data read from the cassette tape with those saved in the buffer memory and confirm that they match each other.

e)WTIMER(ESR, b2)

This checking is only performed after the execution of a WRT command. When this flag indicates "1", write the data again after the execution of a REV command.

f)RTIMER(ESR, b1)

This may be ignored if you do not use the data compare in item (d).

2)IBG length

The IBG length to be inserted depends on the types of your operation whether you select a stop of the tape after an RDH command execution for the next block writing or you select a continuous tape run(ON THE FLY operation).

a)With Start/Stop operation

0.73 inch(18.54mm) ~ 1.14 inch(28.96mm)

b)ON THE FLY operation

0.76 inch(19.30mm) ~ 0.84 inch(21.34mm)

3)Number of blocks which can be recorded in one side of a cassette (Tape length: 86m nominal)

a)For 256 bytes in one block

With start/stop operations: 878 ~ 1087 blocks
ON THE FLY operation: 953 ~ 1077 blocks

b)For 128 bytes in one block
With start/stop operations: 1341 ~ 1757 blocks
ON THE FLY operation: 1524 ~ 1731 blocks

4)Treatment required when an error is detected
When an error is detected by the write back space read check, it is required to write the data again. Fig.12 shows an example for rewriting the data. If the error still occurs at W34 in the figure, regard it as a defective area on the tape. If the data are written correctly before the W34 point, the IBG length will not exceeed 9.84 inch(250mm).

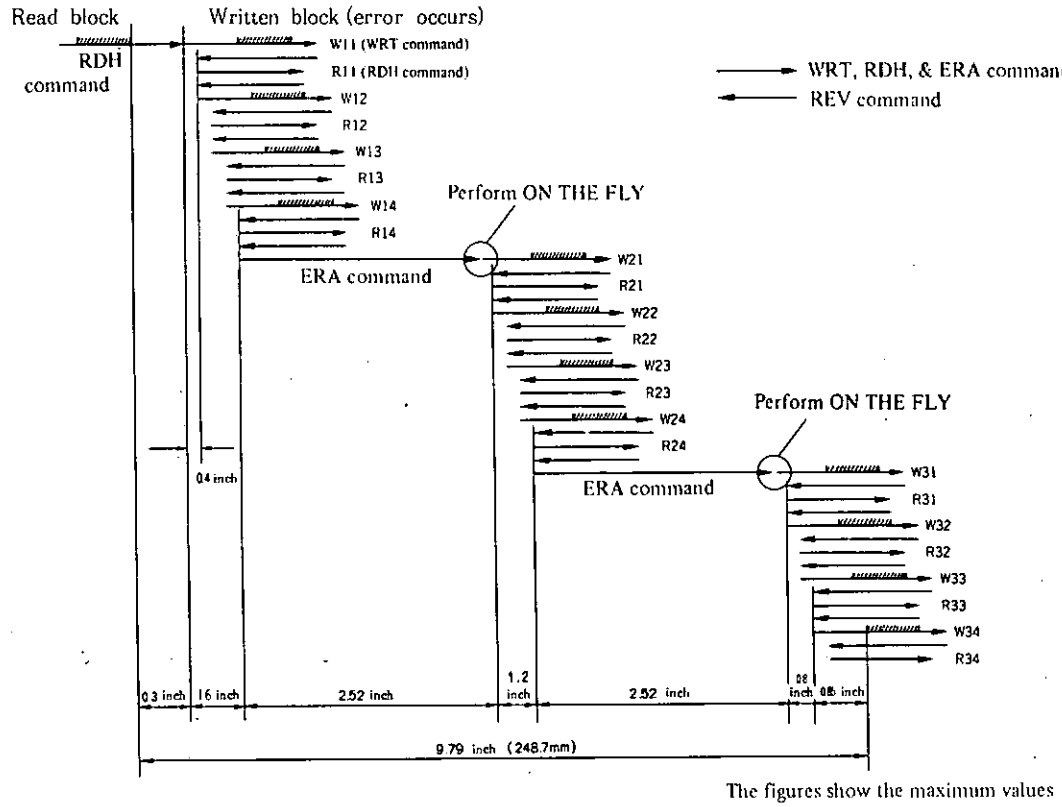


Fig. 12 IBG length after rewriting

5)Other precautions
Confirm that the TM flag(CSR, b1) is "1" by an RDH command when a tape mark is written by a WTM command.

5.3.2. Operation without the Write Back Space Read Check
Write blocks of data by repeating the WRT command.

1)Error checking
After the execution of a WRT command, confirm that the ERR(CSR, b7) flag indicates "0". When it is "1", execute a REV command to reverse the tape to the beginning of the block and execute a rewriting.

2)IBG length
a)With start/stop operation
0.79 inch(20.1mm) ~ 1.21 inch(30.73mm)

b)ON THE FLY operation
0.82 inch(20.8mm)~0.90 inch(22.86mm)

3)Number of blocks which can be recorded in one side of a casstte.
(Tape length: 86m nominal)
a)For 256 bytes in one block
With start/stop operations: 862~1067 blocks
ON THE FLY operation: 937~1057 blocks
b)For 128 bytes in one block
With start/stop operations: 1304~1706 blocks
ON THE FLY operation: 1484~1681 blocks

4)Other precautions
ERR(CSR, b7) will never be "1" by a WTM command except for the circuit troubles in the MTU.

5.4. AFTER TREATMENT FOR THE WRITE OPERATION

It is required to indicate on the tape that the write operation is completed and that no more data are written on the tape. Several methods are shown in the following. You may select the most appropriate method for your programming.

(i)Erase the tape for more than 500mm approx.
(ii)Write tape marks
(iii)Indicate that the block is the last one by the contents of the data block.

In most applications, some of the above methods are used in combination. In various standards, it is specified that the tape after the last block shall be erased for more than 17.8 mm(0.70 inch). Accordingly, it is recommended to execute at least one ERA command at the end.

5.4.1. Erasing the Tape for more than 500mm approx

Be sure to perform this treatment also even if you use either (ii) or (iii) method to show the data end. This method will satisfy the restriction in the various standards and it also assures the treatment of (ii) or (iii). Twelve repetitive executions of ERA commands will erase the tape for more than 23.15 inch(588.0mm). Regard that no data are written any more if LIBG1(ESR, b6) is "1" and it is detected in the read operation.

5.4.2. Writing Tape Marks

1)Taking the worst case into consideration taht the tape mark cannot be detected because of the errors in read operation, write several tape marks(commonly two marks).
2)When you use an HSS command in read operation, execute an ERA command after writing the first tape mark to insert the long IBG between the tape marks.
3)When the data on the cassette tape are divided into several files, the tape mark may be used as punctuation marks for each file. Take the items (i) and (ii) into consideration. In this case, data end shall be indicated by the method of item (i) or by two successive tape marks.

5.4.3. Indicating the Data End by the Contents of the Data Block

For some types of data, this method is not applicable. In such event, use the method of either (i) or (ii). It is recommended to use (i) or (ii) method with this method.

5.5. EXPLANATION OF THE CFR

The CFR(ISR, b4) is used for the CPU to detect that the cassette tape completely stops after executing a control command. For usual applications, the CFR is not always used to confirm the command end, since the next command may be given immediately after detecting CCE(ISR, b7)="1".

5.5.1. How to Use the CRR

Use the CFR according to the following steps.

1)Detect the control command end by CCE="1".
2)Set the CFRE(MDR1, b1) to "1". The CFRIM(MDR1, b2) shall be also set at the same time.
3)When the cassette tape completely stops, the CFR(ISR, b4) becomes "1". When the CFRIM is "0", at that time, the IRQ signal outputs.
4)When the CFR(ISR, b4) is set, the CFRE(MDR1, b1) is reset and becomes ineffective.

5.5.2. Precautions

1)Never write the MDR1 when you do not use the CFR.
2)If you set the CFRE(MDR1, b1) before the input of a control command(when the MTU is waiting for a control command), the CFR(ISR, b4) immediately becomes "1".

5.5.3. Examples for CFR Application

1)For the REW command

When a REW command is given to the MTU, the CCE(ISR, b7) becomes "1" as soon as the execution of the REW command starts. When you want to execute the next control command successively after the completion of the rewinding, you may input the next command after detecting CCE="1". However, when you want to remove the cassette tape after rewinding, you have to detect the end of rewinding by CFR.

2)The CFR is also used to stop the tape before each command.

5.6. POWER ON AND POWER OFF OF THE POWER SUPPLY

The MTU is equipped with a protection circuit to protect the function errors(such as tape shifting, recording of noises, and data erasing) at power-on and power-off. There is no restrictions for the order of power-on/-off nor for rise/fall times of +5V and +12V supplies. However, following precautions shall be referred to:

1)Maintain the RST signal at LOW level until the voltage reaches the stable condition after +5V power-on.
2)Make the RST signal to LOW level at or before the fall of the voltage after +5V power-off.

5.7. POWER SUPPLIES FOR MT-2

Since the MT-2 adopts the reel motor driving system, no components nor parts move even at the power-on condition unless the magnetic tape moves at that time.

1)+12V power line is supplied to reel motor driving circuit, read amplifier, and write amplifier.
2)+5V power line is supplied to the lamp and other electrical circuits.

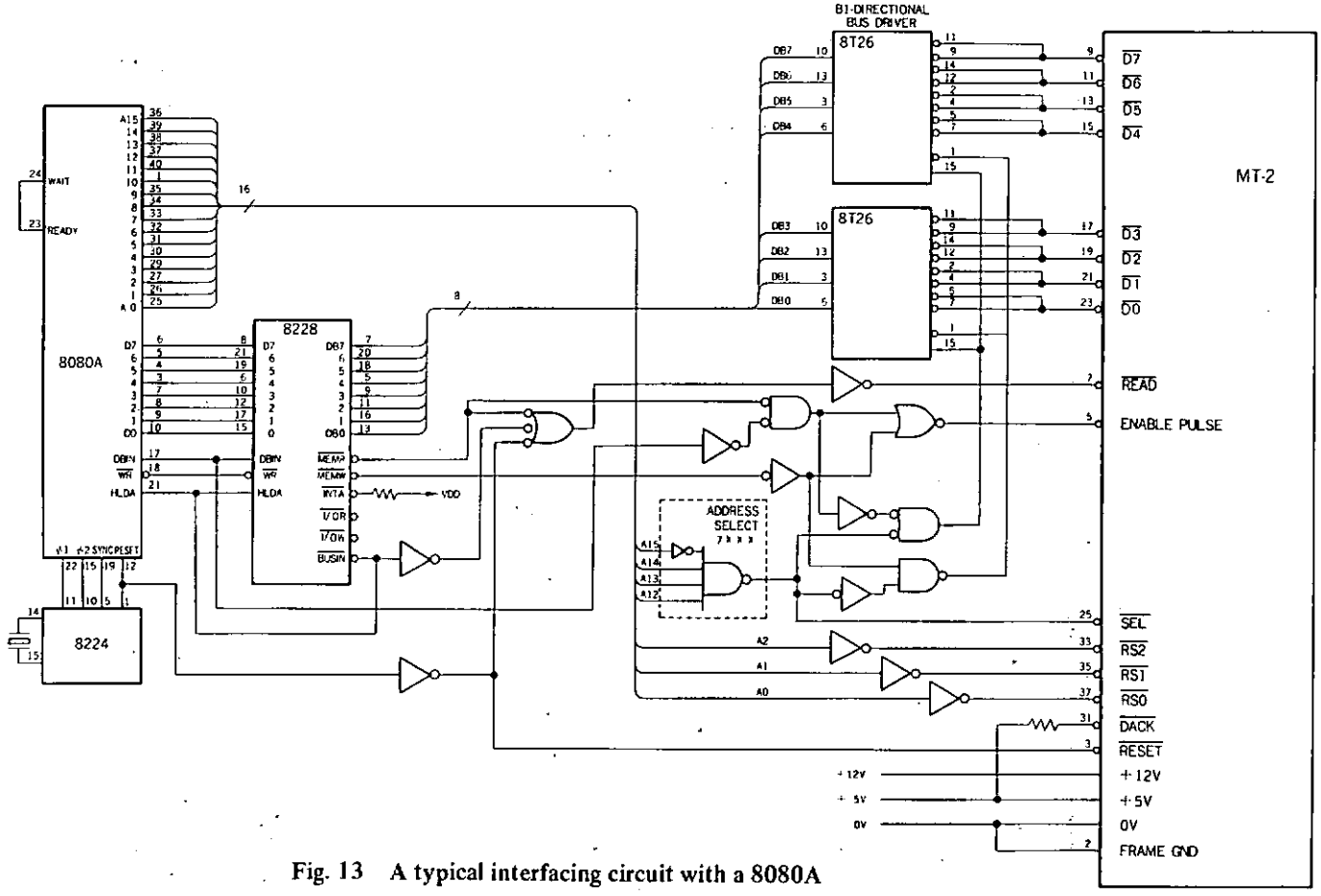


Fig. 13 A typical interfacing circuit with a 8080A

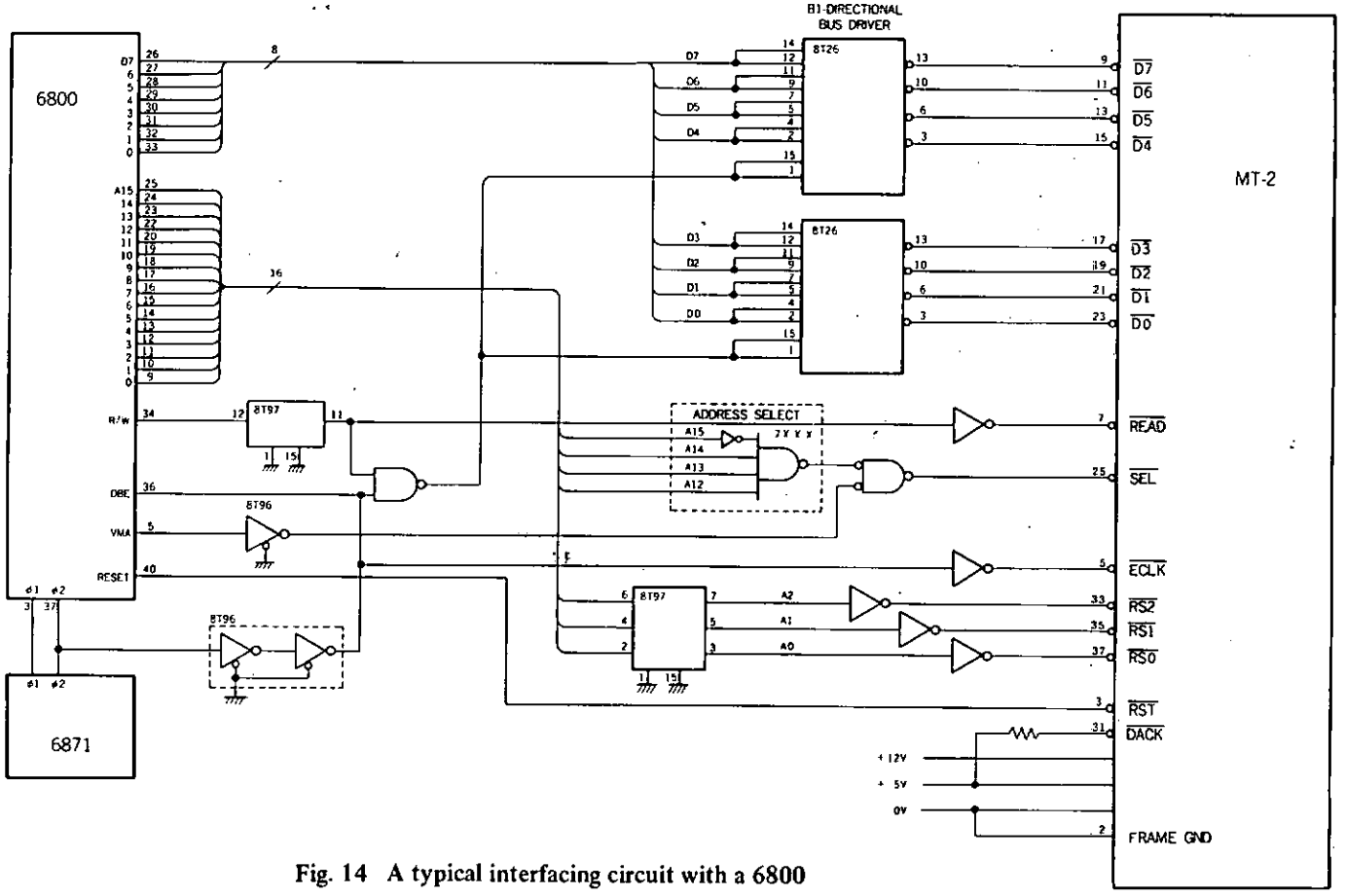


Fig. 14 A typical interfacing circuit with a 6800

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DATAPACK
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TEAC MT-2

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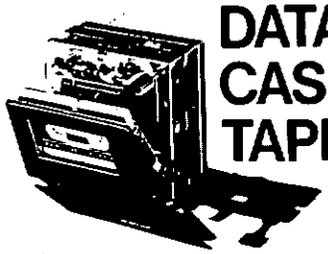

DATAPACK CASSETTE DIGITAL MAGNETIC TAPE MEMORY SYSTEM MT-2

MT-2 Four Versions

Version	Single (Read/Write) Gap Head	Dual Gap Head	Interface Controller
MT-2-01	YES	NO	NO
MT-2-02	YES	NO	YES
MT-2-03	NO	YES	NO
MT-2-04	NO	YES	YES

MT-2 Specifications

Magnetic Tape	ISO-3407
Data Format	800 bpi, Phase Encoding
External Construction	
Height	105 ± 1 mm
Width	120 ± 1 mm
Depth	79 mm (01, 03), 91 mm (02, 04)
Weight	1 kg max. (01, 03), 1.2 kg max. (02, 04)
Installation	Installation at any angle is applicable
Mechanical Construction	
Tape Drive System	D.C. Motor Direct Reel Drive System
Tape Speed Detection	Encoder Detection
Cassette Insertion	Pocket Holder Type
Cassette Eject	Manual by Eject Button
Cassette Load Detector	Micro-Switch
Cassette Side Detector	Micro-Switch
Write Enable Plug Detector	Photoelectric Detector
BOT/EOT Detector	Photoelectric Detector
Magnetic Head	Single Track
Power Requirements	
Voltage & Current	D.C. + 12 V ± 5%, 1.8 A max., 1.0 A nom. & D.C. + 5 V ± 5%, 0.4 A max., 0.35 A nom. (01, 03) or 0.75 A max., 0.7 A nom. (02, 04)
Ripple Voltage	Less than 100 mV p-p
Rise & Fall Time	Unstipulated
Frame Ground	D.C. 0V Separation
Environmental Conditions	
Ambient Temperature	Operating 5°C ~ 40°C Storage −15°C ~ 60°C
Ambient Relative Humidity	Operating 20 ~ 80% Storage 10 ~ 90%
Vibration Operating	Less than 0.5 G (Less than 120 Hz, continuous)
Vibration Non-Operating (Packaged Condition)	Impact : Less than 40 G Continuous : Less than 3 G
Tape Drive Characteristics (01, 03)	
Tape Speed	15 ips ± 3% for Read/Write, 45 ips ± 4% for Rewind/High Speed Search
ISV	Less than ± 5%
Start Distance	0.4" ± 0.1" (15 ips) Less than 2.4" (45 ips)
Stop Distance	0.11" ± 0.08" (15 ips) Less than 1.8" (45 ips)
Start Time	Less than 40 ms
Stop Time	Less than 40 ms (15 ips) Less than 80 ms (45 ips)
Tape Drive Characteristics (02, 04)	
Tape Speed	15 ips ± 3% & 45 ips ± 4%
IBG Length inserted	0.97" ± 0.24" (02) 1.12" ± 0.25" (04)
Erased Length	2.19" ± 0.27"
Initial Gap	2.26" ± 0.40" (02) 2.34" ± 0.40" (04)
Readable IBG Length	0.7" or more
Long IBG Detection Length	15.0" ~ 22.2"
Data Handling Characteristics (Head & Read/Write Circuit)	
Data Transfer Rate	12 kbit/sec.
Resolution	70% or more
Self Erasure	Less than 15%
Erase Efficiency	More than 97%
Feedthrough	Less than 7.5% (03, 04)
Threshold Level	LOW (Read) 18 ± 3% HIGH (Write) 40 ± 5%
MTBF	10,000 hrs. or more (10% Rate of Operation)
I/O Interface	
Input/Output Circuit	TTL Compatible
Interface Connector	No. 3431-2002 by 3M Co. Ltd. or equivalent (01, 03) No. 3433-1002 by 3M Co. Ltd. or equivalent (02, 04)
Command & Status (02, 04)	
Command	Write One Block Write Tape Mark Erase Read One Block (L) Read One Block (H) Skip One Block Reverse One Block Set Load Point Set Load Point With Erase Rewind Start Search Tape Mark High Speed Search
Cassette Status	End of Tape Tape Mark Detect File Protect Cassette Side Not Ready Error Status
Error Status	CRC Error Read Timing Error Write Timing Error Preamble/Postamble Error Word Count Error Long IBG 0 Long IBG 1
LSI Internal Registers (02, 04)	Data Buffer Register Word Counter Command Register Mode Register 0 Cassette Status Register Error Status Register Interrupt Status Register Mode Register 1

Table of Interface Connector Pins MT-2 (02,04)

Signal Designation	Connector Pin Number	Signal Direction
RESET	3	MT-2 ← CPU
ENABLE CLOCK	5	←
READ	7	←
DATA 7	9	↔
DATA 6	11	↔
DATA 5	13	↔
DATA 4	15	↔
DATA 3	17	↔
DATA 2	19	↔
DATA 1	21	↔
DATA 0	23	↔
SELECT	25	←
INTERRUPT REQUEST	27	→
DMA REQUEST	29	→
DMA ACKNOWLEDGE	31	←
REGISTER SELECT 2	33	←
REGISTER SELECT 1	35	←
REGISTER SELECT 0	37	←
+12V	46, 47, 48, 49	←
+5V	43, 44, 45	←
OV	39, 40, 41, 42, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38	↔
FRAME GROUND	2	↔
NO CONNECTION	1	
POLARIZING KEY	50	

Table of Input/Output Signals & Terminal MT-2 (01,03)

Signal Designation	Connector Pin Number	Signal Direction	Waveform
POLARIZING KEY	1	MT-2 → MTC	
FILE PROTECT	9	→	FILE PROTECT
RUN	11	→	RUN
READY	13	→	READY
BOT/EOT	15	→	BOT/EOT
READ DATA A	17	→	
READ DATA B	19	→	
HIGH THRESHOLD	21 (01 only)	←	HIGH THRESHOLD
WRITE PERMIT	23	←	WRITE PERMIT
WRITE DATA	25	←	IBG
SLOW/FAST	27	←	FAST
FORWARD/REVERSE	29	←	REVERSE
STOP/GO	31	←	GO
CASSETTE SIDE A	33	→	SIDE A
+12V	2, 3, 4, 5	←	
+5V	6, 7	←	
OV	8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32	↔	
FRAME GROUND	34	↔	

* Improvements may result in changes of features or specifications without notice.

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