3.0 HARDWARE DESCRIPTION

3.1 Hardware Description - CPU Module

3.1.1 Memory

The T99SS CPU Module is equipped to handle two different types of memory:

> EPROM (TMS2708/Intel 2708) - Two EPROM's, which provide 1024 words (2048 bytes) of program storage, are provided with the T99SS CPU Module. These EPROM's contain a powerful monitor to assist with program development. Two other EPROM's are wired in parallel to provide an optional 1024 words (2048 bytes) of program storage. The two EPROM's may also be programmed using the software provided in the monitor. This provides a convenient means for saving user programs in a read only memory.
>
> RAM (TMS4042) - Four 256x4 RAM's are provided with the T99SS CPU module which provides 256 words (512 bytes) of read/write memory. This memory can be expanded to 1024 words (2048 bytes) by adding twelve more 256x4 RAM's.

The unique address decoding logic allows maximum flexibility in address assignment. A four input NAND (U6-74LS40) detects any reference to the last 2K words of memory. This signal partially enables an OR (U13-74LS32) and a one-of-four decoder (U8-74156). Address bit A4 determines whether the OR or the decoder will be enabled. The jumpers determine which memory will be addressed when the OR or the decodeer is enabled. If these jumpers are installed as shown in the schematic, memory will be addressed as:

> F800-FFFF EPROM (Monitor)
> F000-F7FF EPROM

An OR gate (U7-74S260) detects any reference to the first 1K of memory. This signal enables a second one of four decoder which determines exactly which section of memory is addressed. If the jumpers are installed as shown in the schematic, memory is addressed as:

> 0000-01FF RAM-1 (Basic)
> 0200-03FF RAM-2 (Optional)
> 0400-05FF RAM-3 (Optional)
> 0600-07FF RAM-4 (Optional)

The T99SS CPU Module will ignore a reference to any address not shown above. The CPU will also ignore addresses 0000-07FF if the jumper /FIRST K is removed. This may be

useful if external RAM is added to the system. The jumpers also allow the memory to be reorganized to suit the needs of any particular application. This reorganizing is useful, but should be done carefully. Be certain that you do not enable two different memories with the same signal - this will damage the memory.

3.1.2 Input/Output

Two octal multiplexers (U3, U4-74LS251) and two addressable latches (U1, U2-74LS259) are used for CRU based I/O. The I/O bits are addressed as bits 0-F (hex). Additional I/O may be added to the system by adding appropriate I/O Modules (e.g. T99128).

One of the input bits (0) is used for RS-232/TTY input. If any application requires these bits, but does not require the services of the monitor, the jumper may be removed, which deactivates this input.

One of the output bits (0) is used for RS-232/TTY output and one bit (1) is used to control the on-board EPROM programmer. Like the inputs, these may be disabled by removing the associated jumppers.

3.1.3 Clock Generation

The SN74LS362 clock generator (U10) provides the four-phase MOS timing signals for the 9900. A single capacitor can be used to determine the clock frequency. This is adequate for most applications, but if a more precise frequency is required, a crystal reference can be used.

A simple LC network is used to control the frequency overtone. The SN74LS362 also provides TTL compatible clock outputs. The RC network on the Schmitt-triggered D input provides a power-on reset for the system in addition to the manual reset.

3.1.4 /RESET/, /LOAD, and /INTREQ

The /RESET, /LOAD, and /INTREQ 9900 inputs are used to alter the normal program execution sequence. The encoding logic (U11-74LS377, U25-74148) present the proper interrupt code to the IC0-IC3 lines on the processor. It also synchronizes the interrupt request.

The external load and reset signals are input to the CPU after being synchronized. /RESET is held active (low) for at least three clock cycles by the switch or the power-on RC network. /LOAD is held active (low) for one instruction

time as determined by the 9900 IAQ output.

The load signal is used to enter the monitor. If switch one is in the load position, a load request is generated following any restart. This transfers control to the monitor since the load vector is at ROM locations FFFC-FFFF. If switch one is not in the load position, restarts use the normal restart vector at 000-0003.

3.1.5 EPROM Programmer

A unique feature of the T99SS CPU Module is the on-board EPROM programmer for 2708/2704 Erasable Read-Only Memories. The programming is enabled/disabled by switch three. When disabled, all programming requests are ignored by the hardware. When the programmer is enabled, bit 1 of the CRU output controls the programming. Another important feature is that both the EPROM's are programmed at one time. It is not necessary to program the even bytes, then the odd ones as it is with a single EPROM programmer. Rather, a whole word is programmed at one time.

If programming is enabled (by switch three, and CRU I/O bit 1), then the processor can program any location by simply writing into it. When the write is detected (U12-74123), the address and data are held by placing the processor in wait and a program pulse is generated. After programming, the program mode can be reset to read in order to verify the EPROM's The EPROM must be programmed several times to insure data integrity. Do not continuously reprogram one location, as it may damage the EPROM. The recommended sequence is (R1,R2 preset to source and R3 to EPROM destination):

```
          INCT    R2          ; advance end
          LI      R4,255      ; R4= repeat
LOOP 1    MOV     R1,R5       ; R5= start
          MOV     R3,R6       ; R6= PROM start
          ORI     R6,>F000    ; adjust for PROM
LOOP2     MOV     *R5+,*R6+   ; Do one pass
          C       R5,R2
          JNE     LOOP 2
          DEC     R4          ; Do another pass
          JNE     LOOP 1
```