TEK-AT4

486 SINGLE BOARD COMPUTER
TECHNICAL REFERENCE MANUAL
VERSION 3.0, MARCH 1997

TEKNOR INDUSTRIAL COMPUTERS INC.
616 Curé Boivin
Boisbriand, Quebec
J7G 2A7 CANADA

ref: M703_3-0

If you require information not covered in this manual or in our Application Notes releases, contact our Technical Support department in Canada at (514) 437-5682 or in Germany at +49 811 / 600 15-0.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF DIAGRAMS

FOREWORD

The information in this document is provided for reference purposes only. TEKNOR does not assume any liability for application or use of the information or products described herein.

This document may contain or reference information and products protected by the copyrights or patents of others and does not convey any license under the patent right of TEKNOR, nor the rights of others.

This manual does not discuss standard features of the IBM family of Personal Computers. Instead, it focuses on the superset of features that TEKNOR has implemented into its single board computers.

For information on IBM standard features, please refer to the following books available at your local book stores:

- *IBM AT Technical Reference Manual*
- *DOS Technical Reference*
- *Peter Norton's Programming The IBM PC*

This is by no means an exhaustive list. Many titles exist on these subjects and just as many titles deal with specialized applications such as extended memory transfers, disk drives, ems, and so on.

INTRODUCTION SECTION 1

The TEK-AT4 is a high performance PC/AT type computer on a half-card format (7" x 4.7"). It integrates all the basic functions available on an IBM AT - like a hard disk interface and a floppy disk controller.

Best of all, the TEK-AT4 is designed to operate in environments where a sturdy and compact system is essential. So elements such as a watchdog timer, solid state disks, and a power failure detector were added to make the TEK-AT4 perform even in the most extreme industrial applications.

Built using CMOS technology, the TEK-AT4 consumes very little power. For example, the 33MHz TEK-AT4 typically consumes less than 7.5 watts. The TEK-AT4 is versatile, too. It can be installed in a PC passive backplane or, because of its small size, it can be used as a stand-alone controller by utilizing the four standard mounting holes and separate power connector.

And to top it off, an XT expansion header accommodates TEKNOR's series of display controllers or other optional expansion cards.

Here are more exciting features found on the TEK-AT4 single board computer:

- PC/AT bus or stand alone operation
- 486SX @ 25MHz 486DX @ 33MHz 486DX2 @ 66MHz 486DX4 overdrive @ 100MHz
- 1, 4, or 16MB of system memory with mixed DRAM support
- 1MB of user EPROM or Flash EPROM
- Up to 1MB user SRAM with battery backup
- Supports Shadow RAM BIOS for fast execution
- Flash EPROM boot
- Real-time clock with battery backup
- AT keyboard and speaker port
- One parallel printer port (LPT1)
- Two serial ports with COM2 as RS-232 or RS-485
- Watchdog Timer
- Power Fail Detector
- Low Battery Circuit Detector
- Onboard floppy controller: drives two floppies
- Onboard IDE hard disk interface
- Sleep Mode support
- CMOS technology for low power
- Two year warranty

UNPACKING

If the TEK-AT4 appears to be damaged, please notify TEKNOR immediately. Save the box and packing material in case you need to ship the card back in the future.

The TEK-AT4 package is comprised of the card itself, a keyboard cable, a 3.5" floppy disk containing the utilities, this technical reference manual, and a software utility manual. The TEK-AT4 is preconfigured at the factory to operate as a standard IBM AT processor card.

BASIC MODES OF OPERATION

The TEK-AT4 single board computer is an exceptionally versatile board that will function either on a passive backplane or as a stand-alone controller. In fact, it is a real performer in true industrial applications functioning without disks, keyboard and monitor.

Following is a brief description of the operating modes available on the TEK-AT4.

Passive Backplane

The TEK-AT4 can be used in a PC/AT Passive Backplane in conjunction with any PC/AT and XT compatible cards. Power is drawn directly from the PC Bus. Video cards may be used but are not a prerequisite for operation.

☞ **To avoid damage, make certain the power is off before inserting or retrieving a card from the passive backplane.**

User Interface

The TEK-AT4 operates with any PC Bus compatible display card. Or, if stand-alone mode is desired, a TEKNOR Mezzanine SVGA card may be used.

A VT100 terminal (or a PC emulating VT100) may be used as an inexpensive alternative to a display and keyboard. Refer to Section 5, *Using VT100 Mode* for more details on this procedure.

Stand-Alone Operation

An alternate power connector is available for supplying the necessary voltages to the TEK-AT4 board. This is useful in situations where a Passive Backplane system is not appropriate.

In fact, by utilizing a TEKNOR Mezzanine card, you can assemble a complete computer in a 7x4.7x1.25" area - without ever using a passive backplane system at all.

And when your applications calls for it, the TEK-AT4 is fully operational without any user interfaces at all - running without disks, keyboard, and video.

Diskless Operation

The TEK-AT4 can operate without mechanical drives in any basic mode of operation. A Flash disk can be configured as a bootable disk and temporary data may be securely stored on SRAM disks.

In essence, the TEK-AT4 is an ideal industrial controller withstanding shock, vibration, and temperature variations - all major concerns in industrial environments.

CONFIGURATION
SECTION 2

JUMPERS

The TEK-AT4 is designed to allow for minimal hardware configuration. The following is a list of the basic configuration jumpers available on the TEK-AT4.

Jumper	State[1]	Function
Power Detection Circuitry		
W1	*(1-2)**	*Power Failure Detector*
	(2-3)	*Low Battery Detection*
SRAM Battery Backup		
W2	*Open**	*No Batt*
	Closed	*Vbatt*
Hard Disk Interface		
W3	*Open**	*Enabled*
	Closed	*Disabled*
Watchdog Timer		
W4	*Open*	*Disable*
	*Closed**	*Enable*
Power Monitoring		
W5	*Open**	*Disabled*
	Closed	*Enable*

1 * as shipped

Flash EPROM

W6	*Open*	*No Flash*
	*Closed**	*Flash Installed*

BIOS Boot Flash[2]

W7	*Open**	*EPROM BIOS*
	Closed	*Flash BIOS*

Teknor BIOS Extension

W8	*Open**	*Enable*
	Closed	*Disable*

COM2 Configuration

	RS-232	*RS-485*
W9	*(1-2)**	*(2-3)*
W10	*(1-2)**	*(2-3)*
W11	*Open**	*Closed*
W12	*Open**	*Closed*
W13	*(1-2)**	*(2-3)*
W14	*(1-2)**	*(2-3)*

BUSCLK[3]

W14A	*CPUCLK*	*ASYNC*	*CPUCLK*
	25/50MHz	*16MHz*	*33/66MHz*
	1-2	*2-3*	*Open*

---

2 Not yet supported.

3 BUSCLK can be setup to boot 25MHz or 33MHz boards (Synchronous mode) or either (Asynchronous mode). However, when set to Asynchronous mode the boot process is much slower. Moreover, regardless of the CPU speed setting, the SYSCLK will always be at 8MHz after the boot up process.

CPU Type[4]

	486SX	486DX/DX2/DX4
W15	(1-2)	(2-3)
W16	Open	(1-2)
W17	Open	Closed

CPU Speed[4]

	25MHz	33/66/100MHz	50MHz
W18(1-2) S0	Closed	Open	Closed
W18(3-4) S1	Closed	Closed	Closed
W18(5-6) S2	Closed	Closed	Closed

Graphics

W19	Open*	Mono, EGA, VGA
	Closed	Color CGA Only

SRAM Memory Type

W20(1-2)	32Kx8, 128Kx8 Devices*
W20(2-3)	256Kx8, 512Kx8 Devices

Boot From Flash EPROM

SW2(1-2)	Open*	Boot From Drives
	Closed	Boot From Flash

COM1/COM2 Select for VT100 or Remote Download

SW2(3-4)	Open	Use COM1*
	Closed	Use COM2

Console is VT100

SW2(5-6)	Open*	Standard Display Mode
	Closed	VT100 Mode

---

4 **Factory configured.**

Remote Download

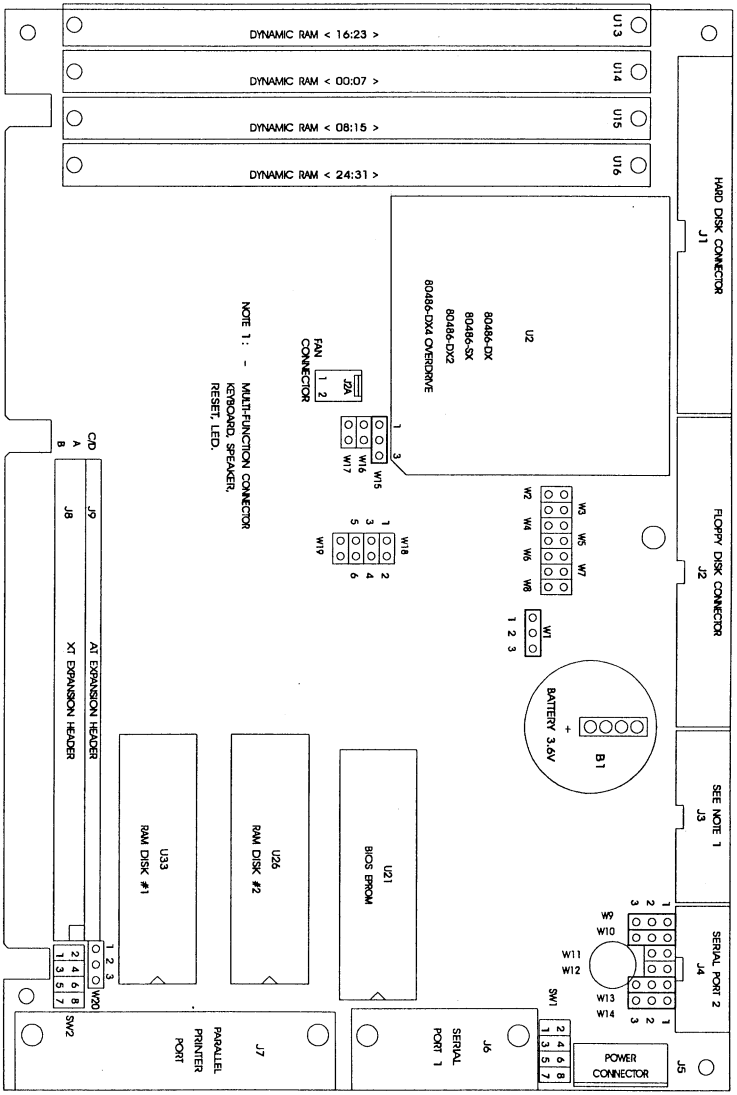
SW2(7-8)	*Open**	*Normal*
	Closed	*Remote Download*

Please refer to *Table 2-1* and *Diagram 2-1* for exact jumper locations.

TABLE 2-1 CONFIGURATION JUMPERS

JUMPER	FUNCTION	JUMPER	FUNCTION
W1(1-2)	Power Failure Detector	W1(2-3)	Low Battery Detection
W2	SRAM Battery Backup	W3	Hard Disk Interface
W4	Watchdog Timer	W5	Power Monitoring
W6	Flash EPROM	W7	BIOS Boot Flash
W8	Teknor BIOS Extension	W9	Serial In 2 (SIN2)
W10	Request To Send 2 (RTS2)	W11	CTS2 to RTS2
W12	DTR2 to DSR2	W13	Serial Out 2 (SOUT2)
W14	CTS2	W14A	SYSCLK Setup vs CPU Speed
W15-W17	CPU Type Selection	W18	CPU Speed Selection
W19	Color/Monochrome Selection	W20	SRAM Memory Type
SW2(1-2)	Boot from Flash	SW2(3-4)	COM1/COM2 Select
SW2(5-6)	Console is VT100	SW2(7-8)	Remote Download

DIAGRAM 2-1 JUMPER LOCATIONS



BIOS SETUP

The TEK-AT4 is fully software configurable. The setup program allows for minimal hardware configuration.

Setup Utility

The SETUP program is located within the BIOS and can be activated at boot time by following the instructions that appear on screen. In *VT100 Mode*, press <CTRL-R> at the configuration prompt during the power up sequence. Once the SETUP screen is displayed you can modify the date, time, or other setup information contained in the clock CMOS RAM. The system will reboot upon exiting from SETUP.

To modify an entry, simply follow the instructions that appear at the bottom of the SETUP screen. Use the arrow keys to select the item you want to change. When the item is selected, press <+> or <-> keys to change an entry.

Press <F10> to save the current configuration (press "Q" in *VT100 Mode*) and to exit. The configuration, with the exception of the time and date, is not saved until <F10> is pressed. Press <ESC> to exit without saving the setup.

User's Setup Configuration Information

The SETUP program can set the following:

Time of day and Date
Floppy disk configuration
Fixed disk configuration
System memory size
Extended memory size
EMS memory size
Video type
Execute BIOS from RAM or ROM Shadow
Wait state selection
Initial CPU speed

MEMORY AND I/O MAP SECTION 3

MEMORY MAPPING

The TEK-AT4 supports from 1 to 16 Megabytes of DRAM with parity check for system memory. You also have room for up to 2 Mbytes of solid state disks (SSDs): U21 allows up to 128Kbytes of EPROM for the BIOS and U11 supports 1 Megabyte of FLASH EPROM. Sockets U26 and U33 are reserved for up to 1 Megabyte of battery-backed SRAM disk.

EXPANDED AND EXTENDED MEMORY

Memory on the TEK-AT4 consists of two areas: memory below 1 Mbyte (0-640K) referred to as the standard or base memory, and memory located above 1 Mbyte which is either *Expanded* or *Extended* memory (memory located between 640K and 1 Mbyte is reserved for *Shadowing*. This is described later in this section).

Expanded and *Extended* memory refer to the mapping scheme that is used to access memory above 1 Mbyte in real mode. Since DOS requires real mode to operate, different techniques are available. The TEK-AT4 offers the following options:

Expanded Memory

In *Expanded* memory mode, hardware is used to remap a defined area of memory. This mode is driven by standard software commonly referred to as the *LIM Standard* or *EMS*. A hardware-specific device driver (supplied with your single board computer) is loaded in the CONFIG.SYS file to setup the software in order for it to access memory above 1 Mbyte.

Extended Memory

In *Extended* memory mode, the CPU's own protected mode is used to access the memory above 1 Mbyte. This mode requires that the software jump into protected mode, perform the transfer and return back to real mode. This is available through the BIOS using INT 15h function 87h.

TEK-AT4 Memory Mode

On the TEK-AT4, memory above 1 Mbyte can be defined either as *EMS* or *Extended*. If *EMS* is used, the *EMS* hardware must be enabled[5] and the *EMS* driver loaded[6].

---

5 EMS is enabled by entering SETUP at boot up.

6 Type the following command (or its equivalents) in the CONFIG.SYS file: DEVICE=EMM386.EXE

Shadow RAM

As previously mentioned, memory between 640K and 1 Mbyte is used for *Shadow RAM* or *Shadowing*. This is simply the process of copying EPROM based code, such as the BIOS and BIOS extensions, into DRAM (which is located in the same physical memory map). *Shadowing* allows your code to run faster.

☞ **If Shadow RAM is enabled, the RAM memory used for shadowing is no longer available as EMS or Extended memory.**

Configuring The TEK-AT4

Configuring your TEK-AT4 is purely a matter of the application at hand. As an example, a 2 Mbyte system can be defined as 640K base + 384K shadow + 1 Mbyte extended memory, or, 640K base + 384K shadow + 512K extended + 512K EMS and so on. The user is free to adapt the configuration to his particular needs.

TABLE 3-1 TEK-AT4 MEMORY MAPPING

1 Mbyte User EPROM	FFFFFF E00000	
U11 Flash EPROM	DFFFFF D00000	1-15 Mbytes User DRAM
U26 RAM backup #1	CFFFFF C80000	
U33 RAM backup #0	C7FFFF C00000	
1-13 Mbytes User DRAM	BFFFFF 100000	
64K System BIOS	OFFFFF 0F0000	64K System BIOS
BIOS EXTENSION	0EFFFF 0E0000	BIOS EXTENSION
Not Decoded Available To User	0DFFFF 0C0000	Not Decoded Available to User
128K Video RAM	0BFFFF 0A0000	128K Video RAM
640K User RAM	09FFFF 000000	640K User RAM

I/O MAP

The following table outlines the I/O ports used by the TEK-AT4:

TABLE 3-2 ONBOARD DECODED I/O MAP

ADDRESS	FUNCTION
000-00F	DMA controller 1
020-03F	Interrupt controller 1
040-05F	Timer
060-06F	Keyboard (8742)
070-07F	Real-time clock, NMI mask
080-09F	DMA page register
0A0-0BF	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0-0FF	Math coprocessor
1F0-1F7	Hard disk
201	Watchdog timer, PDO, user
378-37A	LPT1
2F8-2FF	COM2
3F2-3F7	Floppy disk
3F8-3FF	COM1

ONBOARD UTILITIES SECTION 4

DMA CONTROLLER (8237)

The TEK-AT4 supports eight direct memory access (DMA) channels. Two DMA controllers, functionally equivalent to the 8237, are used with four channels on each chip. Channel 0 is reserved for the DRAM refresh. Channel 4 is used to cascade channels 0 through 7 to the microprocessor, and Channel 2 is reserved for the floppy controller.

TABLE 4-1 8237 CONTROLLER TABLE

DMA 0	Refresh
DMA 1	Available
DMA 2	Floppy controller
DMA 3	Available
DMA 4	Cascade controller # 1
DMA 5	Available
DMA 6	Available
DMA 7	Available

INTERRUPT CONTROLLER (8259)

Two 8259 interrupt controllers handle the interrupts on the TEK-AT4. Six interrupt lines are directly linked to the keyboard controller, timer, the real-time clock, both serial ports and the parallel port.

TABLE 4-2 8259 CONTROLLER TABLE

CONTROLLER # 1		CONTROLLER # 2	
IRQ 0	Timer 0	IRQ 8	Real-time clock*
IRQ 1	Keyboard	IRQ 9	Available
IRQ 2	Cascade controller #2	IRQ 10	Available
IRQ 3	COM 2*	IRQ 11	Available
IRQ 4	COM 1*	IRQ 12	Available
IRQ 5	Available	IRQ 13	Available
IRQ 6	Floppy controller	IRQ 14	Fixed disk*
IRQ 7	LPT 1*	IRQ 15	Available

* All functions marked with an asterisk (*) can be disabled.

TIMER (8254)

The 8254 timer features three independent 16-bit timer/counters. Channel 0 is tied to interrupt 0, channel 1 is used to generate refresh with DMA Channel 0, and Channel 2 is used for the speaker port.

KEYBOARD CONTROLLER

The keyboard controller on the TEK-AT4 is a single-chip microcomputer (Intel 8042) that is programmed to support the keyboard serial interface.

The keyboard controller receives serial data from the keyboard, checks data parity, translates scan codes, and presents the data to the system as a byte of data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

TABLE 4-3 KEYBOARD CONTROLLER

ADDRESS		REGISTER
060	read	keyboard output buffer register
060	write	data write
064	read	Status register
064	write	Command write

KEYBOARD , SPEAKER, RESET and KEYLOCK INTERFACE

Connector J3 on the TEK-AT4 provides all the necessary signals for connecting the keyboard, speaker, reset, and keylock interface devices. The following diagram shows the signal connections at J3 (referred to as the Keyboard Header):

TABLE 4-4 J3 KEYBOARD HEADER

PIN NUMBER / SIGNAL FLOW / SIGNAL						PIN NUMBER / SIGNAL FLOW / SIGNAL
KBDCLK	O	1		2	-	GND
KBDDATA	O	3		4	-	GND
VCC	-	5		6	-	VCC
SPKR	O	7		8	-	VCC
KBDINH	I	9		10	-	GND
AUTO*	I	11		12	-	GND
PBRES*	I	13		14	-	GND
ACT*†	O	15		16	-	VCC

† ACT: See Hard Disk LED below

The following functions are available on the keyboard header, J3:

i. Speaker: An 8 ohm speaker can be directly connected to J3-7 and J3-8. All necessary drivers are on the TEK-AT4.

ii. Keyboard Disable: The keyboard can be disabled or locked up by shorting J3-9 and J3-10.

iii. Hard Disk LED: The onboard IDE interface activates an external LED. The LED must be connected *anode* on J3-16 and *cathode* on J3-15. No external current limiting resistor is required since one is already present on the TEK-AT4.

iv. Reset: The TEK-AT4 can be reset by shorting J3-13 and J3-14.

v. Auto: This signal, J3-11, when shorted with J3-12, puts the TEK-AT into *Download Mode* at boot up. *Auto* has the same effect and is in parallel with SW2 7-8.

MATH COPROCESSOR

The TEK-AT4 DX version comes complete with a built-in math coprocessor. The math coprocessor is contained within the CPU and works in parallel with the microprocessor.

The parallel operation decreases operating time by allowing the coprocessor to do mathematical calculations while the microprocessor continues to do other functions.

The presence of the math coprocessor is automatically detected by the BIOS.

SUPERVISOR UTILITIES

Special Note on Register 201 (hex)

IBM PCs use address 201 (hex) as the game port. TEKNOR computers utilize this address space in a manner which gives industrial PC users the greatest amount of I/O addressing space possible. This ultimately renders the game port unusable.

Hence, some problems may occur with various test software packages that intentionally write to the game port and leave it with unknown values.

The following diagram illustrates how TEKNOR computers utilize I/O Register 201 (hex):

TABLE 4-5 REGISTER 201 (hex)

Bit	Function
0	Enable Watchdog (1=enable, R/W bit)
1	Watchdog activate (1-0-1 to toggle, R/W bit)
2	Flash VPP enable (1=VPP 12v, 0=VPP 5v, R/W bit)
3	Enable direction control RS-485 (1=enable RS-485 only, write only)/ (Read=PDO* Status)
4	Make printer 8 data bits read only[7] (1=input, 0=output, write only)
5	Select alternate SW1/SW2 (TEK-AT4, TEK-AT3L, TEK-AT4) (1=select SW1, read only)
6	Not used
7	Not used

[7] **This feature is available on all TEK-AT computers except TEK-AT1 revision 3 and earlier.**

☞ **Not all bits are R/W. Therefore, be certain to keep a mirror image of register 201(hex) when programming it.**

☞ **All bits are 0 after a hardware RESET or power up condition.**

Watchdog Timer

The *Watchdog Timer* is extremely useful in embedded systems where human supervision is not required. Following a reset, the *Watchdog* is always disabled. The *Watchdog* is enabled once you write "1" in bit "0" at address 201(hex) the first time. When enabled, the microprocessor must refresh the *Watchdog*. This is done by writing alternatively "0" and "1" to bit 1 at address 201(hex), once every 1.6 seconds to verify proper software execution.

If a hardware or software failure occurs such that the *Watchdog* is not refreshed, a reset pulse is generated by the *Watchdog* to restart the processor.

☞ **The user program must provide the first access to address 201(hex), and must also include the refresh routine. In addition, be certain to keep a mirror image of register 201(hex) when programming it. This is necessary since register 201(hex) is a write-only user register and, as a result, is not used by the BIOS.**

TABLE 4-6 WATCHDOG TIMER REGISTER

ADDRESS		REGISTER
201 bit 0	read/write	Watchdog enable
201 bit 1	read/write	Watchdog refresh

Jumper W4 must be installed to permit activation of the *Watchdog*. If jumper W4 is removed, the *Watchdog* is disabled.

Power Failure Detector

The power failure detector, which generates a non-maskable interrupt (NMI) when a failure occurs, provides a 1.25V threshold for DC power fail warning, low battery detection W1(2-3), or when monitoring a power supply other than +5VDC W1(1-2). The Power Detection Output (PDO) of the power failure detection circuit is connected to IOCHECK (NMI). Jumper W5 allows the user to disable this feature. However, the PDO status is still available by reading I/O address 201 bit 3.

TABLE 4-7 POWER MONITORING

JUMPER		FUNCTION
W5	Open	Power monitor disable
W5	Closed	Power monitor enable

The detection circuit generates a non-maskable interrupt when a power failure occurs. The status of the PDO is available at I/O address 201 bit D3. For example, if it reads 0, the circuit has detected a low power warning from the power detect pin on J5-6.

Pin 6 on connector J5 is used for the power detection input. This input can only accept DC voltage. The line is monitored via two user-defined external resistors, R40 and R39, which are connected to the power failure input (Note: R40 is a surface mount resistor and R39 is fixed to 1K). The user should position the resistors according to the monitoring level desired. If the voltage level supplied to this line drops below 1.3V typical, a *Power Fail* status is detected and directed to the NMI line.

Example:
Assume the TEK-AT4 is powered by a 9V DC battery and it is required that the battery be monitored for a low battery warning at 7.5V DC. In this case, R40=4700Ω and R39=1000Ω.

So, if the battery voltage goes below 7.5V, it will generate a non-maskable interrupt (NMI) and the status can be read at address 201 bit D3. If bit D3 is 0, a low battery is indicated.

Bear in mind that R40 and R39 should be tailored to fit your specific application. The values for these two resistors can be identified by using the following formula:

$$\left(\frac{R39}{R40+R39} \right) * 7.5V \leq 1.3V$$

where: $R40 = \left(\frac{1000Vmon - 1300}{1.3} \right)$

Please contact our technical support department if more details are needed.

☞ **All TEK-AT boards are equipped with an onboard detection circuit which is activated when +5V drops below 4.75V. When this occurs, the system is reset disabling access to SRAM, DRAM, and so on.**

Low Battery Detection

The TEK-AT4 allows you to detect a *Low Battery Voltage*. This procedure uses the same circuit as the *Power Failure Detector*, and thus, both cannot be used at the same time.

The *Low Battery Detector* generates an NMI when the battery voltage drops below 3 volts.

To monitor a *Low Battery Voltage*, install jumper W1(2-3) and jumper *W5*. The status of PDO can be read back at I/O port 201 hex D3.

☞ **Although the *Low Battery Detector* uses the same circuit as the *Power Failure Detector*, J5-6, R40 and R39 are not utilized. Instead, we have added two other resistors for this function: R37 and R36.**

REAL-TIME CLOCK

The RTC is compatible with the popular MC146818. It combines a complete time-of-day clock with a one-hundred year calendar, an alarm, a programmable periodic interrupt, and 114 bytes of low-power static RAM. A battery backup facility is provided for the RTC. The internal clock circuitry uses 14 bytes of this RAM, and the rest is reserved for configuration information.

PARALLEL PORT (LPT1)

The parallel port is 100% PC/AT compatible. It provides the necessary control signals for use as a Centronics-compatible parallel interface. The connection is done through a DB-25 connector, J7, located at the edge of the board.

TABLE 4-8 LPT1 (J7)

PIN NUMBER / SIGNAL	SIGNAL FLOW				PIN NUMBER / SIGNAL	SIGNAL FLOW
STB*	O	1		2	I/O	P0
P1	I/O	3		4	I/O	P2
P3	I/O	5		6	I/O	P4
P5	I/O	7		8	I/O	P6
P7	I/O	9		10	I	ACK*
BUSY	I	11		12	I	PE
SLCT	I	13		14	O	AFD*
ERR*	I	15		16	O	INIT*
SLIN*	O	17		18	-	GND
GND	-	19		20	-	GND
GND	-	21		22	-	GND
GND	-	23		24	-	GND
GND	-	25				

Changing Direction on LPT1

The 8 bit data is set to *output* by default. It can be changed to 8 bit *input* simply by writing 10h to address 201h (set bit 4).

☞ **Port 201h is also used to control the *Watchdog Timer*. Therefore, it is highly recommended you keep a mirror image of port 201h in memory.**

SERIAL COMMUNICATION PORTS

The TEK-AT4 features two UARTs which are functionally equivalent to the NS16450. They are both configured as DTE. The COM1 (J6) port is buffered directly on the board for RS-232 operation. The COM2 port may be buffered for either RS-232 or for RS-485. To configure COM2 for RS-485, please refer to *Section 2, Configuration Jumpers.*

COM1 (J6) Hardware Configuration

The COM1 port is configured as RS-232, and is 100% compatible with the IBM-AT serial port.

TABLE 4-9 COM1 (J6)

PIN NUMBER					PIN NUMBER	
SIGNAL FLOW					SIGNAL FLOW	
SIGNAL						SIGNAL
DCD	I	1	2	I		RX
TX	O	3	4	O		DTR
GND	-	5	6	I		DSR
RTS	O	7	8	I		CTS
RI	I	9				

COM2 (J4) Hardware Configuration

COM2 (J4) as RS-232

The COM2 port is configured as RS-232, and is 100% compatible with the IBM-AT serial port.

TABLE 4-10 COM2 (J4) RS-232

PIN NUMBER					PIN NUMBER	
SIGNAL FLOW					SIGNAL FLOW	
SIGNAL						SIGNAL
DCD	I	1	2	I		DSR
RX	I	3	4	O		RTS
TX	O	5	6	I		CTS
DTR	O	7	8	I		RI
GND		9				

☞ **The pinout for J6 and J4, shown above, may appear to be different. However, since J4 (COM2) is a 10 pin flat ribbon connector, the flat ribbon cable will produce an identical pinout as J6 (COM1) when crimped to a DB9 connector provided pin 1 is kept aligned.**

COM2 (J4) as RS-485

If the TEK-AT4 is configured for RS-485 operation. It can support either full-duplex or party line communication.

Full Duplex Operation

Upon power-up or reset, the RS-485 interface circuits are automatically configured for full duplex operation. J4(3,4) act as the receiver lines and J4(5,6) as the transmitter lines.

Party Line Operation

In order to enable party line operation, the user must first write "1" to bit 3 at I/O address 201. This allows the transceiver (J4 3,4) to be controlled by the RTS signal. Upon power-up or reset, the transceiver is by default in "receiver mode" in order to prevent unwanted perturbation on the line.

In party line operation, termination resistors R12 and R13 must be installed only on the boards at both ends of the network.

TABLE 4-11 COM2 (J4) RS-485

PIN NUMBER SIGNAL FLOW SIGNAL				PIN NUMBER SIGNAL FLOW SIGNAL		
RESERVED	-	1	2	I	NC
RXD(-)	I/O	3	4	I/O	RXD(+)
TXD(-)	O	5	6	I	TXD(+)
NC	O	7	8	I	NC
GND	-	9			

POWER MANAGEMENT

Average system power consumption can be reduced by de-activating or slowing the chip set and processor clock during idle periods.

If a non-static CPU is used, the processor clock can be slowed down. By using a static CPU, the processor clock can be stopped completely.

On the TEK-AT4 a "sleep mode" is provided in which a HALT instruction executed by the CPU triggers the slowing or stopping of PROCCLK.

Using Sleep Mode

Sleep Mode can be enabled by software. The low power mode or *Sleep Mode* turns off the floppy disk controller, the crystal oscillator, both UARTS and the processor. CMOS technology consumes more power when it is made to oscillate faster. Therefore, by reducing the oscillating speed of the chip set and processor, overall power consumption is also greatly reduced.

In *Sleep Mode*, power consumption of the TEK-AT4 is reduced to approximately 700mw.

If more details are required, please contact our technical support department.

FLOPPY DISK CONTROLLER

The floppy disk controller on the TEK-AT4 is IBM PC and AT compatible (single and double density). It handles 3.5 inch and 5.25 inch low and high density drives. Up to two drives can be supported in any combination.

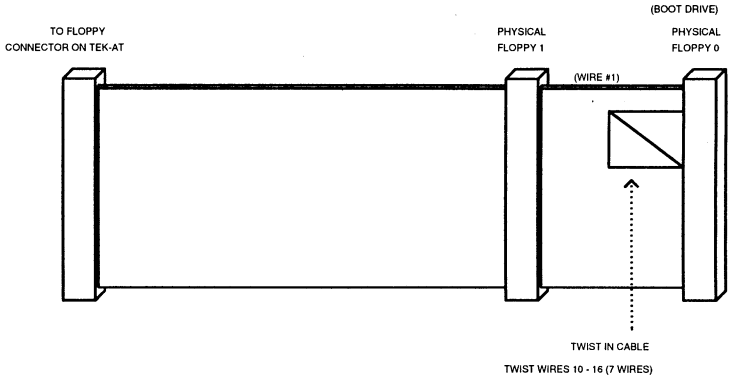
Mechanical Floppy Disk Installation

The installation of floppy drives on the TEK-AT4 is done via a standard IBM 34-pin flat ribbon cable that connects to J2. The pin-out is described below:

TABLE 4-12
FLOPPY DISK CONNECTOR PINOUT (J2)

Pin Number	Signal Flow	Signal
2	*O*	*RPM/LC*
4	-	*N.C.*
6	-	*N.C.*
8	*I*	*INDEX**
10	*O*	*MOTRENA**
12	*O*	*DRIVESB**
14	*O*	*DRIVESA**
16	*O*	*MOTRENB**
18	*O*	*DIRC**
20	*O*	*STEP**
22	*O*	*WRITE DATA**
24	*O*	*WRITE ENABLE**
26	*I*	*TRACK0**
28	*I*	*WRITE PROTECT**
30	*I*	*READ DATA**
32	*O*	*HEAD SELECT**
34	*I*	*DCHG*
1-33 (ODD)	-	*GND*

DIAGRAM 4-1 FLOPPY DISK CABLE



HARD DISK CONTROLLER

The TEK-AT4 supports AT Integrated Disk Drives. The AT embedded drive architecture incorporates drive electronics and controller circuitry on a single printed circuit board which is mounted directly to the disk drive chassis. The integration of drive and controller functions increases reliability and performance by eliminating redundant circuitry. Thus, providing increased performance at reduced cost.

Hard Disk Installation

To connect an IDE hard disk to the TEK-AT4, a 40-pin dual row header signal connector is required. This connector handles all command, data, and status I/O lines. The 40-pin male header connector located at J1 on

the TEK-AT4 connects directly with the cable. A maximum cable length of 18 inches is recommended.

The drive itself can be mounted in any horizontal or vertical plane. The hard drive must be indicated in the CMOS setup. The number of cylinders, heads, sectors per track, landing zone, and write precompensation must all be specified. This is done through selecting a standard drive type listed in the setup screen or by using a user defined drive type (type 48), whereby the user can enter the required parameters.

Your drive manufacturer can supply this information.

☞ **The onboard hard disk interface can be disabled on the TEK-AT4 by installing jumper W3.**

TABLE 4-13 HARD DISK CONNECTOR PINOUT (J1)

Pin Number	Signal Flow	Signal
3	I/O	SD7
4	I/O	SD8
5	I/O	SD6
6	I/O	SD9
7	I/O	SD5
8	I/O	SD10
9	I/O	SD4
10	I/O	SD11
11	I/O	SD3
12	I/O	SD12
13	I/O	SD2
14	I/O	SD13
15	I/O	SD1
16	I/O	SD14
17	I/O	SD0
18	I/O	SD15
1	I	RST*
23	I	IOW*
25	I	IOR*
33	I	SA1
35	I	SA0
36	I	SA2
37	I	CS0*
38	I	CS1*
31	O	IRQ14
32	O	I/OCS16*
39	O	ACTIVE*
20	-	KEY (NOT CONNECTED)
21	-	RESERVED (NOT CONNECTED)
34	-	PDIAG
2,19,22,24 26,30,40	-	GND

SOLID STATE DISKS

The TEK-AT4 has two, 32-pin sockets that can be used for solid state (semiconductor) disks. Solid state disks (SSDs) have no moving parts and are far less susceptible to dirt, moisture, vibration and temperature variations than mechanical floppy disks. Two types of SSDs are

available on the TEK-AT4, Flash EPROM and Static-RAM (SRAM).

Flash EPROM Disk

The non-volatile characteristics of Flash memory eliminate the risk of losing valuable data updates (a concern with battery-backed SRAM). As a result, Flash memory offers major advantages in applications like automated factories, remote systems, portable equipment and similar environments. Plus, Flash memory is obtainable at a much lower cost than EPROM or battery-backed SRAM. The TEK-AT4 comes standard with 1Mbyte of Flash EPROM in a TSOP design.

Flash disks "look" identical to floppy disks. Therefore, all the functions that can be performed on floppy disks are available on the Flash disks: e.g. booting, reading, copying, and so on.

The only difference between the two drive types is that Flash disks are read only. Hence, whenever an attempt is made to write to the Flash disk, a write-protect error is generated. Writing to Flash disks is explained below and in detail in TEKNOR's *XFLASH User's Manual.*

☞ **In order for the TEK-AT4 to recognize the Flash disk, Jumper W6 must be installed.**

Writing To Flash Disks

To create a Flash disk (i.e. writing information to it), use the XFLASH utility found on the utilities diskette which came with this board.

The XFLASH software utility allows you to choose files from floppy and hard disks and write them to the Flash disks.

Information can be transferred to the Flash disk by directly running XFLASH on the TEK-AT4 computer, or remotely - by using a serial link. The second option is referred to as *Download Mode* and is enabled by installing jumper SW2(7-8).

In addition, the Flash disk can be made to boot simply by installing SW2(1-2). This function causes the Flash disk to replace floppy disk 0 from the "A" position - leaving the mechanical floppy unused. Floppy 0 must then be physically moved to the floppy 1 position where it becomes the "B" drive. Please refer to the *Physical Devices Table* for more information.

SRAM Disk

The TEK-AT4 comes with two SRAM sockets which are automatically configured as a read/write battery-backed SRAM disk.

The SRAM disk also "looks" just like a floppy disk since you can read and write directly to it using regular DOS commands. The only limitation is that the SRAM disk is not bootable. Therefore, the boot process must take place in either the Flash disk, floppy 0 or hard disks.

The TEK-AT4 supports 32Kx8, 128Kx8, 256Kx8 and 512Kx8 devices. The SRAM disk can be configured from 32K to 1Mbyte. The SRAM devices cannot be mixed, but the SRAM disk may be made up of a single device if so desired. SRAM bank 0 and SRAM bank 1 are located at sockets U33 and U26 respectively.

☞ **If a single SRAM device is used it must be installed on the lower socket (U33), i.e. the one closest to the bus connector.**

Once installed, the device types must be configured on the board as indicated in the following table:

TABLE 4-14 STATIC-RAM DISK

JUMPER	FUNCTION
W20(1-2)	32kx8 and 128kx8 devices
W20(2-3)	256kx8 and 512kx8 devices

If SRAM disk operation is not desired, but battery-backed SRAM memory is needed, simply install a device on the top socket, U26 (i.e. the one farthest from the bus connector). The BIOS will then ignore this device leaving its contents intact.

☞ **SRAM power consumption is usually less than 5μA in 3V backup mode. So files transferred to battery-backed SRAM disks typically stay resident for two years. Actual life, however, is dependent on the actual consumption of the SRAM devices installed.**

Installing SRAM Disks

It is extremely important that Pin 1 be properly located on the SSD chips before inserting them into their mating sockets on the TEK-AT4.

SRAM devices generally contain an indented circle or a notch on one end of the device's case. Check both ends of the device thoroughly before assuming you have located Pin 1. Sometimes, circles can be found on both ends of the chip. When this happens, look for the circle with the deeper groove. Pin 1 is located at this end.

Use the *Jumper Locations Diagram* in this manual to help you locate Pin 1 on the TEK-AT4 computer card. Align Pin 1 on the chip with Pin 1 on the TEK-AT4 SRAM socket and insert the device. Pay special attention not to bend or crack the chip's pins.

☞ **Do not assume that all TEK-AT cards have Pin 1 oriented in the same direction. Although the TEK-AT4 boards are all similar, the TEK-AT3 series, for example, have Pin 1 aligned in the opposite direction.**

Note that 32Kx8 SRAM chips come in a 28-pin configuration. Therefore, four extra pins will remain visible on the socket after the device has been installed. The four extra pins on the socket are those at the end where Pin 1 is located.

Be sure to always use your *TEK-AT Technical Reference Manual* to properly locate the SSD sockets and Pin 1 whenever inserting devices onto your single board computer.

Battery Backup Circuit

A 350maH lithium battery is installed on the TEK-AT4. If the TEK-AT4 is strapped to be powered by the battery back-up, the RAMs will retain their information after a power down.

TABLE 4-15 BATTERY BACKUP CIRCUIT

JUMPER		FUNCTION
W2	open	NC
W2	closed	Vbatt

☞ **Removing jumper W2 will cause the set-up and real-time clock information to be lost.**

The TEK-AT4 comes with a 350 maH TL5186 TADIRAN battery with a shelf life of approximately 10 years (under "no-load" conditions).

TEK-AT4 draws approximately 14μA typical. This means the battery will last 2 years if no power is applied to the board. Remember, when the 5V is supplied, the battery is electronically disconnected. Virtually as if it were on the shelf.

The actual life of the battery depends on the amount of time DC power is not applied and on environmental (temperature) conditions. The TADIRAN TL5186 has an operating range of -55^0 to 75^{0}C and discharge characteristics vary with temperature.

The TADIRAN TL5186 is U.L. recognized. Its U.L. component recognition is MH12193.

☞ **The actual voltage supplied by the battery is 3.6 volts. This can be verified at pins 16-32 on the SRAM sockets using a standard voltmeter.**

BUS CLK SPEED

It is very important that the correct BUS Clock Speed be selected. In order to set it to the 8 MHz standard, you must install *Jumper W14A(2-3).*

Then, go to the *Advanced Chipset Setup* in the TEK-AT4 SETUP menu, and set the *Fast Busclock Divider* and the *Slow Busclock Divider* to */2*. The procedure is the same for all four TEK-AT4 processor speeds (i.e. SX-25, DX-33, DX2-66 or DX4-100).

POWER CONNECTOR (J5)

This connector can be utilized to supply the TEK-AT4 when you are not using a passive backplane. The pin-outs are shown below:

TABLE 4-16 POWER CONNECTOR PINOUT (J5)

PIN NUMBER SIGNAL FLOW SIGNAL					PIN NUMBER SIGNAL FLOW SIGNAL
VCC		1	2		GND
GND		3	4		+12V
-12V		5	6		PD

OPERATION
SECTION 5

CONFIGURATION JUMPERS (SW2)

The TEK-AT4 has an onboard BIOS extension which controls certain functions of the BIOS related to industrial applications. The extended BIOS reads the status of the SW2 jumpers and acts accordingly.

Upon system start-up, the BIOS automatically determines how much ROM/RAM disk memory is available to the system, and what equipment is connected to the system. Jumpers SW2 are to be set by the user as needed. The following table lists the available modes:

TABLE 5-1 SW2 JUMPER SETTINGS

JUMPER	FUNCTION
SW2(1-2)	Boot From Flash Devices
SW2(3-4)	Reserved
SW2(5-6)	Boot From VT100 Terminal
SW2(7-8)	Activate Serial Download Mode

LOGICAL DISK CONFIGURATION

The TEK-AT4 can detect two semiconductor drives - A Flash EPROM disk drive and a battery-backed SRAM disk drive.

These drives are installed as follows:

If SW2(1-2) is installed (i.e. booting MS-DOS from Flash EPROMs), then Drive A: is the Flash Disk (assuming jumper W6 is installed). Drive B: is Floppy 1 (if installed) or the next available drive according to the following list of priorities:

1- Floppy 1
2- Flash Disk if not already installed as A:
3- RAM Disk (if installed)
4- Hard Disk (if installed)

Subsequent logical drives are installed following the above priority list.

If SW2(1-2) is not installed (i.e. booting operating system from F/H drives), then Drive A: is Floppy 0. Drive B:, and subsequent drives, follow the priority list above.

Please refer to the *Physical Devices Table* for complete information.

☞ **The RAM disk is automatically detected and installed upon booting. The beginning of the disk is checked and reformatted if it is found to be corrupt or if data is unrecognizable.**

TABLE 5-2 PHYSICAL DEVICES TABLE

PHYSICAL DEVICES INSTALLED & DRIVE ASSIGNMENTS						
CONFIGURATION AND PHYSICAL DEVICES INSTALLED	JUMPER OR NO JUMPER FLOPPY 0 FLOPPY 1 NO FLASH DISK	NO JUMPER FLOPPY 0 FLOPPY 1 FLASH DISK	JUMPER FLOPPY 0 OR NO FLOPPY 0 FLOPPY 1 FLASH DISK	NO JUMPER FLOPPY 0 FLASH DISK	JUMPER FLOPPY 1 FLASH DISK	JUMPER FLASH DISK
DRIVE NAME:						
A:	FLOPPY 0	FLOPPY 0	FLASH	FLOPPY 0	FLASH	FLASH
B:	FLOPPY 1	FLOPPY 1	FLOPPY 1	FLASH	FLOPPY 1	AVAILABLE
C:	AVAILABLE	FLASH	AVAILABLE	AVAILABLE	AVAILABLE	AVAILABLE
D:	AVAILABLE	AVAILABLE	AVAILABLE	AVAILABLE	AVAILABLE	AVAILABLE

NOTES: The indication "FLASH DISK" assumes at least one Flash device is installed at U24 with a valid DOS content. "Floppy 0" specifies the physical drive connected to the twisted end of the flat cable. "Floppy 1" specifies the physical drive connected to the untwisted end of the flat cable. "Jumper" specifies configuration Jumper SW2(1-2). All other drives are installed following the above assignments in this manner: RAM Disk, and then Hard Disk. Therefore, with a full configuration, RAM Disk is "D" and the Hard Disk is "E".

VT100 OPERATION (SW2(5-6))

The TEK-AT4 utilizes a feature known as *VT100 MODE.* This mode enables your single board computer to run without a local keyboard or screen. That is, operation can be controlled via a remote terminal or a computer with a terminal emulation program.

Requirements

To use *VT100 Mode*, the TEK-AT board must be supplied with +/-12 volts. This is the voltage required by the RS-232 drivers.

The terminal you are using should emulate a VT100 or ANSI terminal. Although this is not an absolute requirement, strange characters may appear on screen if it does not. This occurs because the VT100 recognizes these control characters, and causes them to perform a specific function. For example, screen erase, cursor position, and so on.

Hardware Setup And Configuration

Follow these steps to setup for *VT100 Mode*:

- Install jumper SW2(5-6) to enable *VT100 Mode* {note: *VT100 Mode* runs on COM1 (3F8H)}.

- Setup the communications cable as shown in *Diagram 5-1* {Note: If you do not require a full cable for your terminal, you can setup a partial cable using only the TXD and RXD lines. The control lines can be ignored by looping them back as shown in *Diagram 5-2*}.

- Boot up your terminal and set it up with the following parameters:

  19200 Baud
  8 Bits
  No Parity
  Echo off (or full duplex)

☞ **Use CTRL-R to configure your system in *VT100 Mode*.**

Running Without A Terminal

If you wish to disconnect the VT100 terminal or if you decide to run without a terminal, you must ensure the control lines are in an active state. Failing this, the system may "hang" while waiting for the control lines to become active. Wiring the system according to *Diagram 5-2* allows the lines to remain active.

Furthermore, you can run without any console at all simply by not enabling VT100 mode and by not installing a video card.

DIAGRAM 5-1 VT100 FULL CABLE SETUP

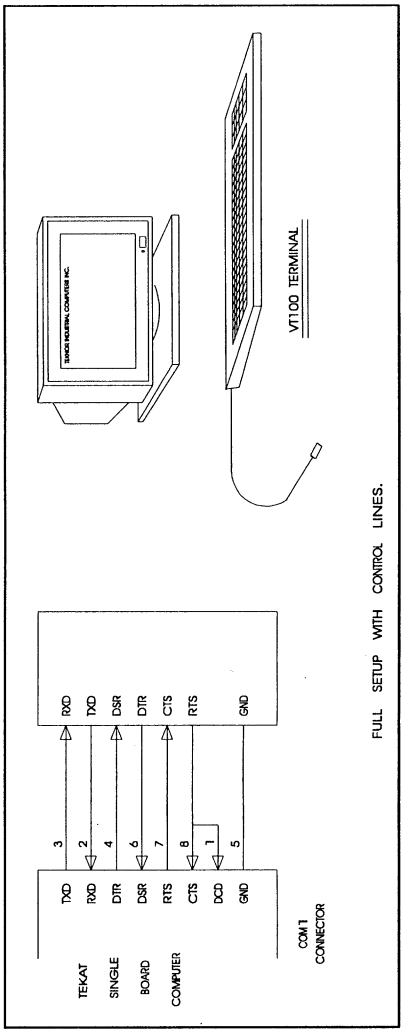
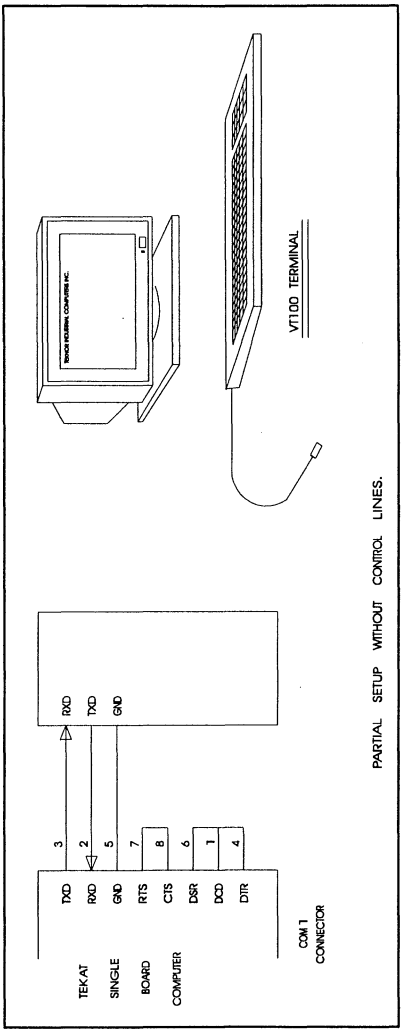


DIAGRAM 5-2 VT100 PARTIAL CABLE SETUP



DISK DRIVES AND SEMI CONDUCTOR DISKS

All disk drives and semi conductor disks operate identically in both regular and VT100 mode, and all drive assignments remain the same.

Downloading software to Flash devices is done through XFLASH, TEKNOR's transfer utility software. Please refer to the *XFLASH User's Manual* for details.

BAUD RATE RESTRICTIONS

The baud rate is re-initialized each time a call to INT 1OH (display to console) is made. This is due to some software programs, such as MS-DOS, changing the baud rate when loading.

GRAPHICS/STAND-ALONE (SW2(5-6))

The TEK-AT4 can operate without any video controller, keyboard or mechanical drives. The TEK-AT4 will automatically detect the presence of video, keyboard and mechanical drive devices and act accordingly. The TEK-AT4 can be used with the TEK-PG VGA card or any IBM compatible graphics controller card. Before starting the system, the user should also verify that the color monitor attached to the system can support the desired graphics mode.

TEK-AT4 BIOS SECTION 6

OVERVIEW AND FEATURES

The TEK-AT4 uses the CHIPS AND TECHNOLOGY PC/AT BIOS. This BIOS provides a software interface between the MS-DOS operating system and the hardware of the TEK-AT4 single-board computer. The interface provided by the BIOS is 100% IBM AT compatible. That is, all functions accept similar inputs and provide the same results as IBM, although the program code itself is different.

ERROR HANDLING

TEKNOR BIOS can be configured to handle errors differently. Two possibilities exist:

Stop: The BIOS will stop the booting process if an error is detected and request the user to press F1.

Warning: The BIOS will display an error message but will continue the booting procedure

The following lists the error sources and their default values.

[Warning]	*Diskette*
[Warning]	*Fixed Disk*
[Warning]	*Keyboard*
[Warning]	*Video*
[Warning]	*Memory size*
[Warning]	*CMOS checksum*
[Warning]	*Real-Time Clock*
[Warning]	*POST configuration*
[Warning]	*Coprocessor*
[Warning]	*Other*

SPECIFICATIONS SECTION 7

TEK-AT4 DC CHARACTERISTICS

Supply Voltage:	Vcc min.:	4.75V
	Vcc max.:	5.25V
	+12V:	+/-5%
	-12V:	+/-5%

Supply Current: Standard PC/AT Application[8]

TABLE 7-1 SUPPLY CURRENT

	SX 25MHz	DX 33MHz	DX2 66MHz	DX4 100MHz
Icc typ.	1.25A	1.50A	1.80A	1.65A
Ipp+12V	15mA	15mA	15mA	15mA
Ipp -12V	5mA	5mA	5mA	5mA

TEK-AT4 ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:

0°C to 70°C [9]

Non-Condensing relative humidity:

5% to 95%

---

8 This current was measured with 4 Mbytes of DRAM, 1 Mbyte of User Flash EPROM, 256K SRAM, along with hard disk, floppy disk, keyboard and monitor installed.

9 Casing temperature.

DIAGRAM 7-1 MECHANICAL SPECIFICATIONS

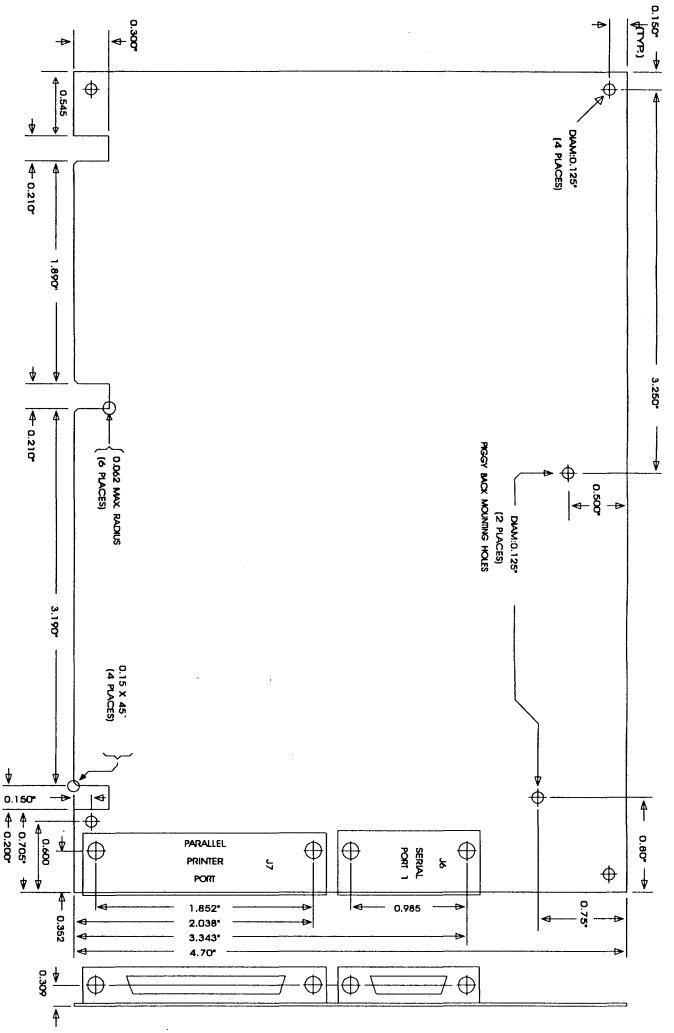


DIAGRAM 7-2 ASSEMBLY

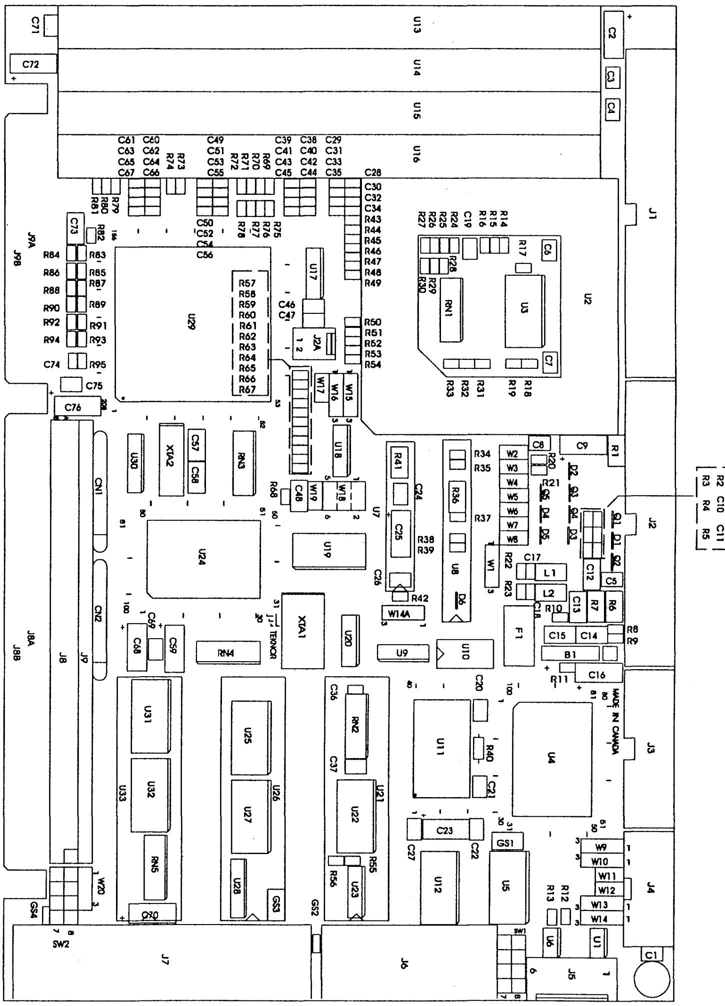
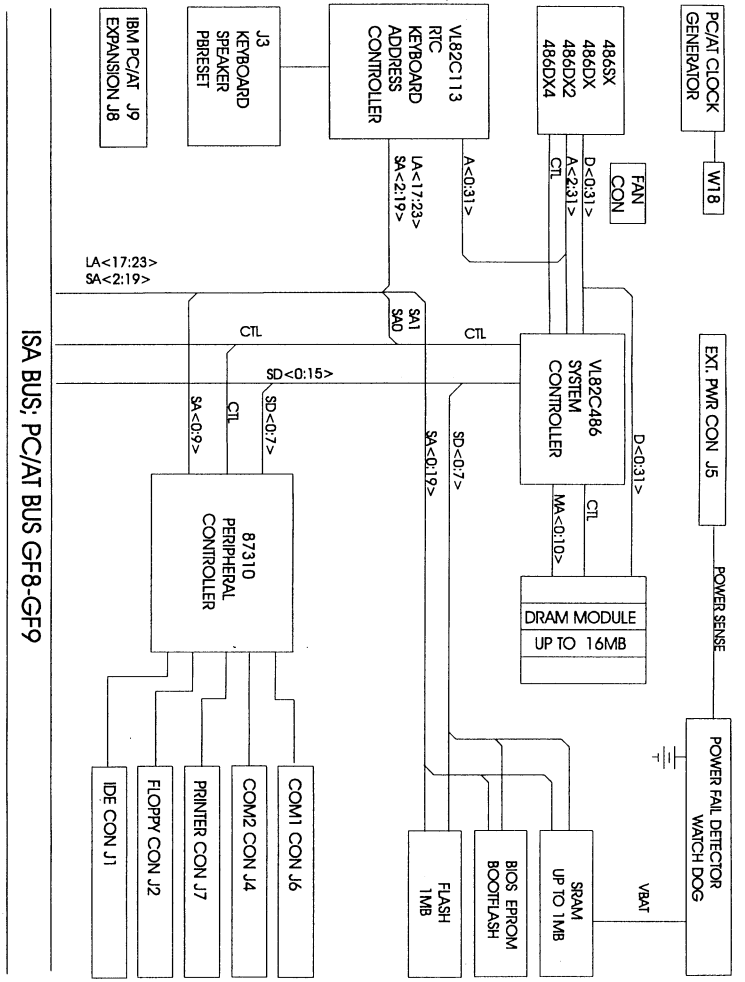


DIAGRAM 7-3 BLOCK DIAGRAM



CONNECTOR OVERVIEW

J5 POWER CONNECTOR

PIN NUMBER SIGNAL FLOW SIGNAL				PIN NUMBER SIGNAL FLOW SIGNAL		
VCC	-	1		2	-	GND
GND	-	3		4	-	+12V
-12V	-	5		6	-	PD

J3 KEYBOARD CONNECTOR

PIN NUMBER SIGNAL FLOW SIGNAL				PIN NUMBER SIGNAL FLOW SIGNAL		
KBDCLK	O	1		2	-	GND
KBDDATA	O	3		4	-	GND
VCC	-	5		6	-	VCC
SPKR	O	7		8	-	VCC
KBDINH	I	9		10	-	GND
AUTO*	I	11		12	-	GND
PBRES*	I	13		14	-	GND
ACT*	O	15		16	-	VCC

J7 PRINTER CONNECTOR

PIN NUMBER SIGNAL FLOW SIGNAL					PIN NUMBER SIGNAL FLOW SIGNAL
STB*	O	1	2	I/O	P0
P1	I/O	3	4	I/O	P2
P3	I/O	5	6	I/O	P4
P5	I/O	7	8	I/O	P6
P7	I/O	9	10	I	ACK*
BUSY	I	11	12	I	PE
SLCT	I	13	14	O	AFD*
ERR*	I	15	16	O	INIT*
SLIN*	O	17	18	-	GND
GND	-	19	20	-	GND
GND	-	21	22	-	GND
GND	-	23	24	-	GND
GND	-	25			

J6 COM1 CONNECTOR

PIN NUMBER / SIGNAL FLOW / SIGNAL				PIN NUMBER / SIGNAL FLOW / SIGNAL		
DCD	I	1		2	I	RX
TX	O	3		4	O	DTR
GND	O	5		6	I	DSR
RTS	O	7		8	I	CTS
RI	I	9				

J4 COM2 CONNECTOR RS-232

PIN NUMBER / SIGNAL FLOW / SIGNAL				PIN NUMBER / SIGNAL FLOW / SIGNAL		
DCD	I	1		2	I	DSR
RX	I	3		4	O	RTS
TX	O	5		6	I	CTS
DTR	O	7		8	I	RI
GND	-	9				

J4 COM2 CONNECTOR RS-485

PIN NUMBER / SIGNAL FLOW / SIGNAL						PIN NUMBER / SIGNAL FLOW / SIGNAL
RESERVED	-	1		2	I	NC
RXD(-)	I/O	3		4	I/O	RXD(+)
TXD(-)	O	5		6	I	TXD(+)
NC	O	7		8	I	NC
GND	I	9				

GF8-GF9 PC BUS CONNECTOR

A Side

I/O PIN	SIGNAL NAME	I/O
A1	I/O CH CK*	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	I/O CH RDY*	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

B Side

I/O PIN	SIGNAL NAME	I/O
B1	GND	Ground
B2	RESET DRV	O
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	SMESW*	O
B12	SMEMR*	O
B13	IOW*	I/O
B14	IOR*	I/O
B15	DACK3*	O
B16	DRQ3	I
B17	DACK1*	O
B18	DRQ1	I
B19	REFRESH*	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DACK2*	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

C Side

I/O PIN	SIGNAL NAME	I/O
C1	SBHE*	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MEMR*	I/O
C10	MEMW*	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

D Side

I/O PIN	SIGNAL NAME	I/O
D1	MEM CS16*	I
D2	I/O CS16*	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DACK0*	O
D9	DRQ0	I
D10	DACK5*	O
D11	DRQ5	I
D12	DACK6*	O
D13	DRQ6	I
D14	DACK7*	O
D15	DRQ7	I
D16	+5Vdc	Power
D17	MASTER*	I
D18	GND	Ground

J8 MEZZANINE CARD CONNECTOR

A Side

	I/O PIN	SIGNAL NAME	I/O
1	A1	I/O CH CK*	I
3	A2	SD7	I/O
5	A3	SD6	I/O
7	A4	SD5	I/O
9	A5	SD4	I/O
11	A6	SD3	I/O
13	A7	SD2	I/O
15	A8	SD1	I/O
17	A9	SD0	I/O
19	A10	I/O CH RDY*	I
21	A11	AEN	O
23	A12	SA19	I/O
25	A13	SA18	I/O
27	A14	SA17	I/O
29	A15	SA16	I/O
31	A16	SA15	I/O
33	A17	SA14	I/O
35	A18	SA13	I/O
37	A19	SA12	I/O
39	A20	SA11	I/O
41	A21	SA10	I/O
43	A22	SA9	I/O
45	A23	SA8	I/O
47	A24	SA7	I/O
49	A25	SA6	I/O
51	A26	SA5	I/O
53	A27	SA4	I/O
55	A28	SA3	I/O
57	A29	SA2	I/O
59	A30	SA1	I/O
61	A31	SA0	I/O

B Side

	I/O PIN	SIGNAL NAME	I/O
2	B1	GND	Ground
4	B2	RESET DRV	O
6	B3	+5 Vdc	Power
8	B4	IRQ9	I
10	B5	-5 Vdc	Power
12	B6	DRQ2	I
14	B7	-12 Vdc	Power
16	B8	OWS	I
18	B9	+12 Vdc	Power
20	B10	GND	Ground
22	B11	SMESW*	O
24	B12	SMEMR*	O
26	B13	IOW*	I/O
28	B14	IOR*	I/O
30	B15	DACK3*	O
32	B16	DRQ3	I
34	B17	DACK1*	O
36	B18	DRQ1	I
38	B19	REFRESH*	I/O
40	B20	CLK	O
42	B21	IRQ7	I
44	B22	IRQ6	I
46	B23	IRQ5	I
48	B24	IRQ4	I
50	B25	IRQ3	I
52	B26	DACK2*	O
54	B27	T/C	O
56	B28	BALE	O
58	B29	+5 Vdc	Power
60	B30	OSC	O
62	B31	GND	Ground

J9 PIGGYBACK CONNECTOR

I/O PIN	SIGNAL NAME	I/O
1	SBHE*	I/O
2	LA23	I/O
3	LA22	I/O
4	LA21	I/O
5	LA20	I/O
6	LA19	I/O
7	LA18	I/O
8	LA17	I/O
9	SD08	I/O
10	SD09	I/O
11	SD10	I/O
12	SD11	I/O
13	SD12	I/O
14	SD13	I/O
15	SD14	I/O
16	SD15	I/O
17	MEM CS16*	I/O
18	I/O CS16*	I/O
19	IRQ10	I/O
20	IRQ11	I/O
21	IRQ12	I/O
22	IRQ15	I/O
23	MASTER*	I/O
24	MEMR*	I/O
25	MEMW*	I/O
26	DACK5*	I/O
27	DRQ5	I/O
28	DACK6*	I/O
29	DRQ6	I/O
30	DACK7*	I/O
31	DRQ7	I/O

J2 FLOPPY DISK CONNECTOR PINOUT

PIN NUMBER	SIGNAL FLOW	SIGNAL
2	O	RPM/LC
4	-	N.C.
6	-	N.C.
8	I	INDEX*
10	O	MOTRENA*
12	O	DRIVESB*
14	O	DRIVESA*
16	O	MOTRENB*
18	O	DIRC*
20	O	STEP*
22	O	WRITE DATA*
24	O	WRITE ENABLE*
26	I	TRACK0*
28	I	WRITE PROTECT*
30	I	READ DATA*
32	O	HEAD SELECT*
34	I	DCHG
1-33 (ODD)	-	GND

J1 HARD DISK CONNECTOR PINOUT

PIN NUMBER	SIGNAL FLOW	SIGNAL
3	I/O	SD7
4	I/O	SD8
5	I/O	SD6
6	I/O	SD9
7	I/O	SD5
8	I/O	SD10
9	I/O	SD4
10	I/O	SD11
11	I/O	SD3
12	I/O	SD12
13	I/O	SD2
14	I/O	SD13
15	I/O	SD1
16	I/O	SD14
17	I/O	SD0
18	I/O	SD15
1	I	RST*
23	I	IOW*
25	I	IOR*
33	I	SA1
35	I	SA0
36	I	SA2
37	I	CS0*
38	I	CS1*
31	O	IRQ14
32	O	I/OCS16*
39	O	ACTIVE*
20	-	KEY (NOT CONNECTED)
21	-	RESERVED (NOT CONNECTED)
34	-	PDIAG
2,19,22,24 26,30,40	-	GND

LIMITED WARRANTY SECTION 8

TEKNOR INDUSTRIAL COMPUTERS INC. ("the seller") warrants its products to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise
If your TEKNOR product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (514) 437-5682 or in Germany at +49 811 / 600 15-0. Make certain you have the following at hand: the Teknor Invoice #, your Purchase Order #, and the Serial Number of the defective unit.

2) Give the serial number found on the back of the card and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA # and clearly mark this number on the outside of the package you are returning.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

6) When returning a TEKNOR card:

   i) Make certain that the card is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by TEKNOR):

TEKNOR INDUSTRIAL COMPUTERS INC.
616 Curé Boivin
Boisbriand, Quebec
J7G 2A7 CANADA

TEKNOR INDUSTRIAL COMPUTERS INC.
Zeppelin Str. 4
D-85399 Hallbergmoos
GERMANY

GETTING HELP SECTION 9

Need More Help?
At TEKNOR, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at

Canadian Headquarters
Tel: (514) 437-5682
Fax: (514) 437-8053

European Headquarters
Tel: +49 811 / 600 15-0
Fax: +49 811 / 600 15-33

If you have any questions about TEKNOR, our products or services, you may reach us at the above numbers or by writing to:

TEKNOR INDUSTRIAL COMPUTERS INC.
616 Curé Boivin
Boisbriand, Quebec
J7G 2A7 CANADA

TEKNOR INDUSTRIAL COMPUTERS INC.
Zeppelin Str. 4
D-85399 Hallbergmoos
GERMANY

RECOMMENDED DEVICES AND CONNECTORS

The following is a list of recommended devices and connectors for use on the TEK-AT4. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

DRAM (U13-U16)
DRAM devices with page mode at 70ns maximum access time are recommended for TEK-AT4 boards. For example:

MOSEL	V104BJ9S70	(256Kx9)
OKI	MSC2331A-70YS3	(256Kx9)
OKI	MSC2331B-70YS3	(256Kx9)
HITACHI	HB56G19B-7C (low prof.)	(1Mx9)
IBM	B1A10900A-70	(1Mx9)
MICRON	MT3D19M-7 (low prof.)	(1Mx9)
MOSEL	V104J97-70 (low prof.)	(1Mx9)
MOTOROLA	MCM91430S60	(1Mx9)
MOTOROLA	MCM91430S70	(1Mx9)
NEC	MC-421000A9BA-70	(1Mx9)
OKI	MKC23109B-70DS3	(1Mx9)
OKI	MSC23109-70DJ3	(1Mx9)
SAMSUNG	KMM591000AN-70	(1Mx9)
SAMSUNG	KMM591000BN-60	(1Mx9)
HITACHI	HB56AA49BR7B	(4Mx9)
OKI	MSC23409-70DS9	(4Mx9)
TI	TM4100EAD9-70	(4Mx9)
TI	TM497EU9-70	(4Mx9)

SRAM (U27, U31)
Static RAM CMOS memory with low power consumption for battery backup (no Pseudo-Static) with access time of 200ns, or better. Must be in DIP package. For example:

MITSUBISHI	MH12808NA-10	(128Kx8)
NEC	UPD431000ACZ-70LL	(128Kx8)
SAMSUNG	KM681000ALP-10	(128Kx8)
SAMSUNG	KM681000ALP-70	(128Kx8)
SAMSUNG	KM681000ALP-80	(128Kx8)
HITACHI	HM628512LP-10	(512Kx8)
HITACHI	HM628512LP-10SL	(512Kx8)
NEC	UPD434000CZ-10L	(512Kx8)
NEC	UPD434000CZ-10LL	(512Kx8)
SAMSUNG	KM684000ALP-10	(512Kx8)
SAMSUNG	KM684000ALP-L10	(512Kx8)
SONY	CXK584000P-10L	(512Kx8)
SONY	CXK584000P-10LL	(512Kx8)

INTERFACE CONNECTORS

The following connectors are recommended for interfacing with the I/O devices. The parts shown here do not have a strain relief but one may be added.

Connector	Recommended Mating Part
Hard Disk (J1)	Amp 746285-9 [499252-1*] Robinson Nugent IDS-C40PK-TG Thomas & Betts 622-4030 [622-4041*] (40-pin flat cable connector)
Floppy Disk (J2)	Amp 746285-8 [499252-6*] Robinson Nugent IDS-C34PK-TG Thomas & Betts 622-3430 [622-3441*] (34-pin flat cable connector)
Keyboard (J3)	Amp 746285-3 [499252-8*] Robinson Nugent IDS-C16PK-TG Thomas & Betts 622-1630 [622-1641*] (16-pin flat cable connector)
COM2 (J4)	Amp 746285-1 [499252-5*] Robinson Nugent IDS-C10PK-TG Thomas & Betts 622-1030 [622-1041*] (10-pin flat cable connector)

* optional Amp strain relief part in square brackets

Connector	Recommended Mating Part
Power Connector (J5)	Leoco 2530 S060013 (housing) Leoco 2533 TCB00A0 (crimp) Molex 22-01-1067 (housing) Molex 08-50-0114 (crimp)
COM1 (J6)	Amp 747318-4 <747275-4**> Amphenol 841-17-DEFR-B9P Robinson Nugent IDD-C9SM-440-TG30 Thomas & Betts 609-09S (9-pin flat cable connector)
LPT1 (J7)	Amp 747321-2 [747275-2*] Amphenol 841-17-DBFR-B25P Robinson Nugent IDD-C25PM-440-TG30 [SR-25M-IDD*] Thomas & Betts 609-25P (25-pin flat cable connector)
XT Header (J9)	Samtec ESQ131-12-G-D PCB-mount female connector

* optional Amp strain relief part in square brackets

** optional cable stabilizer part in angle brackets

INDEX