Model 960 Computer Communications Register Unit Manual

Part No. 966313-9701
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SECTION I

INTRODUCTION

This manual describes the Communication Register Unit (CRU) which is the serial Input/Output (I/O) channel of the Texas Instruments Model 960A and Model 960B Computers. This manual is separated into two parts: the first part describes CRU programming and interface modules; the second part explains CRU hardware implementation.

It is assumed throughout the manual that the reader is familiar with the concepts explained in the Model 960A System Description Manual (TI Part No. 226750-9701) or the Model 960B System Description Manual (TI Part No. 942773-9701), and the Model 960 Basic Programming Guide (TI Part No. 955378-9701).

Detailed maintenance information, including parts lists and assembly drawings for all CRU components, may be obtained by purchasing the Model 960 Maintenance Manual, Volume IV (TI Part No. 226750-9704).

Complete programming and electrical information for each CRU module and system peripheral that is attached to the modules is included in the appropriate User's Manual. Available User's Manuals are identified and listed in table 1-1 with the corresponding TI Part Numbers.

Table 1-1. CRU Module and System Peripheral User's Manuals

Module or Peripheral Hardware	TI Manual Number
16 In/16 Out Data Module	966366-9701
32 In Data Module	966367-9701
32 Out Data Module	966368-9701
Contactor Data Module	966369-9701
Interrupt Module	966373-9701
A/D Converter Module	966371-9701
D/A Converter Module	966372-9701
Interval Timer Module	966374-9701
Full Duplex Communications Module	966375-9701
Teletypewriter	966314-9701
Card Reader	966316-9701
Video Terminal	966318-9701
Paper Tape Reader	965940-9701
Paper Tape Punch	965934-9701
Analog Systems	964580-9701
Silent 700 Terminals	959227-9701

SECTION II

OPERATION

2.1 GENERAL

The Communication Register Unit (CRU) is a line-oriented input-output (I/O) channel. The output function of this channel is to set a selected CRU output line to a logic ONE or ZERO, or to output a field of bits from a memory location to a set of consecutive CRU output lines. The CRU input function is to read the logic level on a selected CRU input line into the computer, or to read information on a set of consecutive CRU input lines into a memory location.

In the fully expanded configuration, the CRU channel provides 4,096 output lines and 4,096 input lines. The CRU lines are selected by a 12-bit address that is generated by the computer. Each address selects one input line and one output line. The input or output to a given line address is controlled by the executed instruction.

The CRU channel consists of one CRU interface printed circuit (PC) board and from one to sixteen CRU module printed circuit boards that are installed in the computer mainframe as illustrated in figure 2-1. In addition, an expanded CRU system includes one or more CRU expansion units external to the computer mainframe. Up to 16 CRU modules are installed in each expansion unit.

All CRU input and output lines are physically implemented on the CRU modules.

2.1.1 CRU INSTRUCTIONS

The CRU channel is activated by six computer instructions. Each CRU instruction is described below with the aid of a simplified block diagram to illustrate CRU channel operation. Operation of circuits within the CRU channel is described in greater detail in Section III.

Figure 2-2 shows the major Central Processor Unit and CRU channel hardware items involved in the execution of a CRU instruction.

2.1.1.1 LOAD CRU (LDCR). The LDCR instruction causes a field of data, 1 to 16 bits in length, located in a memory location to be output to consecutive CRU lines. The 32-bit instruction word contains fields from which the data source address and the beginning CRU output address are calculated. Another instruction word field specifies the number of bits to be output.

In the LDCR instruction, the output data field is transferred serially to the CRU channel. The Central Processor Unit (CPU) calculates the 12-bit address of the first CRU line using the contents of CPU Register 7 (either mode)

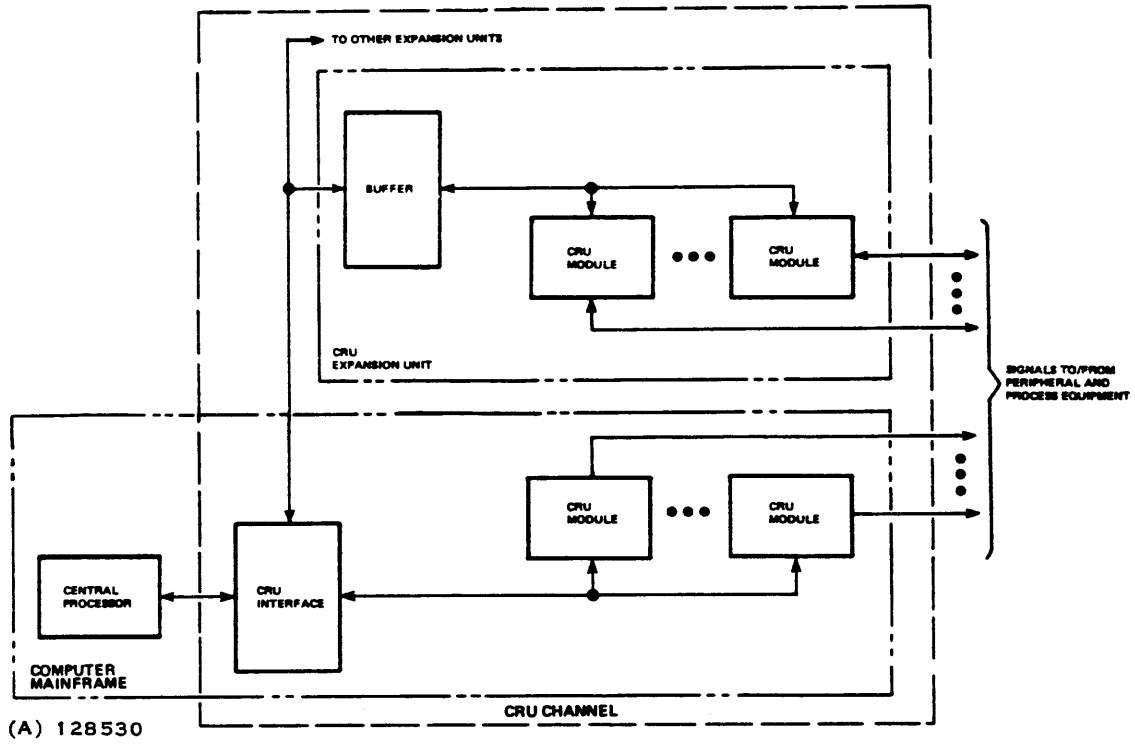

Figure 2-1. CRU Channel System Functional Diagram

and a 10-bit field from the instruction word. This address is stored in the 12 Least Significant Bits (LSB) of the CRU Address Register (CA); i.e., CA bits 4 through 15. The data is fetched from the memory address specified by the contents of CPU Register 4 and another 10-bit field from the instruction. It is stored in the Shift Register (SR). Neither CA nor SR is a program addressable register.

The module select decoder on the CRU interface board is enabled by a code in the most significant four bits (CA04-CA07) of the CRU address. Address bits CA08 through CA11 are decoded to generate one of 16 module select signals. The module select signal enables the line address decoder on the CRU module. The line address decoder generates one of 16 enable signals for the storage flip-flop clocks. The clock input to these gates is generated by gating the system clock with ROM40. ROM40 is an output from the CPU control read-only memory which is true during a CRU output operation.

The CRU module contains 16 output storage flip-flops to which the least significant bit (LSB) of the SR is applied as a data input. The flip-flops are clocked by the gated clocks that are described above.

At the end of a clock signal period, SR bit 15 is clocked into the selected flip-flop, the SR is shifted right one position, and the CA is incremented. At the end of the next clock period, the line address decoder enables a clock

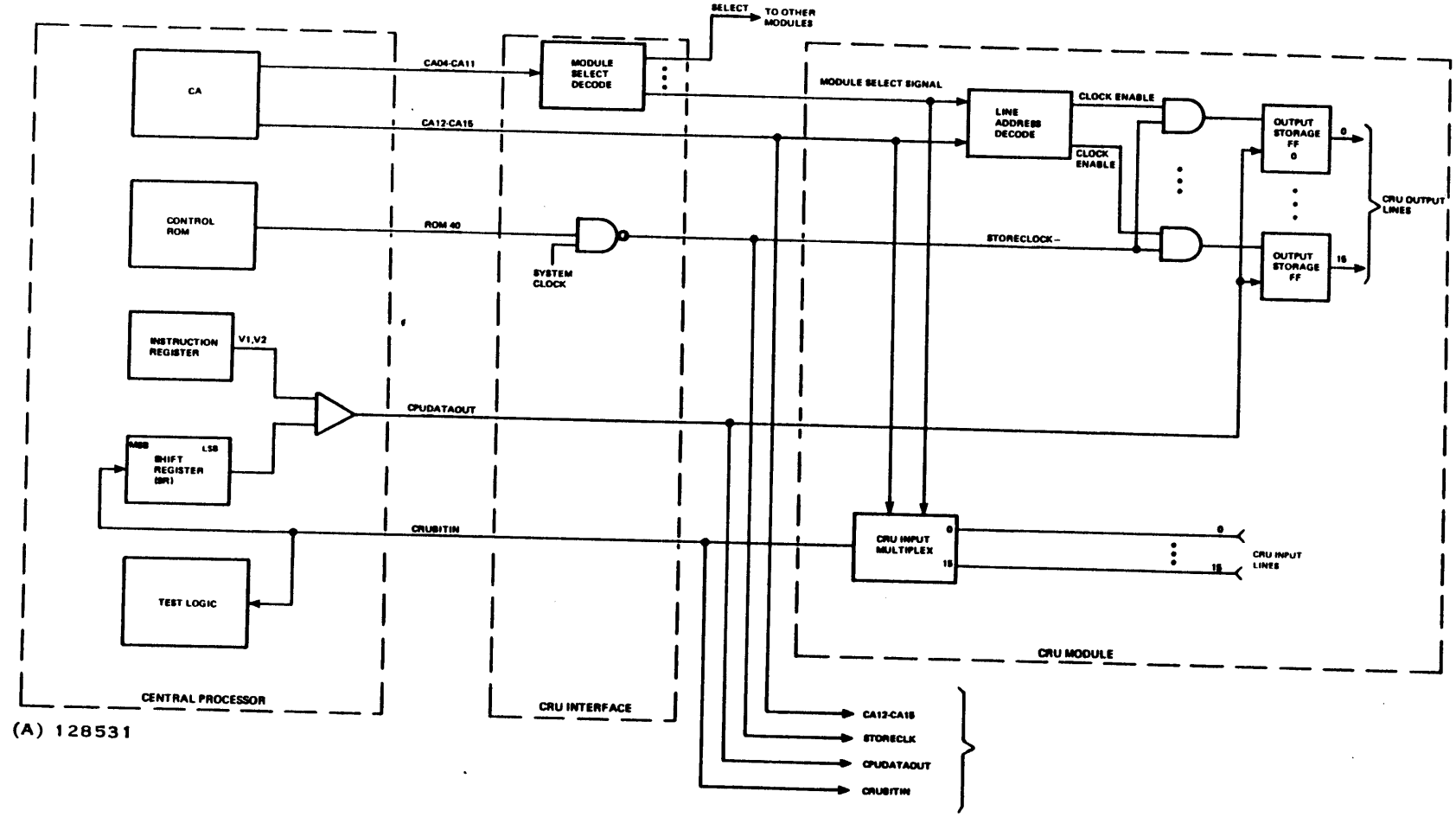

Figure 2-2. CRU Channel Functional Diagram

to the next output flip-flop in sequence and it is loaded with the content of SR bit 15. This process continues until the entire data field is loaded in consecutive storage flip-flops. The outputs of the storage flip-flops are the CRU output lines. The number of bits in the data field is determined by a 4-bit field in the instruction.

Figure 2-3 illustrates the transfer of a 10-bit field from memory to field of CRU output lines.

2.1.1.2 STORE CRU (STCR). The STCR instruction causes the information present on a group of 1 to 16 consecutive CRU input lines to be transferred to the CPU and stored, justified right in a memory location. The instruction word contains fields specifying the starting CRU line address, the storage location, and the number of bits to be transferred.

The CRU interface module select decoder functions as described for the LDCR instruction. The CRU input multiplexer in the CRU module is enabled by the module select signal and addressed by CA12 through CA15. Thus, the first CRU input line is selected through the multiplexer and routed to the most significant bit input of the SR. At the end of each clock period the CA is incremented causing the next input in sequence to be enabled through the multiplexer, and the SR is shifted right one position. This process continues until the specified number of bits has been loaded into the leftmost bits of the SR. If the transferred number of bits is less than 16, the CRU input to the SR is inhibited and the SR shifts right, always forcing the serial input to be the MSB, until the input data is justified right with the sign bit of the original field extended. The contents of the SR is then stored in the specified register or memory location under program control. During an STCR instruction, both the line address decoder and the input multiplexer in the CRU module are enabled. However, the output storage flip-flops are not clocked because the output clock enable signal (ROM40) is false during a store operation.

Figure 2-4 illustrates the transfer of an 8-bit field from a set of CRU input lines to a memory location.

2.1.1.3 SET BIT (SETB). The SETB instruction word contains a field which specifies a CRU output line and a bit (V1) which contains a value to be transferred to the addressed output. When this instruction is executed, the CRU channel operates as described for the LDCR instruction except that V1, rather than SR bit 15, is selected to the CPU DATAOUT line and only the one bit is transferred.

2.1.1.4 TEST INPUT BIT AND SET OUTPUT BIT OR SWITCH MODES (TSBX). The TSBX instruction word contains fields specifying a CRU input line and a CRU output line, a comparison bit (V1), and an output bit (V2). Execution of this instruction causes the value on the selected input line to be

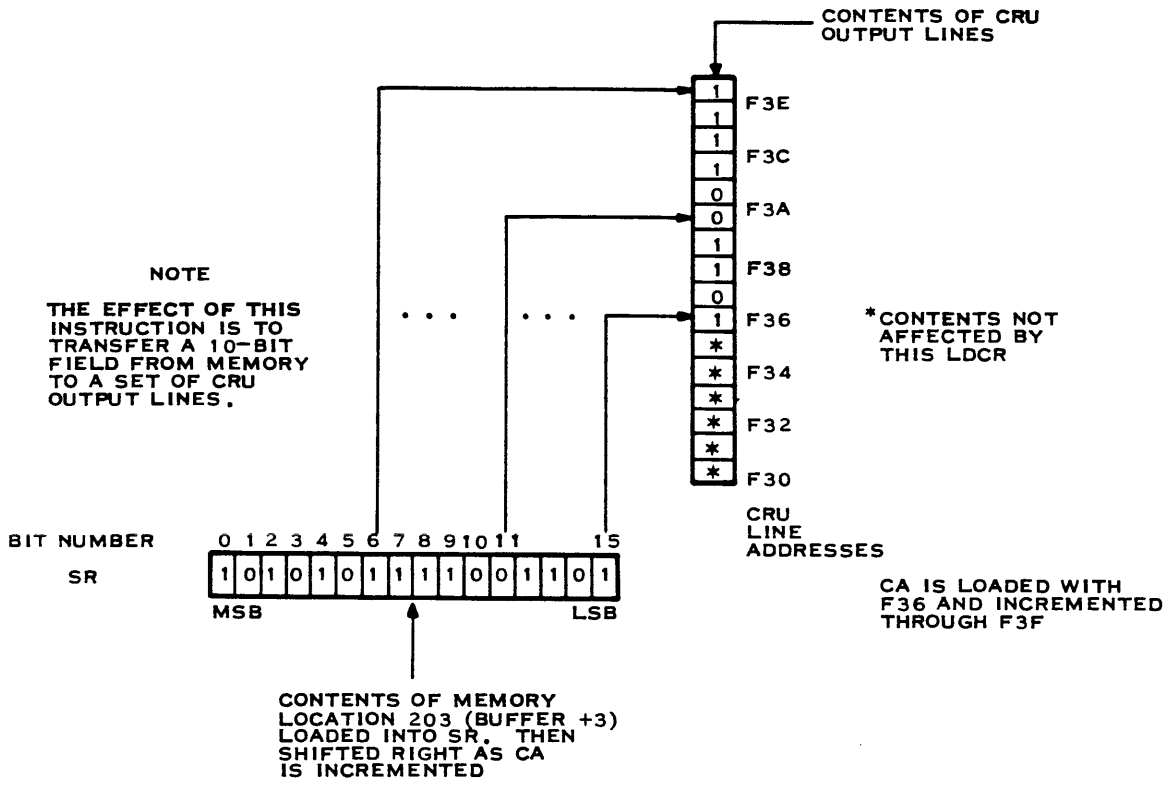

Figure 2-3. Load CRU Instruction

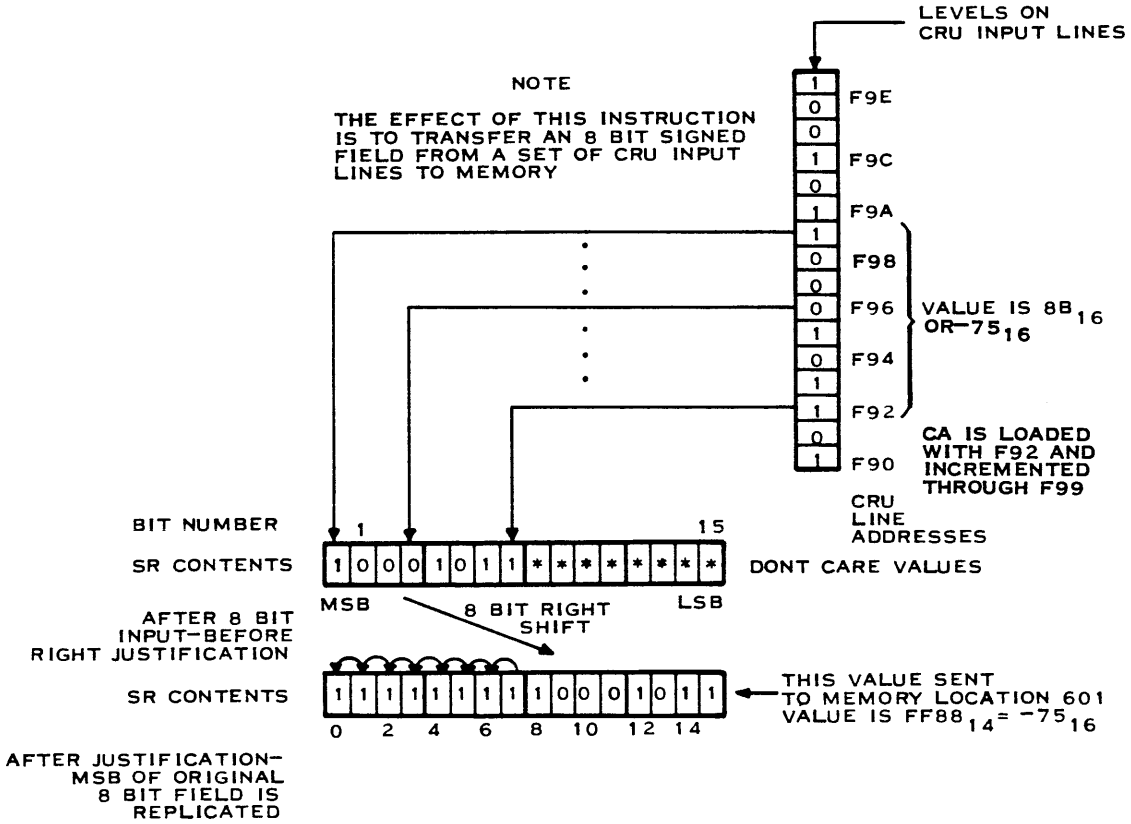

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Figure 2-4. Store CRU Instruction

compared to V1. If the test fails, a program mode change is forced. If the test succeeds, the value stored in V2 is transferred to the specified CRU output line.

2.1.1.5 SWITCH MODES IF BIT NOT EQUAL (XBNE). The XBNE instruction word contains a CRU input line address field and a comparison bit (V1). The specified CRU input line is read into the CPU and compared to V1. If the comparison fails, a program mode change is forced.

2.1.1.6 BRANCH IF BIT NOT EQUAL (BBNE). The BBNE instruction word contains fields which specify a CRU input line address, a program branch address, and a comparison bit (V1). The data on the specified CRU input line is read into the CPU and compared to V1. If the comparison fails, the branch is executed. The branch address is the contents of register 5 added to a 10-bit field from the instruction.

2.1.2 INTERRUPTS

Some CRU modules have interrupt capability. Figure 2-5 shows in simplified form how two of the output storage flip-flops in a CRU module can be connected for interrupt and mask storage.

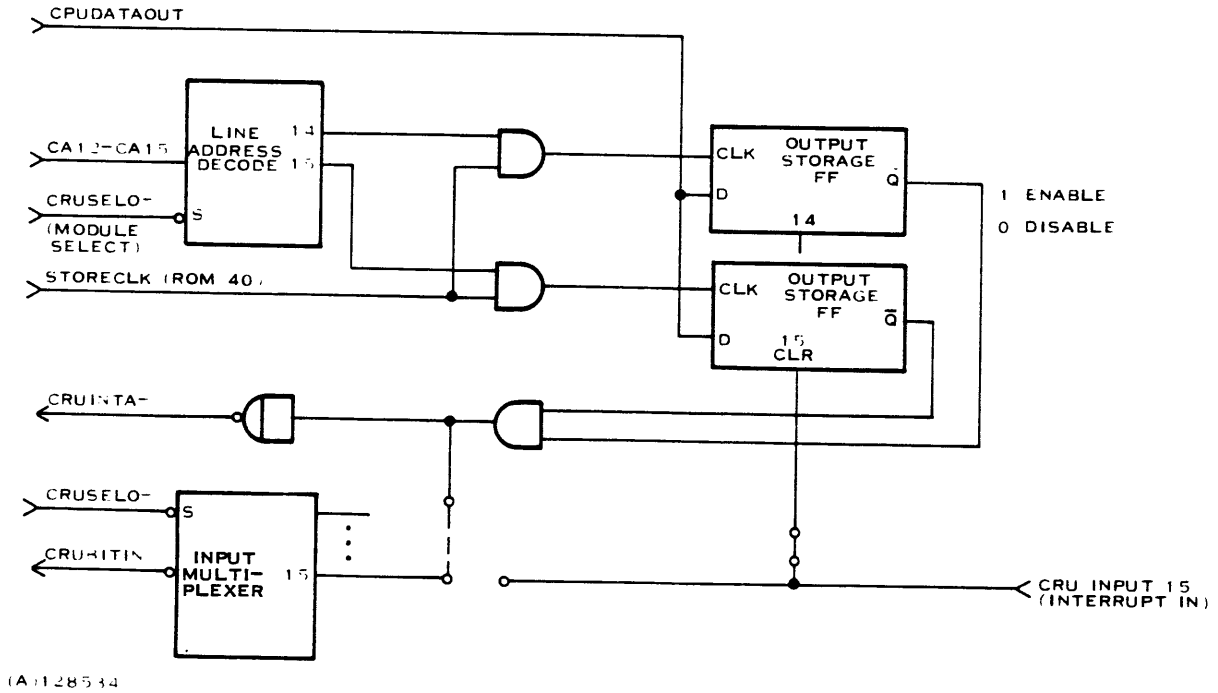


Figure 2-5. CRU Module Interrupt and Mask

The CRU input line 15 is disconnected from the input multiplexer and connected to the clear input of output storage flip-flop 15. The outputs of flip-flops 14 and 15 are gated together. Thus, flip-flop 14 serves as a mask for the interrupt flip-flop.

For a CRU interrupt to be enabled, the mask must be set by a CRU output instruction. Then, when an interrupt condition occurs on CRU input line 15, the interrupt flip-flop is set. Thus, interrupt signal (CRUINTA) to the CPU goes low. The CRUINTA- signal is bussed to all CRU modules in the system. The true interrupt signal that is generated by the mask gate is connected to input 15 of the input multiplexer. To determine the source of a CRU interrupt, instructions must be executed to test CRU input lines serving as interrupts.

The interrupt flip-flop may also be set under program control by executing a CRU output instruction. Once the interrupt flip-flop has been set to the interrupt state, the interrupt can be cleared only be executing a CRU output instruction.

A CRU interrupt module is available with 16 storage flip-flops. This configuration is implemented as 8 interrupt storage flip-flops and 8 masks.

2.1.3 CRU SIGNAL DISTRIBUTION

As described in paragraph 2.1.1, a discrete module select signal is generated for each CRU module in a system. All other CRU module inputs and outputs are bussed in parallel to all modules in the system. The module interrupt and data output signals are generated by open collector gates. The data output gate is enabled only on a selected module, while the data output gate of all other modules remains high.

The interrupt output gates are not gated with the module select signal; therefore, an interrupt or one or more modules will pull the CRUINTA- line low.

2.2 CRU MODULES

This section introduces the currently available CRU modules and describes the functional characteristics of each module with brief programming examples. Further detail is included in the Texas Instruments' User's Manuals which are listed in Section I of this manual.

All CRU modules have an 80-pin bottom edge connector tab which plugs into the mainframe or into a CRU expansion unit. This connection completes the interface to the address, data, clock, and interrupt signals which are processed to and from the CPU. A 72-pin top edge connector tab on the module is connected to a cable to complete the interface to peripheral or process equipment. An unwired connector that plugs to the top edge of the module is available as TI Part No. 217081-0001. See figure 2-6 for pin nomenclature.

MODULE SOLDER SIDE

36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
$\overline{R}$	$\overline{P}$	$\overline{N}$	$\overline{M}$	$\overline{L}$	$\overline{K}$	$\overline{J}$	$\overline{H}$	$\overline{F}$	$\overline{E}$	$\overline{D}$	$\overline{C}$	$\overline{B}$	$\overline{A}$	Z	Y	X	W	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A

MODULE COMPONENT SIDE

CONNECTOR: PART NUMBER 231447-0800 (VIKING PART NUMBER 2VH-36/1CN-5)

HOOD: TI PART NUMBER 214080-0001

(A) 128536

Figure 2-6. Connector Kit (TI Part No. 217081-0001) Pin Assignment

The basic type of CRU module (data module) provides output storage flip-flops and/or buffered input circuits to the input multiplexer. Other module types contain additional circuitry which perform signal conversion. Each module is described in separate paragraphs which follow.

2.2.1 DATA MODULE, 16 INPUT/16 OUTPUT (TI PART NUMBER 214103)

This module provides two-way communication between the Communications Register Unit (CRU) and devices or transducers which are operated by, or generate discrete (on-off) control signals. The module (circuit board) may be plugged into any CRU port in the CPU chassis or any port in a CRU Expansion Unit.

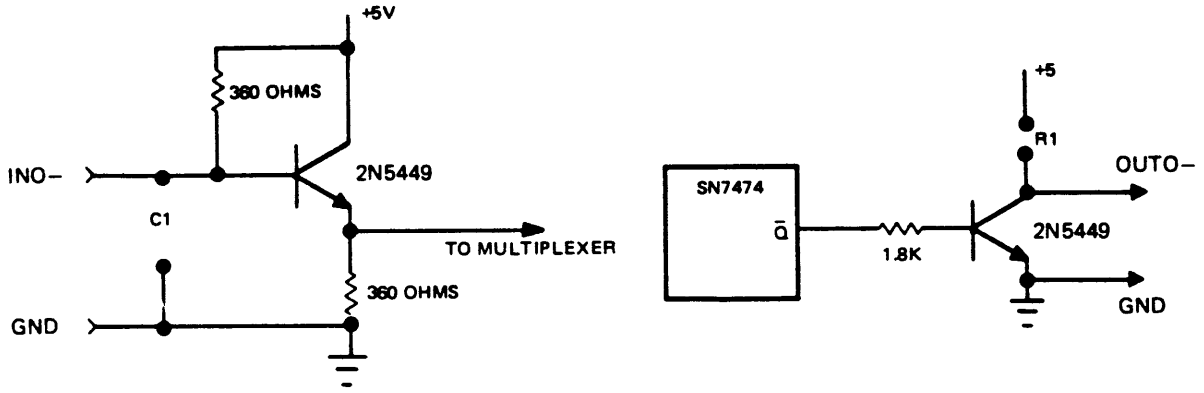
A data module provides 16 inputs and 16 outputs. Each line (input or output) can be addressed as a single independent line, or as a member of a group of lines. Each output circuit contains a storage flip-flop that maintains the output until changed by the CPU. An alternate version of the data module is available which provides 15 normal input channels, 14 output channels, one interrupt mask, and one interrupt input channel.

2.2.1.1 SPECIFICATIONS. Specifications for this data module are listed in table 2-1.

2.2.1.2 INTERFACE. The inputs and outputs are negative logic levels switching between 0 volts and a positive voltage. (See figure 2-7.) For each flip-flop buffered output, an open-collector output transistor is provided. The collector can be attached to an external pull-up resistor and power supply (up to 30 volts and 50 milliamperes) or resistors can be placed on the module itself for +5-volt output level. The inputs are to the base of emitter-follower transistors which operate at TTL levels. Filter capacitor pads for each input are provided on the module.

Table 2-1. Data Module (16 Input/16 Output) Specifications

Characteristic	Specification
Inputs(16):	0V to 1.0V = Logic ONE 3.0V to 5.0V = Logic ZERO
Outputs(16):	0V to 0.4V = Logic ONE Open = Logic ZERO
Option:	15 inputs, 1 interrupt input 14 outputs, 1 interrupt mask, 1 interrupt clear
Power Requirements:	+5.0 Vdc @ 0.5A



INPUT

C1 DESIGNATES PADS FOR SMALL FILTER CAPACITOR, IF REQUIRED.

OUTPUT

R1 DESIGNATES PADS FOR COLLECTOR RESISTOR.

(A) 128535

Figure 2-7. Data Module Input and Output Buffers

An option allows the 16th input to be an interrupt. Jumper options allow this interrupt to be turned on by a ONE level, a ZERO level, or by a positive or negative level transition. This same option provides an output line as an interrupt mask, controlled by the computer.

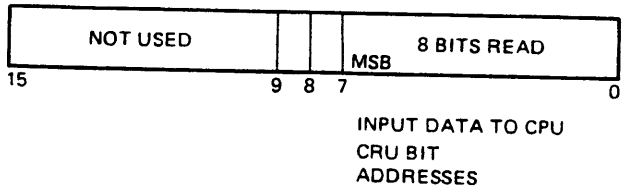
Connections to the input or output lines are completed through an edge connector with pin assignments as listed in table 2-2.

Table 2-2. CRU Bit Functions for the Data Module

CRU Output Bit Address*	Function	Pin Assignment OUT-/GND	CRU Input Bit Address*	Function	Pin Assignment IN-/GND
0	General-purpose output lines	$\overline{L}/\overline{K}$	0	General-purpose input lines	$\overline{M}/\overline{N}$
1		$\overline{F}/\overline{E}$	1		$\overline{H}/\overline{J}$
2		$\overline{B}/\overline{A}$	2		$\overline{C}/\overline{D}$
3		X/W	3		Y/Z
4		T/S	4		U/V
5		N/M	5		P/R
6		J/H	6		K/L
7		D/C	7		E/F
8		32/31	8		33/34
9		28/27	9		29/30
10		24/23	10		25/26
11		20/19	11		21/22
12		16/15	12		17/18
13		12/11	13		13/14
14	General output or interrupt mask FF	8/7	14		9/10
15	General output or interrupt FF	4/3	15	General input or interrupt input	5/6

*Add the CRU port address for actual program address.

2.2.1.3 PROGRAMMING. The data module is the standard interface for paper tape readers and punches, line printers, and analog systems. Additionally the data module is part of many special purpose digital interfaces. Programming methods used on the data module are as diverse as the devices it is used with. As an example, consider the paper tape reader interface that is described as follows:



Input bits 0-7 are the data currently being read (ONE = hole; ZERO = no hole). Input bit 8 is character present (ONE = present; ZERO = not present). Input bit 9 is unit ready (ONE = ready; ZERO = not ready).

Bit values 1 and 0 represent data as contained in memory.

Only one output is used, bit 0. The data line associated with bit 0 must be normally 3 to 5 volts. The reader is advanced one character by generating a pulse on that data line of 0-0.4 volts for a minimum of 10 microseconds.

```
READIN    L      7, CRUA       Assume location CRUA contains
                                CRU address of reader
          LA     4, BUF        Location of BUF in Register 4
          LA     5, READIN     Set up Program Base Register -
                                necessary for BBNE's
          L      0, N          Get number of characters to be
                                read in Register 0

LOOP      BBNE   9, 1, LOOP    Wait for Reader Ready
          SETB   0, 1          Cause output 0 to be 0 volts
          NOP                  Delay of about 3 microseconds
          SETB   0, 0          Cause output 0 to be 5 volts
          BBNE   8, 0, $       Wait for current character to go
                                away
          BBNE   8, 1, $       Wait for new character
          STCR   (0, 8), 0     Put character in memory
          AA     4, 1          Increment pointer to BUF
          ARB    -1, LOOP, 0   Decrement loop counter and
                                branch if not finished.
            |        |
            v        v
          Through Remainder of Program
```

The preceding sequence identifies the most direct program for reading N characters from reader storage into memory one per word starting at location BUF. The following sequence causes a pulse of approximately 10 microseconds:

```
SETB   8, 1
NOP
SETB   8, 0
```

If longer pulses were required, a timing loop could be used.

In many programming situations it would be undesirable to wait for the character to appear, as this time amounts to many milliseconds. In such cases, the character present signal could be used to initiate a CRU interrupt and more sophisticated programs would be required to service the interrupt and execute the routine that reads data from the paper tape.

If the data module is used with the interrupt option, the instruction SETB 14, 1 enables input 15 to initiate an interrupt. The instruction SETB 14, 0 masks any such interrupt. Output flip-flop 14 is used as the interrupt on the data module. Output flip-flop 15 is used to retain the interrupt indication when the interrupt signal is a short pulse. This flip-flop may be cleared by a SETB 15, 0 or set by a SETB 15, 1. In both of these examples, the bit value for address 14 and 15 is important rather than the instruction SETB. An LDCR applying these values to 14 and 15 would serve as well.

2.2.2 DATA MODULE, 32 INPUT (TI PART NUMBER 217382)

This module provides 32 input data lines for one-way communication between the computer and devices or transducers which generate discrete (ON-OFF) signals. Each line can be addressed as a single line or as a member of group of lines. The input data module is particularly effective for use in applications where the number of input lines exceeds the number of output lines. Like the 16 I/O data module, this module may be plugged into any CRU port in the CPU chassis or any port in a CRU expansion unit.

2.2.2.1 SPECIFICATIONS. Specifications for this data module are listed in table 2-3.

Table 2-3. Data Module (32 Input) Specifications

Characteristic	Specification
Inputs(32):	0V to 1.0V = Logic ONE +3.0V to +5.0V = Logic ZERO
Power Requirements:	+5.0 Vdc @ 0.7A

2.2.2.2 INTERFACE. The inputs are negative logic TTL levels. (See figure 2-7.) An emitter-follower input circuit is used to increase noise margin. Connections to the input lines can be made through an edge connector. The pin assignments are listed in table 2-4.

2.2.2.3 PROGRAMMING. This module is addressable as two sets of 16-input lines. The addresses of each set are separated by 100_{16}. This is further explained in the theory of operation section of this manual.

Table 2-4. CRU Bit Functions for the 32 Input Module

CRU Input Bit Address*	Function	Pin Assignments IN-/GND
0	16 General-purpose input lines	0 3/C
1		1 4/D
•		2 5/E
•		3 6/F
•		4 7/H
•		5 8/J
•		6 9/K
•		7 10/L
•		8 11/M
•		9 12/N
•		10 13/P
•		11 14/R
•		12 15/S
•		13 16/T
•		14 17/U
15		15 18/V
256	16 More general-purpose input lines	16 19/W
257		17 20/X
•		18 21/Y
•		19 22/Z
•		20 23/$\overline{A}$
•		21 24/$\overline{B}$
•		22 25/$\overline{C}$
•		23 26/$\overline{D}$
•		24 27/$\overline{E}$
•		25 28/$\overline{F}$
•		26 29/$\overline{H}$
•		27 30/$\overline{J}$
•		28 31/$\overline{K}$
•		29 32/$\overline{L}$
•		30 33/$\overline{M}$
271		31 34/$\overline{N}$

*Add the CRU port address for actual program address.

2.2.3 DATA MODULE, 32 OUTPUT (TI PART NUMBER 217380)

This module provides 32 output data lines for one-way communication between the computer and devices or transducers which are operated by discrete (ON-OFF) signals. Each line can be addressed as a single independent line or as a member of a group of lines. The output data module is particularly effective in applications where the number of output lines exceeds the number of input lines. Like the 16 I/O data module, each output circuit contains a storage flip-flop that maintains the output until changed by the CPU.

This module may be plugged into any CRU port in the CPU chassis or any port in a CRU expansion unit.

2.2.3.1 SPECIFICATIONS. Specifications for this data module are listed in table 2-5.

Table 2-5. Data Module (32 Output) Specifications

Characteristic	Specification
Outputs (32):	0.0V to 0.4V = Logic ONE Open = Logic ZERO
Options:	Collector Resistors to +5.0 Vdc on Module or up to +30 V External Supply
Power Requirements:	+5.0 Vdc @ 0.7A

2.2.3.2 INTERFACE. The data module outputs are negative logic levels switching between 0 volts and a positive voltage. Each output line is driven by a transistor switching circuit which is controlled by its corresponding storage flip-flop. (See figure 2-7.) The circuit is capable of sinking up to 50 milliamps and holding off up to +30 Volts dc. An 0.25W resistor on the module can be inserted between the individual transistor collector output and a supply voltage +5V (or a customer supply of up to +30V). Connections to the output lines can be made through an edge connector. The pin assignments are listed in table 2-6.

2.2.3.3 PROGRAMMING. This module contains two 16-bit output registers. The addresses for each set are separated by 100_{16}. This addressing scheme is explained in the theory of operation section of this manual.

2.2.4 DATA MODULE CONTACTOR (TI PART NUMBER 214111)

This module provides two-way communication between the computer and external relay-controlled devices. Isolated relay contacts are used for outputs. Isolated relay coils are used for inputs. There are eight inputs and eight outputs, each of which may be addressed as a single independent line, or as a member of a group of lines. Each output circuit contains a storage flip-flop that maintains the output until changed by the CPU. The module may be plugged into any CRU port; however, the module is thicker than a normal module. Therefore, this module should be used in a high profile CRU port.

2.2.4.1 SPECIFICATIONS. Specifications for this data module are listed in table 2-7.

Table 2-6. CRU Bit Functions for the 32 Output Module

CRU Output Bit Address*	Function	Pin Assignments OUT-/GND
0	16 General-purpose output lines	3/C
1		4/D
•		5/G
•		6/F
•		7/H
•		8/J
•		9/K
•		10/L
•		11/M
•		12/N
•		13/P
•		14/R
•		15/S
•		16/T
•		17/U
•		18/V
15		19/W
256	16 More general-purpose output lines	20/X
257		21/Y
•		22/Z
•		23/$\overline{A}$
•		24/$\overline{B}$
•		25/$\overline{C}$
•		26/$\overline{D}$
•		27/$\overline{E}$
•		28/$\overline{F}$
•		29/$\overline{H}$
•		30/$\overline{J}$
•		31/$\overline{K}$
•		32/$\overline{L}$
•		33/$\overline{M}$
•		34/$\overline{N}$
271		

*Add the CRU port address for actual program address.

Table 2-7. Data Module Contactor Specifications

Characteristic	Specification
Inputs (8):	TRUE data is +4.5V to +6.0V across 200 OHM Coil
Outputs (8):	SPST contact, 250 Vdc maximum, 3A maximum
Power Requirements:	+5.0 Vdc @ 0.5A

2.2.4.2 INTERFACE. Isolated relay coils are used for inputs. A logic ONE is represented by 30 mA current and a logic ZERO represents no current. The input relays have operate and release times of approximately 1.0 millisecond and 0.85 millisecond, respectively. A diode is placed in parallel with each coil to protect the drive circuitry.

The outputs are used to drive external devices through isolated contacts. These output contacts are capable of handling 50 Watts at 250 Vdc maximum or current switched at 3.0 Amperes maximum. The approximate operate and release times for these output contacts are 3.0 milliseconds and 1.3 milliseconds, respectively. Each output is one SPST relay contact with a logic ONE closing the contact. Connections between the input/output relays and external devices can be made through an edge connector. Pin assignments are listed in table 2-8.

Table 2-8. CRU Bit Functions for the Contactor Module

CRU Output Bit Address*	Function	Pin Assignment OUT/RTN	CRU Input Bit Address*	Function	Pin Assignment IN/RTN**
0	8 General-purpose output contacts	$\overline{L}/\overline{K}$	0	8 General-purpose isolated inputs	$\overline{M}/\overline{N}$
1		$\overline{F}/\overline{E}$	1		$\overline{H}/\overline{J}$
•		$\overline{B}/\overline{A}$	•		$\overline{C}/\overline{D}$
•		X/W	•		Y/Z
7		T/S	7		U/V
8	Not Used	N/M	8	Not Used	P/R
•		J/H	•		K/L
•		D/C	•		E/F
•			•		
15			15		

*Add the CRU port address for actual program address.
**IN must be positive with respect to RTN

2.2.5 EIA DATA MODULE (TI PART NUMBER 966630)

The EIA data module provides a general-purpose 16-bit input and output interface between the CPU and external devices using interface levels that are compatible with EIA Standard RS232C. An output register is provided to hold the output data. The output registers only change on programmed instruction, and are not subject to the CPU master reset. Input data is not stored in register; therefore, the data sense during the time of interrogation will be stored in memory.

2.2.5.1 SPECIFICATIONS. Specifications for the EIA data module are listed in table 2-9.

Table 2-9. EIA Data Module Specifications

Characteristics	Specifications
Input Signal Levels:	±25V absolute maximum ±15V recommended maximum ±3V minimum
Output Signal Levels:	±8V typical ±5V minimum
Signal Polarity from Device:	Negative voltage equals a memory logic ONE Positive voltage equals a memory logic ZERO
Power Requirements:	+5Vdc @ 0.34A +15Vdc @ 0.11A - 15Vdc @ 0.07A

2.2.5.2 INTERFACE. See figure 2-8 for pin assignments.

2.2.5.3 PROGRAMMING. The EIA data module is used in the same manner as the 16-input/output data module. Programming details are included in paragraph 2.2.1.3.

2.2.6 INTERVAL TIME MODULE (TI PART NUMBER 214114)

The interval timer module accepts a 14-bit binary number from the computer and counts it down to zero in pre-selected (1, 2, 4, or 8 milliseconds) time increments. An interval timer module is required when using the Process Automation Monitors (PAM and PAM/D). Normally, one timer module is sufficient for all time interval measurements in a process control application. The interval timer module plugs into any CRU port.

2.2.6.1 SPECIFICATIONS. Specifications for the interval timer module are listed in table 2-10.

2.2.6.2 INTERFACE. Normally external connections to the module are not made. The time increments are generated by dividing a 4096 KHz crystal oscillator. All submultiples of this clock, 1.024 μs to 8 ms, are available at the top edge of the module. The input to the counter is also available there. Since the standard system software expects count intervals of 1.0 ms, this additional flexibility is only useful in special applications. The standard count intervals may be selected with wire jumpers on the component side of the module as follows:

1 ms E3-E5	4 ms E2-E5
2 ms E4-E5	8 ms E1-E5

	Memory Data	Output Register Bit Address	Signature	Interface Connector Pin
(MSB)	0	F	OUT 15-	B
	1	E	OUT 14-	C
	2	D	OUT 13-	F
	3	C	OUT 12-	H
	4	B	OUT 11-	L
	5	A	OUT 10-	M
	6	9	OUT 9-	X
	7	8	OUT 8-	Y
	8	7	OUT 7-	P
	9	6	OUT 6-	N
	A	5	OUT 5-	K
	B	4	OUT 4-	J
	C	3	OUT 3-	E
	D	2	OUT 2-	D
	E	1	OUT 1-	A
(LSB)	F	0	OUT 0-	Z

	Memory Data	Input Bus Bit Address	Signature	Interface Connector Pin
(MSB)	0	F	IN 15-	14
	1	E	IN 14-	P
	2	D	IN 13-	13
	3	C	IN 12-	N
	4	B	IN 11-	8
	5	A	IN 10-	H
	6	9	IN 9-	7
	7	8	IN 8-	F
	8	7	IN 7-	C
	9	6	IN 6-	3
	A	5	IN 5-	B
	B	4	IN 4-	2
	C	3	IN 3-	E
	D	2	IN 2-	5
	E	1	IN 1-	D
(LSB)	F	0	IN 0-	4

(A) 128537

Figure 2-8. CRU Bit Functions for EIA Data Module

Table 2-10. Interval Timer Module Specifications

Characteristic	Specification
Resolution:	1, 2, 4, or 8 milliseconds (selected by wire jumper)
Maximum Count:	16,384 time increments
Interrupt:	At count = 0 timer causes interrupt, but continues to count negative to prevent any loss of real-time due to interrupt servicing by the computer.
Maximum Time Interval Measured:	Unlimited. Software can reset the timer periodically to keep time indefinitely.
Power Requirements:	+5.0 Vdc @ 0.5A

E1, E2, E3, E4, E5 are terminals staked to the board.

2.2.6.3 PROGRAMMING. The program-addressable input and output functions of the interval timer are listed in table 2-11 with applicable line addresses. The 14-bit initialization value may be transferred at any time. This 14-bit value immediately displaces the current counter contents. The CRU address assignment is such that the least significant bit (LSB) in the memory word VALUE selected by the instruction LDCR (1, 14), VALUE is considered to be the LSB of the count value. Similarly, the current counter contents ("Dynamic Count") may be read at any time with the LSB of the counter being the LSB in memory. This means that after the two instructions [LDCR (1, 14), VALUE and STCR (1, 15), COUNT] are executed, VALUE and COUNT will contain the same number. Fifteen bits are read in order that the last bit (15) will be zero, giving a 14-bit positive value in memory (memory bits 0, 1 = 0).

Table 2-11. CRU Bit Functions for the Interval Timer

CRU Output Bit Address*	Function	CRU Input Bit Address*	Function
0	0 = Clear Interrupt	0	Timer Interrupt Status: 1 = Interrupt
1	14-Bit Count Initialization Value from CPU – Bit 1 is LSB	1	14-Bit Dynamic Count – Bit 1 is LSB
•		•	
•		•	
•		•	
•		•	
14		14	
15	1/0 = Start/Stop Control	15	Not used – Always = 0

*Add the CRU port address for actual program address.

When the counter contains a count of ZERO, a CRU interrupt is generated. There is no mask for this interrupt on the module. The interrupt can be cleared by a SETB 0, 0 only if the counter is non-ZERO. The interrupt can also be set independent of the counter by a SETB 0, 1. The counter continues to decrement past zero in order to lose no count intervals. In real-time applications, this allows the program to determine how many count intervals have passed since the interrupt was generated.

2.2.7 INTERRUPT MODULE (TI PART NUMBER 214087)

The interrupt module may be used in any CRU port to provide 8 interrupt flip-flops and 8 mask flip-flops. Additional modules may be used to provide up to 2048 interrupts (one module in every available CRU slot). Interrupt lines can be masked out individually (or in groups) by the computer to disable selected interrupts. When any unmasked interrupt line comes True (i.e., 0 Volts), the computer receives a CRU interrupt and can scan the interrupt lines to determine which interrupt has occurred.

NOTE

Each 16 I/O data module also has the capability of providing a single interrupt line and mask.

2.2.7.1 SPECIFICATIONS. Specifications for the interrupt module are listed in table 2-12.

Table 2-12. Interrupt Module Specifications

Characteristic	Specification
Inputs:	8 buffered TTL level interrupts 0V to 1.0V = Logic ONE 3.0V to 5.0V = Logic ZERO
Outputs:	One interrupt active status line for connection to CRU data inputs. Facilitates fast interrupt scan when several interrupt modules are used.
Power Requirements:	+5.0 Vdc @ 0.5A

2.2.7.2 INTERFACE. The interrupt inputs are negative logic TTL level signals. Zero volts is the "True" or interrupt-on level. Filter capacitor pads for each interrupt input are provided on the module as shown in figure 2-7. External connections to the interrupt lines are made at the top edge of the module through an edge connector. Pin assignments are listed in table 2-13.

Table 2-13. CRU Bit Functions for the Interrupt Module

CRU Output Bit Address*	Function	CRU Input Bit Address*	Function	Pin Assignments IN-/GND
0	1/0 = Set/Clear Interrupts 0–7, respectively	0	Interrupt flip-flops 0–7, 1 = Interrupt	$\overline{M}/\overline{N}$
•		•		$\overline{H}/\overline{J}$
•		•		$\overline{C}/\overline{D}$
7		7		Y/Z
8	1/0 = Enable/Mask interrupts 0–7, Respectively	8	Not used	U/V
•		•		P/R
•		•		K/L
15		15		E/F

*Add CRU port address for actual program address.

2.2.7.3 PROGRAMMING. Table 2-13 lists the CRU bit assignments for the interrupt module. Output addresses 0 through 7 are normally used to clear the interrupt flip-flops; however, these addresses may also be used to set the interrupt flip-flops under program control.

The interrupt flip-flop inputs, input addresses 0 through 7, may be read by any CRU input instruction. Only those interrupt lines that are enabled and have an interrupt stored will be read as interrupts.

2.2.8 A/D CONVERTER-MULTIPLEXER (TI PART NUMBER 217690)

This module converts a single-ended analog voltage signal to a 12-bit, two's complement binary number. Basically, it consists of a 16-channel 12-bit analog-to-digital converter and data multiplexer logic which sequentially reads the converted value into the computer.

This A/D module must be installed in a CRU port wired for ±15 volts power in addition to the standard +5 volts. This module is thicker than normal, dictating that it be inserted in a high profile CRU port.

The A/D converter module is available in four optional configurations:

Option 1 - The basic converter with one input channel

Option 2 - Option 1 plus a sample and hold circuit

Option 3 - Option 2 plus an 8-channel input multiplexer

Option 4 - Option 2 plus a 16-channel input multiplexer

2.2.8.1 SPECIFICATIONS. Specifications for the A/D converter are listed in table 2-14.

Table 2-14. A/D Converter-Multiplexer Specifications

Characteristic	Specification
Input Signal Level:	
Option 1	0 to +10.0V, ±5.0V, ±5.0V, or ±10.0V single-ended
Option 2, 3, or 4	0 to + 10.0V, ±5.0V single-ended
Sample Aperture:	
Option 1	25 microseconds maximum
Option 2, 3, or 4	500 nanoseconds maximum
Input Impedance:	
Option 1	5K ohm (±5.0V input) 10K ohm (±10.0V input)
Option 2, 3, or 4	> 10 megohm
Conversion Time:	
Option 1	25 microseconds
Option 2, 3, or 4	225 microseconds
Accuracy:	
Option 1	±0.5%@ 25°C
Option 2	±0.75%@ 25°C
Option 3 or 4	±1.0%@ 25°C
NOTE Accuracies include reference supply tolerances, quantization error, and where applicable, sample and hold and multiplexer transfer error.	

2.2.8.2 INTERFACE. All power and logic signal connections are made through the CRU connector on the bottom edge of the A/D card. Analog input signal connections are made using an edge connector at the top of the card. Table 2-15 lists the pin assignments.

2.2.8.3 PROGRAMMING. Table 2-16 lists the input and output address functions for the A/D module. The 16 CRU output lines of the CRU port (in which the A/D module is plugged) are used to address one of the 16 possible analog input channels and used to start a conversion. The instruction SETB 9, 1 causes channel 9 to be selected and converted. An LDCR instruction may also be used, provided that at least one bit is a ONE in the output field. If the field contains multiple ONES, the ONE going the lowest numbered CRU line is used to select the input channel. Once a conversion has started, the Busy/Ready line remains a ZERO until the conversion is complete. The 12-bit converted value may then be stored. Input bits 2 and 3 are a logic ONE to indicate full scale negative (800_{16}) or full scale positive ($7FF_{16}$) readings.

Table 2-15. Pin Assignments for A/D Converter Multiplexer Module

Analog Input Number	IN/GND
0	$\overline{M}/\overline{N}$
1	$\overline{H}/\overline{J}$
2	$\overline{C}/\overline{D}$
3	Y/Z
4	U/V
5	P/R
6	K/L
7	E/F
8	33/34
9	29/30
10	25/26
11	21/22
12	17/18
13	13/14
14	9/10
15	5/6

Table 2-16. CRU Bit Functions for the A/D Converter/Multiplexer Module

CRU Output Bit Address*	Function	CRU Input Bit Address*	Function
0	1 = Sample and Convert Channel 0	0	Busy/Ready Status, 1 = Ready
1	1 = Sample and Convert Channel 1	1	Not Used – Always = 0
2	1 = Sample and Convert Channel 2	2	1 = Overscale negative indication
3	1 = Sample and Convert Channel 3	3	1 = Overscale positive indication
4	1 = Sample and Convert Channel 4	4	12-bit converted value
5	1 = Sample and Convert Channel 5	•	Bit 4 is LSB
6	1 = Sample and Convert Channel 6	•	May be Two's complement signed
7	1 = Sample and Convert Channel 7	•	value or straight binary
8	1 = Sample and Convert Channel 8	•	depending on jumper option
9	1 = Sample and Convert Channel 9	•	(See user's manual for details)
10	1 = Sample and Convert Channel 10	•	
11	1 = Sample and Convert Channel 11	•	
12	1 = Sample and Convert Channel 12	15	
13	1 = Sample and Convert Channel 13		
14	1 = Sample and Convert Channel 14		
15	1 = Sample and Convert Channel 15		

*Add the CRU port address for actual program address.

The following instruction sequence is adequate to cause a conversion on analog channel 3 and place the value in READING:

```
SETB    3, 1              Start conversion on channel 3
BBNE    0, 1, $           Wait for Ready
STCR    (4, 12), READING  Get converter value
BBNE    2, 0, FSNEG       Check for full scale
BBNE    3, 0, FSPOS       Readings
```

The last two instructions are not required unless the full scale tests are desired.

2.2.9 D/A CONVERTER WITH REGISTERS (TI PART NUMBER 217686)

This module converts a 12-bit, two's complement binary number to a ±5 volt, ±10 volts, or 0 to +10 volt analog signal. The module is available with 1, 2, or 3 channel output options. Internal reference voltage supplies are included on the module.

The D/A card must be plugged into a CRU port wired for ±15 volts in addition to the standard +5 volts. This module is thicker than normal, dictating that it be inserted in a high profile CRU port.

2.2.9.1 SPECIFICATIONS. Specifications for the D/A Converter are listed in table 2-17.

Table 2-17. D/A Converter Specifications

Characteristic	Specifications
Options	1, 2, or 3 output analog voltages
Output Voltage Range	±5.0V @ 10.0 ma maximum ±10.0V @ 10.0 ma maximum 0 to +10.0V @ 10.0 ma maximum
Output Accuracy	±0.5%@ 25°C (includes reference supply variation and non-linearity)
Output Temperature Coefficient	±30 ppm/°C
Settling Time	5 microseconds maximum to 0.01% of full scale
Power Requirements:	
Option 1 (1 channel)	+5.0V @ 330 ma, ±15.0V @ 60 ma
Option 2 (2 channels)	+5.0V @ 430 ma, ±15.0V @ 120 ma
Option 3 (3 channels)	+5.0V @ 530 ma, ±15.0V @ 180 ma

2.2.9.2 INTERFACE. All power and logic connections are made through the CRU connector on the bottom edge of the D/A card. Connections between the analog output terminals and the external devices are made with an edge connector on top of the D/A card. Table 2-18 lists the pin assignments for the analog output signals.

Table 2-18. Pin Assignments for D/A Module Outputs

Converter Number	OUT/GND
0	$\overline{L}/\overline{K}$
1	$\overline{F}/\overline{E}$
2	$\overline{B}/\overline{A}$

2.2.9.3 PROGRAMMING. Table 2-19 lists the output address assignments for the D/A module. The input lines are not used. Output lines 1, 2, and 3 are used to enable one or more of the three converters. Any CRU output instruction addressed to the D/A Module will initiate conversion by the enabled converters. The following instruction sequence will reset the enable flip-flops and output 3 values to converter number 1:

```
                LDCR    (1, 3), ZERO        Reset Enable FF's
                LDCR    (4, 12), VALUE1     Set Up Value
                SETB    (3, 1)              ENABLE Converter 1 and
                                            Start Conversion
                LDCR    (4, 12), VALUE2     Convert Value 2
                LDCR    (4, 12), VALUE3     Convert Value 3
                  •
                  •
                  •
                  •
ZERO            DATA    0                   VALUES TO BE
VALUE1          DATA    18                  CONVERTED
VALUE2          DATA    20
VALUE3          DATA    27
```

Since the execution time for an LDCR on a 12-bit field is about 7.0 μsec, this will cause three conversions about 7 μsec apart. Converter 1 is not enabled until the SETB 3, 1 which also starts the first conversion. The end of the LDCR instruction causes conversion for VALUE2 and VALUE3. An alternative is to use instructions of the form LDCR (0, 16), VALUE where VALUE

Table 2-19. CRU Bit Functions for the D/A Module

CRU Output Bit Address*	Function
0	Not Used
1	1 = Enable Channel 3 Converter
2	1 = Enable Channel 2 Converter
3	1 = Enable Channel 1 Converter
4 • • • • • 15	12-bit value to be converted Bit 4 is LSB

*Add the CRU port address for actual program address.

contains the number to be converted in memory bits 0 through 11 and bits 12, 13, and 14 contain ones for each converter to be enabled. This enables the converters required, sets up the value to be converted, and starts conversion.

Another use, more typical perhaps, would be a LDCR (4, 12) to load value to be converted followed by SETBX, 1 then SETBX, 0 with X being desired channel; this will load in desired value for channel then remove enable so other values can be loaded for other channels.

2.2.10 DATA COMMUNICATIONS MODULE (TI PART NUMBER 961642)

The communications interface module allows the computer to communicate, through the CRU, with peripheral devices whose interface is specified by EIA document RS232C. This module interfaces to datasets for phone line transmission as well as EIA compatible terminals. A TI ASR733 or KSR733 terminal, or a Teletypewriter ASR33 may be interfaced through this module as an option.

2.2.10.1 SPECIFICATIONS. Specifications for the data communications module are listed in table 2-20.

2.2.10.2 INTERFACE. Dataset connections to the module are made at the top edge of the card; cables are available for modem and EIA devices. Baud rates are selected by jumper wires on the module. The communications module may be used in any CRU port. The port must be wired for ±15V if the EIA functions are to be used. Table 2-21 lists the pin assignments for the interface signals.

Table 2-20. Data Communications Module Specifications

Characteristic	Specification
Operating Modes:	With Bell 103 (A or F) With Bell 202 (C or D) datasets 110 baud 150 baud 300 baud 1200 baud 1200 baud, Bell 202 with reverse channel 1760 baud 1760 baud, Bell 202 with reverse channel 2400 baud 4800 baud 9600 baud
Interface Levels	EIA standard RS232C or 20 ma current loop
Inputs	Received data Dataset ready Data carrier detect Reverse channel received
Outputs	Transmitted data Request to send Data terminal ready Pseudo clear to send Reverse channel transmit Signal ground
Power Requirements	+5.0 Vdc at 0.7 A +15.0 Vdc at 60 ma -15.0 Vdc at 60 ma } Not needed for use with TTY or TI 700/30 printer

The interrupt from the TTY/EIA module is the OR function of three flags:

a. Write Request. - set when a character transmission is complete; reset by output from CPU to CRU address 11

b. Read Request. - set 0.5 bit time after a received character is loaded into the receive buffer circuit; reset by output to address 12

c. New Status. - set when Data Set Ready (DSR) or Data Carrier Detect (DCD) status changes; reset by output to address 13

This interrupt cannot be masked on the module; it must be cleared each time it occurs or the CRU mask bit must be set in the CPU status register.

2.2.10.3 PROGRAMMING. Table 2-22 lists the CRU address assignments for the communications (TTY/EIA) module. The method of programming this module varies with the type of device that is connected at the interface. Modems or data sets have line disciplines that must be followed. The following discussion explains the interface for the ASR33, ASR733 and KSR733 terminals as an example of the interface requirements.

Table 2-21. Pin Assignments for Data Communications Module Interface Signals

Signal	Pin	Comment
TTYHR	33	20 ma Receive Source
TTYLR	35	20 ma Receive Return
TTYRCVOUT–	34	Output of 20 ma Receiver
TTYRCVIN–	22	Jump to TTYRCVOUT– for 20 ma circuit – Jump to GROUND for EIA Circuit
GROUND	Z,$\overline{B}$	–
EIARCVDOUT	$\overline{L}$	Output of EIA Data Receiver
EIARCVDIN	21	Jump to EIARCVDOUT for EIA Circuit – Jump to +5V for 20 ma Circuit
+5V	20	–
RCRE	32	Reverse Channel Receive – EIA Level
DCDE	30	Data Carrier Detect – EIA Level
DSRE	31	Data Set Ready – EIA Level
RCVDE	29	EIA Received Data Input
TTYHX	23	20 ma TRANSMIT Source
TTYLX	16	20 ma TRANSMIT Return
XMTDE	27	EIA TRANSMIT Data Output
RTSE	28	Request to Send – EIA Level
RCTE	26	Reverse Channel TRANSMIT – EIA Level
DTRE	25	Data Terminal Ready – EIA Level
PCTSE	5	Pseudo Clear to Send – Jump to DSRE when not connecting to DATASET
PDCDE	6	Pseudo Data Carrier Detect – Jump to DCDE when not connecting to DATASET.
INT–	24	Interrupt Output of Module

Table 2-22. CRU Bit Functions for the Data Communications Module

CRU Output Bit Address*	Function	CRU Input Bit Address*	Function
0 • • • 7	Character to be transmitted Bit 0 is LSB	0 • • • 7	Received character Bit 0 is LSB
8	Not Used	8	Transmit in progress
9	Data terminal ready: 1 = ON; 0 = OFF	9	Timing error
10	Request to send: 1 = ON; 0 = OFF	10	Reverse channel received
11	Clear write request	11	Write request
12	Clear read request } Data value 1 or 0	12	Read request
13	Clear new status flag	13	Data carrier detect
14	Not Used	14	Dataset ready
15	Not Used	15	Interrupt

1 = ON; 0 = OFF

*Add the CRU port address for actual program address.

The following instruction sequence echoes any character that is typed on the terminal keyboard assuming that the CRU interrupt is masked in the status register and that registers 4, 5, and 7 contain the necessary data, program, and CRU base address:

```
NEXT    BBNE    12, 1, NEXT     Wait on Read Request
        STCR    (0, 8), CHAR    Get Character Typed
        LDCR    (0, 8), CHAR    Put it Back Out
        SETB    12, 0           Turn off Read Request
        B       NEXT
CHAR    DATA    0               Data Storage
```

2.2.11 CARD READER COLUMN BUFFER MODULE (TI PART NUMBER 943795)

The card reader interface is designed to allow the computer to efficiently utilize a True Data Corporation Model 804 card reader via the CRU. It provides storage for one 12-bit column of punched card data, detects errors originating at the reader, and errors due to software timing violations. The card reader may be used in any CRU port.

2.2.11.1 SPECIFICATIONS. Specifications for the card reader column buffer module are listed in table 2-23.

Table 2-23. Card Reader Column Buffer Module Specifications

Characteristic	Specification
Inputs	12 Data Bits (column data) Column Index Card Presence Reader Ready Read Error Feed Error
Outputs	Read Command Clear Error
Standard Interface for	True Data Model 804
Power Requirements	+5.0 Vdc @ 0.5A

2.2.11.2 MODULE INTERFACE. All module inputs are TTL logic levels, utilizing emitter follower circuits (see figure 2-7). Connection is normally made using a TI supplied interface cable. Table 2-24 lists the connector pin assignments.

Table 2-24. CRU Bit Functions for the Card Reader Column Buffer Module

CRU Bit Addresses*	Function		Pin Assignment IN/GND OUT/GND
In 0	Read Error or Feed Error	1 = Error 0 = No Error	$\overline{M}/\overline{N}$ $\overline{P}/\overline{R}$
1	Reader Ready	0 = Ready	$\overline{H}/\overline{J}$
2	Row 8	1 = Hole	$\overline{C}/\overline{D}$
3	Row 9	1 = Hole	Y/Z
4	Row 10	1 = Hole	U/V
5	Row 11	1 = Hole	P/R
6	Row 12	1 = Hole	K/L
7	Card Presence	1 = Present	E/F
8	Row 7	1 = Hole	33/34
9	Row 6	1 = Hole	29/30
10	Row 5	1 = Hole	25/26
11	Row 4	1 = Hole	21/22
12	Row 3	1 = Hole	17/18
13	Row 2	1 = Hole	13/14
14	Row 1	1 = Hole	9/10
15	Column Index – Interrupt	1 = Present	5/6
Out 0 • 10	Not Used		
11	Set End of Record	1/0 = Allow/Prevent End of Card Interrupt	
12	Clear Timing Error	0 = Clear Error and Column Interrupt	
13	Interrupt Mask	1/0 = Allow/Prevent Column Interrupt and Timing Error	
14	Clear Interrupt	1/0 = Clear Interrupt	
15	Read Command	0 = Read Cards and Clear End of Record, Interrupt Mask, Timing Error, and Column Interrupt.	4/3
Out 15	Must be 0 for at least 10 μsec to start reader Clear Error wired to module +5V		8/3

*Add CRU port address for actual program address.

2.2.11.3 PROGRAMMING. Table 2-24 lists the CRU address assignments for the card reader module. The card reader is started by setting the read command line to a ZERO for a minimum of 10 microseconds. If the card feeds, card presence goes True in about 40 ms and 80 column indices occur. Each column index is about 140 microseconds long and each clocks the new column of data into a holding register where it remains until the next column index occurs 1.3 milliseconds later. If the interrupt mask is set to enable the interrupts, an interrupt will occur for each column index. If another column index occurs before the interrupt is cleared, a timing violation is generated to set the error flip-flop. The error flip-flop is also set by the card reader signals read or feed error. The error flip-flop may be cleared by pressing

the START pushbutton on the card reader. Additionally, a timing violation may be cleared by issuing a read command or by using the clear error output line. The organization of column data on the input lines has been selected to simplify the decoding of data into its internal representation. The Basic Programming Guide explains this decoding scheme. The End of Record flip-flop may be set to enable the End of Card interrupt from the card reader. The interrupt mask flip-flop should be used at the same time to disable the column interrupts. The End of Card interrupt cannot be reset. The End of Record flip-flop must be reset after servicing the End of Card interrupt to disable that interrupt.

A simple, non-interrupt controlled loop to read one card and store the 80 columns, one per word starting at KARD, might occur as follows:

```
            LA      0, 79           Loop Counter
            LA      4, KARD         Register 4 Points To KARD
            SETB    13, 0           Mask Interrupts
START       SETB    15, 0           Generate
            NOP                     Read Command
            SETB    15, 1           Pulse 10 usec Long
NXTCOL      BBNE    1, 0, START     Check Ready And
            BBNE    15, 1, $        Try Again. If not Wait for
                                    Column Index
            STCR    (2, 13), 0      Get Column
            BBNE    15, 0, $        Wait for Column Index To Go
                                    Away
            AA      4, 1            Increment Pointer To KARD
            ARB     -1, NXTCOL. 0   Decrement Loop Counter
```

In most situations the card reader routine would operate under interrupt control and would convert the column information into a usable form before storing it in memory. Also the error line must be monitored and the interrupts reset.

2.2.12 OCI DATA MODULE (TI PART NUMBER 966495)

The optically coupled isolator (OCI) input data module provides 32 input data lines which may be driven by external voltage sources of 5, 12, or 24 Vdc. The OCI data module is primarily designed for one way interface communication between the computer and devices or transducers which generate discrete on-off signals but which have a different ground reference than the computer logic ground. Each input may be interrogated by the CPU either individually or as a member of a group of lines.

The OCI data module may be used to sense solid-state logic or isolated contact closures of dc voltages. Like other CRU data modules, the OCI board may be inserted into any CRU slot.

2.2.12.1 SPECIFICATIONS. The OCI data module input circuit is a 22ma optically isolated current sensor. The circuit is capable of responding to input pulses at a maximum rate of 100 kHz. Table 2-25 contains a list of specifications for each type of OCI data module.

Table 2-25. OCI Data Module Input Specifications

Characteristic	Specification		
Input:			
Rated	0-5 Vdc	0-12 Vdc	0-24 Vdc
Maximum ZERO Voltage	1.2 Vdc	1.2 Vdc	1.3 Vdc
Minimum ONE (Typical)	2.1 Vdc	3.9 Vdc	6.9 Vdc
Minimum ONE (Worst Case)	3.9 Vdc	9.3 Vdc	18.3 Vdc
Input (Resistance)	164 ohms	540 ohms	1020 ohms
Logic Levels:	+5.0 Vdc @ 1.04A Maximum Plus 0.96A Maximum (32 inputs @ 30 ma each)		
Power Requirements:			
Logic ZERO	0.0 to 0.1 ma		
Logic ONE	10 to 30 ma from external voltage supply.		

2.2.12.2 OCI DATA MODULE INTERFACE. See table 2-26 for pin assignments. Signals with the "IN" prefix are a positive polarity with respect to the corresponding signal with the "SWIN" prefix which is the ground reference.

2.2.12.3 PROGRAMMING. When an OCI data module is interfaced via the internal CRU chassis, the first 16 data lines (0-15) are addressed as $0FX0_{16}$ through $0FXF_{16}$ respectively, and the second 16 data lines (16-31) are addressed as $0EX0_{16}$ through $0EXF_{16}$, respectively. The letter 'X' in the above CRU bit addresses represents a hexadecimal value corresponding to the CRU slot in which the OCI data module is inserted.

If the OCI data module is interfaced via an external CRU expansion chassis then the first 16 data lines (0-15) are addressed as $0XX0_{16}$ through $0XXF_{16}$ respectively and the second sixteen data lines (16-31) are addressed as $0(X+1)X0_{16}$ through $0(X+1)XF_{16}$, respectively.

Please note that the CRU base address of the second set of 16 data lines is 0100_{16} lower than the base address of the first set only if the interface is

Table 2-26. OCI Data Module Interface Pin Assignments

Data Line	Signal	Top-Edge Connector	Signal	Top-Edge Connector
0	IN0	P2-3	SWIN0	P2-C
1	IN1	P2-4	SWIN1	P2-D
2	IN2	P2-5	SWIN2	P2-E
3	IN3	P2-6	SWIN3	P2-F
4	IN4	P2-7	SWIN4	P2-H
5	IN5	P2-8	SWIN5	P2-J
6	IN6	P2-9	SWIN6	P2-K
7	IN7	P2-10	SWIN7	P2-L
8	IN8	P2-11	SWIN8	P2-M
9	IN9	P2-12	SWIN9	P2-N
10	IN10	P2-13	SWIN11	P2-R
11	IN11	P2-14	SWIN11	P2-R
12	IN12	P2-15	SWIN12	P2-S
13	IN13	P2-16	SWIN13	P2-T
14	IN14	P2-17	SWIN14	P2-U
15	IN15	P2-18	SWIN15	P2-V
16	IN16	P2-19	SWIN16	P2-W
17	IN17	P2-20	SWIN17	P2-X
18	IN18	P2-21	SWIN18	P2-Y
19	IN19	P2-22	SWIN19	P2-Z
20	IN20	P2-23	SWIN20	P2-A-
21	IN21	P2-24	SWIN21	P2-B-
22	IN22	P2-25	SWIN22	P2-C-
23	IN23	P2-26	SWIN23	P2-D-
24	IN24	P2-27	SWIN24	P2-E-
25	IN25	P2-28	SWIN25	P2-F-
26	IN26	P2-29	SWIN26	P2-H-
27	IN27	P2-30	SWIN27	P2-J-
28	IN28	P2-31	SWIN28	P2-K-
29	IN29	P2-32	SWIN29	P2-L-
30	IN30	P2-33	SWIN30	P2-M-
31	IN31	P2-34	SWIN31	P2-N-

within the internal CRU. If the interface is within the external CRU, then the base address of the second set of 16 data lines is 0100_{16} greater than the base address of the first set.

2.2.13 OCI INTERRUPT MODULE (TI PART NUMBER 966787)

The Optically Coupled Isolator (OCI) interrupt module will issue an interrupt to the CPU upon closure of any one of 16 external switches. The input circuits operate from external voltage sources of 5, 12, or 24 Vdc, and are optically coupled to the logic circuits to provide input isolation.

After the interrupt has occurred, the CPU can read the line number which caused the interrupt by properly addressing CRUBIT 12-15. The CPU will service any other interrupts before returning to the program.

Each input can be masked individually or the entire board may be masked so that no interrupt is issued. During the power on sequence, the entire board is automatically masked, so it is necessary to unmask desired bits.

The OCI interrupt module should be installed in a high profile CRU port due to its thicker profile.

2.2.13.1 SPECIFICATIONS. Specifications for the OCI interrupt module are listed in table 2-27.

Table 2-27. OCI Interrupt Module Specifications

Characteristic	Specification
Input Current:	
Logic ZERO	0.0 to 0.1 ma
Logic ONE	10 to 30 ma from external voltage supply
Input Resistance:	
	5Vdc 164 ohms 12Vdc 540 ohms 24Vdc 1020 ohms
Output:	One interrupt active status line for connection to CRU data inputs.
Power Requirements:	+5.0Vdc @ 0.68A plus 0.480A (16 inputs @ 30 ma each) from external voltage supply.

2.2.13.2 INTERFACE. The input circuit of the OCI interrupt module is a 22 ma optically isolated current sensor. Connector pin assignments are as shown in table 2-28.

2.2.13.3 PROGRAMMING. The bit fields used by the OCI interrupt module are shown in table 2-29. The bit values shown are those found in memory. Input bits 1 through 4 contain a number between 0 and F representing the number of the current interrupt. Any output to address 14 causes the current interrupt to be cleared and the scan to be restarted. If any other interrupts are present, input bit 0 will be a 1 and another CRU interrupt will be serviced within 2.7 microseconds.

An output of 1 to bit 15 will mask the CRU interrupt from the module. Input 0 still reflects the presence of an interrupt. An output of 0 to bit 15 permits the CRU interrupt to be generated upon an input switch closure.

Table 2-28. Pin Assignments for the OCI Interrupt Module

Input Number	Pin Number to External Voltage	Pin Number to External Switch
0	3	C
1	4	D
2	5	E
3	6	F
4	7	H
5	8	J
6	9	K
7	10	L
8	11	M
9	12	N
10	13	P
11	14	R
12	15	S
13	16	T
14	17	U
15	18	V

Each input can be masked individually. To do this, a 16 bit code (mask) must be generated which indicates the input or inputs to be masked. Two outputs (LDCR) to bits 0-7 must be used to generate the mask. Input 15 will be masked by the first bit of the first 8 bits. Input 7 will be masked by the first bit of the second 8 bits output. A one is a mask and a zero is unmasked. The board interrupt (Bit 15) should be masked during loading of the input interrupt mask.

2.2.14 REGULATOR MODULE, ±15 VOLT (TI PART NUMBER 226855)

The ±15 volt regulator module must be used to supply two of the voltages required by the A/D and D/A converter modules and the data communications module in the EIA mode of operation when these modules are used in the internal CRU expansion. The module obtains power from the 35 Vac pins of the CRU ports. Up to 360 ma of each voltage is supplied which is adequate to power a number of modules, depending on the individual module options. Requirements for more current may be satisfied by attaching external supplies to the wiring of the CRU backplane. The regulator plugs into the CPU slot labeled REG. In early computers, this slot was labeled EXM and the regulator was plugged into any CRU port inside the CPU.

2.2.14.1 SPECIFICATIONS. Specifications for the regulator module are listed in table 2-30.

2.2.14.2 INTERFACE. Normally there is no external connections to the module. The module supplies ±15V to existing CRU backplane wiring. The ±15 V may be obtained from the top edge connector of the module as listed in table 2-31.

Table 2-29. CRU Bit Functions for the OCI Interrupt Module

Input	Function
0	1/0 = Interrupt has/has not occurred
1, 2, 3, 4	Number of Interrupt; 1 is LSB
5 . . 15	Not Used

Output	Function	
0	1/0 = Mask/Unmask Int	15 or 7
1		14 or 6
2		13 or 5
3		12 or 4
4		11 or 3
5		10 or 2
6		9 or 1
7		8 or 0
8 . . 13	Not Used	
14	Data Value 1 or 0 = CLEAR Current Interrupt and Restart Scan	
15	1/0 = MASK/UNMASK Board Interrupt	

Table 2-30. Regulator Module Specifications

Characteristic	Specification
Inputs	35 Vac @ 1A from CPU power supply
Output	±15V @ 360 ma, ±0.2% total line and load

Table 2-31. ±15V Regulator Pin Assignments

Signal	Pins
+15V	20, 21, X, Y
GND	18, 19, 36, 1, A, V, W, $\overline{R}$
−15V	16, 17, T, U

2.2.14.3 PROGRAMMING. No CRU addresses are assigned to this module as there are no programmable functions.

2.3 CRU SYSTEM CONFIGURATIONS

2.3.1 BASIC SYSTEM

The basic computer mainframe contains the CRU interface card and four connectors for CRU modules. All mainframe components for the CRU system are installed in the card cage at the right rear of the chassis. Figure 2-9 is a top view of the mainframe. The CRU interface card is installed in card location CRI. The four CRU module connectors, labeled EF0 through EF3, are located directly behind the CRU interface card. The four basic module connectors are spaced on 13 mm (0.5-inch) centers; therefore the contactor, A/D converter, and D/A converter modules cannot be installed in these connectors. Any combination of digital and TTY/EIA interface modules may be installed in the four basic locations. The CPU power supply provides ±15V at 100 ma to the four basic CRU module connectors. Cables from the CRU modules to external equipment are routed over the top cover of the power supply and out the rear of the chassis.

2.3.2 MAINFRAME CRU EXPANSION

The CRU module capacity of the mainframe CRU system may be expanded to 16 modules by the installation of a CRU expansion kit (TI Part Number 226722). This kit contains an expansion connector plate and an interconnect board. The expansion connector plate is installed behind the four basic CRU module connectors as shown in figure 2-10. This connector plate contains 12 additional 80-pin connectors for CRU modules. The interconnect board is used to complete the electrical connections between the wire-wrap pins of connectors EF3 of the basic system and EF4 of the expansion connector plate. It is placed over the wire-wrap pins and soldered at each pin. Installation of the interconnect board completes the connection of all required signal and power circuits from the basic to the expansion protions of the CRU system. The CRU module connectors EF4 through EFB are located on 25 mm (1.0-inch) centers to allow installation of high profile CRU modules. The last four connectors, EFC through EFF, are spaced on 13 mm (0.5-inch) centers and will accept only low profile modules. Any combination of CRU modules using only the +5 volt power may be installed on the 16 mainframe connectors. The limit on the number of modules requiring ±15 Vdc is determined by the available ±15 Vdc supply.

2.3.3 EXTERNAL CRU EXPANSION

For systems containing more than 16 CRU modules, the CRU expansion unit is used. The CRU expansion (TI Part Number 966556) is a rack-mount assembly.

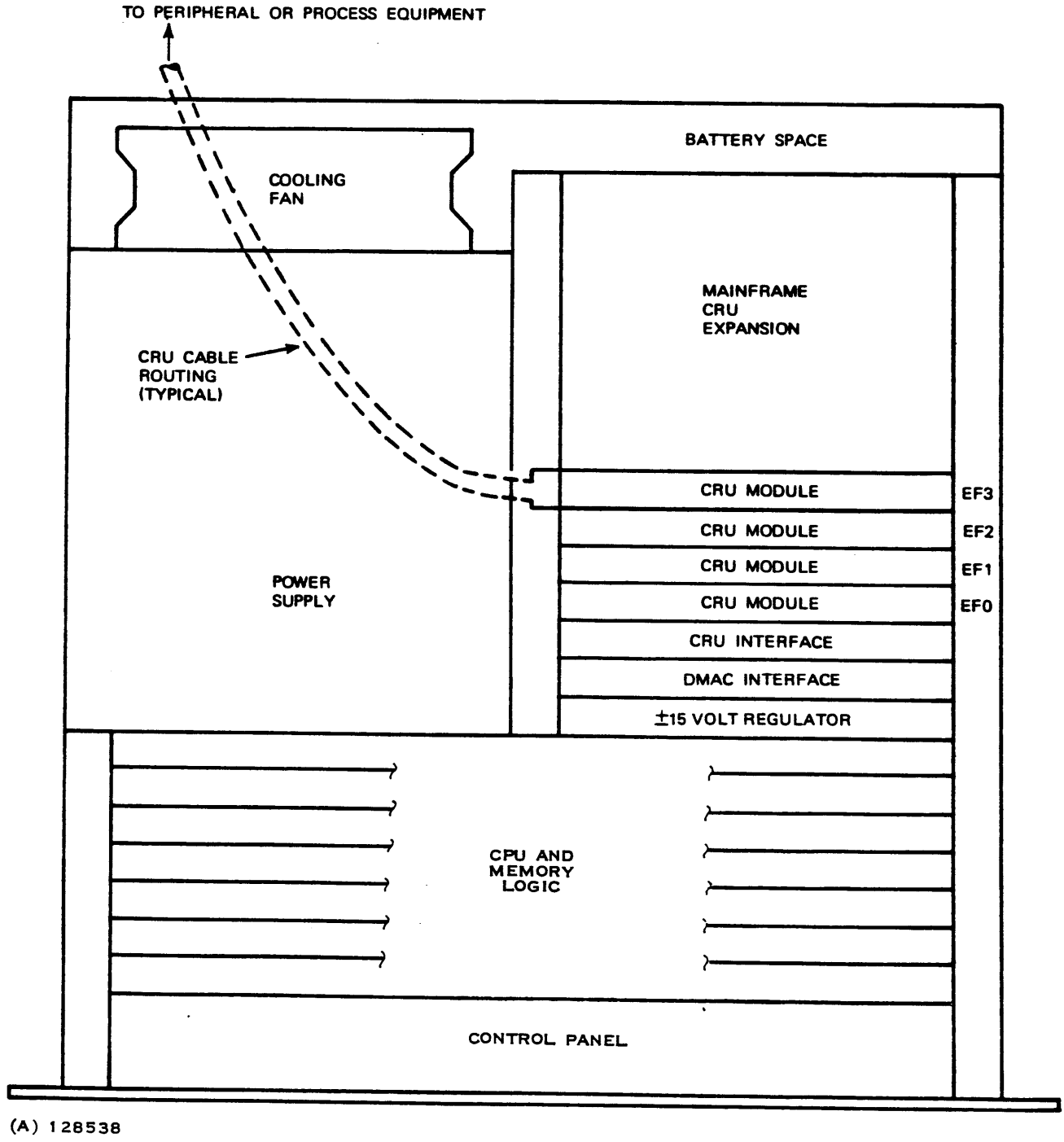


Figure 2-9. Basic CRU System - Mechanical Configuration

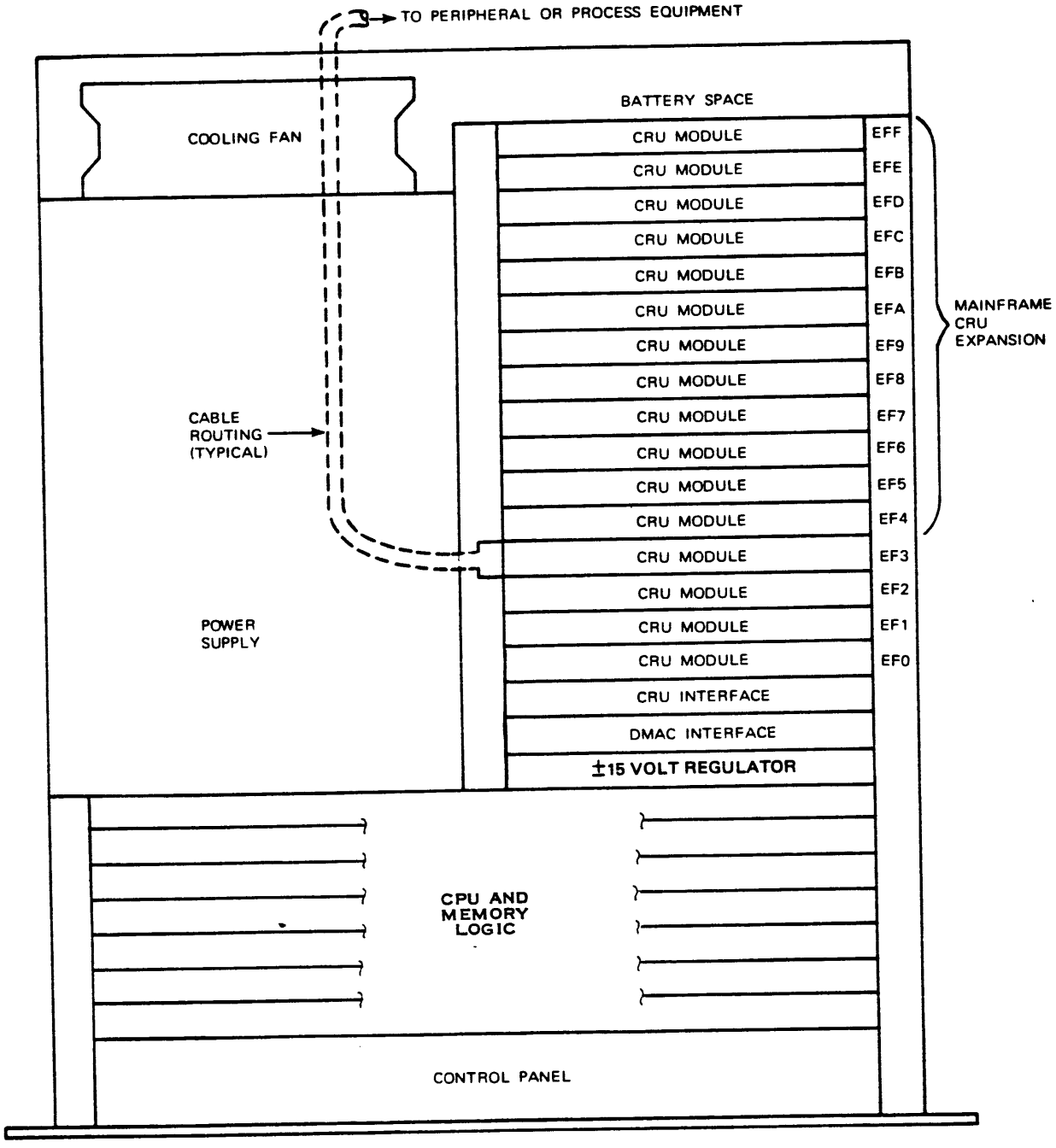


Figure 2-10. Mainframe CRU Expansion - Mechanical Configuration

Each expansion unit contains a power supply, a buffer PC card, and connectors for 16 CRU modules as shown in figure 2-11. The CRU module connectors are spaced to allow installation of a high or low profile module in any location. The buffer card is a double-ended PC card. The 72-pin top edge completes the interface between the CPU and expansion unit. The bottom edge plugs into connector location B of the expansion unit card rack assembly to complete the interface to the expansion unit CRU modules.

NOTE

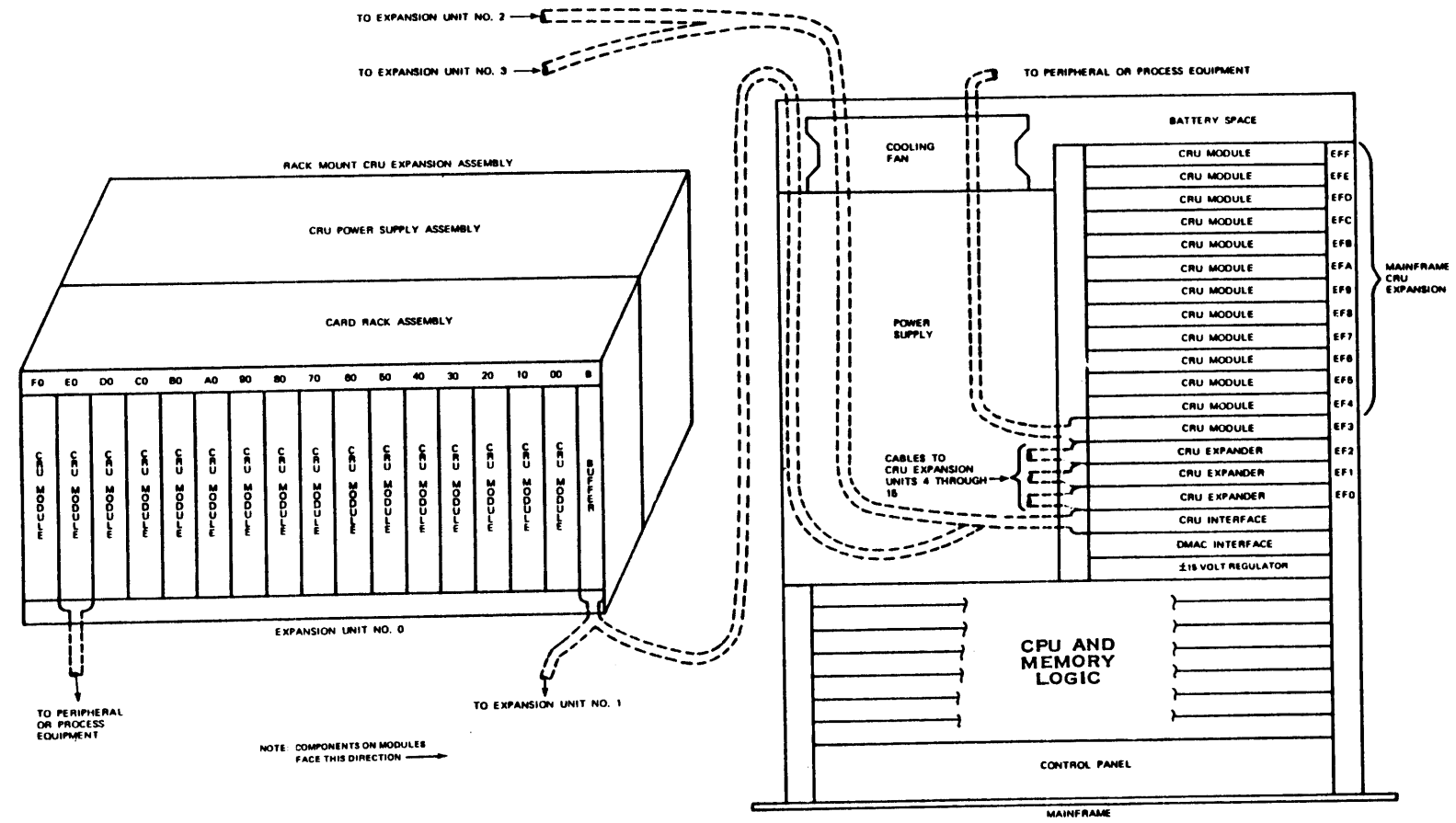
Table 4-2 contains a list of jumpers that must be removed for the various expansion options. These jumpers must be reinstalled if expansion chassis is removed.

Connection to the first four expansion units (0, 1, 2, and 3) is completed through the top edge connector of the CRU interface card in the CPU. The four unit cable assembly branches into two sections at the CRU interface connector. At the expansion unit end, each cable section branches to two connectors for connection to the four expansion units. Other cable assemblies are available for connection from the CRU interface and to one or two expansion units. Also, each cable type is available in lengths of 3.66 or 6.10 m (12 or 20 feet) except for the CPU to one 16 address CRU which is 1.83 m (6 feet). All available types are listed in table 2-32. For other lengths of cable, the factory must be consulted.

For expansion to more than 4 CRU expansion units, a CRU expander card is installed in mainframe connector location EF0, EF1, or EF2. The CRU expander card is a double-ended PC board which completes the interface between the mainframe CRU interface card and external expansion units. One, two, four expansion units may be connected to each expander card using cables listing in the preceding table. By expanding from the CRU interface card plus all three CRU expander cards, a maximum of 16 external expansion units may be connected to the CRU system.

Two electrical options are available for the rack mount CRU expansion units as listed in table 2-33. The basic option (TI Part Number 966556-0001) contains only a +5V logic power supply; therefore, the TTY/EIA interface (as an EIA interface), A/D converter, and D/A converter modules cannot be used in this option.

Texas Instruments Part Number 966556-0002 contains +5-volt, -15-volt, and +15-volt power supplies to provide power for all module types including the A/D converter, the D/A converter, and the TTY/EIA. There is no restriction on the mixture of CRU module types that can be installed in this option.



(A) 128540

Figure 2-11. CRU Expansion Unit - Mechanical Configuration

Table 2-32. CRU Expansion Cables

TI Part Number	Cable Description	Length
955364-0012	CPU to CRU–32 Select	3.66 m (12 ft)
955366-0012	CPU to 2 CRU–32 Select	3.66 m (12 ft)
216094-0012	CPU to 4 CRU–16 Select	3.66 m (12 ft)

Table 2-33. CRU Expansion Unit Options

TI Part Number	Description
966556-0001	CRU Expansion, Rack Mount, +5V
966556-0002	CRU Expansion, Rack Mount, +5, ±15V (EIA, A/D, D/A)

SECTION III
ADDRESSING

3.1 GENERAL

The 12-bit CRU address may be considered as containing three four-bit segments. The function of each address segment is specified in table 3-1.

Table 3-1. Address Segment Functions

Address Bits	Function
CA04-CA07	Selects one set of 16 available module sets (expansion or mainframe
CA08-CA11	Selects one module of selected 16-module set
CA12-CA15	Selects one line of a 16-line set within selected module

Each 4-bit address segment may be represented as a hexadecimal character. Using this notation, the CRU address range is 000_{16} to FFF_{16}. The preceding address description applies only to 16-line modules. The 32-line data module contains two 16-line sets which are addressed the same as two 16-line data modules installed in two different expansion units at the same module location. Therefore, two different codes in the rack select address segment (CA04-CA07) will select two different 16-line sets within the same CRU module. In a system completely filled with 32-line data modules, address bits CA04 through CA07 will select one 16-module set of eight 16-module sets because each module is selected by two rack select codes.

3.2 ADDRESSING OF 16-LINE MODULES

Figure 3-1 illustrates address decoding and module selection for 16-line modules throughout the system.

3.2.1 MAINFRAME CRU SYSTEM

Modules within the mainframe are activated by signals MODSELF0 through MODSELFF from a 1 of 16 decoder on the CRU interface card. This decoder is enabled by a gate which detects F_{16} in CA04-CA07. The decoder is addressed by CA08-CA11. The least significant address segment, CA12-CA15, is buffered on the CRU interface card and supplied to all mainframe CRU modules as signals CRUBIT12-CRUBIT15. The resulting hexadecimal address assignments for mainframe modules are specified in table 3-2.

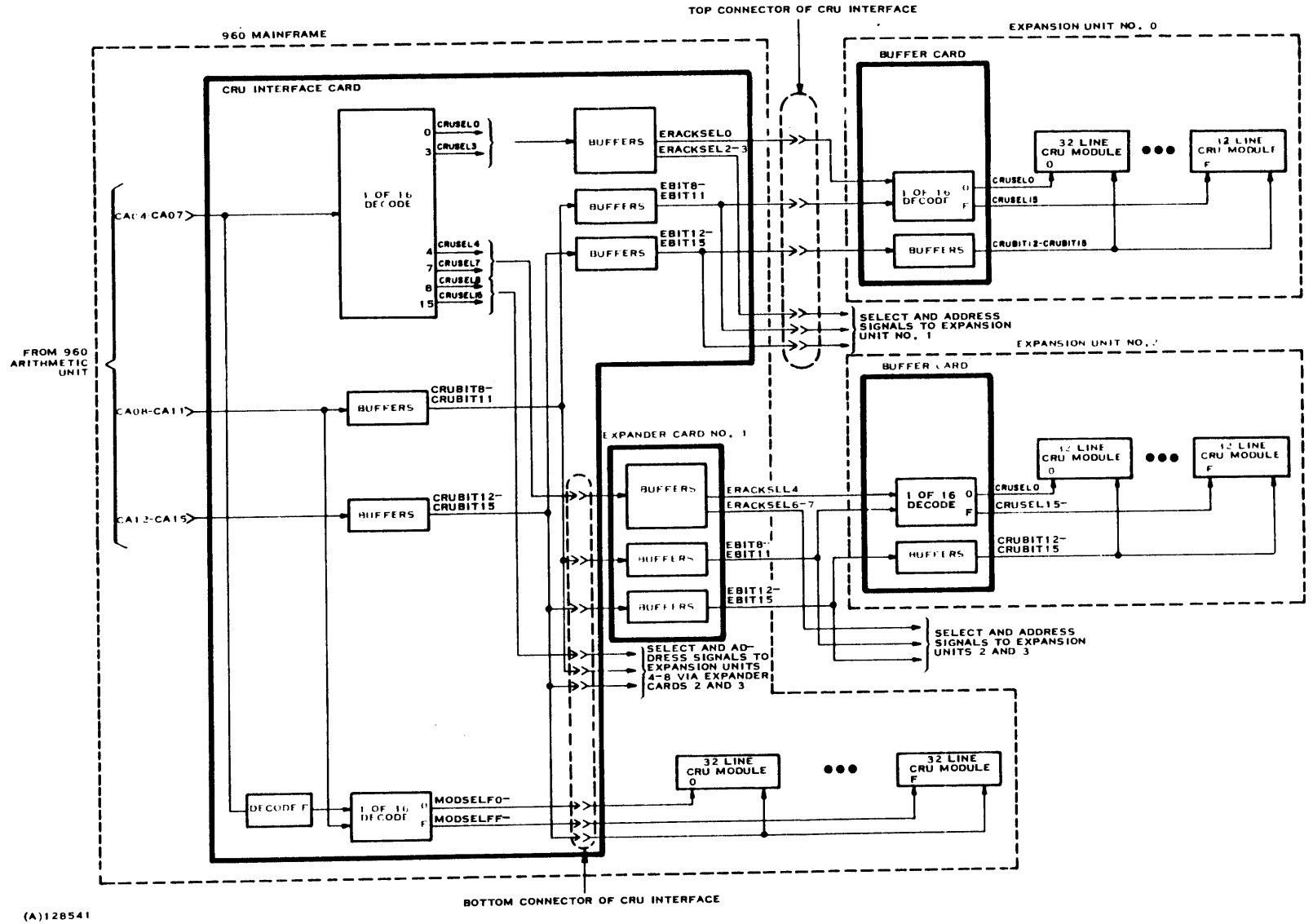


Figure 3-1. Address Decoding and Module Selection, 16-Line Modules

Table 3-2. Expansion Module Address Assignments for 16-Line Modules

Module	Address Assignment
Basic Module No. 1	F00-F0F
Basic Module No. 2	F10-F1F
Basic Module No. 3	F20-F2F
Basic Module No. 4	F30-F3F
Option Module No. 1	F40-F4F
Option Module No. 2	F50-F5F
Option Module No. 3	F60-F6F
Option Module No. 4	F70-F7F
Option Module No. 5	F80-F8F
Option Module No. 6	F90-F9F
Option Module No. 7	FA0-FAF
Option Module No. 8	FB0-FBF
Option Module No. 9	FC0-FCF
Option Module No. 10	FD0-FDF
Option Module No. 11	FE0-FEF
Option Module No. 12	FF0-FFF

3.2.2 EXPANSION TO 1, 2, OR 4 CRU EXPANSION UNIT

Address bits CA04-CA07 are also decoded by a 1 of 16 rack select decoder on the CRU interface card which produces signals CRUSEL0- through CRUSEL15-. Signals CRUSEL0- through CRUSEL3- correspond to codes 0_{16} through 3_{16} which are buffered to produce ERACKSEL0 through ERACKSEL3, respectively. Signals CA08 through CA15 are provided two levels of buffering to produce signals EBIT8 through EBIT15, respectively.

All of the preceding ERACKSEL and EBIT signals are connected to the top edge connector of the CRU interface card. From this card, connection is provided to a maximum of four CRU expansion units. Each of the four ERACKSEL signals enables a 1 of 16 decoder on the buffer card of a CRU expansion unit. The decoder is addressed by EBIT8-EBIT11 to provide outputs CRUSEL0- through CRUSEL15- which activate one of the 16 CRU modules in the expansion unit. Signals EBIT12-EBIT15 are buffered on the buffer card to produce CRUBIT12-CRUBIT15 for line addressing of the modules.

In summary, address assignments for expansion units 0-3 are specified in table 3-3.

3.2.3 EXPANSION TO 5 TO 16 CRU EXPANSION UNITS

For connection to more than four external expansion units, a CRU expander card must be installed in the mainframe for each group of four additional

Table 3-3. Expansion Unit (0-3) Address Assignments

Expansion Unit	Address Assignment
0	000-0FF
1	100-1FF
2	200-2FF
3	300-3FF

expansion units. On the CRU interface card, signals CRUSEL4- through CRUSEL15- from the rack select decoder and address signals CRUBIT8 through CRUBIT15 are routed to the bottom edge connector. These signals are wired to the connectors in which the three CRU expander cards are installed.

Each Expander card contains buffer circuits for four ERACKSEL signals and for address signals CRUBIT8 through CRUBIT15. The output of the buffers on each CRU expander is connected through the top edge connector to 1, 2, or 4 CRU expansion units. Operation of expansion units through the CRU expander card is identical to the operation described for expansion units 0 through 3. CRU expander card locations and address assignments for expansion units 4 through 15 are identified in table 3-4. Address assignments of CRU expansion unit 15 overlap the mainframe CRU modules; however, mainframe CRU addresses F00 through F2F are lost because of the three expander cards installed in a fully expanded system.

Table 3-4. Expander Card Unit Locations and Address Assignments for 16-Line Modules

Card Location	Expansion Unit	Address Range
EF0	4	400-4FF
	5	500-5FF
	6	600-6FF
	7	700-7FF
EF1	8	800-8FF
	9	900-9FF
	10	A00-AFF
	11	B00-BFF
EF3	12	C00-CFF
	13	D00-DFF
	14	E00-EFF
	15	F00-FFF

3.3 ADDRESSING OF 32-LINE MODULES

Address decoding and module selection for 32-line modules are illustrated in figure 3-2.

3.3.1 MAINFRAME CRU SYSTEM

The CRU interface card contains a second 1 of 16 decodes for selection of mainframe CRU modules. This decoder is enabled by the output of a gate which detects E_{16} in CA04-CA07 and is addressed by CA08-CA11. The decoder outputs are MODSELE0- through MODSELEF- which activate the second 16-line group of modules in locations EF0 through EFF, respectively. The first 16-line group in the mainframe modules is activated by MODSELF0- through MODSELFF- as previously described. The resulting address assignments for sixteen 32-line modules installed in the mainframe are listed in table 3-5.

3.3.2 EXPANSION TO 1 OR 2 CRU EXPANSION UNITS

Connection to and operation of CRU expansion units containing 32-line modules is similar to that described for 16-line modules except half as many expansion units are used because each module services 32 line addresses.

The buffer card in each expansion unit contains two 1 of 16 decoders each responding to one ERACKSEL signal. From the CRU interface card top edge connector, ERACKSEL0 and ERACKSEL1 are connected to expansion unit 0, and ERACKSEL2 and ERACKSEL3 are connected to expansion unit 1. The resulting address assignments are identified in table 3-6.

3.3.3 EXPANSION TO 3 TO 8 CRU EXPANSION UNITS

One CRU expander card is installed in the mainframe for each additional pair of CRU expansion units. Expander card locations and 32-line module addresses are listed in table 3-7. In this case, the mainframe module addresses are overlapped by addresses of expansion unit 7, and mainframe addresses E00-F0F, E10-F1F, and E20-F2F are lost because of the three CRU expander cards installed in locations EF0, EF1, and EF2.

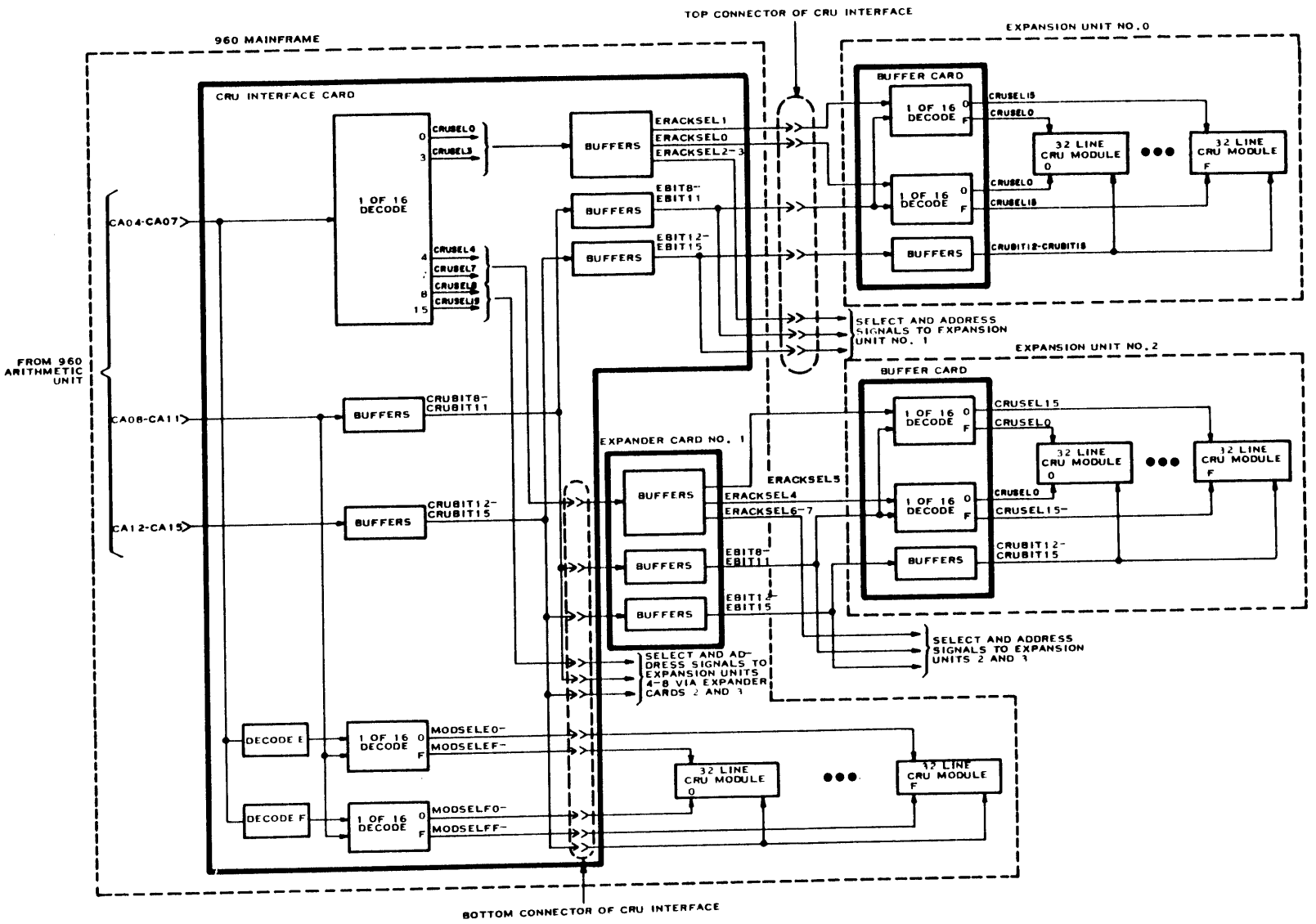


Figure 3-2. Address Decoding and Module Selection, 32-Line Modules

Table 3-5. Expansion Module Address Assignments for 32-Line Modules

Module	First 16-Line Set	Second 16-Line Set
Basic Module 1	F00-F0F	E00-E0F
Basic Module 2	F10-F1F	E10-E1F
Basic Module 3	F20-F2F	E20-E2F
Basic Module 4	F30-F3F	E30-E3F
Option Module 1	F40-F4F	E40-E4F
Option Module 2	F50-F5F	E50-E5F
Option Module 3	F60-F6F	E60-E6F
Option Module 4	F70-F7F	E70-E7F
Option Module 5	F80-F8F	E80-E8F
Option Module 6	F90-F9F	E90-E9F
Option Module 7	FA0-FAF	EA0-EAF
Option Module 8	FB0-FBF	EB0-EBF
Option Module 9	FC0-FCF	EC0-ECF
Option Module 10	FD0-FDF	ED0-EDF
Option Module 11	FE0-FEF	EF0-EEF
Option Module 12	FF0-FFF	EF0-EFF

Table 3-6. Expansion Unit (0-1) Address Assignments

Expansion Unit	Module Addresses	
	First 16-Line Sets	Second 16-Line Sets
0	000-0FF	100-1FF
1	200-2FF	300-3FF

Table 3-7. Expansion Card/Unit Address Assignments for 32-Line Modules

Card Location	Expansion Unit	Module Addresses	
		First 16-Line Sets	Second 16-Line Sets
EF0	2	400-4FF	500-5FF
	3	600-6FF	700-7FF
EF1	4	800-8FF	900-9FF
	5	A00-AFF	B00-BFF
EF2	6	C00-CFF	D00-DFF
	7	E00-EFF	F00-FFF

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section describes in detail the logic implementation and timing of the CRU channel. The implementation of each CRU module is included in the User's Manual for that module.

4.2 MAINFRAME CRU SYSTEM

The mainframe CRU system includes the CRU interface card and 1 to 4 CRU modules in the basic system, or 1 to 16 CRU modules when the mainframe expansion is included.

4.2.1 CRU INTERFACE

Refer to Texas Instruments logic diagram 226807 in Section V of this manual for electrical details of the CRU interface. Bottom edge connector pins on the CRU interface module are labeled P1 and the top edge connector pins are labeled P2. All connections to the CPU and mainframe CRU modules are made through P1.

E_{16} in address bits CA04 through CA07 is decoded by Z16 and Z18 to produce SELENA-, the enable signal for internal module select decoder Z15. F_{16} in CA04-CA07 is decoded by Z18 to produce SELENB-, the enable signal for module select decoder Z17. Module select decoders, Z15 and Z17, are addressed by address bits CA08 through CA11. Z17 generates MODSELF0- through MODSELFF-, the select signals for 16-line modules. Z15 generates MODSELE0- through MODSELEF-, the additional 16 select signals required for 32-line data modules. The MODSELF signals are routed through to the CRU module connectors.

The CRU line address bits, CA12 through CA15, are buffered by the inverters of Z16 and the nand gates of Z10 and Z11. The buffered outputs, CRUBIT12 through CRUBIT15, are bussed through P1 to all mainframe CRU module connectors.

Output data from the AU(CRUBITOUT) is buffered by an inverter and a gate in Z16 and Z12 for distribution to all mainframe CRU connectors as the CPUDATAOUT signal.

The CRU output clock signal, STORECLK-, is generated by a nand gate in Z12 which gates ROM40 from the AU with system clock signal CLK3A1. This signal also is bussed to all mainframe CRU module connectors.

The CRU input data bus (CRUBITIN) connects to pin P1-69 from which R16 acts as a pull-up resistor. The CRU interrupt bus (CRUINTA-) connects to pin P1-75 and pull-up resistor R15.

CRU lines $E\_\__{16}$ and $F\_\__{16}$ may be physically located in either the mainframe or in an external expansion unit. In a CRU input operation, the CRU address must propagate out to the CRU module, the CRU input line must be selected in the CRU module, and the input data must propagate through the CRU module and CRU interface before the shift register in the AU is clocked. When the addressed input line is located in the mainframe, one system clock period is sufficient for signal propagation. Therefore, from mainframe modules, one data bit is clocked into the SR each clock time.

If the addressed input line is located in an external expansion unit, the address and data signals must also propagate through a CRU expander card and a buffer card. In this case, one clock period is insufficient for signal propagation and two clock times per bit are allowed.

Input operation timing is controlled by a signal generated on the CRU interface card. When E00 through EFF are installed in the mainframe, a jumper is installed between terminals E19 and E20 on the CRU interface card. Jumper E17 to E18 is installed if lines F00 through FFF are located in the mainframe. When a mainframe line is selected, SELENA- or SELENB- will go low causing INTMOD-, generated by Z14, to go low. INTMOD- is connected to the control logic in the CPU where it causes one bit to be read in each clock time. If the line address is outside of the range (E00 through FFF) or if the associated jumper is removed, INTMOD- is not generated and two clock times are allowed for the propagation of each input bit.

4.2.2 CRU MODULES

Each CRU module interfaces an external equipment with the CRU interface. Refer to the appopriate user's manual for the equipment interface as listed in Section I of this manual for an explanation of the operation of a particular module.

All mainframe CRU module connectors are wired the same except connectors EF0, EF1, and EF2 carry rack select and address signals which are used only on the CRU expander card. All supply voltages are bussed to all connectors to permit TTY/EIA interface, A/D converter, and D/A converter modules to be installed in any location where connector spacing is not a limiting factor. Connector pin assignments are listed in table 4-1.

4.2.3 SIGNAL LEVELS

All signals at the CRU and CRU module interface are standard TTL levels of 0.0 to +0.4 volts for a logic ZERO and +2.4 to +5.0 volts for a logic ONE.

4.2.4 SIGNAL FLOW

Figure 4-1 shows the overall path through which signals must propagate in the mainframe CRU system.

Table 4-1. CRU Module Pin Assignments

Signal	Bottom Edge Connector Pin(s)	Comment
GROUND	1, 2, 63, 64, 79, 80	
POFF-	3, 4	Power Fail From Arithematic Unit
CRUSEL 7, 11, 15-	6	
CRUSEL 6, 10, 14-	8	Connectors $FF0_9$
CRUSEL 5, 9, 13-	10	EF1, EF2 Only
CRUSEL 4, 8, 12-	49	
MRESET-	11, 12	Master Reset- 0 = Power Supply Not Up
CPU DATAOUT	15, 16	True Data From Arithematic Unit
STORECLK-	21, 22	False Clock- Low For 83 ns
35VAC	30, 31	35VAC For ±15V Supply Module, Mainframe Only (early CPU's only; now only in slot REG)
35VAC	32, 33	
CRUBIT15	33, 34	True Address
CRUBIT 14	37, 38	
CRUBIT 13	39, 40	
CRUBIT 12	41, 42*	
-5V **	35, 36	Present Only on 960A CPU's.
MODSELE-	46	Module Select For Second Set OFF 16 Address on 32 Address Module
MODSELF-	48	Module Select For First 16 Address
+15V	53, 54	
-15V	55, 56	
±15V GROUND	57, 58	
CRUBITIN	59, 60	True Data From CRU Module
RESERVED	61, 62	
CRUINTA-	65, 66	0 = Interrupt Connectors RR0 EF1, EF2 Only
CRUBIT 9	67, 68	
CRUBIT 8	69, 70	
CRUBIT 10	71, 72	
CRUBIT 11	73, 74	
MRESET-	75, 76	
VCC	77, 78	

Pin 41 of
*EF3 And EF4 Connectors is signature MODSELR8
** NOTE: This voltage should not be used for custom user applications.

4.2.5 SIGNAL TIMING

The timing of signals at a mainframe CRU module connector is shown in figure 4-2.

4.3 EXTERNALLY EXPANDED CRU SYSTEM

An externally expanded CRU system includes the CRU interface card, CRU expander cards, and CRU expansion units. CRU expander cards are only required when the system includes more than two 32-line expansion units or four 16-line expansion units.

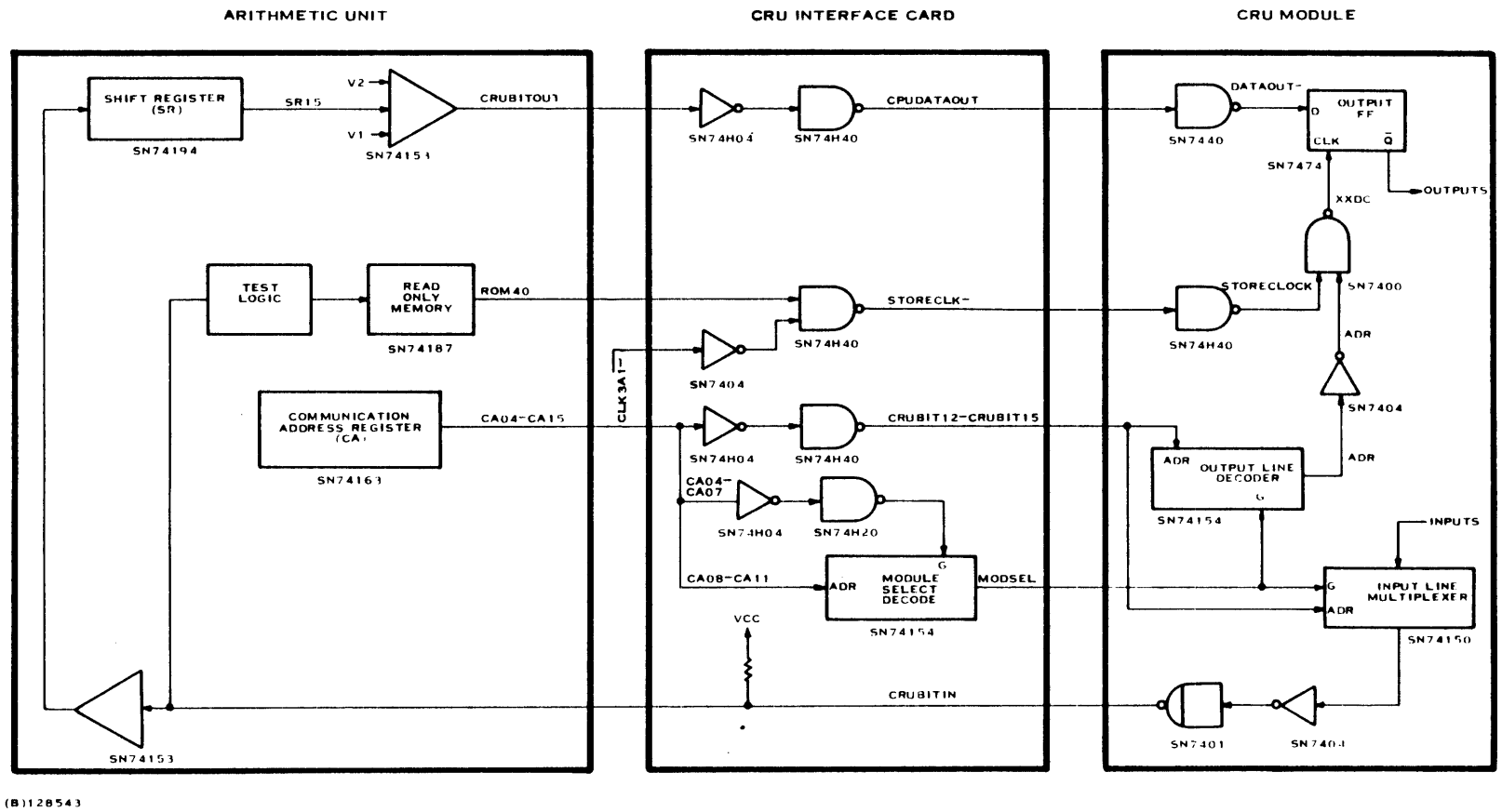


Figure 4-1. Mainframe CRU System-Signal Flow Diagram

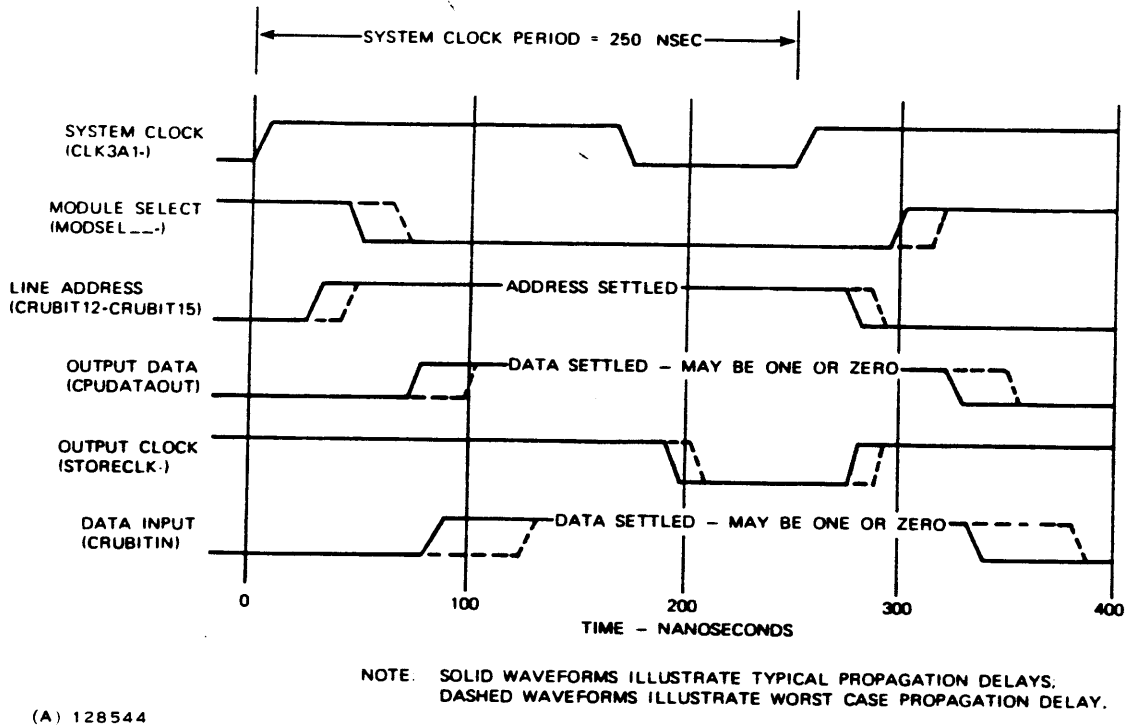


Figure 4-2. Mainframe CRU System - Timing Diagram

4.3.1 CRU INTERFACE

The CRU interface card (TI Drawing 226807) contains logic for generating expansion rack select signals and for buffering address and data signals that are supplied to expansion units which are connected to the top edge connector.

Address bits CA04 through CA07 are decoded by Z19 to produce rack select signals CRUSEL0- through CRUSEL15-. Signals CRUSEL0- through CRUSEL3- are buffered by an inverter and a line terminating resistor to drive the CRU expansion cable. Signals CRUSEL4- through CRUSEL15- are routed through P1 to the CRU expander cards. The STORECLK- signal is inverted by four gates and fanned out as signals ESTORECLOCK0 through ESTORECLOCK3.

Address bits CRUBIT8 through CRUBIT15 are inverted by cable drive circuits and fanned out to two signals for each bit, EBIT8A through EBIT15A and EBIT8B through EBIT15B.

Data and interrupt signals (B0 interrupt through B3 interrupt and B0 DATAIN- through B3 DATAIN-) from expansion units connected to the CRU interface card are routed to the inputs of open collector inverter circuits Z1 and Z2. The CRU interface card is assembled with jumpers which tie the inputs of the data and interrupt inverters to ground. The jumper associated with each expansion unit that has been installed must be removed. (See table 4-2 for

Table 4-2. Jumper Schedule for CRU Expansion

Expansion To	Expanding from CRU Interface		Expanding from CRU Expander	
	DATIN– Remove Jumpers	INTERRUPT– Remove Jumpers	DATAIN– Remove Jumpers	INTERRUPT– Remove Jumpers
One 16 or 32 Address Chassis	E11-E12	E1-E4	E16-E12	E8-E4
Two 16 or 32 Address Chassis	E11-E12, E15-E16	E1-E4, E5-E6	E16-E12, E13-E9	E8-E4, E7-E3
Three 16 Address Chassis	E11-E12, E15-E16 E9-E10	E1-E4, E5-E6 E3-E2	E16-E12, E13-E9 E14-E10	E8-E4, E7-E3 E6-E2
Four 16 Address Chassis	E11-E12, E15-E16 E9-E10, E13-E14	E1-E4, E5-E6 E3-E2, E7-E8	E16-E12, E13-E9 E14-E10, E15-E11	E8-E4, E7-E3 E6-E2, E5-E1

details). Outputs of the interrupt inverters are tied together and connected to CRU interrupt bus CRUINT-. The four data inverter outputs are connected to CRU input data bus CRUBITIN.

4.3.2 CRU EXPANDER

The CRU expander card (TI Drawing 214096) provides buffering and signal flow for the CRU interface to expansion units. Data and interrupt signals from the expansion units are wired in an AND configuration to the CRUINTA- and CRUBITIN busses. The circuits used for these purposes are identical to those used on the CRU interface card as described in paragraph 4.3.1.

4.3.3 BUFFER

The interface between the CRU expander and CRU modules in a CRU expansion unit is the buffer card. (See TI Drawing 217354).

A 1 of 16 decoder (Z3) on the buffer card is enabled by the ERACKSEL signal and addressed by CRU address bits 8 through 11 (EBIT8- through EBIT11-). This decoder generates module select signals (CRUSEL0- through CRUSEL15-) for 16-line CRU modules or for the first 16-line set in 32-line modules.

A second 1 of 16 decoder (Z1) is enabled by the next ERACKSEL signal in sequence and addressed by CRU address bits 8 through 11. Outputs of Z1 are the module select signals for the second 16-line set in a 32-line data module.

All other signals between the CRU interface and expansion modules are inverted on the buffer card. Signals to the CRU modules are inverted using nand buffers to provide sufficient drive for 16 modules. Data and interrupt signals from the CRU modules to the CRU interface are buffered by series terminated line driver circuits.

4.3.4 CRU MODULE

The CRU modules in a CRU expansion unit are designed to function the same as modules installed in the mainframe. Pin assignments for the CRU module connectors are also the same as mainframe connector listed in table 4-1. CRU module connector spacing in the expansion unit is adequate for the installation of any module type in any location.

4.3.5 SIGNAL LEVELS

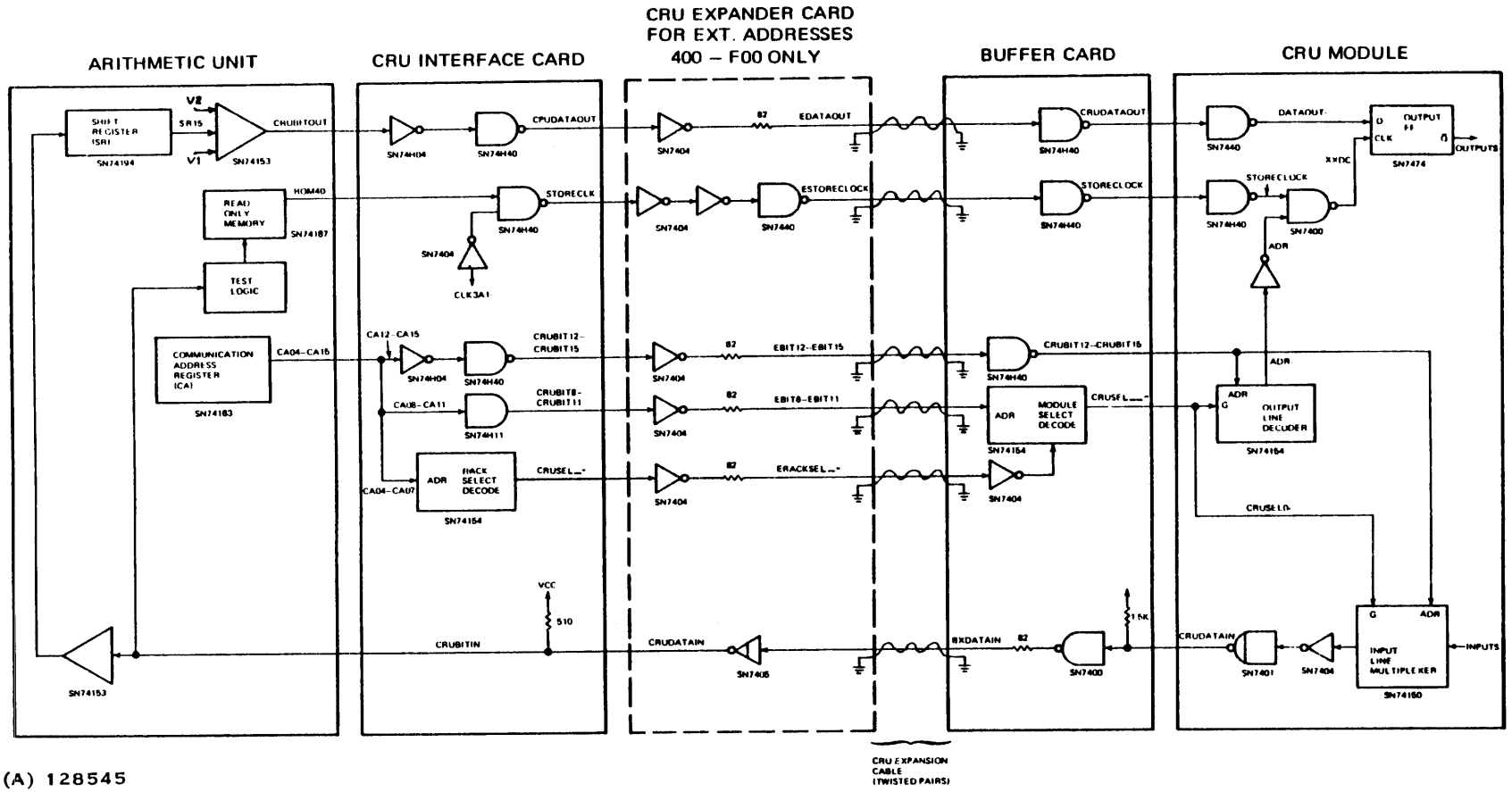
All signals between the buffer card and CRU modules are standard TTL levels of 0.0 to +0.4 volts for a logic ZERO and +2.4 to +5.0 volts for a logic ONE.

4.3.6 SIGNAL FLOW

Figure 4-3 shows the path through which address and data signals must propagate from the CPU to an external CRU module and back. The CRU expander buffer circuits may be located on the expander card or the CRU interface card for different expansion units.

4.3.7 SIGNAL TIMING

Figure 4-4 is a timing diagram for signals at the CRU module connector in an external expansion unit. Time delays for output signals include 40 nanoseconds for propagation through the CRU expansion cable. This cable delay is based on a delay of two nanoseconds for each 305 mm (one foot) for the maximum stock cable length of 3.66 m (12 feet). Cable lengths of up to 15.2 m (50 feet) may be used without exceeding the data input timing margin.



(A) 128545

Figure 4-3. External CRU Expansion - Signal Flow Diagram

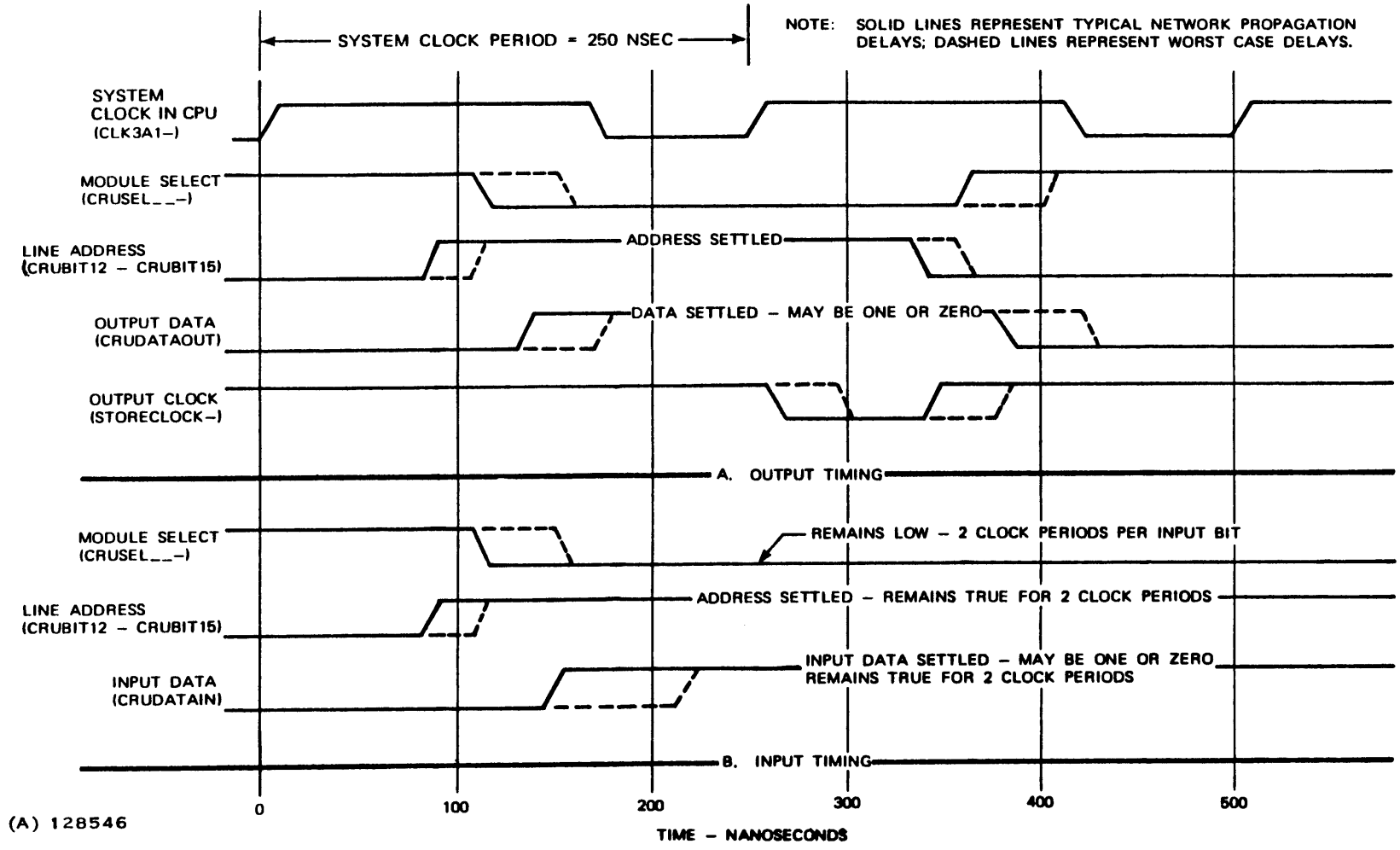


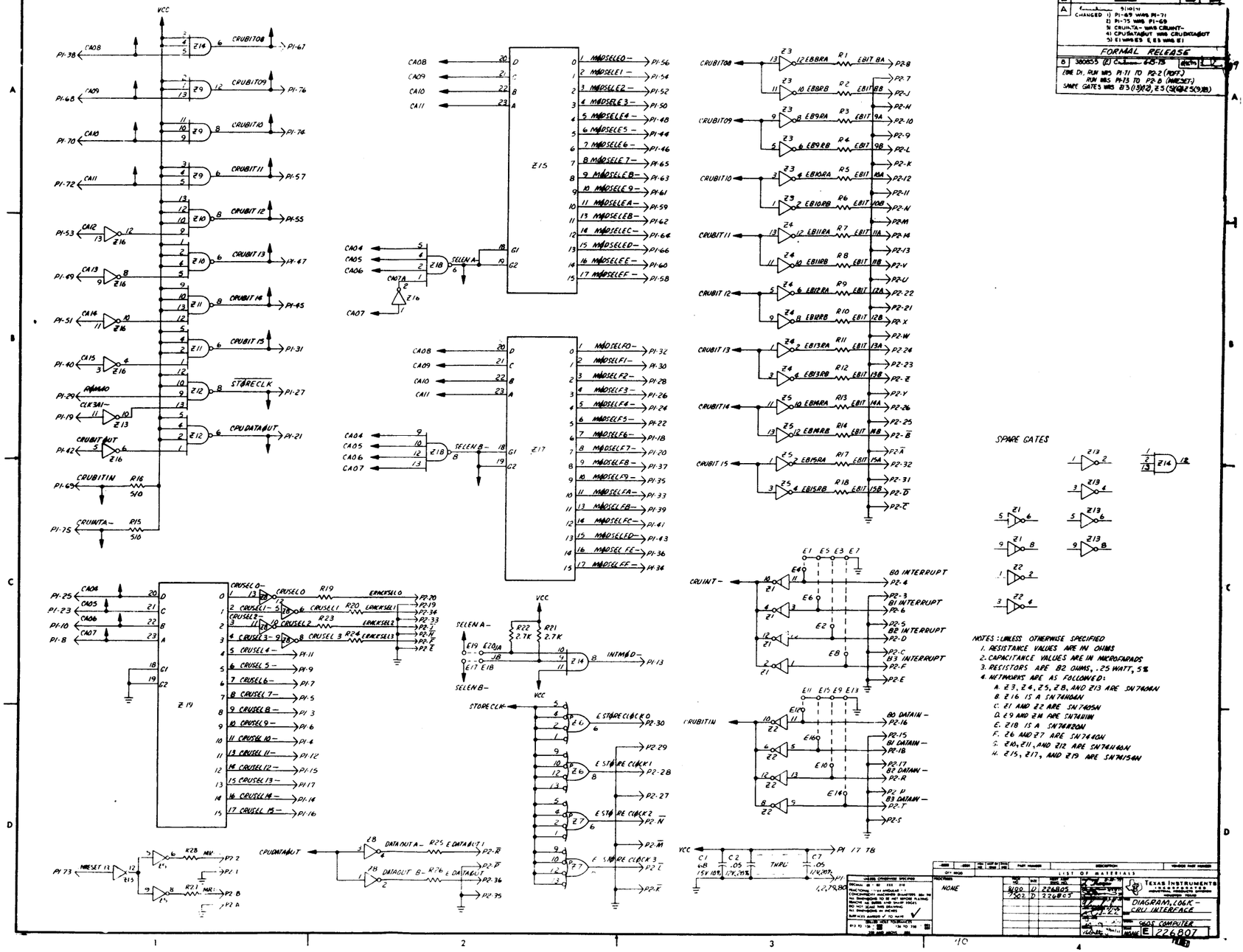
Figure 4-4. External CRU Expansion - Signal Timing

SECTION V

ELECTRICAL DRAWINGS

The following electrical drawings are included to complement the detailed discussions of the CRU:

Title	Drawing No.	Page No.
CRU Interface Module	226807	5-3
CRU Expander Module	214096	5-5
CRU Buffer Module	217354	5-7


VCC
CA08
CA09
CA10
CA11
CA12
CA13
CA14
CA15
CA16
CRUBIT08
CRUBIT09
CRUBIT10
CRUBIT11
CRUBIT12
CRUBIT13
CRUBIT14
CRUBIT15
STORECLK
CPUDATAOUT
CRUBITOUT
CRUBITIN
CRUINTA-
RAMAD
CLK3A1-
MRESET
Z15
Z17
Z19
SELEN A-
SELEN B-
INTMBD-
STORE CLK-
E STORE CLOCK 0
E STORE CLOCK 1
E STORE CLOCK 2
E STORE CLOCK 3
DATAOUT A-
DATAOUT B-
E DATABIT 1
E DATABIT
MADSELE0-
MADSELE1-
MADSELE2-
MADSELE3-
MADSELE4-
MADSELE5-
MADSELE6-
MADSELE7-
MADSELE8-
MADSELE9-
MADSELEA-
MADSELEB-
MADSELEC-
MADSELED-
MADSELEE-
MADSELEF-
MADSELF0-
MADSELF1-
MADSELF2-
MADSELF3-
MADSELF4-
MADSELF5-
MADSELF6-
MADSELF7-
MADSELF8-
MADSELF9-
MADSELFA-
MADSELFB-
MADSELFC-
MADSELFD-
MADSELFE-
MADSELFF-
CRUSEL0-
CRUSEL1-
CRUSEL2-
CRUSEL3-
CRUSEL4-
CRUSEL5-
CRUSEL6-
CRUSEL7-
CRUSEL8-
CRUSEL9-
CRUSELA-
CRUSELB-
CRUSELC-
CRUSELD-
CRUSELE-
CRUSELF-
EBBRA
EBBRB
EBIORA
EBIORB
EBIIRA
EBIIRB
EBI2RA
EBI2RB
EBI3RA
EBI3RB
EBI4RA
EBI4RB
EBI5RA
EBI5RB
EBIT 8A
EBIT 8B
EBIT 9A
EBIT 9B
EBIT 10A
EBIT 10B
EBIT 11A
EBIT 11B
EBIT 12A
EBIT 12B
EBIT 13A
EBIT 13B
EBIT 14A
EBIT 14B
EBIT 15A
EBIT 15B
80 INTERRUPT
B1 INTERRUPT
B2 INTERRUPT
B3 INTERRUPT
80 DATAIN -
B1 DATAIN -
B2 DATAIN -
B3 DATAIN -
SPARE GATES
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS
2. CAPACITANCE VALUES ARE IN MICROFARADS
3. RESISTORS ARE 82 OHMS, .25 WATT, 5%
4. NETWORKS ARE AS FOLLOWED:
A. Z3, Z4, Z5, Z8, AND Z13 ARE SN7406N
B. Z16 IS A SN74H04N
C. Z1 AND Z2 ARE SN7405N
D. Z9 AND Z11 ARE SN74111N
E. Z18 IS A SN74820N
F. Z6 AND Z7 ARE SN74104N
G. Z10, Z11, AND Z12 ARE SN74H40N
H. Z15, Z17, AND Z19 ARE SN74154N
DIAGRAM, LOGIC - CRU INTERFACE
9900 COMPUTER
E 226807

5-3/5-4

REVISIONS			
LTR	DESCRIPTION	DATE	APPD

CRUBIT 8 P1-70 — E1 R21 82 — E BIT 8A — P2-8 / P2-7 / SIGGND
E2 R20 82 — E BIT 8B — P2-J / P2-H / SIGGND

CRUBIT 9 P1-68 — E3 R19 82 — E BIT 9A — P2-10 / P2-9 / SIGGND
E4 R18 82 — E BIT 9B — P2-L / P2-K

CRUBIT 10 P1-72 — E5 R17 82 — E BIT 10A — P2-12 / P2-11 / SIGGND
E6 R16 82 — E BIT 10B — P2-N / P2-M / SIGGND

CRUBIT 11 P1-74 — E7 R15 82 — E BIT 11A — P2-14 / P2-13 / SIGGND
E8 R14 82 — E BIT 11B — P2-V / P2-U / SIGGND

CRUBIT 12 P1-42 — E9 R13 82 — E BIT 12A — P2-22 / P2-21 / SIGGND
E10 R12 82 — E BIT 12B — P2-X / P2-W / SIGGND

CRUBIT 13 P1-40 — E11 R11 82 — E BIT 13A — P2-24 / P2-23 / SIGGND
E12 R10 82 — E BIT 13B — P2-Z / P2-Y / SIGGND

CRUBIT 14 P1-38 — E13 R9 82 — E BIT 14A — P2-26 / P2-25 / SIGGND
E14 R8 82 — E BIT 14B — P2-B / P2-A / SIGGND

CRUBIT 15 P1-34 — E15 R7 82 — E BIT 15A — P2-32 / P2-31 / SIGGND
E16 R6 82 — E BIT 15B — P2-D / P2-C / SIGGND

CRU SEL 0- P1-49 — E17 R24 82 — E RACK SEL 0 — P2-20 / P2-19 / SIGGND
CRUSEL 1- P1-10 — E18 R3 82 — E RACK SEL 1 — P2-34 / P2-33 / SIGGND
CRUSEL 2- P1-8 — E19 R4 82 — E RACK SEL 2 — P2-J / P2-H / SIGGND
CRU SEL 3- P1-6 — E20 R5 82 — E RACK SEL 3 — P2-F / P2-E / SIGGND

STORECLOCK P1-22 — E21 — E STORECLOCK 0 — P2-30 / P2-29 / SIGGND
E STORECLOCK 1 — P2-28 / P2-27 / SIGGND
E STORECLOCK 2 — P2-N / P2-M / SIGGND
E STORECLOCK 3 — P2-L / P2-K / SIGGND

GROUND — WIRE JUMPERS SEE NOTE 3
CRUINT- P1-66 — E4 — BO INTERRUPT — P2-4 / P2-3 / SIGGND
E3 — B1 INTERRUPT — P2-6 / P2-5 / SIGGND
E2 — B2 INTERRUPT — P2-D / P2-C / SIGGND
E1 — B3 INTERRUPT — P2-F / P2-E / SIGGND

GROUND — WIRE JUMPERS SEE NOTE 6
CRUDATAIN P1-60 — E12 — BO DATAIN- — P2-16 / P2-15 / SIGGND
E9 — B1 DATAIN- — P2-18 / P2-17 / SIGGND
E10 — B2 DATAIN- — P2-R / P2-P / SIGGND
E11 — B3 DATAIN- — P2-T / P2-S / SIGGND

CPUDATAOUT P1-16 — E23 R1 82 — E DATAOUT 1- — P2-R / P2-P / SIGGND
E24 R2 82 — E DATAOUT- — P2-36 / P2-35 / SIGGND

CRUMR- P1-76 — E23 R22 82 — MRI- — P2-B / P2-A / SIGGND
E24 R23 82 — MR- — P2-2 / P2-1 / SIGGND
} NOTE 5

NC — NC
NC — NC
NC — NC
NC — NC
NC — NC
NC — NC
} SPARES

P1-77,78 — C1 50 15V; C2 0.1 10V; C3 0.1 10V; C4 0.1 10V; C5 0.1 10V — VCC
P1-1,2,79,80 — GRD

REFERENCE DESIGNATORS	
USED	NOT USED
Z1, Z2, Z3, Z4, Z6, Z7, Z8, Z9, Z10	Z5

NOTES:
UNLESS OTHERWISE SPECIFIED;
1. RESISTORS ARE .25 W ± 5%.
2. RESISTANCE VALUES ARE IN OHMS.
3. CAPACITANCES VALUES IN MICROFARADS.
4. NETWORKS ARE AS FOLLOWS:
   A) Z7, Z8, ARE SN7440N.
   B) Z9 & Z10 ARE SN7405N
   C) Z1, Z2, Z3, Z4, & Z6 SN7404
5. THESE OUTPUTS TO BE USED ONLY ON SPECIAL SYSTEMS WHERE APPLICABLE.
6. CUT JUMPER IF INPUT IS TO BE USED. JUMPER REMOVALS ALLOW EXPANSION TO 4 CRU RACKS FROM 1 EXPANDER BOARD. SEE SPEC # 217329 FOR JUMPER SCHEDULE.

-0002	-0001	ITEM NO	UNIT OF ISSUE	SYMB SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
QTY REQD							

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DECIMAL XX ± .02 XXX ± .010
FRACTIONAL 1/64 ANGULAR ±
CONCENTRICITY MACHINED DIAMETERS .004 TIR
ALL DIMENSIONS TO BE MET BEFORE PLATING
REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING
ALL DIMENSIONS IN INCHES
SURFACES MARKED √ TO HAVE
DRILLED HOLE TOLERANCES
.013 TO .136 .002 .003
.250 AND ABOVE .003 .004

PROCESSES: NONE

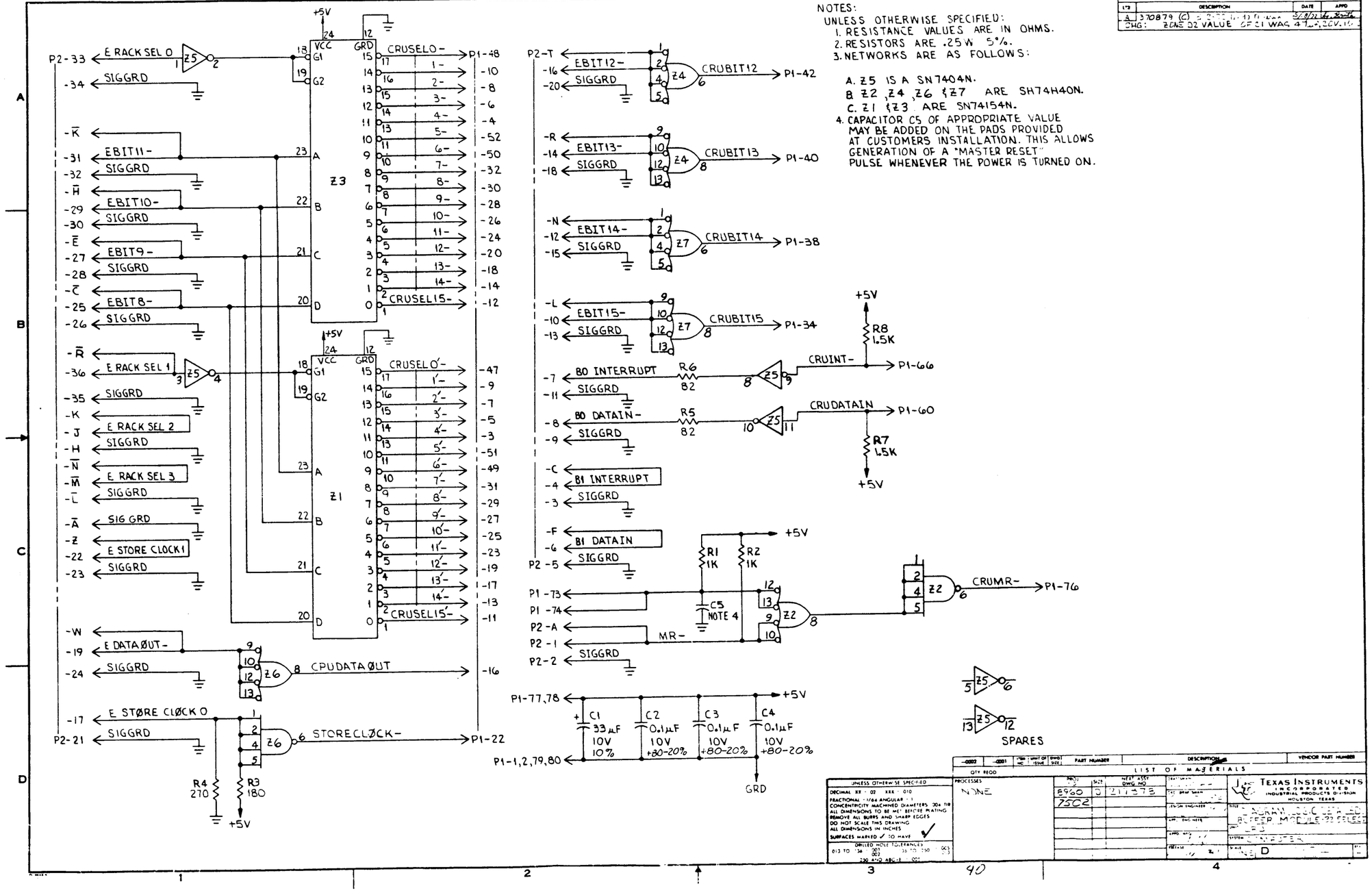
PROJ NO 9960 | SIZE D | NEXT ASSY DWG NO 2409S | 7502

DRAWN 6-5-73
CHECKED
ENGR APPD
MFG APPD
QUAL APPD
PROJ ENGR
MFG ENGR

TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON, TEXAS

DIAGRAM LOGIC DETAILED EXPANDER

SIZE D


NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS.
2. RESISTORS ARE .25W 5%.
3. NETWORKS ARE AS FOLLOWS:
A. Z5 IS A SN7404N.
B Z2, Z4, Z6 & Z7 ARE SH74H40N.
C. Z1 & Z3 ARE SN74154N.
4. CAPACITOR C5 OF APPROPRIATE VALUE MAY BE ADDED ON THE PADS PROVIDED AT CUSTOMERS INSTALLATION. THIS ALLOWS GENERATION OF A "MASTER RESET" PULSE WHENEVER THE POWER IS TURNED ON.
REVISIONS
LTR DESCRIPTION DATE APPD
A 370879 (C) 5/8/72
CHG: ZONE D2 VALUE OF C1 WAS 47 MF, 20V.
E RACK SEL 0
SIGGRD
EBIT11-
EBIT10-
EBIT9-
EBIT8-
E RACK SEL 1
E RACK SEL 2
E RACK SEL 3
E STORE CLOCK1
SIG GRD
E DATAOUT-
E STORE CLOCK 0
CRUSELO-
CRUSEL15-
CRUSELO'-
CRUSEL15'-
CPUDATAOUT
STORECLOCK-
EBIT12-
EBIT13-
EBIT14-
EBIT15-
CRUBIT12
CRUBIT13
CRUBIT14
CRUBIT15
BO INTERRUPT
BO DATAIN-
B1 INTERRUPT
B1 DATAIN
CRUINT-
CRUDATAIN
CRUMR-
MR-
R1 1K
R2 1K
R3 180
R4 270
R5 82
R6 82
R7 1.5K
R8 1.5K
C1 33µF 10V 10%
C2 0.1µF 10V +80-20%
C3 0.1µF 10V +80-20%
C4 0.1µF 10V +80-20%
C5 NOTE 4
+5V
GRD
SPARES
LIST OF MATERIALS
UNLESS OTHERWISE SPECIFIED
PROCESSES
NONE
TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON, TEXAS
SIZE D

USER'S RESPONSE SHEET

Manual Title: Model 960 Computer Communications Register Unit Manual (966313-9701)

Manual Date: 1 May 1977 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

CUT ALONG LINE

Location in Manual	Comment/Suggestion

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