TEXAS INSTRUMENTS

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Model 990/4 Computer System

Field Maintenance Manual

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Model 990/4 Computer System Field Maintenance Manual (945401-9701)

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PREFACE

This manual provides field-level operation and maintenance information required to service the Texas Instruments Model 990/4 Microcomputer System. This manual is intended for use by trained Customer Service Engineers or other qualified maintenance personnel assigned to 990/4 field service support.

This manual contains a brief physical and functional description of the 990/4 system and describes all hardware options and system configurations. The manual also contains a description of the Model 990 Maintenance Unit used to load diagnostics and manually control a "down" system not equipped with a programmer panel or operable 733 ASR data terminal. Fault isolation procedures are also provided to permit rapid tracing of system malfunctions down to the replaceable logic board or cable (or replaceable IC level in some cases). Packaging and shipping instructions are also provided to permit safe shipment of the faulty board(s) back to the factory or other authorized depot maintenance facility where board repair is performed.

Field service instructions for the peripheral subsystems in the 990/4 Microcomputer System are covered in a separate manual entitled *Model 990 Computer Peripheral Equipment Field Maintenance Manual.*

This manual is organized into six major sections and four appendixes including:

I. General Description – Provides an introduction to the Model 990/4 Microcomputer System; describes the physical construction of the system and covers the various hardware options and system configurations which are currently available.

II. Field Service Test Equipment – Describes the 990 Maintenance Unit controls and indicators and provides test setup cabling diagrams for typical system installations. This section also lists the diagnostic tests that are currently available to support field maintenance and provides a list of recommended tools and test equipment.

III. Maintenance – Provides preventive and corrective maintenance procedures for the 990/4 system. This section describes the procedures for installing jumper-wire options and custom ROMs on replacement boards prior to substituting a spare board for a faulty board.

IV. Troubleshooting – Provides a systematic procedure for checking out a system and for tracing system malfunctions down to a replaceable subassembly. After the trouble has been isolated down to a replaceable unit, the unit is replaced in accordance with the instructions in Section III. The system checkout procedures in Section IV should then be repeated to ensure that the system is functioning properly.

V. Troubleshooting Diagrams – Contains a collection of system-level diagrams useful in performing field maintenance fault isolation and repair on the 990/4 system. This section includes a block diagram of each board type used in the 990/4 microcomputer.

VI. Packing and Shipping – Contains instructions for repacking faulty assemblies for shipment back to the factory or other authorized depot maintenance facility.

A. Programming Reference Information – Provides a summary of 990 programming information required for field maintenance of the system.

B. Interrupt Vector Table – Provides a tabular list of interrupt levels and vector locations.

C. Device CRU Formats – Lists and describes the CRU formats associated with the card reader, TTY/EIA devices, and the 913 display system.

D. Hexadecimal to Decimal Conversion Charts

E. Scoping Loop Programs – Provides a collection of commonly used scoping loop programs which may be entered into program memory via the programmer's panel.

RELATED PUBLICATIONS

The following hardware, software and diagnostics publications are available to support programming, operation and maintenance of 990/4 systems:

PROGRAMMING. The following manual provides a detailed description of the instructions, the form and use of assembly language, plus programming conventions.

Title	Part Number
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701

INSTALLATION AND OPERATION. The following series of manuals provide complete information to install and operate 990 peripheral devices including detailed unpacking, installation, operator controls and programming information.

Title	Part Number
Model 990 Computer Model 913 CRT Display Terminal Installation and Operation	943457-9701
Model 990 Computer Floppy Disc Installation and Operation Guide	945253-9701
Model 990/4 Program Development System Operation Guide	945254-9701
Model 990 Computer Prototyping System Operation Guide	945255-9701
Model 990 Computer PROM Programming Model Installation and Operation	945258-9701
Model 990 Computer 733 ASR/KSR Terminal Installation and Operation	945259-9701
Model 990 Computer Line Printer Installation and Operation	945261-9701

Title	Part Number
Model 990 Computer Card Reader Installation and Operation	945262-9701
Model 990 Computer Communications System Installation and Operation	945409-9701

HARDWARE. This manual presents a technical description of all hardware components in the processing unit. It includes interface descriptions, installation and operating instructions, electrical characteristics, and other essential data concerning the processor and associated chassis.

Title	Part Number
Model 990/4 Computer System Hardware Reference Manual	945251-9701

MAINTENANCE. The following manuals contain troubleshooting procedures for fault isolation to a replaceable assembly for each optional peripheral device. Also included are preventive maintenance requirements, disassembly, repair, and assembly instructions. These manuals are required for maintenance of any peripheral within the system.

Title	Part Number
Model 990 Computer Family Peripheral Equipment Field Maintenance Manual	945419-9701
Model 990 Computer Family Maintenace Drawings Volume I – Processors	945421-9701*
Model 990 Computer Family Maintenance Drawings Volume II – Peripherals	945421-9702*

*Manual common to both Field and Depot level maintenance

The following manuals are available to enable qualified personnel to repair (at the component level) the major assemblies.

Title	Part Number
Model 990/4 Computer System Depot Maintenance Manual	945403-9701
Model 990 Computer PROM Programming Module Depot Maintenance Manual	945405-9701
Model 990 Computer Model 913 CRT Display Terminal Depot Maintenance Manual	945406-9701
Model 990 Computer 16 Input/Output TTL Data Module Depot Maintenance Manual	945407-9701

Title	Part Number
Model 990 Computer Full Duplex EIA Module Depot Maintenance Manual	945408-9701
Model 990 Computer 16 Input/Output EIA Data Module Depot Maintenance Manual	945415-9701
Model 990 Floppy Disc Depot Maintenance Manual	945418-9701
Model 990 Computer Family Maintenance Drawings Volume I – Processors	945421-9701*
Model 990 Computer Family Maintenance Drawings Volume II – Peripherals	945421-9702*

*Manual common to both Field and Depot level maintenance

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SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This section provides a brief physical and functional description of the 990/4 Microcomputer System manufactured by Texas Instruments Incorporated, Austin, Texas. This section also describes the various system- and board-level options available with the 990/4 system.

1.2 990/4 MICROCOMPUTER SYSTEM DESCRIPTION

The 990/4 Microcomputer System is a modular data processing system (or general purpose hardware controller in some applications) which is constructed around the Texas Instruments Model 990/4 microcomputer and a wide range of supporting peripherals and controllers.

Typically, a system includes one or more 990/4 microcomputers, one or more (maximum of seven) 990 expansion chassis, and a combination of peripherals and terminals including:

- 911 CRT
- 913A video display terminals
- 733 ASR/KSR data terminals
- 745 KSR data terminals
- 804 card readers
- 306, 588, 2230, or 2260 line printers
- 990 floppy discs
- Customer-designed controllers
- Communications network

A simplified block diagram of a typical 990/4 Microcomputer System is shown in figure 1-1. The 990/4 microcomputer and the I/O expansion chassis are described in greater detail in the following paragraphs. For a description of the peripherals and data terminals, refer to the *Model 990 Peripheral Equipment Field Maintenance Manual.*

1.2.1 **990/4 MICROCOMPUTER.** The 990/4 microcomputer is a general-purpose computer available in three different chassis configurations with a wide-variety of optional memory boards, power supplies and I/O interface boards. Basically, the microcomputer consists of the following assemblies and subassemblies:

- 990/4 microcomputer board – Contains TMS 9900 microprocessor chip, two onboard memories including a 4K RAM and a 1K ROM/RAM and various microprocessor support functions such as clock generator, interrupt encoding logic and CRU interfacing logic.
- Optional 990/4 memory expansion board – Provides additional dynamic RAM memory in sizes ranging from 4K to 20K in 4K increments (factory expandable only).

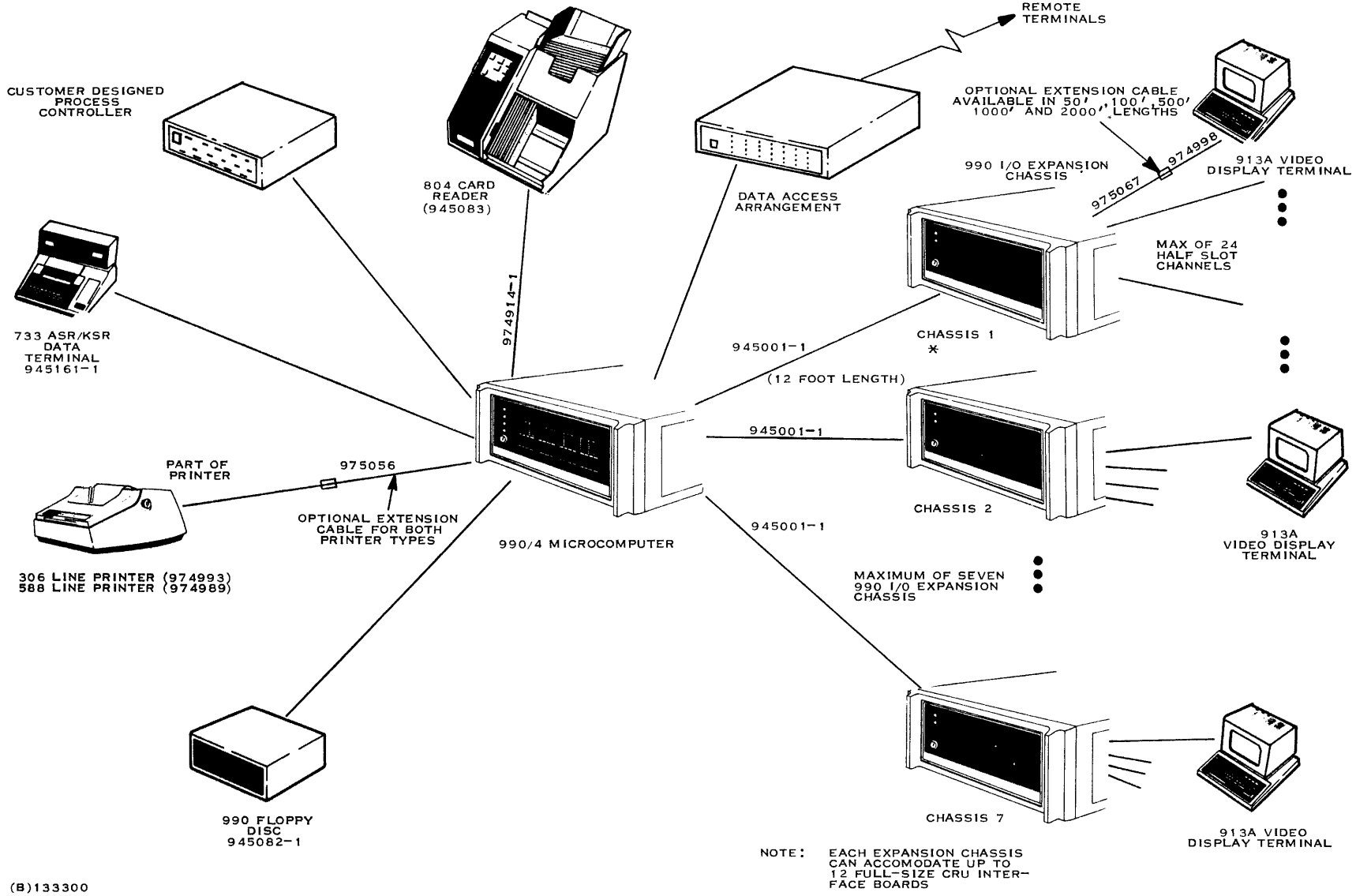


Figure 1-1. 990/4 Microcomputer System

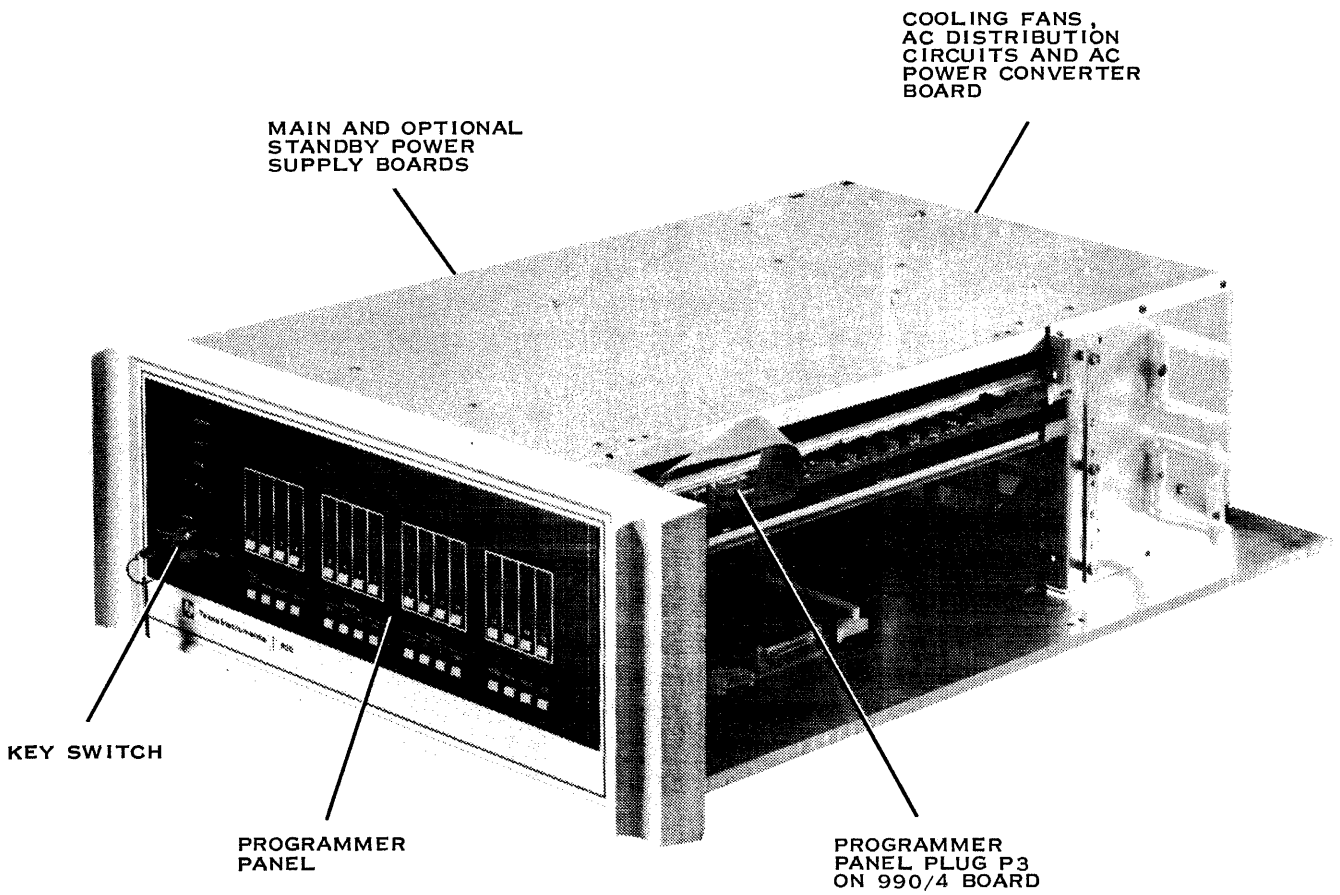
- Optional EPROM memory module – Contains erasable programmable read only memory (EPROM) in sizes ranging from 1K to 8K in 1K increments (field expandable).
- Optional CRU expansion board – Expands the I/O section of the 990/4 microcomputer board to accommodate up to seven additional I/O chassis.
- Optional I/O interface boards – Matches the interface requirements of the 990/4's serial I/O section (CRU) with the interface requirements of various peripherals and terminals in the system.
- Chassis – Houses the above described logic boards and contains built-in regulated power supplies, cooling fans and control panel for all configurations except the 3-slot OEM chassis.
- Optional standby power supplies

The 990/4 microcomputer assemblies and subassemblies are shown in figure 1-2. A simplified block diagram showing the board-level organization of the 990/4 microcomputer is provided in figure 1-3. A functional description of each of the major assemblies and subassemblies is presented in the following paragraphs.

1.2.1.1 **990/4 Microcomputer Board.** The 990/4 microcomputer board contains a TMS 9900 microprocessor chip and all necessary support functions such as on-board memory and clock circuits as found in a conventional minicomputer. The board functions include:

- Microprocessor
- Memory bus gating for external DMA controller
- 4-Phase clock generator
- IK ROM/RAM memory (static RAM)
- 4K MOS RAM Memory (Dynamic RAM)
- Programmer panel interface logic
- CRU interface section (I/O interface)
- Interrupt latches and encoding logic
- Real time clock logic
- External instruction decode (LREX, RSET, IDLE, CKON and CKOF)
- Clock and reset fanout logic
- Load control logic

A functional block diagram of the 990/4 microcomputer board is shown in figure 1-4 and a functional description of the board is provided in the following paragraphs.



(A)135900 (990-576-14-4)

Figure 1-2. 990/4 Microcomputer Assemblies and Subassemblies

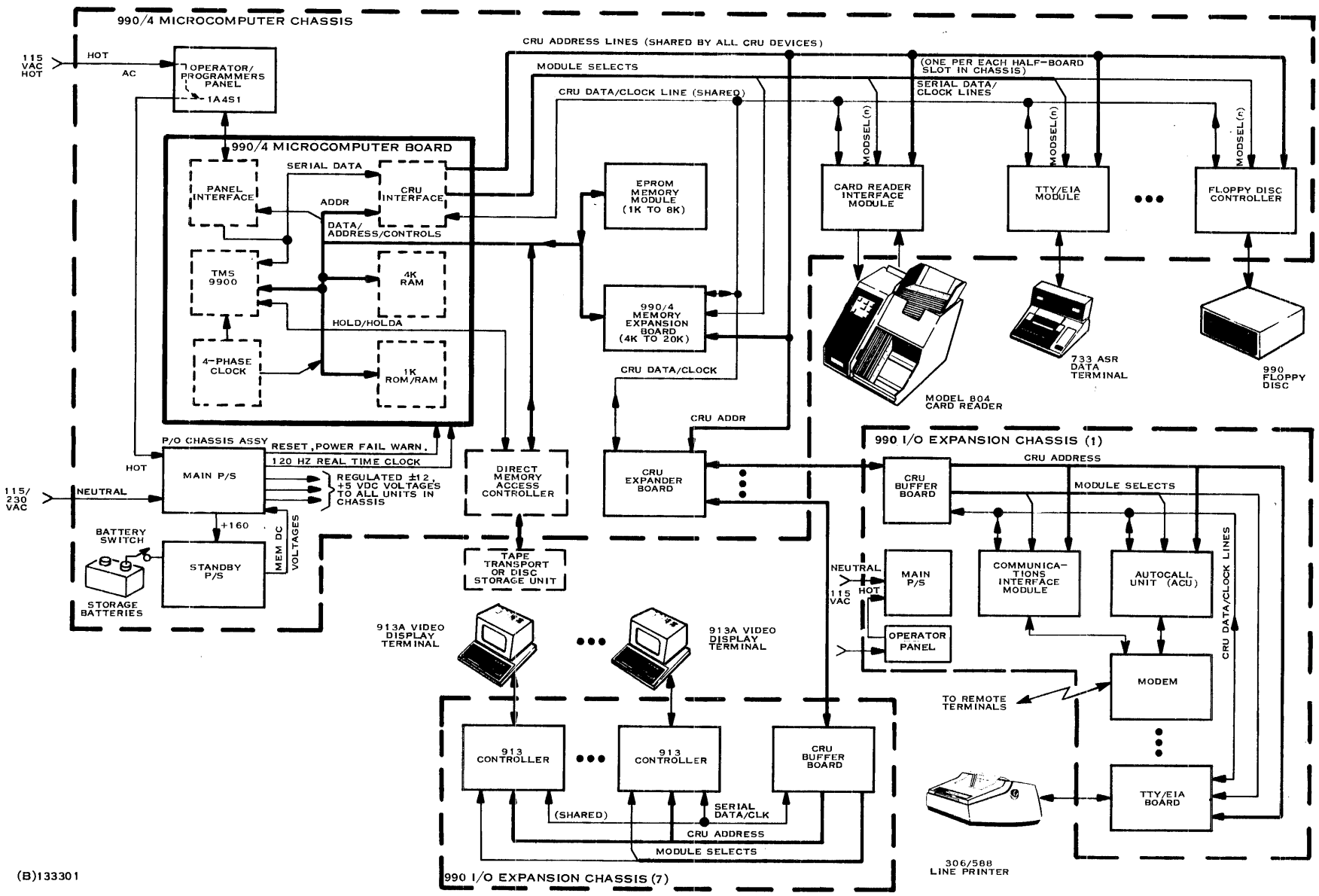


Figure 1-3. 990/4 Board Level Organization

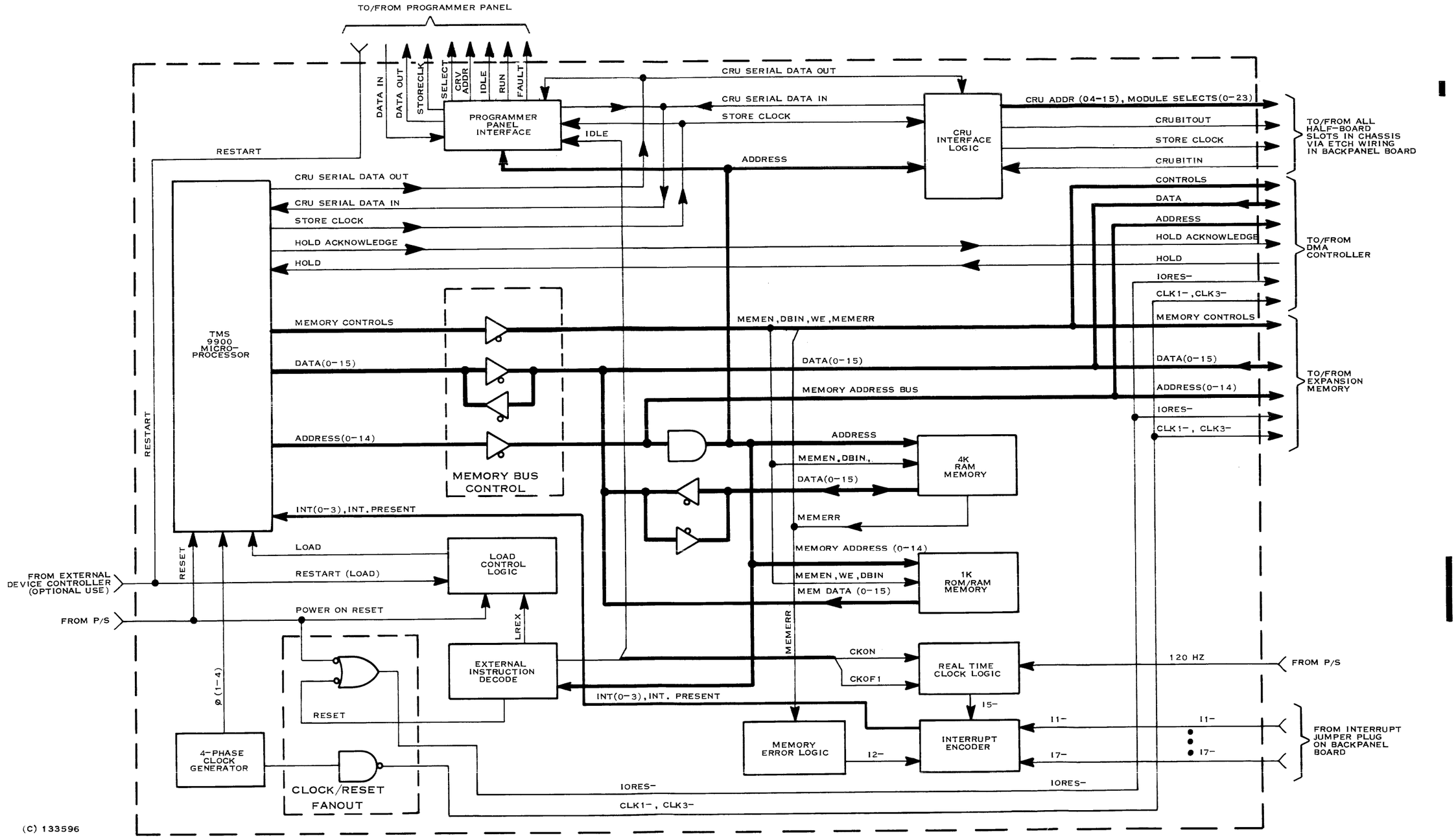


Figure 1-4. 990/4 Microcomputer Board, Functional Block Diagram

Microprocessor. The microprocessor function for the 990/4 microcomputer is provided by the TMS 9900 microprocessor chip. Basically, the chip contains all functions normally found in a minicomputer (with exception of memory which is implemented externally) plus such advanced features as memory-located workspace registers and a directly addressable memory address space of 32K 16-bit words.

The instruction set of the TMS 9900 allows both word and byte operands. Thus, all memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte. The memory space is 65536 bytes or 32768 16-bit words.

The TMS 9900 employs an advanced memory-to-memory architecture whereby blocks of 16 memory words designated as workspace registers replace internal hardware registers as program data registers. The TMS 9900 memory map (general purpose computer configuration) is shown in figure 1-5. As shown in this figure, the first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words ($FFFC_{16}$ and $FFFE_{16}$) are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

Three internal registers are accessible to the user including the program counter, status register and workspace pointer register. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is used by the processor to fetch the next instruction from memory and is then automatically incremented to develop the address of the next instruction in memory. The status register (ST) contains the interrupt mask level and other status information pertaining to the instruction operation. Each bit in the register signifies a particular function or condition that exists in the microprocessor. Some instructions use the status register to check for a prerequisite condition, others affect the values of the bits in the register, and others load the entire status register with a new set of parameters. A description of the instruction set contained in the *Model 990 Computer Assembly Language Programmer's Guide* details the effect of each instruction on the status register.

The workspace pointer register (WP) contains the address of the first word in the currently active set of workspace registers. A workspace register file occupies 16 contiguous memory words in the general memory area as shown in figure 1-6. Each workspace register may be used for data storage or function as operand registers, accumulators, address registers, or index registers. Some workspace registers take on special significance during execution of certain instructions as described in table 1-1. During instruction execution, the processor addresses any of the 16 workspace registers assigned to the program currently being executed by adding the register number to the contents of the workspace pointer as shown in figure 1-6.

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). For example, a context switch operation using a conventional multiregister arrangement would require numerous memory cycles to store and reload the contents of the register file. However, in the 990/4 the context switch is accomplished with only three store and three fetch cycles which results in exchanging the contents of the program counter, status register, and workspace pointer. After the switch, the workspace pointer in the microprocessor contains the starting address of a new 16-word workspace in memory for use with the new routine and the contents of the WP, PC, and ST registers from the previous routine are saved in workspace registers 13, 14, and 15, of the new workspace. The data and addresses in the remaining 12 registers of the

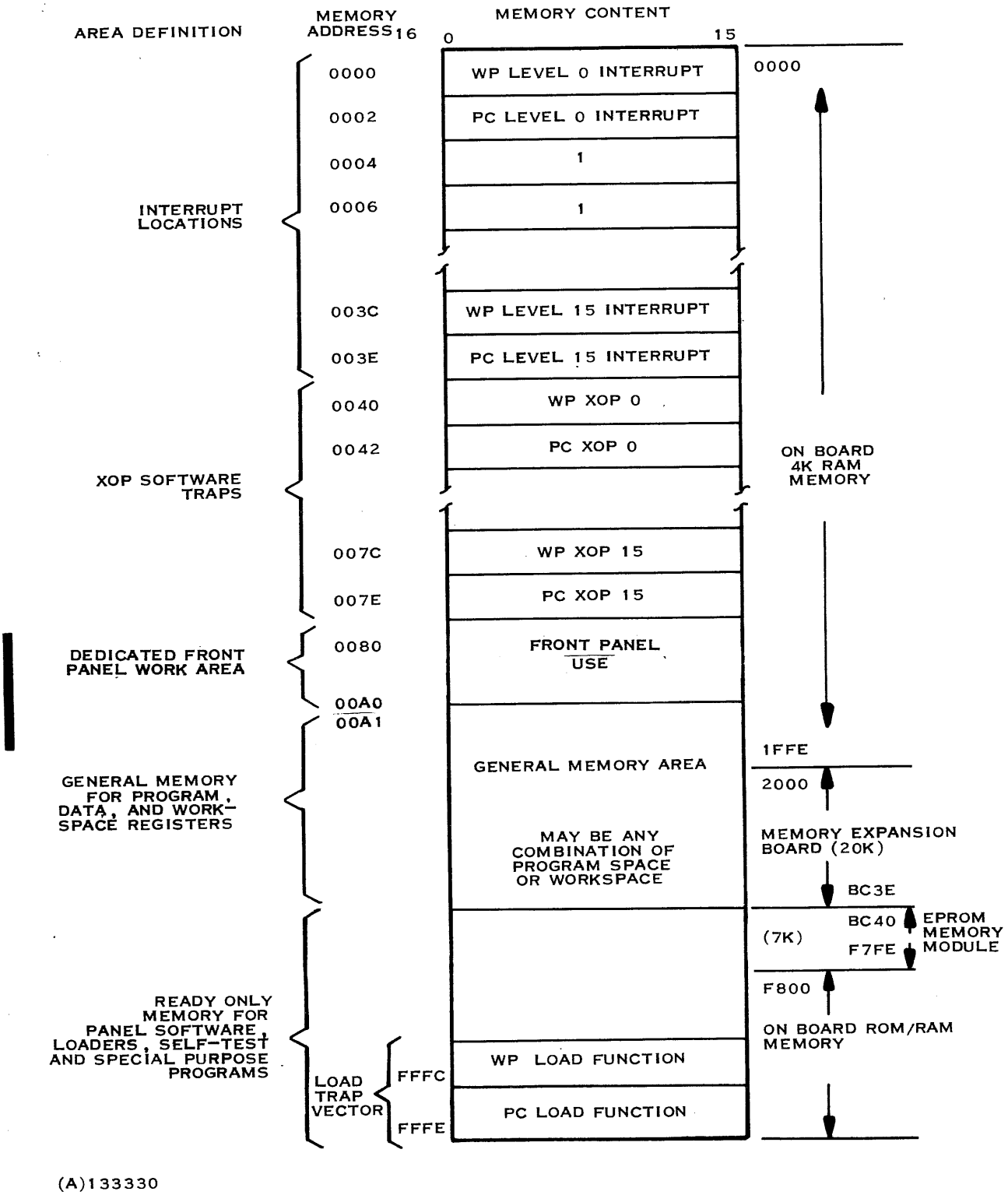


Figure 1-5. 990/4 Memory Map (General Purpose Computer Configuration)

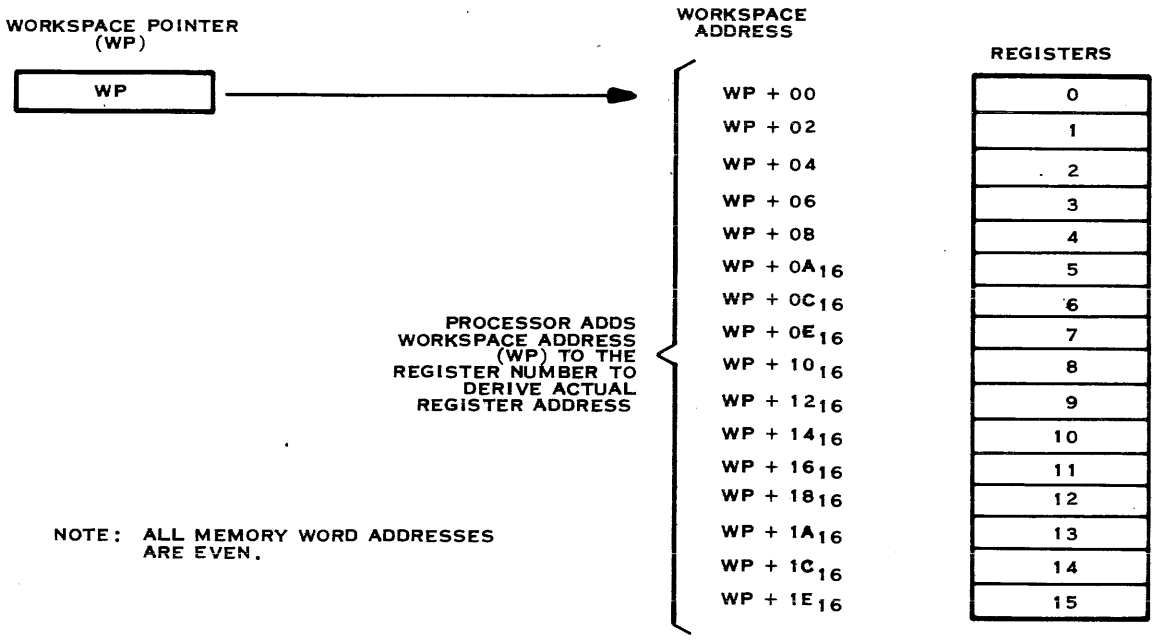


Figure 1-6. Workspace Pointer and Registers

Table 1-1. Dedicated Workspace Registers

Register No.	Contents	Used During
0	Shift count (optional)	Shift instructions (SLA, SRA, SRC and SRL)
11	Return address	Branch and Link (BL) instruction
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR, and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)
14	Saved PC register	Same as above
15	Saved ST register	Same as above

original workspace remain in memory until a switch is made back to the original program. A corresponding saving in time occurs when the original context is restored. The instructions in the microprocessor that result in a context switch include:

- Branch and Load Workspace Pointer (BLWP)
- Return from Subroutine (RTWP)
- Extended Operation (XOP)

Device interrupts, RESET– from the power supply, and LOAD– from the front panel (or LOAD external instruction from the 990/4 board) also cause a context switch by forcing the microprocessor to trap a service subroutine.

The TMS 9900 microprocessor can accommodate up to 16 interrupt levels (0 to 15) but only 8 levels are in the 990/4 configuration. Level 0 is the highest priority and is reserved for the RESET– function. Level 7 is assigned the lowest priority. Interrupt levels 1 through 7 are used for events external to the TMS 9900. Anytime power is applied to the system, the microprocessor continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the microprocessor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace. The microprocessor then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for level 0 interrupt that loads 0 into the mask. This allows only interrupts of higher priority to interrupt a service routine. The microprocessor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur. All interrupt requests must remain active until recognized by the microprocessor and the device- service routine. The individual service routines then reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower priority interrupt. All interrupt subroutines normally terminate with the return instruction which restores original program parameters.

The TMS 9900 microprocessor uses a versatile direct command-driven I/O interface designated as the Communications Register Unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of 1 to 16 bits. The microprocessor employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus at the interface to the CRU system. The microprocessor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its flexible data format, the CRU interface is used for a wide range of control and data transaction operations. These applications may be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The microprocessor instruction set includes three single-bit CRU instructions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the microprocessor develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the microprocessor generates a CRUCLK pulse and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a ONE for SBO and a ZERO for SBZ). The test bit instruction is an input operation that transfers the addressed CRU bit from CRUIN input line to bit 2 (equal bit) of the status register.

The microprocessor develops the CRU-bit address for the single-bit operations using the CRU base address in workspace register 12 (W12) and the signed displacement field (bits 8 through 15) of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 1-7 illustrates the development of a single-bit CRU address.

The microprocessor also performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in figure 1-8. Although the figure shows a full 16-bit transfer operation, any number of bits from 1 to 16 may be involved. The LDCR instruction fetches a word from memory and executes a series of right-shifts to serially transfer the word to the CRU device via the CRUBITOUT data line. If the LDCR involves 8 or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves 9 or more bits, those bits come from the

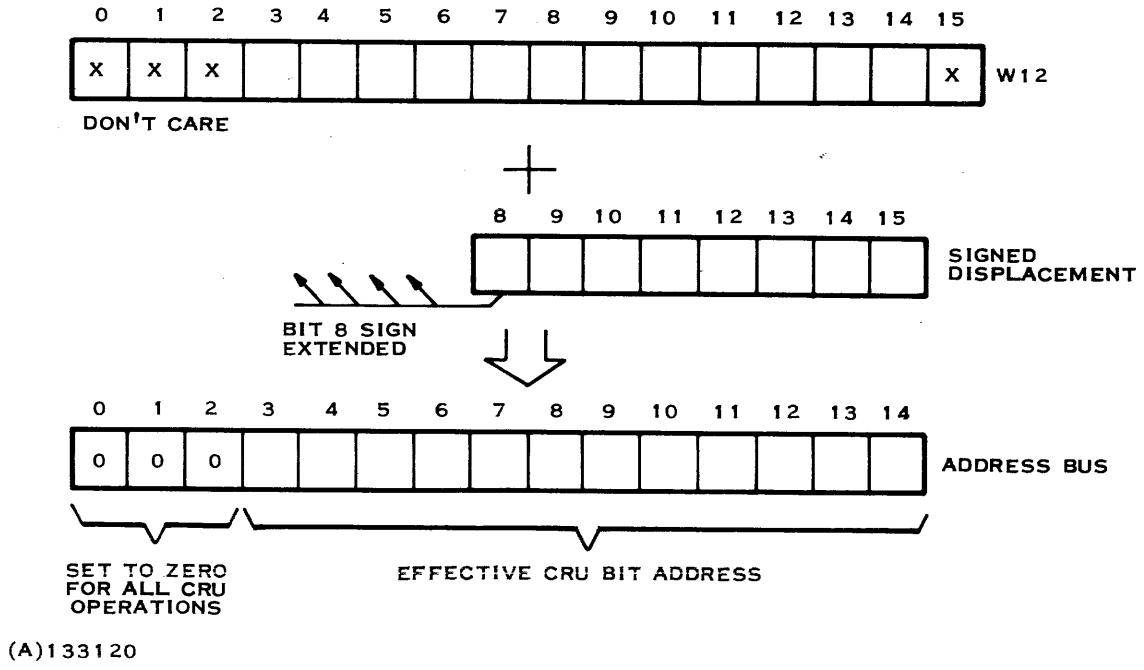


Figure 1-7. TMS 9900 Single-Bit CRU Address Development

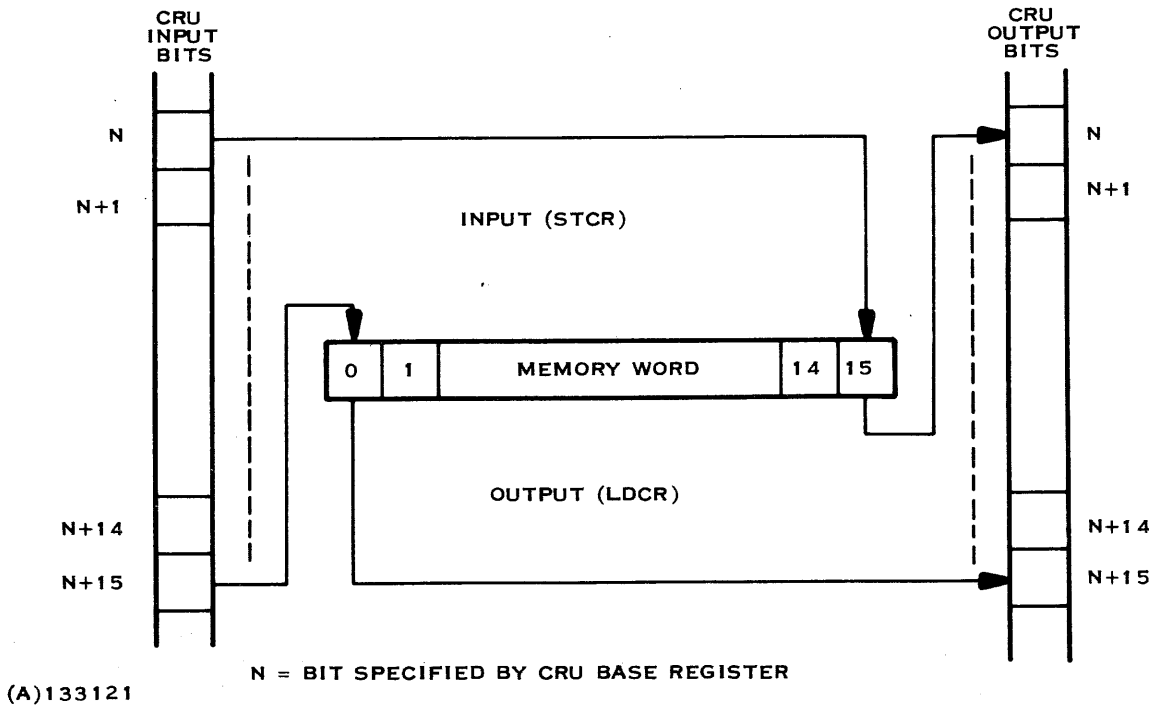


Figure 1-8. TMS 9900 LDCR/STCR Data Transfer

right-justified field within the whole memory word. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves the transfer of 8-bits or less, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

The TMS 9900 also contains a 16-bit parallel memory bus interface which is to access the ROM and RAM memories in the 990/4 system. The address bus portion of the memory interface (AB 0-14) is shared by the CRU interface. To distinguish between CRU addresses and memory addresses, the TMS 9900 generates a memory enable signal for each memory cycle.

Memory Bus Gating for External Controller. The 990/4 microcomputer board contains a number of tri-state drivers (and associated control logic) which permit external direct memory access (DMA) controllers to share the full 32K memory address space with the TMS 9900 microprocessor.

During normal operation, all memory transfers are controlled by the TMS 9900. However, an external controller may gain access to any of the 32K address space by generating an active HOLD signal. In response to this signal, the TMS 9900 sends back a HOLDA (hold acknowledge) signal which is used on the 990/4 board to gate the memory bus tri-state drivers to/from the microprocessor to the high impedance state. The hold acknowledge also informs the controller that it has access to memory. After completion of the direct memory access, the controller relinquishes memory to the microprocessor by deactivating the HOLD line to the TMS 9900. As a result, hold acknowledge goes away and the microprocessor's memory bus lines are activated once more.

4K Dynamic RAM. The "dash 2" configuration of the 990/4 microcomputer board is equipped with a 4K onboard dynamic RAM memory which is used for data and program storage. This memory is implemented with 16 TMS 4051 4096 X 1-bit RAM memory chips. In a standard system, this memory is assigned a starting address of 0000_{16} by a jumper between terminals E16 and E17 (see figure 1-9). Optionally, the starting address can also be set to 2000_{16} (4K boundary) by placing the jumper between E16 and E18. The onboard RAM memory occupies a contiguous block of 4K addresses beginning with the selected starting address.

The operation of the 4K RAM memory is as follows. Each time a Memory Enable signal is generated by either the TMS 9900 (or by an external controller), the addressing logic associated with the 4K RAM examines the memory address on the address lines. If the address is below or above the address assigned to the 4K RAM, the 4K RAM ignores the memory cycle. However, if the address falls within the RAM's address space, a 4K address OK is generated which permits a fetch or store cycle at the specified address.

A factory-installed parity option is also available with the 4K RAM which includes a 17th TMS 4051 RAM chip in the U74 slot (see figure 1-5) and two SN74180 parity generator/checker ICs which are installed in slots U43 and U81. This option results in a parity bit being generated and stored with each write data word. During subsequent read cycles at the same address, new parity bits are generated for the read data word and compared with the parity bit previously stored during the write cycle. If an error is detected, a memory error interrupt is generated which normally is wired to interrupt level 2 on the 990/4 board (jumper between terminals E13 and E14).

1K ROM/Static RAM. The 1K ROM/RAM memory section is normally used for loader ROMs, self-test ROMs and the programmer panel software ROMs plus any special-purpose programs whose high-usage merits placing the programs on custom ROMs. The ROMs used in this section are SN74S287 256 X 1-bit programmable ROMs. This section may also be converted to RAM storage (in 256 word blocks) using TMS 4043 256 by 4-bit RAM chips.

Functionally, the 1K ROM/RAM section consists of 4, 256-word banks (bank 0 through bank 3). Each bank consists of 4 ROM or 4 RAM chips (a given bank must contain all ROM or all RAM chips) placed in a vertical column as shown in figure 1-9. Bank 0 is the left-most column (U37, U53, U59 and U76) and bank 3 is the right-most column. Jumper wires must be installed across the two terminals which correspond to a memory bank equipped with ROM memory. No jumpers are required for banks containing RAM memory.

In the standard "dash 1" configuration of the 990/4 microcomputer board, bank 3 comes factory equipped with TMS 4043 static RAM chips (figure 1-10) and the jumper between terminals E1 and E2 is clipped. The remaining three banks may contain any combination of ROM or RAM memory as long as all four chips in a given bank are the same type. Similarly, jumper wires must be installed for each bank containing ROM memory as shown in figure 1-9.

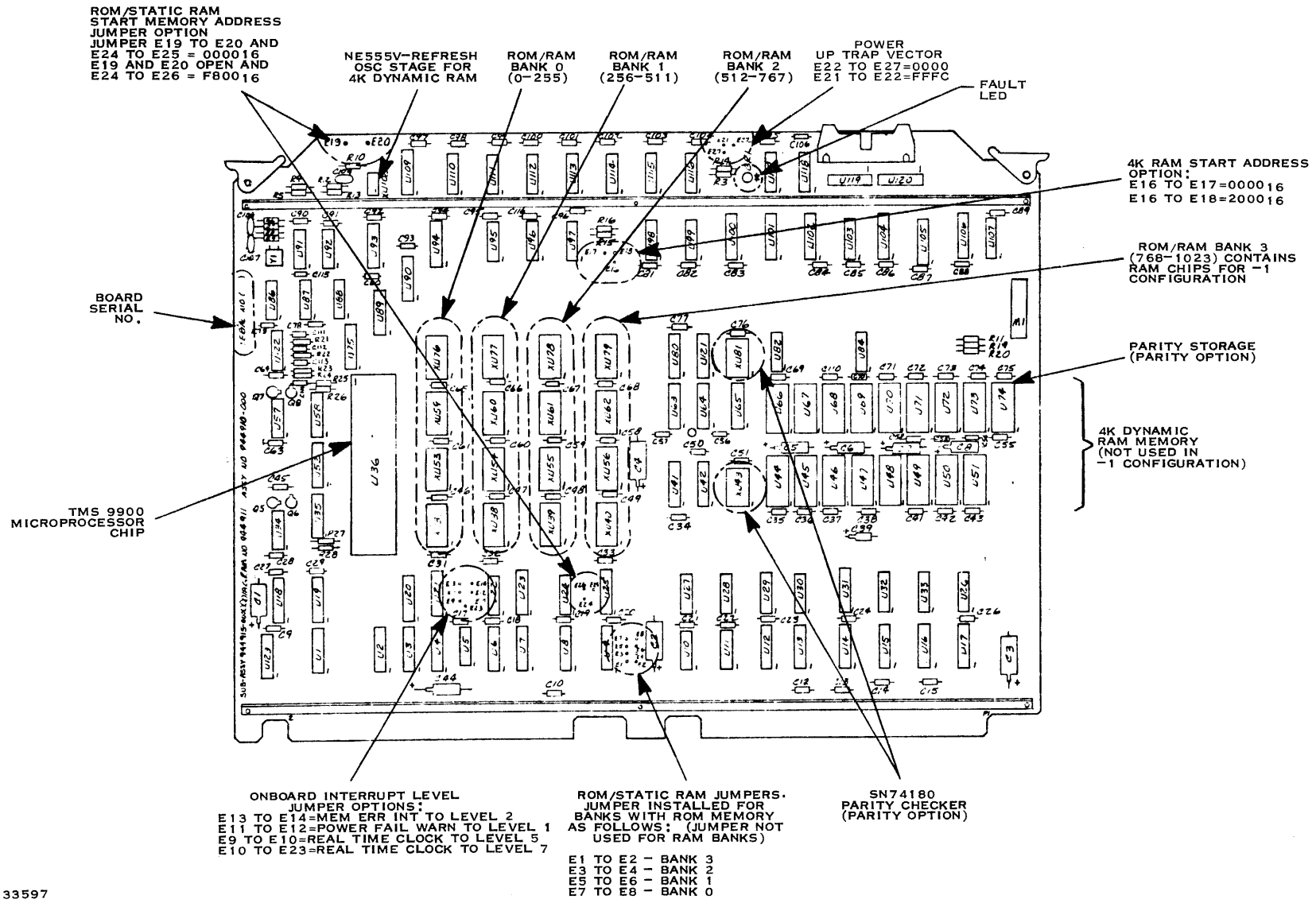
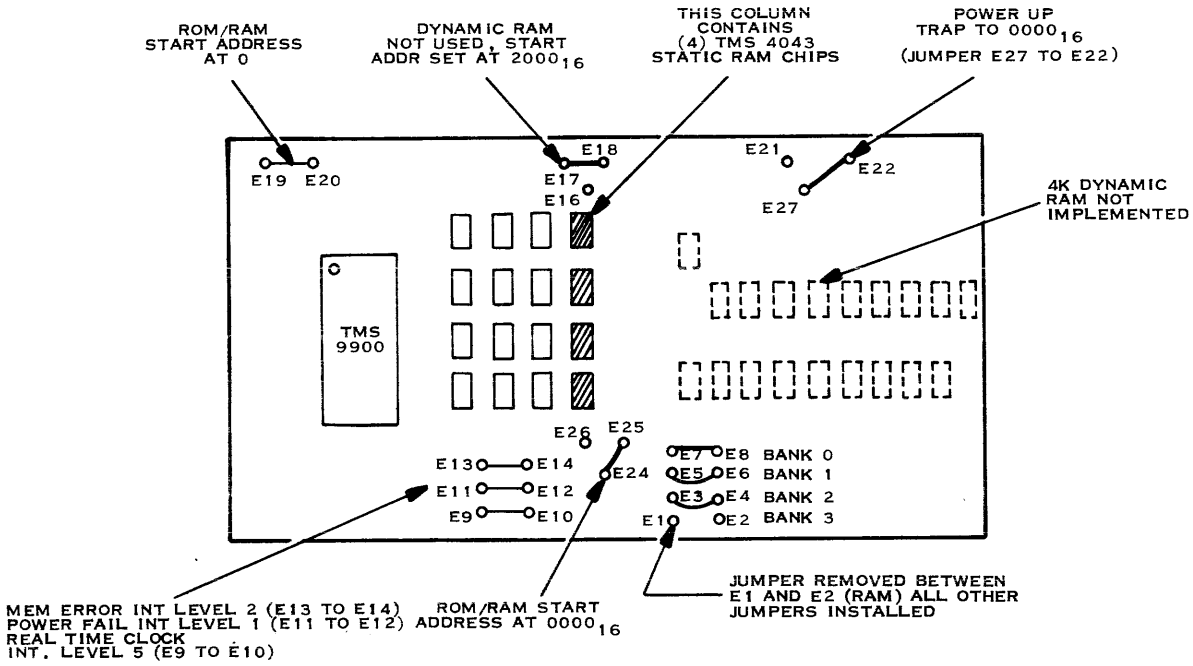
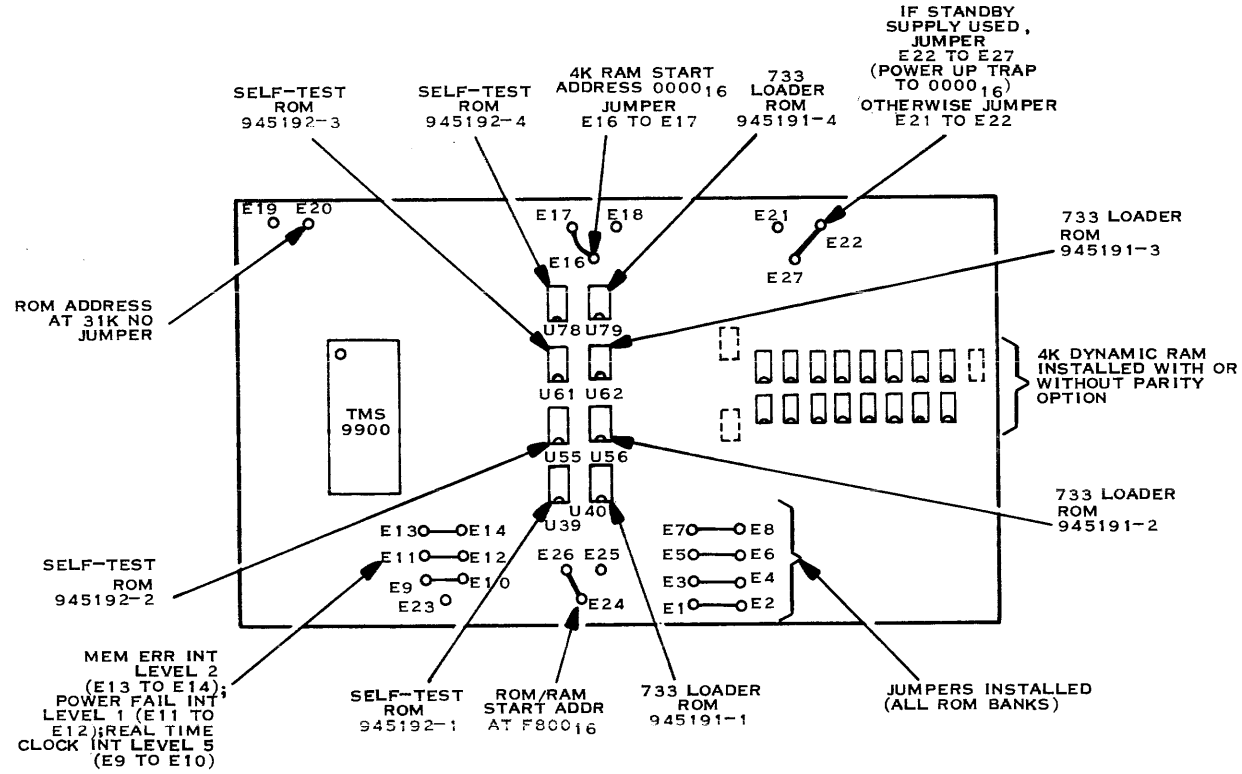


Figure 1-9. 990/4 Microcomputer Board Options



(A) MACHINE CONTROLLER CONFIGURATION (944910-1)



(B) GENERAL PURPOSE COMPUTER CONFIGURATION (944910-2)

(B)133342

Figure 1-10. 990/4 Microcomputer Board Standard Configurations

In the standard "dash 2" configuration, a set of 8 special purpose ROMs are installed in banks 2 and 3 as shown in figure 1-10. These ROMs contain the 733 ROM loader, programmer panel software and the self-test routine. Other optional ROM sets are also identified in figure 1-11. In addition to these special-purpose ROMs, the user may also install custom ROMs which may be identified by the absence of part numbers or part numbers different from those listed in figure 1-11.

CAUTION

When replacing a 990/4 microcomputer board in a system, these custom ROMs must always be transferred to the replacement board in the exact same locations.

Load Control Logic. The load control logic on the 990/4 microcomputer board generates a LOAD signal which causes the TMS 9900 to trap to memory location FFFC under the following conditions:

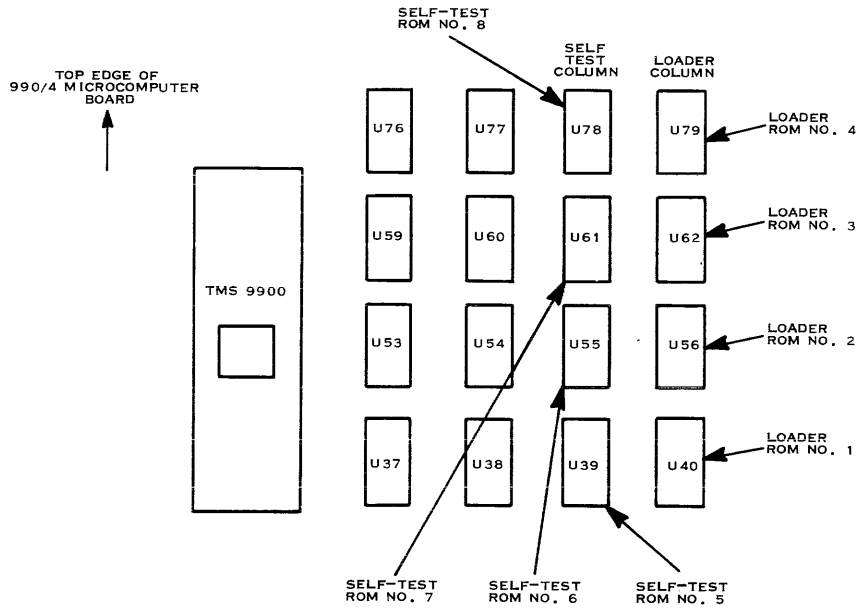
- When power is initially applied to the chassis (if the jumper is installed between terminals E21 and E22). If the jumper is installed between terminals E22 to E27, the LOAD signal is inhibited and the microprocessor traps to memory location 0000 when the power reset (TLPRES–) occurs.

- When the programmer panel is in the RUN mode (RUN LED lit), the key switch is in the UNLOCK position and the HALT/SIE switch is pressed on the panel. This results in a RESTART signal being generated by the panel which causes the load control logic on the 990/4 board to generate a load signal. The same signal is generated by the operator panel when the key switch is set to the LOAD position.

- When the panel is in the HALT mode and the HALT/SIE switch is pressed on the programmer panel, the panel software utility executes an SBO instruction which is decoded on the 990/4 board to generate an SIECLK– (single instruction clock). After one user instruction is executed, the load control logic generates a LOAD signal resulting in another trap to memory location FFFC.

- When an LREX external instruction is decoded. This instruction permits software to initiate a load when location FFFC contains the loader program vector.

In the standard configuration, memory location FFFC contains the workspace pointer (WP) value for the panel software and the next memory location (FFFE) contains the associated program counter (PC) value for the panel software. For systems not equipped with a programmer panel, locations FFFC and FFFE contain the WP and PC values for the loader ROM.



ROM KIT PART NO.	DESCRIPTION	ROM PART NO.'S U40	U56	U62	U79	U39	U55	U61	U78
945121-1	733 ASR/CARD READER ROM LOADER	945191-7	945191-8	945191-9	945191-10	–	–	–	–
945121-2	733 ASR/CARD READER LOADER WITH SELF TEST	945191-1	945191-2	945191-3	945191-4	945192-1	945192-2	945192-3	945192-4
945121-3	FLOPPY DISC LOADER	945190-7	945190-8	945190-9	945190-10	–	–	–	–
945121-4	FLOPPY DISC LOADER WITH SELF TEST	945190-1	945190-2	945190-3	945190-4	945192-1	945192-2	945192-3	945192-4
945121-5	733 ASR ROM LOADER WITH SELF TEST (PROTOTYPING)	945191-13	945191-14	945191-15	945191-16	945192-9	945192-10	945192-11	945192-12

(B)133598

Figure 1-11. 990/4 Microcomputer Board ROM Loader Options

External Instruction Decode. The TMS 9900 contains provisions for five external instructions which result in "NO OPS" internal to the chip. These instructions include:

- IDLE – Causes the programmer interface logic on the 990/4 board to send a signal to the programmer panel which lights the IDLE LED on the panel indicating microprocessor inactivity.
- RSET – Results in a system reset signal (IORES–) being sent out to all boards in the system and causes the FAULT LED on the programmer panel to be reset.
- CKON/CKOF – These two instructions are used to enable and reset the real time clock interrupt circuit.
- LREX – This instruction is decoded on the 990/4 board and sent to the load control logic to generate a LOAD signal.

Real Time Clock Logic. The real time clock logic receives a 120 Hz pulse train continuously from the main power supply board. Software makes use of these pulses to generate interrupts by executing a sequence of CKON and CKOF external instructions. A CKON instruction enables the real time clock logic and an interrupt is generated when the next clock pulse is received from the power supply. The interrupt is reset by a CKOF instruction. To enable another interrupt, the software must issue another CKON instruction and then reset that interrupt with a CKOF instruction.

As shown in figure 1-9, the real time clock interrupts may be connected to either interrupt level 5 or interrupt level 7 using terminals E9, E10, and E23. Interrupt level 5 is selected when the jumper is installed between E9 and E10 (standard jumper configuration) and interrupt level 7 is selected when the jumper is installed between E10 and E23. If no jumper is installed, the real time clock interrupts are disabled.

Programmer Panel Interface Logic. The programmer panel interface logic provides an interface between the TMS 9900 microprocessor and the programmer panel. This section generates a module select for the programmer panel whenever a CRU transfer is addressed to the panel and permits 990 software to light the FAULT, RUN and IDLE LEDs on the programmer panel. This logic also skews the memory address bits 11 to 14 to develop CRU address bits 12-15. These address bits are used in the programmer panel to select one of 16 possible input data sources during a serial transfer from the panel to the CPU or to specify a command type to the panel during a CPU to panel transfer (e.g., start debounce timer or enable switch scanner logic).

The programmer panel interface also fans out a store clock and the serial output data line (CRUBITOUT) to the panel and buffers the power on reset signal from the power supply to light the POWER LED when the reset signal goes away.

CRU Interface Logic. The CRU interface logic monitors addresses on the memory address lines during nonmemory transfers (memory enable not present) and decodes CRU addresses between 000_{16} and $17F_{16}$ to generate a low-active signal on one of 24 module select lines (each P1 slot receives one module select line and each P2 slot receives 2 module select lines as listed in table 1-2). For a 6-slot chassis, software ensures that the highest CRU base address for the main chassis is limited to $09F_{16}$ which results in 1 of 12 module select lines going low. In order for a given interface board to respond to a CRU address, its module select line must be active. All other boards ignore the CRU address. The CRU interface logic also fans out memory address lines 03-14 as CRU address lines 04-15.

Table 1-2. CRU Interface Signals

Signature	CRU Addr	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
MODSEL0-	000	P1-23	Slot 13, P2-48	Module select signals generated by the microprocessor from address bits 7-11 (CRUBITS 8-11) for use within the main or an expansion chassis. Note that P1 in each slot of the backpanel receives one module select signal whereas P2 receives two module select signals. This configuration permits P2 to use 32 bits of the CRU. Note that pin 48 of successive P2 connectors in the chassis slots are connected to even-numbered module select signals and at the CRU circuit board level carries a MODSELA– signature. Pin 46 of successive P2 connectors in the chassis slots are connected to pin 48 of P1 of that slot and then to an odd-numbered module select signal and carries a signature of MODSELB–. Pin P1-48 is not used when a full-sized CRU circuit board is implemented in a chassis slot. MODSEL signal lines will drive 10 TTL loads.
MODSEL1-	020	P1-35	Slot 13, P1-48 and P2-46	
MODSEL2-	040	P1-37	Slot 12, P2-48	
MODSEL3-	060	P1-43	Slot 12, P1-48 and P2-46	
MODSEL4-	080	P1-44	Slot 11, P2-48	
MODSEL5-	0A0	P1-45	Slot 11, P1-48 and P2-46	
MODSEL6-	0C0	P1-46	Slot 10, P2-48	
MODSEL7-	0E0	P1-47	Slot 10, P1-48 and P2-46	
MODSEL8-	100	P1-48	Slot 9, P2-48	
MODSEL9-	120	P1-49	Slot 9, P1-48 and P2-46	
MODSEL10-	140	P1-51	Slot 8, P2-48	
MODSEL11-	160	P1-53	Slot 8, P1-48 and P2-46	
MODSEL12-	180	P1-61	Slot 7, P2-48	
MODSEL13-	1A0	P1-67	Slot 7, P1-48 and P2-46	
MODSEL14-	1C0	P1-69	Slot 6, P2-48	
MODSEL15-	1E0	P1-76	Slot 6, P1-48 and P2-46	
MODSEL16-	200	P2-38	Slot 5, P2-48	
MODSEL17-	220	P2-36	Slot 5, P1-48 and P2-46	
MODSEL18-	240	P2-34	Slot 4, P2-48	
MODSEL19-	260	P2-32	Slot 4, P1-48 and P2-46	
MODSEL20-	280	P2-22	Slot 3, P2-48	
MODSEL21-	2A0	P2-18	Slot 3, P1-48 and P2-46	
MODSEL22-	2C0	P2-16	Slot 2, P2-48	
MODSEL23-	2E0	P2-13	Slot 2, P1-48 and P2-46	
CRUBIT4 (Chassis Select)		P1-56	P1-56	Address bit generated by the microprocessor to select a particular chassis (bits 4-6), a 16-bit module within that chassis (bits 7-11), and a particular bit from that module (bits 12-15). CRUBITS 4-11 are capable of driving at least 12 normalized TTL loads, CRUBITS 12-15 are capable of driving 30 normalized TTL loads.
CRUBIT5 (Chassis Select)		P1-54	P1-54	
CRUBIT6 (Chassis Select)		P1-52	P1-52	
CRUBIT7 (Module Select)		P1-50	P1-50	
CRUBIT8 (Module Select)		P1-62	P1-62	
CRUBIT9 (Module Select)		P1-64	P1-64	
CRUBIT10 (Module Select)		P1-68	P1-68	
CRUBIT11 (Module Select)		P1-70	P1-70	
CRUBIT12 (P/O Bit Select)		P1-36	P1-36, P2-36	
CURBIT13 (P/O Bit Select)		P1-32	P1-32, P2-32	

Table 1-2. CRU Interface Signals (Continued)

Signature	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
CRUBIT14 } P/O Bit Select	P1-38	P1-38, P2-38	
CRUBIT15 } P/O Bit Select	P1-34	P1-34, P2-34	
CRUBITOUT	P1-18	P1-18, P2-18	Serial data line for transfer of data from the microprocessor to the addressed CRU bit(s). This line is active only when STORECLK– goes low. (This line will drive 30 normalized TTL loads.)
CRUBITIN	P1-60	P1-60, P2-60	Serial data line for transfer of data from the addressed CRU bit(s) to the microprocessor. This line must be driven by an open collector gate and only when the module is selected. A 470-ohm pull-up resistor is mounted on the 990/4 circuit board for this line.
STORECLK-	P1-22	P1-22, P2-22	An active-when-low pulse that indicates to the selected CRU module that the operation is a write (Set Bit or LDCR) operation. This pulse transfers the data on the CRUBITOUT line into a holding flip-flop that is the CRU bit. (Will drive 30 TTL loads.)
TLIORES-	P1-14	P1-14, P2-14	I/O Reset: A normally high signal that, when low, resets all connected devices. This signal is a minimum 250 nanoseconds pulse that is generated by a RSET instruction in the microprocessor. This signal is also low until dc power is up and stable. (Will drive 30 TTL loads.)
TLPFWP-	P1-16	P1-16, P2-16	Power Failure Warning Pulse: A low signal of at least 7.0 milliseconds duration that indicates that a power failure is imminent. (Will drive 30 TTL loads.)
TLPRES-	P1-13	P1-13, P2-13	Power Reset: A normally high signal that goes low to reset connected devices at least 10 microseconds before dc voltages begin to fail during power down.

In addition, the CRU interface logic provides buffering for the CRU Store Clock, CRUBITOUT and CRUBITIN lines used to transfer serial data between an interface board (or write protect circuit on the 990/4 memory expansion board) and the microprocessor.

Interrupt Encoder Logic. The 990/4 microcomputer board contains a 7-bit interrupt register and an interrupt encoder circuit used for processing of onboard and external interrupts. These circuits provide for temporary storage of interrupts received from the half-board slots in the chassis (via the jumper plugs on the backpanel board) and from certain onboard interrupt conditions and generate a 4-bit interrupt code corresponding to the highest priority interrupt present. Interrupt level 1 is the highest priority interrupt external to the TMS 9900 (interrupt level 0 is assigned to the power on RESET signal). Level 7 is assigned the lowest priority level.

All on-board interrupt signals are connected to selected interrupt levels through jumper wires on the 990/4 board as shown in figure 1-9.

The onboard interrupt options include:

- Power failure warning – May be connected to interrupt level 1 via a jumper between E11 and E12.
- Memory error interrupt – May be connected to interrupt level 2 by means of jumper between E13 and E14.
- Real time clock interrupt – May connect to interrupt level 5 (jumper between E9 and E10) or interrupt level 7 (jumper between E10 and E23).

4-Phase Clock Generator. The 4-phase clocks, used to synchronize all TMS 9900 internal operations and all memory operations, are developed by a crystal-controlled oscillator on the 990/4 microcomputer board. Each of the 4-phase clocks (which are designated I1 through I4) are approximately 60 nanoseconds wide and have a cycle time of 333 nanoseconds.

Clock and Reset Fanout. The 990/4 board contains provisions for fanning out the "bar" phase 1 and "bar" phase 3 clocks (CLK1– and CLK3–) which are used to synchronize operations on all memory boards and DMA-type controllers. The power on reset (TLPRES–) from the power supply board is ORed with the reset generated by the execution of an RSET external instruction and fanned out to all boards in the system as IORES–. This signal initializes all control circuits and resets all interrupt flip-flops.

1.2.1.2 **990/4 Memory Expansion Board.** The 990/4 memory expansion board provides additional dynamic RAM memory space in 4K increments ranging from 4K to 20K (factory installed only). Other factory options include the parity option and the write protect option.

Parity Option. The parity option is a factory installed option that consists of a parity error LED on the top edge of the board, a 17th memory chip in each implemented memory bank (A16U1 through A16U4), parity generator/checker ICs (SN74180s), and a parity error flip-flop. When implemented, this section develops and stores a parity bit with each 16-bit data word. During a subsequent read cycle at the same memory location, the parity generator/checker circuits develop a new parity bit and compare this bit against the parity bit read from memory. In the event of a data error, the logic generates a memory error signal which is ORed with the memory error signal from the 990/4 microcomputer board's 4K RAM memory to develop the memory error interrupt. A parity error also lights the LED on the memory board. This LED may be manually cleared using switch bit 1 on U37 or by a system reset signal IORES– from the 990/4 microcomputer board.

Write Protect Option. The 990/4 memory expansion board may also be equipped with an optional (factory installed) write protect circuit which may be used to prevent write cycles into software specified memory areas. The protected area is defined by a 16-bit vector (protect mode bit and upper and lower bounds of the protected area) sent from the TMS 9900 to the write protect's bounds register via a load CRU instruction. The 16-bit vector is transferred to the memory board via a standard CRU interface. In the event that a write cycle is attempted in a protected memory location, the write cycle is inhibited, the protect violate (PV) flip-flop is set, and an interrupt is generated. Software may then read the contents of the PV flip-flop through a store CRU instruction or reset the flip-flop via an SBO CRU instruction.

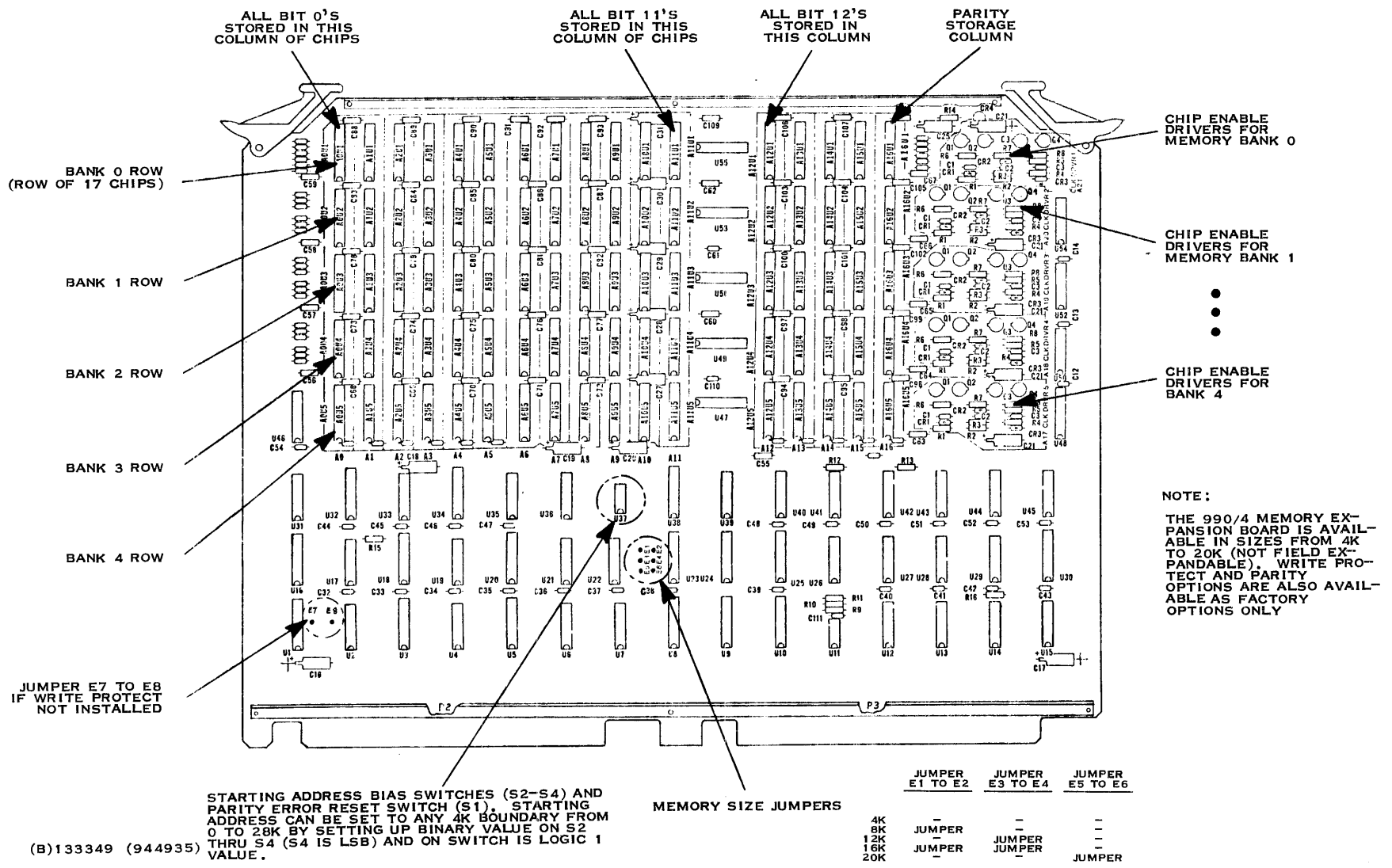
If the write protect option is *not* installed on the 990/4 memory expansion board, a jumper wire must be installed between terminals E7 and E8.

If a system is equipped with two memory expansion boards, only one of the boards may be equipped with write protect. However, the board with the write protect feature can detect attempted writes into protected areas on the second board and generate an interrupt although the write cycle will be permitted.

Memory Bank Organization. The memory section, implemented on the 990/4 memory expansion board, is organized into 4K banks as shown in figure 1-12. Bank 0 is the uppermost bank and bank 4 is the lowermost bank. Each 4K bank is implemented with 16 TMS 4050 4096 X 1-bit random access memory chips (plus an optional parity storage chip). All bit 0s are stored in the leftmost memory chip in each bank and all subsequent bit positions are arranged in numerical order from left to right. In addition, all similar bit positions (e.g., all bit 0s) in all banks are wire-ORed together. Therefore, a bit failure which shows up in one of the memory banks could actually be caused by a chip in the same bit position in one of the other banks.

Starting Address Option. The starting address of the memory expansion board may be set to any 4K boundary from 0 to 28K in the 990/4's 32K address space using the miniature switches S2 through S4 in the DIP switch package in U37 (see figure 1-12). These switches are set up in binary fashion with S2 being the MSB and S4 being the LSB. The starting address settings include:

Address Boundary (Decimal and Hex Byte Addresses)	S2	S3	S4
0 (0000_{16})	off	off	off
4K (2000_{16})	off	off	on
8K (4000_{16})	off	on	off
12K (6000_{16})	off	on	on
16K (8000_{16})	on	off	off
20K ($A000_{16}$)	on	off	on
24K ($C000_{16}$)	on	on	off
28K ($E000_{16}$)	on	on	on



	JUMPER E1 TO E2	JUMPER E3 TO E4	JUMPER E5 TO E6
4K	–	–	–
8K	JUMPER	–	–
12K	–	JUMPER	–
16K	JUMPER	JUMPER	–
20K	–	–	JUMPER

Figure 1-12. 990/4 Memory Expansion Board Options

Memory Size Jumper Options. The amount of memory implemented on the memory expansion board must be encoded using jumpers in terminals E1 through E6 as follows:

Memory Size	Required Jumpers
4K	none
8K	E1 to E2
12K	E3 to E4
16K	E1 to E2, E3 to E4
20K	E5 to E6

1.2.1.3 **EPROM Memory Module.** The EPROM memory module is an optional memory board with IC sockets and associated control circuitry to accommodate from 1K to 8K (field expandable) of eraseable programmable read-only-memory (EPROM). This memory is implemented with INTEL 2708 1024 X 4-bit EPROM ICs. Two memory chips are required for each 1K memory bank. As shown in figure 1-13, a maximum of 8 memory banks may be installed on the board with the leftmost column identified as bank 0 and the rightmost vertical column of two chips being bank 7.

The board jumper options are briefly described in the following subparagraphs.

Computer Type ID Jumper. The 990 EPROM memory module may be used in either a 990/4 or 990/10 computer. For use in a 990/4 chassis, a jumper wire must be installed between terminals E11 and E12 (E10 to E11 designates 990/10 chassis).

Starting Memory Address Bias. The starting address of the EPROM memory module may be placed at any 1K boundary in the 990/4's 32K address space between 0 and 31K as controlled by the five switch positions on DIP switch S2. Switch bit 1 is the MSB and switch bit 5 is the LSB. To select a starting address, the switches are set up in straight binary fashion with a switch in the "on" position designating a logic 1 and a switch in the "off" position designating a logic 0. For example, a starting address at 0 would be set up with all five switches in the off position; a starting address at 1K would have only switch 5 set to the on position and all others set to the off position; and a starting address of 31K would have all five switch bits set to the on position.

Memory Size Jumpers. A group of 9 terminals (E1 through E9) are used to encode the amount of memory implemented on the board (1K to 8K). These jumpers are set up as follows:

Memory Size	Jumper Connections
1K	E1-E2, E4-E5, E7-E8
2K	E1-E2, E4-E5, E8-E9
3K	E1-E2, E5-E6, E7-E8
4K	E1-E2, E5-E6, E8-E9
5K	E2-E3, E4-E5, E7-E8
6K	E2-E3, E4-E5, E8-E9
7K	E2-E3, E5-E6, E7-E8
8K	E2-E3, E5-E6, E8-E9

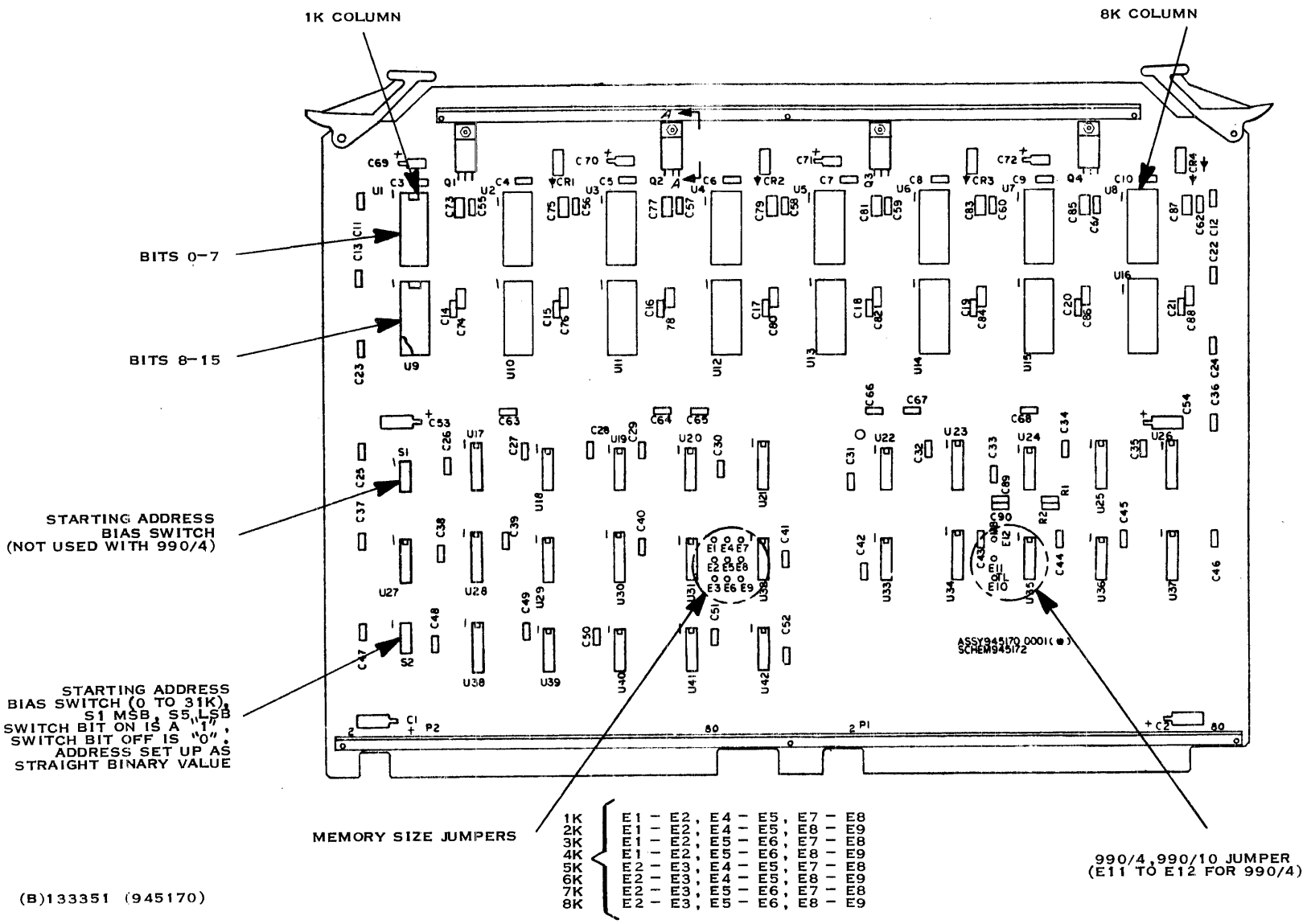


Figure 1-13. EPROM Memory Module Options

1.2.1.4 **990/4 Chassis.** The 990/4 microcomputer may be housed in one of three chassis types including:

- 3-Slot OEM chassis (requires external power supply and cooling)
- 6-Slot chassis – Contains built-in 20 amp power supply and optional standby supply for semiconductor memory protection during power failure conditions; also contains either programmer or operator panel for system control.
- 13-Slot chassis – Contains built-in 40 amp or 20 amp main power supply, optional standby power supply and either a programmer or operator panel. This chassis is basically the same as the 6-slot chassis except that it contains provisions for additional full-size logic boards.

6- and 13-Slot Chassis Interconnections. All internal connections (with exception of the ac distribution circuits) are accomplished through the connectors and the etch wiring on the backpanel board. Interconnections between each peripheral or data terminal and the computer is accomplished by an interface cable which connects to the top edge of its dedicated interface board (see figure 1-14) in the main computer chassis. In general, the 990/4 microcomputer board must be installed in slot 1 and various other peripheral interface boards in the standard configuration must be installed in accordance with the chassis map shown in figure 1-15. This standard configuration is required to assure software compatibility. However, some boards such as memory expansion, EPROM memory module and CRU expander may be installed in any slot (other than slot 1) since these devices respond to dedicated CRU addresses (see figure 1-26). Those logic board slots which are marked "spare" may be used to house any CRU interface

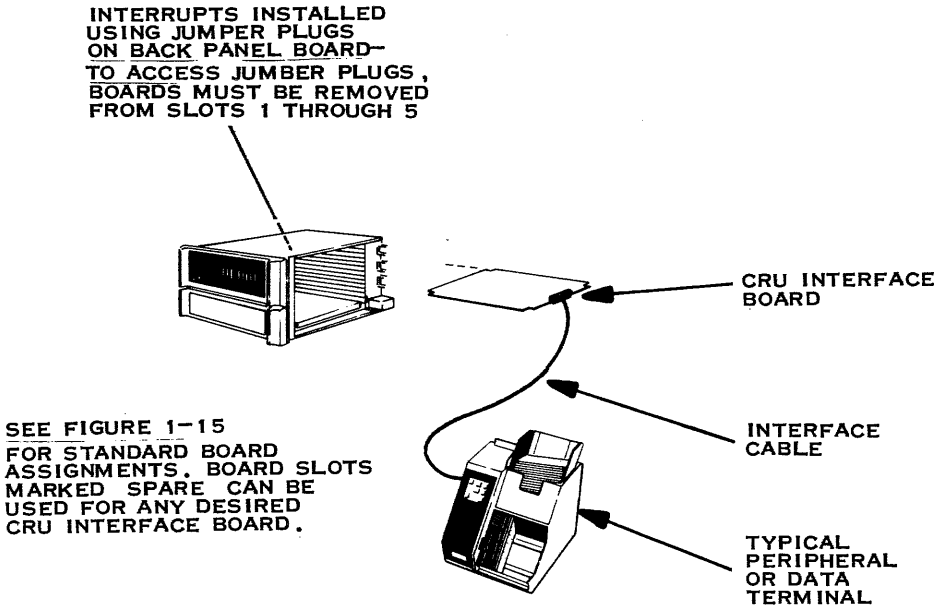


Figure 1-14. System Interconnections, Simplified Diagram

SLOT NUMBER	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 AU	N/A	N/A	990/4 AU	N/A
2	02E0	MEMORY EXPANSION OR SPARE		02C0	MEMORY EXPANSION OR SPARE	
3	02A0	MEMORY EXPANSION OR SPARE		0280	MEMORY EXPANSION OR SPARE	
4	0260	SPARE		0240	SPARE	
5	0220	SPARE		0200	SPARE	
6	01E0	SPARE		01C0	SPARE	
7	01A0	SPARE	(13)*	0180	SPARE	(13)*
8	0160	CRT 3	(9)*	0140	CRT 3	(9)*
9	0120	CRT 2 OR CRU EXPANDER	(10)*	0100	CRT 2 OR CRU EXPANDER	(10)*
10	00E0	CRT 1	(11)*	00C0	CRT 1	(11)*
11	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
12	0060	LINE PRINTER	(14)*	0040	CARD READER	4
13	0020	PROM PROGRAMMER	(15)* NOT USED	0000	733 ASR/KSR	6

*INTERRUPTS PREWIRED BUT NOT RECOGNIZED BY 990/4. MUST BE RECONFIGURED FOR USE WITH 990/4.

(A)133090

(B) 13-SLOT PREWIRED CHASSIS

SLOT NO.	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 AU	N/A	N/A	990/4 AU	N/A
2	0120	MEMORY EXPANSION OR SPARE	N/A	0100	MEMORY EXPANSION OR SPARE	N/A
3	00E0	913A VDT NO. 1	3	00C0	913A VDT NO. 1	3
4	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
5	0060	SPARE	N/A	0040	CARD READER	4
6	0020	PROM PROGRAMMER	NOT USED	0000	733 ASR/KSR	6

(A)133082

(A) 6-SLOT PREWIRED CHASSIS

Figure 1-15. Factory Prewired Chassis Configurations

board not otherwise identified on the chassis map. However, the software system must reflect the board locations.

NOTE

The map on top of the chassis should always indicate the latest hardware configuration to prevent inadvertently placing a replacement board in the wrong slot.

Interrupt Wiring. Interrupt wiring for the three chassis configurations is accomplished using jumper plugs in jacks 1A1J3 and 1A1J2 on the backpanel board. These jacks may be accessed by removing the logic boards from the first 5 slots.

NOTE

The standard 990 chassis is prewired to reflect the interrupt levels shown in figure 1-15. For use of the 13-slot chassis as a 990/4 main chassis, interrupt levels above 7 must be rewired since the 990/4 does not implement interrupt levels 8 through 15. Also, if chassis is used as expansion chassis, the interrupts must be reconfigured depending on expansion software and types of peripherals used.

The interrupt jumper plugs are molded plastic connectors with two rows square holes for inserting jumper wires. The jumper plug associated with each chassis contains several holes to accommodate jumper wires. Each hole has a plastic detent that holds the jumper wires in place when it is completely inserted into the hole. Figure 1-16 illustrates the mating of the jumper

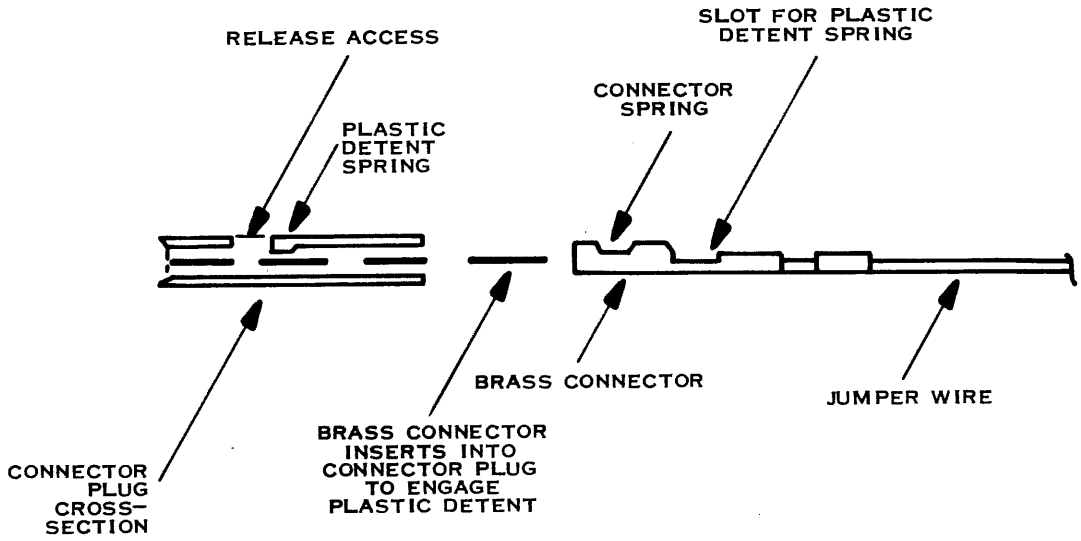


Figure 1-16. Interrupt Jumper Wire Installation

wire with the plastic jumper plug. Notice that the brass connector on the jumper wire must be oriented properly when inserted into the jumper plug so that the plastic detent can engage the slot in the top of the jumper wire brass connector. The jumper wire can be removed from the jumper plug by lifting up on the plastic detent to free the jumper wire brass connector to slide out the rear of the jumper plug. The spring force of the detent is slight enough that only a fingernail is required to lift it up to release the jumper wire.

Figure 1-17 illustrates the position assignments on the interrupt plugs for both the 6- and the 13-slot chassis. Notice that each interrupt generated by a module has two positions on the plug assigned to it. This configuration allows interrupts that will be recognized on the same level to be daisy-chain linked to each other. A typical daisy-chaining example is provided in figure 1-18.

OEM Chassis Connectors. The OEM chassis is a minimum configuration chassis that accommodates a 990/4 microcomputer board in slot 1 and two full-size logic boards (or a combination of full- and half-size boards) in slots 2 and 3. All electrical interconnections between the logic boards and the remainder of the system are accomplished through etch circuits on the chassis' backpanel board and interface cables on the top edge of the CRU interface boards in the chassis as shown in figure 1-14.

The OEM chassis also requires an external power supply, real time clock source, several control signal inputs and an external source of cooling air (approximately 300 cubic feet/minute). The control signal and dc power connections to the chassis are accomplished through the terminal strip on the rear of the chassis as shown in figure 1-19. The electrical connections include:

- Processor Restart – An external input used to cause the microprocessor to trap to memory location 0000_{16} or $FFFC_{16}$ depending on a jumper option on the 990/4 microcomputer board.

- Restart – An output from a circuit on the backpanel board in the chassis which causes the microprocessor on the 990/4 microcomputer board to initiate a level 0 interrupt and trap to location 0000_{16} when power is initially applied to the computer. This output is also available at the terminal strip for external use in the system.

- Power Fail Warning – A user-supplied power condition signal which is true a few milliseconds before a power failure occurs. This signal may be wired to interrupt level 1 through a jumper option on the 990/4 microcomputer board.

- 120 Hz Real Time Clock – A user-supplied real time clock source for the programmable real time clock interrupt logic on the 990/4 microcomputer board. This interrupt source may be wired into interrupt level 5 or 7 depending on a jumper option on the 990/4 microcomputer board.

- +5 Main and ±12 Main – User-supplied regulated dc voltages used in all logic circuits except some of the MOS memory circuits (990/4 microcomputer board and the 990/4 memory expansion board). If an optional standby power supply (with storage batteries) is not used, the +5 Main and the +12 Main voltages are jumpered to the +5 Mem and the +12 Mem inputs, respectively.

- ±5 Mem and +12 Mem – Regulated dc inputs from the user's standby power supply which are routed to the memory refresh circuits on boards containing MOS memory.

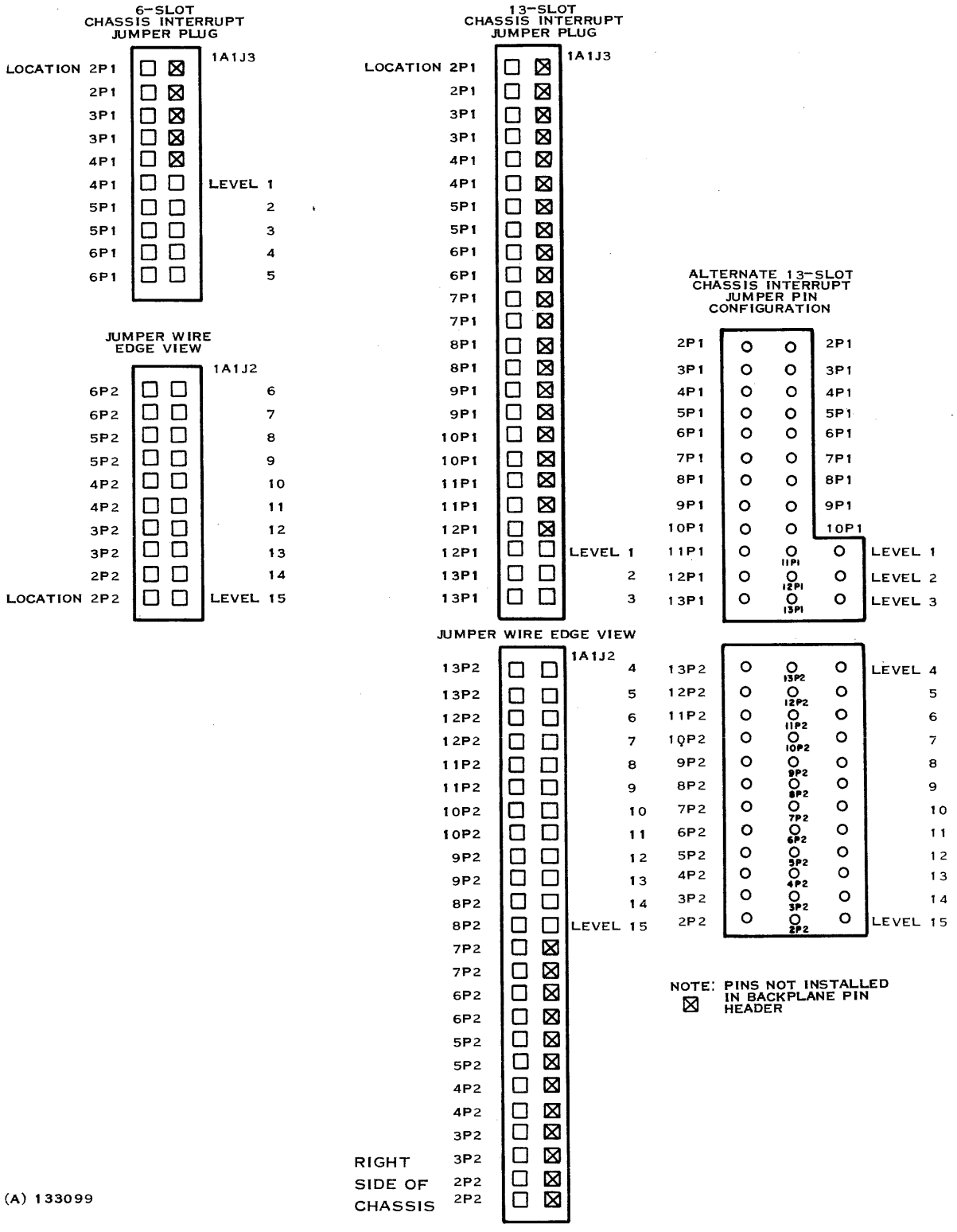


Figure 1-17. Chassis Interrupt Jumper Plugs

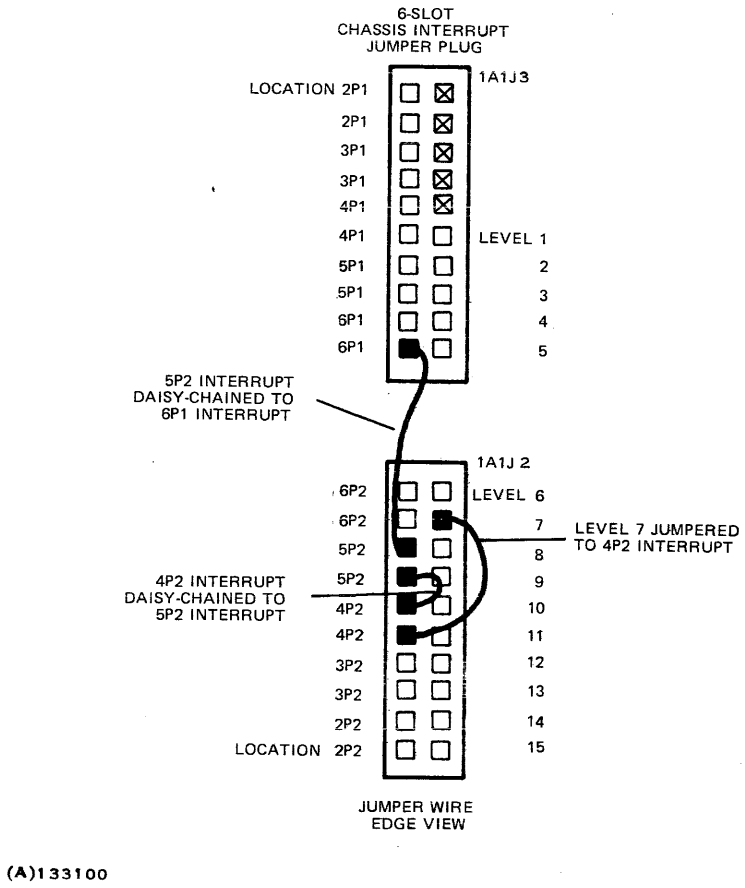


Figure 1-18. Jumper Plug Daisy Chain Sample Connection

1.2.1.5 **Programmer Panel.** The programmer panel provides for manual control of a system and permits data to be entered into selected registers in the TMS 9900 (PC, WP, and status registers) or any memory location in the 32K address space and displayed from selected TMS 9900 registers and memory locations. A key-controlled switch on the programmer panel controls the application of ac power to the chassis and prevents unauthorized program intervention (panel cannot be activated with the switch set to LOCK position and key removed).

When power is first applied to the chassis, the system comes up in the RUN mode and all programmer panel switches (except the HALT/SIE switch if the key switch is in the UNLOCK position) are locked out. The DATA LEDs are all forced to a logic 1 (all lit). If the microprocessor goes to the idle state, information may be displayed on the panel under software control.

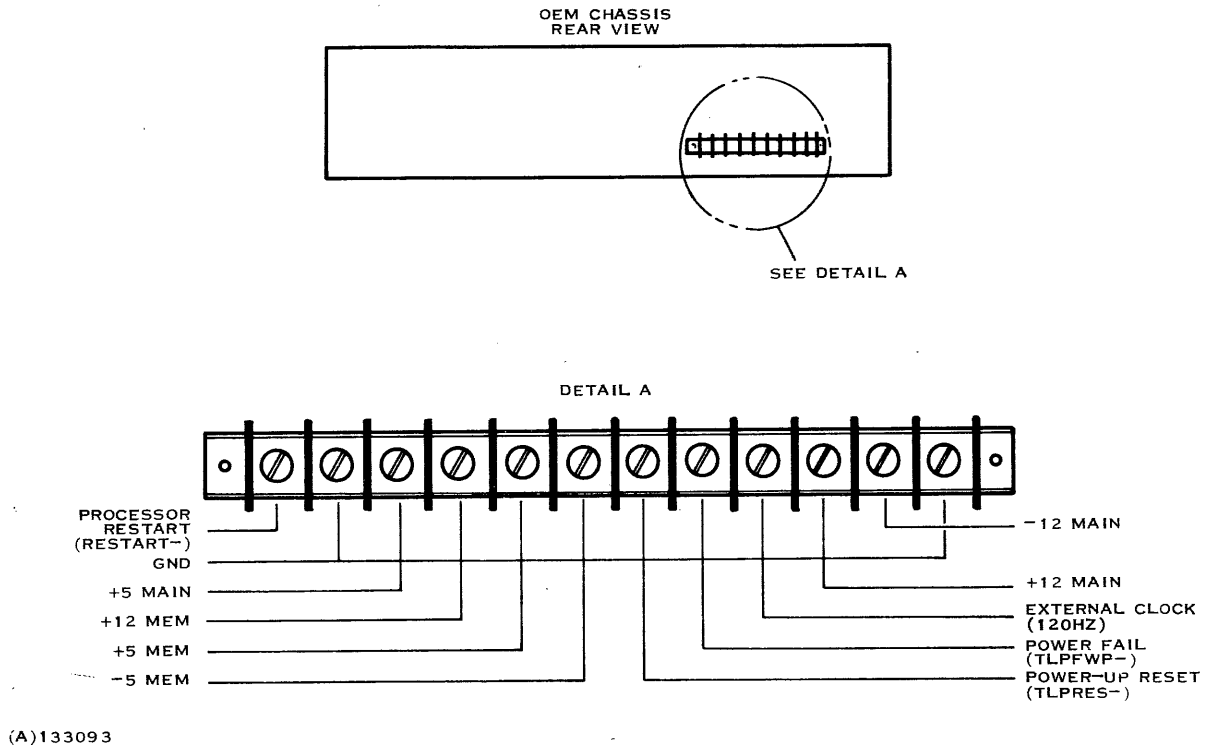


Figure 1-19. OEM Chassis External Connections

To activate the panel, the key switch must be set to the UNLOCK position and the HALT/SIE switch must be pressed. When these two events occur, a LOAD signal is sent to the TMS 9900 which causes the microprocessor to execute a trap to location $FFFC_{16}$ which contains the workspace register pointer value of 80_{16} for the front panel software. The last word in memory (FFFE) contains the program counter value which defines the starting memory address for the panel software. The processor then begins processing the panel utility and constantly monitors the switch outputs via CRU STORE instructions. If any DATA or control switch is pressed, the software activates a debounce timer and then determines when timeout has occurred (approximately 10 milliseconds) by a CRU STORE instruction. The software then reads the switch output and takes the appropriate action. In the case of a DATA switch being pressed, the panel software changes the state of the associated DATA LED (if previously unlit, the LED lights). In case of a control switch entry, the software executes the command.

NOTE

See Section II for a detailed description of the programmer panel controls and indicators.

1.2.1.6 **990 Power Supply**. Both the 6-slot and 13-slot 990 chassis are equipped with built-in power supplies and cooling fans. The 6-slot chassis contains a 20 amp main power supply and an optional standby power supply which protects the semiconductor memories against accidental loss of data due to temporary power failures.

The 13-slot chassis contains either a 20 amp main power supply or a 40 amp power supply and optional standby power supply.

Main Power Supply. The main power supply (both 20 and 40 amp versions) consists of the following:

- Ac distribution circuits
- Ac power converter board
- Main power supply board

A schematic diagram of the 990 power supply system is shown in figure 1-20 and the associated parts location diagram is shown in figure 1-21.

The ac distribution circuits route ac power through a 10-amp fuse 1F1 located at the rear of the chassis, through the key switch on the front panel, and back through a line filter 1FL1 and an optional line transformer (used only in 100, 200 and 230 Vac systems) to a distribution terminal strip 1TB1 all located in the rear of the chassis. Ac power on the terminal strip is tied directly to the blower fans and to the input side of the ac power converter board. Protection against a high surge voltage (230V) on the ac line is provided by 1C2 which temporarily shorts out and blows the fuse if lightning strikes the power lines. When the surge is gone, 1C2 ceases conduction but the fuse 1F1 must be replaced before normal operation can be restored.

The ac power converter board performs two functions in the main supply:

- Develops an unregulated +160 Vdc used to drive the regulators on the main power supply board (both 20 and 40 amp configurations) and the regulators and battery charger circuits on optional standby power supply board.
- Develops a 120 Hz pulse train which is further shaped on the main power supply board and routed to the 990/4 microcomputer board to drive the real time clock interrupt circuit.

The main power supply board (1A3) converts the unregulated +160 Vdc from the ac power converter board into the following regulated dc output voltages: +5 Vdc, +12 Vdc and -12 Vdc. If a standby supply is used, the regulated ±5 and ±12 Vdc outputs from the standby power supply board are routed through P3 on the main power supply board to P1 which connects to the backpanel board. If the standby supply option is not used, a jumper plug is installed on 1A3J3 which routes the main dc voltages developed on the main power supply board onto the memory dc lines at 1A3P1.

The main power supply board also generates a power on reset signal (TLPRES–) when ac power is initially applied to the chassis and generates a power failure warning (TLPFWP–) approximately 8 milliseconds before a power failure occurs. The power failure warning is normally tied into interrupt level 1 on the 990/4 microcomputer board.

The main power supply also provides a pulse shaping and driver function for the 120 Hz real time clock pulse train which originates on the ac power converter board. This pulse train is used to drive the real time clock interrupt logic on the 990/4 microcomputer board.

Standby Power Supply. The standby power supply is an optional power system used to provide the regulated dc voltages used by the semiconductor memories in the 990/4 system. The supply consists of a pair of storage batteries, a battery switch, and protective fuse in the rear of the chassis and a standby power supply board which mounts piggy-back on a set of standoffs on top of the main power supply board.

During normal operation, the standby power supply board converts the +160 Vdc (unregulated) output from the ac power converter board into a regulated +5 Vdc and ±12 Vdc. (The -5 MEM regulated voltage is developed on the main power supply board using the -12 Vdc output from the standby power supply.) This continuously supplies the memory voltages for the first seven slots. The standby power supply board also supplies charging current to the two 6-volt standby batteries which are wired in series to provide a 12-volt output.

In the event of a power failure, the standby power supply board generates an under voltage signal (UV–) which is used by the main power supply to generate a reset (TLPRES–) and then switches over to battery operation. When the batteries discharge to a minimum functional voltage level, the standby power supply shuts down to protect the batteries. When normal ac power is restored, the standby power supply board develops an equalizing voltage used to provide initial charging current for the batteries until the charge current drops to a trickle charge level. The supply then switches to a float voltage to maintain the batteries at full charge. The standby power supply also contains provisions for preventing a switchover to battery operation (even if the battery switch is in the on position) unless ac power has first been applied to the system. This safety feature prevents inadvertent discharging of the batteries. The standby supply is also equipped with over-voltage sensing circuits which disable the standby supply and blows the battery fuse if any of the memory voltages exceed safe levels.

1.2.1.7 **CRU Interface Boards.** Each terminal or peripheral in the 990/4 system requires a separate CRU interface board which plugs into one of the board slots in the main chassis or expansion chassis. These boards may be implemented as either half- or full-size boards. Basically, each interface board provides the address decoding, data buffering and data packing and unpacking functions required to match up the serial CRU interface presented by the 990/4 microcomputer board with the bit-, byte- or word-oriented interface presented by the peripherals and terminals.

Each CRU interface board decodes the address on the CRU address lines when it receives a low-active Module Select signal from the board installed in slot 1 of the chassis (990/4 microcomputer board in main chassis or CRU buffer board in expansion chassis). If a store clock is present when a valid CRU address is on the CRU address lines (and the module select is present), the interface board accepts serial data from the CRUBITOUT line from the microprocessor. If the clock is not present, a CRU read operation is being performed and serial data from the CRU interface board is sent to the microprocessor via the CRUBITIN line. All bit selection for CRU board-to-microprocessor transfers is controlled by 990 software which addresses 1 of 16 bits via the 4 LSBs of the CRU address (bits 12-15). The TTY/EIA terminal interface module, which is used with the 733 ASR data terminal, is described in the following paragraphs. For a detailed description of the various other interface boards available for 990/4 system use, refer to the depot manual for the associated device (e.g., 16 I/O Data Module, Floppy Disc, Synchronous Modem, etc.).

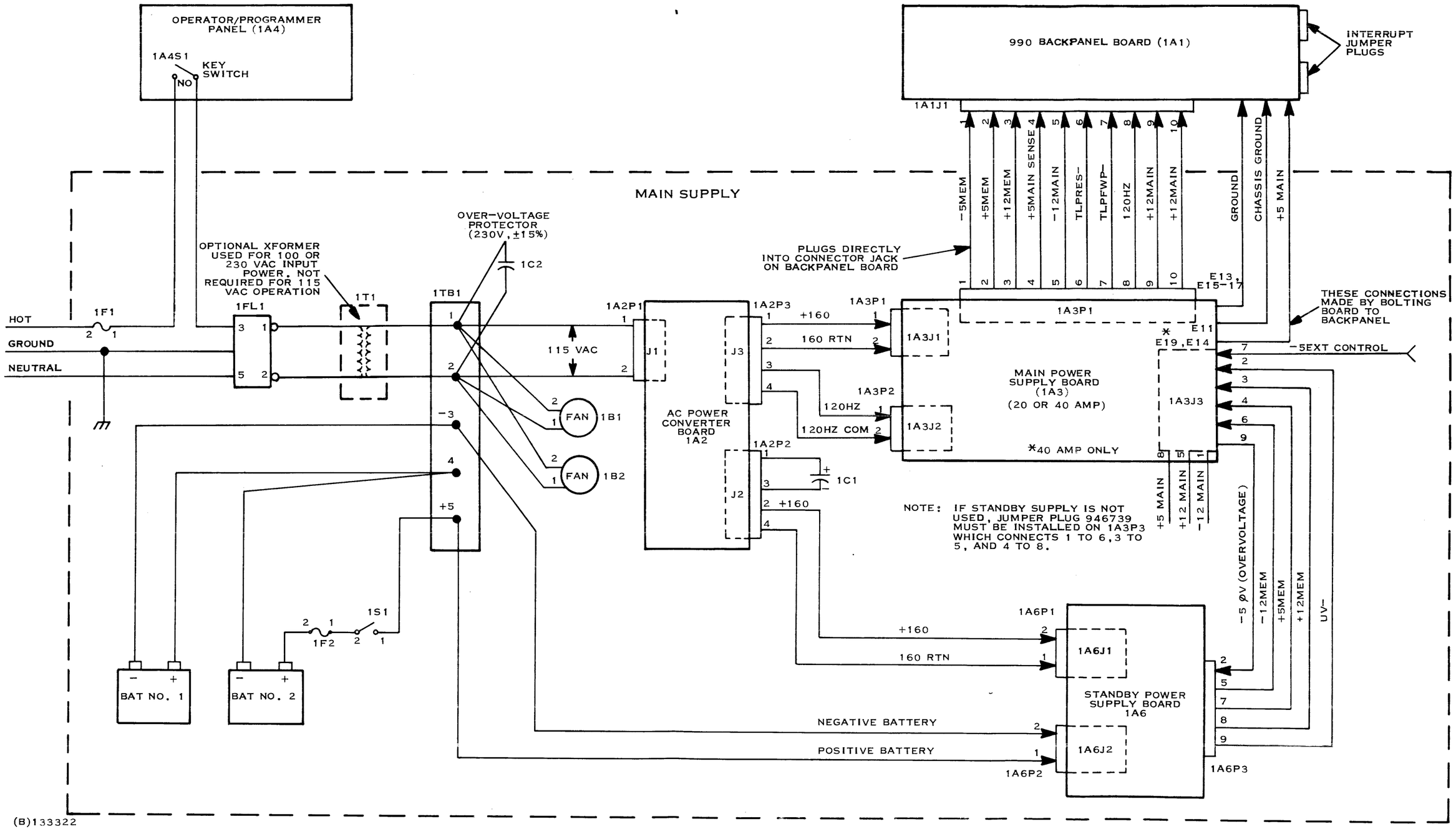
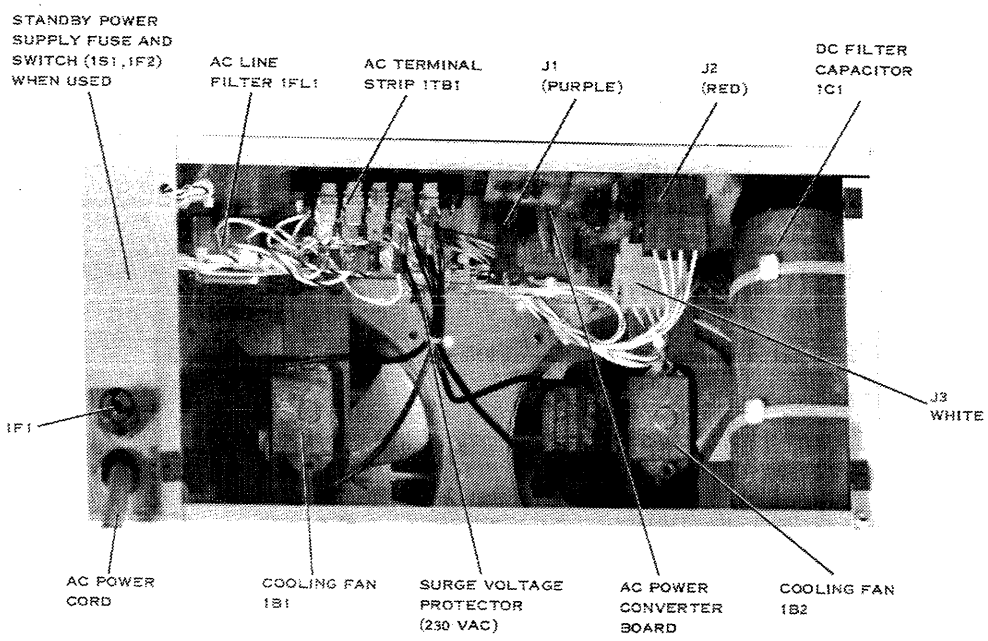
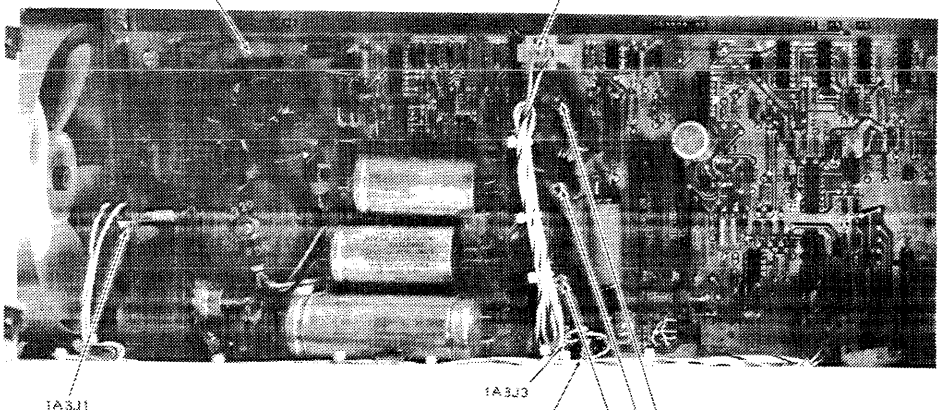


Figure 1-20. 990 Power System Schematic Diagram (6- and 13-slot chassis)



133323 (990-576-14-1)

AC DISTRIBUTION CIRCUITS (REAR OF COMPUTER)



133601 (990-576-74-2)

POWER SUPPLY BOARDS

Figure 1-21. Power Supply Assemblies and Subassemblies

TTY/EIA Terminal Interface Module. The TTY/EIA terminal interface module (Part Number 945075-1) provides an interface between the 990/4 and any terminal device using an EIA standard RS232 interface or 20 milliampere TTY current loop. Some of the 990 peripherals and data terminals which use the TTY/EIA terminal interface module include:

- 733 ASR data terminal
- 745 KSR data terminal
- 733 KSR data terminal
- Model 306 line printer
- Model 588 line printer

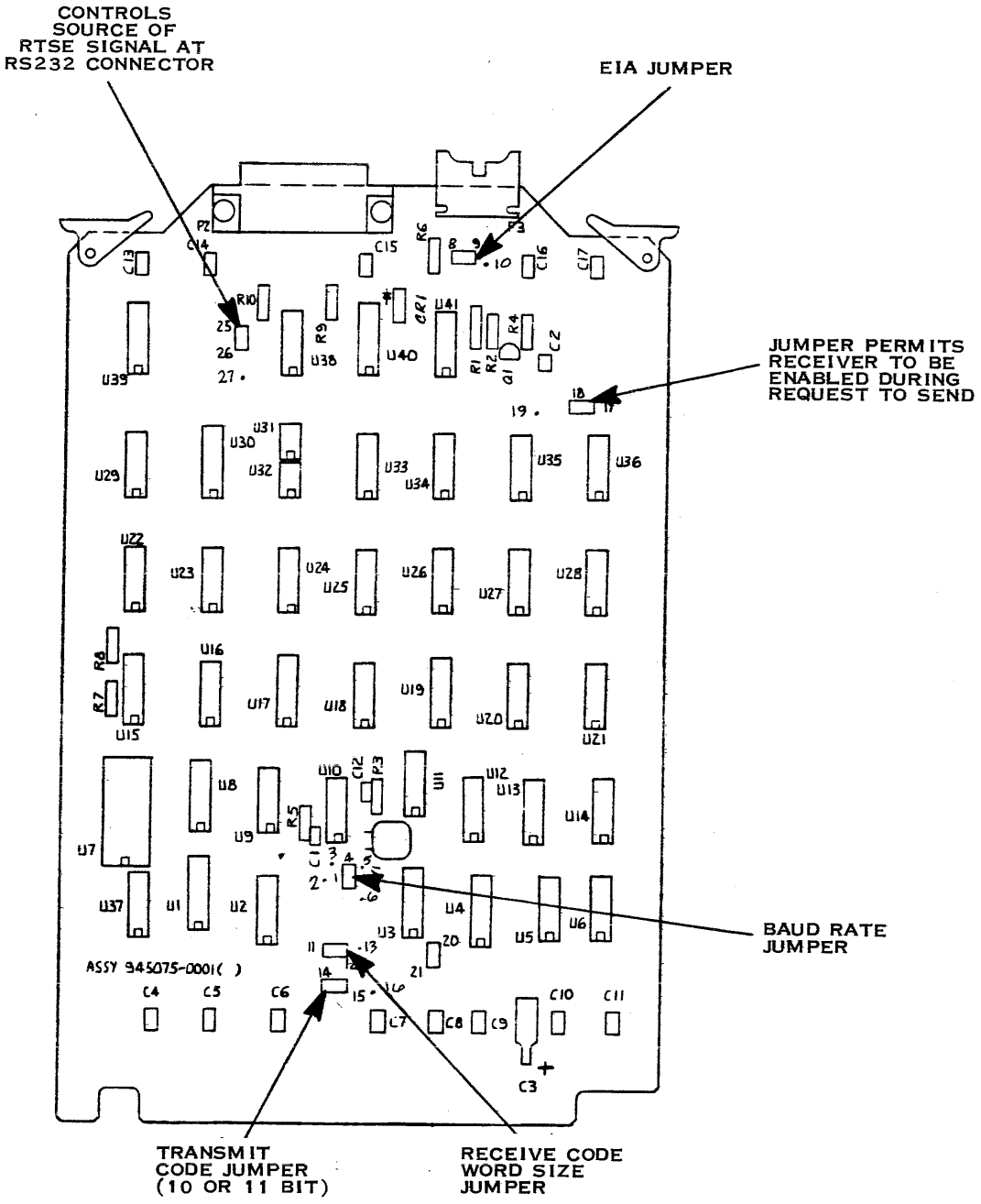
The jumper options used to modify the board operation for use with each device type are summarized in figure 1-22.

1.2.1.8 **CRU Expansion Board.** The CRU expansion board primarily expands the CRU interface in the main chassis to drive up to seven additional 990 expansion chassis. The board monitors for interrupts from the seven chassis using two independent interrupt recognition sections (A and B). If an interrupt occurs in chassis 1 through 4, the expansion board generates an INTA– (interrupt A). If the interrupt occurs in chassis 5 through 7, the expander board generates an interrupt B. The expander board then enables the interrupt ID lines from the highest priority chassis (chassis 1 highest priority, chassis 4 lowest priority in interrupt section A). The 990 software may then determine the source of the interrupt by executing an STCR instruction at address $F80_{16}$ (interrupt vector for section A) or $F90_{16}$ (interrupt vector for section B). As a result of the instruction, the CRU expander board serially transfers a 16-bit vector in the format shown in figure 1-23. As indicated in this figure, the interrupt vector identifies the chassis and the unit within the chassis which issued the interrupt. The vector also indicates the on-line status of each expansion chassis which reports to this interrupt monitoring section (chassis 1-4 for section A; chassis 5-7 for section B).

The CRU expansion board also contains provisions for fanning-in a direct interrupt (IREQ–) from each of the seven chassis and issuing an INTC– to the 990/4 if a direct interrupt is received from any chassis. The direct interrupt scheme is used with peripherals requiring faster interrupt service than is available with the interrupt scanner method.

The interrupt on the originating board is cleared by the interrupt servicing software via a CRU instruction addressed to the board in the respective expansion chassis.

Interrupt Servicing Jumpers. The two interrupt servicing sections on the CRU expansion board are normally enabled by jumper wires between terminals E5 and E6 (section A) and between terminals E7 and E8 (section B). This option permits disabling the interrupt servicing logic on a CRU expander board when two CRU expander boards are installed in the main chassis (see figure 1-24).



SUMMARY OF JUMPER OPTIONS

TERMINAL DEVICE	BAUD RATE	JUMPER CONNECTIONS
733 KSR DATA TERMINAL	300	E1 TO E3, E8 TO E9, E11 TO E12, E14 TO E15, E17 TO E18, E20 TO E21, E25 TO E26
733 ASR DATA TERMINAL	1200	E1 TO E4 (ALL OTHERS SAME AS ABOVE)
588 OR 306 LINE PRINTER	4800	E1 TO E6, E26 TO E27 (ALL OTHERS SAME AS ABOVE)

(A)133602

Figure 1-22. TTY/EIA Module Options

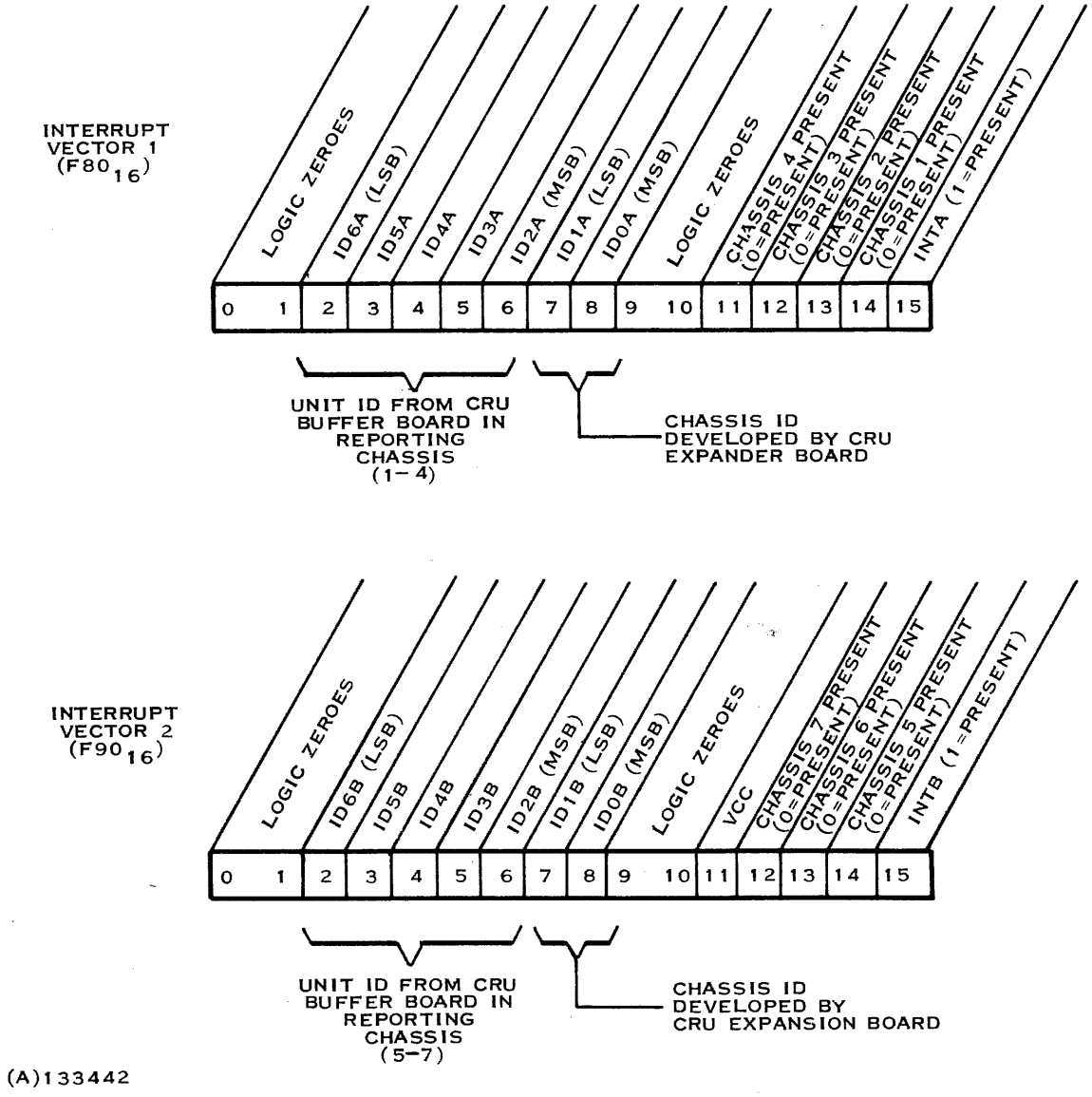


Figure 1-23. Expansion Interrupt Vector Format

Power On Reset Option. The CRU expander board also contains an option to accept either the power on reset from the power supply board (TLPRES–) via a jumper between terminals E1 and E2 or the reset signal from the 990/4 microcomputer board (TLIORES–) via a jumper between E3 and E4 (normal configuration). The IO reset signal from the 990/4 board permits a clear to be generated by either the power supply or by 990 software.

1.2.2 **990 I/O EXPANSION CHASSIS.** The 990 I/O expansion chassis is added to a system when the main chassis does not contain enough board slots to house all of the CRU interface boards required by the system. The chassis used for the I/O expansion chassis is identical to the main computer chassis except that it contains an operator panel instead of a programmer panel and slot 1 of the expansion chassis houses a CRU buffer board instead of a 990/4 microcomputer board. Also, the interrupt wiring for the expansion chassis is accomplished through jumper plugs on the backpanel board similar to the main chassis except that all 15 levels are implemented in the expansion chassis. The dc power supplies in the expansion chassis are identical to the power supply used in the main chassis except that a standby supply is not used with an expansion chassis.

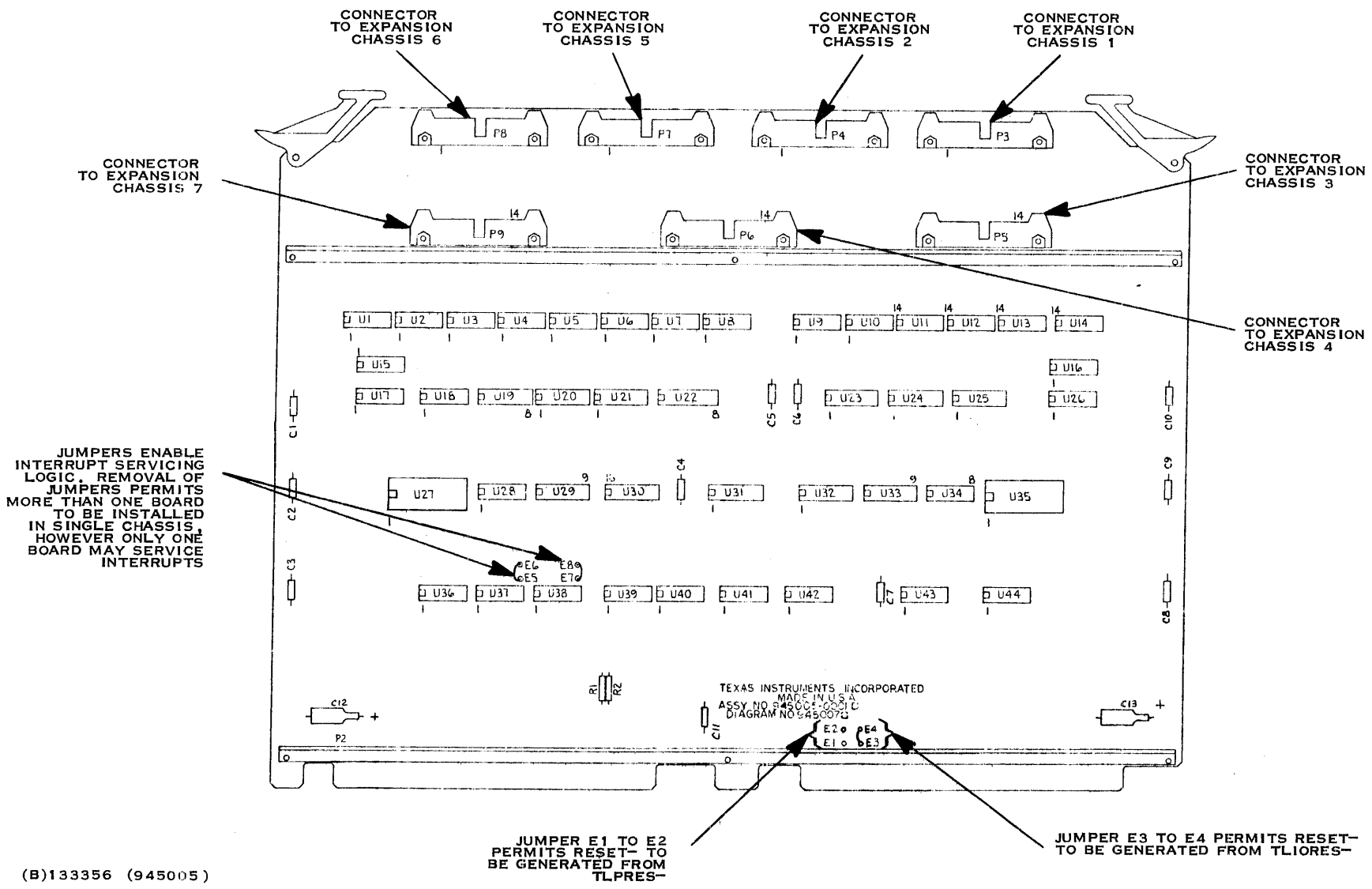


Figure 1-24. CRU Expansion Board Options

The operator panel on the expansion chassis contains a key switch which controls ac power to the chassis and a POWER LED which indicates when the power supplies are functioning properly. The interconnection between the operator panel and the CRU buffer board is accomplished through a 26-pin ribbon cable and connector which attaches to connector plug P5 on the top edge of the buffer board. The interface between the main chassis and the expansion chassis is accomplished through a 12-foot ribbon cable (Part Number 945001-1) which attaches to one of the 7 ports on the CRU expansion board in the main chassis (P3 through P9 depending on chassis number) and attaches to plug P3 on the top edge of the CRU buffer board in the expansion chassis.

1.2.2.1 **Expansion Chassis Interrupt Scheme.** A simplified block diagram of the interrupt system associated with a fully expanded 990/4 microcomputer system is shown in figure 1-25. As indicated in this figure, interrupts from each half-board slot in a given expansion chassis are wired to the interrupt jacks J2 and J3 on the backpanel board. These interrupt lines are then jumpered to selected interrupt levels 1 through 15 using wire jumpers on the backpanel board. The 15 interrupt levels are routed to an interrupt scanner on the CRU buffer board which is located in slot 1 of the expansion chassis. If an interrupt is received on any of the 15 interrupt levels, the CRU buffer board issues an "interrupt present" to the CRU expander board in the main chassis (see figure 1-26). The CRU expander board then responds to the interrupting chassis (having highest priority) with an ID enable signal. This enable is used to gate the four ID bits (which represent the binary value of the interrupt level) back to the CRU expander board. In response to an interrupt request from any of the seven chassis, the CRU expander board issues either an interrupt A (interrupt present in chassis 1-4), an interrupt B (interrupt present from chassis 5 through 7) or an interrupt C (direct interrupt present from interrupt chassis 1 through 7).

Interrupts A and B are used to activate the expander interrupt servicing routine which, in turn, addresses the appropriate interrupt servicing section (A or B) with a store CRU instruction addressed to either $F80_{16}$ (interrupt A) or $F90_{16}$ (interrupt B). As a result of the store CRU instruction, a 16-bit interrupt vector is sent back to the microprocessor. As shown in figure 1-23, the interrupt vector contains the ID of the originating unit (developed by the CRU buffer board in the interrupting chassis), the ID of the expansion chassis (developed in the CRU expander board) and the status of the expansion chassis associated with the reporting interrupt section (chassis 1-4 associated with interrupt section A and chassis 5-7 associated with section B). The interrupt vector is then used to select the proper device interrupt servicing routine associated with the interrupting board.

If a direct interrupt (INT C–) is generated, the interrupt is processed more speedily since the expansion interrupt servicing routine is bypassed and the microprocessor traps directly to the board-level interrupt servicing routine. This interrupt scheme is used when peripherals requiring rapid response to interrupts are located in the expansion system.

1.2.2.2 **CRU Expansion Address Scheme.** A CRU address map for the standard fully expanded 990/4 system is shown in figure 1-27. As indicated in this figure, each chassis is assigned a band of location-dependent CRU addresses which are used to address the CRU interface boards implemented within a given chassis. The chassis number (1 to 7) which is assigned to each chassis is determined by an ID plug on the CRU buffer board.

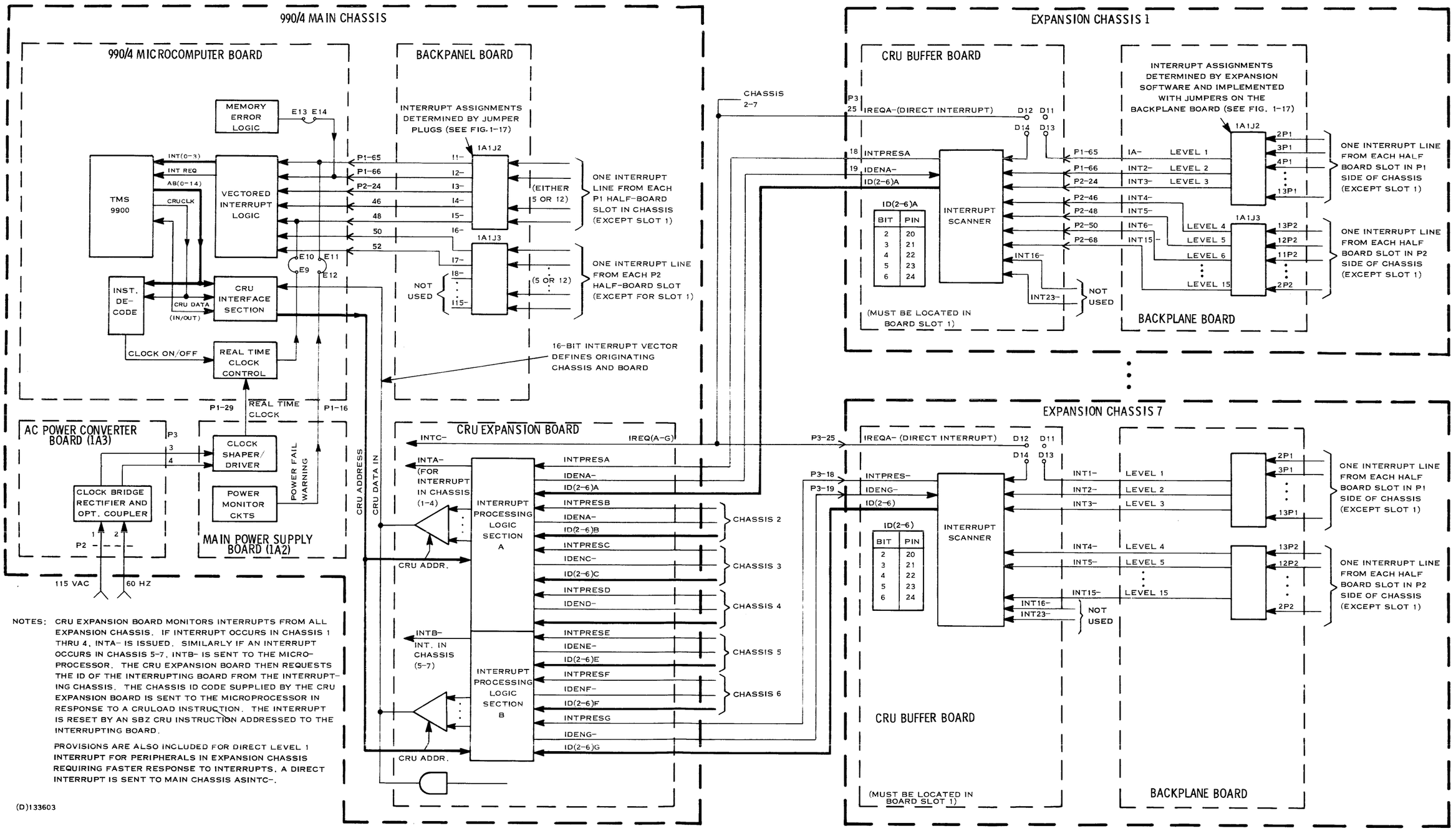


Figure 1-25. 990 Interrupt Paths, Simplified Diagram

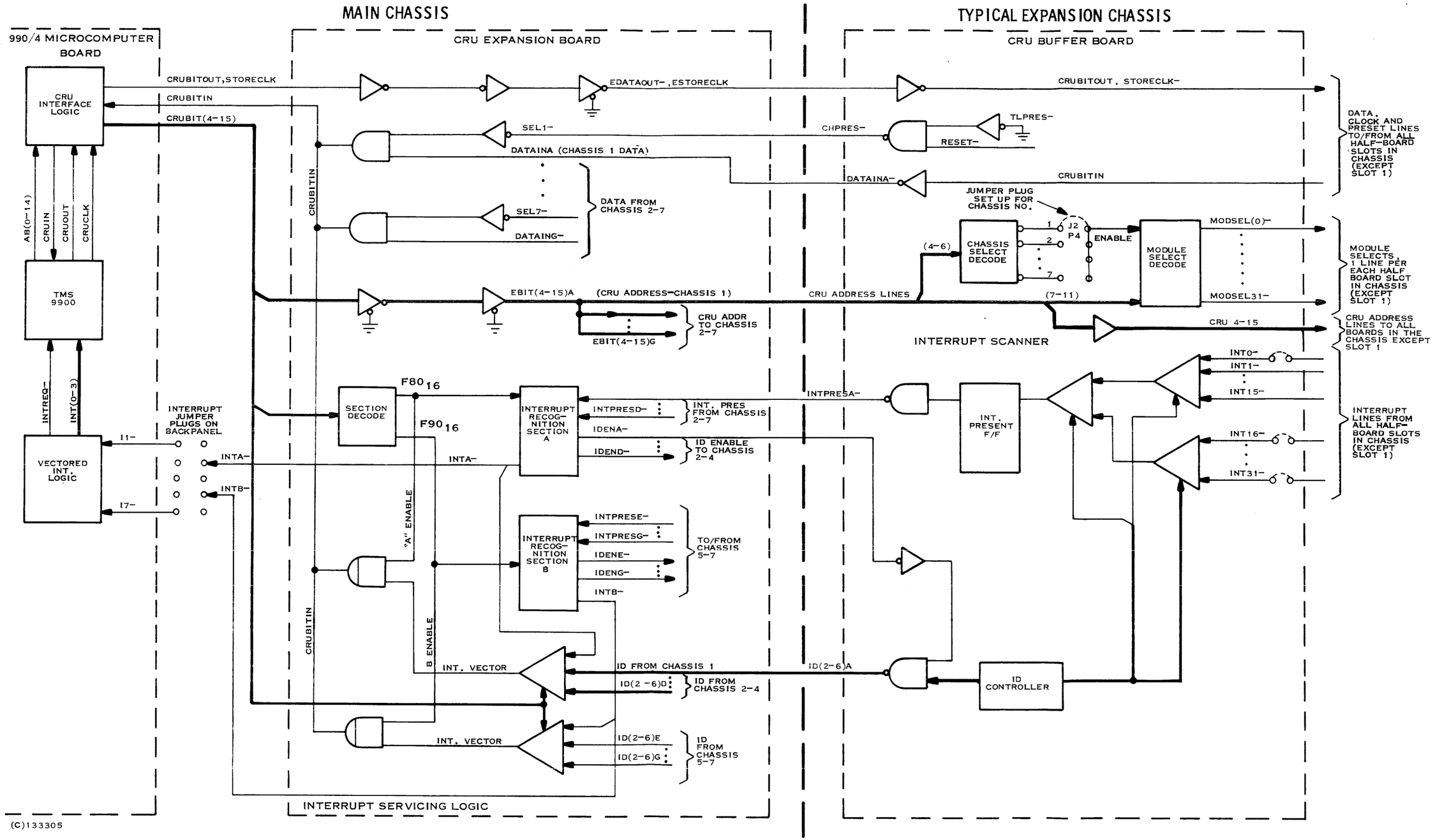


Figure 1-26. CRU Expansion, Simplified Block Diagram

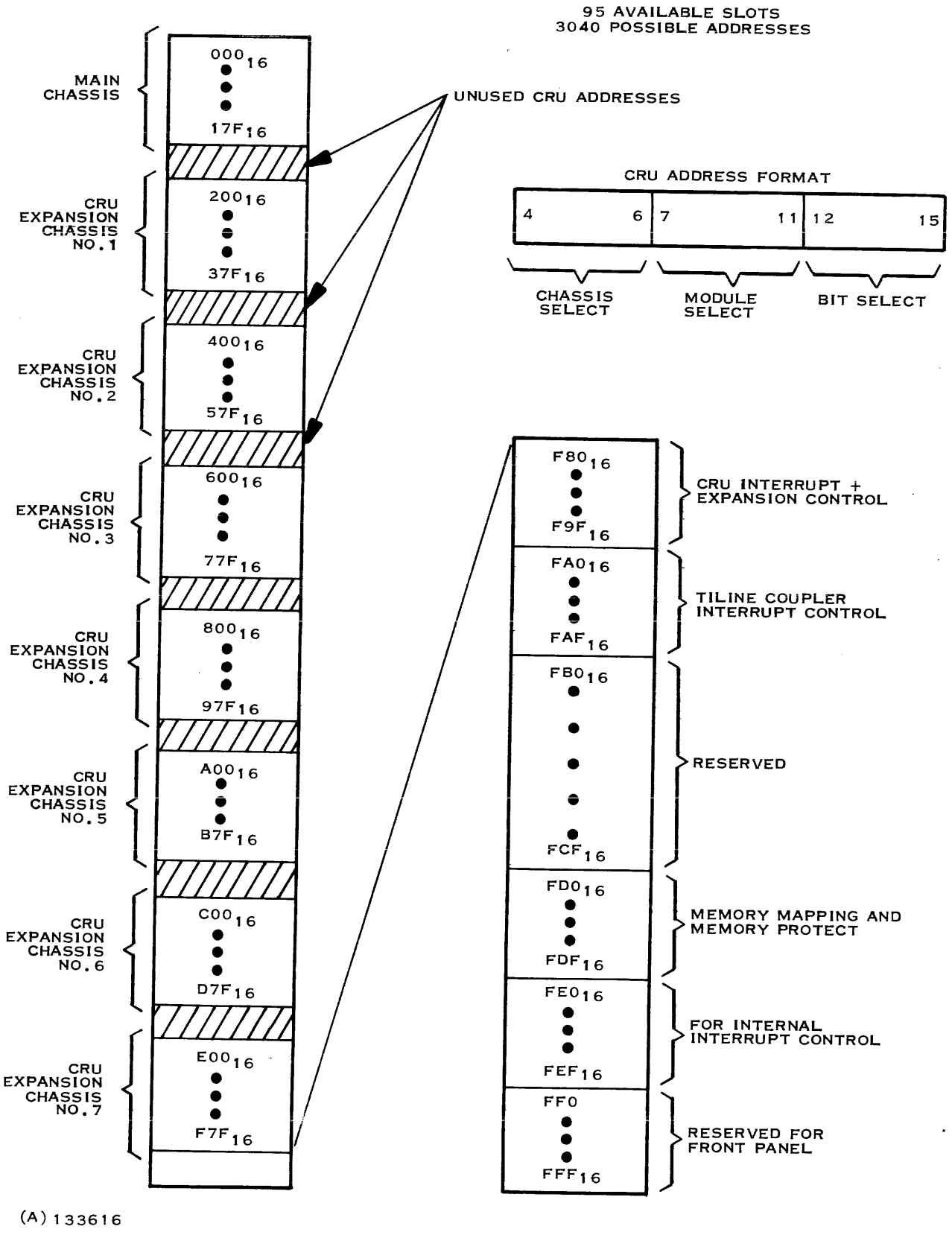


Figure 1-27. CRU Address Map for Standard Expansion Implementation Using 13-slot Chassis

In addition to the location dependent address blocks, several bands of addresses are assigned as dedicated or location-independent addresses. In order to implement the dedicated CRU addresses, the boards associated with these address functions contain decoding logic that permits the board to respond to its dedicated address regardless of location. For example, the two interrupt servicing sections on the CRU expansion board are assigned dedicated addresses F80 and F90, respectively. The interrupt servicing logic on the expander board will respond to these CRU addresses regardless of physical placement of the CRU expansion board. Similarly, the write protect logic on the 990/4 memory expansion board responds to a CRU address ranging between FD0 and FDF regardless of physical placement within the main chassis.

1.2.2.3 **CRU Buffer Board.** The CRU buffer board contains fanout and fanin circuits for the CRU interface signals including CRUBITIN, CRUBITOUT, CRUCLK and CRU address lines. The board also contains an interrupt scanner circuit which monitors the interrupt lines from the various CRU interface boards within the chassis and issues an interrupt to the CRU expander board in the main chassis anytime an interrupt is detected. When the interrupt is acknowledged by means of an ID enable signal, the CRU buffer board sends back the ID code corresponding to the originating interrupt level (1 through 15). The interrupt scanner then halts until software clears the interrupt on the originating board.

The various jumper options on the CRU buffer board are shown in figure 1-28 and are described briefly in the following paragraphs.

Chassis Number Select Plug. The jumper plug P4 may be installed into any of seven slots on J2 to assign a chassis number to a given expansion chassis. This plug determines which of the seven possible chassis decode lines is routed to the module select decode circuitry on the board.

Direct Interrupt Jumper Option. Interrupt level 1 from the interrupt jumper plug on the backpanel board may be routed through the interrupt scanner and processed by the expansion interrupt routine or wired directly to the interrupt plug on the backpanel board in the main chassis to permit faster interrupt processing. The latter method is used when a peripheral requiring fast interrupt processing response time is implemented in one of the expansion chassis.

For conventional scanner processing of interrupt level 1, a jumper wire is installed between DI1, DI3 and DI4. For direct interrupt processing of interrupt level 1, the jumper between DI3 and DI4 is removed and a jumper is installed between DI1 and DI2.

Interrupt Expansion Jumpers. Jumper options are also provided for interrupt levels 0 and 16 through 31 but are not implemented in the current 990/4 system.

Interrupt Scanner Maintenance Options. For normal interrupt scanner option, the jumper wire between E1 and E2 is installed to enable the internal scanner clock. For maintenance operations, the jumper between E1 and E2 may be removed and the interrupt scanner may be driven with an external clock source using terminal E3 as an input point. The scanner may also be cleared by temporarily connecting a ground potential at terminal E4.

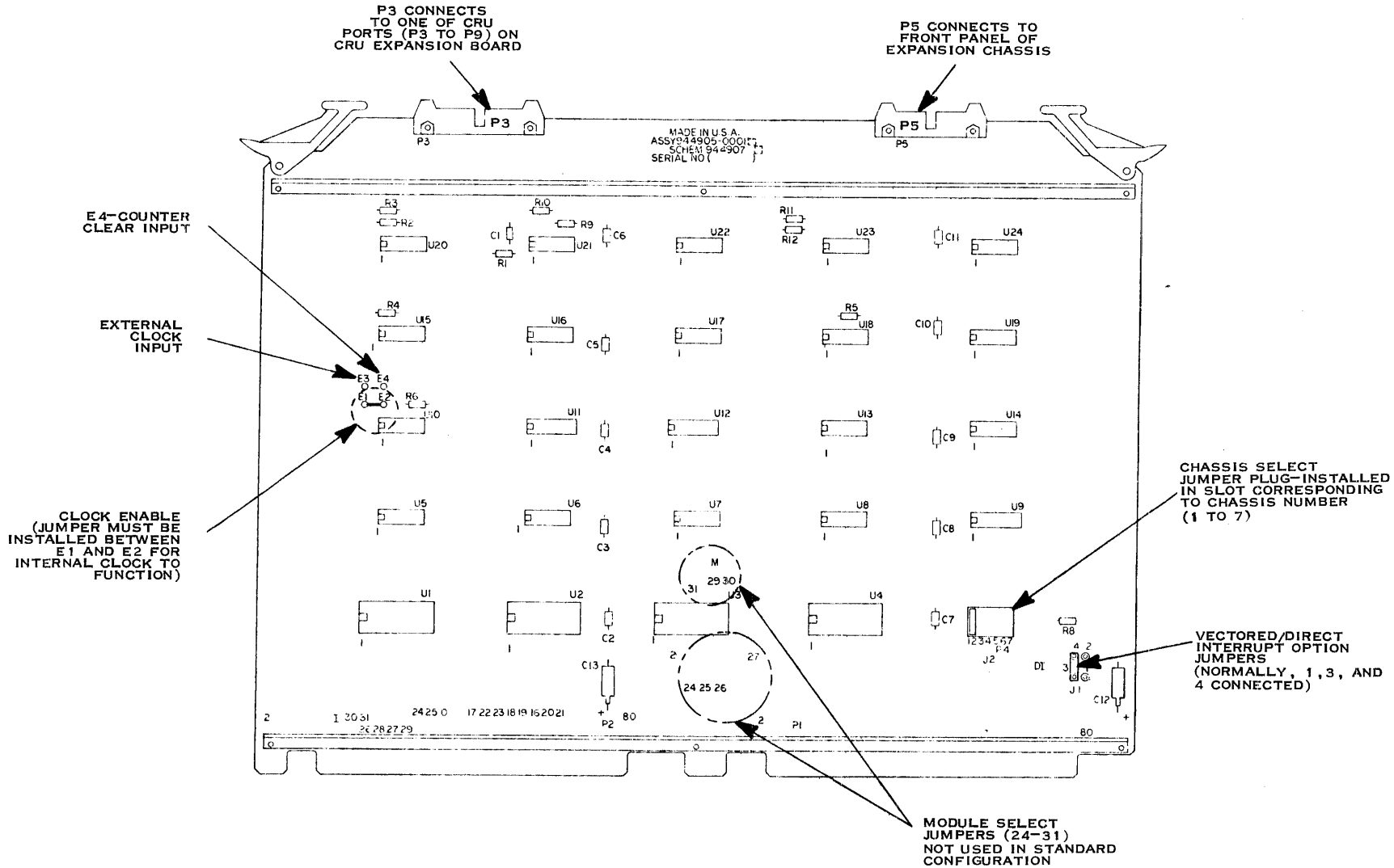


Figure 1-28. CRU Buffer Board Options

SECTION II

FIELD SERVICE TEST EQUIPMENT

2.1 GENERAL

This section describes the 990 Maintenance Unit and other tools, test equipment, diagnostic cassettes and spares required for field-level maintenance of 990/4 Microcomputer Systems.

2.2 TOOLS, TEST EQUIPMENT AND SPARES REQUIRED FOR FIELD MAINTENANCE

A listing of tools, test equipment and replaceable parts required to perform field-level maintenance is provided in tables 2-1 through 2-3, respectively.

2.3 990 MAINTENANCE UNIT

The 990 Maintenance Unit consists of a conventional 990 programmer panel, a 733 ASR cassette transport and a maintenance controller board (containing the cassette read electronics and CRU interfacing logic) all housed in a portable aluminum carrying case as shown in figure 2-1. The maintenance unit permits diagnostics to be loaded into a system not equipped with an operational 733 ASR data terminal and provides for manual control of a computer equipped with an operator panel or inoperative programmer panel. The maintenance unit's carrying case also provides storage space for manuals, CPU ROMs, diagnostic cassettes and interface cables.

Table 2-1. Recommended Tools and Test Equipment for Field-Level Maintenance

Nomenclature	Function	TI Part Number
990 Maintenance Unit (115 Vac Operation)	Used to load diagnostics and display test results in 990/4 systems not equipped with 733 ASR data terminal.	946710-1
990 Maintenance Unit (230 Vac Operation)	Same as above but equipped to operate from 230 Vac input power.	946710-2
14/16 Pin IC inserter/ extractor tool	Used to remove and replace memory ICs.	–
64-pin inserter/ extractor tool	Used to remove and replace TMS 9900 chip.	–
Standard Technician tool kit	Used to assemble/remove assemblies and components and to install new components and assemblies.	–

Table 2-2. 990/4 Diagnostic Tests

Diagnostic Name	Description	TI Part Number
HDT04	Hardware demonstration test; used to verify proper connection of all peripherals.	945460
AU04	990/4 arithmetic unit test.	945434
ROMVER	990 ROM verifier test.	945443
RAM04	990/4 Random access memory test; used to test RAM memory on 990/4 microcomputer board and 990/4 memory expansion board(s).	945440
MEMPRO04	990/4 memory protect test; used to test write protect function on 990/4 memory expansion board.	945442
EROMBT	990 EROM memory module test.	945459
CRUST04	990/4 CRU interface logic test; checks the CRU interface logic on the 990/4 microcomputer board.	945446
TST733	733 ASR/KSR data terminal test.	945447
CRUEXP	990 CRU expansion chassis interface test.	945457
LPTEST	990 line printer diagnostic test.	945448
CARDRD	990 Model 804 card reader test.	945449
CRT913	990 Model 913 CRT diagnostic test.	945450
IO16	990 Model 16 I/O TTL module test.	945452
TTYEIA	990 Full duplex TTY/EIA interface module test.	945453
PROMPG	PROM programmer test.	945454
TILCOM	990 TILINE coupler logic test, synchronous and asynchronous communication interface test.	945458
DAADC	990 Digital to analog and analog to digital converter test.	945438
TINET	990 TINET test.	945448

2.3.1 **TEST CONFIGURATIONS.** The maintenance unit accommodates two different test configurations depending on the system under test. In the first configuration (figure 2-2), the maintenance unit ties into the system under test through P3 on the 990/4 microcomputer board (after removal of the existing interface cable from the chassis-mounted operator or programmer panel). In this configuration, diagnostic programs are loaded into program memory from the cassette tape transport on the maintenance unit and the test results are displayed on the DATA LEDs on the programmer panel in the maintenance unit. This configuration is used when the system is not equipped with an operational 733 ASR data terminal.

Table 2-3. Field Replaceable Components for 990/4 System

Assembly/Subassembly	TI Part Number
LOGIC BOARDS	
990/4 microcomputer board with 4K RAM	944910-2
990/4 microcomputer board with 256 words static RAM	944910-1
990/4 memory expansion board	
• with 4K RAM	944935-1
• with 8K RAM	944935-2
• with 12K RAM	944935-3
• with 16K RAM	944935-4
• with 20K RAM	944935-5
• with 4K and write protect	944935-6
• with 8K and write protect	944935-7
• with 12K and write protect	944935-8
• with 16K and write protect	944935-9
• with 20K and write protect	944935-10
• with 20K, and write protect and parity	944935-10
• with 4K memory parity option	945120-0001
• with 8K memory parity option	945120-0002
• with 12K memory parity option	945120-0003
• with 16K memory parity option	945120-0004
• with 20K memory parity option	945120-0005
990 EPROM memory module	945170-1
CRU expander board	945005-1
CRU buffer board	944905-1
TTY/EIA terminal interface module	945075-1
990 communications interface module	946104-1
913A video display terminal controller	946695-1
Card reader interface module	945185-1
16 I/O EIA data module	945140-1
16 I/O TTL data module	945145-1
Floppy disc controller	945940-1
CHASSIS AND POWER SUPPLY ASSEMBLIES	
3-slot OEM chassis	945040-1
6-slot chassis with programmer panel	944960-1
6-slot chassis with operator panel and 20 ampere power supply	944960-2
13-slot chssis with programmer panel and 40-ampere power supply	945050-1
13-slot chassis with operator panel and 40 ampere power supply	945050-8
AC power converter board	946650-1
20 Ampere main power supply board	944970-1
Standby power supply board	944990-1
Standby power supply kit (with board, batteries and all hardware)	945128-1
International voltage kit, 100 volt service	945125-1
International voltage kit, 230 volt service	945125-2

Table 2-3. Field Replaceable Components for 990/4 System (Continued)

Assembly/Subassembly	TI Part Number
CHASSIS AND POWER SUPPLY ASSEMBLIES (Continued)	
Operator panel assembly	945030-1
Programmer panel assembly	945020-1
Interrupt jumper	975321-4
Chassis center card guide kit	945129-1
CABLE ASSEMBLIES	
CRU expansion cable (12 feet)	945001-1
Model 913A VDT extension cable (50 feet)	974998-50
Model 588/306 line printer extension cable (50 feet)	975056-50
LOADER ROMS, MEMORY CHIPS AND REPLACEABLE ICS	
733 ASR/card reader loader ROM	945121-1
733 ASR/card reader loader ROM with self-test	945121-2
990/4 floppy disc loader ROM	945121-3
990/4 floppy disc loader ROM with self-test	945121-4
733 ASR loader ROM (prototyping)	945121-5
TMS 4050	972659-1
TMS 4043 static RAM (256 X 4-bit)	972658-1
TMS 4051 dynamic RAM (4096 X 1-bit)	972660-1
TMS 4060 dynamic RAM (4096 X 1-bit)	974679-1
1024 by 8-bit EPROM IC	996019-1
SN74180N parity generator/checker	222222-7180
NE 555V	972188-1
TMS 9900 microprocessor chip	972671-1
CHASSIS REPLACEABLE COMPONENTS	
Fuse 1F1, 10 amp slo-blo (BUS MDA10.0)	772995-4
Fuseholder	972690-1
Standby replacement plug	946739-1
13-slot chassis air filter	945152-2
6-slot chassis air filter	945152-1
Terminal block 1TB1	975270-5
Surge voltage protector	974805-7
5-inch fan	947512-1
Ac line filter (1FL1)	972838-5
Capacitor (1C1)	972930-69

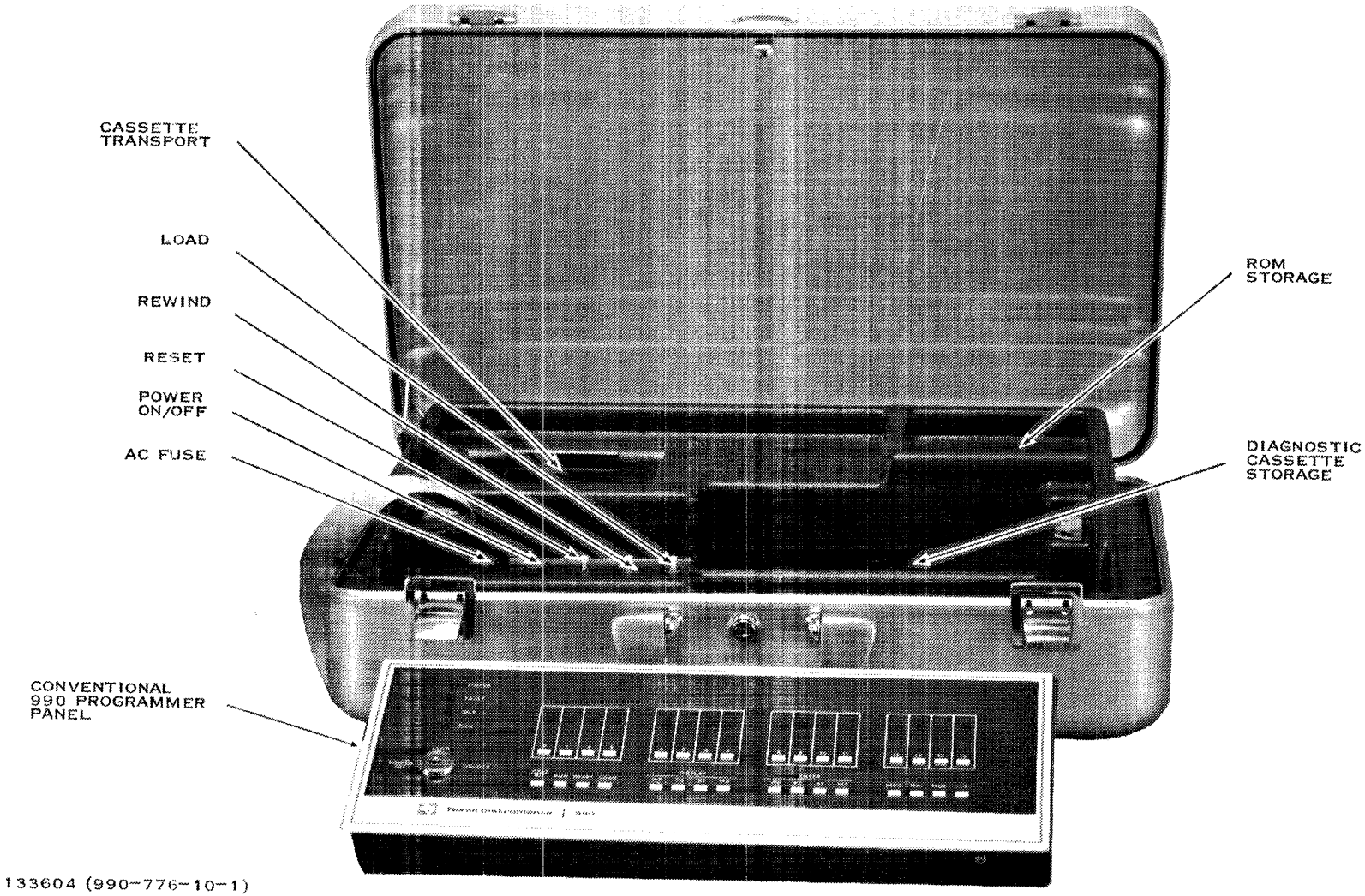


Figure 2-1. Model 990 Maintenance Unit

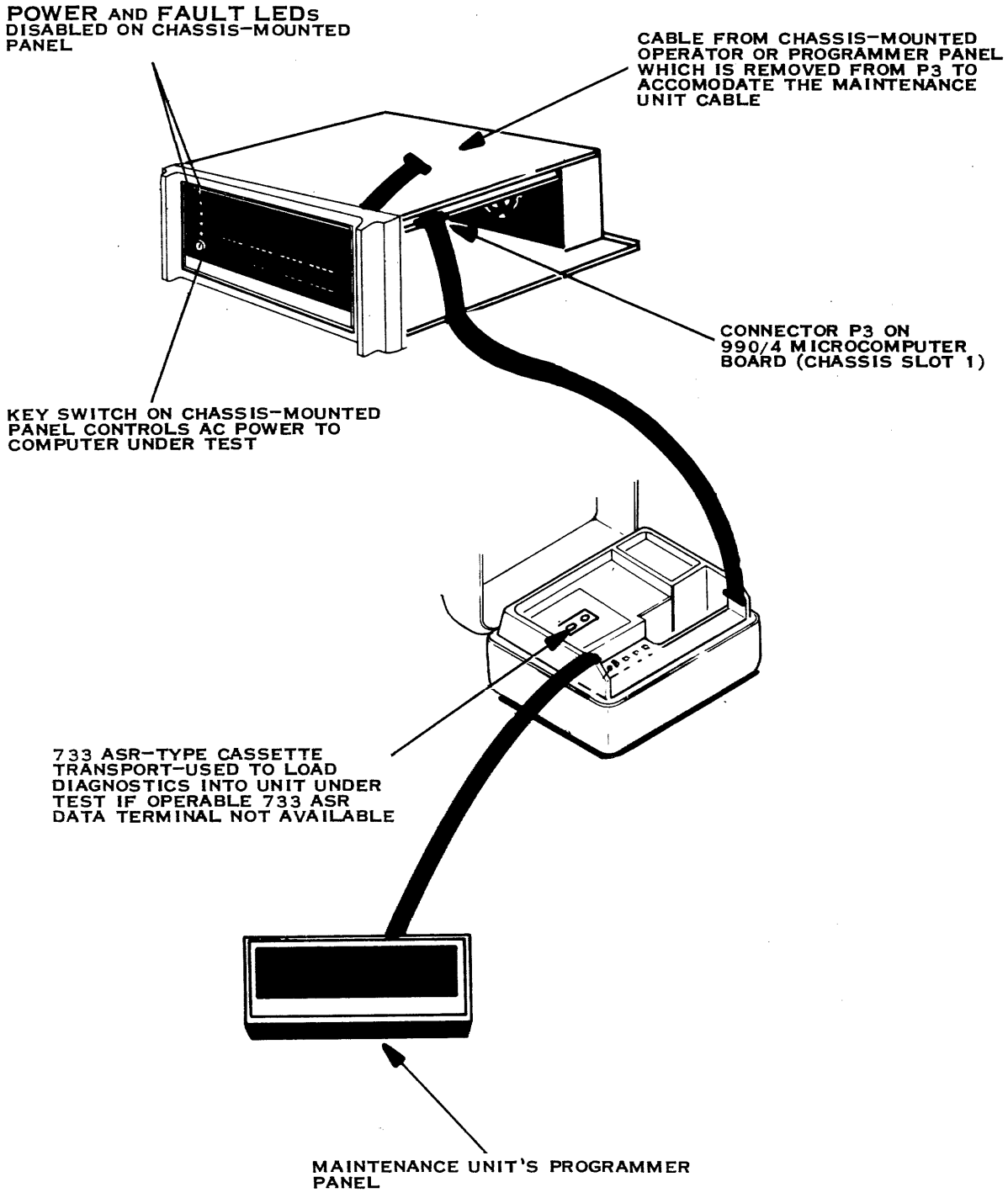


Figure 2-2. Test Setup for System Not Containing Operational 733 ASR Data Terminal

2.3.1.1 **Standalone Programmer Panel.** The programmer panel may also be detached from the maintenance unit and used as a standalone unit. In this case, the existing interface cable from the chassis-mounted operator or programmer panel is removed from P3 on the 990/4 microcomputer board and the maintenance unit's programmer panel interface cable is connected to P3 (see figure 2-3). In this configuration, the key switch on the chassis-mounted panel controls the application of ac power to the computer but all other functions are controlled by the standalone programmer panel.

This configuration is used when the system under test is equipped with an operator panel or inoperative programmer panel but contains an operative 733 ASR data terminal. In this case, the diagnostic cassettes are loaded into the system from the 733 ASR and the programmer panel is used to display test data from selected registers in the TMS 9900 on the 990/4 microcomputer board or from selected memory locations on any of the boards containing memory storage.

2.3.2 **OPERATING CONTROLS AND INDICATORS.** The maintenance unit's operating controls and indicators are shown in figure 2-4 and listed and described in table 2-4. Basically, the maintenance unit contains a POWER ON/OFF switch which controls power to the maintenance unit, a RESET switch which initializes the controller board in the maintenance unit, a REWIND switch which is used to rewind cassette tapes, a LOAD switch which is used to initiate diagnostic load operations plus the conventional controls and indicators found on the 990 programmer panel. However, the function of three of the programmer panel controls and indicators are slightly different when the programmer panel is used as a part of the maintenance unit. These differences include:

- Key switch – Does not affect ac power to the computer or maintenance unit, but otherwise exercises the same key control over program intervention in the computer.
- POWER LED – Indicates the status of the power supply in the maintenance unit rather than the power supply in the computer chassis.
- FAULT LED – May be lit by either the computer (self-test failure) or by the maintenance controller board in the maintenance unit in the event of a faulty tape read operation.

The functions of all other programmer panel controls and indicators are exactly the same as those of a conventional chassis-mounted programmer panel (see figure 2-4 and table 2-4).

2.3.2.1 **Maintenance Unit Operating Procedures.** Some of the more common operating procedures are briefly described in the following paragraphs. These procedures include:

- Changing panel mode of operation
- Mounting cassette tapes in maintenance unit
- Diagnostic load from cassette transport in maintenance unit
- Entering data into CPU registers or memory locations
- Displaying data from CPU registers or memory locations
- Single instruction execution

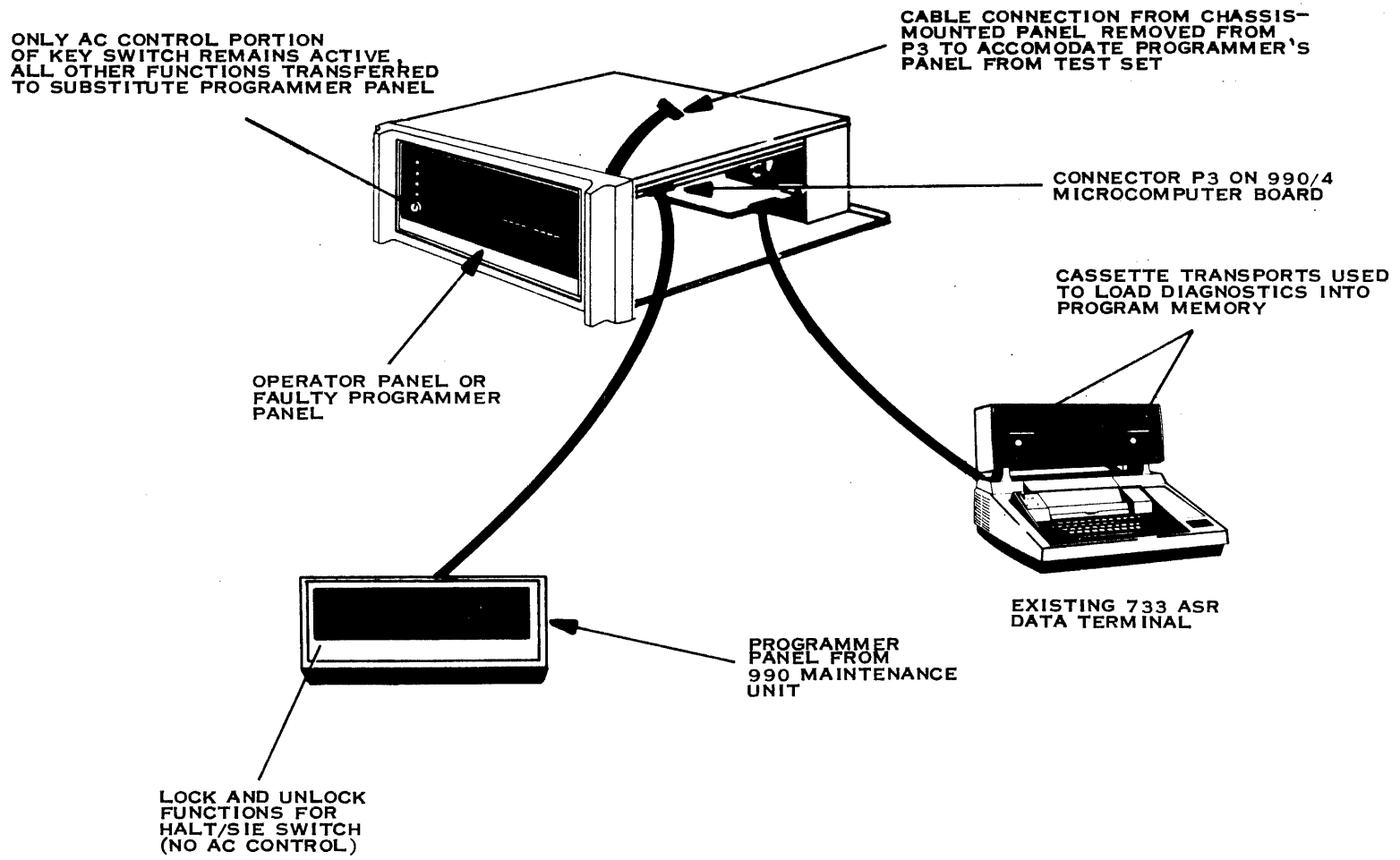


Figure 2-3. Alternate Test Setup Using Programmer Panel Only

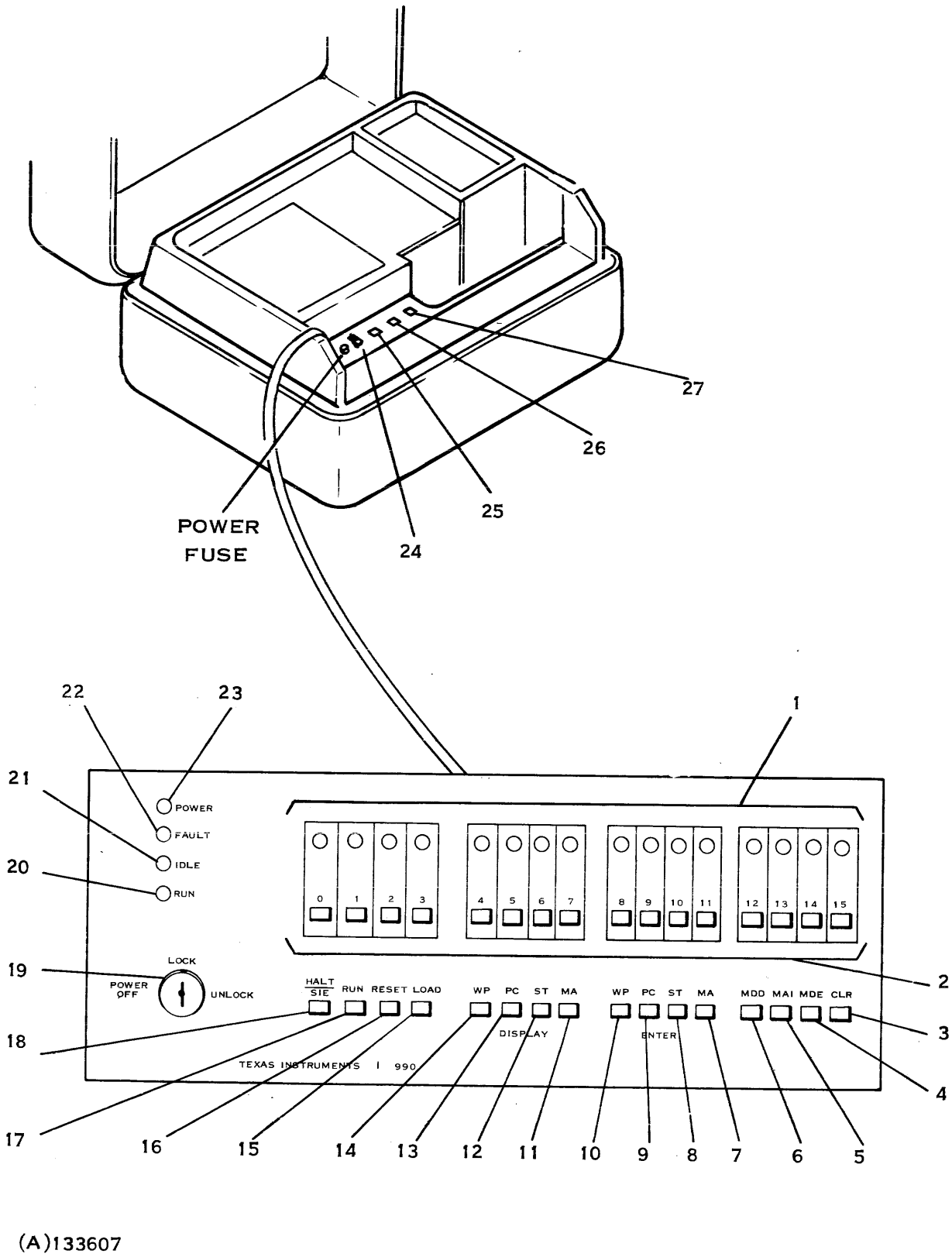


Figure 2-4. Maintenance Unit Controls and Indicators

Table 2-4. Maintenance Unit Controls and Indicators

Ref. No.	Control or Indicator	Function
1	DATA LEDs	The DATA LEDs are used to display data being entered into a CPU register or memory location or data presently stored in a register or memory location. During execution of the diagnostics, error numbers (in hex) are displayed on the right byte and the left byte is forced to all 1's (see error message number descriptions in 990 Computer Diagnostics Handbook). A lit LED denotes a logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the HALT mode, the LEDs display a computer register contents, memory contents or value entered into computer memory via the data entry switches depending on which switches are pressed (see ref. 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel to enter data and addresses into selected computer registers and memory locations (active only when the panel is in the HALT mode of operation). In the HALT mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays.
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.
13	DISPLAY PC	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.

Table 2-4. Maintenance Unit Controls and Indicators (Continued)

Ref. No.	Control or Indicator	Function
14	DISPLAY WP	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.
15	LOAD switch	For a programmer panel on the chassis (or PANEL mode of operation for the maintenance unit), pressing the switch causes the computer to trap to the ROM loader.
16	RESET switch	Pressing the RST switch results in an IORESET– pulse being generated which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the RUN mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the RUN mode (RUN LED is lit), pressing the HALT/SIE switch causes the computer to halt and begin processing the front panel software *if* the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the RUN mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) switch prevents unauthorized computer program intervention. The key must be inserted into the switch and the switch set to the UNLOCK position in order to enable the output of the HALT/SIE switch to the computer. The ac power control function for the 990/4 computer is controlled by the key switch on the chassis-mounted operator or programmer panel.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the RUN mode. When this LED is lit, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	Lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a self-test diagnostic failure or if the maintenance unit has detected a tape data fault.
23	POWER LED	Lights when the POWER ON/OFF switch on the maintenance unit is set to the ON position and the maintenance unit's internal power supply is functioning properly.
24	POWER ON/OFF switch	Controls ac power to the maintenance unit.
25	RESET switch	Initializes the logic on the maintenance unit's maintenance controller board. Has no affect on the system under test.
26	REWIND switch	Causes the cassette tape in the cassette transport to rewind back to the beginning of the tape (tape motion stops when clear leader is sensed).
27	LOAD switch	When the programmer panel is in the HALT mode (RUN LED extinguished), this switch causes the program on cassette tape to be loaded into memory. When the load is complete, program execution begins.

Changing Panel Mode of Operation. The programmer panel in the 990 maintenance unit may be operated in one of two modes including RUN and HALT. The computer initially comes up in the RUN mode when ac power is applied to the computer through the key switch on the chassis-mounted front panel. During this time, the RUN LED and all DATA LEDs on the programmer panel in the maintenance unit light and remain lit until the mode of operation changes. If the key switch on the programmer panel in the maintenance unit is set to the LOCK position, all controls on the panel are disabled. To change from the RUN mode of operation to the HALT mode, the key must be inserted in the switch and the key switch must be rotated to the UNLOCK position. At this point, only the HALT/SIE switch on the panel is enabled. When the HALT/SIE switch is pressed, the computer ceases normal program execution and traps to the panel software utility which is located in a ROM in the upper 256 words of address space on the 990/4 microcomputer board. At this time, the RUN LED on the programmer panel extinguishes and the outputs of the switches on the programmer panel are constantly monitored by software through the programmer panel CRU type interface. At this point, the panel is operating in the HALT mode.

In the HALT mode, a diagnostic tape may be loaded from the maintenance unit or information may be entered into or displayed from selected CPU registers or program memory locations.

In order to switch from the HALT mode of operation to the RUN mode, the RUN switch must be pressed on the programmer panel. This causes the TMS 9900 on the 990/4 microcomputer board to begin program execution at the memory address indicated by its program counter.

Mounting and Removing Tape Cassettes. In order to load a diagnostic tape cassette into the maintenance unit, the cassette transport door must be opened and the cassette inserted with the tape end up. The desired diagnostic title should be facing the operator as shown in figure 2-5. The cassette should then be firmly pressed into the transport such that the capstan and reel motors properly engage the cassette tape and reels. The transport door must then be closed to complete installation of the cassette.

To remove a cassette from the transport, the door should be opened to the first stop and then opened the rest of the way using a quick downward motion. This causes the cassette to eject from the tape transport. When not in use, the transport door should be closed to prevent accumulation of dust or dirt in the tape drive mechanism and read head.

Loading a Diagnostic Into Program Memory. Before initiating a load from a cassette tape, the POWER ON/OFF switch should be set to the ON position and the tape fully rewound by pressing the REWIND switch on the maintenance unit (reference no. 26 in figure 2-4). The tape motion will automatically stop when the clear leader at the beginning of the tape is sensed by the maintenance controller board.

The Key switch on the 990/4 microcomputer's chassis-mounted operator or programmer panel must be set to one of the ON positions (ON, LOCK, or UNLOCK) to apply ac power to the computer. At this point, the RUN and POWER LEDs should light on the programmer panel in the maintenance unit. The panel's mode of operation must then be changed to the HALT mode by setting the Key switch on the maintenance unit's programmer panel to the UNLOCK position and pressing the HALT/SIE switch. The RUN LED on the panel should extinguish indicating the TMS 9900 is now processing the panel software utility. At this point, the panel software begins examining the switch outputs from the programmer panel. The cassette diagnostic load operation may now be initiated by pressing the LOAD switch (reference no. 27 in figure 2-4) on the

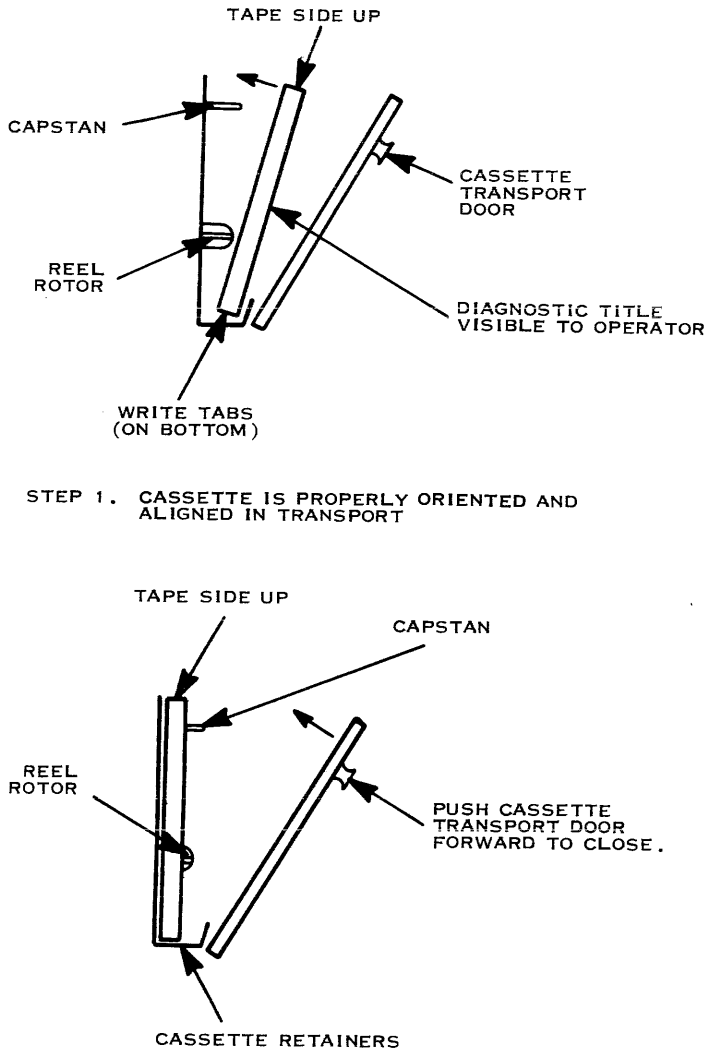
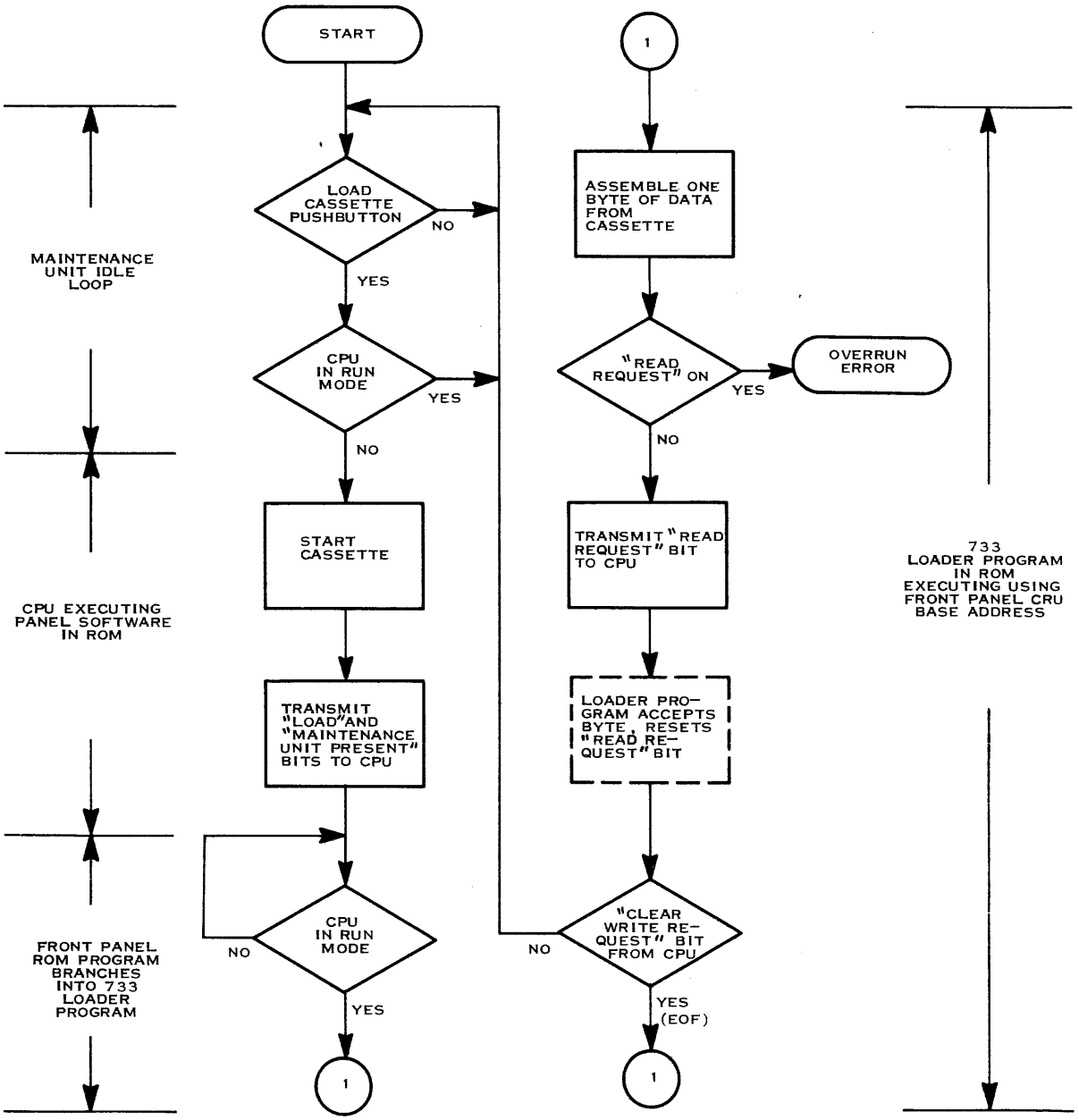


Figure 2-5. Cassette Tape Installation, Simplified Diagram

maintenance unit. The panel software recognizes the combination of the Load signal with the Maintenance Unit Present signal as a "Load from maintenance unit cassette" command (refer to the flowchart in figure 2-6). As a result, the panel software branches to the self-test program (if the loader ROM is equipped with self-test). If the self-test fails to execute correctly, the TMS 9900 lights the FAULT LED on the programmer panel in the maintenance unit and inhibits the diagnostic load operation.

However, if the self-test executes satisfactorily (or if self-test is not present), the CPU branches to the ASR loader program which is also stored in ROM on the 990/4 microcomputer board. Since the load signal occurred with maintenance unit present, the software retains the CRU base address of the front panel.



(A)133609

Figure 2-6. Diagnostic Load From Maintenance Unit, Flowchart

At this point, the maintenance unit waits for RUN to turn on and then begins transmitting tape read data over the programmer panel CRU interface under control of the 733 loader program. Each time the maintenance controller board in the maintenance unit has a byte of data ready for the computer, it sets CRU bit 12 which is interpreted by software as a Read Request. When the 733 loader recognizes the Read Request, it serially transfers the next byte of data from the maintenance unit and resets CRU bit 12, freeing the maintenance unit to ready the next data byte. If the maintenance unit has another byte of data available before the loader has accepted the previous data byte (CRU bit 12 still set to the computer), the load operation is aborted and the FAULT LED lights on the maintenance unit's programmer panel. When the 733 loader decodes an End of File tag, it sets Clear Write Request via CRU output bit 13 which causes the maintenance unit to stop the cassette transport and return to an idle state.

SECTION III

MAINTENANCE

3.1 GENERAL

This section contains preventive and corrective field-level maintenance procedures for 990/4 microcomputer systems. This section includes assembly and disassembly procedures plus instructions for evaluating each system configuration and incorporating the necessary jumper options on replacement boards before installing the boards in a given system.

3.2 PREVENTIVE MAINTENANCE

Preventive maintenance for the 990/4 microcomputer system is limited to cleaning the washable intake air filter on each computer or expansion chassis in the system on a monthly basis (or more often if required) and periodically executing the diagnostics listed in table 2-2 to ensure that the system is functioning properly. All other preventive maintenance procedures are associated with the system peripherals and are described in the *Model 990 Peripheral Equipment Field Maintenance Manual.*

3.2.1 FILTER REMOVAL/REPLACEMENT. The washable filter used in the 990 chassis snaps into place and is removed by applying finger pressure along the top and bottom edges.

3.3 CORRECTIVE MAINTENANCE

Corrective maintenance at the field-level for the 990/4 is limited to the following:

- Removal and replacement of logic boards in the main chassis or one of the expansion chassis
- Removal and replacement of power supply boards
- Removal and replacement of interconnecting cables
- Removal and replacement of plug-in memory chips, ROM loaders and other 16-pin ICs
- Removal and replacement of the TMS 9900 microprocessor chip on the 990/4 microcomputer board
- Removal and replacement of the front panel assembly (programmer panel or operator panel) and/or key switch assembly
- Removal and replacement of cooling fans and ac power distribution components

3.3.1 LOGIC BOARD REMOVAL AND REPLACEMENT PROCEDURES. Logic boards are removed from a computer or I/O expansion chassis using the following procedure.

CAUTION

Always turn off power to the chassis before attempting logic board removal. Failure to observe this precaution may result in damage to the board since connector pins are temporarily misaligned during board removal and installation.

1. Set the KEY switch on the front panel of the chassis to the OFF position and remove the key to prevent accidental turn on before the new board has been installed.

2. Remove any top-edge cable connectors which may be mounted on the board.

3. Free the board from the backpanel connectors using the ejector tabs on the top of the board.

4. Remove board from chassis and immediately tag the board with such information as symptom, chassis and slot which the board was removed from and the system location and number (when several systems are installed at the same site).

5. Carefully record the jumper options and any other options (such as parity option, amount of memory, types of ROM loaders and custom ROMs, etc.) which may be installed on the board. These same options must be installed on the replacement board prior to installing the board in the system.

NOTE

Refer to table 3-1 for a summary of board and system options. Additional board and system option descriptions are provided in Section I of this manual.

6. Install the same options on the replacement board (unless an obvious problem is detected with the original setup of the board).

7. Note the serial number and board options incorporated on the replacement board and transfer this data to the system's configuration chart.

3.3.2 **OPERATOR/PROGRAMMER PANEL REMOVAL AND REPLACEMENT.** The front panel (either operator or programmer panel) may be removed and replaced using the following procedure.

WARNING

Prior to attempting the following removal procedure, disconnect the chassis power cord from ac power. The 115 Vac hot lead is exposed when the panel is removed.

1. Remove the left-side access panel (directly opposite the open side of the chassis) by removing the six holding screws around the perimeter of the panel.

2. Remove two screws from the rear of the panel on each side of the chassis (4 screws total).

3. Remove the two terminal leads from the ac microswitch on the rear of the key switch (the ac microswitch is the leftmost switch as viewed from the rear as shown in figure 3-1).

4. Remove connector plug 1A4P3 from top edge of 990/4 microcomputer board and push plug through slot in chassis.

5. Install replacement panel by reversing the above procedure. See figure 3-2 for correct orientation of connector plug.

3.3.3 **POWER SUPPLY REMOVAL AND REPLACEMENT.** The 990 power supply consists of a 20 or 40 amp main power supply board, an ac power converter board and an optional standby power supply board and batteries. Removal and replacement procedures for these assemblies are provided in the following paragraphs.

WARNING

The chassis ac power cord must be removed from ac power before attempting the following power supply board removal procedures. Dangerous ac and dc voltages are exposed if this precaution is not observed.

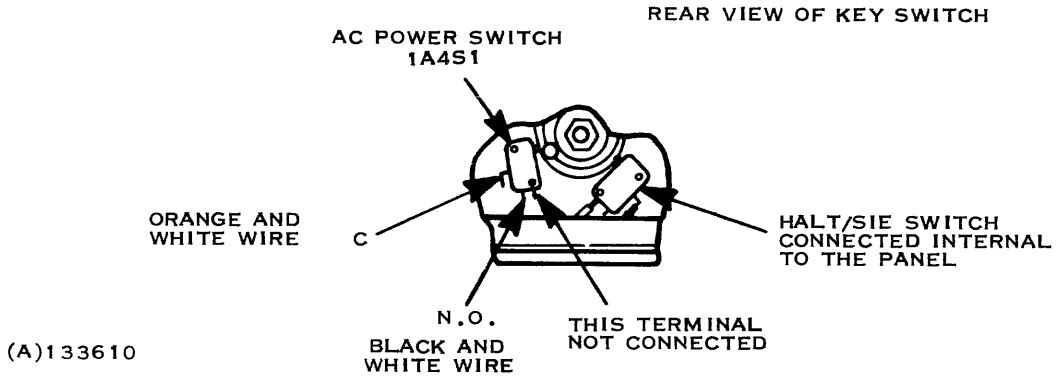


Figure 3-1. 1A4S1 Switch Connections

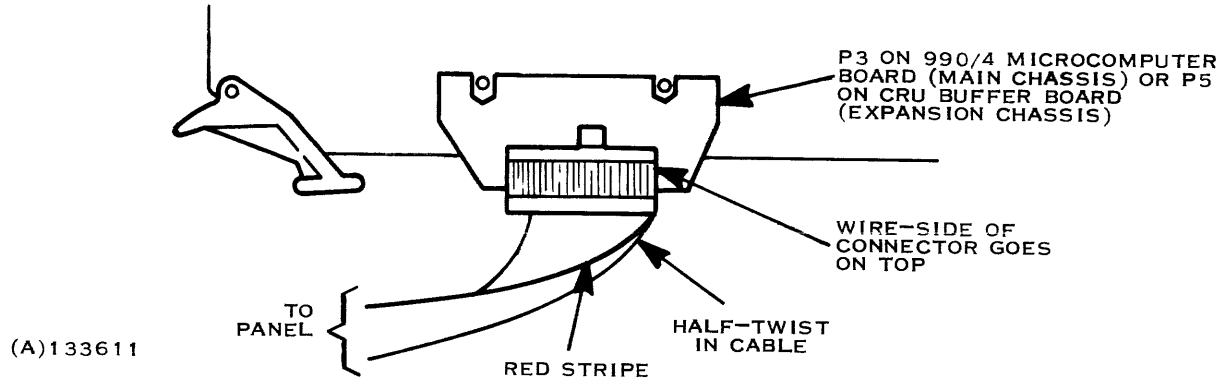


Figure 3-2. Programmer/Operator Panel Cabling Diagram

Table 3-1. Summary of 990/4 Jumper Options

990/4 MICROCOMPUTER BOARD

PROM/RAM Starting Address	Jumper Option
0000_{16} (0)	E19 to E20; E24 to E25
0800_{16} (1K)	E19 to E20; E24 to E26
$F000_{16}$ (30K)	E19, E20 Open; E24 to E25
$F800_{16}$ (31K)	E19, E20 Open; E24 to E26
PROM/Static RAM Option	
Bank 0 = PROM	E7 to E8
Bank 0 = RAM	E7, E8 Open
Bank 1 = PROM	E5 to E6
Bank 1 = RAM	E5, E6 Open
Bank 2 = PROM	E3 to E4
Bank 2 = RAM	E3, E4 Open
Bank 3 = PROM	E1→E2
Bank 3 = RAM	E1, E2 Open
Dynamic RAM Starting Address	
Start address = 0000_{16} (0)	E16 to E17
Start address = 2000_{16} (4K)	E17 to E18
Power-Up Trap Vector	
Vector at address = 0000_{16}	E22 to E27
Vector at address = $FFFC_{16}$	E21 to E22
Clock Interrupt Level	
Level = Interrupt 5	E9 to E10
Level = Interrupt 7	E10 to E23
Clock Interrupt not Connected	E9, E10, E23 Open
Memory Error Interrupt	
Connected to Interrupt 2	E13 to E14
Not Connected	E13, E14 Open
Power-Fail Interrupt	
Connected to Interrupt 1	E11 to E12
Not Connected	E11, E12 Open

Table 3-1. Summary of 990/4 Jumper Options (Continued)

990/4 MEMORY EXPANSION BOARD

Starting Address	Switch Settings
0000_{16} (0)	S2, S3 and S4 off
2000_{16} (4K)	S2, S3 off; S4 on
4000_{16} (8K)	S2 off; S3 on; S4 off
6000_{16} (12K)	S2 off; S3, S4 on
8000_{16} (16K)	S2 on, S3, S4 off
$A000_{16}$ (20K)	S2 on, S3 off; S4 on
$C000_{16}$ (24K)	S2, S3 on; S4 off
$E000_{16}$ (28K)	S2, S3, S4 on

Memory Size	Jumpers Required
4K	None
8K	Jumper E1 to E2 (E3 thru E6 OPEN)
12K	Jumper E3 to E4 (E1, E2, E5 and E6 OPEN)
16K	Jumper E1 to E2, E3 to E4 (E5 and E6 OPEN)
20K	Jumper E5 to E6 (E1 thru E4 OPEN)

Write Protect Option	Jumpers Required
Option installed	E7 and E8 OPEN
Option not installed	Jumper between E7 and E8

EPROM MEMORY MODULE

Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5	Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5
0000	(0)	off	off	off	off	off	9000	(18K)	on	off	off	on	off
0800	(1K)	off	off	off	off	on	9800	(19K)	on	off	off	on	on
1000	(2K)	off	off	off	on	off	A000	(20K)	on	off	on	off	off
1800	(3K)	off	off	off	on	on	A800	(21K)	on	off	on	off	on
2000	(4K)	off	off	on	off	off	B000	(22K)	on	off	on	on	off
2800	(5K)	off	off	on	off	on	B800	(23K)	on	off	on	on	on
3000	(6K)	off	off	on	on	off	C000	(24K)	on	on	off	off	off
3800	(7K)	off	off	on	on	on	C800	(25K)	on	on	off	off	on
4000	(8K)	off	on	off	off	off	D000	(26K)	on	on	off	on	off
4800	(9K)	off	on	off	off	on	D800	(27K)	on	on	off	on	on
5000	(10K)	off	on	off	on	off	E000	(28K)	on	on	on	off	off
5800	(11K)	off	on	off	on	on	E800	(29K)	on	on	on	off	on
6000	(12K)	off	on	on	off	off	F000	(30K)	on	on	on	on	off
6800	(12K)	off	on	on	off	on	F800	(31K)	on	on	on	on	on

Table 3-1. Summary of 990/4 Jumper Options (Continued)

EPROM MEMORY MODULE

Starting Address (Hex Byte Addresses)	Bias Switch Setting S1	S2	S3	S4	S5	Starting Address (Hex Byte Addresses)	Bias Switch Setting S1	S2	S3	S4	S5
7000 (14K)	off	on	on	on	off						
7800 (15K)	off	on	on	on	on						
8000 (16K)	on	off	off	off	off						
8800 (17K)	on	off	off	off	on						

Memory Size	Jumpers Required
1K	E1 to E2; E4 to E5; E7 to E8
2K	E1 to E2; E4 to E5; E8 to E9
3K	E1 to E2; E5 to E6; E7 to E8
4K	E1 to E2; E5 to E6; E8 to E9
5K	E2 to E3; E4 to E5; E7 to E8
6K	E2 to E3; E4 to E5; E8 to E9
7K	E2 to E3; E5 to E6; E7 to E8
8K	E2 to E3; E5 to E6; E8 to E9

Computer Type	Jumper Required
990/4	E11 to E12; E10 OPEN

CRU EXPANSION BOARD

Reset Source	Jumper Required
TLPRES	Jumper E1 to E2, E3 and E4 OPEN
IORES	Jumper E3 to E4; E1 and E2 OPEN

Interrupt Section Enable Option	Jumper Required
Interrupt Section A enabled	Jumper E5 to E6
Interrupt Section B enabled	Jumper E7 to E8

CRU BUFFER BOARD

Chassis No. Select Option	Jumper Required
1	P4 in position 1
2	P4 in position 2
.	.
.	.
.	.
7	P4 in position 7

Table 3-1. Summary of 990/4 Jumper Options (Continued)

Interrupt 1 Options	Jumpers Required
Direct Interrupt	Jumper D11 to D12, D13 and D14 OPEN
Interrupt 1 to Scanner	Jumper D13 to D14, D11 and D12 OPEN

Internal Clock Option	Jumper Required
Internal Clock Enabled	Jumper E1 to E2
Internal Clock Disabled (External clock input at E3; Clear input at E4)	E1 and E2 OPEN

3.3.3.1 **Main Power Supply Board Removal and Replacement.** The main power supply board is removed and replaced using the following procedure:

1. If standby power supply is installed, this board must be removed first using the procedures provided in paragraph 3.3.3.3.
2. Remove 4 holding screws (2 from each end of board) and three standoffs from center of board.
3. Remove connectors 1A3P1A and 1A3P2 from board. Also, remove 1A3P1B if 40 amp main power supply board is being removed.
4. Carefully pull board straight back to unplug connector 1A3P3 from backpanel board.
5. Install replacement board by aligning board with two board guide pins which protrude from the backpanel board.
6. Carefully exert gentle pressure near the middle of the bottom edge of the replacement board to mate the backpanel and board connectors.
7. Install holding screws and standoffs removed from faulty board.
8. Install connectors 1A3P1A and 1A3P2 (also 1A3P1B if 40 amp supply).
9. Install 1A3P3 on 1A3J3 if standby power supply option is used. If standby option is not used, install standby replacement plug (Part Number 946739-1) on 1A3J3.

3.3.3.2 **Ac Power Converter Board Removal and Replacement.** The ac power converter board is removed and replaced using the following procedures.

WARNING

Remove chassis power plug from ac outlet before attempting the following removal/replacement procedures.

1. Remove the chassis filter by applying finger pressure along the top and bottom edges of the filter.

2. Remove the rear access cover (directly behind the filter unit) by removing the six screws around the perimeter of the cover.

3. Remove three cable connectors (1A2P1, 1A2P2, and 1A2P3) from board.

4. Remove single screw from center of board and remove board from chassis.

5. The replacement procedures are essentially the reverse of the removal procedures described in steps 1 through 4.

3.3.3.3 **Standby Power Supply Board Removal and Replacement.** The standby power supply is removed and replaced using the following procedures.

WARNING

Do not attempt removal of the standby power supply board without first unplugging the chassis power plug from the ac outlet.

1. Remove connector plugs 1A6P1 and 1A6P2 from standby board and remove 1A6P3 from 1A3J3 on main power supply board.

2. Remove five holding screws from board.

3. Installation of a replacement board is the reverse of steps 1 and 2.

3.3.3.4 **Cooling Fan Removal and Replacement.** The cooling fans in the 990 chassis may be removed and replaced using the following procedure.

WARNING

Before removing the rear access cover, remove chassis power plug from ac outlet.

1. Remove chassis filter by applying finger pressure at top and bottom of filter.

2. Remove rear access cover plate by removing six screws around perimeter of cover plate.

3. Remove two plug-on terminal wires from faulty motor.

4. Remove holding screws and lift motor out of chassis.

5. Install new motor by reversing steps 1 through 4.

3.3.4 **IC REMOVAL AND REPLACEMENT.** All memory ICs used on 990/4 logic boards are plug-in types which are installed in soldered-in IC sockets. These ICs may be removed and replaced using an IC extractor/installer tool. Since the IC leads are slightly flared, a special tool must be used to compress these leads during removal and installation.

NOTE

Failure to use the proper tool can result in bent pins and improperly seated ICs.

Also, correct IC orientation must be observed when installing a new IC. As shown in figure 3-3, the IC index should face the left side of the board for horizontally mounted ICs and face the bottom of the board for vertically oriented sockets.

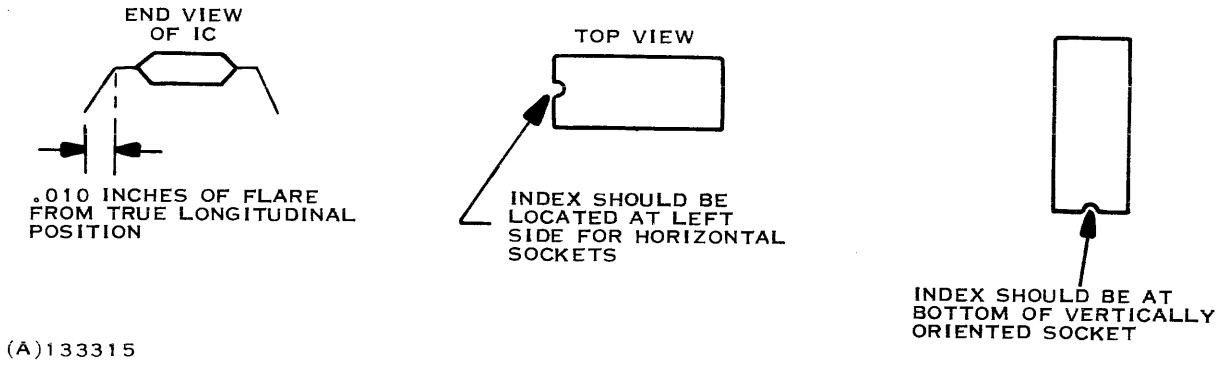


Figure 3-3. IC Installation Diagram

SECTION IV

TROUBLESHOOTING

4.1 GENERAL

This section provides troubleshooting procedures to permit rapid isolation of system failures down to a replaceable logic board or cable assembly. Once a suspect subassembly has been identified, the subassembly is removed and replaced in accordance with the corrective maintenance procedures provided in Section III. In the case of a peripheral failure, additional maintenance information is provided in the *Model 990 Computer Peripheral Equipment Field Maintenance Manual.*

4.2 MAINTENANCE PHILOSOPHY

The maintenance philosophy for the 990/4 Microcomputer System at the field-maintenance level is based on a careful evaluation of the customer-failure report. Then the system checkout chart in table 4-1 helps locate system malfunctions, and the procedures provided in table 4-2, combined with the field service test equipment described in Section II and the system-level troubleshooting diagrams in Section V, isolate the malfunction down to the replaceable subassembly (logic card, power supply board, programmer panel/operator panel, cable or plug-in type IC in some cases).

Once a suspect board is identified, the board is removed in accordance with the procedures provided in Section III and the suspect board is *immediately* tagged. The replacement board (or other subassembly) is then modified to incorporate the jumper-wire options and any other options originally installed on the faulty board (see instructions in Section III). The replacement board is then installed in the system and the system is retested in accordance with the procedures provided in table 4-1.

4.2.1 DISPOSITION OF FAULTY SUBASSEMBLY. The removed subassembly (less any special-purpose ROMS) should then be packaged for shipment back to the factory using the packing materials removed from the replacement subassembly. In order to avoid damage in shipment, the subassembly should be carefully packed according to the instructions provided in Section VI.

4.3 TROUBLESHOOTING PROCEDURES

A logical approach to troubleshooting a 990/4 microcomputer system is presented in table 4-1. Once a malfunction is discovered, the fault-isolation procedures in table 4-2 should be used to identify the faulty subassembly.

Table 4-1. 990/4 Microcomputer System Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	Evaluate system problem report and hardware configuration to determine if 990 Maintenance Unit or the unit's programmer panel will be required to troubleshoot the system. If the system is equipped with both an operable 733 ASR data terminal and operable programmer panel, the Maintenance Unit is not required. However, if the system under test does not contain a 733 ASR, the 990 Maintenance Unit is connected to P3 on the 990/4 microcomputer board and all programmer panel functions (except ac power control) is transferred to the programmer panel in the maintenance unit (see figure 2-2). If the system contains a 733 ASR but does not contain an operable programmer panel, install the programmer panel from the maintenance unit on P3 of the 990/4 microcomputer board as shown in figure 2-3.	–	–
2	If system is off, set key switch on chassis front panel to the LOCK or ON position and observe the POWER LED on the active programmer panel.	POWER LED lights	See step 1 in table 4-2
3	Observe RUN LED on active programmer panel.	RUN LED should light	See step 5 in table 4-2
4	Set key switch on active programmer panel (either chassis-mounted or panel in the 990 Maintenance Unit) to UNLOCK position.	–	–
5	Press HALT/SIE switch on active programmer panel.	RUN LED extinguishes	See step 4 in table 4-2
6	If 733 data terminal will be used to load diagnostics into system, proceed to step 7. If the maintenance unit is hooked to the system, skip to step 8 and continue the procedural steps.	–	–
7	DIAGNOSTIC LOAD PROCEDURE FOR 733 ASR TERMINAL		
	a. Install AU04 diagnostic (part no. 945434) into cassette transport (either 1 or 2) and set the PLAYBACK/RECORD switch so that transport containing diagnostic is in PLAYBACK mode. Set POWER switch to ON.	–	–
	b. Rewind the cassette by momentarily pressing REWIND.	END LED lights and tape motion ceases.	See 733 ASR Operating Manual
	c. Press LOAD/FF to position tape at the beginning.	READY LED lights	–
	d. Setup the terminal's control switches for online operation as follows: • Set ONLINE switch to ONLINE position • Set KEYBOARD, PLAYBACK and PRINTER switches to LINE positions		
	e. Press LOAD switch on active programmer panel.	PLAYBACK ON LED on the 733 lights; cassette tape moves forward in short jerky steps. When load is complete, diagnostic ID is printed out on terminal and program execution begins.	See step 6 in table 4-2
	f. Proceed to step 9 of this table.		
8	DIAGNOSTIC LOAD FROM MAINTENANCE UNIT		
	a. Install AU04 diagnostic cassette (part no. 945434) into cassette transport on maintenance unit.	–	–
	b. Set POWER ON/OFF switch to ON position.	–	–

Table 4-1. 990/4 Microcomputer System Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
8 (Cont)	c. Press REWIND switch. d. Press LOAD on the maintenance unit.	Cassette rewinds and halts at clear leader. Tape load begins; tape moves forward in short jerky steps. When load is complete, ID is displayed on programmer panel.	See step 6 in table 4-2
9	The AU04 diagnostic checks each instruction in the TMS 9900 microprocessor's instruction set and verifies the real time clock interrupt logic on the 990/4 microcomputer board. NOTE This test is applicable only for the dash 2 configuration of the 990/4 board with 4K RAM memory. For a description of the test options available with the AU04 test, refer to the 990 Computer Diagnostic Handbook.	No error message printout (733) or error number display on programmer panel. (Error message numbers are displayed in the right byte of the DATA LEDs and the left byte is forced to FF_{16} when using programmer panel for error message displays)	Reference error message descriptions in diagnostics handbook; see steps 7 thru 10 in table 4-2.
10	Rewind cassette tape by pressing REWIND on 733 ASR or 990 Maintenance Unit and repeat diagnostic load procedures for the RAM04 diagnostic test (part no. 945440) which checks each memory location as defined at the beginning of the test. (See diagnostics handbook.)	No errors	Refer to diagnostics handbook for error message interpretation and see steps 8, 9, 11, 12, and 13.
11	Rewind cassette and install one of the other standalone tests identified in table 2-2 as dictated by the problem report. NOTE A collection of loop programs which may be entered from the programmer panel to continuously read or write to/from selected memory locations is provided in Appendix E.	No errors	See table 4-2. For peripheral failures, see 990 Computer Peripheral Field Maintenance Manual.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures

Step	Abnormal Indication	Probable Cause	Corrective Action
1	POWER LED does not light and cooling fans inoperative when key switch on front panel is set to LOCK or ON position.	Loss of ac power at the power outlet.	Using multimeter, measure ac voltage at outlet. If voltage is normal (115 Vac, 230 Vac, or 100 Vac as marked on the rear of the chassis next to the power cable outlet), proceed to next substep.
		Blown fuse due to temporary overvoltage condition on ac power line.	Disconnect ac power cord from ac outlet. Remove fuse 1F1 (located at rear of chassis) and perform continuity check using ohmmeter. Replace fuse (if infinite resistance is indicated) and apply power to the system again. If fuse continues to blow, proceed to step 2. If fuse was not blown when first checked, proceed to next substep.
		Open circuit condition in ac distribution system.	UNPLUG AC POWER CORD FROM AC OUTLET. Set key switch on front panel of chassis to LOCK or ON position. Remove rear access cover and perform following resistance checks:
		Faulty power cord.	1. Measure resistance between hot prong of power cord and the black lead of the power cord which connects to pin 2 of the fuse holder 1XF1 (should be 0 ohms). If open, replace power cable. If normal, check resistance between neutral prong of power plug and white lead of power cord which connects to pin 5 of the ac line filter 1FL1. If open circuit is indicated, replace power cord.
		Faulty ac microswitch on rear of operator panel; faulty cam on key switch; loose terminal or broken wire between fuse holder and microswitch or between line filter and ac microswitch.	2. Measure dc resistance between fuse holder (pin 1 or 2) and pin 3 of line filter. If 0 ohms, proceed to next measurement. If infinite or high resistance, remove side access cover (across from logic board side of chassis) and check continuity between the common and normally-open terminals on the ac switch 1A4S4 located directly behind the key switch on the front panel. (The two terminals are the leftmost two terminals on the leftmost switch as viewed from the rear of the panel.) If the switch is open, check the switch cam operation to ensure that the microswitch is being actuated. If not, replace front panel assembly. If the cam is functioning properly, replace 1A4S1. If the switch resistance is normal (0 ohms), use ohmmeter to locate break in wiring between the fuse holder 1XF1 and the N.O. terminal of the switch 1A4S1 or between the common terminal of 1A4S1 and pin 3 of the line filter. If resistance between fuse holder terminal and pin 3 of line filter is normal, perform next check.
		Open circuit in line filter.	3. Measure dc resistance between line filter pins 1 and 3 (0 ohms) and between 2 and 5 (0 ohms). Replace filter if either path is open.
		Loose terminal or break in wiring between line filter and terminal strip.	4. Measure dc resistance between pin 1 of line filter and terminal 1 on terminal strip and between pin 2 of line filter and terminal 2 of terminal strip. If either reading indicates open circuit, repair break in wiring or loose terminal.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
2	Fuse continues to blow when replaced.	Shorted winding on one of the blower motors or shorted surge voltage protector.	TURN OFF AC POWER TO CHASSIS. Disconnect 1A2P1 (purple plug on the end of the ac power converter board). Install new fuse and retest system. If fuse does not blow, proceed to next substep. If fuse blows, remove the hot lead of each blower motor from terminal 1 on the terminal strip (end terminal on the right), one motor at a time, and measure the dc resistance of the motor (normally between 20 and 30 ohms). Replace any motor with obvious shorted windings. If all motors test good, measure dc resistance between terminals 1 and 2 of terminal block. If less than 5 ohms, replace surge voltage protector 1C2. If all resistance checks are normal, disconnect hot leads of all blower motors and replace one at a time. After each lead is reconnected, turn on ac power to system. Then check fuse. Repeat for each motor until fuse blows. Replace last motor connected when fuse blows.
		Short circuit condition on ac power converter board (1A2).	TURN OFF AC POWER TO THE CHASSIS. Remove all connector plugs from ac power converter board and measure dc resistance between pins 1 and 2 of J1 (purple jack) using R × 1K scale on ohmmeter. Should be approximately 5K ohms in one direction and a minimum of 100K when the leads are reversed. If abnormal, replace ac power converter board. Then proceed to next substep to ensure that a faulty main power supply or standby power supply board did not result in failure of the converter board.
		Short circuit condition on main power supply board (1A3).	Using R × 1K scale on ohmmeter, measure input resistance to main power supply by measuring resistance between pins 1 and 2 of 1A2P3 (white plug removed from ac converter board). Normal resistance is approximately 4.5K in one direction and 11K ohms in the reverse direction. If lower resistance is measured, replace main power supply board. If normal, measure resistance between pins 3 and 4 of the same plug (1A2P3) using the R × 1K scale. Normal values are approximately 2K in one direction and 20K in the reverse direction. If resistance is much lower than normal values, replace main power supply board. If readings are normal, proceed to the next substep.
		Short circuit condition on input side of standby power supply board 1A6 (if used).	Measure dc resistance between pins 2 and 4 of 1A2P2 (red plug removed from ac power converter board) using R × 1K scale on ohmmeter. Normal reading is approximately 4K and 10K (reverse direction). If short circuit is indicated, replace standby power supply board. If standby option is not used, locate and correct short-circuit condition in wiring harness. If resistance is normal (above values if standby supply is used or infinity if supply is not used), proceed to next substep.
		Leaking filter capacitor 1C1.	Measure dc resistance of capacitor 1C1 using RX100 scale by measuring between pins 1 and 3 or connector plug 1A2P2 (red plug removed from ac power converter board). Normal indication is a near-zero initial reading with a gradual movement of the meter pointer toward the infinity side of the scale. If resistance value is low or if capacitor shows signs of leakage, replace capacitor.
			Reconnect the plugs originally removed from ac power converter board. The plugs are keyed such that the plugs will mate in only one way.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
2	(Continued)	Faulty main power supply board or ac power converter board under full load conditions.	If all static dc resistance tests are normal, swap out main power supply board first. If problem is still present, swap out ac power converter board and ICs if problem continues.
3	POWER LED on front panel fails to light when key switch is set to LOCK or ON position; cooling fans function normally; system inoperative.	Faulty main power supply board 1A3 or low output voltage from ac converter board 1A2.	Remove and replace main power supply board. If problem persists, remove 1A3P1 from main power supply and measure dc voltage between pins 1 and 2 (pin 1 is POSITIVE lead). Set key switch on chassis front panel to OFF position. If less than 130 Vdc, replace ac power converter and/or capacitor 1C1. If problem still persists, proceed to next substep.
		Short circuit on one of the boards in the chassis.	Remove all logic boards from the chassis (as each board is removed, ensure that the board location chart on the top of the computer chassis accurately reflects the boards installed in each slot). Then, install known good 990/4 microcomputer board (or CRU buffer board if problem exists in expansion chassis) in slot 1. If problem is solved, install original boards in remaining slots (one at a time) and retest the system as each board is installed. CAUTION Always turn off power to the chassis when removing and replacing logic boards to avoid damage to the boards due to temporary misalignment of pins. If all original boards are reinstalled (except board in slot 1) and system functions normally, the original board in slot 1 is faulty. If the problem returns as one of the other original boards is installed, the last board installed before reappearance of the power failure is the faulty board and should be replaced. Reinstall all other original boards and retest system.
4	Unable to get programmer panel into halt mode; same symptom appears when programmer panel from 990 Maintenance Unit is substituted for chassis panel. NOTE If symptom appears only with chassis-mounted panel, remove and replace panel.	Custom ROMS installed in bank 3 of 1K ROM memory on 990/4 microcomputer board.	Replace custom ROMs in bank 3 (or banks 2 and 3) with one of the standard ROM loader configurations as shown in figure 1-11. Move custom ROMs to another location in the ROM memory and ensure that address change is reflected by customer's software.
		Faulty 1K ROM memory section or faulty load generation logic on 990/4 microcomputer board.	Remove and replace 990/4 microcomputer board. Ensure that all jumper options, ROM loaders and custom ROMs are properly installed on replacement board.
		1K ROM memory starting address set up for lower 1K of memory address space (jumper between E19 and E20) on 990/4 microcomputer board.	Carefully evaluate memory system. If the panel software is to be used, the jumper between E19 and E20 must be removed since the last two addresses in memory ($FFFC_{16}$ and $FFFE_{16}$) must contain ROM WP and PC values for the panel software program which is also located in bank 3 of the ROM memory.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures

Step	Abnormal Indication	Probable Cause	Corrective Action
5	System fails to come up in RUN mode when power is applied to the chassis.	Loss of power up clear signal from main power supply board or faulty driver stage on 990/4 microcomputer board.	Remove and replace 990/4 microcomputer board after transferring all custom ROMs onto replacement board and setting up the jumper options correctly (see Section I). If problem persists, replace main power supply board. Reinstall original 990/4 board if problem was narrowed down to main power supply board. NOTE Problem may also be TMS 9900 on 990/4 microcomputer board. If replacement 990/4 board is not available and problem is not on main power supply board, replace TMS 9900 on 990/4 board.
6	Unable to load diagnostics from Maintenance Unit; FAULT LED lights when LOAD is initiated.	Self-test failure due to faulty self-test ROMs. memory or microprocessor error.	Remove and inspect all jumper options on 990/4 microcomputer board and all memory boards in the chassis. Ensure that no two memory sections occupy the same address space. If all jumper options are correctly installed, replace the loader ROMs in the 1K memory section on the 990/4 microcomputer board (see figure 1-11). If problem persists, replace 990/4 microcomputer board (ensure that replacement board is properly configured and that all custom ROMs from faulty board have been transferred to replacement board). If problem persists, proceed to next substep.
		Loss of memory voltage(s).	If standby power supply option is not installed, ensure that standby jumper plug is installed on 1A3J3. Using multimeter, observe the following memory voltages at any connector slot in backplane (use extender board if available): • P2-71: -5 MEM • P2-73: +5 MEM • P2-75: +12 MEM If standby supply option is not used, replace main power supply board if any of these voltages are abnormal. If standby supply is used, replace standby supply if the voltages are abnormal. (-5 MEM may also be due to failure on main power supply board.)
7	Failure of one or more instructions when executing AU04 diagnostic.	Faulty TMS 9900 or support functions on the 990/4 microcomputer board.	Replace 990/4 microcomputer board. Ensure that all jumper options, loader ROMs and custom ROMs are correctly installed on new board. NOTE If spare board is not available, replace TMS 9900 and retest suspect board.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
8	ROM04 diagnostic printout indicates single bit error at one or more memory location(s) in 4K RAM address space on 990/4 microcomputer board. NOTE See Appendix E for loop program which may be entered from the programmer panel to loop on a selected address or band of addresses.	Faulty TMS 4051 memory chip.	Remove and replace TMS 4051 memory chip corresponding to bit position as follows: BIT NO. — CHIP LOCATION 0 — U44 1 — U45 2 — U46 3 — U47 4 — U48 5 — U49 6 — U50 7 — U51 8 — U66 9 — U67 10 — U68 11 — U69 12 — U70 13 — U71 14 — U72 15 — U73 Parity — U74 If problem persists after replacement of memory chip, remove and replace 990/4 microcomputer board after carefully implementing all jumper options and loader options on the replacement board (see Section I for option descriptions).
9	Memory failure on 4K RAM address space on 990/4 microcomputer board. Board replaced and problem persists.	One of the expansion memory boards is operating with the same starting address due to an improperly selected starting address or faulty address decode on the board.	Check the starting address associated with each memory expansion board or EPROM memory module in the chassis in accordance with the information provided in figures 1-12 and 1-13. If starting address for each board is properly setup, replace each memory board and repeat diagnostic. Last board replaced when diagnostic board executes properly is the faulty board. Reinstall the other board(s) and repeat the test to ensure that only one problem exists in the system.
		Starting address of 4K RAM memory improperly jumpered.	Recheck jumper options on 990/4 microcomputer board (see figures 1-9 and 1-10).
10	Real time clock interrupt error.	Interrupt jumper between E9 and E10 or faulty circuit on 990/4 microcomputer board.	Check for jumper between E9 and E10 on 990/4 microcomputer board. If present, replace board (after installing all options and ROMs to replacement board. If problem persists, proceed to next substep.
		Loss of 120 Hz pulses from power supply.	Remove and replace main power supply board and repeat test. If problem persists, replace ac power converter board. If problem persists, proceed to next substep. NOTE Faulty subassembly is the last unit replaced before normal test results are obtained. Reinstall other subassemblies and repeat test to ensure that only one faulty subassembly exists on the system.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
10	(Continued)	Software problem.	See 990 Assembly Language Programmer's Guide concerning use of CKOF instructions.
11	Low order memory banks on 990/4 memory expansion board inoperative, high order banks normal.	Improperly set starting address switches on DIP switch U37.	Refer to figure 1-12 and set up switch positions S2 thru S4 to correspond to expansion memory starting address. In conventional system, the starting address is set at 4K (2000_{16}) with S2 and S3 of U37 OFF and S4 ON. If properly set, replace board.
12	High order memory address space on 990/4 memory expansion board inoperative, low order banks functioning normally.	Memory size jumpers improperly installed.	Set up maximum memory size jumpers (terminals E1 to E6) in accordance with figure 1-12 to reflect the amount of memory implemented on the board. If properly set, replace memory expansion board.
13	Single bit failure in one or more addresses in the 990/4 memory expansion board's address space.	Faulty TMS 4050 memory chip.	Remove and replace TMS 4050 memory chip in memory bank corresponding to faulty address at bit position corresponding to faulty data bit (see figure 1-2). If problem persists, replace TMS 4050 ICs in same column in the remaining memory banks. If problem still persists, remove and replace memory expansion board.
14	Unexpected write protect error on memory expansion board.	Faulty write protect circuit on expansion board.	Replace 990/4 memory expansion board and set up starting address and size jumpers as shown in figure 1-12.
15	Memory failure on address space reserved for EPROM memory module.	Jumpers not properly installed on board or starting address for EPROM board not properly set, faulty EPROM board.	Refer to figure 1-13 and ensure that all board options are properly installed. If so, replace the board. CAUTION All EPROM chips from the faulty board must be transferred to the exact same socket locations on the replacement board. These chips contain custom software programs which will not function if any of the chips are installed out of their original pattern.
16	One peripheral device within main chassis is inoperative; all other peripherals function normally.	Peripheral's interface board installed in wrong slot (see figure 1-15 for standard configuration recognized by software). Interrupt not wired properly on backpanel board. Improperly seated interface board or loose cable connector. Faulty interface board or jumper options improperly installed.	Move interface board to correct location. If properly located, proceed to next substep. Remove first five logic boards in chassis and ensure that jumper is installed correctly (see figure 1-17). If so, replace boards and proceed to next substep. Check interface board and associated interface cable connectors for snug fit. If device is 733 ASR, 733 KSR or line printer, see figure 1-22 to verify proper jumper connections. At this point, refer to the 990 Computer Peripherals Field Maintenance Manual for additional fault isolation procedures.

Table 4-2. 990/4 Microcomputer System Fault Isolation Procedures

Step	Abnormal Indication	Probable Cause	Corrective Action
17	All peripherals implemented within one expansion chassis are inoperative; peripherals implemented in other expansion chassis function properly.	If POWER LED on chassis is lit and fans are functioning properly, the CRU buffer board is most likely at fault. NOTE If POWER LED and blower motors in expansion chassis are inoperative, see steps 1 and 2 at the beginning of this procedure.	Remove CRU buffer board from chassis and check to see that the jumper plug (P4) on the board is inserted in the slot corresponding to the correct chassis number as follows: CRU EXPANDER PORT / CHASSIS NO. P3 1 P4 2 P5 3 P6 4 P7 5 P8 6 P9 7
		Faulty CRU expander board in main chassis or faulty interface cable between CRU expander board in main chassis and CRU buffer board in expansion chassis.	If the jumper plug is properly installed, replace the CRU buffer board and set up the jumper plug (as described above) on the replacement board. If the problem persists, replace the interface cable between the CRU expander board in the main chassis and the CRU board in the expansion chassis and/or CRU expansion board in the main chassis. If problem persists, preceed to next substep.
		Interrupt jumpers not properly installed on expansion chassis backpanel.	Refer to figures 1-16 and 1-17. Check interrupt jumpers in chassis backpanel board to ensure that the interrupt assignments listed on the chassis map (top of chassis) are correctly implemented.
18	One or more function keys on chassis-mounted programmer panel inoperative; programmer panel on Maintenance Unit functions properly.	Defective switch block on programmer panel.	Remove and replace chassis-mounted panel in accordance with the instructions in Section III.
19	One or more function keys inoperative on chassis-mounted programmer panel; same problem exists with programmer panel on maintenance unit.	Faulty panel software ROM on 990/4 microcomputer board.	Install new ROM loader ICs in the 1K ROM memory in accordance with the information provided in figure 1-11. If problem persists, replace 990/4 microcomputer board. NOTE Ensure that all jumper options on the replacement board match the options installed on the faulty board and that all custom ROMs in the 1K ROM memory have been transferred to the replacement board.

SECTION V

TROUBLESHOOTING DIAGRAMS

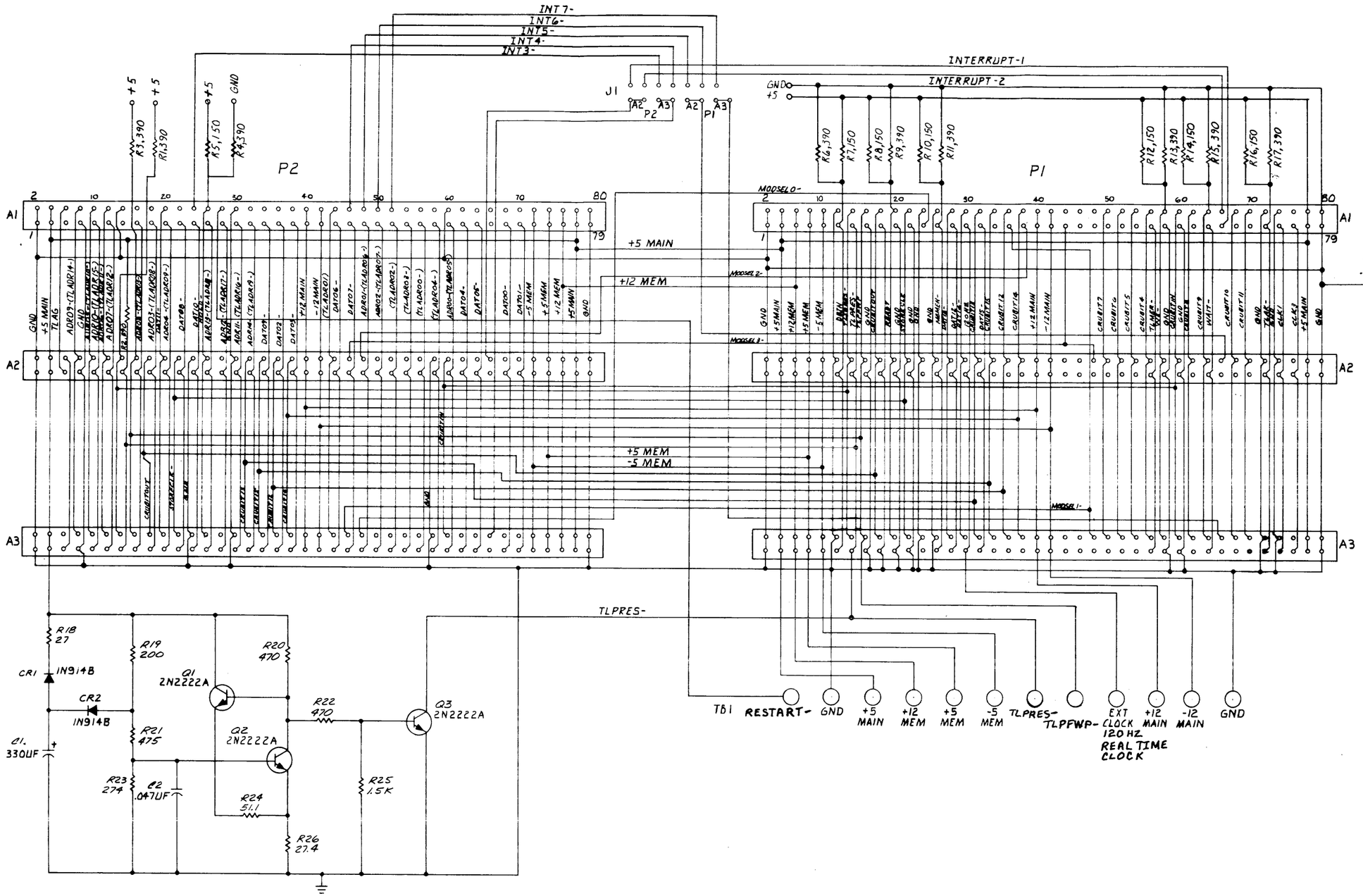
5.1 GENERAL

This section contains a collection of chassis wiring diagrams, backpanel schematics and logic board block diagrams (complete with interface pin assignments) useful in performing field-level maintenance. An index to the drawings in this section is provided in table 5-1.

NOTE

Logic diagrams, IC schematics and power supply schematic diagrams are available in the *990 Computer Family Maintenance Drawings Manual.*

Table 5-1. Diagram Index



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944918

Figure 5-1. OEM Chassis Backpanel Schematic

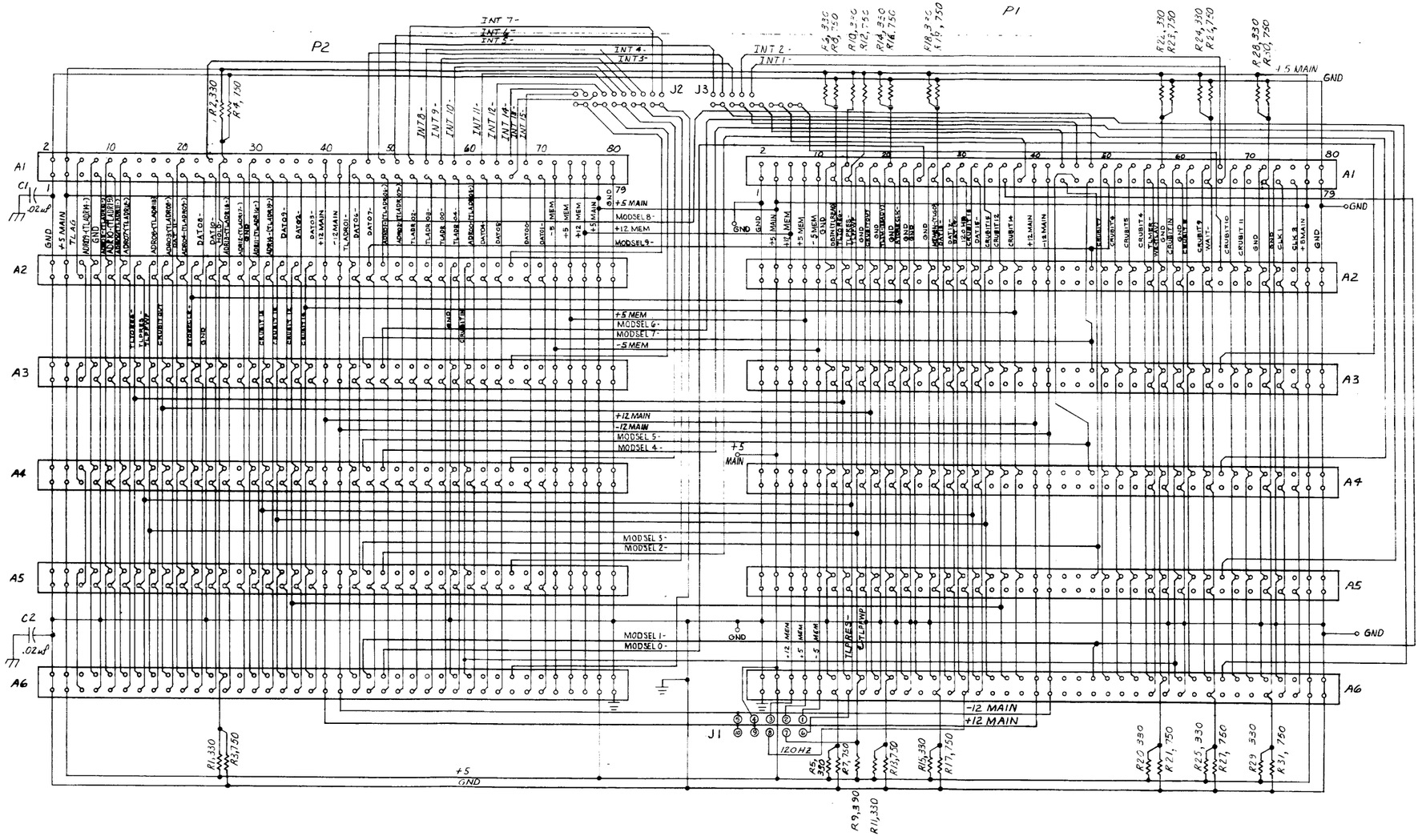


Figure 5-2. 6-slot Chassis Backpanel Schematic

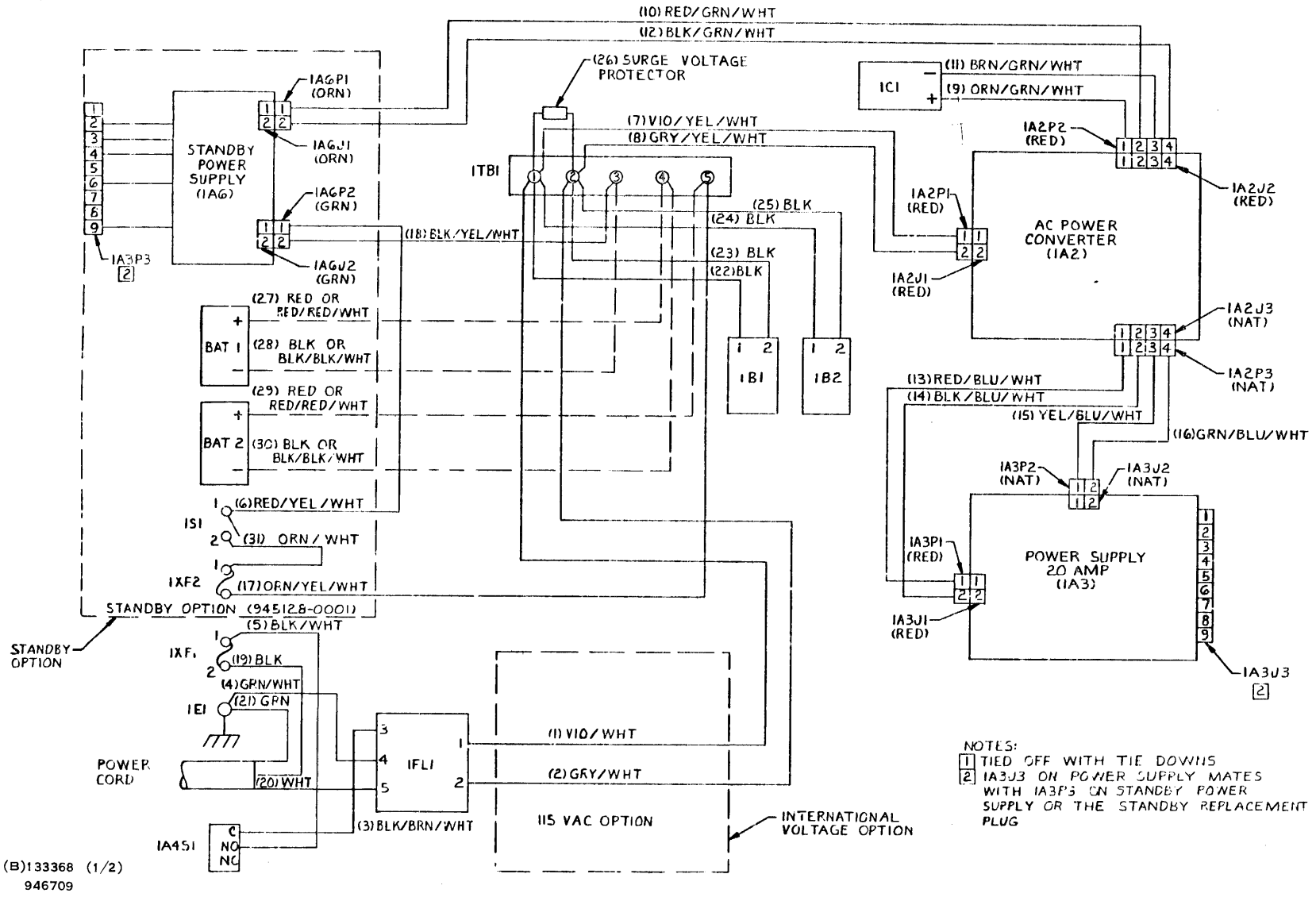
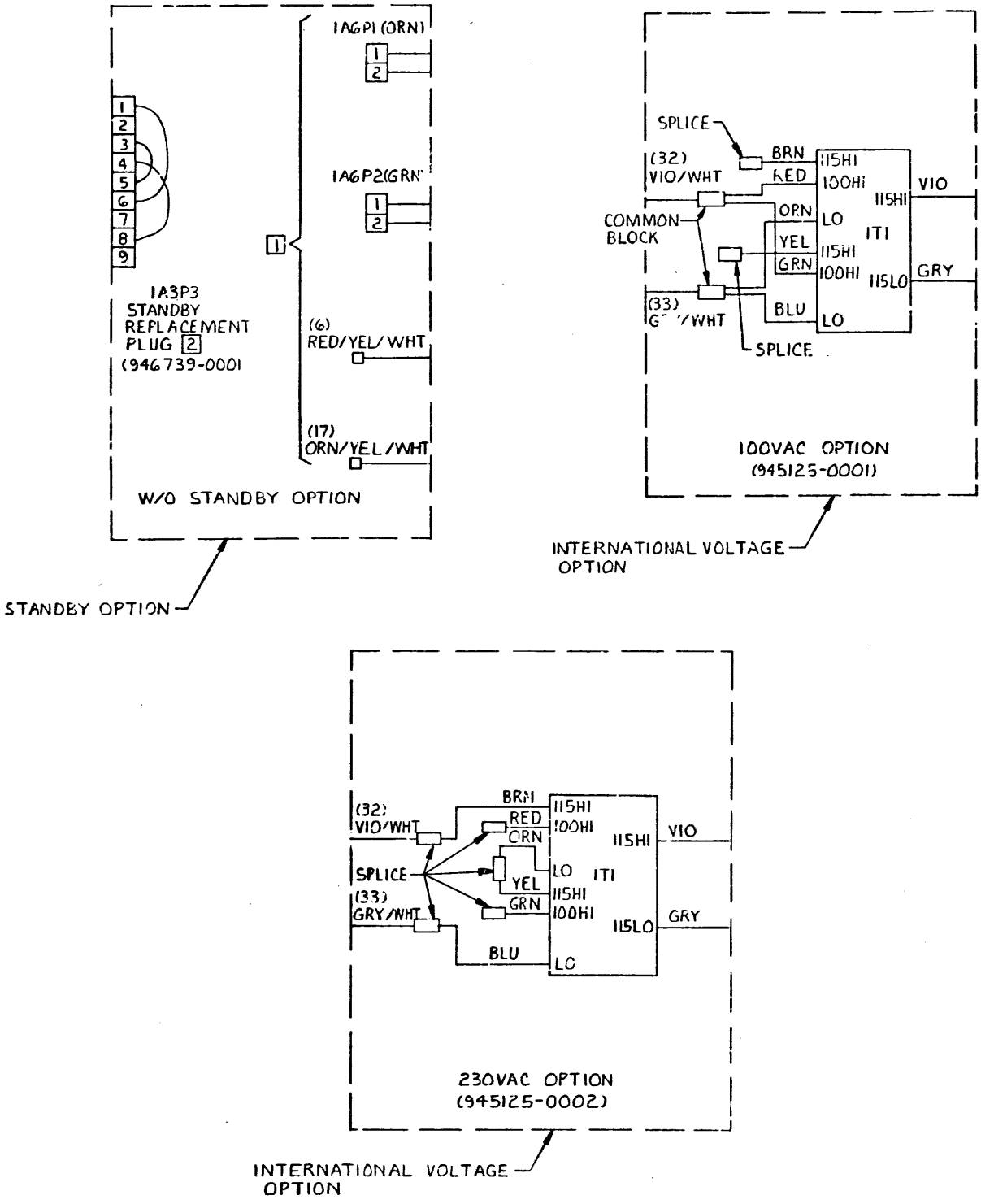


Figure 5-3. 6-slot Chassis Wiring Diagram (Sheet 1 of 2)



(B)133368 (2/2)
946709

Figure 5-3. 6-slot Chassis Wiring Diagram (Sheet 2 of 2)

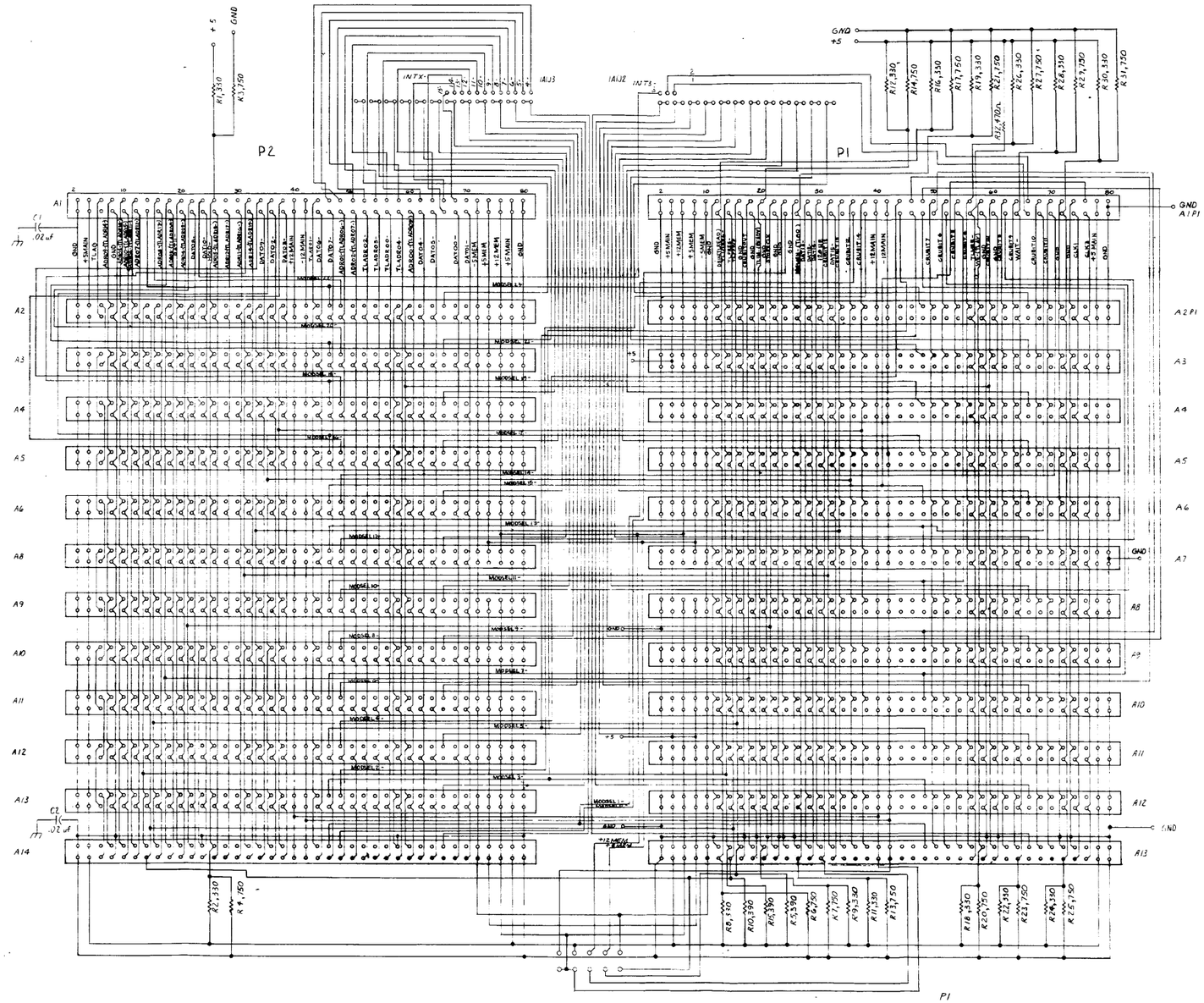


Figure 5-4. 13-slot Chassis Backpanel Schematic

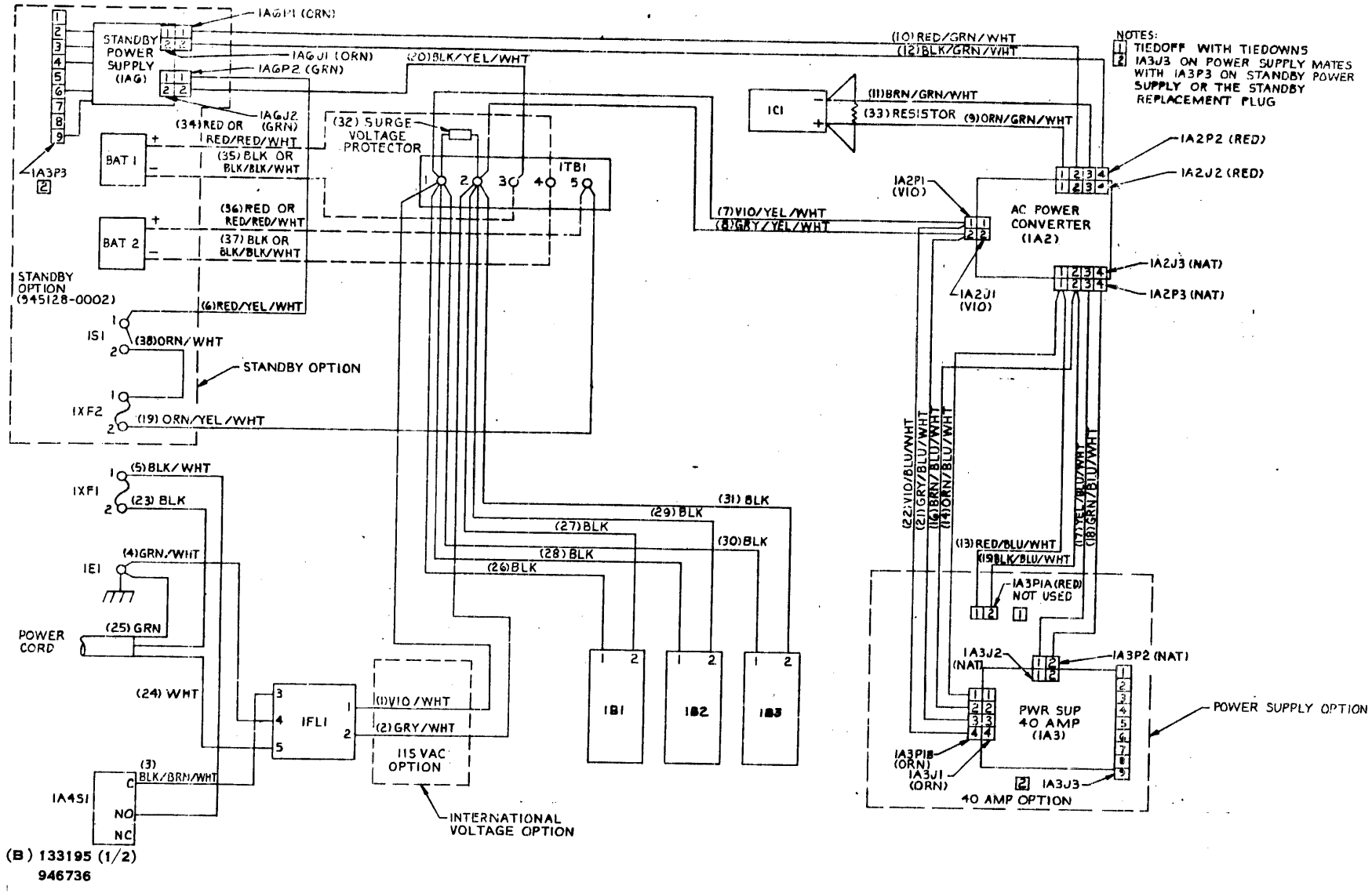
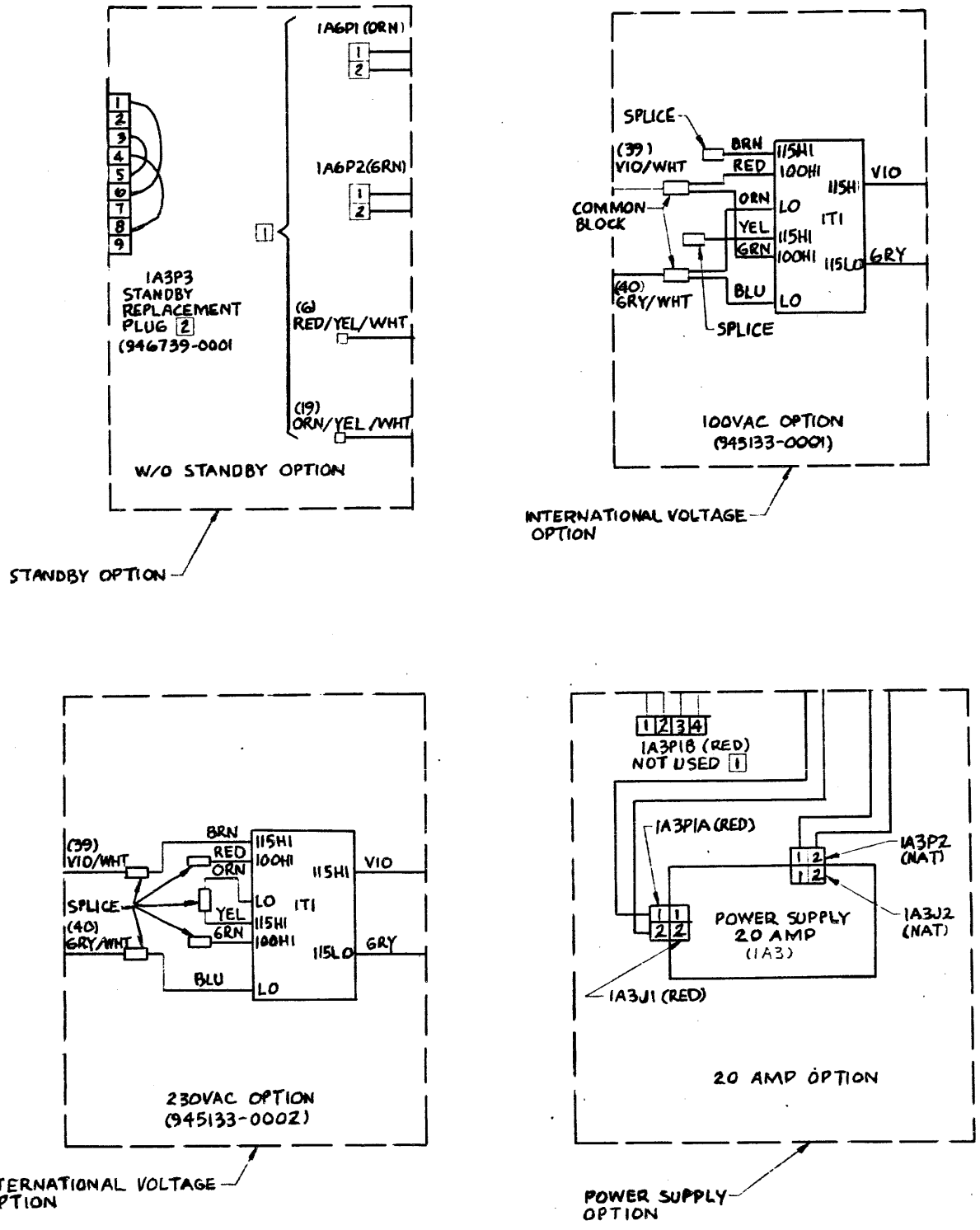


Figure 5-5. 13-slot Chassis Wiring Diagram (Sheet 1 of 2)



(B) 133195 (2/2)
946736

Figure 5-5. 13-slot Chassis Wiring Diagram (Sheet 2 of 2)

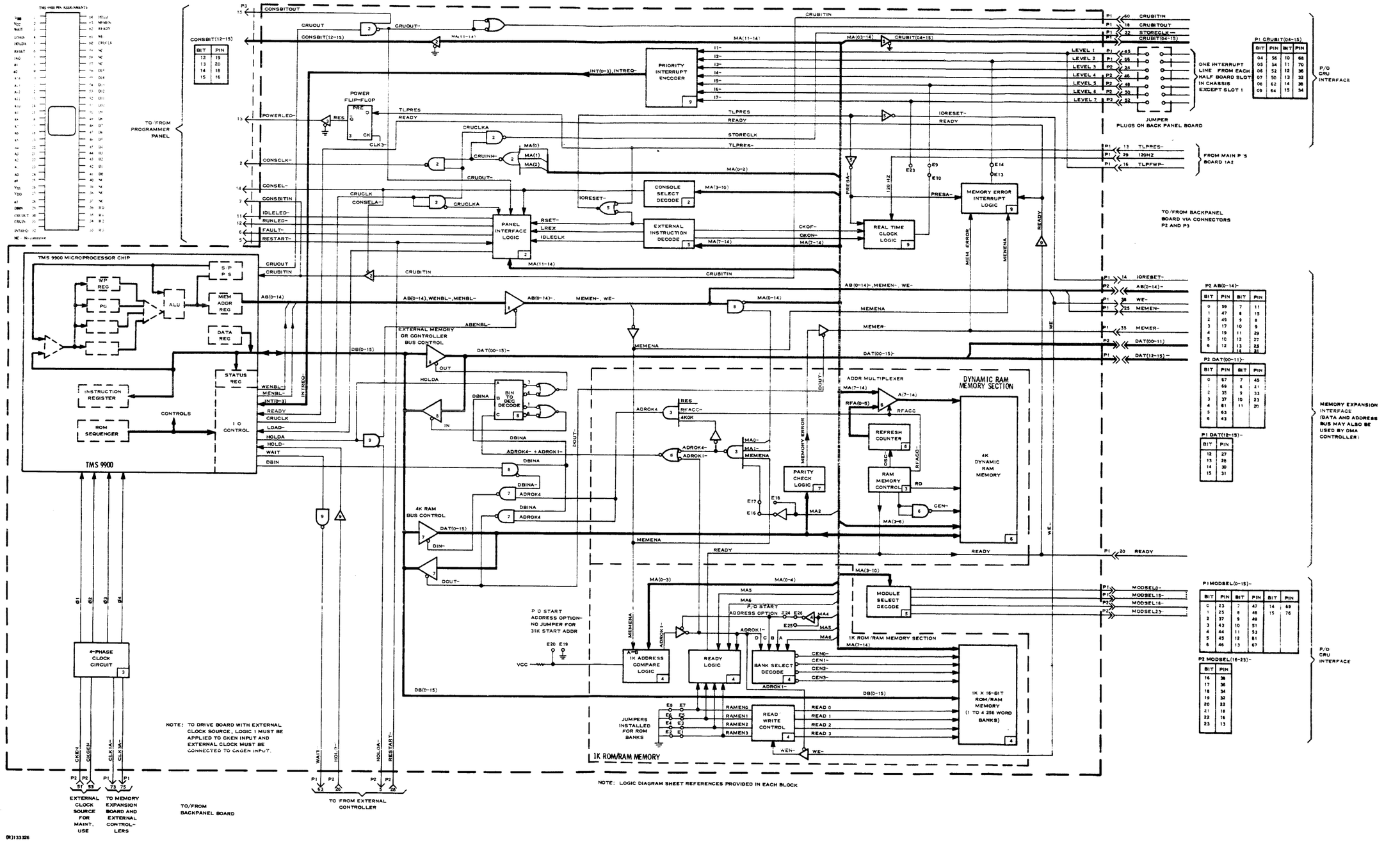


Figure 5-6. 990/4 Microcomputer Board Block Diagram

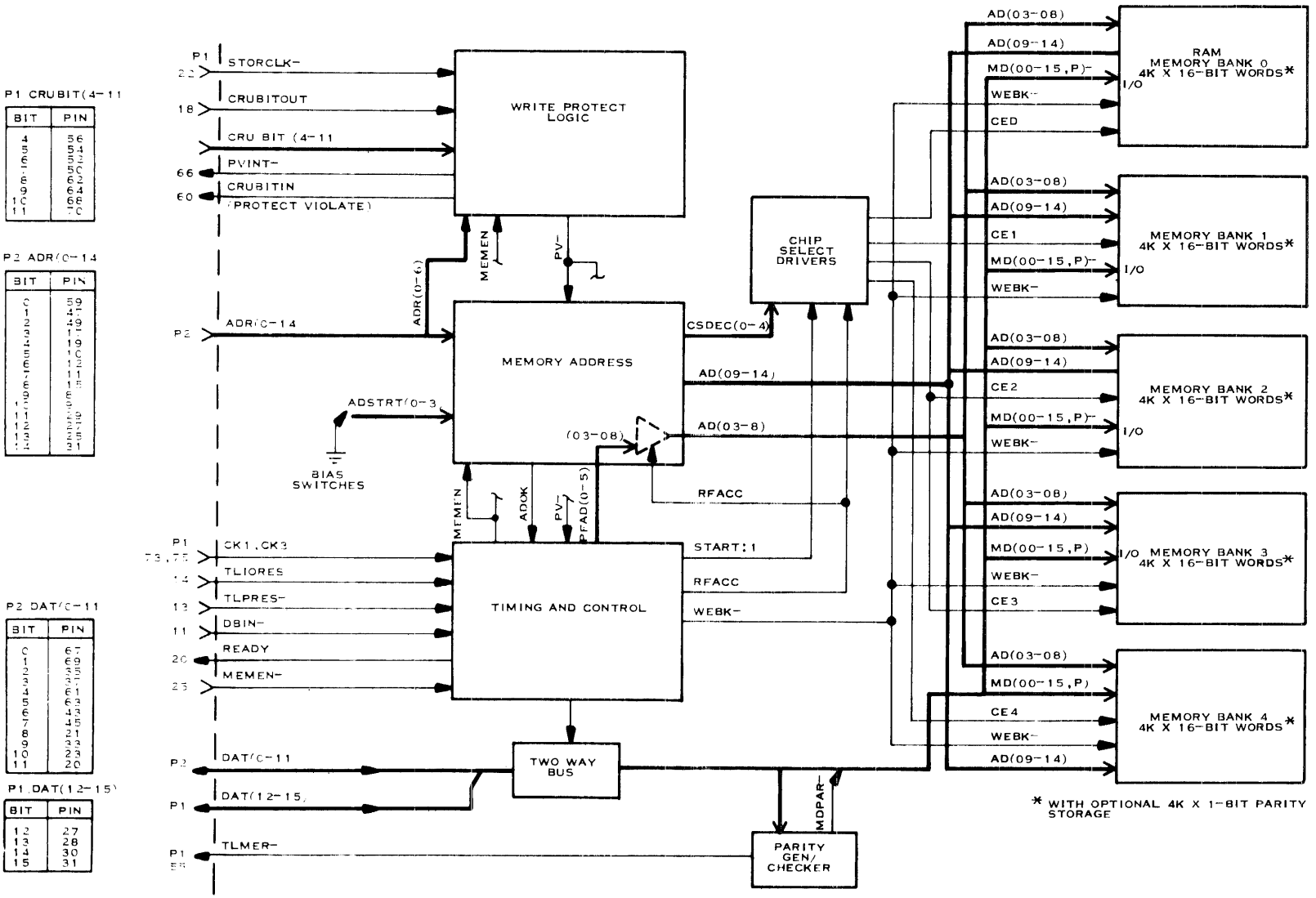


Figure 5-7. 990/4 Memory Expansion Board Block Diagram

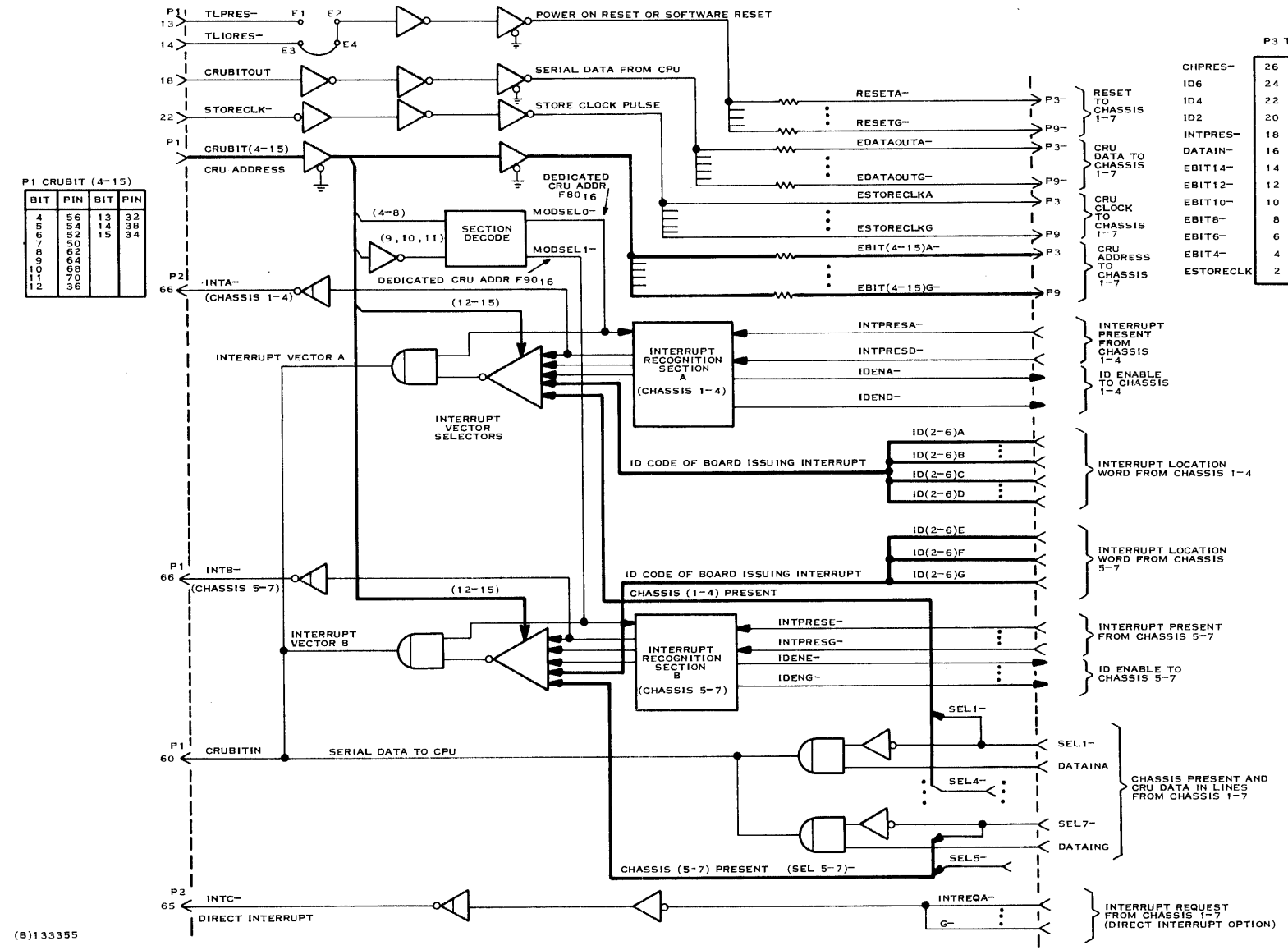
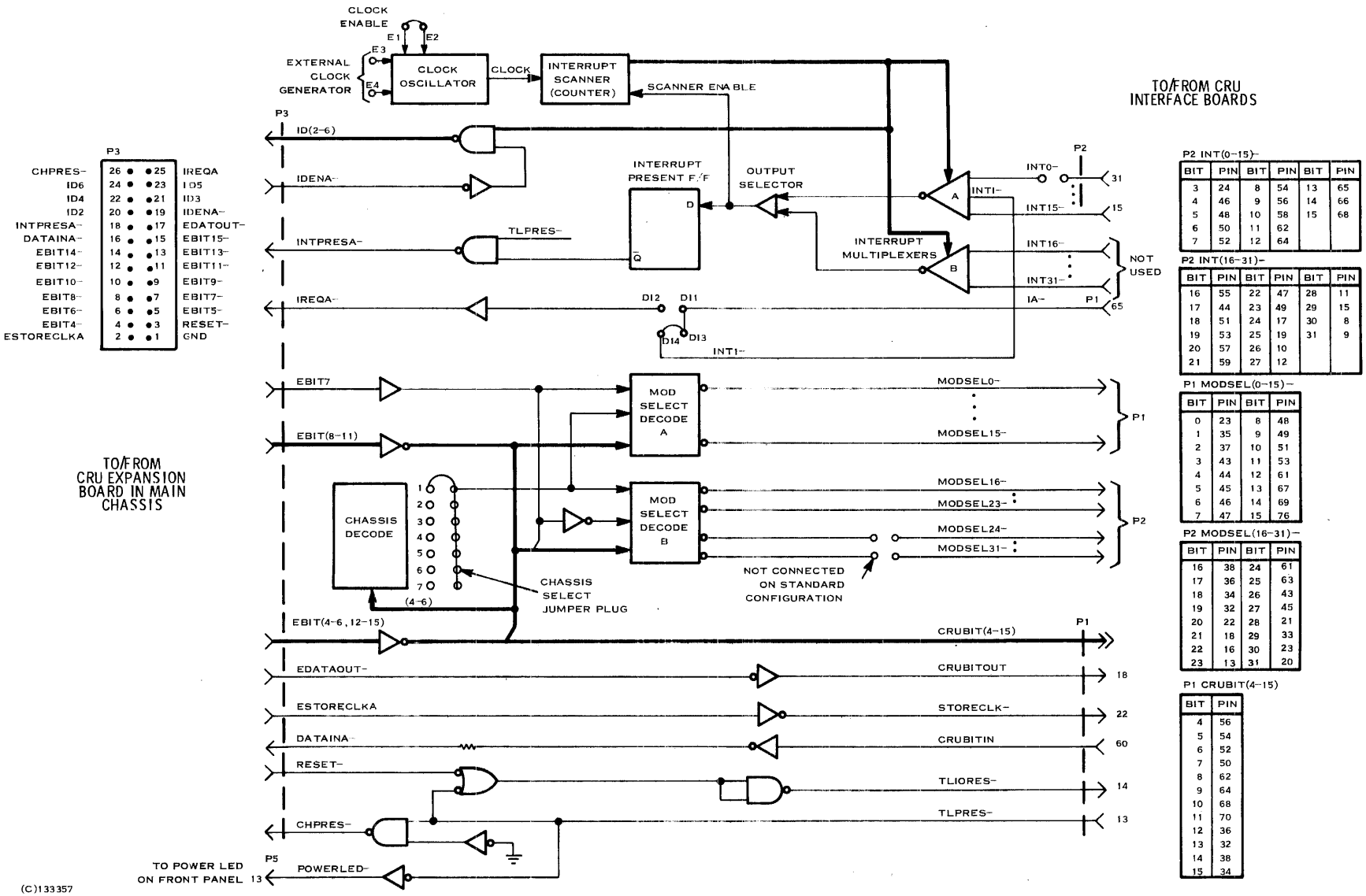


Figure 5-8. CRU Expander Board Block Diagram



P2 INT(0-15)-

BIT	PIN	BIT	PIN	BIT	PIN
3	24	8	54	13	65
4	46	9	56	14	66
5	48	10	58	15	68
6	50	11	62		
7	52	12	64		

P2 INT(16-31)-

BIT	PIN	BIT	PIN	BIT	PIN
16	55	22	47	28	11
17	44	23	49	29	15
18	51	24	17	30	8
19	53	25	19	31	9
20	57	26	10		
21	59	27	12		

P1 MODSEL(0-15)-

BIT	PIN	BIT	PIN
0	23	8	48
1	35	9	49
2	37	10	51
3	43	11	53
4	44	12	61
5	45	13	67
6	46	14	69
7	47	15	76

P2 MODSEL(16-31)-

BIT	PIN	BIT	PIN
16	38	24	61
17	36	25	63
18	34	26	43
19	32	27	45
20	22	28	21
21	18	29	33
22	16	30	23
23	13	31	20

P1 CRUBIT(4-15)

BIT	PIN
4	56
5	54
6	52
7	50
8	62
9	64
10	68
11	70
12	36
13	32
14	38
15	34

Figure 5-9. CRU Buffer Board Block Diagram

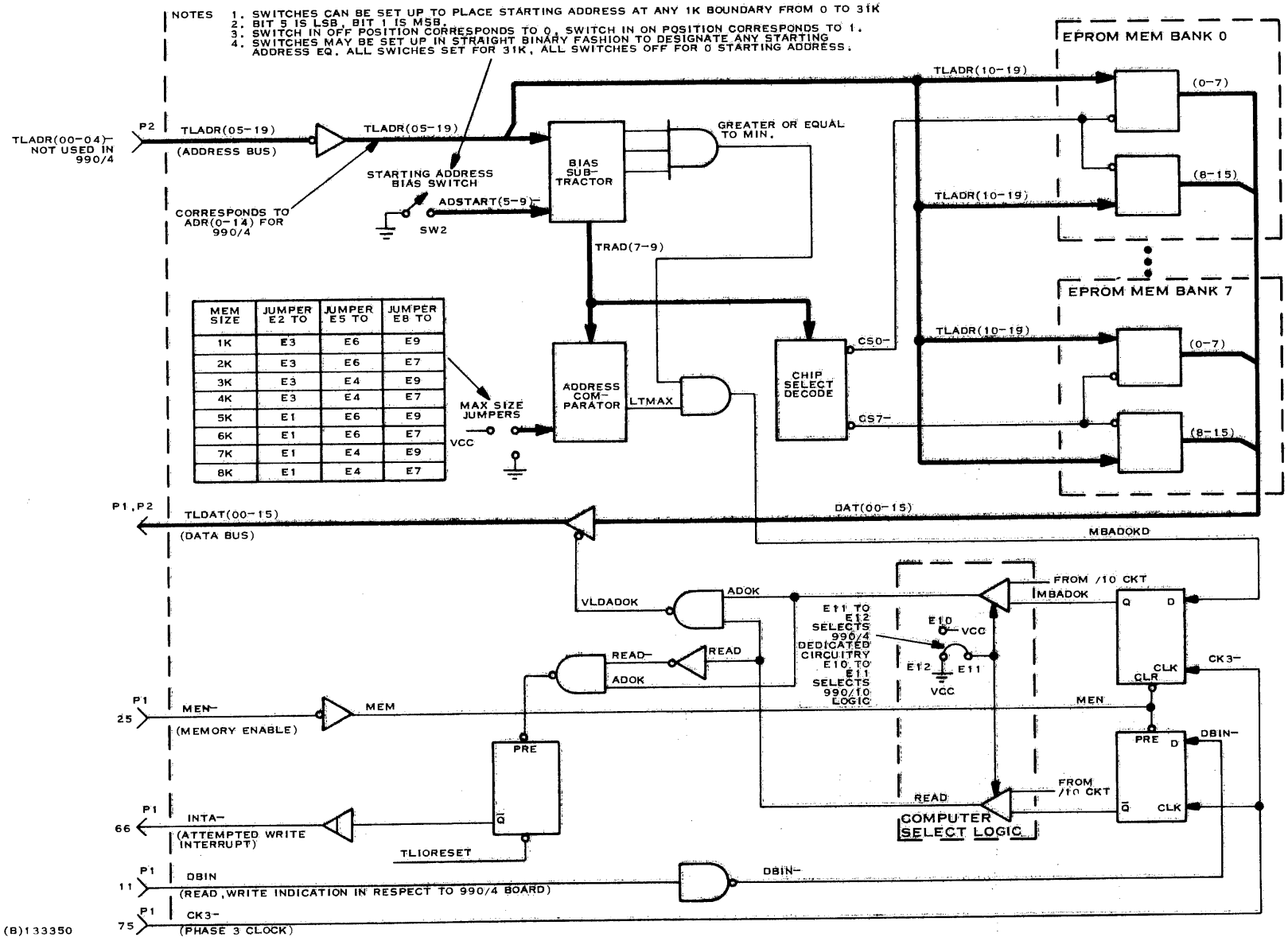


Figure 5-10. EPROM Memory Module Block Diagram

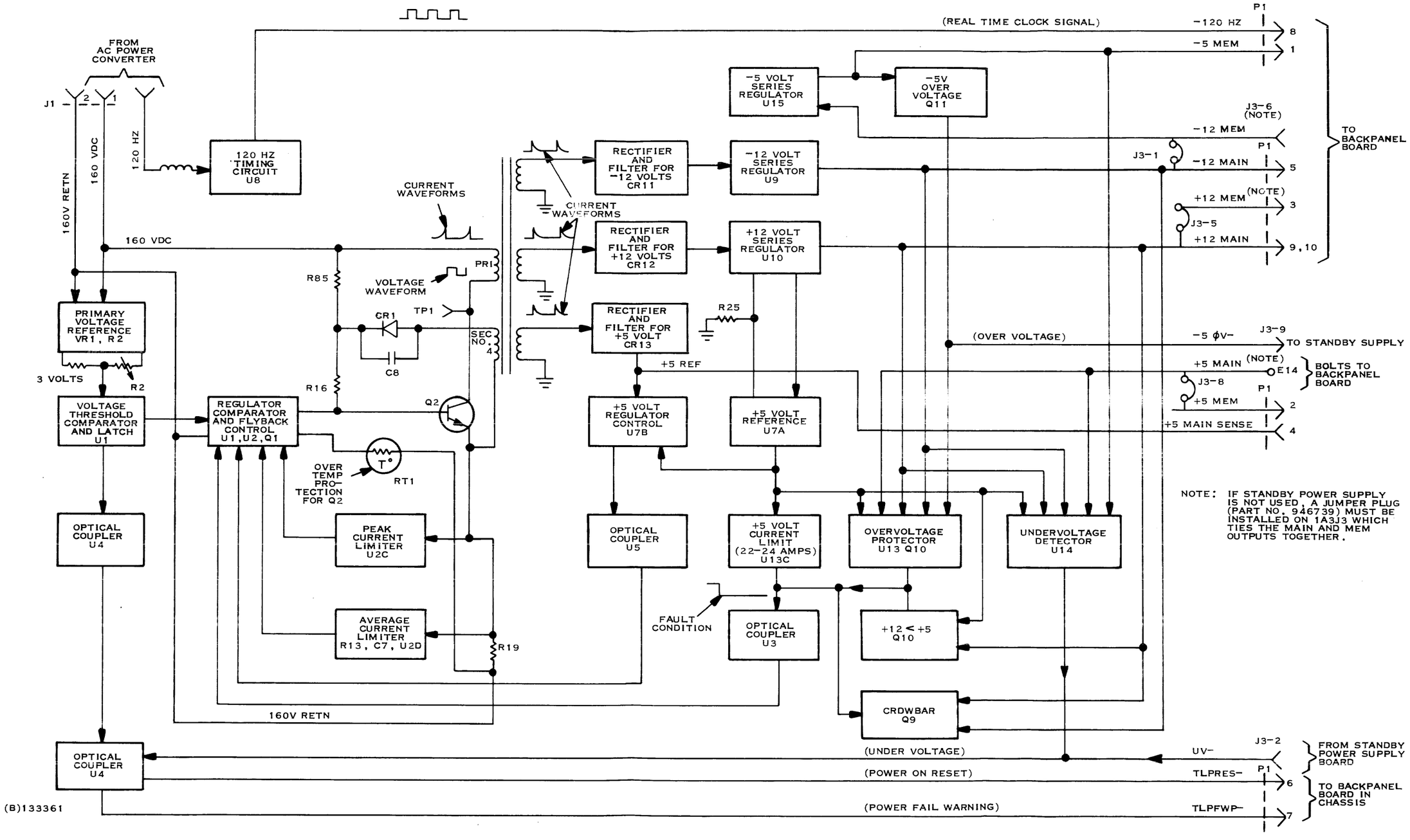


Figure 5-11. Main Power Supply Board Block Diagram

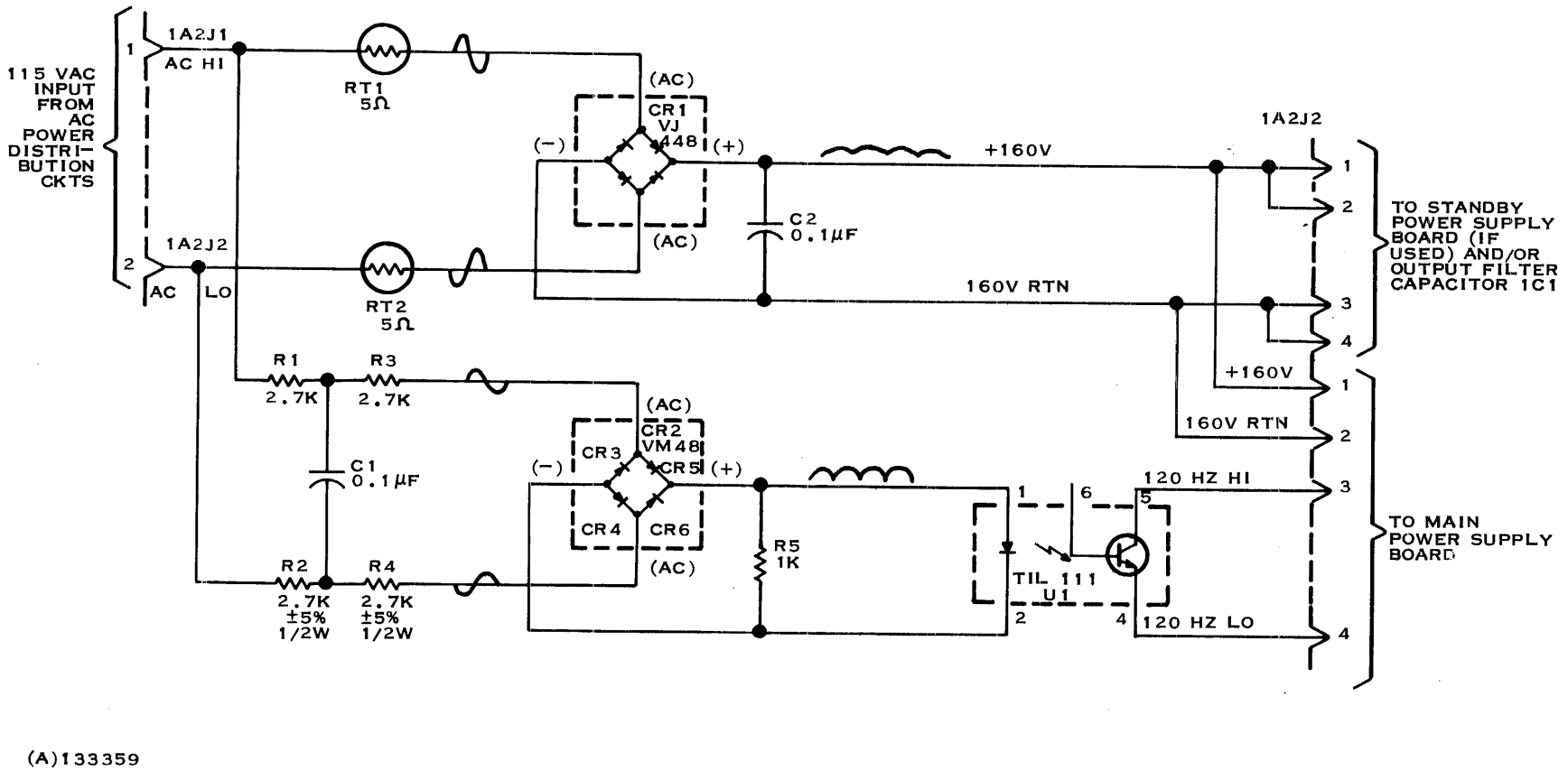


Figure 5-12. Ac Power Converter Board Schematic Diagram

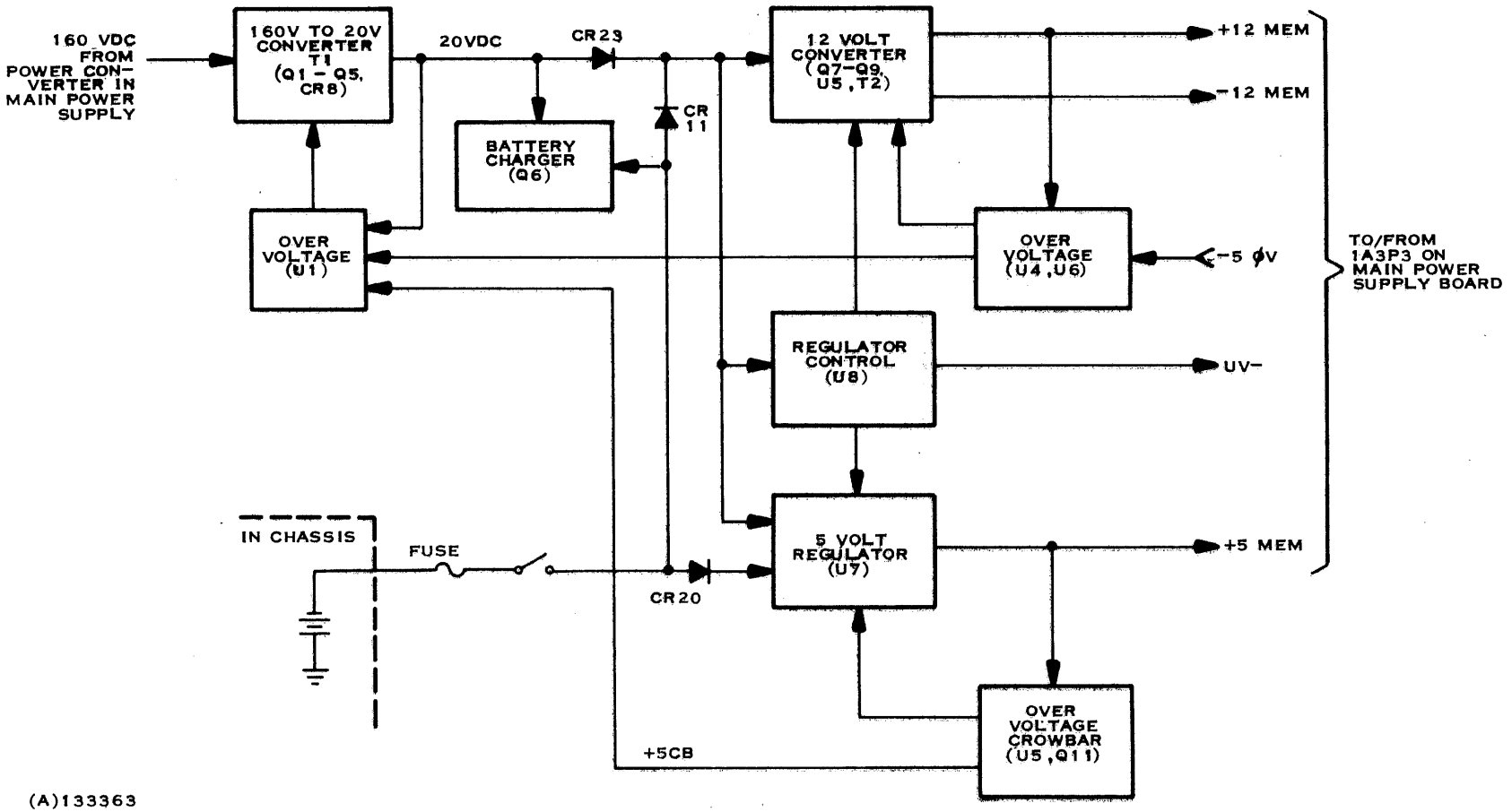


Figure 5-13. Standby Power Supply Board Block Diagram

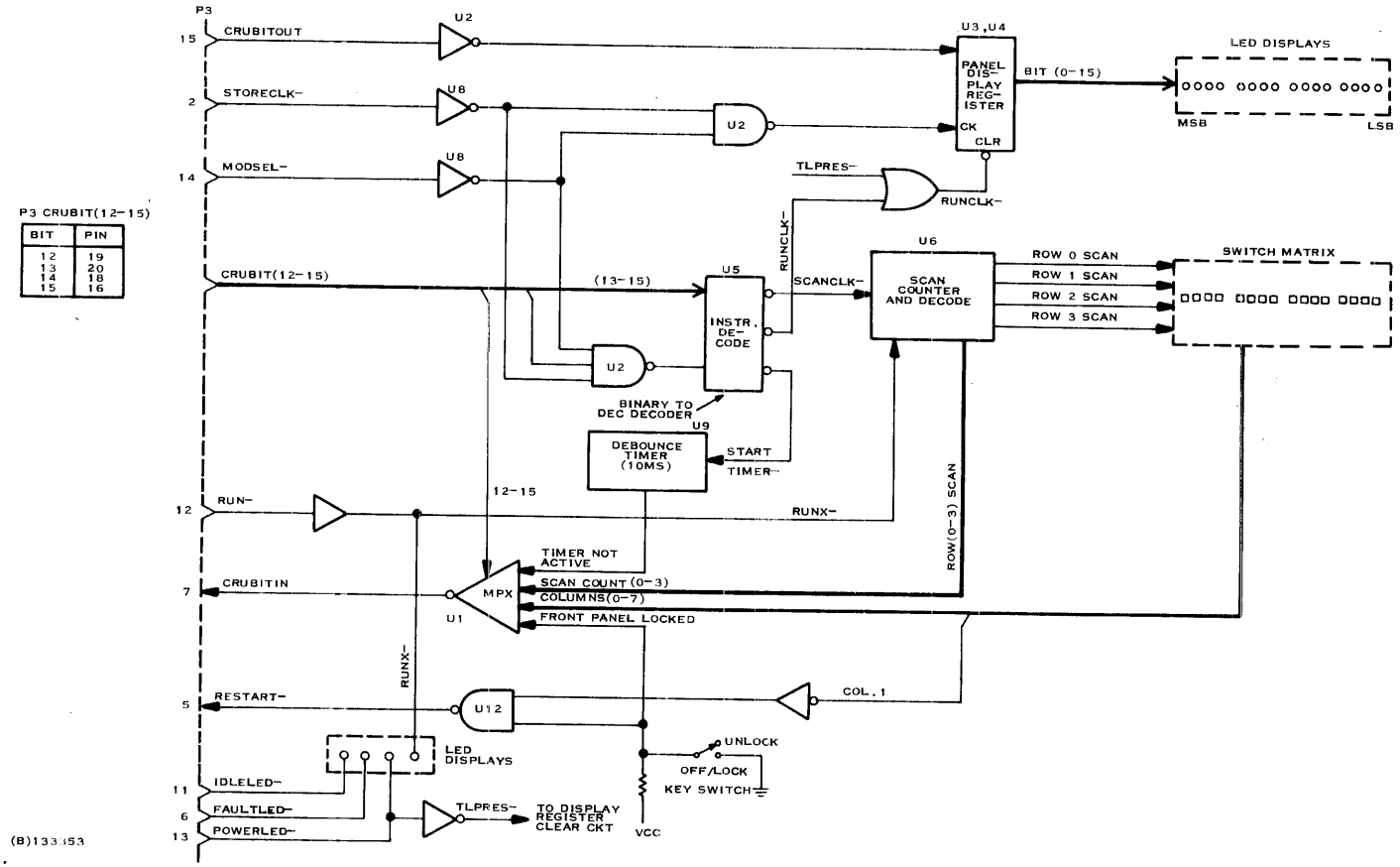


Figure 5-14. Programmer Panel Block Diagram

SECTION VI

PACKING AND SHIPPING

6.1 GENERAL

This section provides instructions for unpacking new units and packing faulty assemblies for reshipment to the factory for repair. In most cases, the subassembly will consist of a printed circuit card or cable and will be packed using the packing materials from the replacement subassembly. The procedures for repacking the subassemblies are provided in the following paragraphs.

6.2 UNPACKING/PACKING (6- AND 13-SLOT CHASSIS)

The computer is shipped in a corrugated cardboard container together with the circuit boards and interconnecting cables required to install the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. Following preliminary inspection, perform the following steps to remove the computer from its container and ready it for operation. Figure 6-1 illustrates the required steps.

NOTE

Save shipping carton and all packing materials for use in reshipment of the unit.

1. Position container so that the address label is right-side up.

2. Open top of container and remove cushioning material from corners.

NOTE

If the computer has the table top enclosure (6-slot chassis only) no foam block is required to secure circuit boards in chassis.

3. Remove cardboard inner sleeve and foam block (rackmount configurations) from shipping container.

WARNING

Use proper lifting techniques to avoid backstrain when lifting computer chassis.

4. Remove computer and attached shipping pallet from container. When lifting assembly, lift from under the assembly to avoid undue strain on the chassis assembly.

CAUTION

To prevent the mounting screws on the underside of the shipping pallet from scratching table surface, place a shielding material (the packing sleeve removed in step 3 makes an excellent shield) on the table before setting the assembly on the table.

5. Place the removed assembly on a convenient, protected work surface.

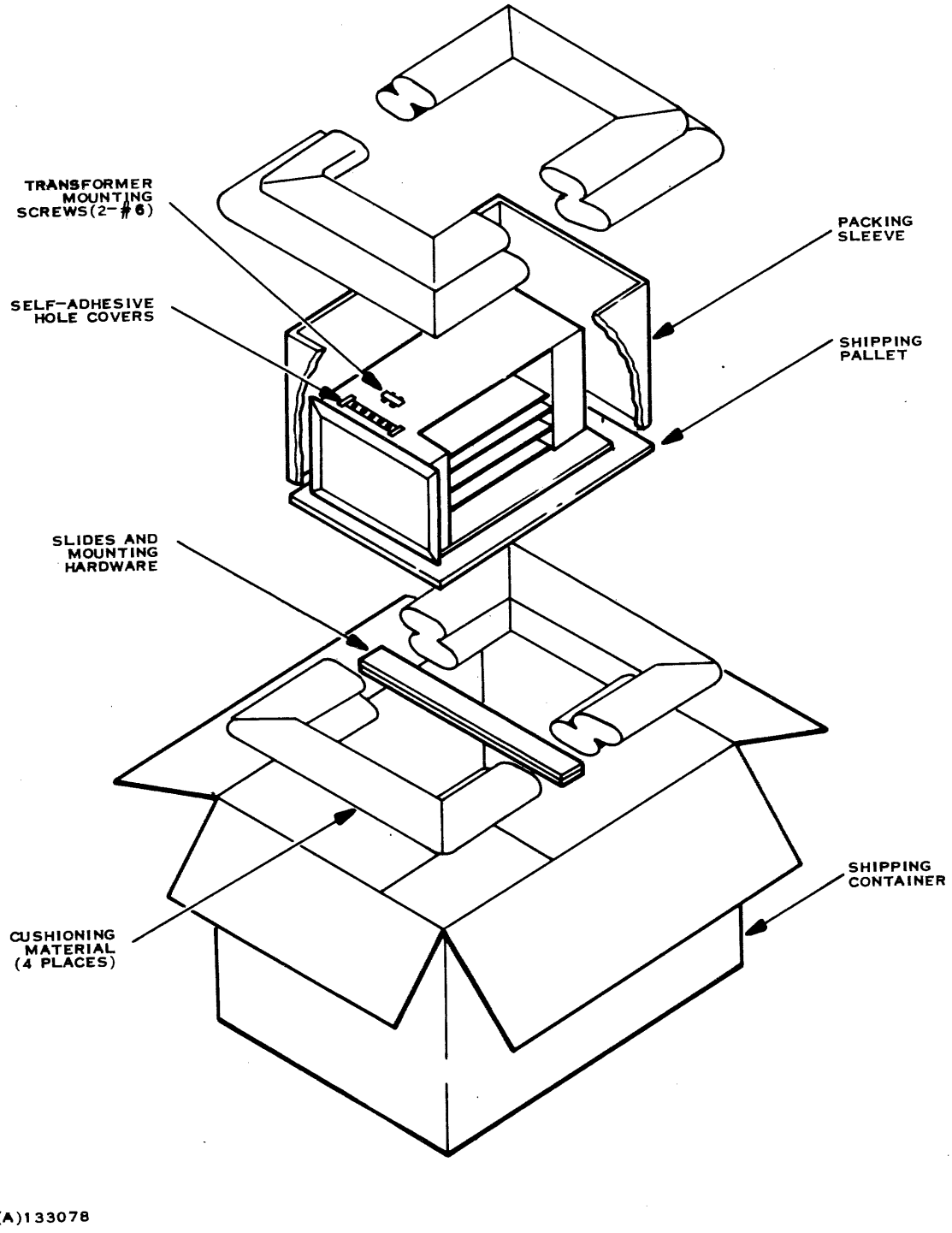


Figure 6-1. Computer Shipping Packaging

NOTE

For rackmount configurations, the slides are packed in the bottom of the shipping container.

6. Remove the rackmount slides (if present) and the interface cables from the bottom of the shipping container.

CAUTION

In the following steps, do not allow the unit to overhang the work surface so far that it will fall off the surface.

7. Position the computer and shipping pallet assembly so that the front edge of the assembly overhangs the edge of the work surface to reveal two (2) #10 mounting screws that secure computer to shipping pallet. See figure 6-2 for location of all mounting screws.

8. Use a straight blade screwdriver to remove the two screws and their associated washers and lock washers. Save the screws and washers for reshipment.

9. Reposition the computer and shipping pallet assembly so that the rear edge of the assembly overhangs the edge of the work surface to reveal three (3) #10 mounting screws that secure computer to shipping pallet.

10. Remove the three screws, washers and lockwashers and save for reshipment.

NOTE

If the computer was ordered for overseas operation, two (2) additional mounting screws are visible on the underside of the shipping pallet. If these screws are not included on the unit being installed, skip step 11.

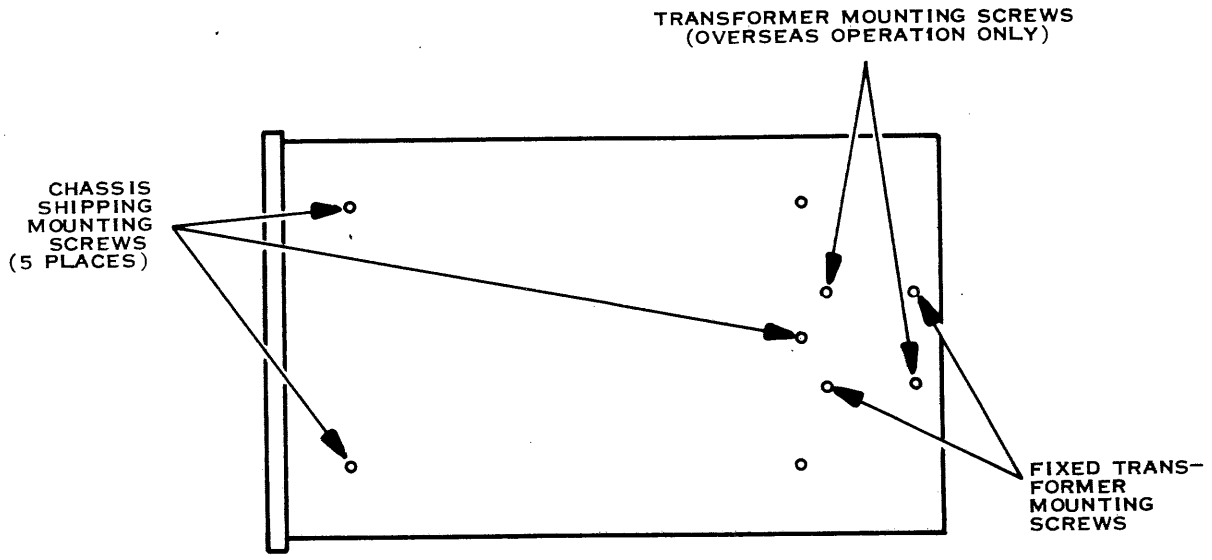
11. Remove two (2) #6 transformer mounting screws and their associated washers and lockwashers and save for reshipment.

12. Lift computer chassis from shipping pallet and place it on the work surface such that the rear of the unit overhangs the work surface to reveal the holes for the removed mounting screws.

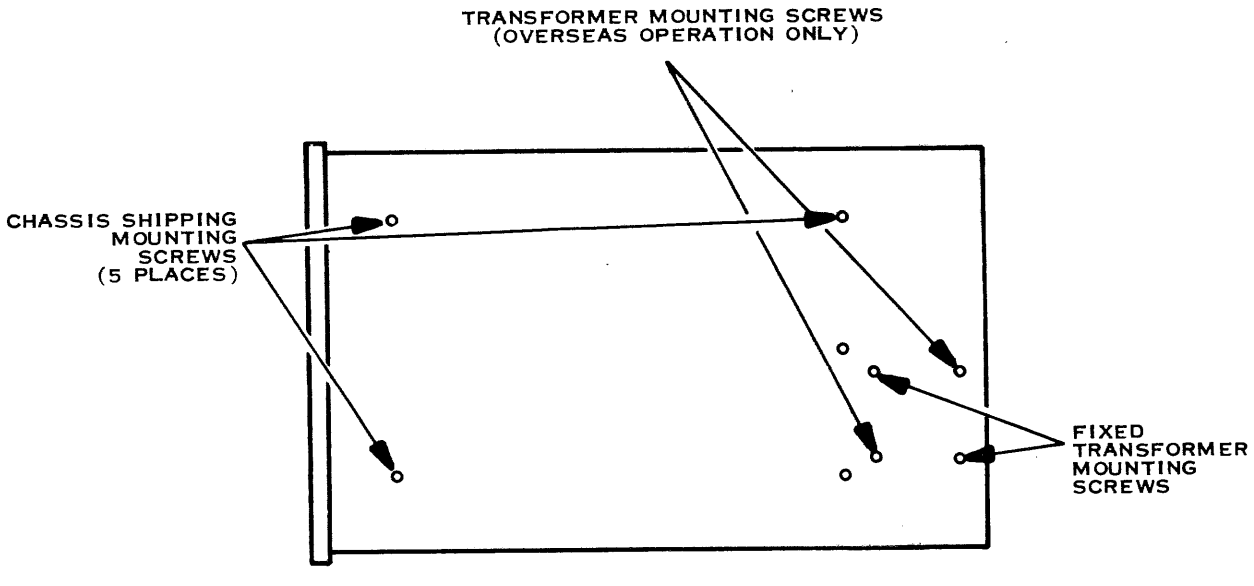
NOTE

If the unit being installed did not have the two #6 mounting screws (see step 11), skip the following step.

13. Remove two (2) #6 screws taped to the top of the computer chassis and insert them in the holes vacated by the two #6 mounting screws moved in step 11. Tighten the two new screws to secure the transformer to the chassis.



(A) 6-SLOT AND TABLE TOP CHASSIS BOTTOM VIEW



(B) 13-SLOT CHASSIS BOTTOM VIEW

(A)133079

Figure 6-2. Location of Chassis Shipping Pallet Mounting Screws

14. Remove the strip of self-adhesive hole covers that are taped to the top of the computer chassis. Use three of the hole covers to cover the three mounting screw holes along the rear of the chassis.

15. Reposition the computer chassis such that the front edge overhangs the work surface to reveal the mounting holes for the front mounting screws.

16. Use the remaining two (2) self-adhesive hole covers to cover the front mounting screw holes.

17. Set the computer chassis in a safe position on the work surface to continue with the remaining portions of the installation procedure.

18. Pack all shipping materials into the original shipping container and store the container for use in reshipment of the unit.

19. Inspect the computer chassis and included components for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse the above procedure using the original packing material.

6.3 UNPACKING/PACKING (OEM CHASSIS)

The OEM chassis is shipped in a corrugated cardboard container together with the circuit boards and mounting hardware for the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. Following preliminary inspection, perform the following steps to remove the chassis from its container. Figure 6-3 illustrates the material included in the packing container.

NOTE

Save shipping carton and all packing materials for use in reshipment of the unit.

1. Position container so that the address label is right-side up.

2. Open top of container and remove chassis assembly enclosed in cushion wrap.

3. Remove cushion wrap from chassis assembly.

4. Remove bag containing mounting hardware from chassis assembly.

NOTE

If circuit boards are included in shipment, they are secured in place by pieces of tape. If no circuit boards are included, skip step 5.

5. Remove pieces of tape that secure circuit boards in chassis.

6. Inspect the chassis and all included components for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

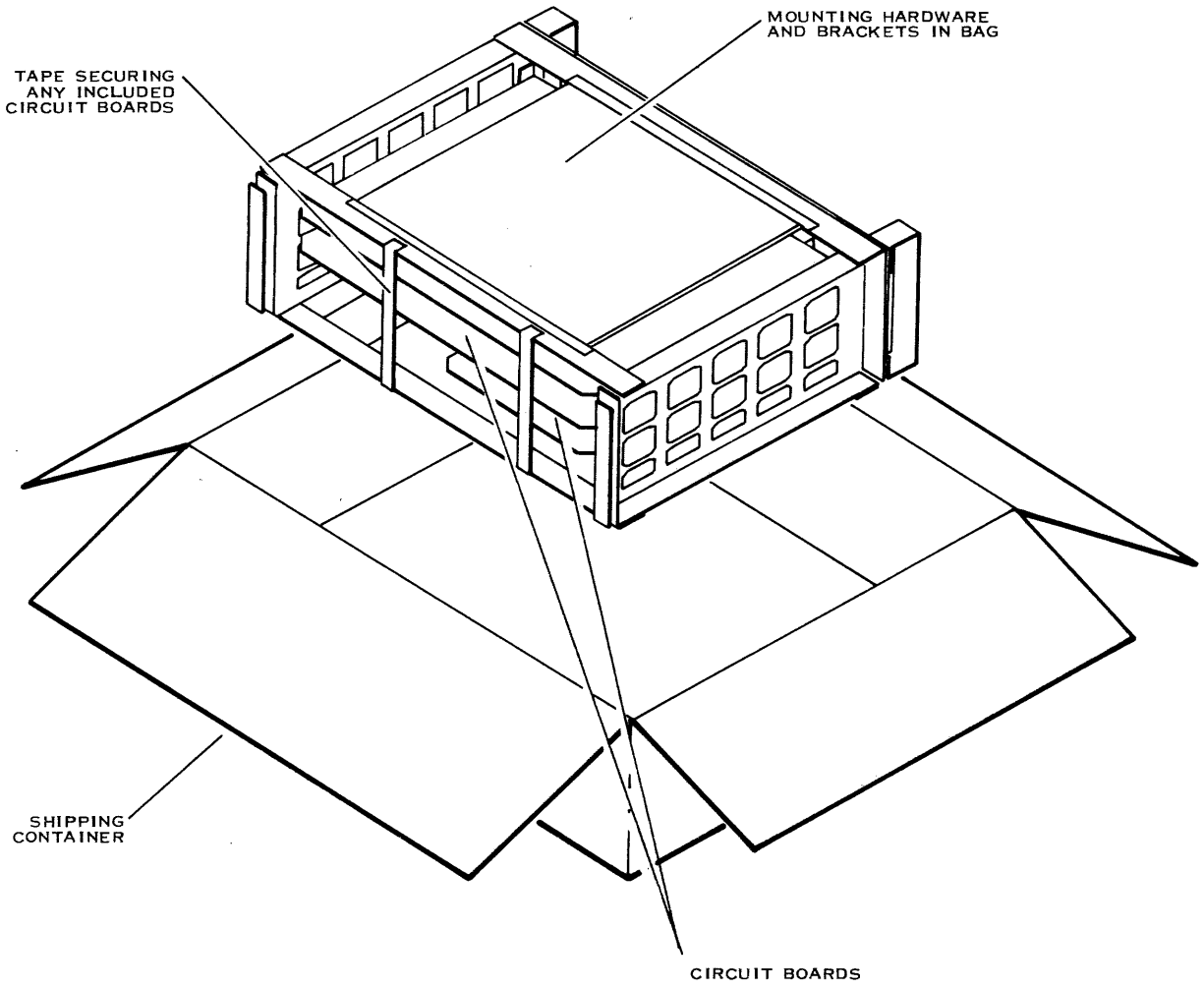


Figure 6-3. OEM Chassis Shipping Packaging

6.4 BOARD PACKING/UNPACKING

The logic board assemblies and power supply boards are shipped in bubble-wrap and corrugated cardboard containers. When removing the shipping materials from a spare subassembly, save the bubble wrap and corrugated cardboard for packing faulty boards for reshipment back to the factory.

APPENDIX A

PROGRAMMING REFERENCE DATA

990/4 INSTRUCTION SET (ALPHABETICAL ORDER)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
A	A000	Add Words	I
AB	B000	Add Bytes	I
ABS	0740	Absolute Value	VI
AI	0220	Add Immediate	VIII
ANDI	0240	AND Immediate	VIII
B	0440	Branch	VI
BL	0680	Branch and Link	VI
BLWP	0400	Branch and Load Workspace Pointer	VI
C	8000	Compare Words	I
CB	9000	Compare Bytes	I
CI	0280	Compare Immediate	VHI
CKOF	03C0	Clock Off	VII
CKON	03A0	Clock On	VII
CLR	04C0	Clear Operand	VI
COC	2000	Compare Ones Corresponding	III
CZC	2400	Compare Zeros Corresponding	III
DEC	0600	Decrement By One	VI
DECT	0640	Decrement By Two	VI
DIV	3C00	Divide	IX
IDLE	0340	Computer Idle	Vii
INC	0580	Increment By One	VI
INCT	05C0	Increment By Two	VI
INV	0540	Invert	VI
JEQ	1300	Jump Equal	II
JGT	1500	Jump Greater Than	II
JH	1B00	Jump High	II
JHE	1400	Jump High Or Equal	II
JL	1A00	Jump Low	II
JLE	1200	Jump Low Or Equal	II
JLT	1100	Jump Less Than	II
JMP	1000	Jump Unconditional	II

990/4 INSTRUCTION SET (ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
JNC	1700	Jump No Carry	II
JNE	1600	Jump Not Equal	II
JNO	1900	Jump No Overflow	II
JOC	1800	Jump On Carry	II
JOP	1C00	Jump Odd Parity	II
LDCR	3000	Load Communication Register	IV
LI	0200	Load Immediate	VIII
LIMI	0300	Load Interrupt Mask Immediate	VIII
LREX	03E0	Load or Restart Execution	VII
LWPI	02E0	Load Workspace Pointer Immediate	VIII
MOV	C000	Move Word	I
MOVB	D000	Move Byte	I
MPY	3800	Multiply	IX
NEG	0500	Negate	VI
ORI	0260	OR Immediate	VIII
RSET	0360	Computer Reset	VII
RTWP	0380	Return From Interrupt Subroutine	VII
S	6000	Subtract Word	I
SB	7000	Subtract Byte	I
SBO	1D00	Set Bit To One	II
SBZ	1E00	Set Bit To Zero	II
SETO	0700	Set Ones	VI
SLA	0A00	Shift Left Arithmetic	V
SOC	E000	Set Ones Corresponding, Word	I
SOCB	F000	Set Ones Corresponding, Byte	I

990/4 INSTRUCTION SET (ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
SRA	0800	Shift Right Arithmetic	V
SRC	0B00	Shift Right Circular	V
SRL	0900	Shift Right Logical	V
STCR	3400	Store Communication Register	IV
STST	02C0	Store Status	VIII
STWP	02A0	Store Workspace Pointer	VIII
SWPB	06C0	Swap Bytes	VI
SZC	4000	Set Zeros Corresponding, Word	I
SZCB	5000	Set Zeros Corresponding, Byte	I
TB	1F00	Test Bit	II
X	0480	Execute	VI
XOP	2C00	Extended Operation	IX
XOR	2800	Exclusive OR	III

990/4 INSTRUCTION SET (HEXADECIMAL OP CODE ORDER)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0200	LI	Load Immediate	VIII
0220	AI	Add Immediate	VIII
0240	ANDI	AND Immediate	VIII
0260	ORI	OR Immediate	VIII
0280	CI	Compare Immediate	VIII
02A0	STWP	Store Workspace Pointer	VIII
02C0	STST	Store Status	VIII
02E0	LWPI	Load Workspace Pointer Immediate	VIII
0300	LIMI	Load Interrupt Mask Immediate	VIII
0340	IDLE	Computer Idle	VII
0360	RSET	Computer Reset	VII
0380	RTWP	Return From Interrupt Subroutine	VII
03A0	CKON	Clock On	VII
03C0	CKOF	Clock Off	VII
03E0	LREX	Load ROM and Execute	VII
0400	BLWP	Branch And Load Workspace Pointer	VI
0440	B	Branch	VI
0480	X	Execute	VI
04C0	CLR	Clear Operand	VI
0500	NEG	Negate	VI
0540	INV	Invert	VI
0580	INC	Increment By One	VI
05C0	INCT	Increment By Two	VI
0600	DEC	Decrement By One	VI
0640	DECT	Decrement By Two	VI
0680	BL	Branch and Link	VI
06C0	SWPB	Swap Bytes	VI
0700	SETO	Set Ones	VI

990/4 INSTRUCTION SET
(HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0740	ABS	Absolute Value	VI
0800	SRA	Shift Right Arithmetic	V
0900	SRL	Shift Right Logical	V
0A00	SLA	Shift Left Arithmetic	V
0B00	SRC	Shift Right Circular	V
1000	JMP	Jump Unconditional	II
1100	JLT	Jump Less Than	II
1200	JLE	Jump Low Or Equal	II
1300	JEQ	Jump Equal	II
1400	JHE	Jump High Or Equal	II
1500	JGT	Jump Greater Than	II
1600	JNE	Jump Not Equal	II
1700	JNC	Jump No Carry	II
1800	JOC	Jump On Carry	II
1900	JNO	Jump No Overflow	II
1A00	JL	Jump Low	II
1B00	JH	Jump High	II
1C00	JOP	Jump Odd Parity	II
1D00	SBO	Set Bit To One	II
1E00	SBZ	Set Bit To Zero	II
1F00	TB	Test Bit	II
2000	COC	Compare Ones Corresponding	III
2400	CZC	Compare Zeros Corresponding	III
2800	XOR	Exclusive OR	III
2C00	XOP	Extended Operation	IX
3000	LDCR	Load Communication Register	IV
3400	STCR	Store Communication Register	IV
3800	MPY	Multiply	IX
3C00	DIV	Divide	IX

990/4 INSTRUCTION SET (HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
4000	SZC	Set Zeros Corresponding, Word	I
5000	SZCB	Set Zeros Corresponding, Byte	I
6000	S	Subtract Word	I
7000	SB	Subtract Byte	I
8000	C	Compare Words	I
9000	CB	Compare Bytes	I
A000	A	Add Words	I
B000	AB	Add Bytes	I
C000	MOV	Move Word	I
D000	MOVB	Move Byte	I
E000	SOC	Set Ones Corresponding, Word	I
F000	SOCB	Set Ones Corresponding, Byte	I

APPENDIX B

INTERRUPT VECTOR TABLE

990/4 Interrupt

Interrupt Priority	Interrupt Name	Reason for Interrupt	Transfer Vector Memory Location	Interrupt Cleared by	Remarks
0	Power Restored	Ac power restored and power supply voltages are stabilized (RESET - LOW)	0000		All other interrupts are masked, level 0 cannot be masked.
1	Power Fail (Jumper E11 to E12)	The power supply senses loss of ac. Approximately 7 milliseconds of program time is available before the system will reset.	0004	Power Restored Reset (TLPRES-)	Optional jumper at E11 and E12
2	Memory Error (Jumper E13 to E14)	[1] A memory parity error has occurred either on the 990/4 board or the memory expansion board (if available).	0008	CRU Bit 12 of console base address-1FE8 or Manual reset on expansion board or power reset (TLPRES-)	Memory parity on the 990/4 board or memory expansion board is optional - on the memory expansion board, switch S1 will disable memory parity error detection. On memory expansion board the Parity Error LED will indicate.
2	Memory Error (Jumper E13 to E14)	[2] An attempt to write into an area assigned as protected memory. Protected memory is an optional feature.	0008	Same as [1]	On optional memory protect the protected areas are defined by an LDCR to a dedicated CRU address of 1FA0.
3	External Device		000C		
4	External Device		0010		

990/4 Interrupt (Continued)

Interrupt Priority	Interrupt Name	Reason for Interrupt	Transfer Vector Memory Location	Interrupt Cleared by	Remarks
5	Real Time Clock	When enabled with CKON, an interrupt will occur on the next cycle of the 120hz clock	0014	An output command sequence of CKOF and CKON or RESET.	This interrupt can be jumpered to either level 5 or level 7 or disconnected.
6	External Device		0018		
7	External Device		001C		The real-time clock may be jumpered to level 7 instead of level 5.

APPENDIX C

DEVICE CRU FORMATS

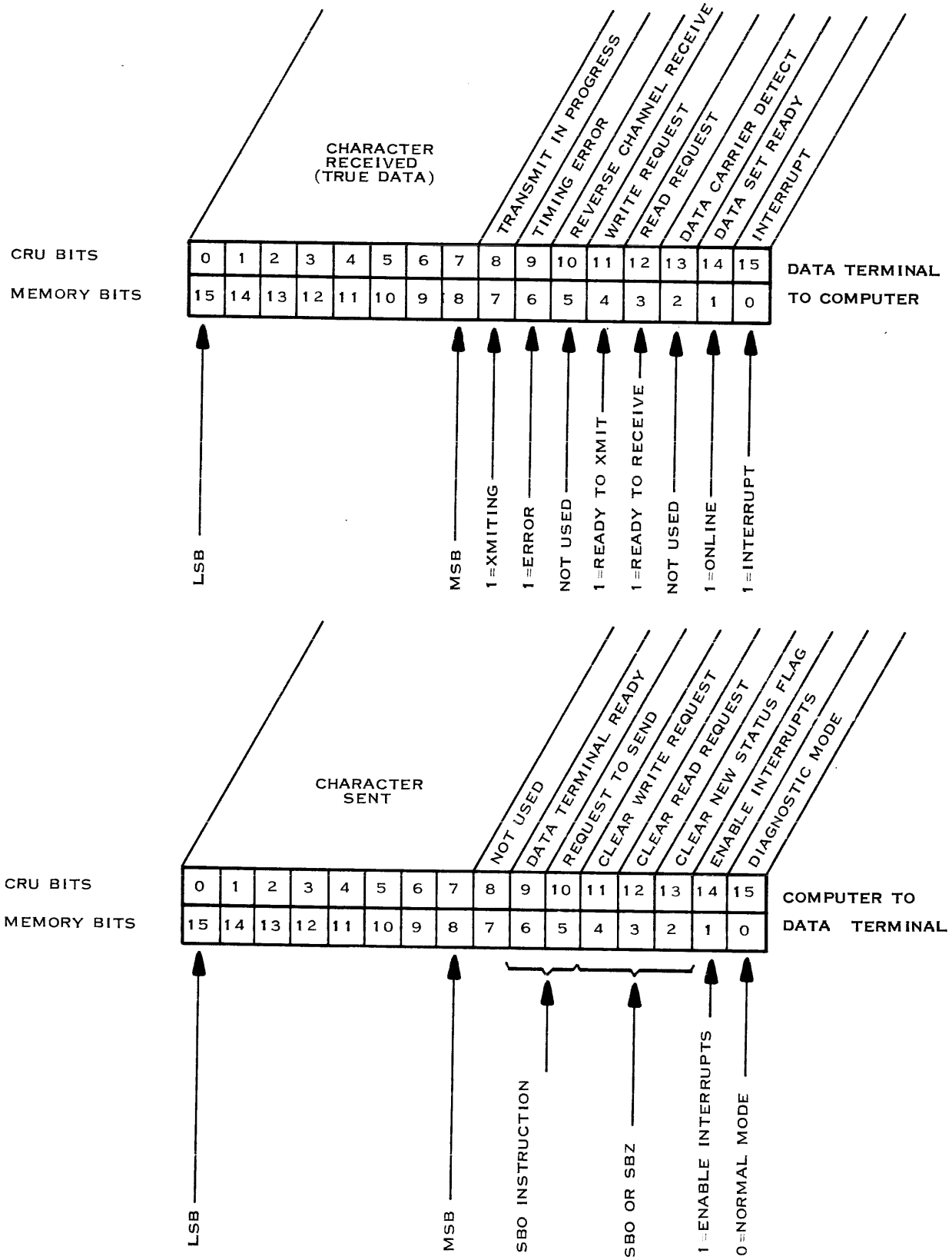


Figure C-1. 733 Data Terminal CRU Formats

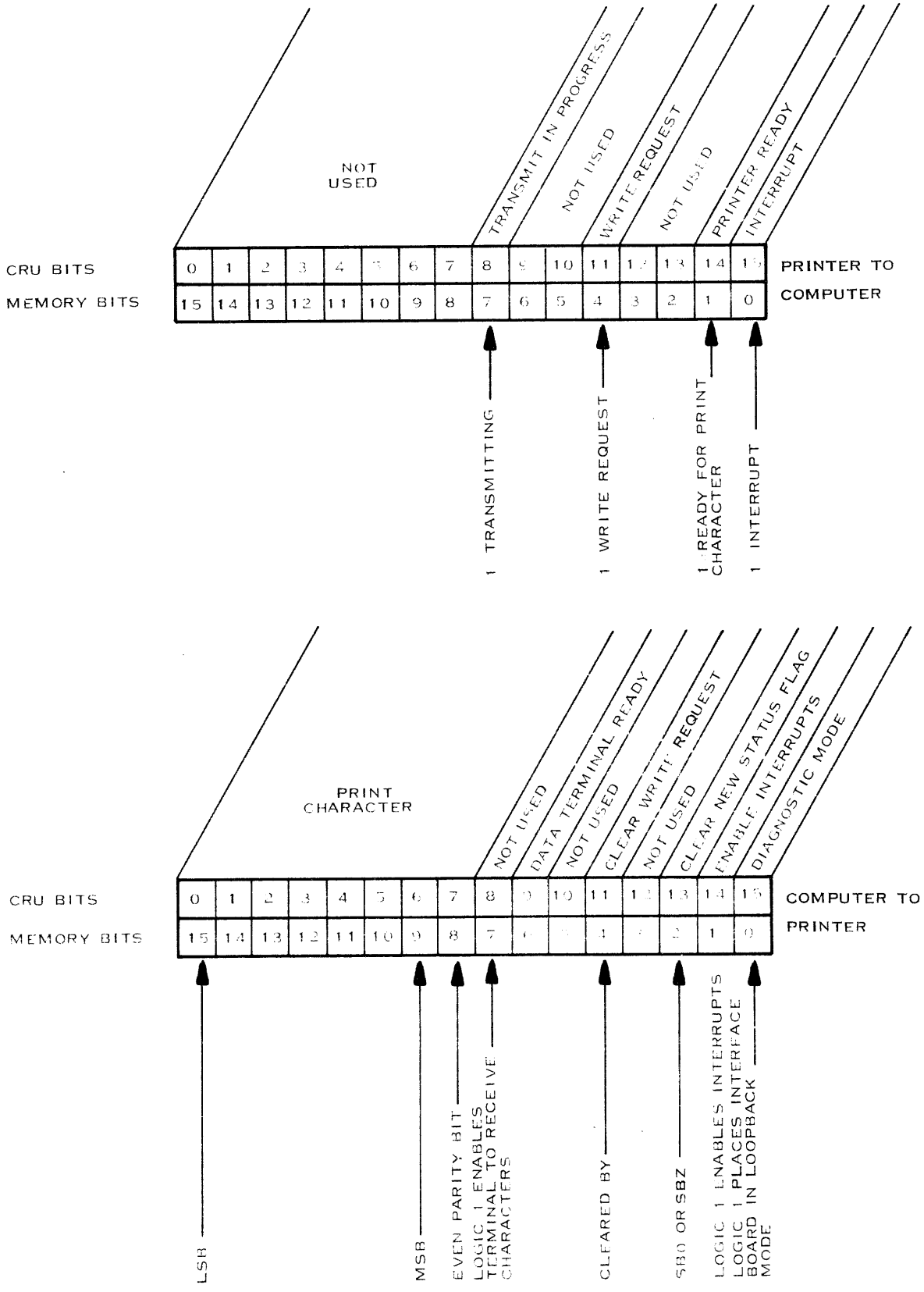


Figure C-2. Model 306/588 Line Printer CRU Formats

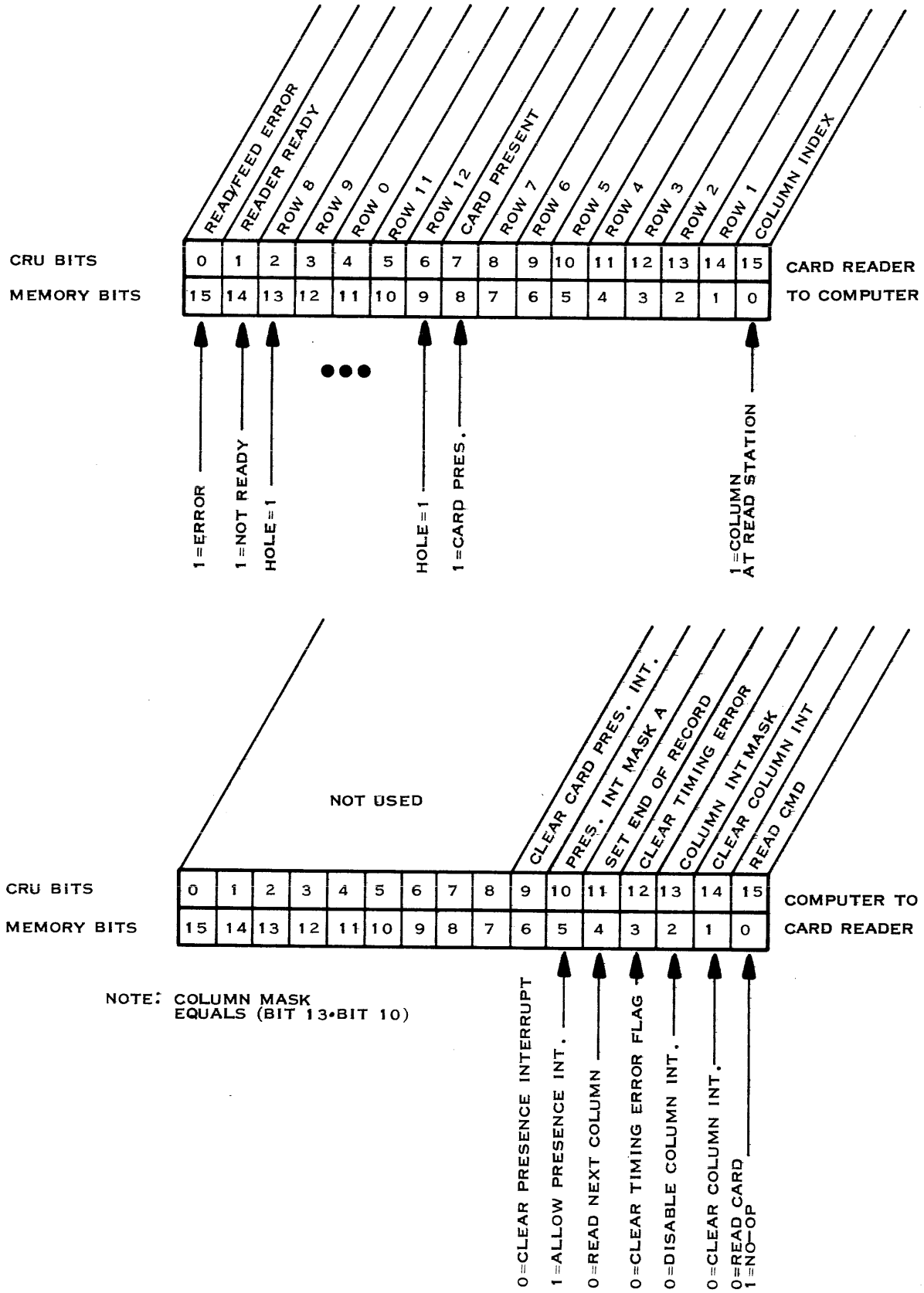


Figure C-3. 804 Card Reader CRU Formats

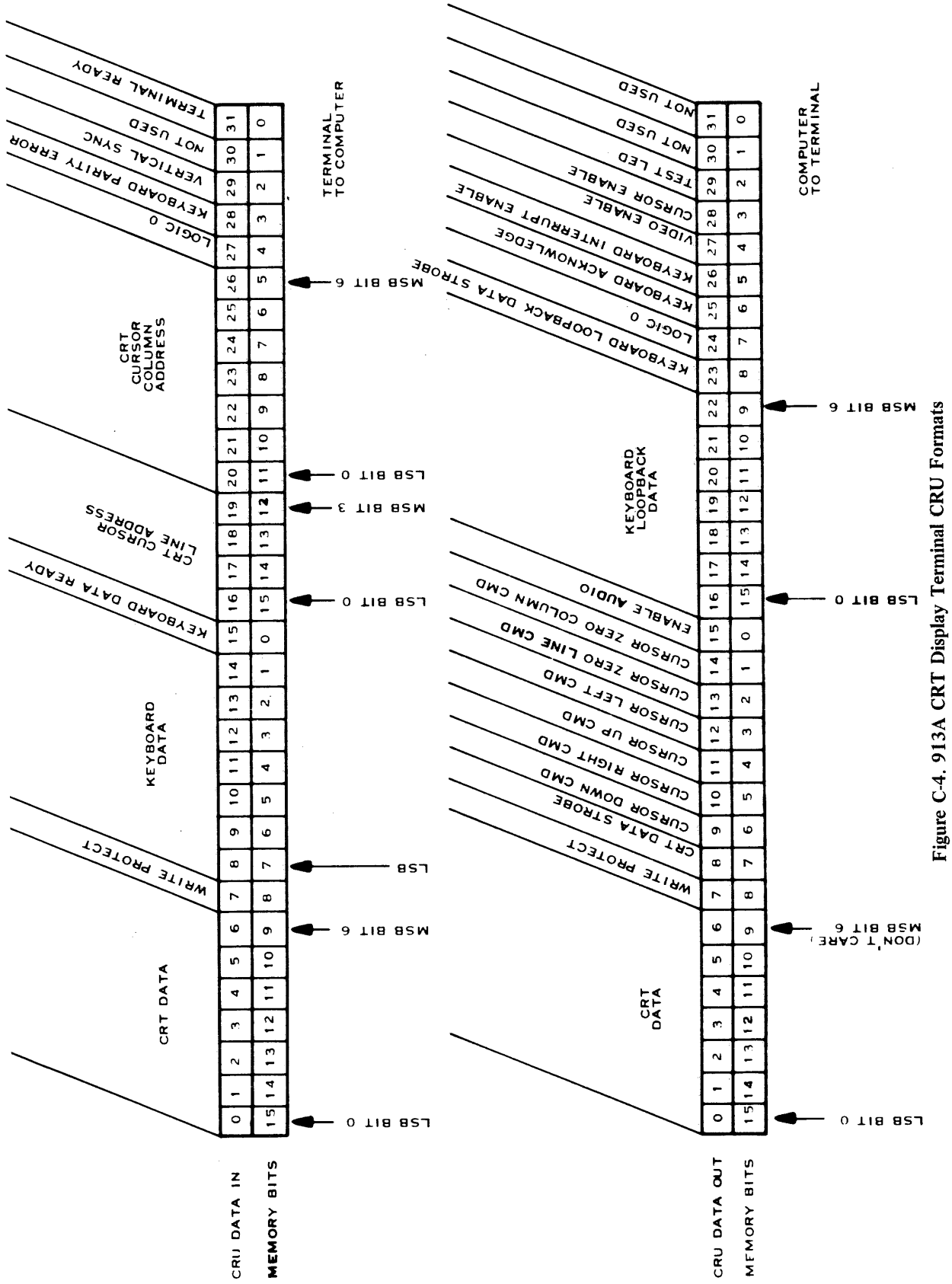


Figure C-4. 913A CRT Display Terminal CRU Formats

APPENDIX D

HEXADECIMAL TO DECIMAL CONVERSION CHARTS

Table D-1. Hexadecimal Arithmetic

ADDITION TABLE

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

MULTIPLICATION TABLE

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

Table D-2. Table of Powers of 16_{10}

16^n	n	16^{-n}
1	0	0.10000 00000 00000 00000 x 10
16	1	0.62500 00000 00000 00000 x 10^{-1}
256	2	0.39062 50000 00000 00000 x 10^{-2}
4 096	3	0.24414 06250 00000 00000 x 10^{-3}
65 536	4	0.15258 78906 25000 00000 x 10^{-4}
1 048 576	5	0.95367 43164 06250 00000 x 10^{-6}
16 777 216	6	0.59604 64477 53906 25000 x 10^{-7}
268 435 456	7	0.37252 90298 46191 40625 x 10^{-8}
4 294 967 296	8	0.23283 06436 53869 62891 x 10^{-9}
68 719 476 736	9	0.14551 91522 83668 51807 x 10^{-10}
1 099 511 627 776	10	0.90949 47017 72928 23792 x 10^{-12}
17 592 186 044 416	11	0.56843 41886 08080 14870 x 10^{-13}
281 474 976 510 656	12	0.35527 13678 80050 09294 x 10^{-14}
4 503 599 627 370 496	13	0.22204 46049 25031 30808 x 10^{-15}
72 057 594 037 927 936	14	0.13877 78780 78144 56755 x 10^{-16}
1 152 921 504 606 846 976	15	0.86736 17379 88403 54721 x 10^{-18}

Table D-3. Table of Powers of 10_{16}

10^n	n	10^{-n}
1	0	1.0000 0000 0000 0000
A	1	0.1999 9999 9999 999A
64	2	0.28F5 C28F 5C28 F5C3 x 16^{-1}
3E8	3	0.4189 374B C6A7 EF9E x 16^{-2}
2710	4	0.68DB 8BAC 710C B296 x 16^{-3}
86A0	5	0.A7C5 AC47 1B47 8423 x 16^{-4}
F 4240	6	0.10C6 F7A0 B5ED 8D37 x 16^{-4}
98 9680	7	0.1AD7 F29A BCAF 4858 x 16^{-5}
5F5 E100	8	0.2AF3 1DC4 6118 73BF x 16^{-6}
3B9A CA00	9	0.44B8 2FA0 9B5A 52CC x 16^{-7}
2 540B E400	10	0.6DF3 7F67 5EF6 EADF x 16^{-8}
17 4876 E800	11	0.AFEB FF0B CB24 AAFF x 16^{-9}
E8 D4A5 1000	12	0.1197 9981 2DEA 1119 x 16^{-9}
918 4E72 A000	13	0.1C25 C268 4976 81C2 x 16^{-10}
5AF3 107A 4000	14	0.2D09 370D 4257 3604 x 16^{-11}
3 8D7E A4C6 8000	15	0.480E BE7B 9D58 566D x 16^{-12}
23 86F2 6FC1 0000	16	0.734A CA5F 6226 F0AE x 16^{-13}
163 4578 5D8A 0000	17	0.B877 AA32 36A4 B449 x 16^{-14}
DE0 B6B3 A764 0000	18	0.1272 5DD1 D243 ABA1 x 16^{-14}
8AC7 2304 89E8 0000	19	0.1D83 C94F B6D2 AC35 x 16^{-15}

Table D-4. Table of Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5

Table D-5. Hexadecimal–Decimal Integer Conversion Table

The table appearing on the following pages provides a means for direct conversion of decimal integers in the range of 0 to 4095 and for hexadecimal integers in the range of 0 to FFF.

To convert numbers above those ranges, add table values to the figures below:

Hexadecimal	Decimal	Hexadecimal	Decimal
01 000	4 096	20 000	131 072
02 000	8 192	30 000	196 608
03 000	12 288	40 000	262 144
04 000	16 384	50 000	327 680
05 000	20 480	60 000	393 216
06 000	24 576	70 000	458 752
07 000	28 672	80 000	524 288
08 000	32 768	90 000	589 824
09 000	36 864	A0 000	655 360
0A 000	40 960	B0 000	720 896
0B 000	45 056	C0 000	786 432
0C 000	49 152	D0 000	851 968
0D 000	53 248	E0 000	917 504
0E 000	57 344	F0 000	983 040
0F 000	61 440	100 000	1 048 576
10 000	65 536	200 000	2 097 152
11 000	69 632	300 000	3 145 728
12 000	73 728	400 000	4 194 304
13 000	77 824	500 000	5 242 880
14 000	81 920	600 000	6 291 456
15 000	86 016	700 000	7 340 032
16 000	90 112	800 000	8 388 608
17 000	94 208	900 000	9 437 184
18 000	98 304	A00 000	10 485 760
19 000	102 400	B00 000	11 534 336
1A 000	106 496	C00 000	12 582 912
1B 000	110 592	D00 000	13 631 488
1C 000	114 688	E00 000	14 680 064
1D 000	118 784	F00 000	15 728 640
1E 000	122 880	1 000 000	16 777 216
1F 000	126 976	2 000 000	33 554 432

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0529	0521	0522	0523	0524	0525	0526	0527
210	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
220	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
230	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
240	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
250	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
260	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
270	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
280	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
290	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A0	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B0	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C0	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D0	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E0	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F0	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767

Table D-5. Hexadecimal - Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
300	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
310	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
320	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
330	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
340	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
350	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
360	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
370	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
380	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
390	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A0	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B0	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C0	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D0	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E0	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
400	1024	1025	0126	0127	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1291	1293	1294	1295
510	1296	1297	1298	1299	1399	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1329	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1367	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1429	1421	1422	1423
590	1324	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
3B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1515	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1592	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	17231	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
700	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	8102	1803	1804	1805	1806	1807
710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1818	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1909	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	3496	2397	2398	2399
960	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
970	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
980	2432	2433	2434	24351	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2479	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559
A00	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2626	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775

APPENDIX E

SCOPING LOOP PROGRAMS

APPENDIX E

SCOPING LOOP PROGRAMS

E.1 GENERAL

This section contains a collection of loop programs which may be entered into the computer through the programmer panel. The procedure for entering all of these programs is essentially the same as outlined in paragraph E.2.

E.2 READ FOLLOWED BY WRITE AT SAME MEMORY LOCATION

The following program may be used to loop on a single specified address within the 32K address space of the 990/4:

MEM Location	Machine Code	Comments
0900	02E0	LWPI, >100
0902	0100	
0904	0208	LI R8, (location)
0906	2000	Desired memory address (byte address)
0908	0209	LI R9, (data)
090A	0F0F	(or any desired data pattern)
090C	C609	Mov R9, *R8
090E	10FE	JMP $-1

The scoping loop is entered into the computer from the programmer panel using the following procedure:

1. Set the key switch on the programmer panel to the UNLOCK position.

2. If the RUN LED is lit, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinguished.

3. Press the CLR switch to clear the panel's display register.

4. Press the ENTER ST (enter status) switch to clear the status register in the TMS 9900.

5. Set up 0900_{16} on the data display LEDs using the data entry switches. This is the address in memory where the first instruction of the scoping loop is to be stored.

NOTE

When a data display LED is lit, it indicates a "1".

6. Press ENTER MA switch to load the memory address value 0900 into the memory address register of the TMS 9900.

7. Press CLR to clear the displays for the next entry.

8. Set up the instruction code ($02E0_{16}$) on the data LED displays using the data entry switches.

9. Press MDE switch which causes 02E0 to be loaded into memory location 0900.

10. Press MAI which increments the memory address value stored in the memory address register and repeat steps 8-11 to enter the following program values into successive memory locations:

    - 0100
    - 0208
    - Address on which the test will loop (0000 to 1FFFE inclusive)
    - 0209
    - Data to be written into the looped memory location (e.g., $1F1F_{16}$)
    - C609
    - 10FE

11. Press CLR to clear the displays.

12. Enter 0900 into the displays (address of first instruction in the scoping loop).

13. Press ENTER PC to load the value into the program counter.

14. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

E.3 CONTINUOUS READ FROM SELECTED MEMORY LOCATION

The basic scoping loop program described in E.2 may be modified to perform a continuous read at a selected memory address by changing the instruction at memory location 090C in the previous program from C609 to C258 which is a MOV *R8,R9 instruction. This change to the basic program causes data to be read from a selected address and stored in memory location 0112 (workspace register 9). For maintenance purposes, the scoping loop may be interrupted at any time and the value stored in the workspace register may be examined using the following procedure:

1. Halt the processor by pressing HALT/SIE. The RUN LED should extinguish.

2. Press CLR to clear the displays.

3. Enter 0112 into the displays using the data entry switches.

4. Press ENTER MA to load 0112 into the memory address register.

5. Press MDD. The resulting value displayed on the panel LEDs should be the same value stored in memory location 90A of the scoping loop program.

E.4 SCOPING LOOP FOR A BAND OF MEMORY ADDRESSES

The basic scoping loop program may also be modified as follows to permit looping over a band of memory addresses in which the beginning and ending addresses are specified in the program:

Scoping Loop for Reading Band of Memory Addresses

MEM Location	Machine Code	Comments
0900	02E0	LWPI >80
0902	0100	
0904	020A	LI R10, ENDLOC
0906	ENDLOC	Ending address +2
0908	0209	LI R9, DATA
090A	DATA	
090C	0208	LI R8, LOC
090E	LOC	
0910	CE09	MOV R9, *R8+
0912	820A	C R10, R8
0914	14FB	JHE
0916	10FC	JMP

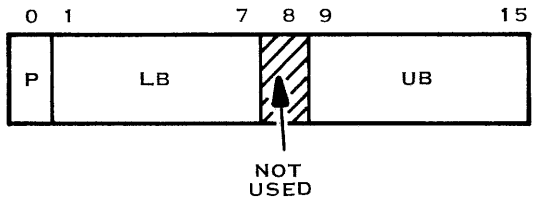
The procedures for entering this program into computer memory are essentially the same as described in paragraph E.2.

E.5 SCOPING LOOP FOR WRITE PROTECT

The following scoping loop will permit the write protect register on the memory expansion board to be loaded with a protect value and will then attempt to write into the protected memory space resulting in a protect violate condition. The program then loops back and repeats these functions to permit a dynamic test of the write protect section.

MEM Location	Machine Code	Comments
0200	0300	LIMI >0
0202	0000	
0204	02E0	LWPI >100
0206	0100	
0208	020C	LI R12, >1FA0
020A	1FA0	
020C	0209	LI R9, >1011 (Adr. 2000 to 21FE)
020E	1011	
0210	3009	LDCR R9, 0
0212	C809	MOV R9, >2000 (Attempt write into LOC 2000)
0214	2000	
0216	1F00	TB 0
0218	1D00	SBO 0
021A	10FA	JMP $-6

E.5.1 **SETTING A WRITE PROTECT REGION.** To set a write protect region, the lower and upper bounds must be output to CRU base address $1FA0_{16}$. The most significant bit (bit 0) is the Protect/Permit bit. Bit 0, when set to 1, indicates write permit, and, when set to 0, indicates write protect. To specify the protect region, memory is divided into 256-word blocks. The lower and upper bounds are each seven bits long and serve as an index into the memory addresses to specify which contiguous 256-word block of memory is to be protected. For example, the lower bound of the protect region equal to 2000_{16} would be represented in the Protect register as 10_{16}. The memory block beginning at location 2000_{16} is the sixteenth 256-word (512-byte) memory block. A bound is calculated by dividing the starting address of the memory block by 200_{16} (512_{10}). In this example, 2000_{16} divided by 200_{16} is equal to 10_{16}. The upper bound is not included in the protect region. When outputting to the CRU Protect register to specify the protect bounds, a Load CRU (LDCR) instruction with a count of 16 must be used to sell all 16 bits because the Protect register works like a shift register. To protect the memory range 2000_{16} to 4000_{16}, the lower bound is set equal to 10_{16}, the upper bound is set equal to 20_{16}, and the Protect bit is set to 0. Therefore, the Protect register is set to 1020_{16} by outputting these fields to the CRU in the format specified in figure E-1.



BIT FIELDS

P	PROTECT/PERMIT BIT 0=PROTECT 1=PERMIT
LB	LOWER BOUND
UB	UPPER BOUND

NOTES

THE CRU OUTPUT DATA FORMAT IS THE SAME AS THE FORMAT OF DATA IN MEMORY BEFORE LDCR INSTRUCTION IS EXECUTED.

BITS 1 AND 9 ARE THE MOST SIGNIFICANT BITS, AND BITS 7 AND 15 ARE THE LEAST SIGNIFICANT BITS OF THE LB AND UB FIELDS.

(A)133373

Figure E-1. Write Protect Vector Format

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

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