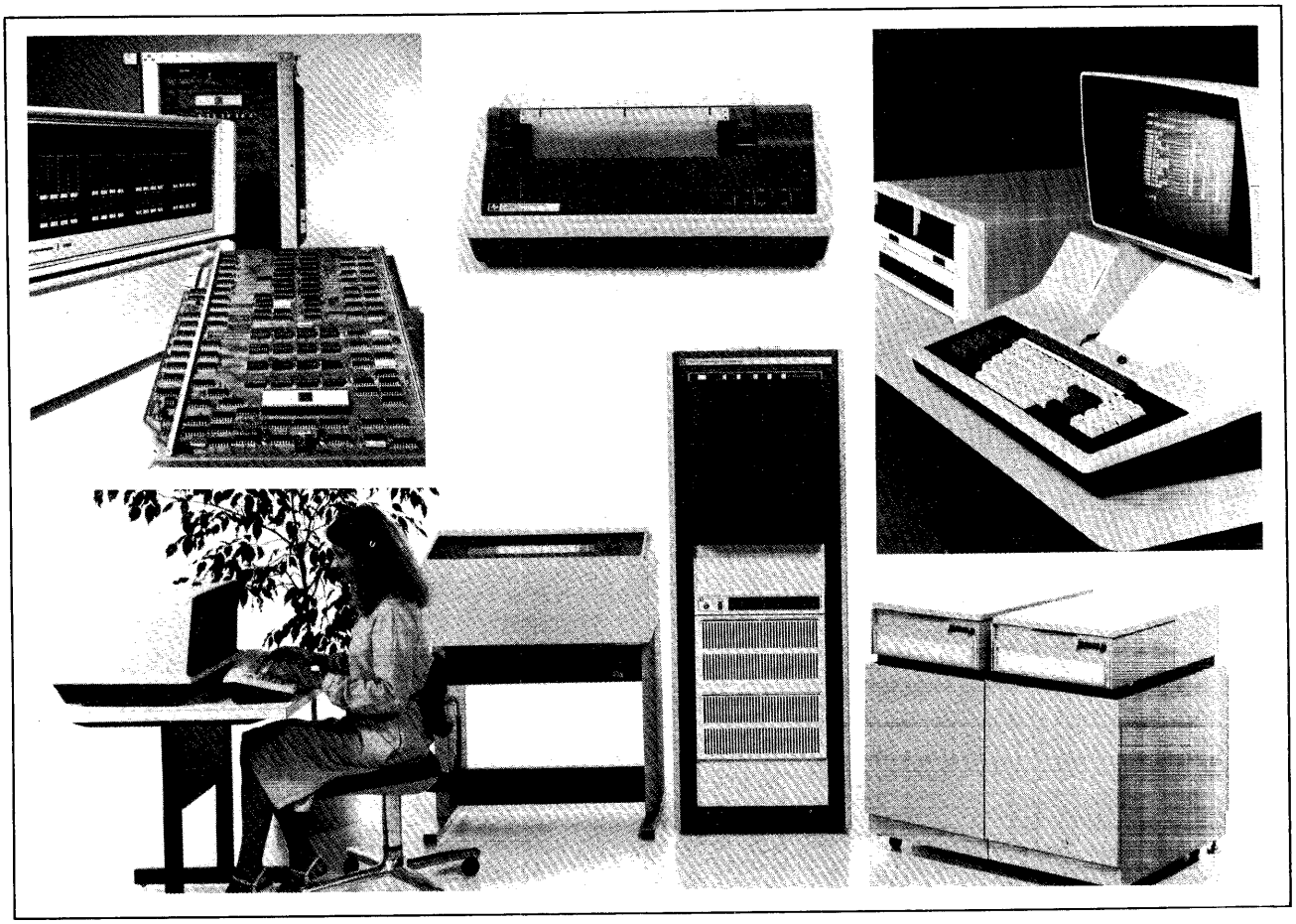
Model 990 Computer
Model DS80 Disk System
Installation and Operation Manual



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1 July 1982

TEXAS INSTRUMENTS

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Preface

This manual provides detailed instructions for installing and operating a Model DS80 disk system with a Model 990 computer and TILINE* data bus. Programming information for those users who wish to write their own input/output routines is included also. Information in this manual is divided into four sections as follows:

Section

1 General Description — Briefly describes the features and major components of the disk system.

2 Installation — Provides site requirements and step-by-step instructions for unpacking and installing the disk system.

3 Programming — Presents information for use by programmers in designing device service routines that interface directly with the disk system.

4 Operation — Describes system operating procedures.

The following documents contain additional information related to the Model DS80 disk system:

Title	Part Number
Model 990/12 Computer Hardware User's Manual	264446-9701
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990/5 Computer Hardware User's Manual	946294-9701
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990/12 Computer Assembly Language Programmer's Guide	2250077-9701
Model 990 Computer Family Maintenance Drawings, Volume I — Peripherals	945421-9702
Model 990 Computer Diagnostics Handbook	945400-9701

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Title	Part Number
Model DS80 Disk System Field Maintenance Manual	2302630-9701
Error Correcting Disk Controller Depot Maintenance Manual	2272082-9701
DS990 Systems Field Maintenance Instructions	2250696-9701
Century Data Systems Trident Disk Drive Maintenance Manual	76205-300

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1

General Description

1.1 GENERAL

The Texas Instruments Model DS80 80-megabyte Disk System (Figure 1-1), is a random-access, mass data storage unit that provides 80 megabytes of online data storage and features a removable disk pack. Up to four disk drives may be connected in a daisy-chained configuration to any TI Model 990 computer with a TILINE data bus.

System features include:

- Removable disk pack
- Single circuit board disk controller
- Up to four disk drives (can have different storage capability) per controller
- Independent manual write-protection of media
- Individual disk drive interrupt masking
- Microprocessor-based controller logic
- Error checking and correction capability
- Extended fault isolation
- Fast average seek access time (30 milliseconds)
- 9.67 MHz bit transfer rate at disk interface
- Accurate track-following servo
- Dynamic spindle brake allowing quick pack change
- Automatic power sequencing of disk drives
- Integral power supply

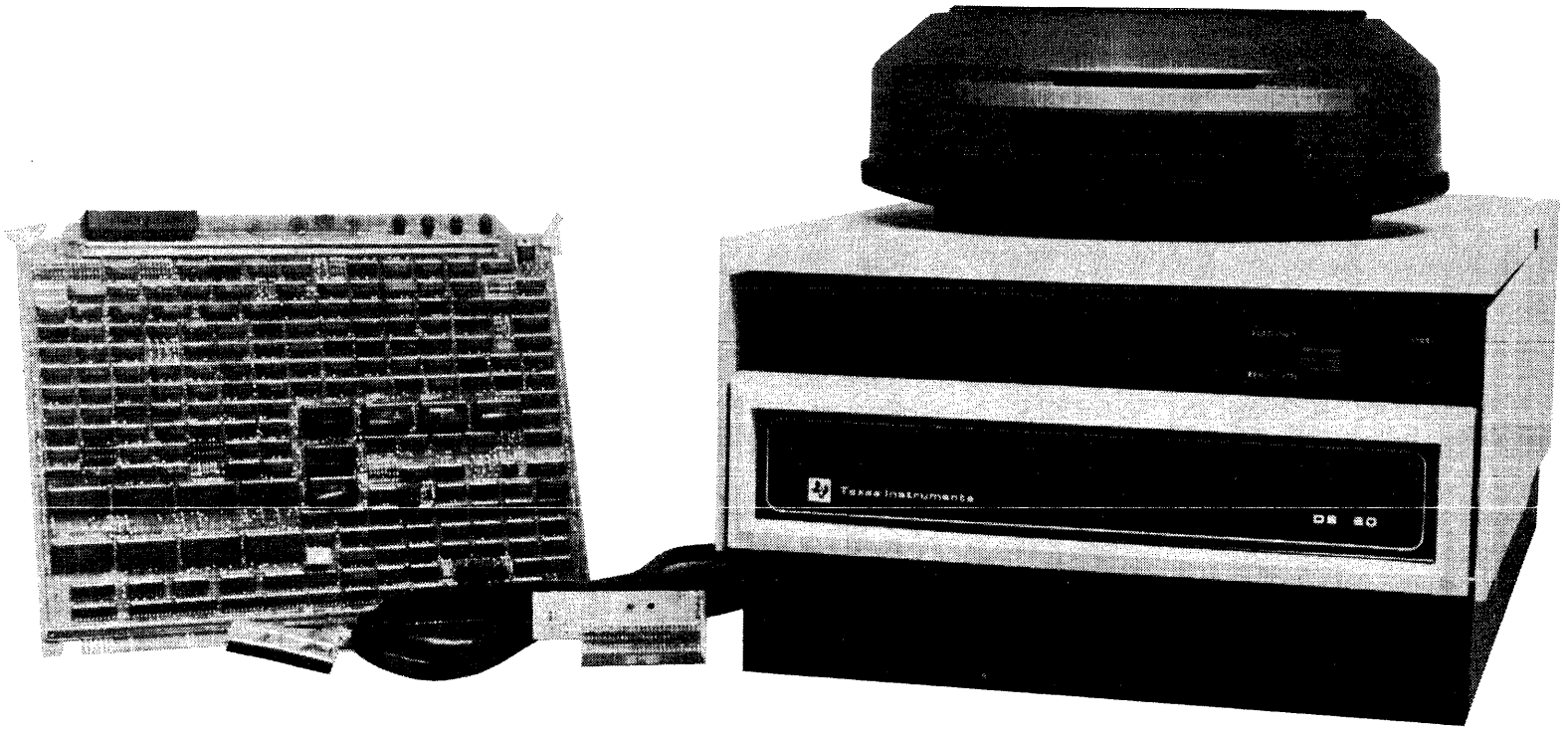

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Figure 1-1. Model DS80 Disk System

1.2 SYSTEM COMPONENTS

The Model DS80 disk system consists of a disk controller, up to four disk drives, a terminator, and associated interconnecting cables. Major system components and part numbers are listed in Table 1-1, and are described in the following paragraphs.

Table 1-1. Disk System Components and Part Numbers

Item	Part Number
Model DS80 disk system	2308467-00XX
Model DS80 disk drive	2308469-00XX
Error correcting disk controller	2269405-0002
Model DS80 disk terminator	2308480-0001
I/O cables	
Controller-to-drive	2308634-0001
Drive-to-drive	2308634-0003
DS80 disk pack	2308475-0001
Documentation:	
Model DS80 Disk System Installation and Operation	2302629-9701
Model DS80 Disk System Field Maintenance Manual	2302630-9701
Error Correcting Disk Controller Depot Maintenance Manual	2272082-9701

1.2.1 Error Correcting Disk Controller

The Error Correcting Disk controller (Figure 1-2) is a full-width circuit board that occupies one slot in the 990 computer chassis or TILINE expansion chassis. Note that this controller is also used with the CD1400 disk system, and a CD1400 disk drive may be daisy-chained with up to two DS80 disk drives using a single controller. The TILINE data bus, dc power lines, and the interrupt system are accessed through connectors at the bottom of the chassis slot. All control, select, status, and data communications between the 990 computer and the disk drives are handled by the disk controller. Controller operation is initiated when the computer transmits a block of eight control words over the TILINE. These control words contain a command code and a set of parameters that completely describe the required operation. The controller acts independently during the operation, freeing the 990 processor for other tasks. All necessary record location, control/status signal interchange, memory access, data transmission, error checking and correction, and format

conversion operations are handled by the controller. Upon completion of the operation, which optionally causes an interrupt, the processor may read controller, drive, and operational status words located at the control word addresses.

1.2.2 Model DS80 Disk Drive

The Model DS80 disk drive basic unit (Figure 1-3) contains 80 megabytes of unformatted data capacity on a removable, five-platter disk pack. The drive is completely self-contained in the drive chassis, which may be mounted on a secure tabletop or on a pedestal.

A rotation speed of 3600 revolutions per minute enables the disk drive to operate at a 9.67-MHz data rate. Head positioning is performed through the use of a closed-loop proportional servo system, with both acceleration and velocity feedback. The carriage is driven by a voice-coil linear actuator that uses positioning information derived from a dedicated servo surface on one of the pack surfaces. The disk pack consists of five platters; three of the platters are used for data storage and servo information, and two platters (top and bottom) protect the inner platters of the disk pack.

The disk drive chassis contains the spindle, spindle drive motor, head carriage and heads, linear motor, logic card cage containing drive control electronics, air shroud, blower, power supply, relay assembly, operator controls, and front, rear, and disk pack covers. Figure 1-4 shows the location of each of these major assemblies.

1.2.2.1 Spindle. The disk pack is mounted on the spindle, which is then rotated by the spindle drive motor.

1.2.2.2 Spindle Drive Motor. The spindle drive motor turns the spindle through a 1:1 drive belt system.

1.2.2.3 Head Carriage and Heads. Five read/write heads and one servo head are mounted on the head carriage that moves laterally over the disk surfaces to select different cylinders. The linear motor, connected directly to the head carriage, positions the head carriage. The carriage allows the heads to fly over disk platter surfaces whenever the heads are extended over the platter surfaces.

1.2.2.4 Linear Motor. The linear motor positions the heads to the desired cylinder using servo information derived from signals from the drive servo electronics. The linear motor uses a voice coil actuator and magnet to position the head carriage.

1.2.2.5 Logic Card Cage. The logic card cage houses the major disk drive electronics on six plug-in printed wiring boards (PWBs). All drive interface, control, read/write logic, and servo circuits are contained on these boards.

1.2.2.6 Blower. The blower provides clean cooling air to the drive motor and electronics. The blower operates when power is applied to the drive.

1.2.2.7 Air Shroud. The air shroud surrounds the disk pack and directs air flow to the disk pack from the blower. The disk pack cover is also mounted to the air shroud.

1.2.2.8 Disk Pack Cover. The disk pack cover seals and protects the disk pack area from contamination. The cover is raised to load and unload the disk pack.

NOTE

Power must be applied before opening the disk pack cover.

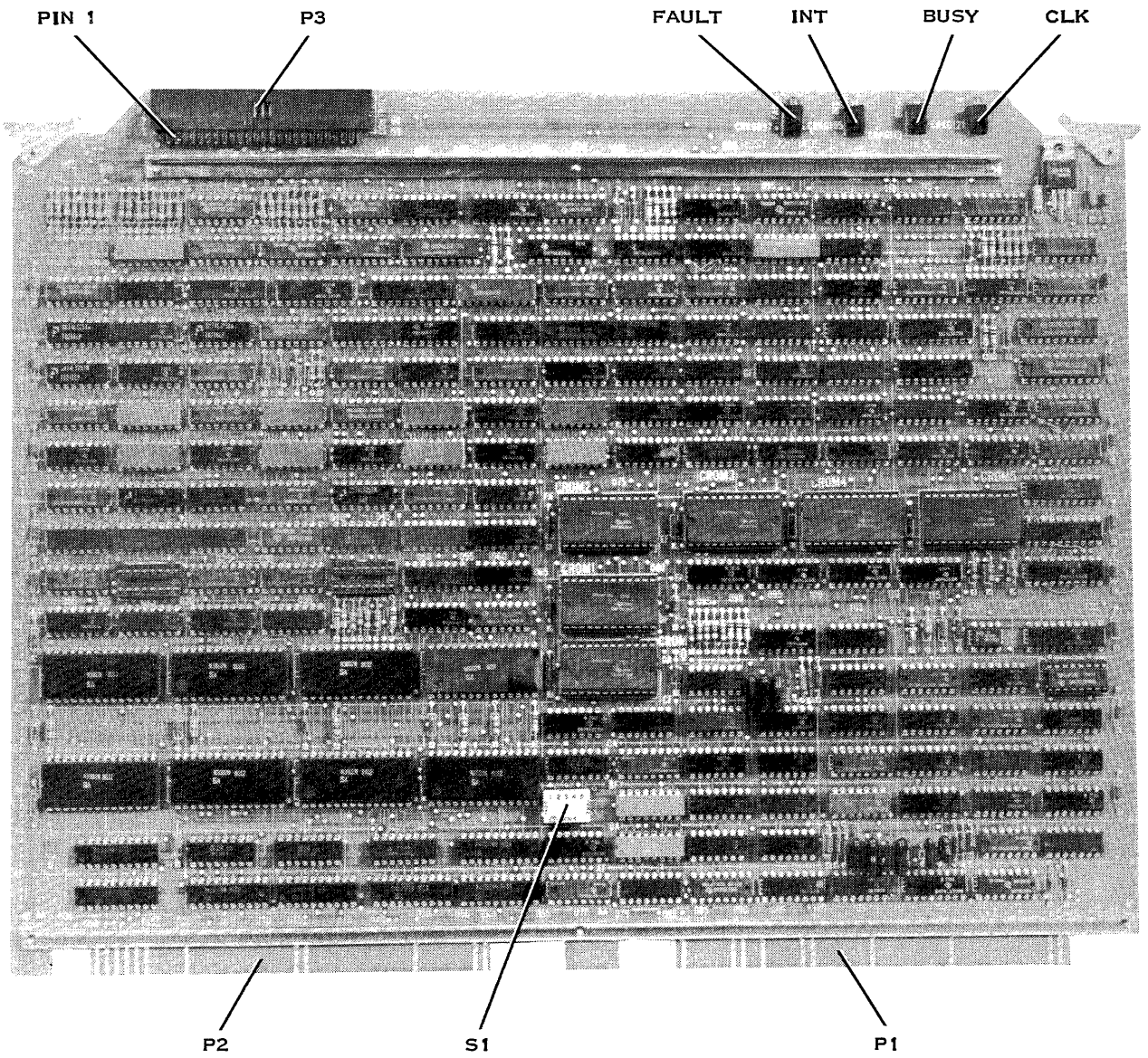

Figure 1-2. Error Correcting Disk Controller

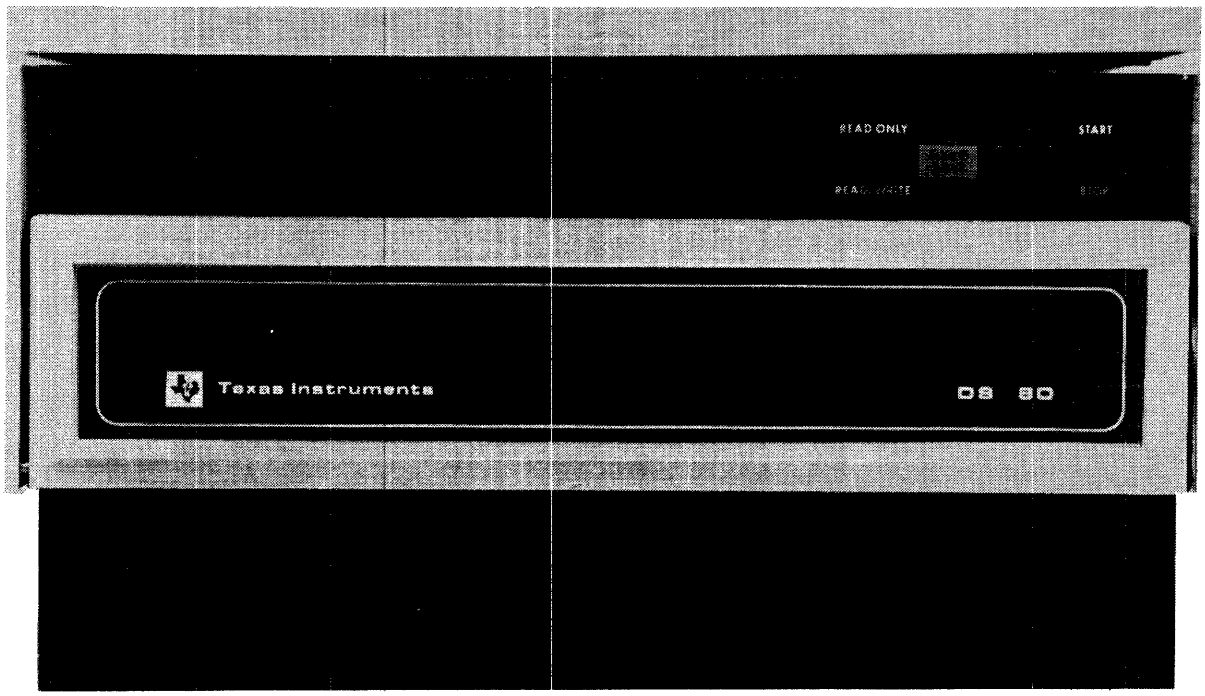

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Figure 1-3. Model DS80 Disk Drive

1.2.2.9 Front and Rear Covers. The front and rear covers protect the disk drive chassis. They are removable for maintenance purposes. The front cover contains the pre-filter.

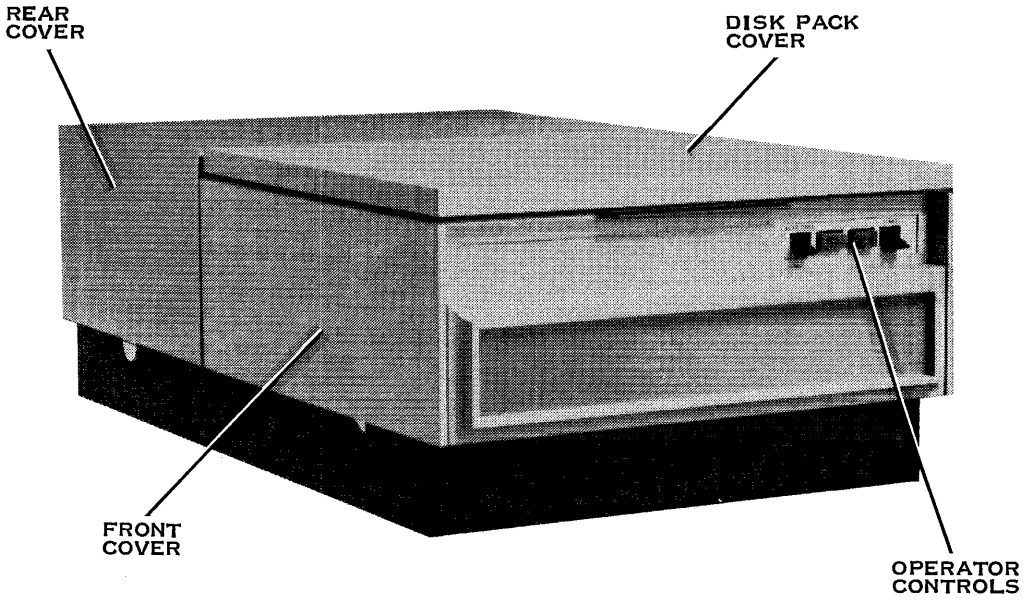
1.2.2.10 Power Supply. The power supply provides all necessary dc voltages to operate the disk drive.

1.2.2.11 Relay Assembly. The relay assembly contains the relay and solid-state switches that control power sequencing operations.

1.2.2.12 Operator Control Panel. The operator control panel contains the indicator lights and switches used to control the disk drive. Controls and indicators on the front panel are the START/STOP switch, DEVICE CHECK indicator, green ready indicator, and READ ONLY-READ/WRITE switch. Refer to the operation section of this manual for instructions for using these switches and indicators.

1.3 SYSTEM OPERATIONAL DESCRIPTION

The following paragraphs describe how the TILINE data bus, disk controller, and disk drive interact with the 990 computer to provide on-line data storage functions. Figure 1-5 is a block diagram that shows system interconnections.



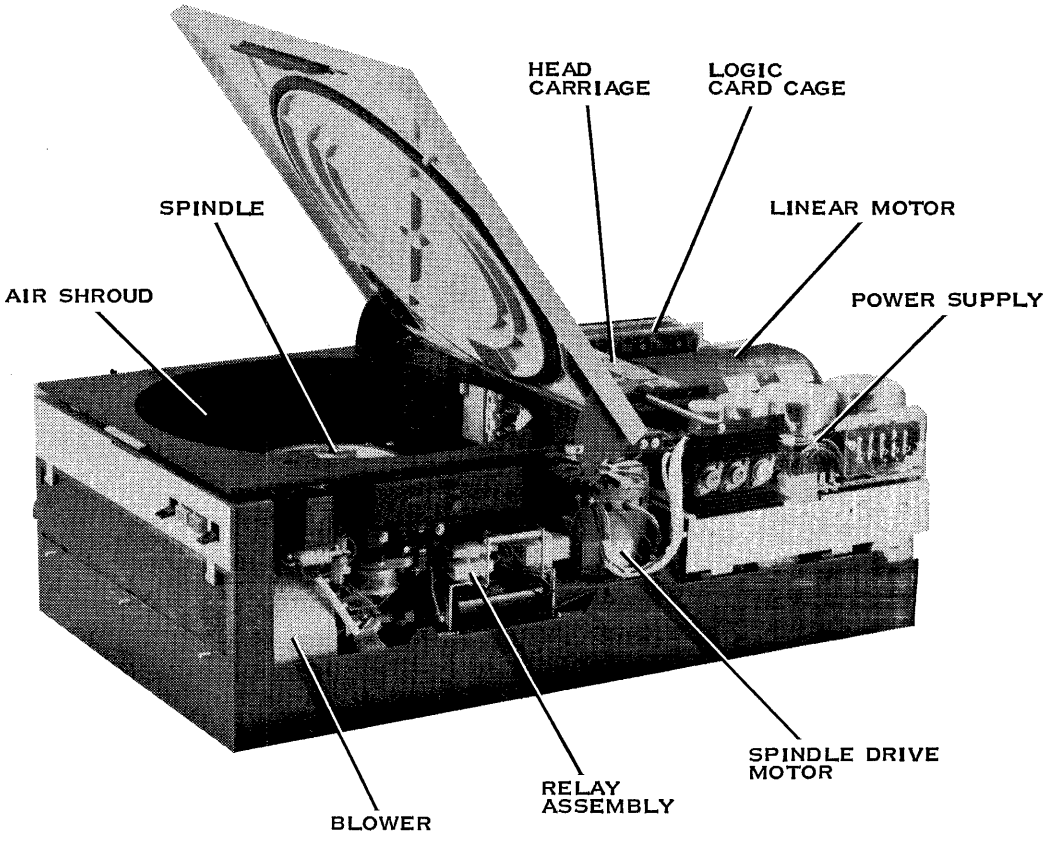


Figure 1-4. Disk Drive Major Assemblies

1.3.1 TILINE Bus

The TILINE is an asynchronous 16-bit parallel data bus that transfers data between high-speed system elements such as the 990 main memory, 990 central processing unit (CPU), and disk controllers. The 16 bits of data accompany a 20-bit TILINE address that only one device can recognize as falling within the range of addresses allocated to it. Devices on the TILINE act as either masters or slaves. Master devices, such as the CPU, contend for access to and control of the TILINE in order to initiate data transfers. Slave devices, such as the main memory, respond only when addressed by a master device.

1.3.2 Disk Controller Operations

The disk controller can act as either a master or a slave. Acting as a master, it gains control of the TILINE to read from or write to main memory, just as the CPU does. Acting as a slave, it responds when any of its eight on-board memory locations are addressed by a master such as the CPU. The TILINE bus architecture incorporates the disk controller directly into CPU addressable memory space. The CPU addresses the controller in the same way that it would main memory, by transmitting data and address signals over the TILINE. The controller slave logic responds to its allocated range of addresses in the same way that memory does. Thus the TILINE bus provides reliable, high-speed input/output control.

The disk controller operates as a slave device when it receives commands from the CPU, and when the CPU reads controller status. The commands written into the controller's slave memory addresses direct controller operations. When executing an operation, however, the controller functions independently of the CPU and the CPU cannot communicate with the controller except to check idle/busy status. After the controller completes an operation, it writes status information into the same memory locations that held the commands. Then the CPU can address the controller slave logic again to read these locations.

After a command has been initiated, the controller then may become a TILINE master. The controller contends for TILINE access on a positional priority basis by cycle-stealing with the CPU and with other active TILINE master devices. After it attains TILINE access, the controller transfers a 16-bit parallel data word to or from the slave it has addressed, which in most cases is a computer memory board. In addition, the controller manipulates all of the disk interface data and control lines that enable data transfer between the controller and the disk drive.

When data is read from the disk, an error detecting and correcting circuit, using error correcting code (ECC), examines the data and determines if any errors have occurred during the data storage process. If the controller determines that an error has occurred, it rereads the data a certain number of times to attempt to acquire error-free data. If it still reads an error from the disk, the controller determines if the error is correctable. If the controller finds that the error is one of the types that can be corrected, it then will make the correction. After an operation, the controller sets status indicators that show whether errors have occurred and whether corrections have been made. Although there is no guarantee that ECC will provide perfect records, the corrections that it makes offer the highest probability of data integrity.

1.3.3 Disk Drive Operations

The disk drive performs all data reading and writing functions upon operational commands exchanged solely with the disk controller. As shown in Figure 1-5, disk control commands, power sequence, data, and clock signals are fed directly to the disk drive. Status signals, data, and clock signals are returned to the disk controller when requested.

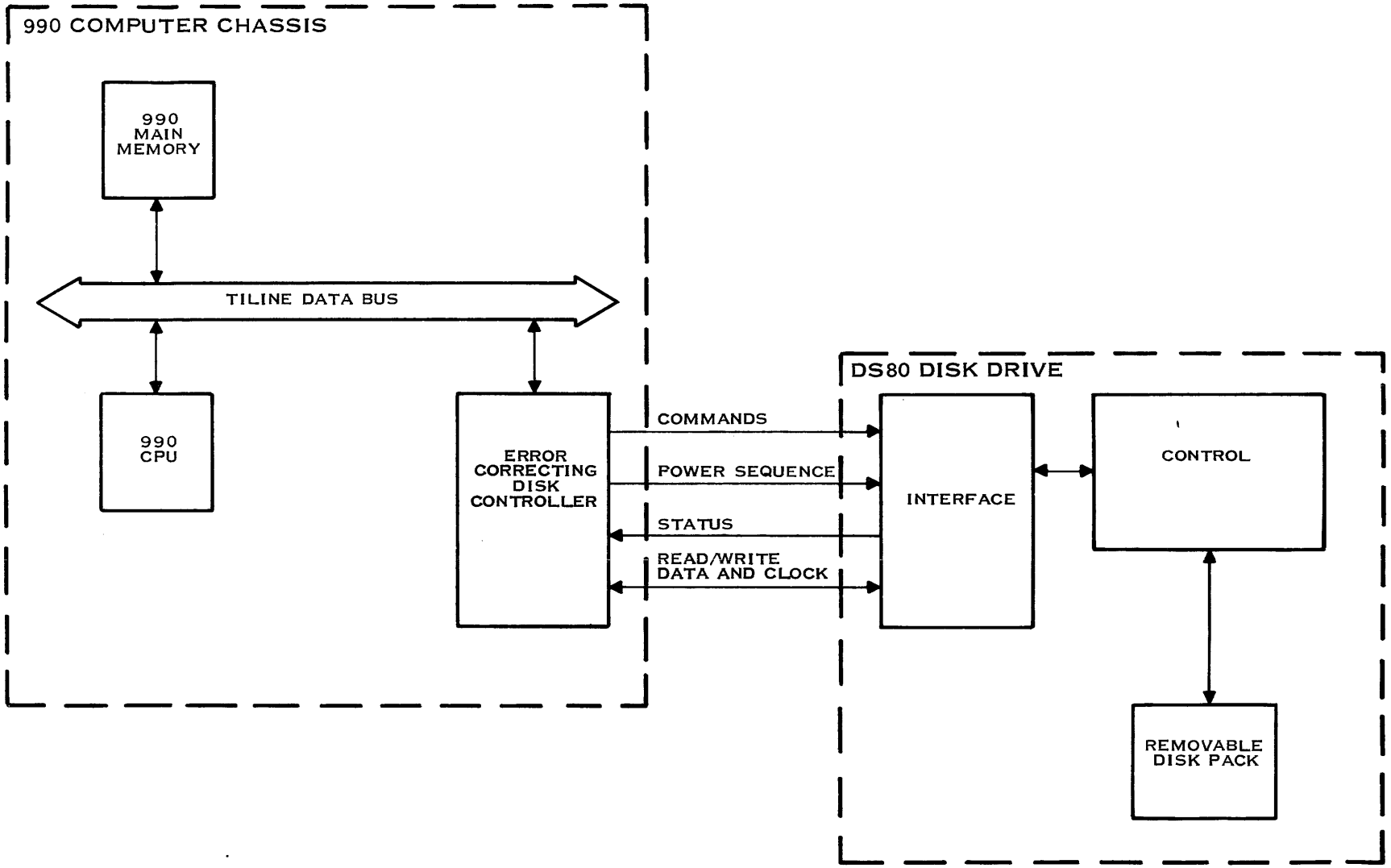


Figure 1-5. Disk Drive System Simplified Block Diagram

1.4 SYSTEM SPECIFICATIONS

Table 1-2 lists specifications for the DS80 disk system.

Table 1-2. Model DS80 Disk System Specifications

Characteristic	Specification
PHYSICAL	
Dimensions:	
Height	264 mm (10.4 in.)
Width	444 mm (17.5 in.)
Length	813 mm (32.0 in.)
Weight:	100 kg (220 lbs)
Number of platters:	5 (two protective, three operational)
Read/write heads:	5
Servo heads:	1
Unformatted bytes per drive:	82,152,000
Formatted bytes per drive:	62,698,240
Cylinders (including two diagnostic cylinders and ten spare cylinders):	815
Track density tracks/millimeters (track/inch):	14.6 (370)
Track spacing millimeters (inches):	0.0684 (0.0027)
ENVIRONMENTAL	
Temperature range:	
Storage/transit	– 40 °C to 70 °C (– 40 °F to 158 °F) 15 °C/hr maximum change
Nonoperating	– 40 °C to 70 °C (– 40 °F to 158 °F) 15 °C/hr maximum change
Operating	13 °C to 40 °C (55 °F to 104 °F) 10 °C/hr maximum change

Table 1-2. Model DS80 Disk System Specifications (Continued)

Characteristic	Specification
Humidity range:	
Storage/transit	5% to 95% relative, noncondensing 10% per hour maximum change
Nonoperating	5% to 95% relative, noncondensing 10% per hour maximum change
Operating	10% to 90% relative, noncondensing 10% per hour maximum change
Altitude:	
Storage/transit	-305 to 12192 meters (-1000 to 40000 feet)
Nonoperating	-305 to 12192 meters (-1000 to 40000 feet)
Operating	-305 to 2134 meters (-1000 to 7000 feet)
Vibration:	
Storage/transit	2.5 mm from 5 Hz to 20 Hz, 2 g from 20 Hz to 50 Hz, 3 g from 50 Hz to 500 Hz, (all three axes)
Nonoperating	2.5 mm from 5 Hz to 20 Hz, 2 g from 20 Hz to 50 Hz, 3 g from 50 Hz to 500 Hz, (all three axes)
Operating	.15 mm from 10 Hz to 60 Hz, 1 g from 60 Hz to 200 Hz, (all three axes)
Shock:	
Storage/Transit	20 g for 11 ms in all three axes and 40 g for 30 ms in the z axis only.
Nonoperating	20 g for 11 ms in all three axes and 40 g for 30 ms in the z axis only.
Operating	3 g for 11 ms at a rate of 2 half-sinewave shock impulses per second in all three axes.

Table 1-2. Model DS80 Disk System Specifications (Continued)

Characteristic	Specification

POWER REQUIREMENTS

Ac power input (disk drive) as supplied from the factory:

Voltage	Frequency	Phase	Amperes (start)	Amperes (run)
100 + 10, -15 V	50 (± 1) Hz	1	30 max	8.0
100 + 10, -15 V	60 (± 1) Hz	1	30 max	8.0
120 + 7, -23 V	60 (± 1) Hz	1	30 max	8.0
220 + 22, -33 V	50 (± 1) Hz	1	13 max	4.0
240 + 24, -36 V	50 (± 1) Hz	1	13 max	4.0

The following voltage tap options may be field selected to match available power:

Voltage tap	Voltage range
100	85 to 107
115	107 to 121
127	121 to 140

Dc power input (disk controller):

Voltage	Current (amperes)
+ 5.0	6.0
– 12.0	0.175

PERFORMANCE

Start time:	30 seconds
Stop time:	35 seconds
Seek time:	
Full	55 ms, maximum
Average	30 ms
Single track	6 ms, maximum
Transfer rate (burst from disk drive to controller):	9.6 MB/second (1.2MB/second)
Rotation speed:	3600 ± 180 rev/min

Table 1-2. Model DS80 Disk System Specifications (Continued)

Characteristic	Specification
Bit density:	239 bits/mm, (6060 bits/inch) nominal inner track
Rotational latency time:	8.33 ms average
Head switching time:	20 μs, maximum
Zero track seek time:	150 μs, maximum
Phase lock synchronization:	6 bytes, maximum
Write-to-read recovery (write gate off to read gate on):	20 μs, maximum
Read-to-write recovery (read gate off to write gate on):	300 ns maximum
Bit cell time:	103.3 ±5.0 ns
Bit rate (nominal):	9.677 Mhz (1.21MB/second)
Recording mode:	Modified frequency modulation (MFM)
Positioning error rate:	<1 in 10^9 seek executions
Audible noise power emissions:	NC63, maximum
CAPACITY	
Number of sectors/track:	61
Number of bytes/sector:	256
Total number of tracks (including ten diagnostic tracks and 50 spare tracks):	4075
Unformatted bytes per track:	20160
Number of addressable cylinders (including two diagnostic cylinders and ten spare cylinders):	815
Number of tracks per cylinder:	5
Total unformatted data storage bytes, excluding diagnostic cylinders:	81.95 MB

1.5 SYSTEM CABLING CONFIGURATIONS

Up to four disk drives in a daisy-chained configuration may be connected to the 990 computer for access via the TILINE data bus. The DS300 disk drive and the CD1400 disk drive also may be included in the daisy chain with the DS80 drive, but no more than a total of four disk drive units may be connected. Note that the CD1400 disk drive contains two logical drive units, so that only one CD1400 disk drive and one or two DS80 or DS300 drives may be connected to the same controller. Refer to the installation section of this manual for details on cabling the disk system.

2

Installation

2.1 GENERAL

This section provides preparation, unpacking, mounting, and cabling information for the Model DS80 disk system. Site requirements and initial verification procedures are detailed also.

Read this entire section before beginning because unusual circumstances may require that procedures be performed in an order different from that described.

CAUTION

Do not connect or disconnect any plug or circuit board when power is applied to the system since voltage transients may damage electronic parts.

Special tools and test equipment required for installing the DS80 disk system are listed in Table 2-1.

Table 2-1. Special Tools and Test Equipment

Tool	Part Number
Model T2000B exerciser	943849-1001
Model T2001A head alignment meter	943849-1002
Digital voltmeter	(Commercially available)
Head alignment disk pack	943849-1003
Scratch disk pack	943849-1004

2.2 SITE REQUIREMENTS

Refer to Section 1 for environmental conditions and limits. Pay particular attention to temperature, humidity, and air cleanliness specifications. Locate the disk drive away from smoking, food consumption, and high traffic areas. Avoid carpets and drapes since they produce lint, collect dust, and increase static discharge problems. Also, locate the drive away from printers, card punching machines, paper tape perforators and similar equipment since paper, carbon, and ink particles reduce the life of the drive air filter and increase chance of drive failure. In addition, install the drive away from windows that would allow direct sunlight to fall on the drive cabinet.

Cooling air is drawn in at the front of the disk drive and exhausted through the rear. Mount the disk drive on a secure tabletop or special pedestal, but take precautions to ensure adequate air flow.

2.3 PREPARATION FOR USE

The following paragraphs detail instructions for preparing the disk drive for use. These instructions include unpacking, inspection, shipping hardware removal, PWB preparation, disk controller preparation, CPU preparation, disk drive mounting, cabling, grounding, and verification before applying power.

A checklist is provided on the following page to assist the user in ascertaining that all necessary preparations have been made prior to using the disk system.

2.3.1 Unpacking

The following paragraphs describe unpacking procedures for the disk drive and disk pack.

2.3.1.1 Unpacking the Disk Drive. The disk drive is shipped attached to a skid and packaged as shown in Figure 2-1. The disk controller and accessories are packed in an accessory carton with the disk drive. Inspect packaging for evidence of abuse immediately upon receipt. After preliminary inspection and opening, perform a parts inventory.

NOTE

Save the shipping cartons and packing materials for reshipment of the disk drive, if required.

CAUTION

To avoid equipment damage, exercise care using tools during unpacking.

Unpack the disk drive according to the following procedure:

WARNING

All personnel should stand clear when the steel straps holding the crate together are cut. Flying loose ends of the strap can cause injury.

1. Remove the steel strapping and open the top flaps.
2. Remove the two spacers from the top of the inner container. Also, remove any loose items packed between the inner and outer containers.

Preparation for Use Checklist

Task	Initials
1. Unpacking and parts inventory complete (paragraph 2.3.1)	_____
2. Inspection complete (paragraph 2.3.2)	_____
3. Shipping material removed (paragraph 2.3.3)	
a. Rear shipping bolt	_____
b. Wooden shipping spacer	_____
c. All glass securing tape and carriage restraints	_____
4. Disk drive PWB preparations (paragraph 2.3.4)	
a. Interface (I/O) board INTERFACE/DEGATE switch and unit number switches set (paragraph 2.3.4.1)	_____
b. Logic III circuit board jumpers installed (paragraph 2.3.4.2)	_____
5. Disk controller TILINE address switches set (paragraph 2.3.5)	_____
6. 990 computer chassis preparations (paragraph 2.3.6)	
a. Slot selected and controller installed	_____
b. Access granted jumper installed	_____
c. Interrupt connected	_____
7. Cabling and connections (paragraph 2.3.8)	
a. I/O cables installed and routed	_____
b. Terminator board installed in last drive	_____
8. Ac power connections (paragraph 2.3.9)	
a. Supply voltage measured and jumper properly installed	_____
b. Terminal board TB1 connections checked	_____
9. Verification before applying power (paragraph 2.3.10)	
a. Logic boards firmly seated	_____
b. Connectors firmly seated	_____
c. Cables checked	_____
d. Overall inspection complete	_____
e. Air filter checked	_____
f. Ac power connections checked	_____
g. Grounding checked	_____

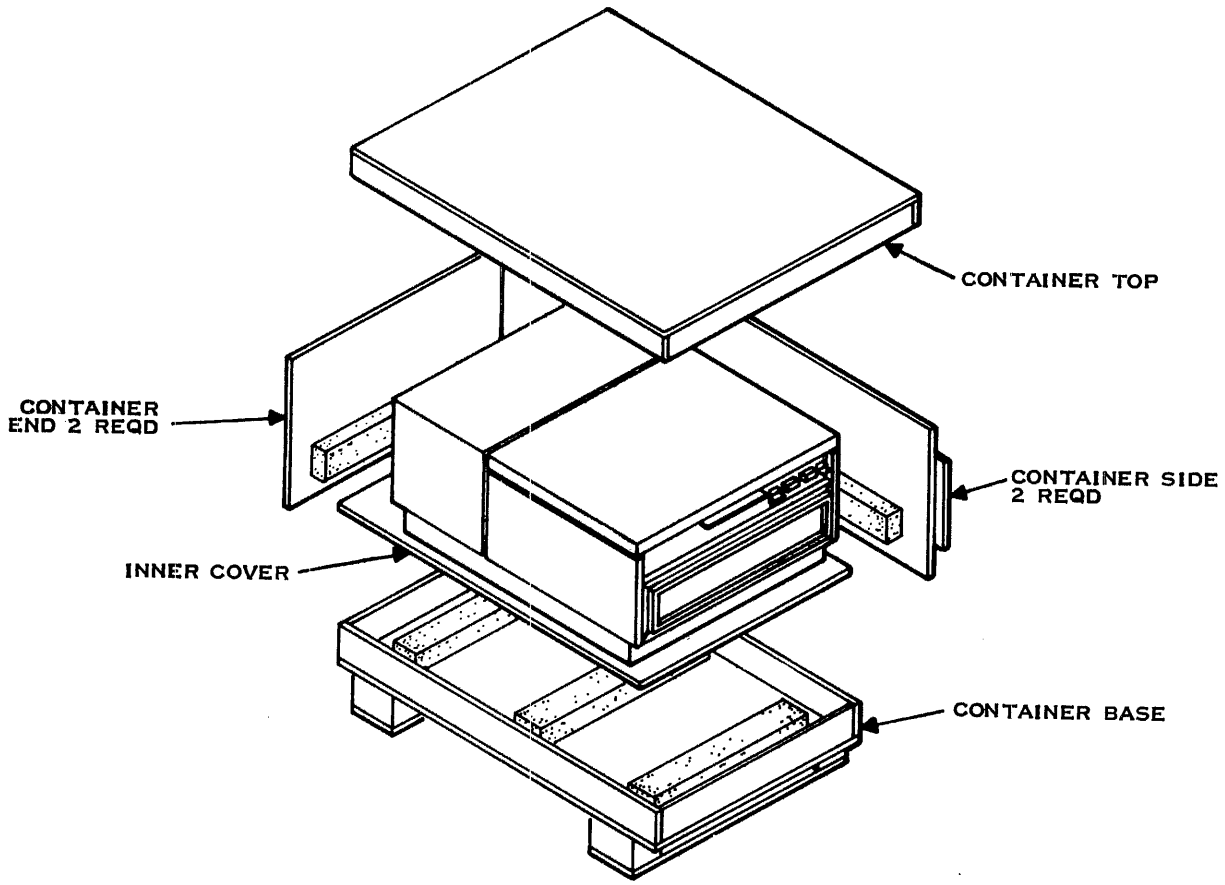


Figure 2-1. Disk Drive Shipping Configuration

CAUTION

Use care not to damage the equipment when using knives or other sharp tools to open shipping containers.

3. Cut through the tape along the top of the inner container and open the top flaps.
4. Cut down and through the four corners of the outer container so that the four sides can be laid flat.
5. In the same way, cut down the sides of the inner container.
6. Remove and retain any loose items that may be packed between the inner container and the disk drive.

7. Remove the cardboard collar surrounding the drive. The plastic-enclosed drive is now fully accessible. Remove the tape that holds the plastic sheeting to the plywood base, but leave the sheeting in place to protect the drive finish.

8. Slide the front end of the drive, the plywood base, and the packing containers over the edge of the supporting bench just far enough to bend down the cardboard container and to remove the bottom front spacer.

9. On the bottom of the plywood base, locate the two machine bolts that attach the base to the front of the drive frame. Remove both bolts.

10. Slide the rear end of the drive, the plywood base, and the packing containers over the edge of the support surface just far enough to remove the remaining bottom spacer and the two bolts that attach the back of the drive frame to the plywood base. Remove both bolts.

WARNING

If a lifting hoist is not available, at least three people are required to lift the disk drive, which weighs 100 kg (220 lbs). To avoid backstrain or other injury, use extreme care when lifting the unit.

11. Lift the disk drive free of its plywood base and other packing materials, preferably using a hoist as described in the following steps. Refer to Figure 2-2.

12. If a lifting hoist is available, use the two wide grooves cut in the top of the plywood base to accommodate the webbing or lifting straps. Raise one end of the drive at a time and slip the lifting straps under the drive at these grooves. Maintain the loop diameter of the lifting straps using a cradle or lifting bar.

13. Place several layers of corrugated cardboard between the top edges of the drive and each strap to protect the top covers when lifting the drive.

14. Lift the drive slightly and check for balance. (The center of gravity is toward the rear of the drive.) Readjust if necessary.

15. Lift the drive free of the plywood base and other packing material.

16. Move the drive to the checkout workstation or final installation location.

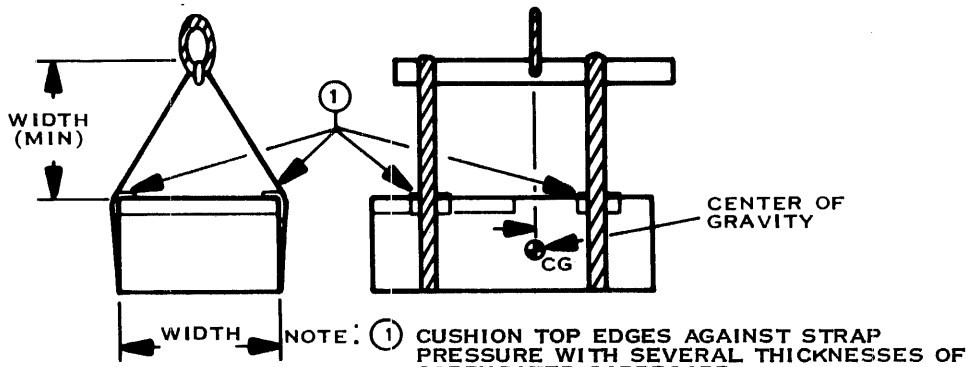


Figure 2-2. Hoisting the Disk Drive

2.3.1.2 Unpacking the Disk Pack. Open the shipping container and unpack the disk pack as follows:

CAUTION

Disk packs are precision instruments built to tolerances less than one micrometer. Exercise caution in handling and storing disk packs to protect valuable data and prevent costly rerun time.

1. Inspect the shipping container for any evidence of damage, such as a crushed corner or torn or open holes in the carton.

2. Remove the disk pack from the shipping carton and the protective bag. Remove the pack from the bottom cover; turn the pack upside down on the top cover and inspect the bottom protective disk. Look for dents or scratches.

3. Carefully clean the inside of the disk pack canister top and bottom covers with a clean, lint-free cloth moistened with water or isopropyl alcohol. Ensure that no foreign matter enters the disk area.

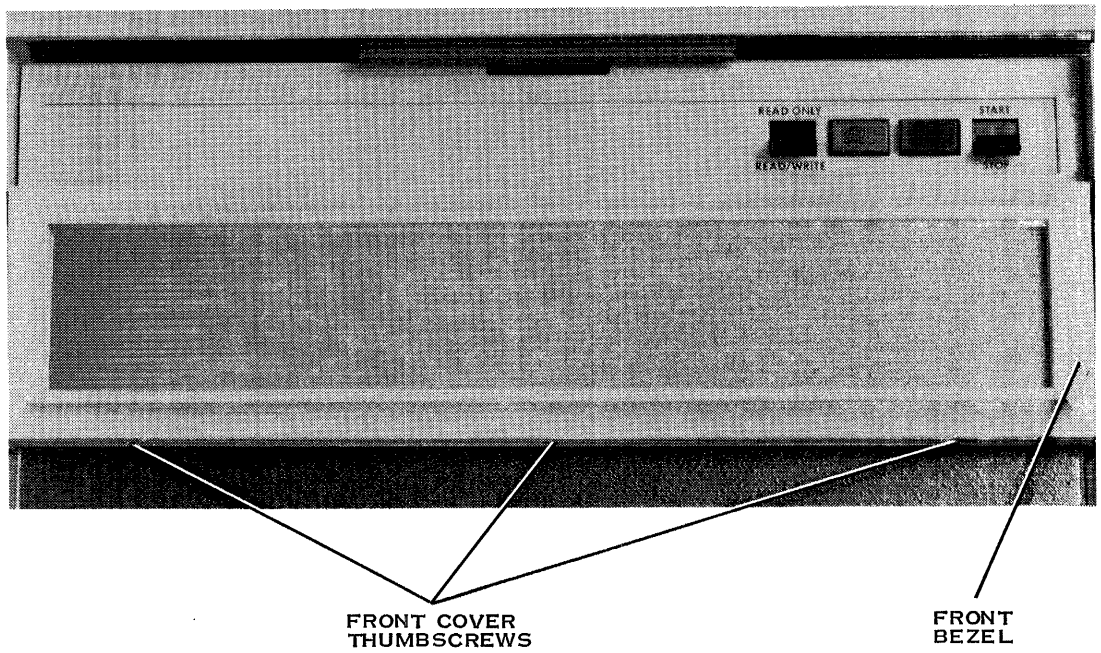
4. Always keep the top and bottom covers of the canister together when the pack is in use. Dust and lint that can later contaminate the pack can accumulate in an open canister.

5. Never use a disk pack that is suspected of being damaged, because it can cause further damage to the disk drive.

2.3.2 Inspection

Remove the disk drive front cover by unscrewing the three thumbscrews under the front bezel (Figure 2-3). Pull the front cover straight forward until it clears the drive. Remove the rear cover by unscrewing the two rear cover screws (Figure 2-4). Slide the cover to the rear; lift it up and off the chassis.

Check interior items such as PWBs, carriage assembly, and read/write heads for shipping damage. Also check for broken or cracked castings, broken harnesses, or loose fixtures. Contact carrier immediately upon discovery of shipping damage.



2278380

Figure 2-3. Disk Drive Front View

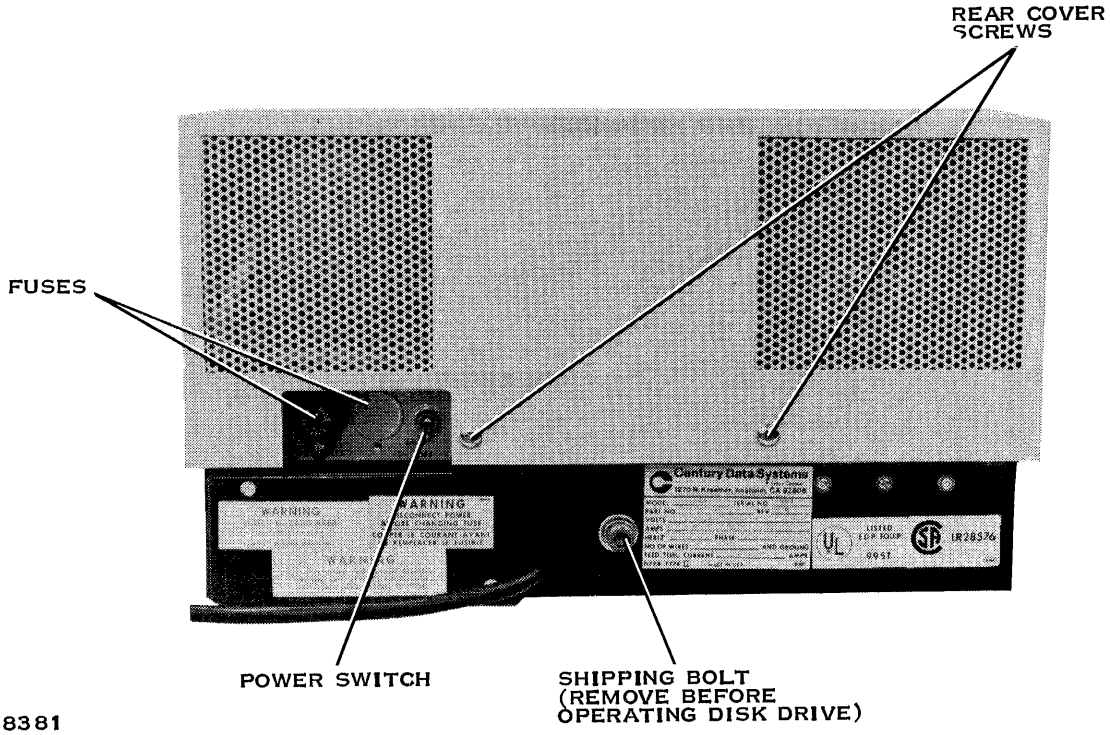


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Figure 2-4. Disk Drive Rear View

2.3.3 Shipping Hardware Removal

Remove the shipping bolt and internal shipping materials by performing the following procedure:

NOTE

Power must be applied before opening the disk pack cover.

1. Refer to Figure 2-4. Remove the shipping bolt, lockwasher, and flat washer located at the center of the disk drive rear panel using a 5/16-inch Allen wrench.

2. Remove the wooden shipping spacer between the linear motor and the bottom casing (Figure 2-5). The spacer is located to the right of the shipping bolt removed in the previous step.

CAUTION

Use extreme caution when removing the head locking bracket. Do not allow the bracket to touch the heads. Do not allow any contamination to remain in the air shroud after removing the bracket. Ensure that no metal filings from the screws are left in the air shroud area.

3. Open the air shroud cover and remove the four screws that secure the bottom cover plate (see Figure 2-5A) to the air shroud.

4. Carefully lift the plastic bracket (Figure 2-5A) up and away from the carriage. Do not allow the bracket to contact the heads.

5. Replace the bottom cover plate and clean the interior of the air shroud, if necessary. Ensure that there is no contamination left in the disk pack area.

6. Remove any tape or other packing material from inside the disk pack area. Manually rotate the spindle to ensure that it turns freely.

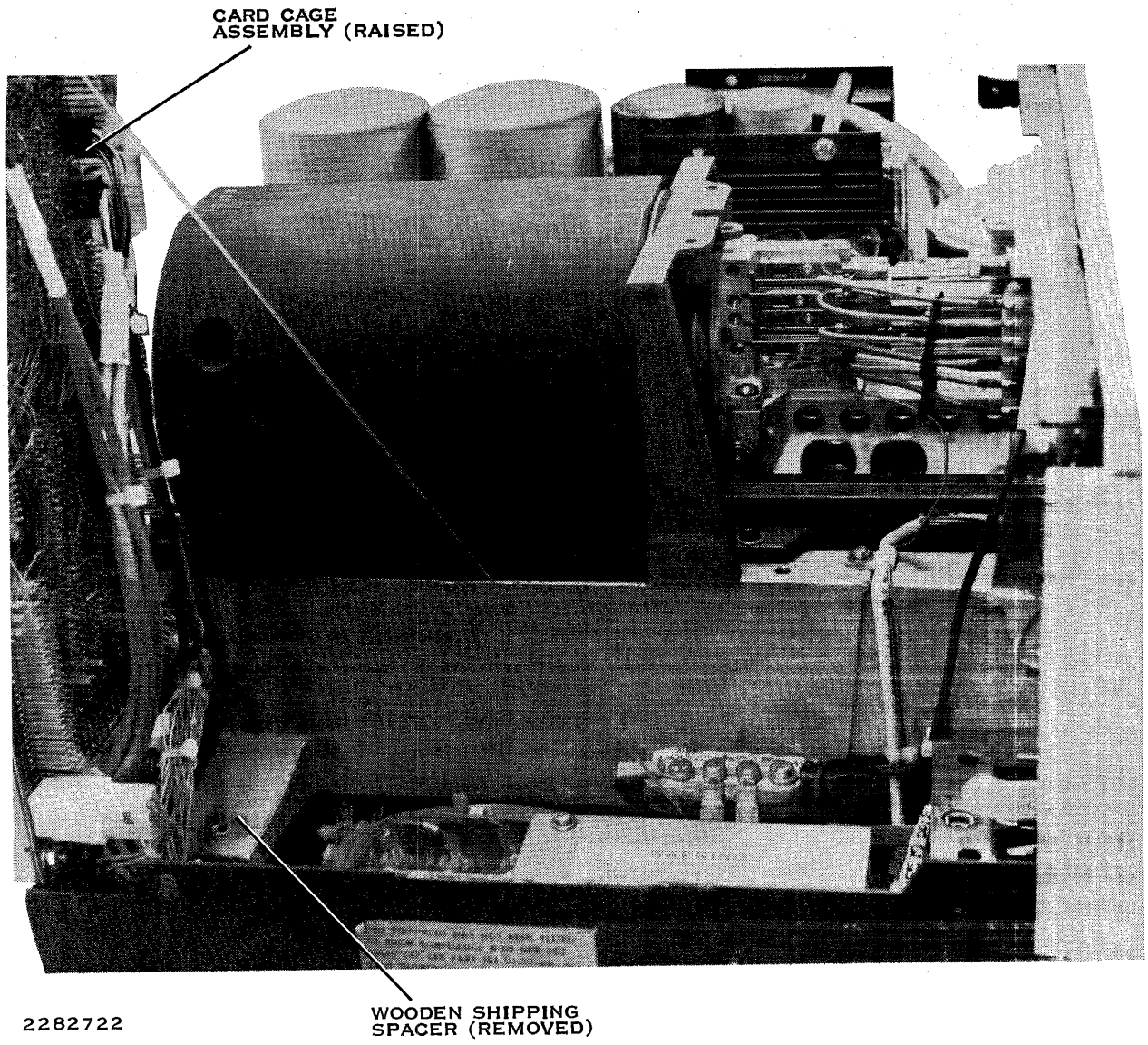


Figure 2-5. T-Block Assembly Shipping Restraints

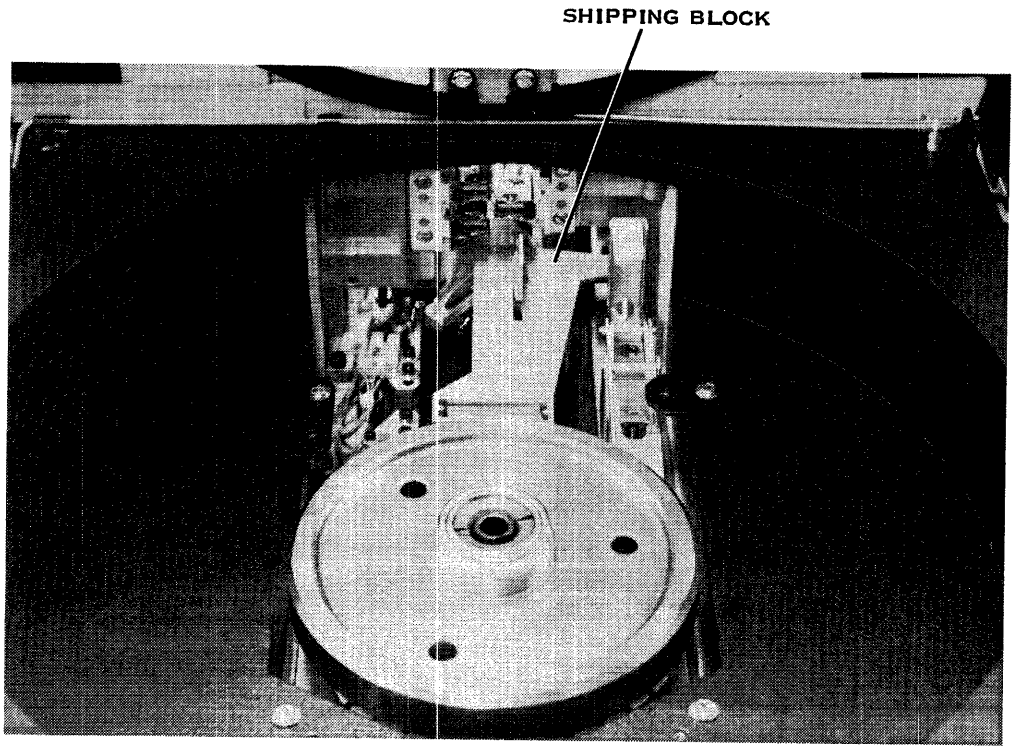


Figure 2-5A. Head Carriage Shipping Restraint

2.3.4 Disk Drive PWB Preparations

The following paragraphs detail preparations to the PWBs in the disk drive that must be completed before operating the system. If the disk drive has been shipped as a complete system, these preparations have been made; however, it is recommended that the boards be checked before operation.

2.3.4.1 Interface (I/O) Board Preparations. The interface board, (Figure 2-6), contains unit number selection switches and the INTERFACE/DEGATE switch. Both switches must be set correctly before use.

INTERFACE/DEGATE Switch. The INTERFACE/DEGATE switch disconnects the disk drive from the controller for certain maintenance operations. The INTERFACE position enables normal, online operation, permitting the disk drive to be powered-up and selected by the controller. The DEGATE position disconnects the disk drive from the controller and enables inputs from the T2000A/B exerciser for maintenance operations. For normal operation, verify that the switch is in the INTERFACE position.

Unit Selection Switch. The unit selection switch, S1, selects the unit number for each drive in the system. Typically, the drive in a single drive system will be designated unit 0, and each additional drive designated the next higher number in sequence. Note that no two drives should be designated with the same drive number, and no more than four drives may be connected in a daisy-chained configuration to a single controller.

Assign unit numbers to each drive in the system by setting switch S1 corresponding to Table 2-2. Note that when the actuator for each switch position is pushed down on the side marked OPEN, the switch is off; when the actuator is pushed down on the unmarked side (opposite to the side marked OPEN), the switch is on.

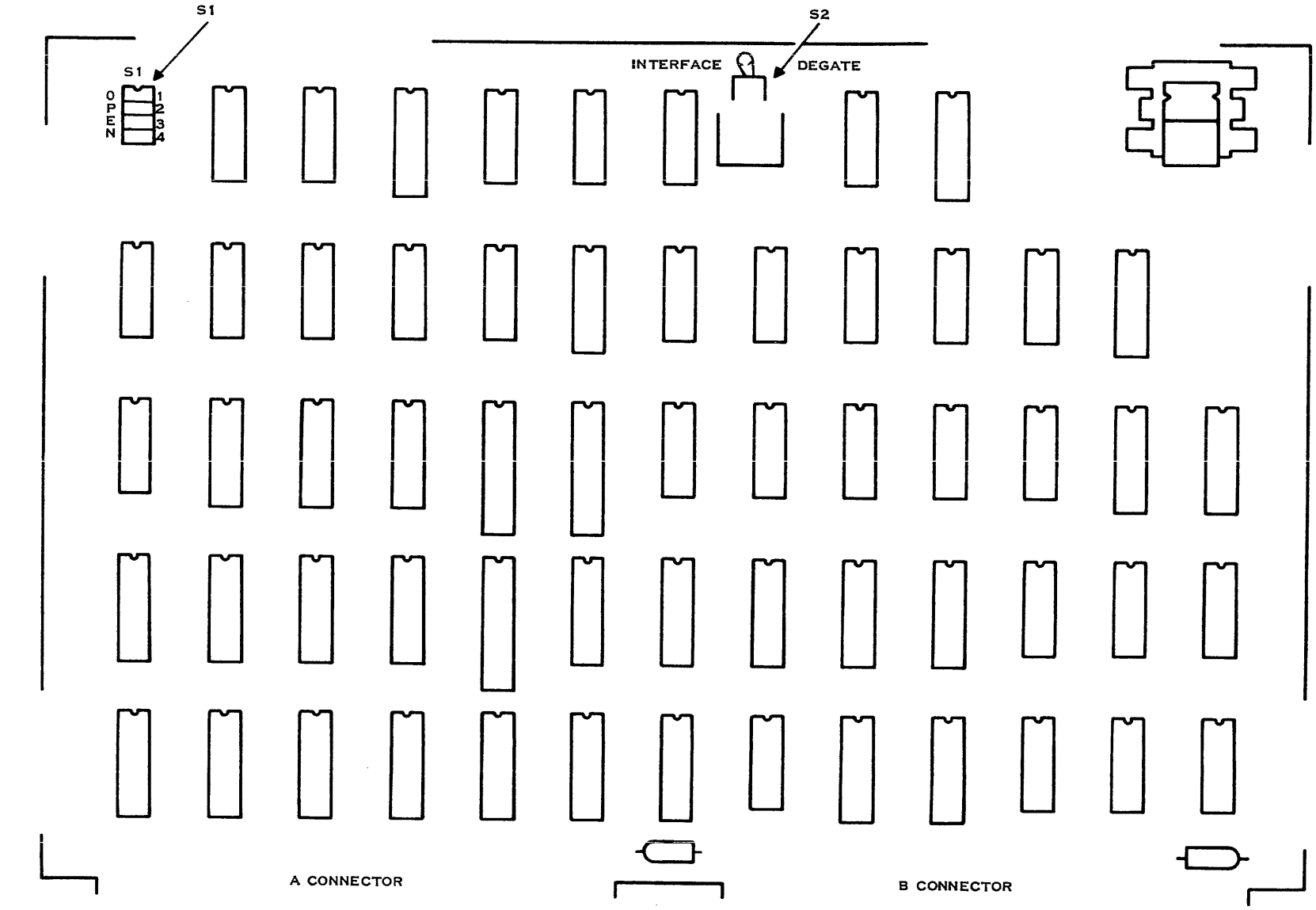


Figure 2-6. Interface (I/O) Board Switch Settings

Table 2-2. Unit Selection Switch Positions

Unit Number	Switch S1 Number/Position 1	2	3	4
0	ON	ON	ON	OFF
1	ON	ON	OFF	ON
2	ON	OFF	ON	ON
3	OFF	ON	ON	ON

Note:

When the actuator is pushed down on the side marked OPEN, the switch is OFF; when pushed down on the unmarked side, the switch is ON.

2.3.4.2 Logic III Board Jumper Configurations. The logic III circuit board contains jumpers that establish the sector length on a disk at 61 sectors per track. Check the jumpers on the board to ensure that they are installed correctly according to the following procedure.

1. Remove the logic III circuit board assembly from card cage slot 5 (Figure 2-7).

2. On the circuit board, locate IC sockets 6A and 6B that are used as jumper connectors. Figure 2-7 shows the socket locations. Install or verify the presence of the jumpers shown in the figure. Check that only those jumpers listed are installed.

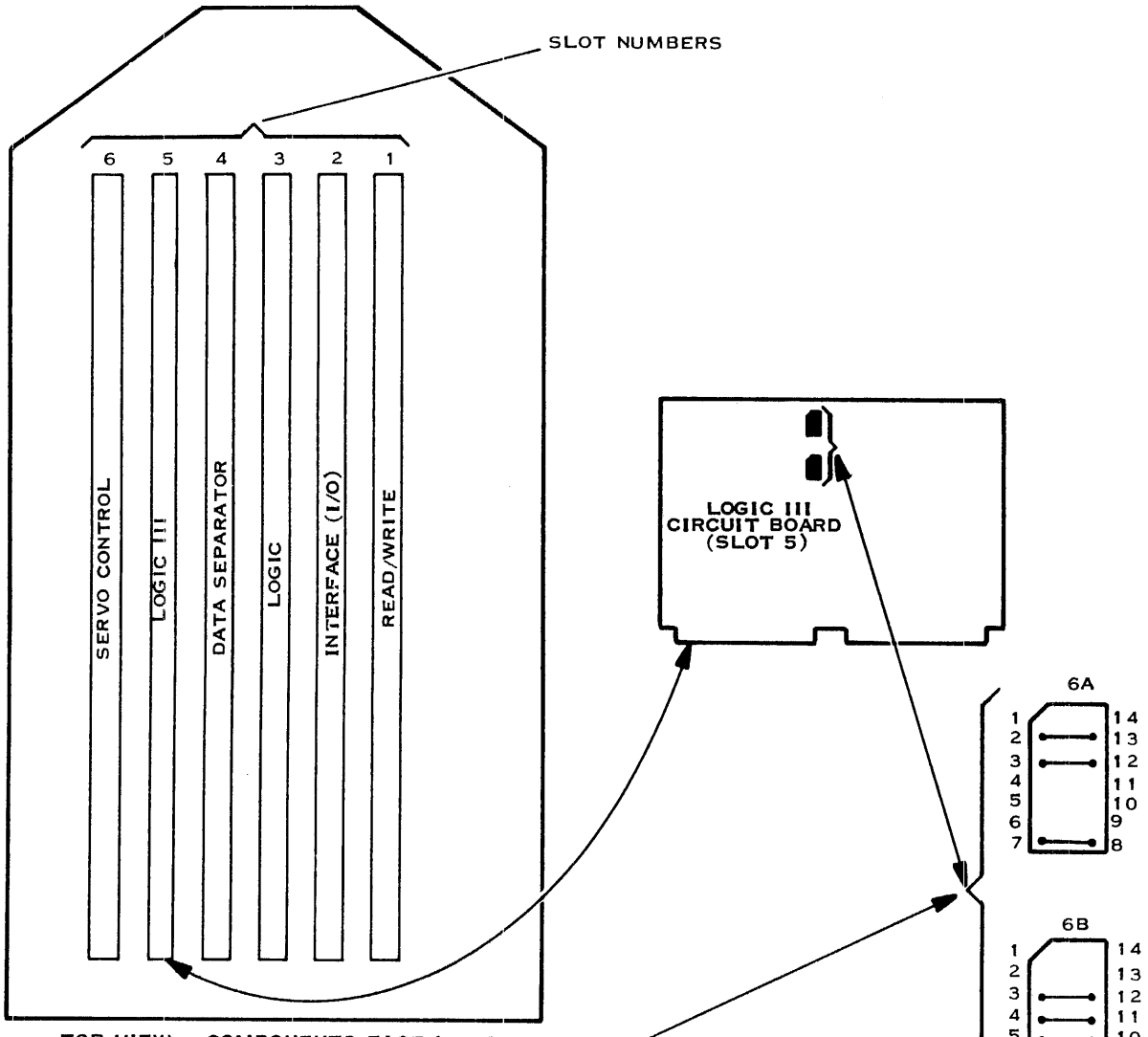
3. Reinstall the logic III circuit board.

2.3.5 Disk Controller Preparations

The CPU incorporates the disk controller into addressable memory space for access via the TILINE. Switches on the disk controller determine the TILINE base memory address and must be set correctly before use. If the disk drive system was shipped as part of a complete system, these switches have been set already, but should be verified before operation. The following paragraphs describe this procedure.

Figure 1-2 shows the disk controller and switch locations. Figure 2-8 lists the TILINE addresses, CPU byte addresses, and corresponding switch positions for each of these addresses. The standard main 990 computer chassis slot assignment for the disk controller is slot 7 for the 13-slot chassis and slot 11 for the 17-slot chassis. The standard CPU byte address is >F800 (all switches in the off position).

If these switches need setting, determine the proper TILINE address according to the operating system software, and set the switches as shown in Figure 2-8. This completes disk controller preparations.



ADD JUMPERS

SOCKET	JUMPER PINS
6A	2 – 13 3 – 12 7 – 8
6B	3 – 12 4 – 11 5 – 10 6 – 9

REMOVE JUMPERS (IF ANY)

SOCKET	PINS
6A	1 – 14 4 – 11 5 – 10 6 – 9
6B	1 – 14 2 – 13 7 – 8

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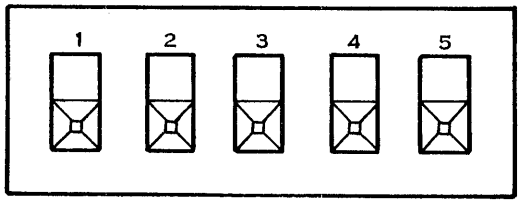
Figure 2-7. Jumper Configuration, Logic III Circuit Board



SWITCHES SHOWN SET AT CPU BYTE ADDRESS $F800_{16}$

TILINE WORD ADDRESS (HEXA-DECIMAL)	CPU BYTE ADDRESS (HEXA-DECIMAL)	SWITCHES					
		1	2	3	4	5	
FFC00	F800	OFF	OFF	OFF	OFF	OFF	DISK CONTROLLERS
FFC08	F810	OFF	OFF	OFF	OFF	ON	
FFC10	F820	OFF	OFF	OFF	ON	OFF	
FFC18	F830	OFF	OFF	OFF	ON	ON	
FFC20	F840	OFF	OFF	ON	OFF	OFF	
FFC28	F850	OFF	OFF	ON	OFF	ON	
FFC30	F860	OFF	OFF	ON	ON	OFF	
FFC38	F870	OFF	OFF	ON	ON	ON	
FFC40	F880	OFF	ON	OFF	OFF	OFF	OTHER TILINE SLAVES
FFC48	F890	OFF	ON	OFF	OFF	ON	
FFC50	F8A0	OFF	ON	OFF	ON	OFF	
FFC58	F8B0	OFF	ON	OFF	ON	ON	
FFC60	F8C0	OFF	ON	ON	OFF	OFF	
FFC68	F8D0	OFF	ON	ON	OFF	ON	
FFC70	F8E0	OFF	ON	ON	ON	OFF	
FFC78	F8F0	OFF	ON	ON	ON	ON	

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Figure 2-8. TILINE Address Switch Configurations

NOTE

If the disk drive system was purchased as part of a complete Texas Instruments 990 Computer System, computer chassis preparation (paragraphs 2.3.6. through 2.3.6.4) is not necessary. In this case, proceed to paragraph 2.3.7.

2.3.6 990 Computer Chassis Preparation for the Disk Controller

The following paragraphs describe 990 computer preparations unique to the Model DS80 disk system. This material is abstracted from the chassis preparation instructions in the computer hardware reference manuals. Refer to the preface for formal titles and part numbers of hardware reference manuals for the 990/5, 990/10, and 990/12 computers.

If the disk controller is shipped as part of a 990 computer system, computer chassis preparation is done at the factory. The controller is assigned a slot location, the interrupt jumpers are installed, and the TILINE access-granted (TLAG) jumpers/switches are correctly set. In this case, after the controller switch settings are verified, the hardware is compatible with the supplied software.

2.3.6.1 Selecting a Chassis Slot for the Controller. Chassis slot selection is based upon interrupt level and TILINE priority considerations. Each of the DS990 package systems already incorporates a planned growth path that specifies preferred slot locations, interrupt levels, and TILINE base addresses for standard peripheral controllers.

Interrupt assignments and TILINE address switch settings must be coordinated with the operating system software by system generation (SYSGEN) procedures. Refer to SYSGEN instructions in operating system documentation upon completion of hardware installation.

2.3.6.2 TILINE Philosophy. The TILINE is a common data path that is connected to all slot positions in the 990 chassis. Users of this bus fall into two major types, masters and slaves. Slave devices are addressed by master devices and commanded to accept or transmit data. Some TILINE peripherals, including the disk controller, have both master logic and slave logic.

In order to resolve conflicts between multiple masters contending for TILINE control, a positional priority scheme is used. The TLAG signal that establishes positional priority among masters is wired along the P2 side of the computer chassis. The TILINE master installed in the highest-numbered slot has the highest priority, and priority decreases with each slot toward the central processor location (slot 1).

The TLAG signal from a higher priority master enters each master on P2, pin 6. The signal leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers are installed on the backpanel to assure line continuity across slots not occupied by masters. Additional masters may be inserted at slot positions of higher or lower priority by opening the jumper between P2-5 and P2-6 (TLAG) for the selected slot location. Installing a board with TILINE master logic, such as the disk controller, requires that:

- The TLAG jumper (P2-5 to P2-6) be opened for the chosen slot. Opening a TLAG jumper consists of either:
  - — Physically pulling out a jumper (current 6-slot, 13-slot chassis)
  - — Cutting a jumper wire or etch (older 6-slot, 13-slot chassis)
  - — Setting a jumper switch to OFF (17-slot chassis)
- Continuity of the TLAG lines between the highest priority master and the central processor board must be preserved. This means that if an intermediate slot is assigned to a TILINE master, that master must be installed to preserve continuity and to allow the priority system to function. It also means that the jumpers must be in place (or jumper switches ON) for all slots not occupied by TILINE couplers or TILINE device controllers.

2.3.6.3 Preparing a 990 Chassis Slot Location for the Disk Controller. Jumper locations and modification procedures differ between versions of the 990 chassis, as described in the following paragraphs.

Slot Preparation — Current Production, 6-slot and 13-slot Chassis. Current production units have the TLAG jumpers accessible from the connector side of the motherboard, as shown in Figure 2-9 (6-slot) and Figure 2-10 (13-slot). For these units, perform the following steps.

1. Turn off power and unplug the ac line cord.
2. Remove any circuit boards necessary for access by rocking the plastic ejector tabs firmly. Note the locations and orientation of the boards so they may be properly reinstalled.
3. Remove the access-granted jumper plug for the selected location.
4. If interrupt levels are to be changed, refer to paragraph 2.3.6.4.
5. Reinstall the circuit boards in the proper locations. Check the configuration label on the chassis to ensure that the boards are installed in the correct slots.
6. Record the new slot assignment on the configuration chart affixed to the chassis.

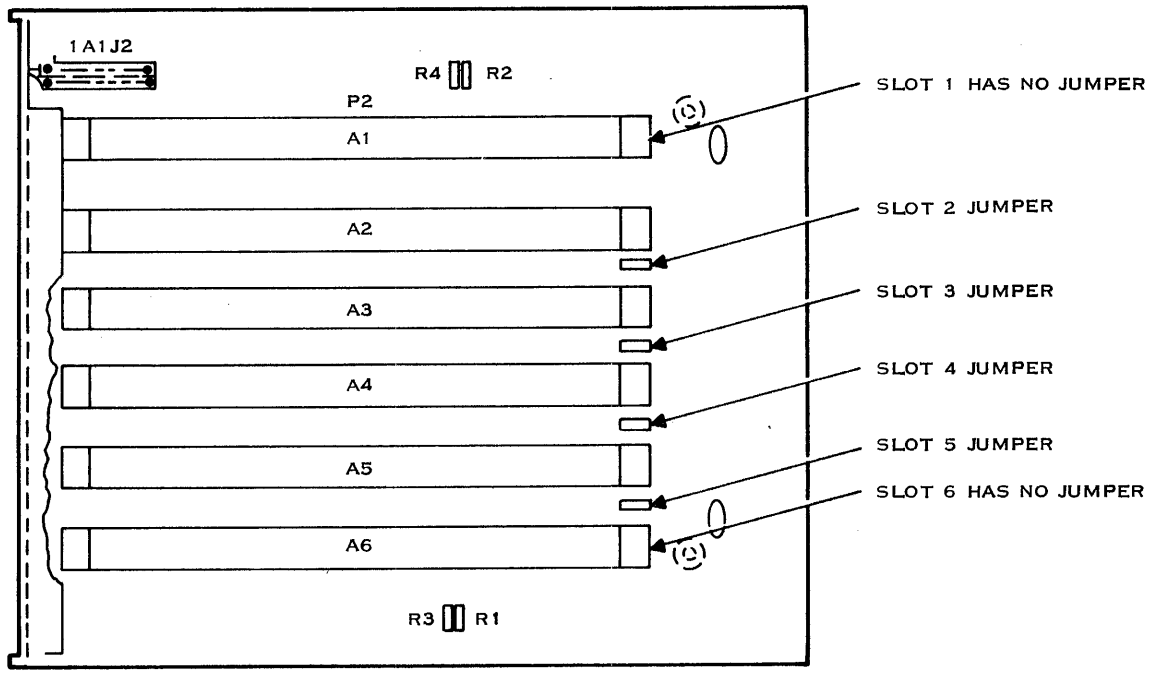


Figure 2-9. TLAG Jumper Locations for 6-Slot Chassis (Current Production)

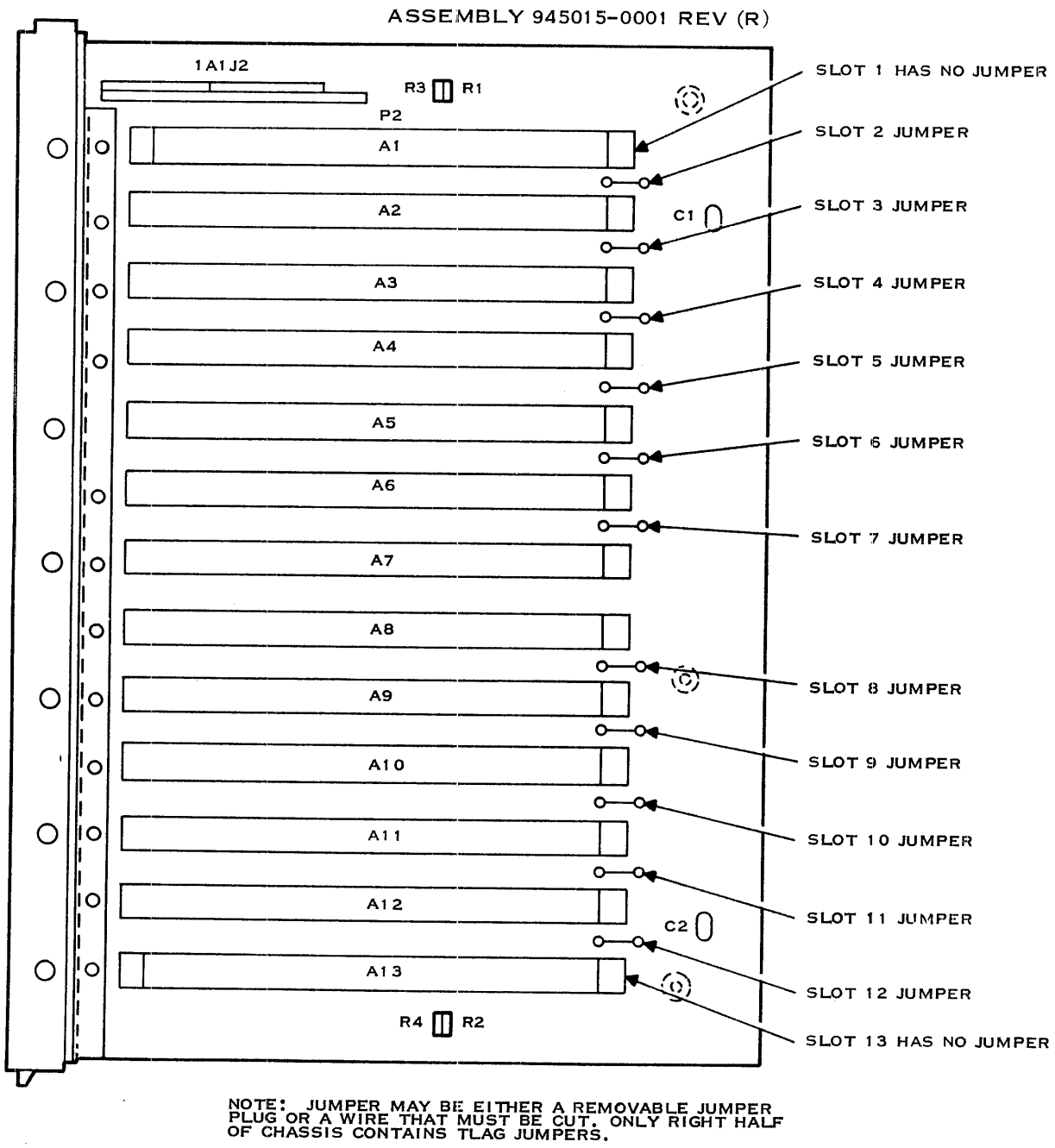


Figure 2-10. TLAG Jumper Locations for 13-Slot Chassis (Current Production)

Slot Preparation — Early Production, 6-Slot and 13-Slot Chassis. If the chassis is an early production version (i.e., it does not have jumpers as shown in Figure 2-9 or Figure 2-10, remove the back cover and power supply to gain access to the TLAG jumpers. For these chassis, the following steps should be followed:

1. Turn off power and unplug the ac line cord.

WARNING

Lethal voltages are exposed when the access cover is removed. The power supply capacitor may retain charges long after ac power is removed.

2. Remove the left access cover (as viewed from the front of the chassis). The cover is fastened by four or six hex-head machine screws.

3. If the chassis is a 13-slot unit with a 20-ampere power supply, slots 1-6 are visible above the power supply. In this case, proceed to step 5.

4. Remove the power supply as follows:

   a. Disconnect color-coded connectors from the component side of the power supply board.

   b. Unscrew the machine screws and standoffs that secure the power supply and RF shield to the frame and to the motherboard.

   c. Carefully pull the power supply board straight forward until the connector at the bottom center of the power supply board is disengaged from the pins protruding from the motherboard. Lift the power supply board out of the chassis.

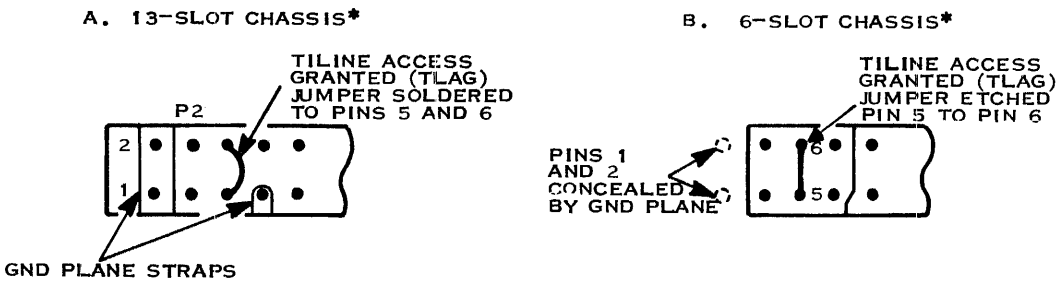
   d. Remove the RF shield.

5. The rear of the motherboard is now exposed. The P2 connectors are at the left side, closest to the fan. Figure 2-11 gives detailed views of the left end of the P2 connector in a 13-slot and a 6-slot chassis.

   In a 13-slot chassis, the TLAG jumpers (P2-5 to P2-6) are wire loops soldered to the connector. Pins 1 and 2 are concealed by the ground plane.

   To remove a jumper in the 13-slot chassis, clip the wire loop in two places and remove the excess wire. To remove a jumper in the 6-slot chassis, cut the jumper etch at two points with a sharp knife and lift or scrape away the excess conductor.

   To install a jumper, solder a short length of #26 AWG wire between P2-5 and P2-6.



*NOTE THESE ARE REAR VIEWS OF THE 990 MOTHERBOARD, I.E., VIEWS FROM THE POWER SUPPLY SIDE.

2277303

Figure 2-11. TLAG Jumpers on Early Production 6-Slot and 13-Slot Chassis

6. To reinstall the power supply, proceed as follows:

CAUTION

The male pins protruding from the lower center of the motherboard will bend if the mating connector on the power supply is not properly aligned with these pins.

   a. Slip the power supply over the cable harness and into the side of the chassis. The metal shell jumper connector (for the standby power supply) should appear at the bottom center of the power supply board.

   b. Align the power supply circuit boards on the two alignment pins and carefully slide the board straight back so that the pins protruding from the motherboard slip into the connector on the power supply circuit board. View of these pins is blocked by the power supply board.

   c. Reinstall the machine screws and standoffs that hold the power supply and RF shield in place. Do not omit the lockwashers because both mechanical and electrical connections are made by the machine screws and standoffs.

   d. Reconnect the power supply to the wiring harness by installing the color-coded plastic connectors.

7. Replace the access cover and secure it with machine screws.

8. Record the new slot assignment on the configuration chart affixed to the chassis.

9. Refer to paragraph 2.3.6.4 for interrupt connections.

Slot Preparation — 17-Slot Chassis. Continuity of the TLAG jumpers in the 17-slot chassis is controlled by two socket-mounted dual inline package (DIP) switches, each with eight individual switch sections. These switches are accessible from the rear of the 17-slot chassis (Figure 2-12). To check or set these switches, perform the following steps.

1. Turn off power and unplug the chassis ac line cord. Allow about 30 seconds for the power supply bleeders to discharge the power supply capacitors.

WARNING

Opening the chassis rear cover (power panel) exposes high voltages if the ac line cord is installed in a power socket. Do not contact the large filter capacitors on the power module.

CAUTION

The wire hinges on the chassis rear cover do not allow the cover to pivot beyond 90 degrees. Attempts to open the chassis rear cover beyond 90 degrees may damage the hinge mountings.

2. Using a coin or flat-bladed screwdriver, release each of the 11 quarter-turn latches on the chassis rear cover. Pull the cover straight back 38 millimeters (1.5 inches) to extend the wire hinges, and then open the cover to the 90-degree position. The hinges are on the right as viewed from the rear of the chassis.

3. Figure 2-13 shows the correspondence between switch sections and chassis slots. Set the appropriate switch segment OFF for any slot that is assigned to a TILINE master device, such as the disk controller. All other switch segments should be ON.

4. Refer to paragraph 2.3.6.4 if interrupt assignments are to be changed.

CAUTION

There is a possibility of interference between heat sinks in the chassis and modules mounted inside the rear access cover as the door is closed. Do not force the door closed if resistance is felt.

5. Rotate the door to fully extend the hinges and to a position parallel to the rear of the chassis. Grasp the rear access cover at the left and right sides and push it straight back to its mounting position against the chassis.

6. Using a coin or screwdriver, lock the 11 quarter-turn latches that hold the access cover in position.

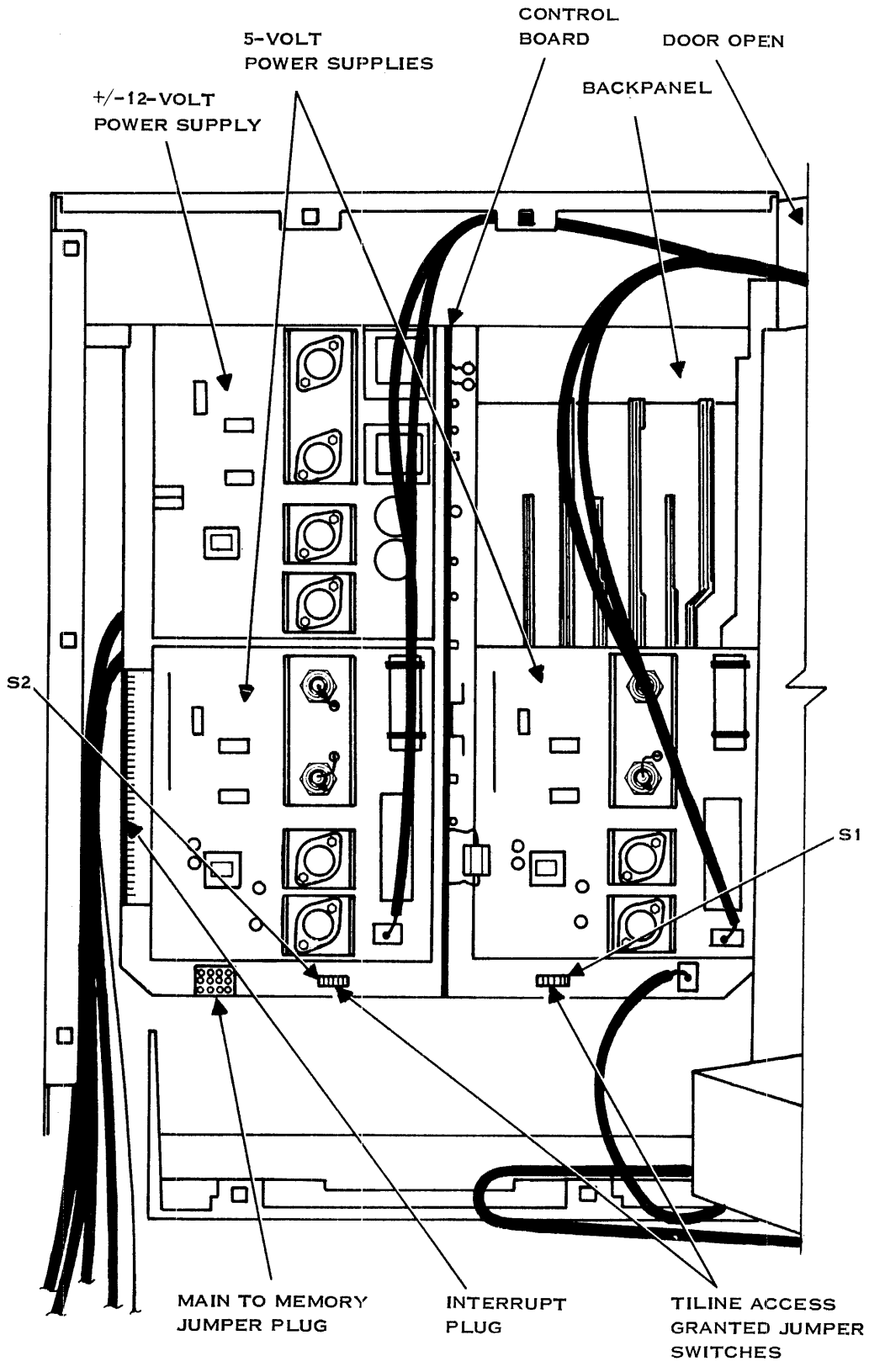


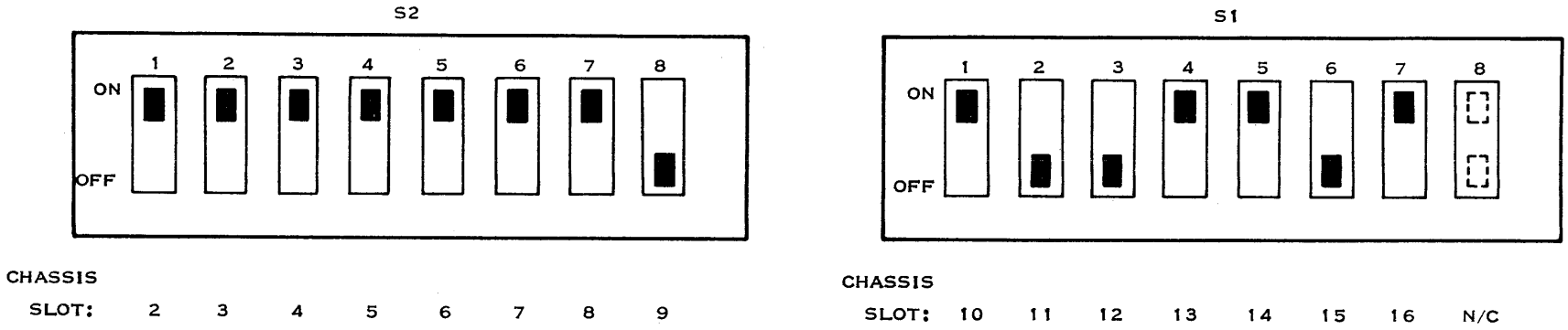
Figure 2-12. Interrupt Plug and TLAG Jumper Switches in the 17-Slot Chassis

17 – SLOT CHASSIS

TILINE ACCESS GRANTED (TLAG) JUMPER SWITCHES

ON = TLAG JUMPERED ACROSS SLOT (P2-6 TO P2-5)

OFF = TLAG NOT JUMPERED – CONTINUITY REQUIRES TILINE CONTROLLER



NOTES: 1. SWITCHES ARE SHOWN SET FOR:

FCCC	– SLOT 9
SYSTEM DISK CONTROLLER	– SLOT 11
979A TILINE MAGNETIC TAPE CONTROLLER	– SLOT 12
FD1000 TILINE FLEXIBLE DISK CONTROLLER	– SLOT 15

2. EACH SWITCH SECTION MUST BE ON UNLESS A TILINE MASTER CONTROLLER IS INSTALLED IN THE CORRESPONDING CHASSIS SLOT. TILINE PRIORITY SYSTEM WILL NOT WORK IF SWITCHES ARE SET INCORRECTLY.

3. SLOT 17 DOES NOT REQUIRE A SWITCH.

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Figure 2-13. 17-Slot Chassis TLAG Jumper Switch Settings

2.3.6.4 Interrupt Connections. Interrupt connections to interface peripheral equipment to the 990 processor usually are made before the system is delivered to the customer. The planned growth path for the DS990 systems avoids the necessity for the customer to modify interrupt levels, except under very unusual circumstances. Preassigned slot assignments do not require modification of the factory prewired interrupt levels. Note, however, that adding a controller to a previously existing installation requires a SYSGEN operation to coordinate hardware and software operation.

The information in the following paragraphs is provided for users who must modify existing interrupt assignments.

The 990 processor has 16 interrupt levels, numbered 0-15. Interrupt level 0, which is internal to the processor, has the highest priority. Interrupt levels 3, 4, and 6-15 are external inputs that are available for assignment to peripheral controllers installed in the chassis. The interrupt input lines are wired from chassis slot 1 to an interrupt header adjacent to slot 1.

Each of the remaining chassis slots (numbered 2 and above) has two interrupt output lines wired to the same interrupt header. Interrupt level to device assignments are made by jumper connections at the interrupt header.

Interrupt Connections for 6-Slot and 13-Slot Chassis. Figure 2-14 shows the location of the interrupt jumper header and interrupt jumper plugs in a 6-slot or 13-slot chassis. Early versions of the chassis use direct pin-to-pin jumpers without jumper plugs.

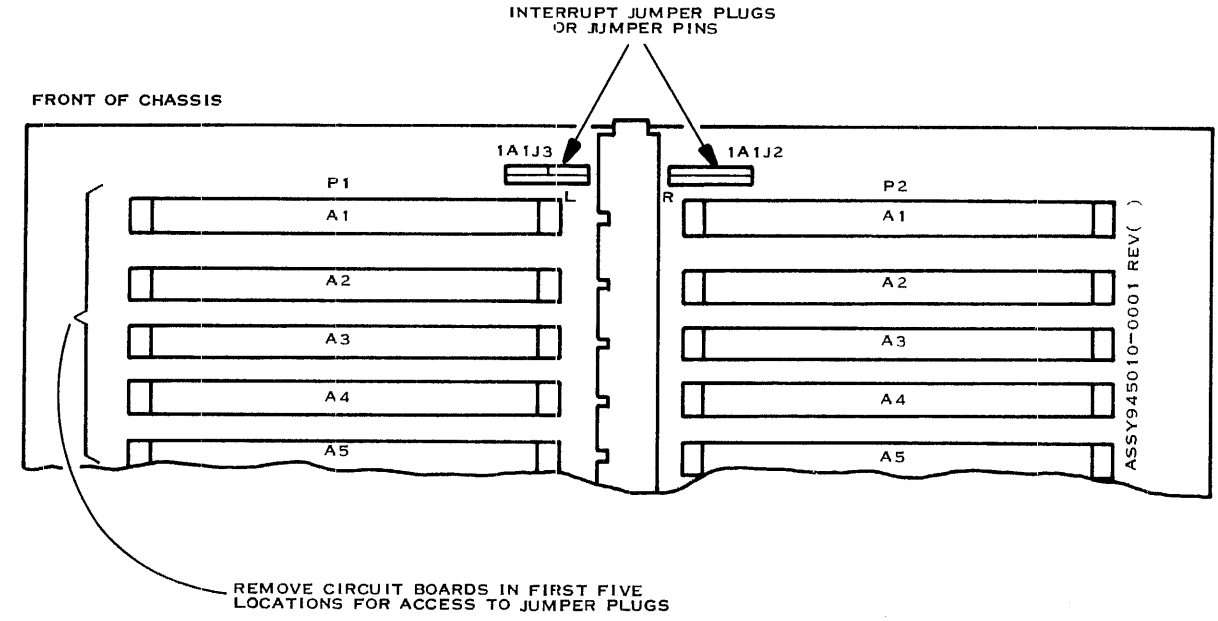

Figure 2-14. Location of Interrupt Jumpers, 6-Slot and 13-Slot Chassis

There are two rows of pins in the header. The top row has 15 pins connected through the motherboard to the 15 interrupt levels of the processor. Additional pins on the top row are provided in the 13-slot chassis for special configurations, such as CRU expansion. The bottom row contains 48 pins in a 13-slot chassis or 20 pins in a 6-slot chassis. Two of these pins are wired to each of the possible circuit board interrupt outputs. This allows multiple interrupts to be connected to one interrupt level.

Interrupt pin assignments are shown in Figure 2-15 and Figure 2-16, which are views of the jumper plugs as seen from the jumper wire side. The X marks identify jumper plug positions that have no corresponding pins on the header. The O marks identify jumper plug positions that have no corresponding pins on the early production header.

The configuration chart on top of the chassis details the interrupt level and chassis slot assignments. Any modifications should be recorded on the chart.

The detailed procedure for assigning and changing interrupt levels is presented in the hardware reference manual for the 990 computer. The information presented here is a brief summary of that procedure.

CAUTION

Do not remove or install any circuit board or modify any jumper while power is applied to the 990 chassis.

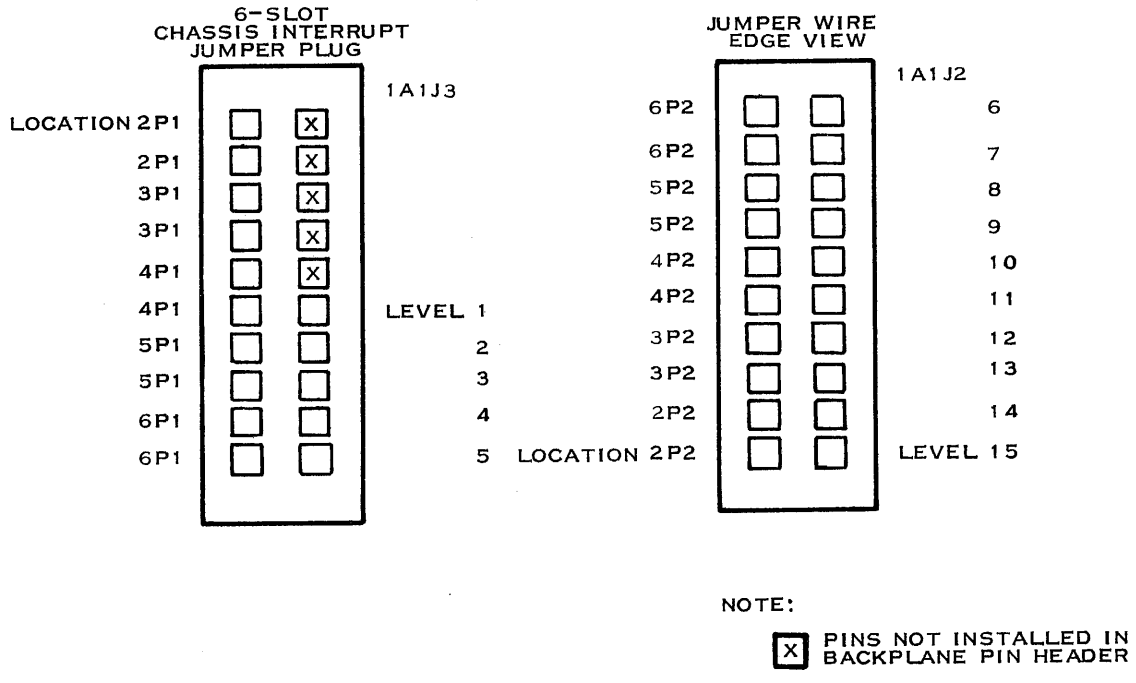

Figure 2-15. 6-Slot Chassis Interrupt Jumper Plugs

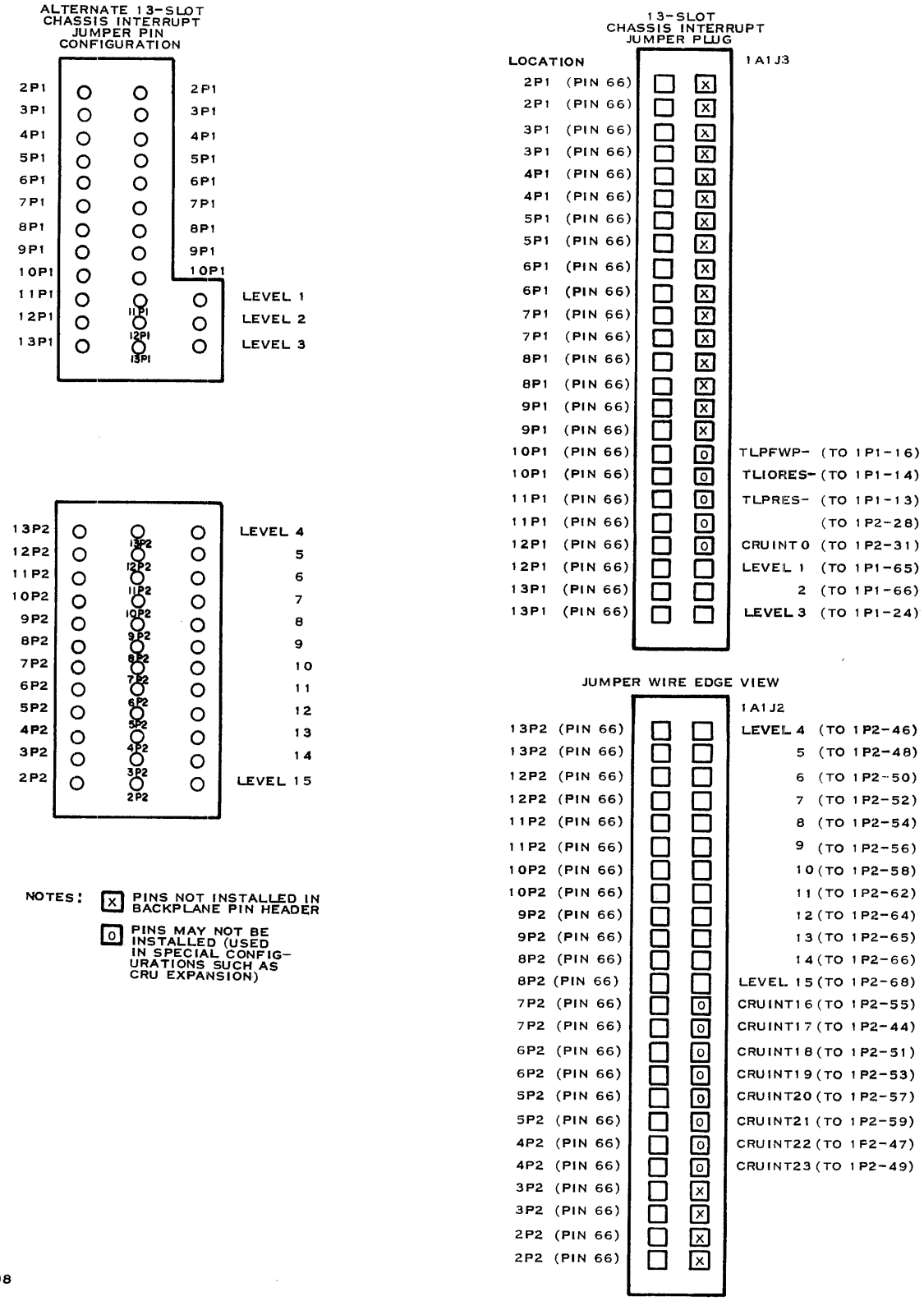

Figure 2-16. 13-Slot Chassis Interrupt Jumper Plugs

To gain access to the interrupt jumpers, remove the circuit boards installed in slots 1-5. The interrupt jumpers will be visible on the motherboard just above the slot 1 connectors. The interrupt output of a full-sized board is on P2 of the assigned slot location. Therefore, if slot 8 is chosen for the disk controller, the interrupt will be found at 8P2 of the wire-wrap pin header. A single jumper should be run from the 8P2 pin to the selected interrupt level input to the processor.

After completing any interrupt jumper modifications, carefully reinstall the removed circuit boards (component side up) according to the configuration chart attached to the top of the computer. Update the configuration chart to correspond to the interrupt jumper modifications.

Interrupt Connections for 17-Slot Chassis. Interrupt lines in the 17-slot chassis are wired to a 70-pin connector accessible from the rear of the chassis. A jumper assembly is plugged into the connector to make the interrupt level to chassis slot connections. This assembly appears at the lower left of the chassis backplane as shown in Figure 2-12.

The jumper assembly supplied with a standard DS990 system is a PWB, so it should not be necessary to alter the standard interrupt level assignments. If it should become necessary to change interrupt levels, the customer may purchase a special variable jumper assembly, or modify the fixed jumper card. Figure 2-17 shows the pin assignments on the interrupt connector.

To gain access to the interrupt jumper assembly, open the chassis rear cover. Remove the interrupt jumper assembly by gently rocking it up and down to loosen the connector and then pulling it straight back. When reinstalling the assembly, make sure the pins are properly aligned before applying mating force.

CAUTION

It is possible to install the interrupt jumper assembly upside down. Note that pin 1 is at the bottom of the interrupt connector.

2.3.7 Disk Drive Mounting

The disk drive may be mounted on a tabletop using rubber feet supplied with the drive, or on a pedestal, part number 947535 (Figure 2-18). To mount the drive on a pedestal, perform the following procedure.

1. Place the pedestal in the desired location, with the cabinet opening toward the front.

2. Carefully place the disk drive on the pedestal, and route the power and signal cables through the opening in the rear of the pedestal.

3. Secure the disk drive to the pedestal by installing bolts (removed from the shipping base) through the three holes in the mounting plate of the pedestal into the disk drive.

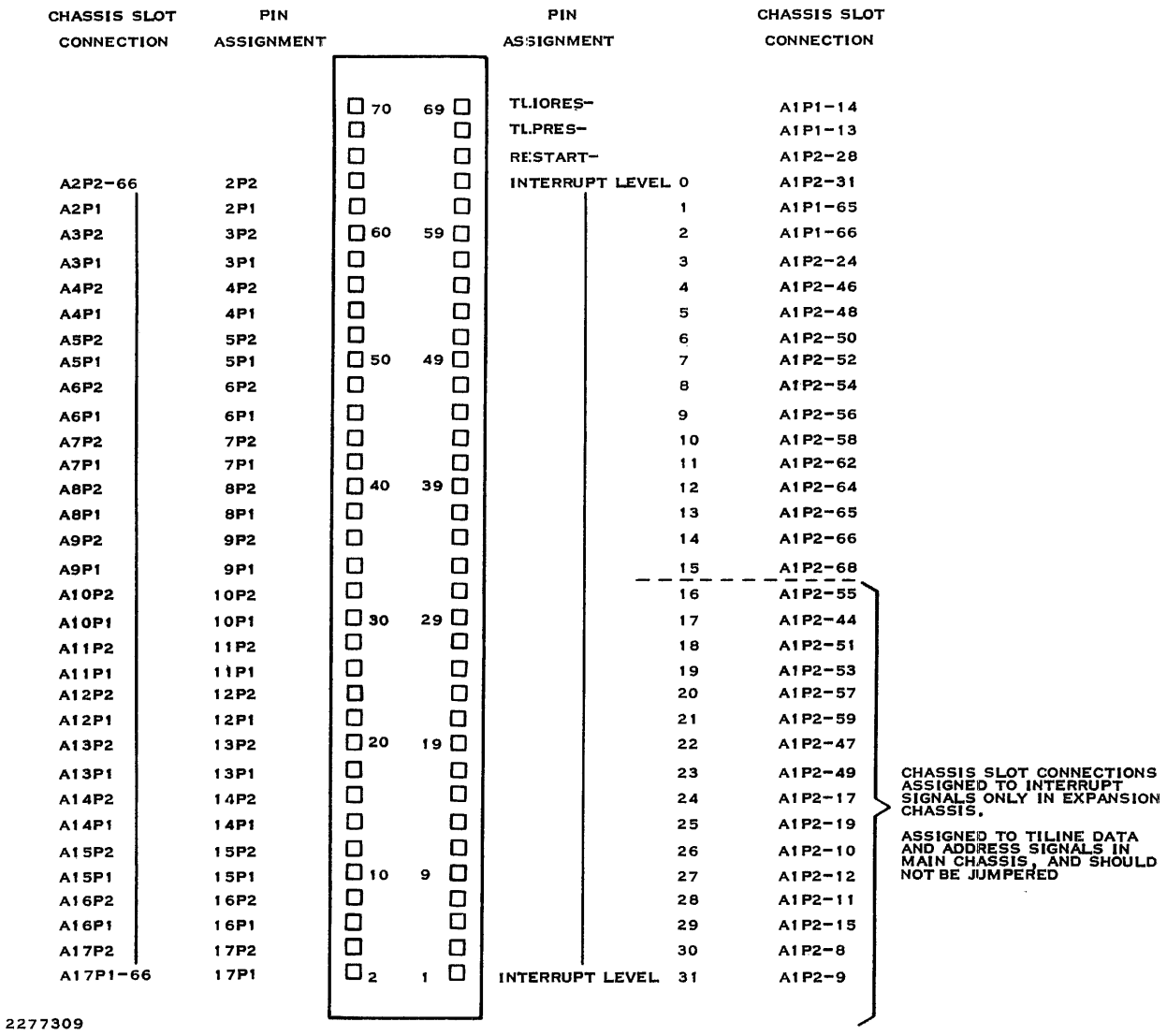

Figure 2-17. 17-Slot Interrupt Jumper Connector

2.3.8 Cabling and Connections

The following paragraphs detail I/O cable installation between the CPU and the disk drive(s).

Up to four disk drive units may be connected to a single disk controller (Figure 2-19). If one disk drive is connected to the controller, the controller-to-drive I/O cable (part number 2308634-0001) is routed from the controller to connector J02 at the rear of the disk drive, and a terminator card is installed in connector J04. Connector J03 is left unconnected, as is connector J01, which is reserved for the T2000B exerciser. If two or more disk drives are connected, the controller-to-drive cable is routed from the controller to connector J02 on the first drive and a drive-to-drive cable (part number 2308634-0003) is routed from bus connector J03 on the first drive to connector J02 on

the second disk drive. This configuration is repeated for each drive in the daisy chain. A terminator board is then installed in bus connector J04 in the last drive in the daisy chain. (Note that in these configurations, either connector J03 or connector J04 is used in any one drive, but there should never be both a connector cable attached to J04 and a terminator in J03 in the same drive.)

Figure 2-20 shows the I/O cable and terminator card installation for a single drive system. Note that if daisy-chaining a Model CD1400 disk drive with the DS80 disk drive that the CD1400 disk drive contains two drive units, and only one CD1400 disk drive may be daisy-chained with one or two DS80 or DS300 drive units. Refer to the CPU installation and operation manual for I/O cable connection details to the CPU, and refer to the installation and operation manuals for the CD1400 and the DS300 disk drive if connecting either of these drives to a controller with the DS80 drive.

NOTE

Unit selection is not determined by cable routing, but by switch settings on the disk drive interface (I/O) PWB. Refer to paragraph 2.3.4.1.

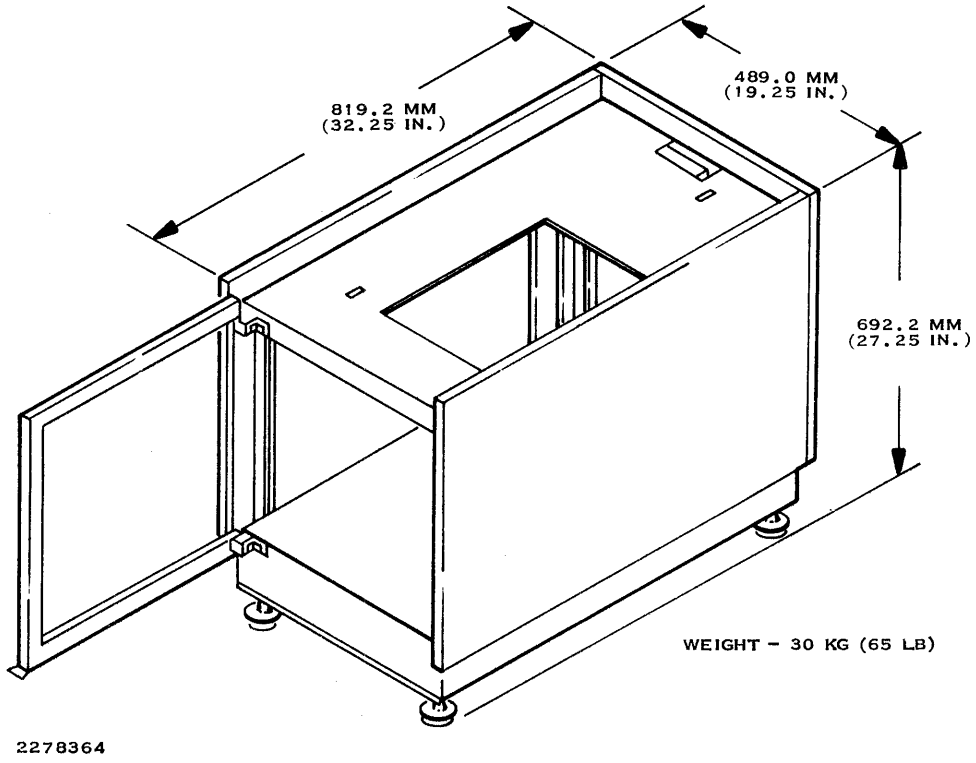

Figure 2-18. Disk Drive Pedestal

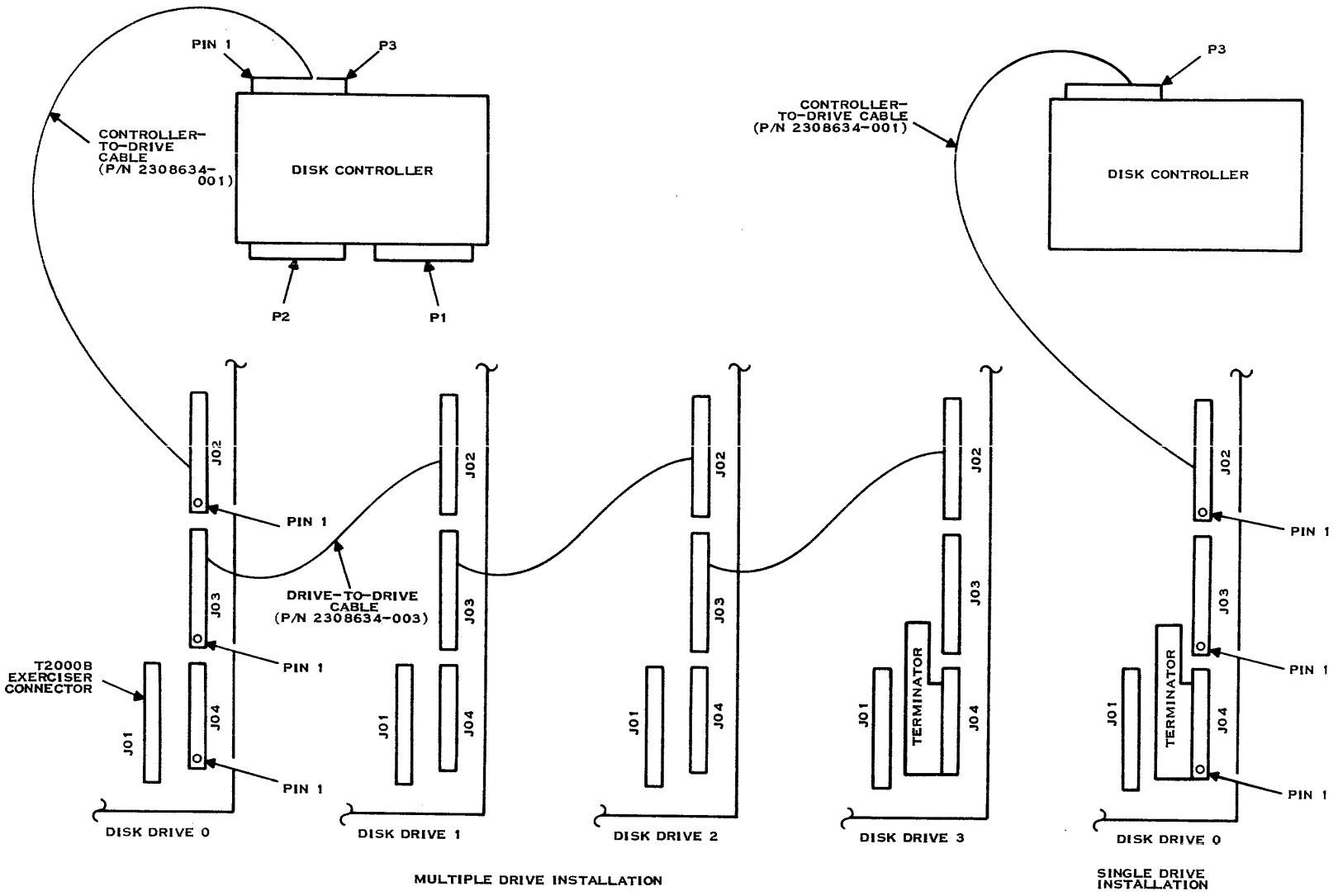

Figure 2-19. Single and Multiple Disk Drive Configurations

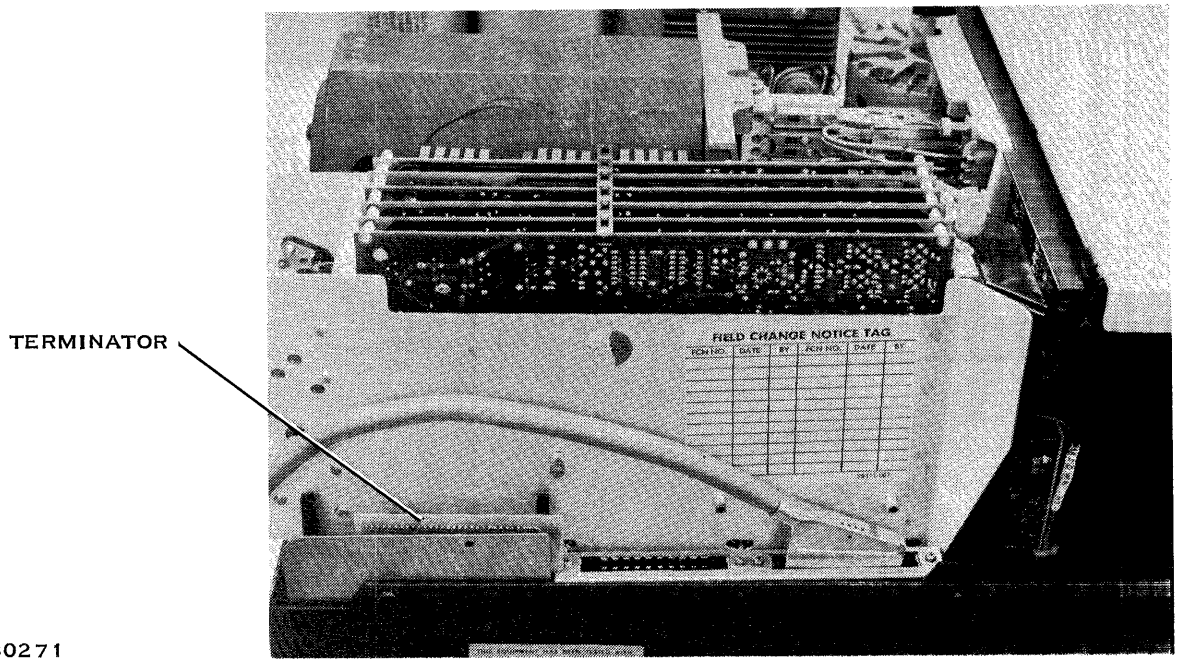

Figure 2-20. I/O Cable Installation

2.3.9 Ac Power Connections

The DS80 disk drive can operate from a nominal primary input power of 100, 115, or 127 Vac, 60 Hz; or 200, 220, or 240 Vac, 50 Hz, single phase. The model number and the primary power requirements are stamped on the nameplate on the rear of each drive. Verify that the power source is compatible, and that the disk drive jumper configuration is correct before connecting the ac line cord.

2.3.9.1 110, 115, and 127 Volt Connections. Perform the following procedure before applying ac power to the drive.

1. Check the identification plate at the rear of the drive for voltage, phase, and frequency of the required input power. Ensure that these match the available power.

WARNING

Never operate the disk drive as a stand-alone unit without the ac and dc grounds shorted together at the power supply. A potential as high as 60 volts can develop between the logic ground and the frame.

2. Refer to Figure 2-21. Verify that the shorting jumper is installed on the spade terminal marked AC/DC GRD SHORT.

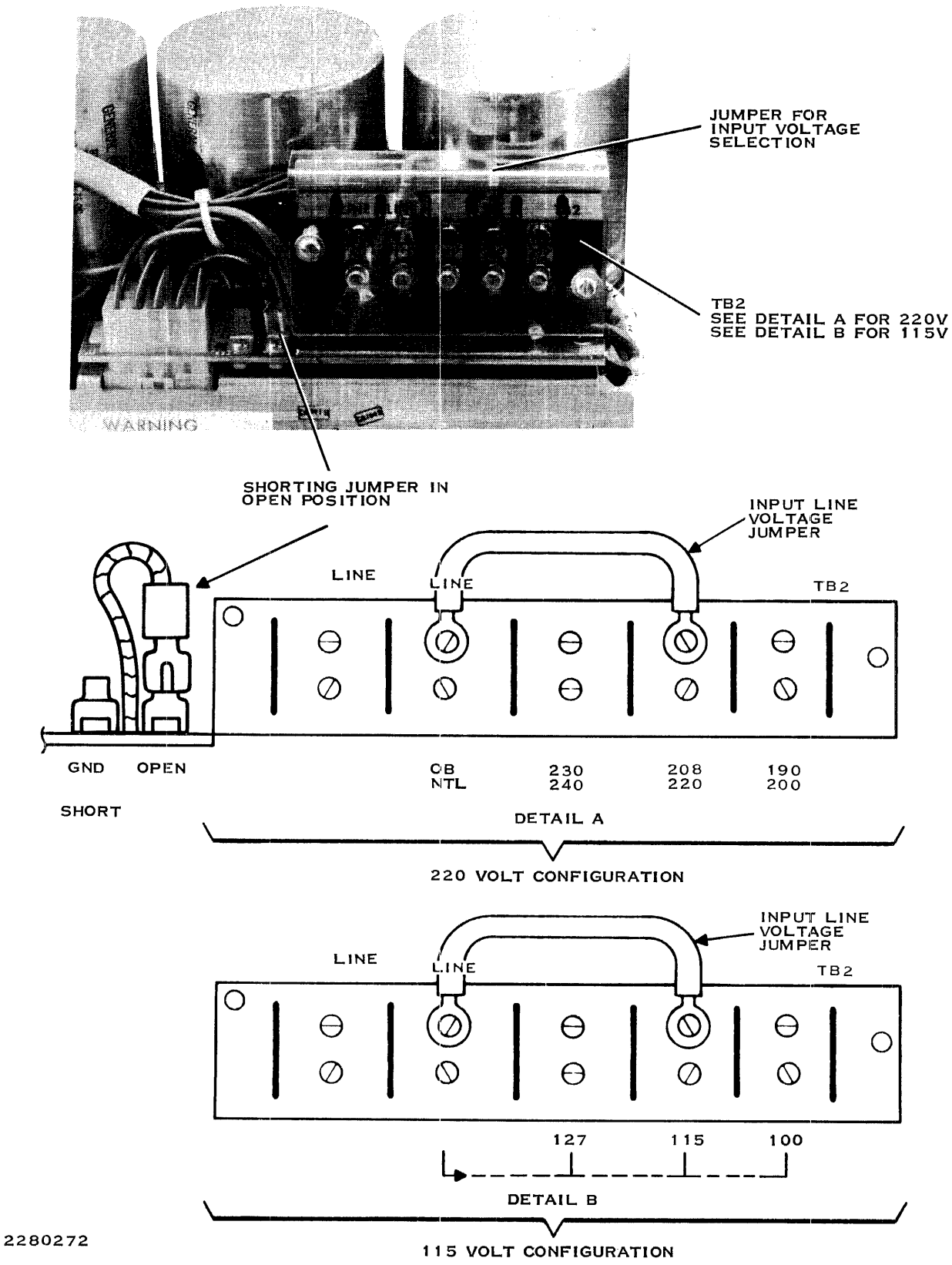

Figure 2-21. Ground Short and Voltage Select Jumpers

CAUTION

Never operate a disk drive that is designed for 100, 115, or 127 Vac from a power source that supplies less than 85 Vac or more than 140 Vac.

3. Measure the ac source voltage that will be used to power the disk drive.

4. Inspect terminal board TB2 (Figure 2-21) located on the power supply assembly. Verify that the jumper is installed between the terminal marked OB/NTL and the terminal corresponding to the measured source voltage as shown in the following chart. Note that the terminal cover markings on the lower part of the cover refer to the 100, 115, and 127 Vac disk drive. If the jumper is not correctly installed, remove and reinstall it in the proper location.

Measured Ac Input Voltage Range	Jumper Terminal
Between 85 and 107	100
Between 107 and 121	115
Between 121 and 140	127

5. Remove the cover from the power cable terminal board TB1 and ensure that all three wires are connected as shown in Figure 2-22 and that the terminals are secure. Reinstall the cover.

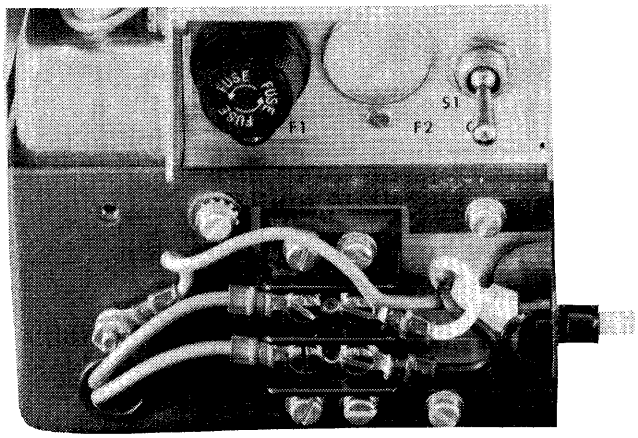

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Figure 2-22. Power Cable Terminal Board TB1

2.3.9.2 200, 220, and 240 Volt Connections. Perform the following procedure before applying ac power to the drive.

1. Check the identification plate at the rear of the drive for voltage, phase, and frequency of the required input power. Ensure that these match the available power.

WARNING

Never operate the disk drive as a stand-alone unit without the ac and dc grounds shorted together at the power supply. A potential as high as 60 volts can develop between the logic ground and the frame.

2. Refer to Figure 2-21. Verify that the shorting jumper is installed on the spade terminal marked AC/DC GRD SHORT.

CAUTION

Never operate a disk drive designed for 200, 220, or 240 Vac from a source that supplies less than 190 Vac or more than 264 Vac.

3. Measure the ac source voltage that will be used to power the disk drive.

4. Inspect terminal board TB2 (Figure 2-21) located on the power supply assembly. Verify that the jumper is installed between the terminal marked OB/NTL and the terminal corresponding to the measured source voltage as shown in the following chart. Note that the terminal cover markings on the upper part of the cover refer to the 200, 220, and 240 Vac disk drive. If the jumper is not correctly installed, remove it and reinstall it in the proper location.

Measured Ac Input Voltage Range	Jumper Terminal
Between 190 and 205	190/200
Between 205 and 224	208/220
Between 224 and 264	230/240

5. Remove the cover from the power cable terminal board TB1 and ensure that all three wires are connected as shown in Figure 2-22 and that the terminals are secure. Reinstall the cover.

2.3.10 Grounding

The disk drive electronics (dc power, logic, and analog signals) are grounded separately from the ac or frame ground. These two grounds are connected only at the grounding studs located next to the voltage select jumpers (Figure 2-21). A ground strap located under the card cage connects between the servo preamp shield retaining screw and the casting (deck) screw near the rear of the drive. To isolate the grounds, place the shorting jumper in the OPEN position and remove the ground strap (retain for future use). To short the grounds, place the shorting jumper in the GND position and connect the ground strap between the servo preamp shield retaining screw and the casting (deck) screw near the rear of the drive. Grounding options are determined according to system configurations, which are explained in detail in the *DS990 Systems Field Maintenance Manual*, part number 2250696-9701. The following general guidelines should be followed when grounding the system.

1. The system should have a single point ground.
2. If one device in the system is grounded, do not ground the disk drive.
3. If no other device in the system is grounded, ground the last disk in the daisy chain.

2.3.11 Verification Before Applying Power

After installation is completed, perform the following verifications before applying power to the disk drive.

1. Verify that all applicable steps listed on the preparation checklist are complete.
2. Verify that all logic cards are firmly seated in the electronics module of the disk drive and the computer chassis.
3. Verify that all connectors and relays are seated firmly.
4. Verify that all cabling is intact and that there are no broken or damaged wires, connectors, or wire-wrap pins.
5. Inspect entire disk drive for foreign material that could cause an electrical short or contaminate the disk drive.
6. Verify that the inlet air filter is installed.
7. Verify that the ac power cord is installed on all disk drives.
8. Install a disk pack using the procedures located in Section 4.

2.4 POWER-ON PROCEDURES

After verification is complete, apply power and purge the disk drives as follows:

1. Turn off the CPU main power. (This is necessary so that power-on sequencing to the disk drives takes place automatically when computer power is applied.)

2. Remove the emergency retract relay (K1) located on top of the power supply (located between the two heat sink assemblies at the front of the unit) from each disk drive.

3. Set the PWR ON/OFF circuit breaker (located on the disk drive rear panel) to ON. The blower fans should start when power is applied to each disk drive.

4. Locate connector J10 on the power supply circuit board (Figure 2-23) and check the dc voltages using a digital voltmeter between the pins listed below. If voltages are not within tolerance, the power supply must be replaced by a qualified maintenance technician.

   a. +8 to +10.5 volts between pin 4 (+) and pin 9 (-).

   b. +30 to +35 volts between pin 1 (+) and pin 2 (-).

   c. -30 to -35 volts between pin 3 (-) and pin 2 (+).

5. Using a digital voltmeter, measure the voltage between logic ground (card cage terminal E11) and the power pins on any of the PWBs (connector A or B, pin 59 or 60). Dc voltage should be between +4.75 and +5.25 volts with an ac ripple component less than 75 millivolts peak to peak.

6. Set the drive START/STOP switch to START.

7. Apply power to the computer.

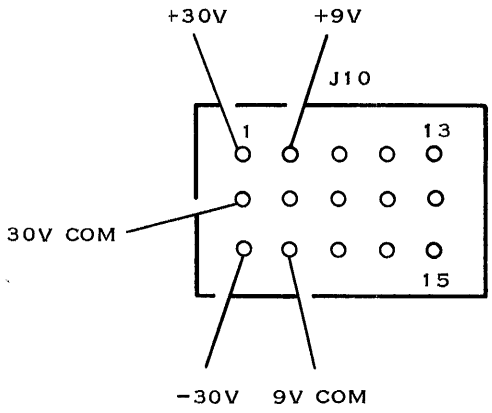
8. Check that the CLK and BUSY LEDs on the disk controller are lit. (These LED locations are shown in Figure 1-2.) Note that the FAULT LED lights for about one-half second after power-up.

9. After 30 seconds, verify that the drive motor on the first disk starts to run. (Allow an additional 60 seconds for the second disk drive in the system to sequence on.) If the drives fail to sequence, check the FAULT LED on the controller. If lit, the controller may be malfunctioning.

10. After all disk drives are up to speed, verify that the FAULT and BUSY LEDs on the controller are out. If the FAULT indicator is lit, the controller may be malfunctioning.

11. Allow the drives to operate for at least 20 minutes to purge the drive of any dust or other contaminants.

12. Set the START/STOP switch on each drive to STOP and allow 30 seconds for the disks to stop rotating.



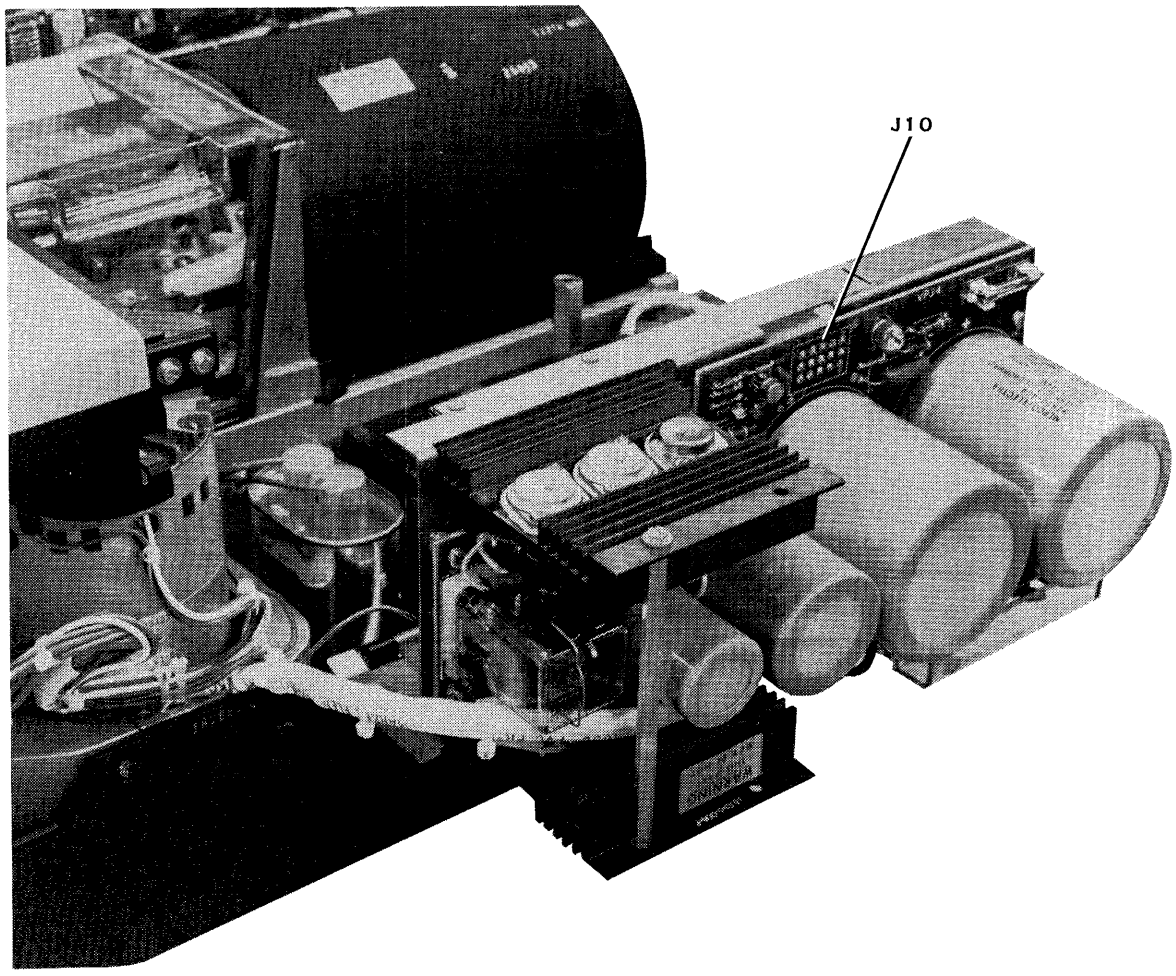


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Figure 2-23. Dc Voltage Measurement Points

13. Replace relay K1 on the power supply.

14. Set the START/STOP switch on each drive to START. Allow 60 seconds between starting each drive to prevent an overload that could trip the main power circuit breakers.

15. When the green ready indicator stops flashing and remains lit, verify that the DEVICE CHECK indicator on each disk drive front panel is out. If this indicator is lit, recycle power to the drive. If the indicator remains lit, refer the problem to a qualified maintenance technician.

16. Set the START/STOP switch to the STOP position, and check that the heads fully unload and the spindle stops.

17. Set the PWR ON/OFF circuit breaker to OFF, and check the head alignment using the following procedure.

    a. Connect the T2000B exerciser to card cage connector J01 on the disk drive. Set all exerciser toggle switches off (down).

    b. Set the DEGATE/INTERFACE switch on the interface (I/O) board to DEGATE. This switch enables exerciser inputs and brings the drive offline.

    c. Connect the T2001A head alignment meter to the disk drive read/write matrix card connector J4 (bottom of card). Set the meter scale switch to OFF.

    d. Set the control panel READ-WRITE/READ ONLY switch to READ ONLY, and install the CE alignment pack on the disk drive.

    e. Set the drive PWR ON/OFF switch to ON. Power up the disk drive by setting the START/STOP switch to START, and wait 30 seconds for the heads to load.

    f. Set the exerciser BUS/BIT switches to >1F0 (Bit switches 256, 128, 64, 32, and 16 up).

    g. Set the FUNCTION SELECT switch to SKALT and press the SINGLE switch down several times until the drive heads move to the alignment cylinder. Set the exerciser DISPLAY SELECT switch to CAR to verify the seek operation. The display indicators should indicate >1F0.

NOTE

Wait for a least 30 minutes before proceeding to allow the rotating CE pack to become thermally stable. If the CE pack was brought into the computer room environment less than 2 hours before use, wait for 1 hour before proceeding.

h. Set the exerciser DISPLAY SELECT switch to SEQUENCE and the FUNCTION SELECT switch to READ. The three low-order bits of the SEQUENCE display show the head selected and should be out (head 0 address). If any other head address is displayed, press the exerciser RSTHD switch down once to reset the head address count to zero.

i. Set the meter scale switch on the head alignment meter to 1250 MICRO IN. and the DIBIT POLARITY switch to R2. Activate the drive read gate by turning the exerciser CONT switch to on.

j. Check the meter reading, and switch the meter scale switch to the most sensitive position possible without pinning the meter.

k. Record the meter reading or algebraic average of the R1 and R2 readings in plus or minus microinches for the head selected (Head 0 for the first record). Set the exerciser CONT switch to OFF.

l. Press the exerciser ADVHD switch once to step to the next head. The binary address of the active head shown by the SEQUENCE display should advance by one. (Pressing the RSTHD switch will reset the head address count back to zero.)

m. Repeat steps j through l for each head until the off-center values of all five heads (0 through 4) have been recorded. The heads must be realigned if any head is greater than ± 125 microinches out of alignment. If alignment is necessary, refer to the *Model DS80 Disk System Field Maintenance Manual*, part number 2302630-9701 for head alignment instructions.

n. Set the disk drive START/STOP switch to STOP and wait for the green ready indicator to stop blinking and remain out.

o. Remove the CE disk pack.

p. Set the disk drive PWR ON/OFF switch to OFF.

q. Disconnect the T2000B exerciser and the T2000A head alignment meter from the disk drive.

18. Replace the disk drive front and rear covers.

2.5 INITIALIZING DISK MEDIA

Before operating the disk drive, the disk media may need initialization. Since initialization procedures differ according to the particular operating system in use, the operator must refer to the software reference manuals for initialization instructions. Three of the operating parameters that must be considered when initializing the media are the physical record size, hardware interleaving factor, and bad track input.

2.5.1 Physical Record Size

In order to maximize disk use, the physical record size should be some multiple of 256 (e.g., 256, 512, 768, etc.). Further details concerning choosing this multiple are found in the software reference manual.

2.5.2 Hardware Interleaving Factor

Variable hardware interleaving is not supported in the DS80 disk system. Use a factor number of 1 when initializing media.

2.5.3 Bad Track Input

Disk packs are generally supplied with bad track information that can be entered into the operating system so that these bad tracks can be deallocated while using the disk system. The ECC controller, however, has the capability of substituting spare tracks for these bad tracks so that the media operates in the system as though it were error free. When using Texas Instruments-supplied media with surfaces that have been analyzed using the Diagnostic Operation Control System (DOCS) surface analysis, bad track information that is supplied with the media must not be entered into the operating system during INV or IDS operations.

Media that has not been supplied by Texas Instruments or has not undergone a TI DOCS surface analysis must have bad track information entered into the system during the INV or IDS operation in order for these bad tracks to be deallocated by the system.

If the 990 computer is operating under the DX10 operating system, refer to the applicable software manual that describes initializing new media for information on bad track input.

Diagnostic operation control system (DOCS) software is available that can map bad tracks on a disk pack. These routines and their loading and operating procedures are described in the *Model 990 Computer Unit Diagnostics Handbook Volumes I and III.*

2.6 SELF-TEST

When the system is powered up or reset, the disk controller automatically conducts a self-test. During execution of the self-test, the FAULT LED on the disk controller lights. If the system passes these tests, the FAULT LED goes out after the self-test is completed successfully. If the FAULT LED does not go out, refer the problem to a maintenance technician.

3

Programming

3.1 GENERAL

This section contains information necessary for an assembly language programmer to write device service routines (DSRs) that communicate with the Model DS80 disk system. The programmer must be familiar with assembly language described in the *Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide* or the *Model 990/12 Computer Assembly Language Programmer's Guide.*

Most users prefer Texas Instruments standard operating system software that includes DSRs and features standardized file manipulation schemes that are essentially independent of I/O device type. These users should refer to the applicable operating system reference manual. Users who wish to perform direct disk I/O operations without using a standard operating system DSR may initiate disk commands and receive disk status as described in this section.

This section is organized into the following four basic parts.

1. Communication between the disk system and the CPU using the TILINE is discussed.
2. Basic programming of the controller is detailed, including command descriptions, disk operation, and command completion.
3. Control and status word formats and descriptions are given.
4. Detailed command descriptions with example command formats and status word formats are discussed.

3.2 TILINE COMMUNICATION

3.2.1 Introduction

The TILINE is an asynchronous 16-bit parallel data bus that transfers data between high-speed system elements such as the 990 main memory, 990 CPU, and disk controllers. The disk controller is assigned a block of eight TILINE memory addresses, and these memory locations reside on the controller board. The 990 processor communicates with the controller by writing 16-bit command words into these eight TILINE addresses. After a disk operation is completed, the disk controller replaces the control words with status words, and the 990 processor can read the words in these same memory locations to determine disk drive status. Controller operations are initiated when control words containing initialization parameters, operation parameters, and command codes, are written into the memory locations assigned to the controller. After initialization, the disk controller acts independently of the 990 processor and transfers data between specified TILINE memory locations and the disk as required by the command. Any computer instruction that reads or modifies general memory can be used to communicate with the disk controller.

3.2.2 Drive Unit Designation

The controller treats each disk drive in a daisy chain as independent logical drive units, and each unit is assigned a separate unit number. Each drive unit may be assigned any unit number from 0 to 3; however, no two drive units should be assigned the same unit number. In a single disk drive installation, the drive is usually assigned unit number 0. Drive unit numbers are assigned using switches located on the disk drive interface (I/O) board.

3.2.3 TILINE Addresses

Standard conventions built into the hardware and software of the Model 990 computer reserve CPU byte addresses >F800 to >FBFF for control and status communication with TILINE peripheral controllers, such as the magnetic tape and disk controllers. This range is called the TILINE peripheral control space (TPCS). Addresses in this range may be mapped by the processor hardware to TILINE addresses in the range >FFC00 to >FFDFF. This mapping requires the 990 processor to be operating either unmapped or in map file 0. The TPCS also can be addressed through alternate map files if the mapping bias value is chosen to yield the correct TILINE address. This programmable mapping feature is standard on some 990 CPUs and optional on others. This feature allows effective use of the entire TILINE address space rather than just the lower 32K words. Depending on the values in the map file registers, memory may be addressed anywhere in the TILINE address space (assuming a memory board exists at that address).

The physical TILINE bus includes 20 address lines, however, each CPU byte address consists of 16 bits. When a CPU byte address falls within the TPCS, all ones are loaded automatically into the upper five bits of the TILINE address, and the least significant bit (LSB) is dropped. (This LSB is a byte selector that is used only within the CPU.) The remaining 15 bits form the lower 15 bits of the TILINE address. Figure 3-1 shows the conversion of a 16-bit CPU byte address to a 20-bit TILINE word address. One way to visualize this conversion is to think of a 21-bit TILINE *byte* address of >1FF800 that loses its LSB (byte selector) to become TILINE *word* address >FFC00. The 1F comes from the 5 ones and the >F800 comes from the original CPU byte address. The only part of this address accessible to the programmer is the CPU byte address, >F800.

The eight addresses are assigned to the controller from a base address to base address + 7 word addresses. The base address is dedicated to control and status word W0, base address + 1 is dedicated to W1 and continues through base address + 7, dedicated to W7.

The base address is selected by a five-section switch on the disk controller board, allowing multiple controllers in one system. Base address selection must be coordinated with the operating system software. Refer to Section 2 of this manual for instructions on setting the base address switches.

The controller is capable of communicating with TILINE memory in any range of the TILINE address space; however, the TPCS is generally reserved only for CPU/controller communications.

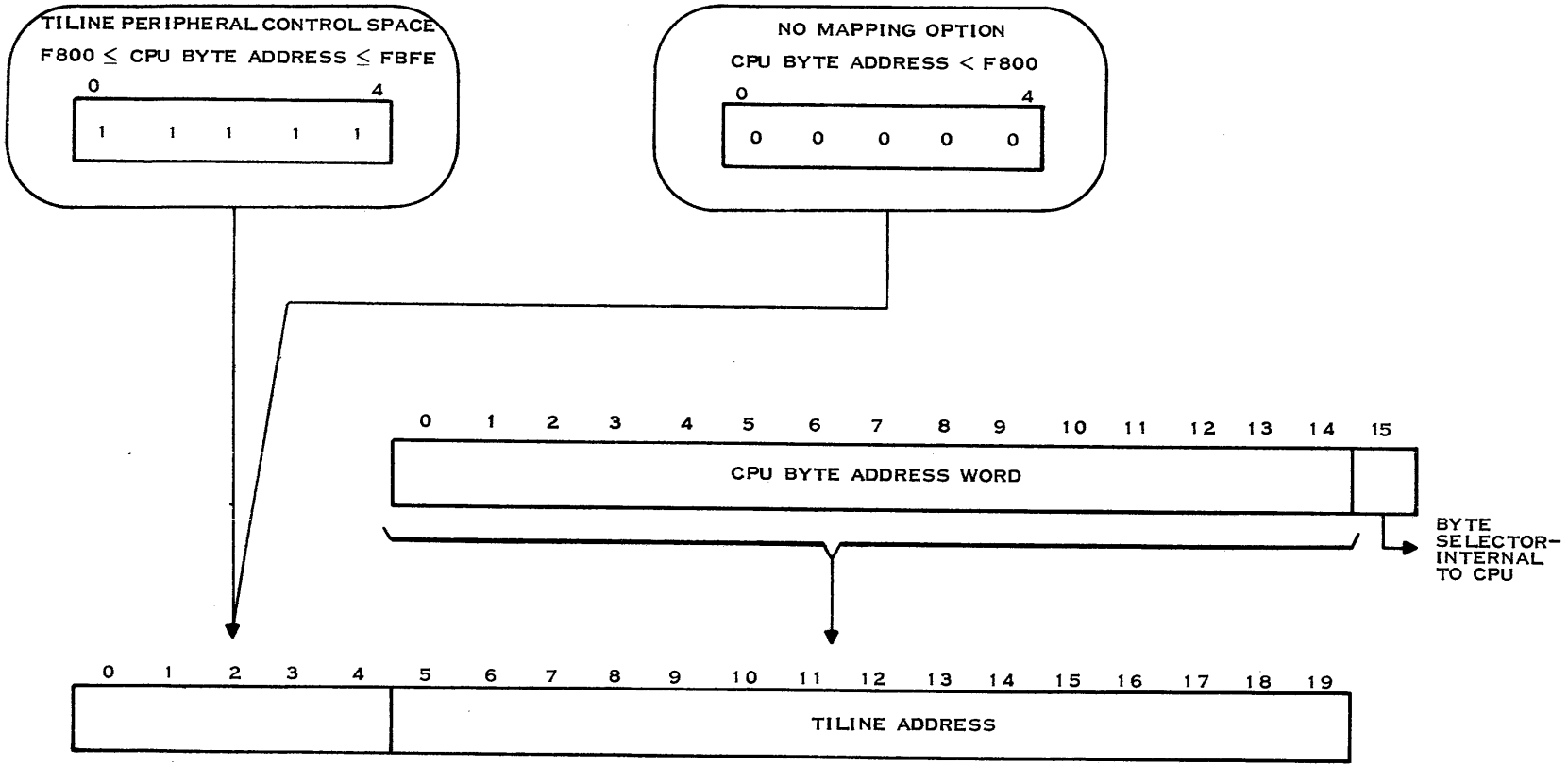

Figure 3-1. Relationship Between TILINE Address and CPU Byte Address

3.3 CONTROLLER COMMAND DESCRIPTIONS

Commands sent to the controller from the CPU cause the controller to perform any of eight basic disk system operations as follows. These eight operations are introduced here for clarity, but detailed command descriptions and examples are deferred until later in the section since these descriptions require complete control word information.

- Store Registers. A store registers command causes the disk controller to return certain critical drive parameters, such as words per track and cylinders available per drive unit, to the CPU. This operation allows the operating system software to determine these parameters prior to using the disk system.

- Write Format. The write format command formats a new disk (or reformats a disk previously in operation) with ID words (that make up the header), fixed data in the data field, an ECC character, and the required gaps. The write format operation must be performed before using any unformatted disk media. Note that the write format command destroys any previously written data on a disk. If a bad track has been relocated, the write format command formats the spare (relocated) track as if it were the specified track.

- Read Data. The read data command transfers data from a specified disk location to a specified location in TILINE memory. If a bad track has been relocated, the read data command reads the data from the relocated track as if it were the specified track.

- Write Data. The write data command reads data at a specified TILINE memory location and records this data at a specified location on a previously formatted disk. If a bad track has been relocated, the write data command writes data onto the relocated track as if it were the specified track.

- Unformatted Read. There are two unformatted read command operations. The unextended unformatted read command simply returns certain disk drive parameters to the software. It operates in this way to ensure compatibility with some existing operating systems that obtain these parameters by reading header information. The extended unformatted read command, on the other hand, reads a specified number of words from the disk without regard to formatting, and is used basically for diagnostic purposes.

- Unformatted Write. The unformatted write command writes data from TILINE memory onto the disk without regard to existing record boundaries, and is used primarily for diagnostic purposes.

- Restore. The restore command reinitializes the cylinder counter and repositions the heads of the selected drive over cylinder zero. The operation clears certain disk error conditions.

- Seek. A seek command is used to position the read/write head over a track to be read or recorded. Since the seek is a relatively slow mechanical operation, the CPU can issue a seek to a particular drive to prepare it for a later data transfer without having to wait for the seek to complete. In addition, data transfers using other drive units in a daisy chain can occur while this seek operation is executing. When the seek is completed, an interrupt can be generated by the controller to signal the CPU that a drive is ready for data transfer. If a seek operation is performed to a bad track, the disk drive performs an additional seek to the relocated track so that a normal read or write operation can then be performed.

- Self-Test. The controller incorporates extensive self-test routines that can be used to locate many controller faults.

- Absolute Write Format. The absolute write format command executes exactly like the normal write format command except that it is nonrelocatable. If the specified track has been relocated to an alternate track due to errors, the normal write format command formats the alternate track. The absolute write format command, however, formats the specified track.

- Relocate Command. The relocate command relocates a bad track to one of the spare tracks. When a bad track has been relocated, a disk operation to a sector on a bad track is automatically performed on the alternate spare track. The disk media then appears to be error free to the operating system.

3.4 PROGRAMMING THE CONTROLLER

The eight control and status words the CPU uses to communicate with the controller contain the following information:

- Word 0 (W0) — Disk Status. Contains disk status codes for the selected drive, and attention bits and attention mask bits for generating interrupts.
- Word 1 (W1) — Command and Head Address. Contains command codes, head address, and several control bits used during certain recovery operations.
- Word 2 (W2) — Sector. Specifies the starting sector address and number of sectors per record.
- Word 3 (W3) — Cylinder Address. Contains the cylinder address.
- Word 4 (W4) — Byte Count. Specifies the number of bytes to be transferred between the disk and CPU memory.
- Word 5 (W5) — LSB Memory Address. Contains the fifteen LSBs of the twenty-bit TILINE memory address.
- Word 6 (W6) — Select and MSB Memory Address. Contains drive select codes and the five most significant bits (MSBs) of the twenty-bit TILINE memory address.
- Word 7 (W7) — Controller Status. Contains controller status codes, the interrupt enable bit, and the idle/busy bit.

To initiate controller operation, the program loads the control words into on-board memory addresses assigned to the controller. The order in which the control words are transmitted is not important except that W7 must be last because the controller immediately begins to execute the operation specified by the control words as soon as controller location W7 is loaded with a word that has bit 0 set to zero.

Transmitting a new set of control words to the controller destroys the status words from the previous operation except for the disk status fields of W0 that are set by the disk drive and cannot be modified by overwriting with a new control word. If overwriting is attempted, the controller ignores the bits placed in the W0 disk status fields.

If the CPU attempts to send a control word to the controller after operation has been initiated, the attempt completes normally, but the controller ignores the control word.

Any status word read from a busy controller is a simulated W7 word in which bit 0 is a zero (busy) and bits 1 through 15 are meaningless. This word is returned regardless of the status word requested. This feature allows the controller to be polled for idle/busy status without interfering with any on-going controller operations.

Before writing a command to the controller registers, W7, bit 0 should first be checked to verify that the controller is idle and will accept the command. If W7, bit 0 is set (controller idle), the command may be written to the controller registers.

3.4.1 Command Completion

An interrupt enable bit in W7 allows the programmer to specify whether the controller will generate an interrupt to the CPU upon completion of an operation. The disk controller may be used with either an interrupt-driven or a polled DSR. The following paragraphs discuss these options.

3.4.2 Command Completion Without Interrupts

To check command completion or controller availability in a polled system, read status word W7 periodically to check bit 0 for idle status. A 0 in this position indicates that the controller is busy; a 1 indicates that the controller is idle and available for commands, and that status indications are valid.

Usually, the program initiates a timing loop when controller operation begins, and checks the idle bit at timer expiration. If the idle bit is still zero, the timer may be restarted and the sequence repeated a preselected number of times. This method requires more program overhead than the interrupt-driven approach.

If a restore or independent seek command has been initiated, the disk may not be ready after the controller has reported completion. To determine if the disk has completed a restore or independent seek command, the program should check the drive status bits of word 0. If the disk drive has finished its operation, the attention line for the selected drive will be set, and either the not ready bit will be inactive or the seek incomplete bit will be set.

3.4.3 Command Completion with Interrupts

The controller can issue two types of interrupts to the computer. One type of interrupt is issued when the controller completes a command, and the other type is issued when the disk drive completes an operation. Most disk drive operations are completed when the controller has completed a command. For independent seek and restore operations, however, the controller completes the command before the disk completes the operation, and the drive completion interrupt may be used to determine when the system is again idle.

3.4.3.1 Command Completion Interrupts. To have the controller issue an interrupt to the 990 processor upon command completion, the interrupt enable bit in W7 must be set when the operation is initiated. When the controller returns to idle, the interrupt is issued to the CPU. This interrupt is cleared by resetting the interrupt enable bit or the appropriate completion bit in W7.

3.4.3.2 Drive Completion Interrupts. Control word 0 contains four attention lines (one for each of the four disk drive unit addresses) and four attention mask lines. Each drive's attention line is set when either the disk drive is ready or a seek error has occurred. When the attention bit and mask bit for any disk drive unit are both set, the interrupt line to the computer is also set.

The programmer can set or reset the mask bits by using any of the computer memory instructions. However, the attention bits and disk status bits are set only by the controller to indicate current disk operation status.

To use the drive completion interrupts during a restore operation, first issue the restore command to the controller; then, after the controller reports command completion (by a controller idle or command completion interrupt), set the mask bit corresponding to the desired drive. When the drive finishes the restore operation and the controller is idle, an interrupt is issued to the CPU. This interrupt may be cleared by resetting the mask bit corresponding to the interrupting drive. The controller resets all controller interrupts when it switches from an idle to a busy condition.

3.5 CONTROL AND STATUS WORD FORMATS

The control and status words described in this section are used for both operating the controller and reporting disk system status. As described earlier, the CPU can write control words into controller memory space to initiate operation, and can read status words in these same memory spaces to determine disk status after an operation has completed. Some bits in the words are used only for disk operation control, some only for status reporting, and some for both control and status. The following paragraphs describe the functions of each of the bits in these control and status words. Figure 3-2 shows the format and bit assignments of each word.

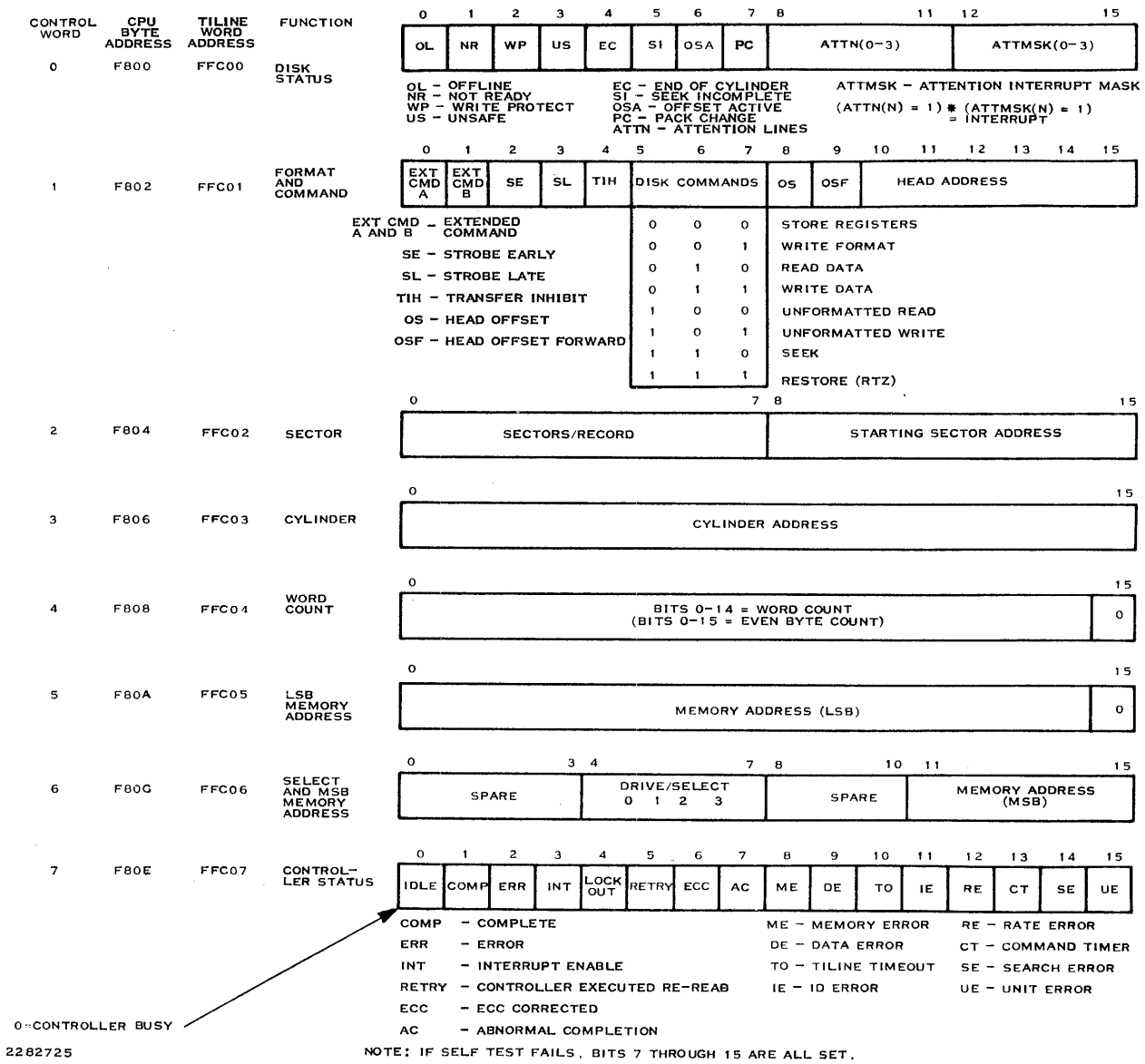

Figure 3-2. Control and Status Word Formats

3.5.1 W0 — Drive Unit Status

W0 (Figure 3-3) enables or inhibits the attention interrupts, indicates which drive unit initiated an attention interrupt, and indicates status of a selected drive unit. The bits in W0 are used only for status reporting, except for bits 12 through 15 that are used only by the CPU to set the attention mask bits.

Bits 0 through 7 contain individual status indicators for a selected drive unit. Bits 8 through 11 contain the attention line status of each drive unit, regardless of the drive unit selected. Bits 12 through 15 are mask bits used with the attention bits to generate interrupts. Each bit is defined as follows:

3.5.1.1 Offline (OL) — W0, Bit 0. Bit 0 is set to indicate that the selected drive unit is not powered up, is not at the proper speed, or is not loaded with a disk pack, or that an unsafe condition exists.

3.5.1.2 Not Ready (NR) — W0, Bit 1. Bit 1 is set when the selected drive unit is offline, or is performing a seek or restore operation.

3.5.1.3 Write-Protect (WP) — W0, Bit 2. Bit 2 is set when the write-protect status (WRITE PROTECT switch) of the selected unit is on. When activated, the write-protect circuit inhibits disk drive write logic and neither format information nor data can be written on the disk.

3.5.1.4 Unsafe (US) — W0, Bit 3. The drive unsafe bit indicates that a fault condition exists that prevents any disk operation (except a restore operation) from being executed. This bit is set if the controller determines that more than one drive unit is selected, no drive unit is selected, no terminator board is installed, or a disk drive fault (such as a dc voltage fault or head select fault) has been reported. A restore command clears unsafe status if the condition causing the unsafe status no longer exists.

3.5.1.5 End of Cylinder (EC) — W0, Bit 4. The end of cylinder bit is set when an illegal head address has been received by the disk drive or the head has been incremented beyond four.

3.5.1.6 Seek Incomplete (SI) — W0, Bit 5. The seek incomplete bit is set if the head carriage has failed to locate the specified cylinder. For example, if the word address is out of range, the operation fails and seek incomplete status is reported. Some seek incomplete errors may be due to an error in the disk drive positioning logic. The system may recover from these errors by performing a restore operation and repeating the desired operation.

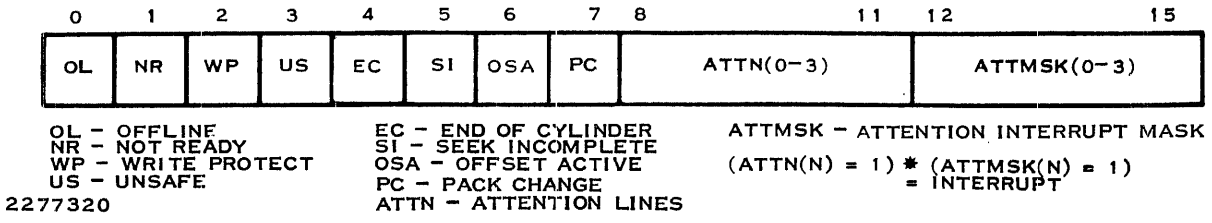

Figure 3-3. Control and Status Word W0 Format

3.5.1.7 Offset Active (OA) — W0, Bit 6. The head offset bit is set if the disk drive carriage offset circuit is active. If data on a selected track is unrecoverable using the normal head position, the CPU can command the controller to attempt data recovery with the head slightly offset, either toward the center of the disk (forward offset) or toward the outer edge of the disk (reverse offset).

3.5.1.8 Pack Change (PC) — W0, Bit 7. The pack change bit is set if a drive unit has not been identified previously to software, or if there has been some parameter change since the last restore command. For example, a power-down cycle or drive sequencing results in PC status the next time the disk drive is selected. A restore command clears PC status. (Note that a store registers command is generally included with a restore command to ensure compatibility with other disk systems.) When PC status is reported, the volume information should be checked to verify that the desired volume is installed.

3.5.1.9 Attention Lines (ATTN0-3) — W0, Bits 8 through 11. The attention bit for a particular disk drive unit is set if either the unit is ready or a seek error has occurred. The bit is used to indicate whether a disk operation, generally a seek or restore, has completed. Since seek and restore commands are relatively slow electromechanical operations, overlapped independent seek and restore capabilities are included in DSRs to speed system throughput. The attention lines (combined with interrupt mask bits 12 through 15) interrupt the 990 processor when seek and restore operations are completed. Read, write, or other operations may proceed on any disk drive not actively executing a seek or restore command.

3.5.1.10 Attention Interrupt Mask (ATTMSK0-3) — W0, Bits 12 through 15. Bits 12 through 15 form a position-coded attention interrupt mask. An interrupt to the 990 processor is generated if the attention mask bit and the corresponding attention bit are both set.

If operations are to be overlapped, the control words for subsequent operations must not erase the attention mask, or the interrupt will not occur. Instead of using a move (MOV) instruction to write a whole new value into W0, the programmer should use a set ones corresponding (SOC) or set zeros corresponding (SZC) instruction to modify bits of W0 as needed.

Note that since there are two possible causes for an interrupt to the CPU, it is not sufficient to assume that the first interrupt after initiating a restore command is an attention interrupt.

3.5.2 W1 — Command Code and Surface Address

W1 (Figure 3-4) contains the command code that specifies the desired controller operation and the head address. Bits 0 through 9 control requested operations; bits 11 through 15 contain the surface address. This word is generally used only as a control word; however, the head address is incremented as disk operations are performed, and the head address at the end of an operation can be read for diagnostic purposes, if desired. Bit functions are described in the following paragraphs.

3.5.2.1 Extended Mode (EXTCMD) — W1, Bits 0 and 1. The three command code bits (W1, bits 5 through 7) allow up to eight unique commands. The extended mode bits (bits 0 and 1), used in conjunction with bits 5 through 7, increase this number by up to 32. If either or both of the extended mode bits are set, the command field in bits 5 through 7 is interpreted as an extended command. Extended commands are less commonly used functions, such as read unformatted and extended test. Refer to paragraph 3.6.1 for more information concerning extended mode commands.

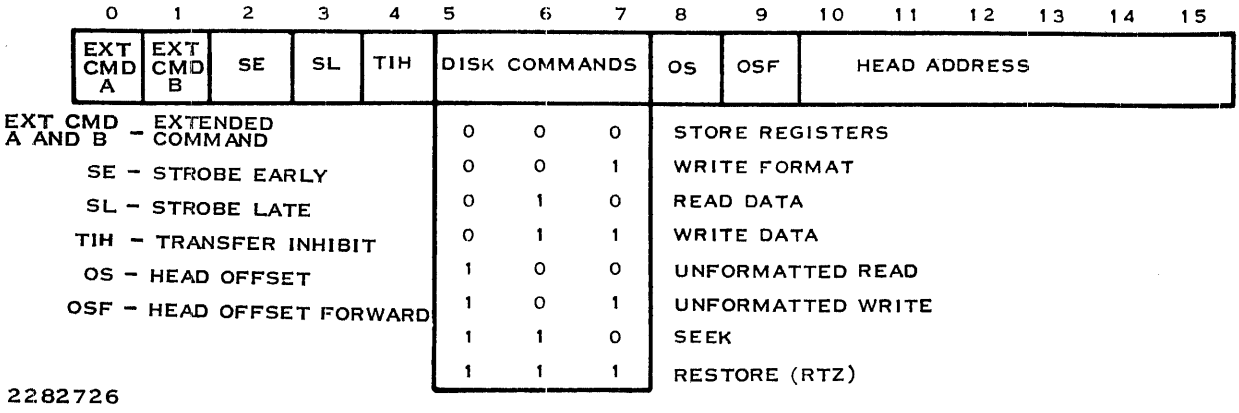

Figure 3-4. Control and Status Word W1 Format

3.5.2.2 Unused — W1, Bit 1. Bit 1 is not used, and should be set to zero.

3.5.2.3 Strobe Early (SE) — W1, Bit 2. When bit 2 is set, the disk drive advances the data strobe. This bit is used with the read data and the unformatted read commands in an attempt to recover data that yields errors when read with normal strobe setting.

3.5.2.4 Strobe Late (SL) — W1, Bit 3. When bit 3 is set, the disk drive retards the data strobe. This bit is used with the read data and the unformatted read commands in an attempt to recover data that yields errors when read with normal strobe settings.

3.5.2.5 Transfer Inhibit (TIH) — W1, Bit 4. When transfer inhibit is set, data is read from the disk, but not transferred on the TILINE. The transfer inhibit function allows the operating system software to check the data integrity of a record without having to provide a memory buffer area to hold the data. When data is read by the controller, the ECC is generated and compared with the ECC generated when the record was written on disk. ECCs that agree indicate a high probability of data integrity.

If the ECC character recorded with the data does not correspond with the ECC character calculated during the read operation, the controller attempts to read the data again. If, after a predetermined number of retries, the controller is still unable to read a sector and obtain equal ECCs, the data error status bit is set.

3.5.2.6 Command Codes — W1, Bits 5 through 7. Table 3-1 lists the normal and extended mode codes and the command names. Detailed command word descriptions and examples are given in paragraph 3.6.

Table 3-1. Command Codes

Extended Mode Bit 0	Extended Mode Bit 1	Command Code Bit 5	Command Code Bit 6	Command Code Bit 7	Command
0	0	0	0	0	Store Registers
0	0	0	0	1	Write Format
0	0	0	1	0	Read Data
0	0	0	1	1	Write Data
0	0	1	0	0	Read Unformatted[1]
0	0	1	0	1	Write Unformatted
0	0	1	1	0	Seek
0	0	1	1	1	Restore
1	0	0	0	0	Store Registers[2]
1	0	0	0	1	Write Format[2]
1	0	0	1	0	Read Data[2]
1	0	0	1	1	Write Data[2]
1	0	1	0	0	Read Unformatted
1	0	1	0	1	Write Unformatted[2]
1	0	1	1	0	Seek
1	0	1	1	1	Self-Test
1	1	0	0	1	Absolute Write Format
0	1	0	0	1	Relocate

Notes:

[1] This command does not actually read unformatted data. Refer to paragraph 3.6.2.1 for operation.

[2] These extended commands perform the same operations that the unextended commands perform. However, to maintain compatibility with other disk systems, only the corresponding unextended command should be used.

3.5.2.7 Head Offset — W1, Bit 8. Bit 8 of W1 is set if data is to be read from the disk with the head offset, either forward or reverse.

3.5.2.8 Head Offset Forward — W1, Bit 9. If bit 8 has been set, bit 9 specifies the direction of the offset. It is set (1) if data is to be read from the disk with the head offset forward, and is not set (0) if data is to be read with the head offset reverse.

3.5.2.9 Head Address — W1, Bits 10 through 15. Bits 10 through 15 select a read/write head and associated platter surface using a standard binary representation. Bit 15 is the LSB.

3.5.3 Sectors per Record and Sector Address — W2

W2 (Figure 3-5) determines the number of sectors per record and the address of each sector. Normally, this word is used only for commands; however, the sector address is updated during disk drive operations, and can be read for diagnostic purposes. The following paragraphs describe the bit functions of this word.

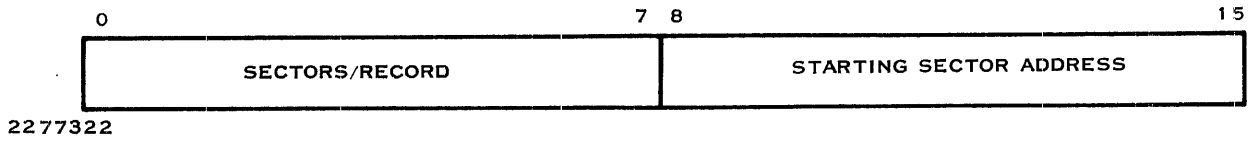

Figure 3-5. Control and Status Word W2 Format

3.5.3.1 Sectors per Record — W2, Bits 0 through 7. Since the recording format is always one sector per record, these bits are ignored by the controller. However, these bits should always be set to >01 to ensure compatibility with other TI disk systems.

3.5.3.2 Starting Sector Address — W2, Bits 8 through 15. These bits select the starting sector for any read or write operation except write format, which does not require a starting sector address. The valid range for sector addresses is >00 to >3C.

A starting sector address larger than the maximum sector address causes a command time out status because the controller cannot locate a starting sector address at which to start executing the command.

W2 also may contain a self-test failure code as a result of self-tests initiated by a CPU command, upon power-up, or by a CPU I/O reset. In any case, a self-test failure causes all ones (FF) to be reported in the right byte of W7, and a 16-bit failure code in W2 (refer to the *Model DS80 Disk System Field Maintenance Manual*, part number 2302630-9701 for more information).

3.5.4 Cylinder Address — W3

W3 (Figure 3-6) selects the cylinder address to which the disk seeks for a read or write operation. The valid number range is >0000 through >032C. This field is also used during self-tests to specify test numbers. Normally, this word is used only for control; however, the cylinder address is updated during disk operations and can be read for diagnostic purposes.

The head address in W1, the sector address in W2, and the cylinder address in W3 form a complete address that locates a record on the disk.

An invalid cylinder address results in a termination, and the unit error (UE) controller status bit in W7 will be set.

Figure 3-6. Control and Status Word W3 Format

3.5.5 Transfer Byte Count — W4

W4 (Figure 3-7) selects the number of eight-bit data bytes to be transferred between the disk and the TILINE. The LSB, bit 15, must be 0 so that only even byte counts can be specified because data is composed of two-byte words. The byte count range is limited by available TILINE memory and the 64K-byte maximum specified in this control word. An attempt to transfer from nonexistent TILINE memory results in TILINE time-out (TT) controller status.

NOTE

If a read with transfer inhibit is selected, the transfer byte count specifies the number of logically sequential bytes to be read from the disk and checked by ECC for data integrity. However, no data is transferred to CPU memory.

3.5.6 Memory Address (LSB) — W5

The TILINE starting address is 20 bits in length. The 15 LSBs occupy bits 0–14 of W5 (Figure 3-8). The five MSBs are located in W6. Bit 15 of W5 must be held to zero because data is composed of two-byte words. Normally, this word is used only as a control word; however, the complete TILINE starting address is incremented during disk drive operations and can be read for diagnostic purposes. If no faults occur, the address in these words should be the ending TILINE memory address. If a memory error causes termination of an operation, the address in this word indicates the byte address of the memory error + 2 (to reflect two-byte words), because the TILINE address is incremented once before the memory error terminates the operation.

During read or write operations, the controller acts as a TILINE master and can store data in or read data from a buffer area in 990 memory. This word specifies the 15 LSBs of the 20-bit TILINE address for the start of the TILINE memory buffer address space. The controller accesses memory starting at the specified TILINE address and increments for the specified word count.

For a read operation, the software must allocate a contiguous area in TILINE memory large enough to accept the data transfer without overwriting other regions of memory.

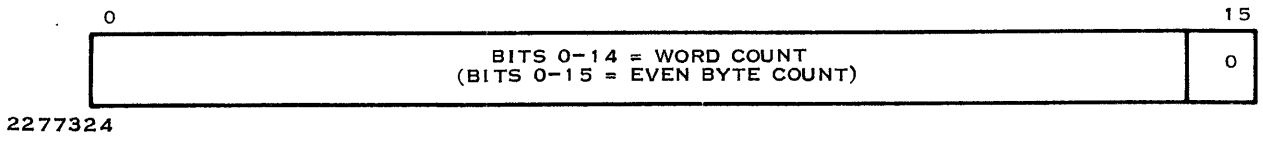

Figure 3-7. Control and Status Word W4 Format

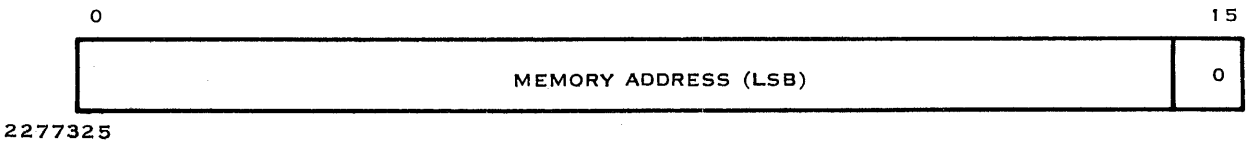

Figure 3-8. Control and Status Word W5 Format

3.5.7 Unit Select and Memory Address (MSB) — W6

W6 (Figure 3-9) contains the unit select bits and the MSBs of the TILINE buffer memory as described in the previous paragraph. Bits 0 through 3 and 8 through 10 are reserved and should be set to 0.

3.5.7.1 Drive Select — W6, Bits 4 through 7. Bits 4 through 7 are a position-coded unit select field. Only one bit position in this field should be set to one. Any code with two or more ones results in an offline status report, and no drive operation will be performed. The valid unit select codes are:

Word 6 Bit				Unit Selected
4	5	6	7	
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3

3.5.7.2 Memory Address (MSB) — W6, Bits 11 through 15. The five MSBs of the 20-bit TILINE memory buffer starting address occupy bits 11 through 15. Refer to the W5 description (paragraph 3.5.6) for additional information.

3.5.8 Controller Status — W7

W7 (Figure 3-10) is used as a control word to set the interrupt enable bit, if desired, and to set the idle/busy bit that initiates controller operation. Controller status is held in this word at the end of an operation. If bits 8 through 15 are all set, a self-test failure has been detected.

3.5.8.1 Idle/Busy Control/Status — W7, Bit 0. The controller must be in the idle mode (bit 0 = 1) for the processor to write control words into the controller, or to read any status other than the idle/busy status bit. This prevents interference with the operation in progress.

After verifying that the controller is idle, control words 0 through 6 may be sent to the controller. Controller operation is initiated when a word with a zero in bit 0 is transmitted to W7.

3.5.8.2 Complete — W7, Bit 1. The complete bit is set by the controller upon error-free completion of a command. The programmer may reset this bit as part of the interrupt service or status checking routine, or may leave it alone until the next block of control words is sent to the controller.

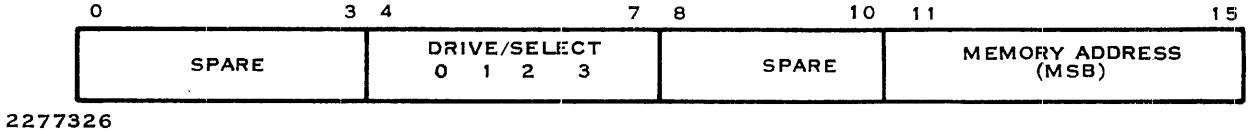

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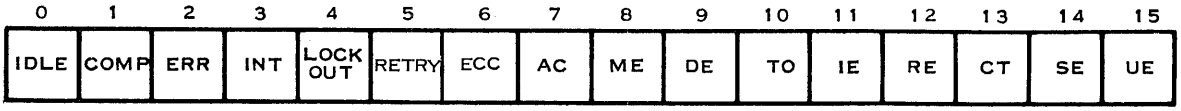
Figure 3-9. Control and Status Word W6 Format



COMP – COMPLETE
ERR – ERROR
INT – INTERRUPT ENABLE
RETRY – CONTROLLER EXECUTED RE-READ
ECC – ECC CORRECTED
AC – ABNORMAL COMPLETION

ME – MEMORY ERROR
DE – DATA ERROR
TO – TILINE TIMEOUT
IE – ID ERROR

RE – RATE ERROR
CT – COMMAND TIMER
SE – SEARCH ERROR
UE – UNIT ERROR

NOTE: IF SELF TEST FAILS, BITS 7 THROUGH 15 ARE ALL SET.

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Figure 3-10. Control and Status Word W7 Format

3.5.8.3 Error — W7, Bit 2. W7, bit 2 is set if an error is detected. The programmer may obtain more detailed error information by examining W7, bits 7 through 15 and W0, bits 0 through 5.

3.5.8.4 Interrupt Enable — W7, Bit 3. Bit 3 may be set to enable the controller to generate an interrupt on normal completion (W7, bit 1) or error termination (W7, bit 2). A command completion interrupt occurs when the following logical condition is met:

IDLE and [(COMPLETE and INTERRUPT ENABLE) or (ERROR and INTERRUPT ENABLE)]

Note that if the enable interrupt bit is set while the controller is idle and the complete or error bit is set, an interrupt is generated immediately. The interrupt enable bit should always be set simultaneously with resetting the idle bit when controller operation is initiated.

The attention interrupts (described with W0, bits 8 through 11 and 12 through 15) are independent of the interrupt enable bit. The attention interrupts are associated with completion of a disk drive operation that may be overlapped with operations involving different drives. The program must read and test the controller status words to determine the cause of an interrupt.

3.5.8.5 Lockout — W7, Bit 4. Bit 4 is set by the controller when W7 is first read. This bit is reset upon power-up and at the end of a command sequence.

3.5.8.6 Retry — W7, Bit 5. Bit 5 is set by the controller to indicate that the controller performed a reread of the data during the last operation because of a data error detected during one or more read operations.

3.5.8.7 ECC Corrected — W7, Bit 6. When bit 6 is set, the ECC routine has corrected bits either somewhere in the data or header of the sector just read, or during the last operation for multiple sector operations.

3.5.8.8 Controller Status — W7, Bits 7 through 15. These bits are used to report controller status after a command has been executed. Valid error information is contained when the error bit (W7, bit 2) is set. Bits 8 through 15 are all on in the event of a self-test failure. If the next command after a self-test failure involves a drive operation, bits 8 through 15 will not clear and the operation will be inhibited. An I/O reset or power reset clears the controller logic and performs a self-test.

Abnormal Completion — W7, Bit 7. Bit 7 is set if a disk operation is terminated because an I/O reset, TILINE power failure warning pulse, or TILINE power reset has been detected.

Memory Error (ME) — W7, Bit 8. The memory error bit is set if a TILINE memory error (ME) is detected during a disk write command. If ME is detected during a write data or write format operation (normal or extended), bad data may have been read from memory and recorded on the disk. All data transfer operations are terminated after ME is encountered. Any remaining data counts are not transferred.

Data Error (DE) — W7, Bit 9. W7, bit 9 is set during a read operation if the calculated ECC character detected an error but was unable to find a correctable pattern in the data stream.

TILINE Time-out (TT) — W7, Bit 10. In order to prevent an error from indefinitely hanging the TILINE, all TILINE peripheral controllers incorporate a timer that allots up to 12 microseconds for a TILINE operation. If the timer expires before completion of the TILINE cycle, the TILINE cycle as well as controller operation is terminated. The TT bit is then set.

The most common cause for a TILINE time-out is a controller attempt to read or write to a nonexistent memory location. A restore operation cannot cause a TILINE time-out.

ID Error (IE) — W7, Bit 11. This bit is set when an ID word comparison error occurs during the ID verification of a read data or write data command. Verification includes comparison of ID words 1, 2, and 3 (the header words) and ECC checking. If bit 9 (data error, DE) is also set, it indicates that the ECC has detected an error in the sector. IE causes command termination.

Rate Error (RE) — W7, Bit 12. The data transfer rate from the disk during a read operation is fixed, but the TILINE data transfer rate from controller to memory is determined by bus activity and priority. Data transfers are corrupted when the TILINE is unable to keep up with the disk interface rate. When this condition occurs, the rate error bit is set.

In a similar way, a TILINE overload during a write data operation corrupts the data recorded on the disk. When this condition occurs, the rate error bit is also set.

All data transfer operations are terminated after RE is encountered.

Command Time-out (CT) — W7, Bit 13. The controller is allotted a predetermined amount of time for each command. If the controller fails to complete the operation before the timer expires, command time-out is set and the operation is terminated. The timer is restarted each time a seek operation is executed, a head address is set or incremented, the controller is at the beginning of the idle routine, or the disk drive power up sequence begins. This bit is also set if a byte count greater than 510 is given for any unformatted command.

Search Error (SE) — W7, Bit 14. Bit 14 is set if the controller does not detect a sync character within one physical sector while attempting to read from the disk. SE causes command termination. No controller retries are attempted after a search error.

Unit Error (UE) — W7, Bit 15. Bit 15 is set when an operation is terminated because of a disk drive error. Causes of a unit error depend upon the command being executed when the error condition is encountered, as follows:

Command	Causes
Restore	Offline
Unextended read unformatted	Offline, not ready, unsafe, seek incomplete, or offset active
Write data, write formatted, write unformatted	Offline, not ready, unsafe, seek incomplete, offset active, or write-protect
Read data, extended read unformatted	Offline, unsafe, seek incomplete, offset active*
Seek	Offline, unsafe, seek incomplete, offset active
Store registers	Offline, not ready, unsafe, offset active, seek error

Note:

* During read commands, offset active creates a unit error only during command initialization and termination.

3.6 DETAILED COMMAND DESCRIPTIONS AND EXAMPLES

3.6.1 Normal Commands

The normal or nonextended commands are the eight commands for which the extended mode bits (W1, bits 0 and 1) are not set; store registers, write format, read data, write data, unformatted read, unformatted write, seek, and restore. These basic commands are used for most normal data storage and retrieval.

3.6.1.1 Store Registers Command. The store registers command provides a means for the operating system software to interrogate a disk system to determine critical parameters such as words per track and cylinders available per drive unit. This command causes the controller to send one, two, or three words to the 990 memory from the disk system, starting at the memory address specified in W5 and W6, and specified by the word count in W4. The three words (Figure 3-11), contain the following information:

- Word 1 — Word 1 is the total number of unformatted words that can be recorded on a disk track.
- Word 2 — Bits 0 through 7 of word 2 specify the number of sectors per track, and bits 8 through 15 specify the number of bytes of overhead per record.
- Word 3 — Bits 0 through 4 of word 3 specify the number of tracks per cylinder and bits 5 through 15 specify the number of cylinders per drive.

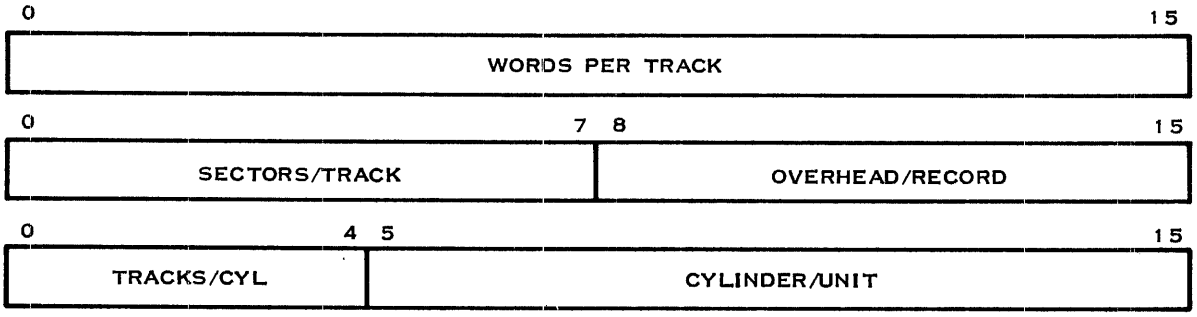

Figure 3-11. Store Registers Data Format

When the drive is interrogated by a store registers command, the following values are returned:

Word 1	>1E80
Word 2	>3D00
Word 3	>2B23

An example of control words used to initiate a store registers operation is given in Table 3-2.

Table 3-2. Example of Control Words in a Store Registers Command

Word Number	Word	Comments
0	>0000	Clear attention mask bits
1	>0000	Store registers command
2	>0000	Not used
3	>0000	Not used
4	>0006	Byte count = 6
5	>1000	Write three words in memory beginning with TILINE byte address >001000
6	>0800	Select drive unit 0; TILINE address MSB = 0
7	>0000	Reset status bits; initiate controller operation

NOTE

A drive must be selected (word 6). If no drive is selected, the disk status word after the command is complete will have the not ready and offline status bits set, the controller status word will have the error and unit error bits set, and no data will be transferred to memory.

3.6.1.2 Write Format Command. The write format command formats a new disk or reformats a disk already in service. One complete track is formatted per command. After receiving all command words, the controller verifies correct disk status (offline, not ready, unsafe, write-protect, offset active, or seek incomplete), seeks to the specified cylinder, and sets the specified head address. A verify ID and ECC are done after the seek. If the specified track is spared, the controller then seeks to the spare track, and formats that track. If the verify ID fails due to a data error or search error, the verify operation is retried up to three times. If the operation is still unsuccessful, the retry bit (bit 5) is reported and the track is then formatted. The controller assembles the ID words from its internal registers and counters and records the word(s) on the disk as header at the specified disk track address. The controller then fills the entire data field following the ID words by repeating a fill data word fetched from the specified TILINE memory address. The ECC is then appended to the data field. Each sector on the track is formatted in this manner with ID words, data, ECC, and required gaps. Figure 3-12 shows the data format of the header, and Table 3-3 shows an example of the control words used to initiate a write format operation.

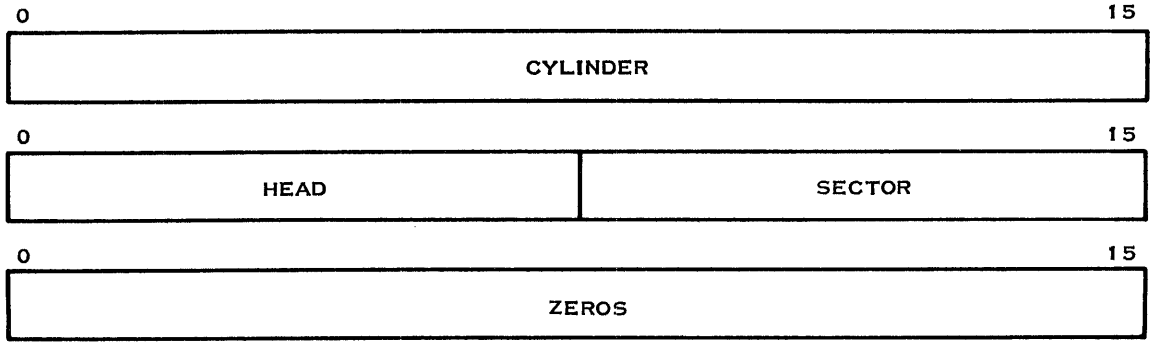

Figure 3-12. Header Data Format

3.6.1.3 Read Data Command. The read data command words identify a record location, specify the number of bytes to be transferred from this location, and give the starting address for the TILINE memory address buffer area to receive data from the disk.

After initialization, the controller performs the following operations:

1. Checks for unit errors by examining disk status (offline, end of cylinder, offset active not ready, unsafe, and seek incomplete).

2. Verfies the ID. If an error occurs, which implies that the carriage is not at the proper location, a seek is issued to position the carriage over the proper track.

3. Verifies the ID if a seek was issued in step 2. This second verification determines if the track now under the heads has been relocated to a spare cylinder. If the ID shows that it has been relocated, an additional seek is then performed to access the relocated track. If errors occur on this verification, it is retried up to three times or until a sector is read without error. If an error still occurs, the appropriate error is set and the operation terminates.

4. Locates the desired starting sector by monitoring the disk drive sector counter and comparing its contents to the desired sector address. When the controller determines that the sector under the heads is the sector immediately before the desired sector, it arms the interface so that the read operation is started when the next sector mark occurs.

5. Reads and assembles 16-bit words from the sector data field.

6. Transfers these words to the specified TILINE address, if transfer inhibit is not set.

7. Verifies the 32-bit ECC character for both the data field and header for the sectors from which data is being transferred.

Table 3-3. Example of Control Words in a Write Format Command

Word Number	Word	Comments
0	0000	Clear attention mask bits
1	0101	Write format command; head address = 1
2	0100	One sector/record, starting sector address not required
3	00CA	Cylinder address = >CA
4	0000	Not used (variable record lengths are not supported)
5	1000	TILINE memory byte address of formatting data word = >001000
6	0800	Selected drive unit 0; TILINE address MSB = 0
7	1000	Reset status bits, set interrupt enable, initiate controller operation

A failure to verify an ID word results in an ID error status (bit 11) and termination of the read data operation. If the ECC is incorrect for the sector from which data is being read, data error status (bit 9) is also set. When the controller encounters the end of a sector but the remaining transfer word count is nonzero, the controller automatically continues reading data on the next sequential logical sector, if it exists. The controller automatically switches heads and/or cylinders if necessary to access the next logical sector.

When the remaining transfer word count is zero but the controller has not encountered the end of a sector, the controller discontinues transmitting data words across the TILINE but continues to read data from the disk until the end of the sector is encountered so that the ECC character can be checked before loading status.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track. The controller then repeats steps 4 through 8 of the process presented in the list at the beginning of this paragraph.

When the controller encounters the end of a cylinder, and the remaining transfer word count is nonzero, and head offset is not specified, the controller automatically seeks to the next cylinder and selects head address zero for the new track. The controller then repeats steps 4 through 8 of the process presented in the list at the beginning of this paragraph.

Table 3-4 shows an example of the command words used to execute a read data operation.

Table 3-4. Example of Control Words in a Read Data Command

Word Number	Word	Comments
0	>0000	Clear attention mask bits
1	>0200	Read data command; head address 0
2	>0100	One sector/record; starting sector 0
3	>0000	Cylinder address = 0
4	>2000	Transfer >2000 bytes
5	>0000	TILINE memory byte address = >1F0000
6	>041F	Select drive 1; TILINE address MSB = 1F
7	>0000	Reset status bits, interrupts not used; initiate controller operation

3.6.1.4 Write Data Command. The write data command causes the controller to record data on a previously formatted track, or to write over a previously recorded sector. After initialization, the disk controller performs the following operations:

1. Checks for unit errors by examining disk status (offline, end of cylinder, not ready, unsafe, write-protect, offset active, or seek incomplete).

2. Verifies the ID. If an error occurs, which implies that the carriage is not at the proper location, a seek is issued to position the carriage over the proper track.

3. Verifies the ID if a seek was issued in step 2. This second verification determines if the track now under the heads has been relocated to a spare cylinder. If the ID shows that it has been relocated, an additional seek is then performed to access the relocated track. If errors occur on this verification, it is retried up to three times or until a sector is read without error. If an error still occurs, the appropriate error is set and the operation terminates.

4. Locates the desired starting sector by monitoring the disk drive sector counter and comparing its contents to the desired sector address. When the controller determines that the sector under the heads is the sector immediately before the desired sector, it arms the interface so that the write operation is started when the next sector mark occurs.

5. Leaves a leading gap, and writes a synchronization character, header, data from the specified TILINE memory location, and ECC character. Leaves a trailing gap at the end of the sector.

If the ID words in step 4 do not compare, the write operation is terminated with an ID status error.

Data is written on the disk until the specified number of words have been transferred unless a terminate condition is encountered. When the transfer word count is less than the sector word count, the controller fills the remainder of the sector with zeros until the sector word count has been decremented to zero. When the number of words is greater than the words per sector, the controller continues to the next sequential sector.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track and selects sector 0 as the next sector to be written. The controller then repeats steps 4 through 7 of the process presented in the list at the beginning of this paragraph.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder, selects head address zero for the new cylinder, and selects sector 0 as the next sector to be written. The controller then repeats steps 4 through 7 of the process presented in the list at the beginning of this paragraph.

Table 3-5 is an example of the command words that execute a write data operation.

Table 3-6 is an example of the status words returned to word locations W0 through W7 after a typical write data operation has been performed. Note that cylinder, head, and sector information have been updated, as well as TILINE memory address. Also note that the word count has decremented to zero. This example is typical for any read or write operation.

Table 3-5. Example of Control Words in a Write Data Command

Word Number	Word	Comment
0	>0000	Reset attention mask bits
1	>0304	Write data command; select head number 4
2	>013C	One sector per record; start writing at sector address >3C
3	>0300	Cylinder address = >300
4	>0300	Transfer byte count = >300
5	>9700	Starting TILINE memory address = >009700
6	>0400	Select drive unit 1; TILINE address MSB = 0
7	>1000	Reset status bits; set interrupt enable; initiate controller operation

Table 3-6. Example of Status Words After Write Operation

Word Number	Word	Comments
0	>00B0	Attention bits for drive units 0, 2 and 3 are set; no unit errors occurred
1	>0300	Head address has been updated to head 0
2	>0101	Sector address has been updated to ending sector address of >1
3	>0301	Cylinder address has been updated to >0301
4	>0000	Word count has been decremented to 0
5	>9A00	TILINE memory address has been incremented to >9A00
6	>0400	TILINE MSB memory address remains >0
7	>D000	Controller idle; operation complete; interrupt enabled; no errors detected

3.6.1.5 Unformatted Read Command. This command is included in order to insure compatibility with Texas Instruments DSRs that acquire disk parameters by reading header information. The unformatted read command (nonextended) does not actually read any data from the disk. Instead, three words are returned to the CPU after this command is executed. Word one of the three returned words contains the head and cylinder addresses; the second word contains the sectors per record number, which is >01, and the sector address; and the third word contains the record word count, which is >80. If a genuine unformatted read operation is desired, the extended unformatted read command words can be used.

3.6.1.6 Unformatted Write Command. An unformatted write command transfers up to 510 bytes of data from a specified TILINE address to a specified disk address. After initialization, the controller seeks to the specified cylinder, selects the specified head address, detects the beginning of sector, generates the correct lead gap, writes a synchronization character, and writes data on the disk. All data is written consecutively without regard to existing sector boundaries until the specified number of words has been transferred or until a termination condition is encountered. The controller adds an ECC character and a trailing gap at the end of the data.

NOTE

The maximum transfer count is 510 bytes.

3.6.1.7 Seek Command. The seek command causes the drive to orient the heads at the cylinder specified in the command words. An interrupt can be generated, if desired, to alert the CPU that this operation has been completed. This operation is used while a different, on-going operation is in progress to complete the relatively slow seek operation before the drive is actually commanded to read or write. Table 3-7 shows an example of the control words used to initiate a seek operation.

Prior to execution of a seek operation, the controller performs a verify ID operation. If an error occurs, which indicates that the head is not over the desired cylinder, the seek operation is then executed. Note that no error is reported in this case.

3.6.1.8 Restore Command. The restore command reinitializes the cylinder counter and repositions the heads of the selected disk drive unit over cylinder zero. The restore command is generally used to clear an unsafe condition at the disk drive. This command is required if seek incomplete or unsafe status is detected. Before executing the restore operation, the controller finds out whether a unit error exists by examining offline disk status. If it finds a unit error before it initiates the restore command, it sets the unit error bit in W7. Completion of the restore operation is determined by enabling a disk drive completion interrupt (attention bit interrupt) or by monitoring the attention bit for the selected drive unit.

3.6.2 Extended Mode Commands

The extended mode commands are those commands for which the extended mode bit (word 1, bit 0) is set. The extended mode bit allows the command code field (word 1, bits 5 through 7) to select from an additional set of commands. These are the commands that are less commonly used during the course of data storage and retrieval operations.

Refer to paragraph 3.5 for the complete set of unextended and extended mode commands. Except for the extended read unformatted and extended self-test commands, extended mode commands perform functions identical to the unextended commands.

Table 3-7. Example of Control Words in a Seek Command

Word Number	Word	Comments
0	>0000	Clear attention mask bits
1	>0601	Seek command; head address = 1
2	>0100	One sector/record; starting sector address not required.
3	>00CA	Cylinder address = >CA
4	>0000	Word count not used
5	>0000	Memory address not used
6	>0800	Selected drive unit 0
7	>1000	Reset status bits; set interrupt enable; initiate controller operation

3.6.2.1 Read Unformatted (100 — Extended). The extended unformatted read command allows the programmer to read a sector and to examine a specified number of words starting immediately after the sync character without regard to ECC errors or standard sector formatting. This is primarily a diagnostic feature.

After initiation, the controller selects the proper head and seeks to the specified cylinder. When the sector is located, the controller transfers the specified number of words to TILINE memory, starting with the first word after the sync character.

The ID words, data fields, ECC words, and trailing gap are read and transferred to memory as though they were all data words. There are normally glitches in the trailing gap due to write head turn-on and turn-off transients and differing write clock phases recorded during formatting and write operations. These glitches may cause apparent shifting of word boundaries.

An ECC check is performed at the end of the operation, and data error status is reported if the ECC check shows an error. However, no ECC correction is attempted.

The word transfer count is limited to 510 bytes. Command time-out occurs if too many bytes are requested. An example of the command words used to initiate an extended read unformatted operation is given in Table 3-8.

Table 3-8. Example of Control Words in an Extended Unformatted Read Command

Word Number	Word	Comment
0	>0000	Resets attention mask bits
1	>8401	Extended read unformatted command; select head 1
2	>0101	One sector per record; starting sector address = 1
3	>00CA	Select cylinder >CA
4	>0006	Transfer three words (6 bytes)
5	>1000	TILINE memory byte address = 001000
6	>0400	Select drive unit 1; TILINE memory address MSB = 0
7	>1000	Enable interrupt; initiate controller operation

3.6.2.2 Self-Test Commands (111 — Extended). This command causes the controller to execute the self-test routines specified by the value in W3. The self-test routines are described in the *Error Correcting Disk Controller Depot Maintenance Manual*, part number 2272082-9701.

Certain of these extended test commands hang the controller in a test loop until an I/O reset or power reset aborts the test. Refer to the depot maintenance manual for a complete description of the self-test routines.

3.6.2.3 Absolute Write Format (001 — Extended). The absolute write format command causes the controller to execute a write format command that formats a disk in the same manner as described for the normal write format command except that the ID is not verified and relocated tracks are ignored. Note that if a bad track is encountered, it is formatted as described in paragraph 3.6.1.2 and any header information that causes the drive to relocate to an alternate track is lost.

3.6.2.4 Relocate (001 — Extended). The relocate command relocates a bad track to a spare track so that all normal disk operations to a bad track are performed on a spare (relocated) track. After initialization, the controller performs the following operations.

1. Verifies ID of the bad track.
2. Formats the bad track so that the header words 1 and 2 contain the cylinder and the head and sector address of the bad track, and word 3 contains the bad track flag (>8000).
3. Seeks to the spare track address.

4. Verifies the spare track ID.

5. Formats the spare track address with the header of the bad track and the fill word specified by the relocate command at the TILINE address plus 2.

The format of the relocate command is as follows.

- Word 0 — Zeros
- Word 1 — Most significant byte: >41; least significant byte: head address of bad track
- Word 2 — Zeros
- Word 3 — Cylinder address of bad track
- Word 4 — TILINE byte count: >0004
- Word 5 — TILINE address
- Word 6 — Unit address and TILINE address
- Word 7 — Zeros

Two words must be placed at the TILINE address (word 5) and the TILINE address plus 2. The first word at the TILINE address must contain the spare track address; bits 0 through 4 must contain the head address, and bits 5 through 15 must contain the cylinder address. The second word at TILINE address plus 2 must contain the fill word used to format the spare track.

Table 3-9 shows an example of the command codes for a relocate command.

Table 3-9. Example of the Command Codes for a Relocate Command

Word Number	Word	Comments
0	>0000	Zeros
1	>4100	Relocate command; head address 0
2	>0000	Zeros
3	>0008	Cylinder address = 0008
4	>0004	Byte count = 4
5	>0000	TILINE memory address = 1F0000
6	>041F	Select drive 1; TILINE address MSB = 1F
7	>0000	Restart status bits, initiate controller operation

4

Operation

4.1 GENERAL

This section describes normal operating procedures for the Model DS80 disk system, including:

- Power-up, stop, and power-down
- Disk pack criteria, handling, installation, storage, and removal
- Fault operation

The TILINE disk controller requires no operator intervention after installation. On-board controls and indicators are intended only for installation and maintenance use. The controller should be serviced only by qualified personnel. Before operating, read and observe all of the following listed precautions.

Operating Precautions

To prevent damage, observe the following precautions when operating the disk drive.

1. Keep the disk pack cover closed at all times to prevent entry of atmospheric contaminants.
2. If a pinging or scratching sound (caused by head-to-disk contact) is heard and persists, stop the unit by following the stop and power-down procedures found in this section, then call maintenance personnel. If a head crash is suspected, do not place another disk pack into the drive until the system can be checked or else further damage can result to the disk pack and the disk drive.
3. Never use a disk pack suspected of damage in any other disk drive. A damaged disk pack can cause head crashes.
4. Never place heavy test equipment or other heavy objects on top of the disk drive. Do not sit on the disk drive. Never stack disk drives.
5. Always carefully follow disk pack handling, installation, storage and removal procedures found in this section.
6. Use only Texas Instruments supplied disk packs to ensure data integrity and maintain system performance.
7. Never attempt to override any interlocks in the system.

4.2 CONTROLS AND INDICATORS

All operator controls and indicators are located on the front panel except for the PWR ON/OFF circuit breaker, located on the rear panel. Figure 4-1 shows locations of these controls and indicators; Table 4-1 describes their functions.

4.3 DISK PACK CRITERIA, HANDLING, INSTALLATION, STORAGE, AND REMOVAL

The following paragraphs discuss removable disk pack criteria, handling, installation, storage, and removal procedures.

CAUTION

Follow the procedures in this section carefully to prevent damage to the disk drive or disk pack as well as to protect data written on the platters.

4.3.1 Disk Pack Criteria

The disk pack used in the DS80 disk system must meet the following special criteria. For these reasons, Texas Instruments supplied disk packs must be used in the system since standard disk packs do not meet these critical specifications.

1. Cylinder 0 must be error free to ensure reliable operating system performance.
2. All (if any) media defects must appear on the defect map located on the disk pack canister. This defect information is subsequently used by the software operating system to avoid using these tracks.

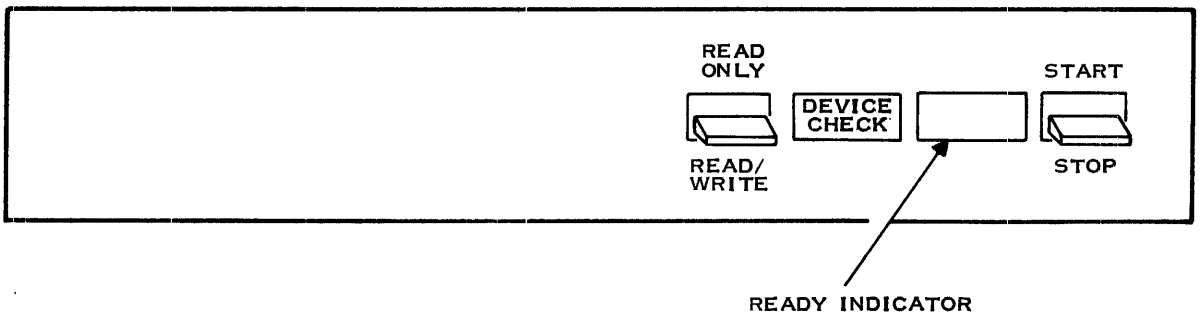

Figure 4-1. Controls and Indicators

Table 4-1. Controls and Indicators

Control or Indicator	Function
START/STOP toggle switch:	When in the START position, energizes the spindle motor and initiates the first seek mode, provided the following conditions are met: 1. The drive PWR ON/OFF switch is ON. 2. The disk pack is loaded and the air shroud lid is closed and latched. 3. The drive DEVICE CHECK light is off. When in the STOP position, removes power from the spindle motor and halts all drive operation.
Ready indicator: (Unlabeled green indicator)	Lights when unit is up to speed, heads are loaded, and no fault exists requiring manual intervention. The indicator blinks throughout the spindle start and stop procedure.
DEVICE CHECK indicator:	Lights to indicate a fault condition. The indicator is reset if the fault condition is cleared or if drive power is recycled.
READ ONLY-READ/WRITE toggle switch:	When in the READ ONLY position, the drive write circuits are disabled, preventing data from being written on any platters. When in the READ/WRITE position, both read and write operations are enabled.
PWR ON/OFF circuit breaker (located on rear panel):	Applies primary ac power to disk drive.

4.3.2 Disk Pack Handling

The disk pack (Figure 4-2) consists of a stack of five separate platters mounted on a spindle hub. The top and bottom platters are protective platters and are not used for recording. Of the middle three platters, five surfaces are used for recording data, and one surface contains prerecorded servo information.The disk pack is enclosed in a rigid plastic canister to protect the disk surfaces from damage and contaminants. Observe the following precautions when handling disk packs.

CAUTION

To prevent dust, dirt, and other foreign material from entering the disk pack and contaminating the platters, always keep the disk pack in its canister when not in use.

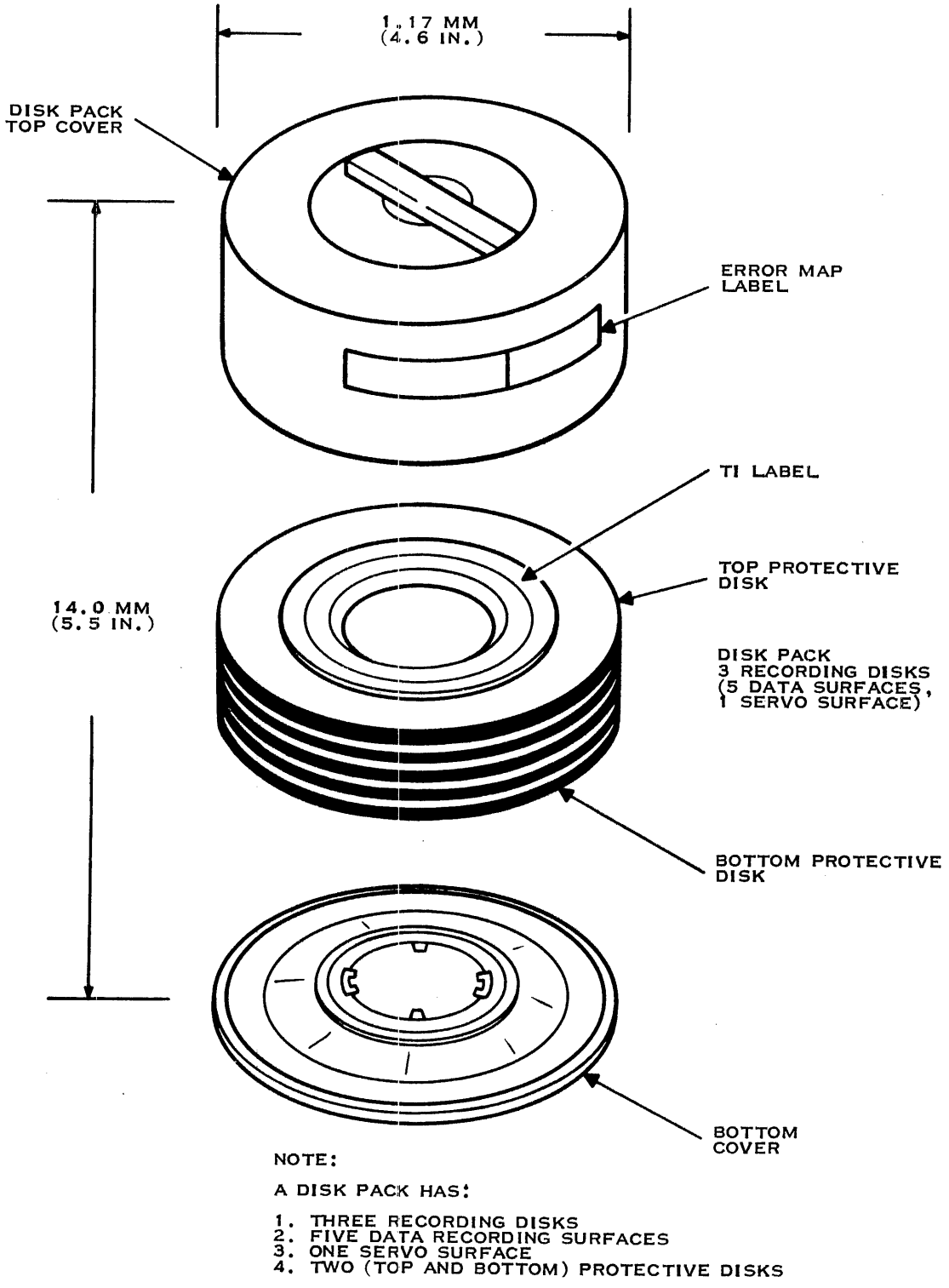

Figure 4-2. Disk Pack

1. Always use the canister handle to transport the disk pack. The handle locks onto the spindle hub and supports the disk pack at its center, which keeps damaging stresses from the platters and hardware.

2. Always attach the bottom cover while holding the pack vertically by the handle.

3. To eliminate damaging or contaminating the exposed bottom platter, never set the disk pack on any surface without having the bottom cover in place.

4. Never stack disk packs.

5. Never disturb the lead weights that are attached to the spindle hub. Tampering with these weights can seriously affect dynamic balance.

6. Never attempt to stop the disk pack from rotating on the drive. The spin-down time is drive-controlled to minimize wear to the drive spindle bearings and to prevent large torques from being transmitted to disk pack components.

4.3.3 Disk Pack Storage

Observe the following precautions when storing disk packs.

CAUTION

Always store disk packs in their canisters (and shipping containers if storing for long periods of time) on a flat surface and in a horizontal position. Never stack disk packs, unless packed in their shipping containers.

1. Store the disk packs in the following environment.

Temperature:	-40 to 60°C (-40 to 150°F)
Humidity:	8 to 80%, excluding all conditions that can cause condensation

2. If a disk drive has been subjected to temperatures outside the operating range of the disk drive (13 to 40°C (55 to 104°F)), store the disk pack in the operating environment for at least 24 hours before use. During this conditioning period, the disk packs should be removed from their shipping container, but not from the protective canister.

3. For long term storage, replace disk packs in their shipping containers. Do not stack shipping containers more than eight high.

4.3.4 Disk Pack Installation

To install a disk pack, perform the following procedure.

NOTE

Power must be applied before opening the disk pack cover.

1. Set the disk drive START/STOP switch to STOP and wait for the green ready light to stop blinking.
2. Unlatch and open the disk pack cover. The cover latch is located above the front panel, centered beneath the front edge overhang.
3. Check the interior of the air shroud. The interior should be clean, and the heads should be completely retracted.
4. Remove the lower cover from the disk pack by pressing the two plastic ears together, and carefully lower the top cover with the disk pack onto the disk drive spindle.
5. Press down the top cover handle to engage the spindle-locking mechanism and rotate the handle clockwise to lock the disk pack to the spindle and to disengage the top cover.
6. Carefully lift the top cover and remove it from the disk drive and close the disk pack cover. Ensure that the disk pack cover latch is locked.
7. If the installed disk pack is a permanent record, set the READ ONLY-READ/WRITE switch to READ ONLY to protect the disk pack from inadvertent overwriting. If the disk pack is to be recorded, set the READ ONLY-READ/WRITE switch to READ/WRITE.
8. Replace the bottom cover on the canister to minimize dust accumulation inside the case.
9. Set the disk drive START/STOP switch to START.

4.3.5 Disk Pack Removal

To remove a disk pack from the disk drive, perform the following procedure.

1. Set the disk drive START/STOP switch to STOP and wait until the green ready light stops blinking and remains out.
2. Unlatch the disk pack cover and open it.
3. Separate the top and bottom covers of the disk pack canister and lower the top cover by the handle over the disk pack.

4. Press down the top cover handle to engage the spindle-locking mechanism and rotate the handle counter-clockwise to unlock the disk pack from the spindle and to reengage the top cover onto the disk pack.

5. Carefully lift the top cover and disk pack from the disk drive and close the disk pack cover.

6. Replace the bottom cover on the disk pack canister and return the pack to storage.

4.4 OPERATING PROCEDURES

The following paragraphs detail disk drive normal operation including power-up, write-protect, stop, and power-down procedures.

4.4.1 Power-Up for Online Operation

Since the disk drive draws a high amount of current upon start-up, disk drives in multiple drive systems should be powered up one at a time to prevent circuit breakers from tripping due to start-up overload. Under normal conditions, the disk controller supervises application of power and start-up of the disk drive. To allow the controller to perform this power application sequencing, ensure that the PWR ON/OFF circuit breakers are ON on all disk drives and the front panel START/STOP switches are set to ON prior to applying power to the CPU. When power is applied to the CPU, the controller automatically sequences power to all drives in the system. If the disk drive(s) in single or multiple drive installations are not powered up and the CPU is powered up and online, perform the following procedure to power up the drive(s):

1. Ensure that the START/STOP switch is set to STOP.
2. Set the PWR ON/OFF circuit breaker on the rear panel to ON.
3. Install a disk pack in the disk drive using the disk pack installation procedures detailed above.
4. Set the START/STOP switch to ON.
5. Verify that the green ready indicator ceases blinking and remains constantly lit. This occurs after the disk drive is up to speed and the heads are loaded (approximately 20 seconds).
6. Verify that the DEVICE CHECK indicator is not lit.
7. Repeat this procedure one at a time for all drives in the system.

4.4.2 Write-Protect

To ensure that data is not inadvertently written on a disk pack, activate the write-protect feature. Set the READ ONLY-READ/WRITE switch to READ ONLY to protect the media in the disk drive. To then disable the write-protect feature, set the switch to READ/WRITE.

4.4.3 Stop

The disk drive can be stopped whether or not a disk function is being performed. If a disk function is being performed, the operation stops, and the carriage retracts. To stop the disk drive, set the START/STOP switch to STOP. The ready indicator blinks until the platters cease rotating. The disk pack now may be removed, if desired, using disk pack removal procedures.

4.4.4 Power-Down

Application and removal of power is generally accomplished by the CPU as described in the power-up procedures. Power-down of a single drive generally is accomplished only by maintenance personnel. If it is necessary to remove power from a disk drive, stop the unit as previously described, ensure that the spindle has stopped rotating (ready light out), and set the PWR ON/OFF circuit breaker on the rear panel to OFF.

4.5 FAULT OPERATION

If the DEVICE CHECK indicator lights during operation or power-up, proceed as follows:

1. Set the START/STOP switch to STOP and wait for the ready light to stop flashing and remain extinguished.

2. Set the START/STOP switch to START. If the DEVICE CHECK indicator lights again after recycling power, an equipment malfunction is indicated. Refer the problem to maintenance personnel. Do not attempt to operate the disk drive.

Appendix A

Self-Tests

A.1 ERROR CORRECTING CONTROLLER SELF-TEST FUNCTION

NOTE

For formats of the control and status words mentioned in the following paragraphs, refer to Figure 3-2.

The controller incorporates extensive self-test routines that isolate faults to specific functional areas of the board. Most of these tests are performed automatically during the power-up sequence, and a short self-test is run before the command execution. Detection of a fault condition sets the last eight bits of status word W7 high and returns the failure code to status word W2. The FAULT LED is enabled automatically at the beginning of the power-up sequence and remains lit until all self-tests successfully complete.

Table A-1 lists each of the self-test routines, and the specific portion of the controller exercised by each test. Control and status word W3 specifies the particular test to be performed. Status word W2 is loaded with the appropriate failure code at the completion of each test. The first eight bits of word W2 contain the failure code and the last eight bits indicate the self-test that failed. Note that a core failure indicates an extensive malfunction that prevents proper execution of the self-test.

Initiation of IORES during the power-up sequence, or interrupt conditions TLPRES or TLPFWP call Test 0. Test 0 (execute all tests) causes Tests 1 through 5, 7 through 9, and Test A to be executed. Test 9 is a short test of the CPE, P-bus, FIFO, and interface logic, and is performed prior to the execution of each controller command.

Each of the self-test routines can be executed individually by the following procedures:

1. Power up the system using normal operating procedures.
2. Enter >8700 into the memory location for control and status word W1. This calls the extended mode self-test command.
3. Specify the particular test desired by entering the most significant byte of the test number into control and status word W3.
4. Execution of Test B requires that a valid unit number be entered into control and status word W6.
5. Enter >0000 in all other control word locations. W7 must be entered last.

6. Upon completion of test execution read location W7 to determine the test results. If the system passes all tests, >C000 is returned (or >C800 if lockout bit is set). If a failure is detected, >A0FF is returned (or >A8FF with lockout).

7. If a failure occurs, read control and status word W2 and refer to Table A-1 for a failure description.

For diagnostic and troubleshooting purposes, a particular self-test routine can be continuously repeated in a scope loop. This is done by setting the most significant bit of control and status word W3 high (other bits are set for the desired self-test) and following the procedures outlined in the foregoing paragraph. For example, if >8800 is loaded into W3, a repeating loop is established for the bidirectional bus and counters test.

Table A-1. Self-Test Descriptions

Test	Word 3	Word 2	Description of Test
0	>0000		Execute all tests. Executes Tests 1 through 5, 7 through 9, and Test A
1	>0100		CPE Test
		>FFFF	Core failure, NRA sequencer, CROM, immediate field decode, CPE
		>FF01	Core failure
		>0801	Carry-in, carry-out bits
		>0701	Branch ROM
		>0601	Arithmetic and logical carry
		>0501	Immediate field
		>0401	Shift operations
		>0301	P-bus constants
		>0201	Clock stop and word select
		>0101	CPE instructions and registers
		>0001	No failure in Test 1
2	>0200		P-bus and A-bus Test
		>FFFF	Core failure
		>FF02	Core failure
		>0102	P-bus
		>0002	No failure in Test 2

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
3	>0300		Register and Register File Clock Test
		>FFFF	Core failure
		>FF03	Core failure
		>0103	Register file and register file clock
		>0003	No failure in Test 3
4	>0400		Interrupts and Command Timer Test
		>FFFF	Core failure
		>FF04	Core failure
		>0104	Interrupts and command timer
		>0004	No failure in Test 4
5	>0500		Master Slave Logic Test
		>FFFF	Core failure
		>FF05	Core failure
		>0205	Idle and memory error bits
		>0105	Busy bit
		>0005	No failure in Test 5
6	>0600		Reserved
		>FFFF	Core Failure
		>0006	No failure in Test 6

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
7	>0700		FIFO Test
		>FFFF	Core failure
		>FF07	Core failure
		>1107	Drive deselect failure, select, drive, I/O cable
		>1007	FIFO not ready, FIFO, FIFO control, CLRFIFO, CLRSTB
		>0F07	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0E07	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0D07	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0C07	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0B07	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0A07	Data pattern >AAAA failed, FIFO
		>0907	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0807	Data pattern >5555 failed, FIFO
		>0707	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0607	Data pattern >9696 failed, FIFO
		>0507	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0407	Data pattern >9669 failed, FIFO
		>0307	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0207	Data pattern >A55A failed, FIFO
		>0107	FIFO not empty failure, FIFO, FIFO control
		>0007	No failure in Test 7

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
8	>0800		Bidirectional Bus and Counters Test (Note that a cable or drive failure can cause this test to fail. Disconnect cable and repeat test for problem isolation.)
		>FF08	Core failure
		>1308	Drive deselect failure
		>1208	Selected or multiselect reset failed, bus receiver, TESTMODE, TESTCLK
		>1108	CONTROLSTB failed to set
		>1008	Bibus ADDR0 failed to set
		>0F08	Bibus ADDR1 failed to set
		>0E08	Bibus ADDR2 failed to set
		>0D08	Index flag set failure on index pulse, status bus receiver, CLRSECTINDX, deglitcher
		>0C08	Sector flag set failure on test index pulse, status bus receiver, deglitcher
		>0B08	Sector-index flag reset failure, CLRSECTINDX
		>0A08	Selected or multiselect set failed, set failed, status bus receiver, TESTCLK, TESTMODE
		>0908	Sector flag set failed, status bus receiver, TESTCLK, deglitcher
		>0808	Bibus pattern >199 failed, bibus latches and drivers
		>0708	Bibus pattern >296 failed, bibus latches and drivers
		>0608	Bibus pattern >155 failed, bibus latches and drivers
		>0508	Bibus pattern >2AA failed, BUSTODISK
		>0408	Bibus pattern >FFF failed, BUSTODISK
		>0308	Bibus direction failed to change to read
		>0208	Bibus tags or latches reset failed, CLRSTB, BUSTODISK
		>0108	Core Failure
		>0008	No failure in Test 8

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
9	>0900		CPE, P-Bus, FIFOS, and Interface Logic Test (Note that a cable or drive failure can cause this test to fail. Disconnect I/O cable and repeat test for problem isolation.)
		>FFFF	Core failure
		>FF09	Core failure
		>1109	Drive deselect failure, bibus, drive, I/O cable
		>1009	Sync mark fails, ECC failure, serial/parallel converter failure, TESTINDEX, XFERSTART, TESTMODE, sync detect failure, read/write drivers
		>0F09	FIFO not ready, CLRFIFO, FIFO, FIFO control
		>0E09	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0D09	FIFO pattern >0356 failed, FIFO, ECC
		>0C09	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0B09	FIFO pattern >ACEA failed, FIFO, ECC
		>0A09	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0909	FIFO pattern >C259 failed, FIFO, ECC
		>0809	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0709	FIFO pattern >1285 failed, FIFO, ECC, word counter failed
		>609	FIFO not ready, immediate field decode, FIFO, FIFO control
		>0509	FIFO pattern >8448 failed, FIFO, ECC, word counter failure
		>0409	Interface reset failure, interface control, word counter failure
		>0309	FIFO not empty failure, FIFO and control, word counter failure
		>0209	Bibus reset failure, bibus latch, interface control, bibus drivers
		>0109	Not used, test failure
		>0009	No failure in Test 9

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
A	>0A00		Rate Error Test (Note that a cable or drive failure can cause this test to fail. Disconnect I/O cable and repeat test for problem isolation.)
		>FFFF	Core failure
		>FF0A	Core failure
		>040A	Drive deselect failure, select, drive, I/O cable
		>030A	Forced read rate error failure, interrupts, FIFO clear, read/write drivers, serial/parallel converter, sync detect, ECC, TESTMODE, XFERSTART, TESTINDEX, DISKREAD
		>020A	Bibus reset failure (read rate error), FIFO control, latches, drivers
		>010A	Forced write rate error failure, interrupts, FIFO control, XFERSTART, interface bit
		>000A	No failure in Test A or execute all test
B	>0B00		I/F Cable Test (select unit in W6) (Note that a cable or drive failure can cause this test to fail)
		>0B0B	Terminator in status fails, drive power, terminator, cabling, status receiver
		>0A0B	Multiple units selected (MULTISEL), unit select, cable, drive I/O card, bibus
		>090B	Drive selected not received, drive offline or not ready, CSAFE reset, unit select, bibus tags
		>080B	Drive loopback failure (>2AA), bibus latches, drivers, tags, terminator, cable, drive
		>070B	Drive loopback failure (>155), bibus
		>060B	Drive loopback failure (>199), bibus
		>050B	Drive loopback failure (>296), bibus
		>040B	No index pulse flag, drivers, deglitcher, cable, drive
		>030B	Disk sector counter not equal to pulses received, sector flag, CLRSECTINDEX, drive
		>020B	Wrong number of sector pulses received
		>010B	Core failure
		>000B	No failure in Test B

Table A-1. Self-Test Descriptions (Continued)

Test	Word 3	Word 2	Description of Test
C	>0C00		Reserved
		>XX0C	Core failure
		>000C	No failure in Test C
D	>0DXY		Disk Drive Diagnostic Port Access (The procedure executed under Self-Test D reads or writes to diagnostic ports located in the disk drive. Refer to paragraph A.1.1 for information concerning the use of Self-Test D)
E			ECC Options
		>FFFF	Core failure
	>0E00	>000E	Enable ECC correction firmware (normal)
	>0E0F	>000E	Inhibit ECC correction firmware
F			Retry Options
		>FFFF	Core failure
	>0F00	>000F	Enable controller retries (normal)
	>0F0F	>000F	Inhibit controller retries

A.1.1 Self-Test D — Disk Drive Diagnostic Port Access

Self-Test D is used to read or write to diagnostic ports located in disk drives connected to the controller. The form of word 3 for this operation is >0DXY where X specifies the type of operation (read or write) and Y specifies the port location. A write operation is specified when X = 8 (>0D8Y). Port locations in the disk drive are specified as follows:

Word 3	BIBUS Address		
>0DX0	ADDR2 = 1	ADDR1 = 0	ADDR0 = 0
>0DX1	ADDR2 = 1	ADDR1 = 0	ADDR0 = 1
>0DX2	ADDR2 = 1	ADDR1 = 1	ADDR0 = 0
>0DX3	ADDR2 = 1	ADDR1 = 1	ADDR0 = 1
>0DX4	ADDR2 = 0	ADDR1 = 0	ADDR0 = 0
>0DX5	ADDR2 = 0	ADDR1 = 0	ADDR0 = 1
>0DX6	ADDR2 = 0	ADDR1 = 1	ADDR0 = 0
>0DX7	ADDR2 = 0	ADDR1 = 1	ADDR0 = 1

For example, if word 3 is loaded with >0D84, a write operation of port address four is specified. An automatic read is performed after the write, and information from the drive is returned to control and status word W4.

After each operation of Self-Test D, status word W5 contains the internal flag register. Bit values for this word are as follows:

Bit 0 = 1 Self-test mode (fixed value)
Bit 1 = 0 (Fixed value)
Bit 2 = X Retry inhibit
Bit 3 = X ECC inhibit
Bit 4 = 0 (Fixed value)
Bit 5 = 0 (Fixed value)
Bit 6 = 0 (Fixed value)
Bit 7 = 0 (Fixed value)
Bit 8 = 0 (Fixed value)
Bit 9 = X Overlapped seeks enable
Bit 10 = X Trident sector format
Bit 11 = X Preseek VID Flag (Implies that store register subtracts spare cylinder content)
Bit 12 = 0 (Fixed value)
Bit 13 = 0 (Fixed value)
Bit 14 = 0 (Fixed value)
Bit 15 = 0 (Fixed value)

X = 1 indicates active; X = 0 indicates inactive.

A.1.2 ECC and Retry Options

Tests B and C enhance controller diagnostics but are not called during Test 0 because they require special set-up conditions. Test B uses loopback tests to check signal drivers and receivers and requires the operating drive to be connected to the controller. Test C requires the disk drive to be powered up if it is connected to the controller but it does not require them to be connected.

During diagnostic operations, it may be helpful to inhibit ECC correction processes or controller retries. During normal operation, the controller reads a sector a certain number of times in order to recover marginal data or data that the ECC logic indicates is erroneous. The retry logic can be inhibited by issuing a self-test command of >0F0F to control and status word W3.

During normal operation the ECC logic also attempts to correct certain data error patterns if detected. The ECC logic can be inhibited by issuing a self-test command of >0E0F to control and status word W3. Although no error correction is attempted in this mode, the ECC character is still generated and the status of any detected error is reported in control and status word W7. Both the ECC and retry logics can be disabled by entering both self-test commands sequentially.

With both options inhibited, the controller checks the data in a given sector once but attempts no error correction. With only the retry logic disabled, the controller checks the data and, if necessary, attempts corrections. With only the ECC logic disabled, the controller performs multiple retries up to the maximum number and checks for data errors, but makes no corrections.

The retry logic can be enabled again by issuing the command >0E00 to control and status word W3 and by performing an I/O reset or recycling power to the controller. To enable the ECC logic, issue a self-test command of >0F00 to control and status word W3 and perform an I/O reset or recycle power to the controller.

NOTE

With both options enabled, status word W2 always returns >000E or >000F unless a catastrophic failure occurs.

Appendix B

Field-Replaceable Parts

B.1 Field-Replaceable Parts Descriptions

The disk controller, interconnecting cables, and terminator are field-replaceable assemblies. The disk drive is a field-repairable unit containing a significant number of field-replaceable components and subassemblies. Table B-1 contains a description of these components and subassemblies. Figure B-1 shows the location of the field-replaceable components and subassemblies within the disk drive.

Table B-1. Field-Replaceable Components and Assemblies

Replaceable Unit Name	TI Part Number (CDS Part Number)	Description
Absolute filter	943841-0041 (13367-001)	The absolute air filter removes contaminants from the air blown into the disk drive.
Ac input control assembly	943841-0231 (13372-001)	The ac input control assembly contains the ac power switch, the line filter, and ac fuses.
Air shroud lid gasket	943841-0186 (16712-001)	The air shroud lid gasket seals the air shroud from outside air contaminants.
Blower assembly, 220 Vac	943841-0162 (12450-001)	The blower assembly provides cooling air to the air shroud assembly and to the disk drive electronics.
Blower assembly, 115 Vac	943841-0193 (16224-001)	Same as 220 Vac blower assembly.
Card cage assembly	943841-0298 (24543-001)	Provides six slots for drive logic PWBs.
Control panel assembly	943841-0163 (13254-121)	The control panel contains all operator controls and indicators.
Data pack	2308475-0001	The data pack is a removable disk pack containing three recording and two protective disks that provide 80 megabytes of data capacity.
Data separator PWB	943841-0179 (17530-001)	The data separator PWB contains the phase synchronizer circuits, write encoder logic, and data separator circuit.

Table B-1. Field-Replaceable Components and Assemblies (Continued)

Replaceable Unit Name	TI Part Number (CDS Part Number)	Description
Grounding brush	943841-0168 (91535-001)	The grounding brush drains static charges off of the spindle.
Indicator lamps	943841-0158 (17374-001)	The indicator lamps illuminate operator controls and indicators.
Interface (I/O) PWB	943841-0296 (24530-001)	The interface PWB contains the bibus receiver/drivers and decoders, degate switch and logic, unit select switch and logic, and interface logic.
Lid closed microswitch	943841-0030 (14906-001)	The lid closed microswitch senses when the air shroud lid is closed.
Linear motor bobbin assembly	943841-0157 (12275-001)	The linear motor bobbin assembly is used in the linear motor assembly.
Linear motor assembly	943841-0159 (12274-001)	The linear motor assembly positions the carriage and way assembly, which locates the heads over the desired track.
Logic PWB	943841-0297 (24533-001)	The logic PWB contains the servocontrol, ready, read-only, error-detection, seek-incomplete, and end-of-cylinder logic
Logic III PWB	943841-0006 (12348-001)	The Logic III PWB contains the sequence oscillator and counter, pack-on and sequence logic, and speed detection circuits.
Matrix PWB	943841-0181 (17589-001)	The matrix PWB contains head selection logic and preamplifiers.
Motherboard assembly	943841-0298 (24543-001)	The motherboard is mounted in the logic card cage assembly and provides a backplane for the logic PWBs.
Motor pulley, 60 Hz	943841-0086 (19293-001)	The motor pulley provides the proper ratio reduction to turn the spindle at the proper speed.
Off-rack microswitch	943841-0134 (96997-002)	The off-rack microswitch senses when the carriage has extended the heads past their rest position.
Power-sequence relay, (K1)	943841-0026 (11102-003)	Power relay is used in the preceding sequence relay assembly.
Power supply, 115 Vac	943841-0147 (12449-002)	The power supply provides all dc voltages necessary to operate the disk drive.

Table B-1. Field-Replaceable Components and Assemblies (Continued)

Replaceable Unit Name	TI Part Number (CDS Part Number)	Description
Power supply, 220 Vac	943841-0148 (12449-001)	Same as 115 Vac power supply.
Read/write PWB	943841-0191 (17771-001)	The read/write PWB contains the read/write preamplifiers, amplifiers, and matrix.
Read/write head, (Numbers 01, 04)	943841-0062 (18507-003)	The read/write heads read and record data on the disk. There is one read/write head for each recording surface in the disk pack.
Read/write head, (Numbers 00, 03)	943841-0063 (18507-004)	Same as numbers 01, 04.
Read/write head, (Number 02)	943841-0064 (18508-006)	Same as numbers 01, 04.
Sequence-relay assembly, 220 Vac	943841-0172 (12452-001)	The sequence-relay activates when the disk drive has been selected by the controller to power-up.
Sequence-relay assembly, 115 Vac	943841-0184 (12452-002)	Same as 220 Vac sequence-relay assembly.
Servocontrol PWB	943841-0074 (18752-001)	The servocontrol PWB contains the servo head preamplifier, position logic, AGC, gapclock, and D/A converter and drivers.
Servo head	943841-0068 (13502-001)	The servo head reads positioning signals previously recorded on the servo surface of the disk pack. These signals allow the positioning circuits to position the heads over the center of a recording track.
Servo preamp PWB	943841-0002 (14912-001)	The servo preamp PWB contains the servo preamplifiers.
Solid-state relay, 115 Vac, K2 on −2 and −3 Relay Assy	943841-0082 (18867-001)	The solid-state relay controls ac power to the spindle drive motor.
Solid-state relay, 115 Vac, K3 on −2 and −3 Relay Assy	943841-0083 (18867-002)	Same as above.
Solid-state relay, 208/220 Vac, K3 on −1 Relay Assy	943841-0084 (18867-003)	Same as above.
Speed pickup transducer	943841-0161 (12539-001)	The speed pickup transducer provides spindle speed signals to the drive motor speed control circuit.

Table B-1. Field-Replaceable Components and Assemblies (Continued)

Replaceable Unit Name	TI Part Number (CDS Part Number)	Description
Spindle assembly	943841-0195 (12311-002)	The disk pack mounts on the spindle, which is rotated by the spindle drive motor.
Spindle drive belt	943841-0027 (95304-001)	The spindle drive belt transfers rotational motion from the spindle drive motor to the spindle.
Spindle lock assembly	943841-0219 (12360-001)	The spindle lock assembly stops spindle movement during pack loading.
Transformer assembly, 220 Vac	943841-0156 (13371-060)	The transformer steps down the high ac line voltage for input to the power supply.
Transformer assembly, 115 Vac	943841-0194 (18784-060)	Same as 220 Vac transformer assembly.
Velocity pickup transducer	943841-0095 (13263-001)	The velocity pickup transducer provides linear motor velocity signals to the positioning logic.
Velocity tach rod transducer	943841-0096 (13263-002)	

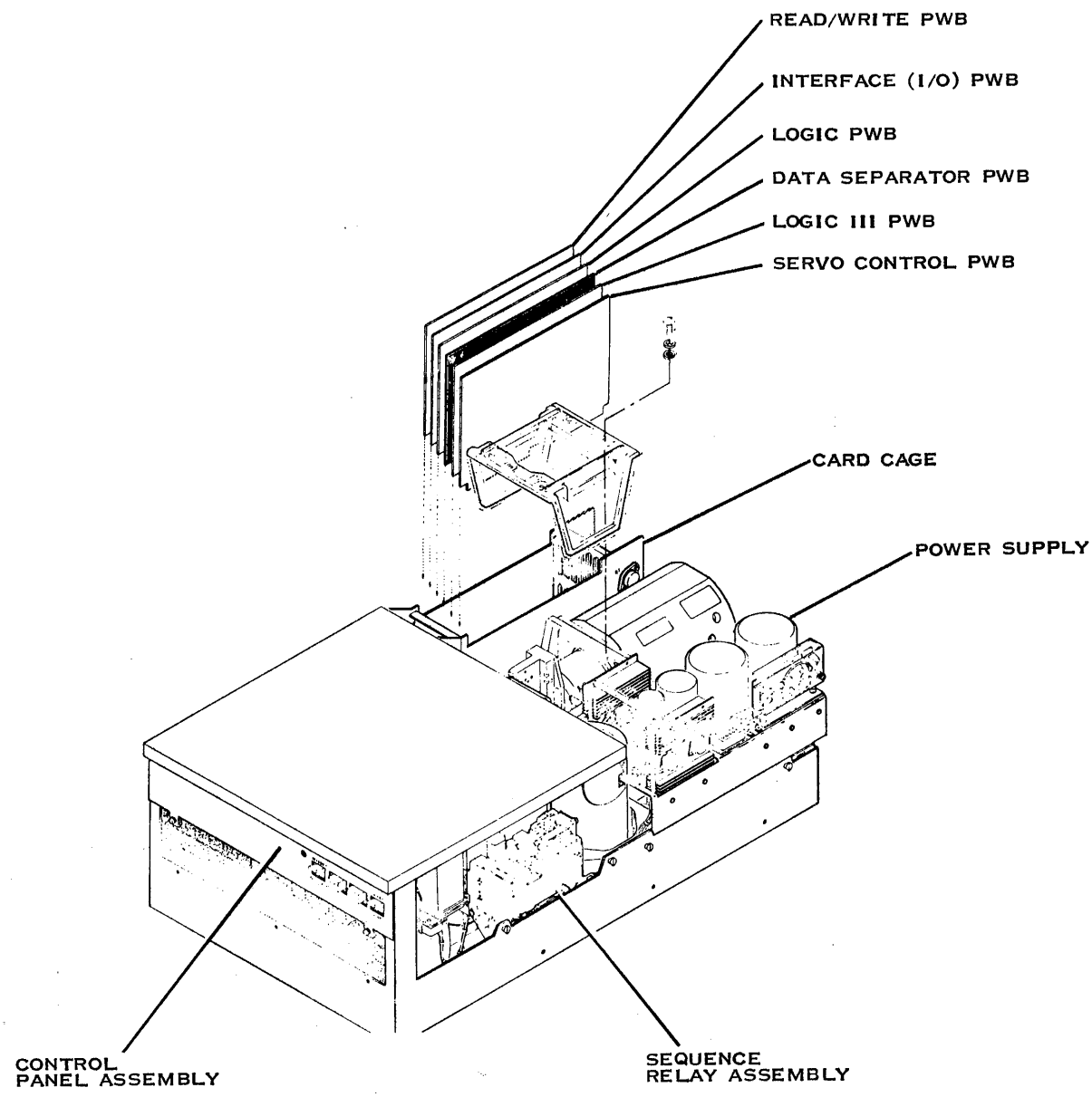

Figure B-1. Locations of Major Replaceable Units (Sheet 1 of 6)

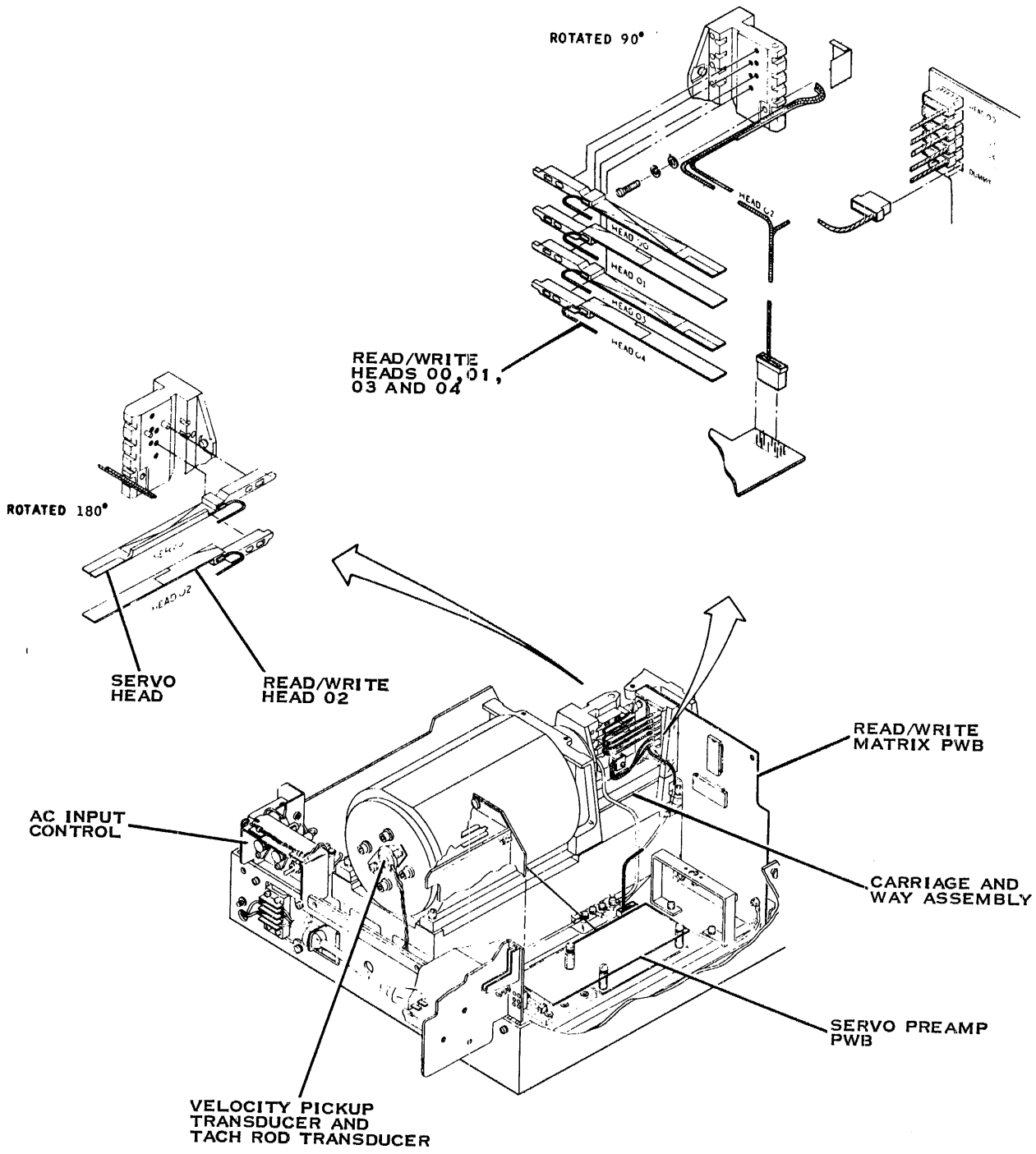

Figure B-1. Locations of Major Replaceable Units (Sheet 2 of 6)

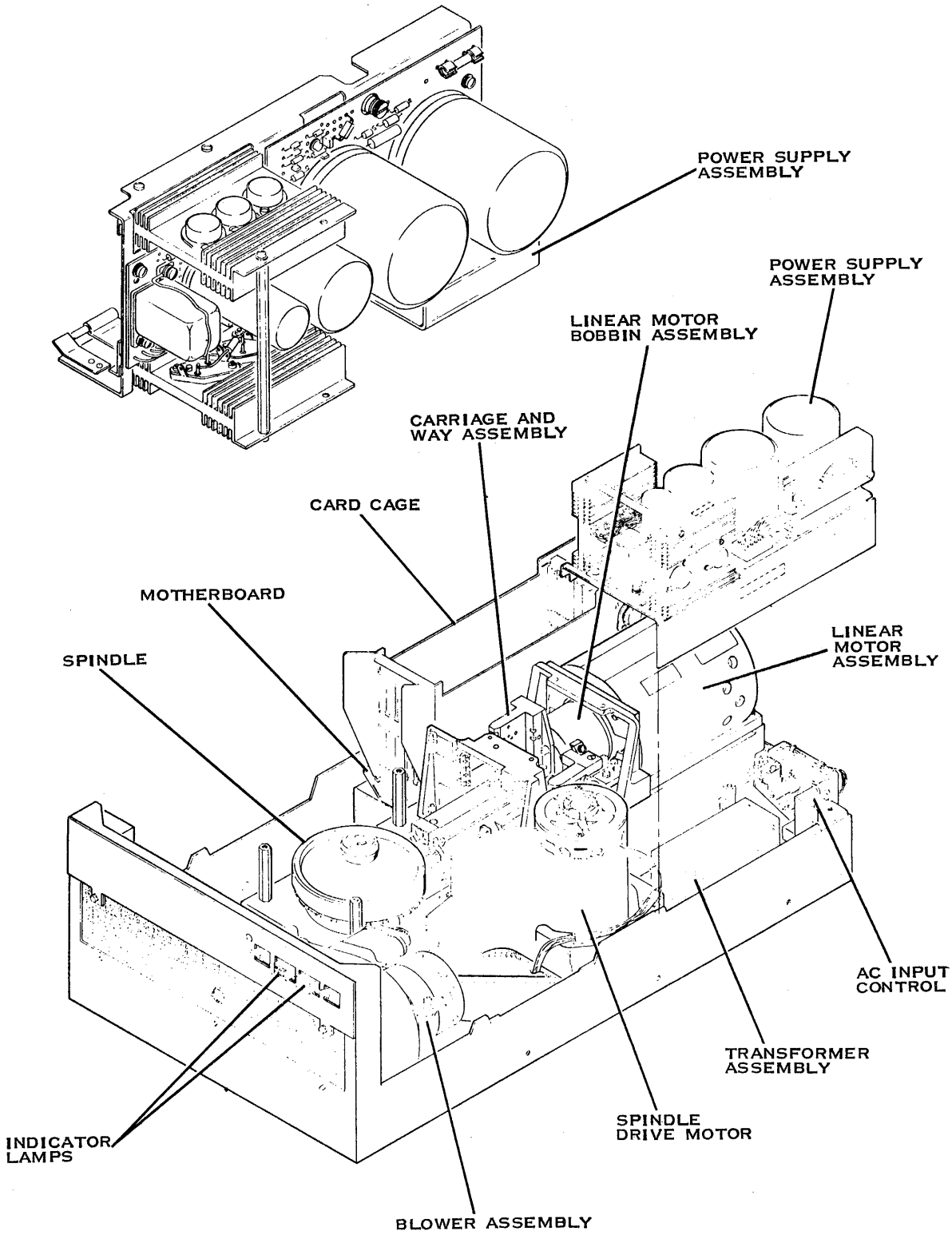

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Figure B-1. Locations of Major Replaceable Units (Sheet 3 of 6)

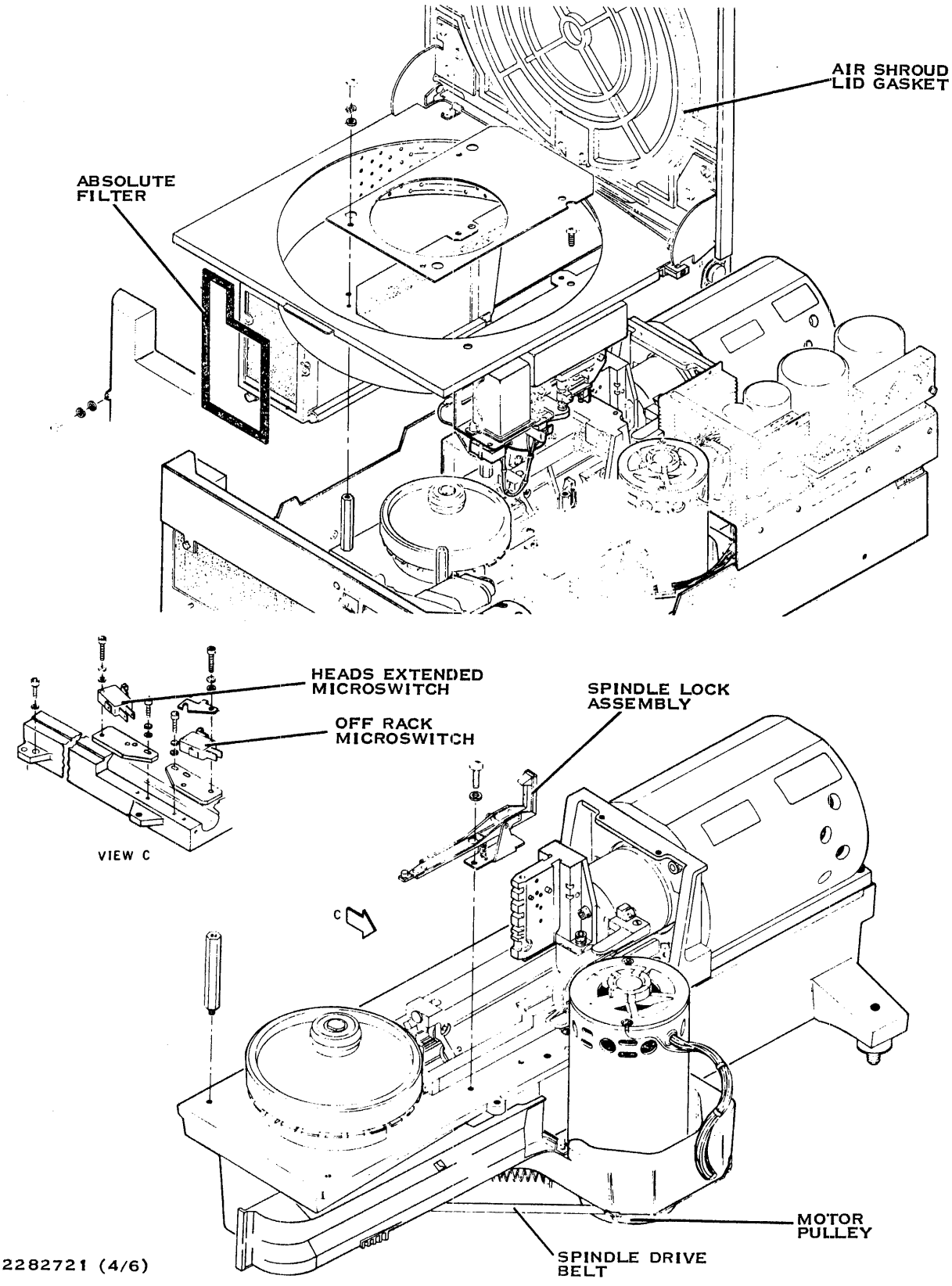

Figure B-1. Locations of Major Replaceable Units (Sheet 4 of 6)

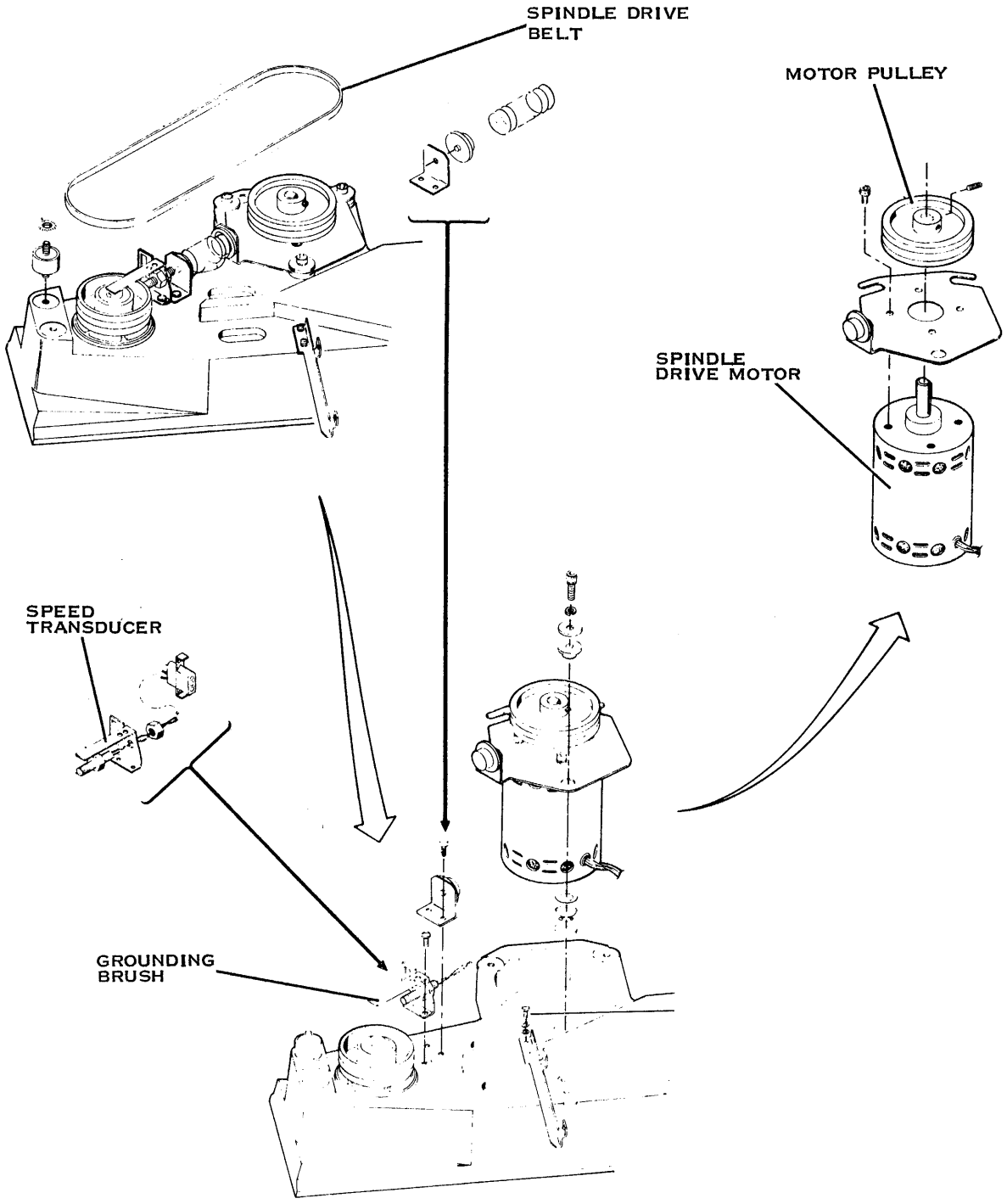

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Figure B-1. Locations of Major Replaceable Units (Sheet 5 of 6)

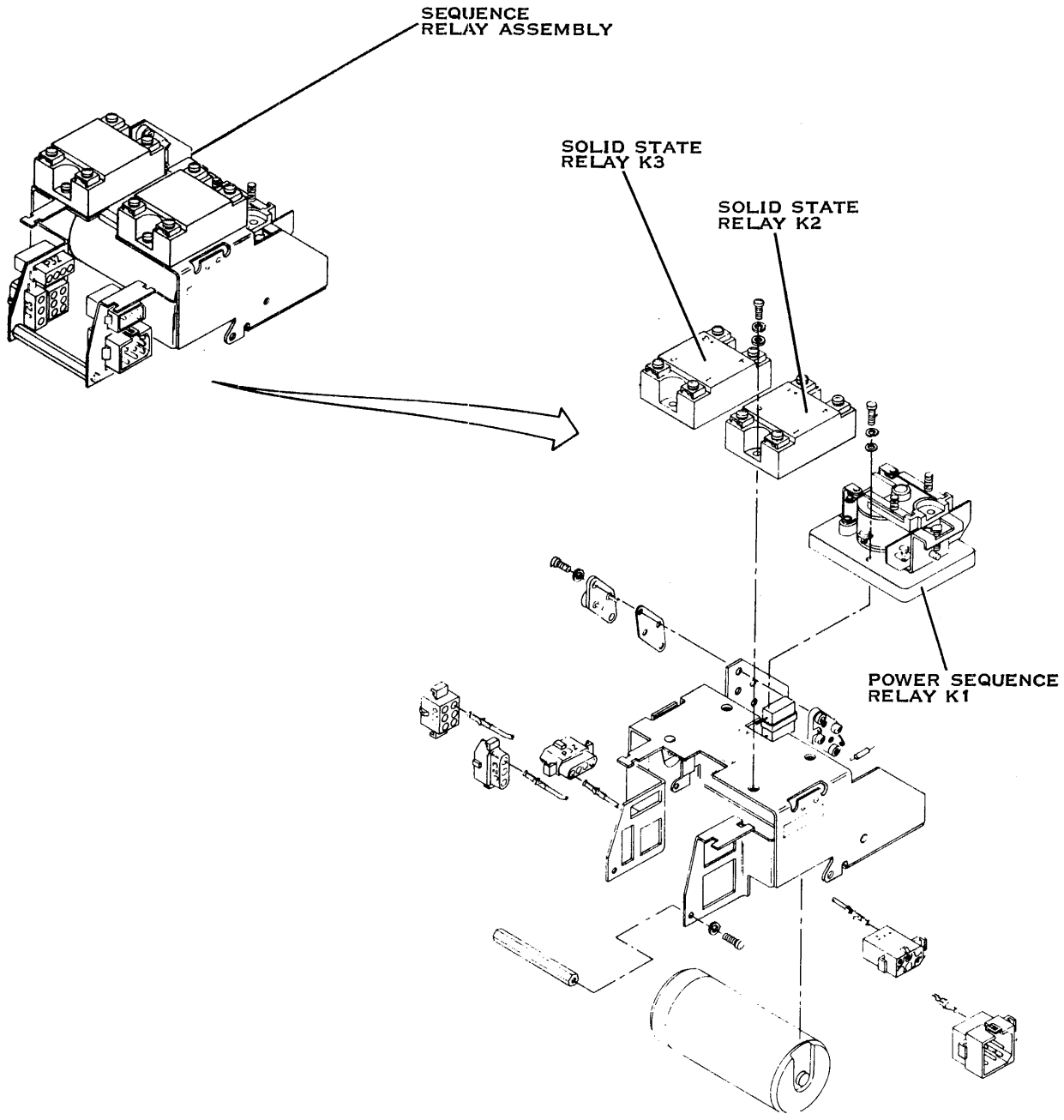

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Figure B-1. Locations of Major Replaceable Units (Sheet 6 of 6)

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections — Reference to Sections of the manual appear as "Sections x" with the symbol x representing any numeric quantity.
- Appendixes — Reference to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs — Reference to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph may be found.
- Tables — References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number.

  Tx-yy

- Figures — References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number.

  Fx-yy

- Other entries in the Index — References to other entries in the index preceded by the word "See" followed by the referenced entry.

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