Section 3

Programming

3.1 INTRODUCTION

This section contains information necessary for an assembly language programmer to write device service routines (DSRs) that communicate with the WD900 disk drive and the MT3200 tape unit. The programmer must be familiar with assembly language as described in the Model 990 TMS9900 Microprocessor Assembly Language Programmer's Guide or the Model 990/12 Computer Assembly Language Programmer's Guide.

Most users prefer the Texas Instruments standard operating system software that includes DSRs and features standardized file manipulation schemes that are essentially independent of I/O device type. These users should refer to the applicable operating system reference manual. Users who want to perform direct disk I/O operations without a standard operating system DSR can initiate disk commands and receive disk status as described in this section.

This section is organized as follows:

* Communication between the disk and the CPU using the TILINE
* Communication between the tape and the CPU using the TILINE
* Basic programming of the controller, including command descriptions, disk operation, tape operations, and command completion
* Control and status word formats and descriptions
* Detailed command descriptions with example command formats and status word formats

3.2 TILINE COMMUNICATION

The TILINE is an asynchronous 16-bit parallel data bus that transfers data between high-speed system elements such as the 990 main memory, 990 CPU, and the WD/MT controller. There are two classes of controllers that interface to the TILINE: the TILINE master controllers, which initiate data transfers, and TILINE slave controllers, which transmit or receive data in response to a master controller's request. A system with masters and slaves is configured so that only one master controller has control of the TILINE input/output (I/O) lines and only one slave controller recognizes a particular address. The WD/MT controller has both master and slave controllers. The controller is assigned two blocks (one for the disk and one for the tape) of four TILINE memory addresses, and these memory locations reside on the controller board. The 990 processor communicates with the controller by writing 16-bit command words into the eight disk or tape TILINE addresses. After a disk or tape operation is completed, the controller replaces the control words with status words, and the 990 processor can read the words in these same memory locations to determine disk or tape status. Controller operations are initiated when control words containing initialization parameters, operation parameters, and command codes are written into the memory locations assigned to the controller. After initialization, the controller acts independently of the 990 processor and transfers data between specified TILINE memory locations and the disk as required by the command. Any computer instruction that reads or modifies general memory can be used to communicate with the controller.

3.2.1 TILINE Addresses

Standard conventions built into the hardware and software of the Model 990 computer reserve CPU byte addresses >F800 to >FBFF for control and status communication with TILINE peripheral controllers, such as the WD/MT controller. This range is called the TILINE peripheral control space (TPCS). Addresses in this range can be mapped by the processor hardware to TILINE addresses in the range >FFC00 to >FFDFF. This mapping requires the 990 processor to operate either unmapped or in map file 0. The TPCS also can be addressed through alternate map files if the mapping bias value is chosen to yield the correct TILINE address. This programmable mapping feature is standard on some 990 CPUs and optional on others. This feature allows effective use of the entire TILINE address space rather than just the lower 32K words. Depending on the values in the map file registers, memory can be addressed anywhere in the TILINE address space (assuming a memory board exists at that address).

The physical TILINE bus includes 20 address lines; however, each CPU byte address consists of 16 bits. When a CPU byte address falls within the TPCS, all 1s are loaded automatically into the upper five bits of the TILINE address, and the least significant bit (LSB) is dropped. This LSB is a byte selector that is used only within the CPU. The remaining 15 bits form the lower 15 bits of the TILINE address. Figure 3-1 shows the conversion of a 16-bit CPU byte address to a 21-bit TILINE word address. One way to visualize this conversion is to think of a 21-bit TILINE byte address of >1FF800 that loses its LSB to become TILINE word address >FFC00. The 1F comes from the five 1s, and the >F800 comes from the original CPU byte address. The only part of this address accessible to the programmer is the CPU byte address, >F800.

The eight addresses of each controller interface are assigned to the controller from a base address to a base address plus 7 word address. The base address is dedicated to control and status word 0 (W0). Base address plus 1 is dedicated to word 1 (W1) continuing through base address plus 7, dedicated to word 7 (W7).

The base address for each interface is selected by one eight-section switch on the controller board (refer to Table 2-4), allowing multiple controllers in one system. Base address selection must be coordinated with the operating system software. Refer to Section 2 of this manual for instructions on setting the base address switches.

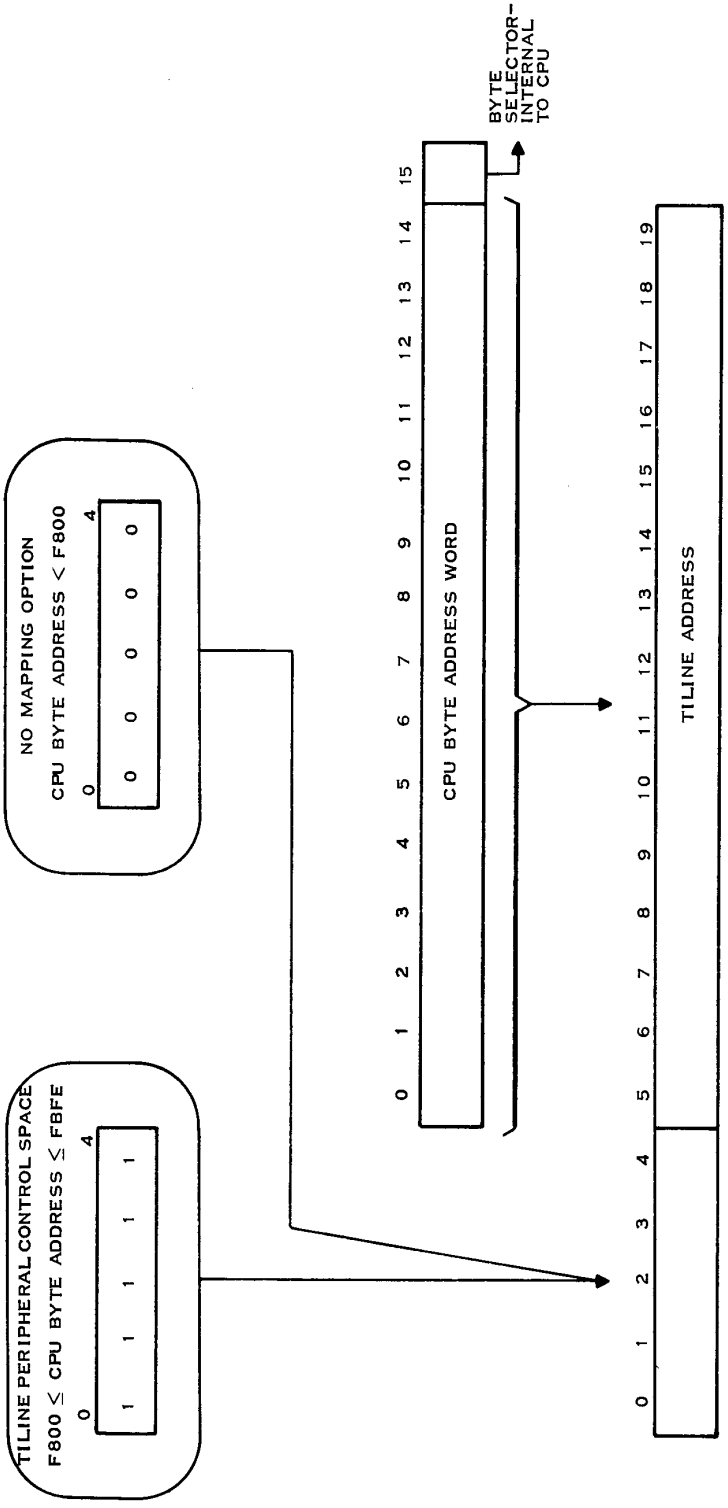

Figure 3-1 Relationship Between TILINE Address and CPU Byte Address

3.3 CONTROLLER COMMAND DESCRIPTIONS (DISK SECTION)

Commands sent to the WD/MT controller from the CPU cause the controller to perform any of the following nine basic disk system operations.

* Store Registers. A Store Registers command causes the controller to return certain critical drive parameters, such as words per track and cylinders available per drive unit, to the CPU.

* Write Format. The Write Format command formats a new disk (or reformats a disk previously in operation) with identification (ID) words (which make up the header), fixed data in the data field, an error-checking character (ECC), and the required gaps. The write format operation must be performed before using any unformatted disk media. One complete track is formatted per command.

* Read Data. The Read Data command transfers data from a specified disk location to a specified location in TILINE memory.

* Write Data. The Write Data command reads data at a specified TILINE memory location and records this data at a specified location on a previously formatted disk.

* Unformatted Read. There are two Unformatted Read command operations. The Unextended Unformatted Read command returns certain disk drive parameters to the software, which ensures compatibility with some existing operating systems that obtain these parameters by reading header information. The Extended Unformatted Read command, on the other hand, reads a specified number of words from the disk without regard to formatting, and is used primarily for diagnostic purposes.

* Unformatted Write. The Unformatted Write command writes data from TILINE memory onto the disk without regard for existing record boundaries and is used primarily for diagnostic purposes.

* Restore. The Restore command reinitializes the cylinder counter and repositions the heads of the selected drive over cylinder zero. This operation clears certain disk error conditions.

* Seek. A Seek command is used to position the read/write head over a track that is to be read or recorded. Since the seek operation is a relatively slow mechanical operation, the CPU can issue a Seek command to a particular drive to prepare it for a later data transfer without having to wait for the seek operation to complete. In addition, data transfers that use other drive units in a daisy chain can occur while this seek operation is executing. When the seek operation is completed, the controller can generate an interrupt to signal the CPU that a drive is ready for data transfer. However, since mapped drives contain two (or more) logical units that share a common read/write head, preseek operations are not supported. Overlapping seek operations can be used effectively on direct (unmapped) drives in the expanded emulation mode.

* Self-Test. The controller incorporates extensive self-test routines that can be used to locate many controller faults.

3.4 PROGRAMMING THE CONTROLLER (DISK SECTION)

The eight control and status words that the CPU uses to communicate with the controller contain the following information:

* Word 0 (W0), Disk Status -- Contains disk status codes for the selected drive, and attention bits and attention mask bits for generating interrupts

* Word 1 (W1), Command and Surface Address -- Contains command codes, head address, and several control bits used during certain data recovery operations

* Word 2 (W2), Record Format and Sector Address -- Determines the number of sectors per record and the address of each sector

* Word 3 (W3), Cylinder Address -- Contains the cylinder address

* Word 4 (W4), Byte Count -- Specifies the number of bytes to be transferred between the disk and CPU memory

* Word 5 (W5), LSB Memory Address -- Contains the 15 LSBs of the 20-bit TILINE memory address

* Word 6 (W6), Select and MSB Memory Address -- Contains drive select codes and the five MSBs of the twenty-bit TILINE memory address

* Word 7 (W7), Controller Status -- Contains controller status codes, the interrupt enable bit, and the idle/busy bit

To initiate a controller operation, the program loads the control words into the on-board memory addresses assigned to the controller. W7 must be the last control word; otherwise, the order in which the control words are transmitted is not important. This is because the controller immediately begins to perform the operation specified by the control words as soon as controller location W7 is loaded with a word that has bit 0 set to zero.

Transmitting a new set of control words to the controller destroys the status words from the previous operation, except for the disk status fields of W0. Word 0 disk status fields are set by the disk drive and cannot be modified by overwriting with a new control word. If overwriting is attempted, the controller ignores the bits placed in the W0 disk status fields.

If the CPU attempts to send a control word to the controller after an operation is initiated, the attempt is completed normally, but the controller ignores the control word.

Any status word read from a busy controller is a simulated W7 word in which bit 0 is a zero (busy) and bits 1 through 15 are meaningless. This word is returned regardless of the status word requested. This feature allows the controller to be polled for idle/busy status without interfering with any on-going controller operations.

Before writing a command to the controller registers, verify that W7, bit 0 of the controller (controller idle) is set. If W7, bit 0 is set, the command can write to the controller registers. Note that the controller is not busy until it receives a command.

3.4.1 Command Completion

An interrupt enable bit in W7 allows the programmer to specify if the controller will generate an interrupt to the CPU upon completion of an operation. The disk controller can be used with either an interrupt-driven or a polled DSR. The following paragraphs discuss these options.

3.4.1.1 Command Completion Without Interrupts. To check command completion or controller availability in a polled system, you must read status W7, bit 0 for an idle status. The controller is idle and available for commands if W7, bit 0 is equal to 1. In a normally completed operation, W7, bit 1 is set to 1. If an error occurs during operation, W7, bit 2 is set to 1. Read other status words to obtain more detailed status information.

Usually, the program initiates a timing loop when controller operation begins, and checks the idle bit at timer expiration. If the idle bit is still zero, the timer can be restarted and the sequence repeated a preselected number of times. This method requires more program overhead than the interrupt-driven approach.

If a Restore or Independent Seek command is initiated, the disk may not be ready after the controller reports a completion. To determine if the disk completed a Restore or Independent Seek command, the program checks the drive status bits of WO. If the disk drive completes its operation and the correct drive is selected, either the seek incomplete line is set, or the not ready bit is inactive. If the attention line of the selected drive is set, the drive has completed its operation.

3.4.1.2 Command Completion With Interrupts. The controller can issue two types of interrupts to the computer. One type of interrupt is issued when the controller completes a command, and the other type is issued when the disk drive completes a seek or restore operation.

3.4.2 Command Completion Interrupts

The interrupt enable bit (W7, bit 3) must be set when an operation is initiated. This bit is set in order to have the controller issue an interrupt to the 990 processor upon command completion. When the controller returns to idle, the interrupt is issued to the CPU. This interrupt is cleared by resetting the interrupt enable bit (W7, bit 3) or the appropriate completion bit (complete W7, bit 1, or error W7, bit 2).

3.4.2.1 Seek and Restore Complete Interrupts. Control word 0 contains four attention lines (one for each of the four disk drive unit addresses) and four attention mask lines. The attention line for each drive is set when the seek operation is complete for that drive. When the attention bit and mask bit for any drive are both set, the interrupt line to the computer is also set.

The programmer can set or reset the mask bits by using any of the computer memory instructions. However, the computer cannot set or reset the attention bits directly. The attention bits are set by the controller to indicate current disk status.

To use the seek and complete interrupts, first issue a Seek or Restore command to the controller. When the controller reports the command completion (by a controller idle or command completion interrupt), set the mask bit that corresponds to the desired drive. When the drive finishes the seek operation, an interrupt is issued to the CPU. This interrupt can be cleared by resetting the mask bit corresponding to the drive that requested the interrupt. All disk controller interrupts are reset when the controller switches from an idle to a busy condition.

3.5 WD900 CONTROL AND STATUS WORDS

The control and status words described in this section are used for both operating the controller and reporting disk system status. As described earlier, the CPU can write control words into device control registers (DCRs) to initiate operation, and can read status words in those registers to determine disk status after an operation has completed. Some bits in the registers are used only for disk operation control, some only for status reporting, and some for both control and status. Table 3-1 gives an overview of the TPCS registers and Table 3-2 through Table 3-9 describe each of these registers in more detail.

Table 3-1 WD900 TPCS Registers (Device Control Registers)

Bit:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
REG. 0	Off Line	Not Rdy	WRT PRT	UN-SAF	End Cyl	SK Inc	SP	PC	Attn Lines 0	1	2	3	Attn Mask 0	1	2	3
REG. 1	Ext A	Ext B	STB EAR	STB LAT	TIH	Command			OFF SET	OFS FWD	Head Address					
REG. 2	Sectors/Record								Starting Sector Address							
REG. 3	Cylinder Address															
	Self-Test/Extended Status Cmd.								Return Extended Status							
REG. 4	Transfer Byte Count															0
REG. 5	TILINE Address (LSB)															0
REG. 6	Spare 0	0	0	0	Drive Select 0	1	2	3	Spare 0	0	0	TILINE Address (MSB)				
REG. 7	IDLE	OP CMP	ERR	INT ENB	LOK OUT	RET	ECC	ABN CMP	MEM ERR	DAT ERR	TL TO	ID ERR	RT ERR	CMD TMR	SER ERR	UT ERR
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3.5.1 WO -- Disk Status

Control word WO is used to enable/inhibit the attention interrupts, to determine which drive initiated an attention interrupt, and to determine the status of the selected drive. Table 3-2 defines the bit assignments for WO on the WD900 drive. Bits 0 through 6 contain the individual status indicators for the selected drive.

Table 3-2 WO -- Disk Status

Bit	Description
0	Offline -- The selected drive is either not powered up or is not at the proper speed.
1	Not Ready -- The selected drive is either offline or performing a seek or restore operation.
2	Write Protect -- The selected drive is write-protected and no format information or data can be written on the disk.
3	Unsafe -- The selected drive is in an unsafe condition, indicating a fault that prevents normal disk operation. A Store and Restore command clears unsafe status if the unsafe condition no longer exists.
4	End of Cylinder -- This bit indicates that the head address exceeds the maximum allowable head number for the specific drive.
5	Seek Incomplete -- The head carriage failed to locate the specified cylinder. A restore operation and a retry is required to recover.
6	Not used -- This bit is not used and is set to 0.
7	An unsafe condition exists because of the following: * The drive lost power * The drive sequencing finished * The cable to the host CPU is disconnected This bit is reset by a Restore command.

Table 3-2 W0 -- Disk Status (Continued)

Bit	Description
8-11	Attention Lines (0-3) -- The attention line for a drive is set unless the drive is performing a seek or restore operation. The attention lines notify the 990 processor when seek and restore operations are complete.
12-15	Attention Interrupt Mask (0-3) -- An interrupt to the 990 is generated if the attention mask bit and its corresponding attention bit are both set and the controller is idle. Set the mask bits corresponding to the drive unit (after the command is issued and the controller is idle) to detect completion of a seek or restore operation.

3.5.2 W1 -- Format and Command

Control word W1 contains command codes, head addresses, and control bits that are used during certain data operations. Table 3-3 defines the bit assignments for W1 of the WD900 drive.

Table 3-3 W1 -- Command Code and Surface Address

Bit	Definition
0-1	Extended Commands A and B -- The three command code bits (5-7) allow up to eight unique commands. The extended mode bits (bits 0 and 1) are interpreted as additional command code bits.
2	Strobe Early -- Enables a strobe early condition.
3	Strobe Late -- Enables a strobe late condition.
4	Transfer Inhibit -- Inhibits transfer of data to the TILINE interface during read operations. This function allows a check on the integrity of a record without providing a memory buffer area to hold the data. When data is read by the controller, ECC verifies the data written to the disk.

Table 3-3 W1 -- Command Code and Surface Address (Continued)

Bit	Definition
5-7	Command -- The normal and extended command codes are:

Extended Mode Bits 0	1	Command Code Bits 5	6	7	Command
0	0	0	0	0	Store Registers
0	0	0	0	1	Write Format
0	0	0	1	0	Read Data
0	0	0	1	1	Write Data
0	0	1	0	0	Unformatted Read(1)
0	0	1	0	1	Unformatted Write
0	0	1	1	0	Seek(2)
0	0	1	1	1	Restore
1	0	0	0	0	Store Registers(3)
1	0	0	0	1	Write Format(3)
1	0	0	1	0	Read Data(3)
1	0	0	1	1	Write Data(3)
1	0	1	0	0	Unformatted Read
1	0	1	0	1	Unformatted Write(3)
1	0	1	1	0	Seek(2,3)
1	0	1	1	1	Self-Test(4)
1	1	0	0	1	Absolute Write
0	1	0	0	1	Relocate
0	1	1	0	0	Surface Analysis Assist

8	Head Offset -- This bit is set when data is read from the disk with the head offset (forward or reverse).

NOTES:

1. This command does not actually do an unformatted read. Refer to paragraph 3.6.1.5 for details.

2. Seek commands are ignored in some instances. Refer to paragraph 3.6.1.7.

3. For compatibility with other drives, do not use these particular extended commands. Use the normal commands that perform identical operations.

4. The controller contains self-test microdiagnostics. Refer to paragraph 3.6.2.2.

Table 3-3 W1 -- Command Code and Surface Address (Continued)

Bit	Definition
9	Head Offset Forward -- This bit is set if bit 8 is set and if data is read from the disk with the head offset forward. Bit 9 is not set if data is read with the head offset reverse.
10-15	Head Address -- This selects the read/write head and the associated cylinder surface. The head selection codes are as follows:

	Head Select Bits					
Head	10	11	12	13	14	15
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	0	0	1	0	0	1
10	0	0	1	0	1	0
11	0	0	1	0	1	1
12	0	0	1	1	0	0
13	0	0	1	1	0	1
14	0	0	1	1	1	0
15	0	0	1	1	1	1
16	0	1	0	0	0	0
17	0	1	0	0	0	1
18	0	1	0	0	1	0
19	0	1	0	0	1	1
20	0	1	0	1	0	0
21	0	1	0	1	0	1
22	0	1	0	1	1	0
23	0	1	0	1	1	1

3.5.3 W2 -- Record Format and Sector Address

Control word W2 determines the number of sectors per record and the address of each sector. Table 3-4 defines the bit functions of W2.

Table 3-4 W2 -- Record Format and Sector Address

Bit	Definition
0-7	Sectors per Record -- These bits are ignored by the controller since the recording format is always one sector per record.
8-15	Starting Sector Address -- These bits select the starting sector address for all reads and writes except for a write format. Write format does not require a starting sector address. A starting sector address larger than the maximum sector address causes a command time-out, because the controller cannot locate the address at which to start executing the operation.

3.5.4 W3

Control word 3 is used to specify maintenance commands and to select the cylinder address for read and write operations.

3.5.4.1 W3 -- Cylinder Address. W3 selects the cylinder address that the disk seeks for a read or write operation. The valid range of addresses is 0 through maximum number of cylinders less 1 in hexadecimal. The number of cylinders on a 425-megabyte drive is 693. The number of cylinders on a 138-megabyte drive is 805. An invalid cylinder address terminates the current operation, and the unit error (UE) controller status (control W7) is set. The disk status (control W0) indicates a seek incomplete (SI) status. This field is also used during self-test. The most significant byte specifies test numbers, and the least significant byte returns the current revision level of the ROMs used in the disk section of the controller.

The combination of the head address in W1, the sector address in W2, and the cylinder address in W3 forms a complete address that locates a record on the disk. Table 3-5 shows the bits of a cylinder address.

Table 3-5 W3 -- Cylinder Address

Bit	Definition
0-15	Cylinder Address -- Bit 15 is the least significant and bit 0 is the most significant.

3.5.4.2 W3 -- Maintenance Commands. When the extended mode bit 0 of W1 is set to one and the primary command field of W1 (bits 5-7) is set to FF hexadecimal, W3 bits 0 through 7 are a maintenance command field. In this mode the W3 bits are defined as follows:

Table 3-6 W3 -- Maintenance Commands

Bit	Definition
0	Loop bit -- When this bit is set to one, the specified self-test command is repeated until a reset is received. This function gives the system a scope loop capability.
1	Controller bit -- When this bit is set to one, the controller intercepts the command.
2-7	Maintenance command bits -- These bits specify the individual maintenance commands. Refer to the TILINE Peripheral Bus Interface Depot Maintenance Manual for a complete list and explanation of the maintenance commands and error codes.

3.5.5 W4 -- Transfer Byte Count

W4 sets the number of 8-bit data bytes to be transferred between the disk and the TILINE. The specified number of bytes for transfer must be even (bit 15 is always set to 0). The byte count range is limited by the available TILINE memory and the 64K byte maximum specified in the control word. An attempt to transfer to or from nonexistent TILINE memory results in a TILINE time-out (TT) controller status. Table 3-7 shows the bits of the transfer byte count.

Table 3-7 W4 -- Transfer Byte Count

Bit	Definition
0-15	Transfer Byte Count -- The byte count must be an even number (bit 15 set to 0). If a read with transfer inhibit is selected, the transfer byte count specifies the number of logically sequential bytes on the disk that must be checked.

3.5.6 W5 -- LSB Memory Address

The TILINE starting address is 20 bits in length. The 15 LSBs occupy bits 0 through 14 of control W5. The five MSBs are located in control W6. The 20 bit TILINE address specifies the start of the buffer address space. The controller accesses memory starting at the specified TILINE address and increments for the specified word count (byte count/2). For a read operation, the software must allocate a contiguous area in TILINE memory that is large enough to accept the data transfer without overwriting other regions of memory. The byte count and starting address must be specified in the control words. Table 3-8 shows the bits for W5.

Table 3-8 W5 -- LSBs Memory Address

Bit	Definition
0-15	Starting Memory Address, LSBs -- The TILINE starting memory address is 20 bits in length with the 15 LSBs contained in bits 0-14 of W5. Bit 15 is always held at 0. The 5 MSBs are in W6.

3.5.7 W6 -- Unit Select and MSB Memory Address

W6 contains the unit select bits and the MSBs of the TILINE buffer memory. Bits 0 through 3 and 8 through 10 are reserved and should be set to 0. Table 3-9 defines the bits of W6.

Table 3-9 W6 -- Unit Select and MSB Memory Address

Bit	Definition
0-3	Not used.
4-7	Position-coded unit select field. Only one bit position in this field can be set to 1. Any code with two or more positions set to 1 causes an offline status to be reported and no drive operations are performed. A 100 microsecond time delay is required after the unit select field is changed before the status information in W0 in updated for the newly selected unit. The valid unit select codes are listed below.

W6 Bits 4	5	6	7	Unit Selected
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3

8-10	Not used.
11-15	Starting TILINE memory address MSB. These are the five MSBs of the 20-bit TILINE starting memory address. Refer to the W5 description for more information.

The controller supports up to two physical drives. Each drive can be divided into two logical units, making it possible to have a maximum of four addressable units. Units are numbered consecutively with no holes in the numbering scheme. For example, if three units are supported, the units are numbered unit 0, unit 1, and unit 2. A unit would not be numbered unit 3 because one of the lower numbers would be skipped.

3.5.8 W7 -- Controller Status

W7 contains control bits from the 990 processor at the beginning of an operation and contains controller status data at the completion of an operation.

NOTE

W7 is the last word loaded during operation setup. This is because the idle/busy bit (W7, bit 0) initiates controller operation when forced low by the processor. W7 must be the first status word checked after an operation.

Table 3-10 defines the functions of the W7 bits.

Table 3-10 W7 -- Controller Status

Bit	Definition
0	Idle -- The controller is idle when this bit is 1. The host can read and write into the registers only when bit 0 is set to 1. The host sets this bit to zero to activate any command. The command activated is contained in W1, bits 5 through 7. The TPBI sets this bit to 1 when command execution is complete, either normally or as a result of an error condition. The TILINE interrupt for each slave set is active only when bit 0 is set to 1.
1	Complete -- This bit is set when the controller completes a command without error. Setting this bit to zero clears the command complete interrupt, if enabled by bit 3.
2	Error -- This bit is set if an error is detected. W7 bits 7-15 and W0 bits 0-7 provide more detailed error information.

Table 3-10 W7 -- Controller Status (Continued)

Bit	Definition
3	Interrupt Enable -- This bit must be set to enable the controller to generate an interrupt when a command completes either idle and complete or error. Note that if the interrupt enable bit is set while the controller is idle and the complete or error bit is set, an interrupt is generated immediately. Attention interrupts in WO are independent of this interrupt enable bit.
4	Always 0.
5	Retry -- This bit is set when the controller performs a re-read operation because of a data error.
6	ECC Corrected -- This bit is set when the controller corrects data within its buffer during a read operation.
7	Abnormal Completion -- This bit is set if a disk operation is terminated due to either an I/O reset, a TILINE power-failure warning, a TILINE power reset, or a Write Format or an Unformatted Write command that is issued with the format enable switch set to disable.
8	Memory Error -- This bit is set if a TILINE memory error is detected during a disk write. Data transfer is terminated when a memory error is detected.
9	Data Error -- This bit is set if an uncorrectable ECC error is detected during a read operation.

Table 3-10 W7 -- Controller Status (Continued)

Bit	Definition
10	TILINE Time-Out -- This bit is set if the 50-microsecond timer on the controller expires before the completion of any TILINE cycle. A common cause of time-out is an attempt to read or write to a nonexistent memory.
11	Header Error -- This bit is set if an ID word comparison error occurs during an ID verification of ID words 1, 2, 3, and ECC checking. If bit 9 is also set, it indicates an ECC data error in the sector read. This error causes command termination.
12	Rate Error -- This bit is set if the TILINE is not able to keep up with the disk. The data buffer prevents this error from occurring.
13	Command Time-Out -- This bit is set if the controller fails to complete an operation before the command timer expires. The timer is started at the following times: when a seek operation is performed, when a head address is set or incremented, when the controller is at the beginning of the idle routine, after each successful sector read or write, and during execution of the disk drive power-up sequence.
14	Search Error -- This bit is set if the controller does not detect a synchronization character within one physical sector during a read operation. If either the internal or external ECC inhibit flag is set, a search error status is reported and the command is aborted.

Table 3-10 W7 -- Controller Status (Continued)

Bit	Definition
15	Unit Error -- This bit is set if an operation is terminated due to a disk drive error. The causes of a unit error depend on the command being performed when the error occurs. Listed below are the commands and the causes of the command termination.

Terminated Command	Possible Causes
Restore	Unit offline
Unextended Unformatted Read	Unit offline, not ready, unsafe, seek incomplete, or offset active
Write Data, Write Formatted, Unformatted Write, Absolute Write Format, Relocate	Unit offline, not ready, unsafe, seek incomplete, offset active, or write protected
Read Data, Extended Read Unformatted	Unit offline, unsafe, seek incomplete, offset active, or not ready
Seek (performed by the selected drive), as well as operations performed as part of other read or write commands	Unit offline, unsafe, seek incomplete, or offset active

3.6 DETAILED WD900 CONTROLLER COMMAND DESCRIPTIONS

The following are the normal and extended disk controller command descriptions.

3.6.1 Normal Commands

Store Registers, Write Format, Read Data, Write Data, Unformatted Read, Unformatted Write, Seek, and Restore are the normal commands of the controller.

3.6.1.1 Store Registers Command. The Store Registers command allows the operating system software to determine critical disk parameters such as words per track and cylinders available per drive unit. This command causes the controller to send one, two, or three words to the 990 memory from the disk system. The Store Registers command starts at the memory address specified in W5 and W6, and is specified by the word count in W4. The three words contain the following information:

* W1 -- W1 contains the total number of unformatted words that can be recorded on a disk track.

* W2 -- Bits 0 through 7 of W2 specify the number of sectors per track, and bits 8 through 15 specify the number of bytes of overhead per sector.

* W3 -- Bits 0 through 4 of W3 specify the number of tracks per cylinder, and bits 5 through 15 specify the number of cylinders per drive.

3.6.1.2 Write Format Command. The Write Format command formats a new disk or reformats existing media. One complete track is formatted per command. After receiving all command words, the controller verifies correct disk status (offline, not ready, unsafe, write protect, offset active, or seek incomplete), seeks the specified cylinder, and sets the specified head address. A verify ID and an ECC are performed after the seek. Relocation from a bad track to a spare track is allowed when the spare track is formatted. The track is formatted if the verify ID fails due to a data error or search error. The verify ID error or search error is retried up to three times before formatting. The Write Format command returns an ID error status if the ID is incorrect and an ECC error does not exist. Any retries are returned if either a data error or search error is encountered during the verify ID. The controller assembles the ID words from its internal registers and counters, and records the word(s) on the specified disk track address. The controller then records the entire data field following the ID words with the data word in the specified TILINE address. This is repeated for all data word positions and the ECC. The controller formats each sector on the

track with ID words, data, ECC, and the required gaps. All sectors contain ID words and the ECC field.

3.6.1.3 Read Data Command. The Read Data command identifies a record location, specifies the number of bytes to be transferred from this record, and gives the starting address to the TILINE memory address buffer area that receives data from the disk. After firmware initialization, the controller performs the following operations:

1. Checks for unit errors by examining the disk status bits (offline, offset active, not ready, unsafe, and seek incomplete).

2. Seeks the specified cylinder.

3. Sets the specified head address.

4. Searches for the right ID as the data passes under the head. If the ID is not found before the next index mark, sector pulses are counted from the index mark to locate the correct sector to be transferred.

5. Performs the read after the correct sector is located.

6. Terminates the read operation with an ID status error (W7, bit 11), if the sector count fails to find the correct ID.

Normal controller operation for the WD/MT controller allows a maximum number of six retries to find two consecutive reads to yield the same error syndrome. If two consecutive syndromes are found to be equal, error correction is attempted, otherwise data error status is set. If the error is not correctable, data error status is set. Note that when retries are attempted, the retry status is set; and when ECC correction takes place, the ECC corrected status is set.

3.6.1.4 Write Data Command. The Write Data command causes the controller to record data on a previously formatted track or to write over a previously recorded sector. After firmware initialization, the disk controller performs the following operations:

1. Checks for unit errors by examining disk status (offline, not ready, unsafe, write protect, offset active, or seek incomplete).

2. Seeks the specified cylinder.

3. Selects the specified head address.

4. Locates the desired starting sector by reading the ID words of each sector and comparing its contents to the desired sector address. If the words contain the defective track bit and no ECC error exists, a re-seek is issued to the head and the cylinder address specified in the data field, and the operation continues on this alternate track. When the controller detects the sector immediately before the desired sector, it arms the interface so that the write operation is started when the next sector mark occurs.

5. Waits for the correct sector and performs the write.

If the ID words in step 4 do not compare, the write operation is terminated with an ID status error.

Unless a terminate condition is encountered, data is written on the disk, sector by sector, until the specified number of words have been transferred. When the transfer word count is less that the sector word count, the controller fills the remainder of the sector with zeros until the sector word count has been decremented to zero. When the number of words is greater than the words per sector, the controller continues to the next sequential sector.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 in the preceding list.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder, selects head address 0 for the new cylinder, and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 in the preceding list.

3.6.1.5 Unformatted Read Command. To ensure compatibility with the DSRs, the Unformatted Read command (nonextended) does not actually read any data from the disk. Instead, three words are returned to the TILINE memory after this command is performed. W1 contains the head and cylinder addresses. The second word contains the sectors-per-record number (>01) and the sector address. The third word contains the record word count (>80).

If a genuine unformatted read operation is desired, the Extended Unformatted Read command words can be used.

3.6.1.6 Unformatted Write Command. An Unformatted Write command transfers up to 510 bytes of data from a specified TILINE address to a specified disk address. The controller seeks the specified cylinder (after the firmware is initialized), sets the head

address, detects the beginning of the sector, generates the correct lead gap, writes a synchronization character, and writes data on the disk. All data is written consecutively regardless of sector boundaries until a termination condition is encountered. The controller adds an ECC character and a trailing gap at the end of the data.

3.6.1.7 Seek Command. If a physical drive is configured as two logical drives, independent seek operations can cause head thrashing. Head thrashing is when the head assembly moves all the heads from one read/write location to the next specified read/write location, only to return to finish the first operation on the original track. Head thrashing is eliminated by ignoring any pre-seek command from the software to the drives that are logically divided. This command is performed on drives that are not divided logically. The Seek command causes the drive to orient the heads to the cylinder specified in the command words. An interrupt can be generated via the attention bits in W0 to alert the CPU that this operation has completed.

3.6.1.8 Restore Command. The Restore command reinitializes the cylinder counter and repositions the heads of the selected drive over cylinder zero. The Restore command also issues a Fault Clear command to the drive. The Restore command is used to clear an unsafe condition or seek error at the drive. This command is required if a seek incomplete or unsafe status is detected. Before initiating the restore operation, the controller determines if a unit error exists by examining the offline bit. If the controller finds a disk status error before it initiates the Restore command, it sets the unit error bit in W7.

Completion of the restore operation can be determined by enabling a disk drive completion interrupt (attention bit interrupt, W0) or by monitoring the attention bit for the selected drive unit.

3.6.2 Extended Mode Commands

The extended mode commands set the extended mode bits (W1, bits 0 and 1). The extended mode bits allow the command code field (W1, bits 5 through 7) to select from an additional set of commands. These commands are less commonly used during the course of data storage and retrieval operations.

Except for the extended Read Unformatted, Write Format Flagged, and extended Self-Test commands, extended mode commands perform functions identical to the unextended mode commands.

3.6.2.1 Read Unformatted (100 -- Extended). The extended Unformatted Read command allows the programmer to read a sector and to examine a specified number of words starting immediately after the synchronization (sync) character without regard to ECC errors or standard sector formatting. This is primarily a diagnostic feature.

The programmer specifies a sector of the selected track to start the read process. When the sector is located, the controller transfers the specified number of words to TILINE memory, starting with the first word after the sync character.

The ID words, data fields, ECC words, and trailing gap are read and transferred to memory as data words. There are normally glitches in the trailing gap due to write-head turn-on and turn-off transients and differing write-clock phases that are recorded during formatting and write operations. These glitches can cause shifting of word boundaries. This shifting occurs when the word count is large enough to require data to be written beyond the normal position of the ECC characters.

An ECC check is performed at the end of the operation, and data error status is reported if the ECC check shows an error. However, no ECC correction is attempted. A data error occurs unless the byte count is the correct value to allow comparing the calculated ECC checkbits against the read checkbits.

The word transfer count is limited to 510 bytes. Command time-out occurs if too many bytes are requested. The extended Read Unformatted command can also be used to read the information.

3.6.2.2 Self-Test Commands (111 -- Extended). The WD/MT controller automatically performs a sequence of self-tests on power-up. Self-tests can also be initiated by self-test commands (see Table 3-11). In either case, self-test failures cause all 1s (>FF) to be reported to the controller in the right byte of W7. Two 16-bit failure codes, one in W2 and the other in W4, are also reported.

You can access the extended command field for the controller self-test by entering >8700 in slave W1 and >0000 in slave W3. W3, bit 0 is a loop bit for self-test. To loop on all self-tests, enter >8000 in W3. An IORESET is the only method to exit the looping self-test. Note that the Execute Self-Tests command (W3, >0000) is the same one used for power-up conditions. Self-test results for both the Execute Self-Test command and the power-up self-test are returned to register 2 and register 4 (refer to paragraph 1.3.10) but the self-test LED only lights during the power-up self-test. The FAULT LED cannot be reset unless the self-test passes. W2 and W4 contain error status information.

The disk controller ROM revision level is available through the extended self-test mode. You can obtain this information by setting the most significant byte of W3 to 7C hexadecimal. The revision level of the ROMs used in the disk section of the WD/MT controller is reported in the least significant byte of W3.

Table 3-11 Extended Commands

Command	Device Register 3 Bits 0	1	2	3	4	5	6	7
Controller:								
Report ROM Revision Level	0	1	1	1	1	1	0	0
Execute Self-Test	0	0	0	0	0	0	0	0
Loop on Self-Test	1	0	0	0	0	0	0	0

3.6.2.3 Absolute Write Format Command. This is a nonrelocatable Write Format command. The controller performs the following functions:

1. Checks for unit errors by examining disk status (off-line, not ready, unsafe, write protect, offset active, or seek incomplete)
2. Seeks the specified cylinder
3. Sets the specified head address
4. Waits for the correct starting sector
5. Formats the track with the fill word specified by the TILINE address

The format of this command is:

W0: 0
W1: MSB = #C1, LSB = Head Address of Track
W2: 0100
W3: Cylinder Address of Track
W4: TILINE Byte Count=0002
W5: TILINE Address
W6: Unit Address and TILINE Address
W7: 0

The TILINE address contains the fill word to format the track.

3.6.2.4 Relocate Command. This command relocates a bad track to a spare track. The format of the command is as follows:

W0: 0
W1: MSB = #41 LSB = Head Address of Bad Track
W2: 0
W3: Cylinder Address of Bad Track
W4: TILINE Byte Count = 0004
W5: TILINE Address
W6: Unit Address and TILINE Address
W7: 0

The spare track address and format word should be on the following TILINE address:

TILINE ADR=SPARE TRK ADR; HDADR=BITS 0-4, CYLADR=BIT 5-15.

TILINE ADR+2=WORD TO FORMAT SPARE TRACK WITH.

The disk controller performs the following operations:

1. Verifies the ID of the bad track.

2. Formats the bad track so that header words 1 and 2 contain the cylinder, head, and sector addresses of the bad track. W3 contains the bad track flag (>8000). The data field contains the spare track address where SPARE TRACK ADR: HD ADR=BITS 0-4, CYL ADR=BITS 5-15.

3. Seeks the spare track address.

4. Verifies the spare track ID.

5. Formats the spare track address with the header of the bad track, and fills the word specified by the Relocate command at TILINE ADR and TILINE ADR+2. Command statuses that apply to this command are UE, SE, CT, RE, ID (the track may already be relocated), TT, DF, ME, AC, and RETRY.

3.7 CONTROLLER COMMAND DESCRIPTIONS (TAPE SECTION)

Tape commands sent to the WD/MT controller from the CPU cause the controller to perform any of eleven basic tape operations. The command code that selects the operation to be performed by the controller is formed by bits 4 through 7 of word 6 (W6). The command code assignments are shown in the description of W6, and the tape commands are described in the following:

* No-Operation (NOP) Command -- Any NOP command results in an idle and complete status. The controller recognizes all NOP commands and returns the system to idle after setting the idle and complete bits.

* Buffer Sync (Write Sync) -- Use this command to ensure that all pending writes complete. The controller remains busy until the entire contents of the controller and transport buffers are written on tape.

* Write End Of File (EOF) -- This command causes the file mark record to be written on tape preceded by a 101.6-millimeter (4-inch) gap. For a phase encoded (PE) tape transport, the controller verifies that the file mark was properly written on the tape. A PE hard error status is reported if the file mark was not properly written on the tape.

The end of tape (EOT) and offline status are reported in the same manner as the write binary operation.

When EOF completes, either operation complete or error status is reported and an interrupt is issued if the interrupt enable bit (W7, bit 3) is set.

* Record Skip Reverse -- This command is performed after the skip forward operation except in the following instances:

  - The tape is moving in the reverse direction.

  - The operation terminates when beginning of tape (BOT) (instead of EOT) is detected. In this case, the BOT status is reported and the tape is positioned in the same place as during a rewind command.

* Read Binary Forward -- Data from the tape is transferred to the main memory via the TILINE in a read binary operation. The controller accesses the TILINE as needed and transfers the tape characters, assembled in 16-bit words, and transmits the words into successive memory locations.

* Record Skip Forward -- In the skip forward operation, the read head passes over the records in a forward direction with no transfer of data to TILINE memory. The number of records to skip is indicated in W4, which is decremented each time a record is skipped. If the initial record number is zero, the controller attempts to skip 65 536 records and stops on EOT or EOF.

* Write Binary Forward -- The controller fetches data from main memory via TILINE and records it on the tape in a write binary operation. The 20-bit starting address of the memory buffer is specified in W6 (bits 11 through 15) and W5 (bits 0 through 14). The number of 8-bit characters to be recorded is specified in W4.

* Erase -- A portion of tape is deleted when this command is performed. The maximum length of tape that can be erased with one command is 1082.0 millimeters (42.6 inches). During an erase operation, an EOT or offline error can occur.

* Read Transport Status -- The Read Status command selects a transport and returns transport status information without performing any transport functions. The controller responds to the command by returning a transport status word (W0) and a controller status word (W7).

* Rewind -- The controller tests the unit to determine if it is already rewinding. If the unit is not rewinding, the controller issues the Rewind command and reports an idle and operation complete status in W7. If the unit is rewinding, the controller reports tape rewind status in W0, and idle, error, and tape status in W7.

* Rewind and Offline -- The Rewind and Offline command causes the tape to rewind and unload from the transport and also causes the offline bit to be set.

3.8 MT3200 CONTROL AND STATUS WORDS

The control and status words described in this section are used to operate the tape and report tape status. Table 3-12 gives an overview of the MT3200 TPCS registers. A more detailed explanation of the bits follows in Table 3-13 through Table 3-19.

Table 3-12 MT3200 TPCS Registers (Device Control Registers)

Bit:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
REG. 0	Off Line	BOT	EOR	EOF	EOT	WR RNG	RW	CMD TO	Rewind Bits 0	1	2	3	Rewind Mask 0	1	2	3
REG. 1	Read Overflow Status Count (16 LSBs)															
REG. 2	Read Overflow Status (8 MSBs)								Error Classification							
REG. 3	Read Offset															
	Extended Command															
	Track in Error								Retry Count							
REG. 4	R/W Character Count, Skip Record Count, or Erase Length															
REG. 5	TILINE Memory Buffer Starting Address (15 LSBs)															0
REG. 6	Unit Select 0 1				Command				WR DIAG		TILINE Address (5 MSBs)					
REG. 7	IDLE	OP CMP	ERR	INT ENB	1	0	PE FMT	ABN CMP	IP ERR	COR ERR	HRD ERR	MEM ERR	TIM ERR	TL TO	FMT ERR	TAP ERR
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3.8.1 WO -- Tape Transport Status

Word 0 (WO), bits 0 through 7 contain individual status indicators for the tape drive. Bits 8 through 11 contain the rewind status for the tape unit. The rewind status bits generate interrupts when enabled by the corresponding rewind mask bits located in bits 12 through 15. Table 3-13 shows the tape transport status for WO.

Table 3-13 WO -- Tape Transport Status

Bit	Definition
0	Offline -- This bit indicates that the transport is not ready and is not rewinding. The error and tape error bits are also set when this bit is set.
1	Beginning of Tape (BOT) -- This bit is set when the BOT marker is detected while performing a Skip Reverse command. The error and tape error status bits are set when this bit is set. It is not considered an error when a Read Transport Status command is performed.
2	End of Record (EOR) -- The EOR status bit is set when a Read Binary Forward command specifies more characters to be read than actually exist in the tape record. The error and tape error status bits are also set when this bit is set.
3	End of File (EOF) -- This is set when an EOF mark is encountered during a Read Binary Forward, Record Skip Forward, or Skip Reverse command. The tape error and error bits are also set when this bit is set.
4	End of Tape (EOT) -- This bit is set when the EOT marker is detected during a forward tape movement. The EOT does not abort a write operation but reports when an ongoing operation completes. It is not considered an error condition when a Read Tape Status command is performed.
5	Write Ring -- This is set if a Write Binary, Write EOF, or Erase command is specified when the tape does not have a write ring inserted in the tape file reel. Setting this bit causes the operation to abort. The error and tape error status bits set when this bit is set. It is not considered an error when a Read Tape command is performed.
6	Tape Rewinding -- This bit is set whenever a command is performed and the drive is in the rewind mode. The error and tape error status bits are set when this condition exists.

Table 3-13 W0 -- Tape Transport Status (Continued)

Bit	Definition
7	Command Time-Out -- This bit indicates that the drive failed to respond within a controller-selected time interval. The error and tape error bits are set when this bit is set. If during a Read Binary or Skip Forward command, a nonzero value is in device register 4, then an EOR is also reported.
8-11	Rewind Status -- This bit indicates the rewind status of the transport and is set whenever the transport is rewinding.
12-15	Rewind Mask -- These bits enable the assigned unit to generate a rewind complete interrupt. The rewind complete interrupt is set when the rewind mask bit is on and the rewind status bit is off. Software can disable the interrupt by resetting the rewind mask bit. The interrupt is reported only when the controller is not performing a previously initiated command.

3.8.2 W1 -- Read Overflow Status Count (LSB)

The 16 bits of W1 are normally meaningful only when a Read Binary Forward command is performed. These 16 bits plus the eight MSBs of W2 form a 24-bit read overflow status count. The read overflow status count contains a count of the number of characters that were contained in the record, minus the initial read offset character count and the initial read buffer character count. Table 3-14 defines the bit assignments for W1.

Table 3-14 W1 -- Read Overflow Status Count

Bit	Definition
0-15	Contains the upper 16 bits of the 24-bit read overflow status count.

3.8.3 W2 -- Read Overflow Status Count (MSB)

The eight MSBs of W2 contain the eight MSBs of the 24-bit read overflow status count. The eight LSBs of W2 return an error classification status from the transport when a hard error occurs. Table 3-15 defines the functions of these bits.

Table 3-15 W2 -- Read Overflow Status Count MSB

Bit	Definition
0-7	Contains the lower 8 bits of the 24-bit read overflow status count
8-15	Used to return the status on a hard error (refer to W7, bit 10 for more information)

3.8.4 W3 -- Read Offset

During normal operation, this register is used for read offset and is used by the controller to provide a means of reading large records when only small memory buffer areas are available. Read offset is normally used by the controller when a Read Binary Forward command is performed. The controller decrements the read offset count each time a character is read and inhibits transfer of characters into the memory buffer until the read offset count reaches zero. The largest read offset value that can be specified is 65,535. No characters are transferred into TILINE memory if the record contains a character count less than or equal to the read offset value. This register is also used to return special transport status when a hard error condition is encountered. Table 3-16 defines the bit assignments for W3.

Table 3-16 W3 -- Read Offset

Bit	Definition
0-15	Read Offset -- These bits define the number of characters to read before starting a transfer to memory.

3.8.5 W4 -- Character Count

W4 serves several functions, depending on which command is performed. The commands that use W4 are Read Binary Forward, Write Binary, Record Skip Forward, Record Skip Reverse, and Erase. Table 3-17 defines the bit assignmentsfor W4.

Table 3-17 W4 -- Character Count

Bit	Definition
0-15	The count supplied in W4 is used with Read commands and is counted down as each character is read. W4 contains the remaining number of bytes not read if an error occurs. The Write command uses the count just like the Read commands but it indicates the number of bytes not written.

W4 for the Read Binary Forward command corresponds to the size of the TILINE memory buffer available to the controller. At the end of the operation, W4 contains the decremented character count. The controller writes the exact number of characters specified by the CPU and the write binary operation unless an abortive condition occurs. W4 is decremented each time a character is written on tape. W4 contains 0 when a normal operation reaches completion.

The Erase command uses W4 to control the length of tape erased, which is increased by one character length for each count in W4. The count is decremented and is normally 0 for a successful erase operation.

The Record Skip Forward and Record Skip Reverse commands use W4 to count the number of records to skip. The count is decremented each time a record is skipped. If an EOF mark is detected before the count is decremented to 0, the operation is aborted and W4 contains the decremented skip count. W4 is normally 0, if an EOF mark is not encountered when the Skip command completes.

3.8.6 W5 -- Buffer Address (LSBs)

Bits 0 through 14 of W5 are loaded by the CPU via the TILINE with the 15 LSBs of the 20-bit TILINE memory buffer starting word address. The LSB of this register is forced to 0 by the controller. At the end of an operation, W5 contains the incremented memory buffer address, shifted right one place. This word is used only by the Write Binary and Read Binary Forward commands.

3.8.7 W6 -- Command and Transport Select
W6 contains the unit select, command buffer, and data buffer memory address information. Table 3-18 defines the bit assignments for W6.

Table 3-18 W6 -- Command and Transport Select

Bit	Definition
0-1	Unit Select -- Bit 0 set to one to select unit 0. Bit 1 set to one to select unit 1. If more than one bit is set, the controller selects only one unit with priority to the MSB.
2-3	Not used, always set to 0.
4-7	Command Codes -- Specify which command the controller performs. The following list summarizes the command assignments. Refer to the following paragraphs for a description of the commands.

Bit 4 5 6 7	Command
0 0 0 0	No operation (NOP)
0 0 0 1	Buffer Sync
0 0 1 0	Write EOF
0 0 1 1	Record Skip Reverse
0 1 0 0	Read Binary Forward
0 1 0 1	Record Skip Forward
0 1 1 0	Write Binary Forward
0 1 1 1	Erase
1 0 0 0	Read Transport Status
1 0 0 1	Read Transport Status
1 0 1 0	Rewind
1 0 1 1	Rewind and Offline
1 1 0 0	NOP
1 1 0 1	NOP
1 1 1 0	NOP
1 1 1 1	Extended Control and Status

Refer to the extended mode commands in paragraph 3.9 for more information.

3.8.7.1 W6, Bit 8 -- Write Diagnostic. The Write Diagnostic command bit is used to to verify the error detection features of the tape transport.

3.8.7.2 W6, Bits 9 and 10. These bits are not used and are normally set to zero.

3.8.7.3 W6, Bits 11 Through 15. Bits 11 through 15 are the five MSBs of the TILINE starting memory address. These bits are used by the controller during the Read Binary and the Write Binary commands.

3.8.8 W7 -- Status and Control
W7 contains both control and status information. The control information is entered into W7 by the CPU. The status information is entered by the controller as described in Table 3-19 and Table 3-20.

Table 3-19 W7 -- Status and Control

Bit	Definition
0	Idle -- This bit is set to 0 by the software to activate the controller and begin performing the commands in bits 4 through 7 of W6. When a command finishes successfully or terminates due to an error, the controller sets bit 0, 1, or 2. If a command is used when the idle bit is 0, the controller ignores the command.
1	Operation Complete -- This bit is set when a command completes without an error.
2	Error -- This bit is set when an operation is terminated due to an error. This bit is reset by the software.
3	Interrupt Enable -- This bit enables the controller to generate an interrupt when the operation completes or error bit is set. Note that WO interrupts (rewind complete) are independent of W7.
4	Not used.
5	Not used.
6	PE Format -- This bit is always set for the MT3200.
7	Abnormal Completion -- This is set if a tape operation is terminated due to an I/O reset or a power-fail warning that is detected by the TILINE.

Table 3-19 W7 -- Staus and Control (Continued)

Bit	Definition
8	Interface Parity error -- This is set if the controller detects parity errors on the transport read data lines.
9	Error Correction Enabled -- This bit is set when a read binary operation is performed on a PE tape and a single bit dropout is corrected by the vertical parity information recorded on the tape. The error status bit is also set.
10	Hard Error -- There are two types of hard errors, one is recoverable and the other is not recoverable. The unrecoverable hard error results when the tape drive exhausts all retry capabilities and fails to correct the error. This error causes the TILINE hard error status and offline status bits to set. If the hard error status is true after command completion, an offline status is issued in W0, bit 0. This type of hard error results from the situations listed below. * A hard error occurring in a true write operation that goes beyond 16 automatic retries. * An attempt to write records greater than 32K bytes in length. * A transport transmission error when the cache transfer rate exceeds the rate the controller can handle. * An attempt to write a new block during a write edit operation that is greater than the original block.

Table 3-19 W7 -- Staus and Control (Continued)

Bit	Definition
10 (cont.)	The recoverable hard error condition is returned to the controller prior to command completion. This causes the hard error status and online status in WO, bit 0 to set. This type of hard error results from the situations listed below. * A transport record length error during a a read or write operation. This happens when the record is greater than the maximum block size setting but less than 32K bytes. * A write parity error. All media write errors are automatically corrected by the MT3200 unit recovery logic. * The record that was read contains an uncorrectable read data error. * An invalid software command was issued. For either type of hard error, the three bytes of transport status are returned to the TILINE interface in W2, bits 8 through 15, and W3. Refer to Table 3-20 for the TPCS status of the MT3200.
11	TILINE Memory Read Parity Error -- This bit sets after a Write Binary command completes and a memory read error occurs during a data transfer. The error status bit is also set.

Table 3-19 W7 -- Status and Control (Continued)

Bit	Definition
12	TILINE Timing Error -- This bit is set when there is a data transfer timing error. During a read operation, the TILINE did not transfer a word before the next word was assembled. During a write operation, the TILINE did not have a new word available when it was required by the controller. The TILINE timing error does not abort operations. The error status bit is set.
13	TILINE Time-Out Error -- This bit is set if a transfer cycle is not completed within 10 microseconds after the controller gains TILINE access. Time-out is reported only during a Read Binary or Write Binary command. Tape operation is not stopped to assure proper interrecord gap (IRG) positioning. The error status bit is set.
14	Format Error -- Always set to zero.
15	Tape Error -- This bit is set if one of the Transport errors listed belows occurs. * Offline * BOT * EOR * EOF * Write Ring * Tape Rewinding * EOT * Command Time-Out

Table 3-20 MT3200 TPCS Status

TPCS Reg.	Bit	Contents
2		Error Classification
	8	Density Found/Operating Density (bpi)
		000 = 800
	9	010 = 3200
		100 = 1600
	10	110 = 6250
	11	Write from host to cache overrun
	12	Read from tape to cache overrun
	13	Cache automatically expanded block size:
	14	000 = 9K bytes 110 = 32K bytes
	15	100 = 16K bytes 011 = 64K bytes
		010 = 24K bytes
3		Track in Error
	0	Track 0 in error
	1	Track 1 in error
	2	Track 2 in error
	3	Track 3 in error
	4	Track 4 in error
	5	Track 5 in error
	6	Track 6 in error
	7	Track 7 in error
	15	Track P in error
		Read/Write Retry Count in Current Host Record
	8 Through 14	MSB LSB

3.9 DETAILED MT3200 CONTROLLER COMMAND DESCRIPTIONS

The following paragraphs describe the detailed tape controller command descriptions and the extended mode self-test status commands.

3.9.1 Buffer Sync (Write Sync)

Use this command to ensure that all pending writes complete. The controller remains busy until the entire contents of the controller and transport buffers are written on tape.

3.9.2 Write EOF

This command causes the file mark record to be written on tape preceded by a 101.6-millimeter (4-inch) gap. For a PE transport, the controller verifies that the file mark was properly written on the tape. A PE hard error status is reported if the file mark is not properly written on the tape.

The EOT and offline status are reported in the same manner as the write binary operation.

When EOF completes, either operation complete or error status is reported and an interrupt is issued if the interrupt enable bit (W7, bit 3) is set.

3.9.3 Record Skip Reverse

This command is performed after the skip forward operation except in the following instances:

* The tape is moving in the reverse direction.

* The operation terminates when BOT (instead of EOT) is detected. In this case, the BOT status is reported and the tape is positioned in the same place as during a Rewind command.

3.9.4 Read Binary Forward

Data from the tape is transferred to the main memory via the TILINE in a read binary operation. The controller accesses the TILINE as needed and transfers the tape characters, assembled in 16-bit words. The characters (bytes) are read sequentially from tape and deposited into successive memory locations. The characters are read starting at the address specified by W6, bits 11 through 15 (MSBs), and W5, bits 0 through 14 (LSBs). The controller transfers the number of characters specified by W4.

The transfer stops when the last character of the record has been assembled and transferred to main memory, provided that the character count specifies more characters than actually exist in the record. Instead of an operation complete at the end of the operation, the end of record (EOR) tape error and error status are set. In this situation, when the record contains an odd number of characters, the right half of the last assembled and transferred word contains ones (FF).

W3 (read offset) specifies the number of characters read from tape before the start of transfer to the main memory. Use this feature to read data out of long records when only small buffers are available. The controller continues to read the record (until it detects the postamble) after the specified number of characters are assembled and transferred to main memory. W1 (LSBs) and the left half of W2 (MSBs) contain the number of characters read from the record and not transferred after W4 reaches zero. This forms the 24-bit count of the remaining characters on the record.

3.9.5 Record Skip Forward

In the skip forward operation, the read head passes over the records in a forward direction with no transfer of data to TILINE memory. The number of records to skip is indicated in W4. The controller decrements W4 each time a record is terminated in one of the following ways:

* W4 reaches 0 and the head is properly positioned on the IRG following the last record skipped. EOF status is reported if the last record was a file mark record.

* W4 did not reach 0 but a file mark record was detected. The tape stops with the head positioned on the IRG following the file mark record. This record is counted as a normal record. In this case EOF status is reported.

* W4 did not reach 0 but EOT was detected during the last record skipped. This causes EOT status to be reported. The EOT status is also reported when the last record skipped is a file mark record.

3.9.6 Write Binary Forward

The controller fetches data from main memory via TILINE and records it on the tape in a write binary operation. The 16-bit words fetched from main memory are specified by the starting address of W5 and W6. The number of characters specified by W4 are written by the controller. If the initial contents of this register are 0, the controller starts the tape motion and reports the operation complete status. This is done after the controller erases the same length of tape that is indicated by the Erase command.

During a write binary operation, the read circuitry of the controller is active. Checks are performed on the written data as it passes across the read head. The read portion of the controller checks for vertical parity and any type of PE hard error. The following errors can also occur during a write binary operation.

* Timing Error -- Some of the characters are written twice on the tape.

* TILINE Time-Out Error -- The controller fetched at least one defective word. This causes at least two defective characters to be written on the tape.

* Offline -- Offline condition occurred on the transport during a write binary operation. When this happens, the length of the written record is random and the preamble and postamble may not be written on the tape.

* EOT -- The EOT marker passed across the EOT sensor during a write binary operation. The EOT status does not report again once the reflective strip passes the EOT sensor and a new forward operation is active for the same transport.

The write binary operation also has special diagnostic provisions that are described in W6, bit 8.

3.9.7 Erase

A portion of tape is deleted when this command is performed. The maximum length of tape that can be erased with one command is 1082.0 millimeters (42.6 inches). During an erase operation, an EOT or offline error can occur.

3.9.8 Read Transport Status

The Read Transport Status command reads W7, bit 6 to identify the transport type selected. This bit is always set. The controller then checks if the unit is offline. An idle, error, and tape error status are reported to W7, and an offline status is reported to W0 if the unit is offline. The controller then checks for a rewinding unit if it is not offline. If the unit is not rewinding, the controller reports an idle, error, and a tape error status in W7 and tape rewinding status in W0. If the unit is not offline and not rewinding, the controller reports an idle and operation complete status in W7 and the proper condition for BOT, EOT, and write ring in W0.

3.9.9 Rewind

The controller tests the unit to determine if it is already rewinding. If the unit is not rewinding, the controller issues the Rewind command and reports an idle and operation complete status in W7. If the unit is rewinding, the controller reports tape rewind status in W0 and idle, error, and tape status in W7.

3.9.10 Rewind and Offline

The Rewind and Offline command is processed the same as the Rewind command except that the controller issues a Rewind and Offline command.

3.9.11 No-Operation (NOP) Commands

Any NOP command results in an idle and complete status. The controller recognizes all NOP commands and returns the system to idle after setting the idle and complete bits.

3.9.12 Self-Test, Extended Command Status

The controller is capable of operating in the extended mode for maintenance. The extended commands initiate self-test routines, read the controller ROM revision, obtain status from the drive, and issue commands to the drive. To operate in the extended command mode for either control or status, enter an >F in the command block of W6. Then enter the appropriate command code in W3, bits 0 through 7. Table 3-21 defines the codes that must be placed in W3 for extended control and status. Table 3-22 lists the transport status that is available via the extended status. Read extended status bits retain information about the control status, configuration status, error history status, machine status, and the error history reset status.

Use the following two commands for each block of data transferred to get the status from the transport:

* Enter the Read Extended Status command by placing >F in the command block and by placing >22 (from Table 3-21) in the MSB of W3.

* Issue the command for the desired transport status by entering >F in the command block and the appropriate code from Table 3-21 in the MSB of W3. At the same time, the second command must include a transfer character count (up to 16 bytes) in W4 and a TILINE memory address for up to 16 bytes of status in W5.

The controller self-test can be called from the extended command field by entering >0000 in W3. A loop bit (bit 0) is provided in W3 to allow for scope loops on self-test. Placing >8000 in W3, bit 0 allows a loop on all self-tests. An IORESET is then the only exit method. It is a good practice to place zeroes in all other slave words, with W7 always being the last word entered to the controller.

If >7C is entered in the most significant byte of W3 during self-test, the revision level of the ROMs used in the tape/TILINE section of the board is reported in the least significant byte of W3.

After the controller issues the command code from W3 to the MT3200 drive, the controller enters a read transfer mode and transfers the number of bytes specified to the TILINE memory. If a write command is issued, a command time-out status occurs and the controller terminates with a normal completion status for those commands that do not result in a read (RSTR-) or write (WSTR-) strobe issued from the tape drive.

Table 3-21. Extended Commands

Command	Device Register 3 Bits 0	1	2	3	4	5	6	7
Controller:								
Report ROM Revision Level	0	1	1	1	1	1	0	0
Execute Self-Test	0	0	0	0	0	0	0	0
Loop on Self-Test	1	0	0	0	0	0	0	0
Tape Transport:								
Read Forward	0	0	1	0	0	0	0	0
Read Reverse	0	0	1	1	0	0	0	0
Read Reverse Edit	0	0	1	1	0	0	1	0
Write*	0	0	1	0	1	0	0	0
Write Edit*	0	0	1	0	1	0	1	0
Write File Mark	0	0	1	0	1	1	0	0
Erase Variable Length	0	0	1	0	1	0	0	1
Erase Fixed Length	0	0	1	0	1	1	0	1
Security Erase	0	0	1	0	1	1	1	1
Space Forward	0	0	1	0	0	0	0	1
Space Reverse	0	0	1	1	0	0	0	1
File Search Forward	0	0	1	0	0	1	0	0
File Search Forward (Ignore Data)	0	0	1	0	0	1	0	1
File Search Reverse	0	0	1	1	0	1	0	0
File Search Reverse (Ignore Data)	0	0	1	1	0	1	0	1
Write Sync	0	0	1	0	0	0	1	1
3200 bpi	0	0	1	1	0	1	1	1
1600 bpi (PE)	0	0	1	0	0	1	1	1
Read Extended Status	0	0	1	0	0	0	1	0
Read Current Status	0	0	1	0	0	0	0	0
Read Configuration Status	0	0	1	1	0	0	0	0
Read Error History Status	0	0	1	0	0	0	1	0
Read Machine Status	0	0	1	1	0	0	1	0
Read Error History Reset	0	0	1	1	0	0	1	1

Note:

* Results in command TILINE timing error because data transfer to the drive is not supported in this mode. Using these commands may result in lost data at the specified TILINE address as well as erasing a portion of tape.

Table 3-22. Read Extended Tape Status (Current Status)

Byte No.	Bit*	Contents	
		Current Status Block — Access Code 00100000	
0		Tape Status Byte #1:	
	0	IDENT-	Note — For all blocks:
	1	HER-	1 = True/Yes
	2	ICER-	0 = False/No
	3	FMK-	(Unless otherwise specified)
	4	RDY-	
	5	IONL-	
	6	RWD-	
	7	FPT-	
1		Tape Status Byte #2:	
	0	LDP-	
	1	EOT-	
	2	Read Retries Exceeded	
	3	Write Parity Error at Interface	
	4	Write Hard Error	
	5	Illegal Command	
	6		
	7		
2		Error Classification:	
	0, 1, 2	Cache Auto-Expanded Block Size	000 = 9K, 001 = 16K, 010 = 24K, 011 = 32K, 100 = 64K
	3	Read From Tape to Cache Overrun	
	4	Write From Host to Cache Overrun	
	5		
	6		
	7		
3		Track in Error:	
	0	Track 7	
	1	Track 6	
	2	Track 5	
	3	Track 4	
	4	Track 3	
	5	Track 2	
	6	Track 1	
	7	Track 0	

Note

* Bit 0 = LSB; Bit 7 = MSB, unless otherwise specified.

Table 3-22. Read Extended Tape Status (Current Status) (Continued)

Byte No.	Bit*	Contents
4	0	Track P in error
	1 Through 7	LSB … MSB: Read/Write Retry Count on Current Host Record
5	0 Through 4	LSB … MSB: Front Panel Error Code
6		Density Code
	0	Density Found/Operating Density (bpi):
	1	000 = 800 001 = 1600
	2	010 = 3200 011 = 6250
	3	Density Requested:
	4	000 = 800 001 = 1600
	5	010 = 3200 011 = 6250
	6	Read Density Conflict
	7	Write Density Conflict
7		Unfixed Block Count (includes file marks):
	0 Through 7	Block Detachable Structures Remaining in Cache
		Fixed Block Count From BOT (includes file marks):
8		Low Order Byte
9		Mid Order Byte
10		High Order Byte
		Sequence Number of Record in Hard Error:
11		Low Order Byte
12		Mid Order Byte
13		High Order Byte

Note

* Bit 0 = LSB; Bit 7 = MSB, unless otherwise specified.

Table 3-22. Read Extended Tape Status (Current Status) (Continued)

Byte No.	Bit*	Contents			
		Configuration Status Block — Access Code 00110000			
0		Capability:			
	0	800 bpi	0 = Do Not Have Capability		
	1	1600 bpi	1 = Do Have Capability		
	2	3200 bpi			
	3	6250 bpi			
	4	Other			
1		Vendor Code:			
2		Model Code:			
	0, 1, 2 Through 7	000 = Other 001 = M890-1 010 = M890-11	011 = M891-1 100 = M891-11 101 = M990-1	110 = M990-1 111 = M991-HPGCR	
3		Configuration State:			
	0	EOT Location	1 = EOT Search	0 = STD	(U3T-1)
	1	Parity	1 = External	0 = Internal	(U3T-2)
	2, 3	Maximum Block Size	00 = 9K 01 = 16K	10 = 24K 11 = 32K	(U3T-3) (U3T-4)
	4	Ramps	1 = Disabled	0 = Enabled	(U3T-5)
	5, 6, 7	LSB, Simulated Speed Setting, MSB			(U3T-6) (U3T-7) (U3T-8)
4		Software Configuration:			
	0				
	1				
	2				
	3	Post-EOT Streaming			(U5W-4)
	4	3200 bpi IDENT			(U5W-5)
	5				
	6				
	7				

Note

* Bit 0 = LSB; Bit 7 = MSB, unless otherwise specified.

Table 3-22. Read Extended Tape Status (Current Status) (Continued)

Byte No.	Bit*	Contents
		Error History Block — Access Code 00100010
0		Read Retry Count — Since Unload (255 MAX):
1		Write Retry Count — Since Unload (255 MAX):
		Track History — Error Counts Per Track (255 MAX):
2		Track 0
3		Track 1
4		Track 2
5		Track 3
6		Track 4
7		Track 5
8		Track 6
9		Track 7
10		Track P
		Machine Status Block — Access Code 00110010
		Head Position and Tachometer Count in Multiples of 1.28 inches:
0		Low Order Byte of Tach Count
1		High Order Byte of Tach Count
		Logical Command History:
2		Previous Host Command
3		2nd Previous Host Command
4		3rd Previous Host Command
5		4th Previous Host Command
6		5th Previous Host Command
7		Operating Status:
	0 1	Reel Size: 00 = Unknown, 01 = 7 Inch, 10 = 8½ Inch, 11 = 10½ Inch
	2	Door Lock Status: 0 = Unlocked, 1 = Locked

Note

* Bit 0 = LSB; Bit 7 = MSB, unless otherwise specified.