EXPLORER™ II PROCESSOR AND AUXILIARY PROCESSOR OPTIONS GENERAL DESCRIPTION

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, can cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computer device pursuant to Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference; in which case, the user at the user's own expense will be required to take whatever measures necessary to correct the interference.

WARNING: High voltages are present inside the chassis of this equipment. Only qualified service personnel who are familiar with the dangers of high voltages are permitted to open the chassis of this equipment to the service access position.

MANUAL REVISION HISTORY

Explorer™ II Processor and Auxiliary Processor Options General Description (2537187-0001)

Original Issue ..... June 1987

Texas Instruments Incorporated
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Austin, Texas 78769-2909

THE EXPLORER™ SYSTEM HARDWARE MANUALS

System Level Publications

Explorer 7-Slot System Installation 2243140-0001
Explorer System Field Maintenance 2243141-0001
Explorer System Field Maintenance Documentation Kit 2243222-0001
Explorer System Field Maintenance Supplement 2537183-0001
Explorer System Field Maintenance Supplement Documentation Kit 2549278-0001
Explorer NuBus™ System Architecture General Description 2537171-0001

System Enclosure Equipment Publications

Explorer 7-Slot System Enclosure General Description 2243143-0001
Explorer Memory General Description (8-megabytes) 2533592-0001
Explorer 32-Megabyte Memory General Description 2537185-0001
Explorer Processor General Description 2243144-0001
68020-Based Processor General Description 2537240-0001
Explorer II Processor and Auxiliary Processor Options General Description 2537187-0001
Explorer System Interface General Description 2243145-0001
Explorer NuBus Peripheral Interface General Description (NUPI board) 2243146-0001

Display Terminal Publications

Explorer Display Unit General Description 2243151-0001
CRT Data Display Service Manual, Panasonic code number FTD85055057C 2537139-0001
Model 924 Video Display Terminal User's Guide 2544365-0001

143-Megabyte Disk/Tape Enclosure Publications

Explorer Mass Storage Enclosure General Description 2243148-0001
Explorer Winchester Disk Formatter (ADAPTEC) Supplement to Explorer Mass Storage Enclosure General Description 2243149-0001
Explorer Winchester Disk Drive (Maxtor) Supplement to Explorer Mass Storage Enclosure General Description 2243150-0001
Explorer Cartridge Tape Drive (Cipher) Supplement to Explorer Mass Storage Enclosure General Description 2243166-0001
Explorer Cable Interconnect Board (2236120-0001) Supplement to Explorer Mass Storage Enclosure General Description 2243177-0001

143-Megabyte Disk Drive Vendor Publications

XT-1000 Service Manual, 5 1/4-inch Fixed Disk Drive, Maxtor Corporation, part number 20005 (5 1/4-inch Winchester disk drive, 112 megabytes) 2249999-0001
ACB-5500 Winchester Disk Controller User's Manual, Adaptec, Inc., (formatter for the 5 1/4-inch Winchester disk drive) 2249933-0001

1/4-Inch Tape Drive Vendor Publications	Series 540 Cartridge Tape Drive Product Description, Cipher Data Products, Inc., Bulletin Number 01-311-0284-1K (1/4-inch tape drive)	2249997-0001
	MT01 Tape Controller Technical Manual, Emulex Corporation, part number MT0151001 (formatter for the 1/4-inch tape drive)	2243182-0001
182-Megabyte Disk/Tape Enclosure MSU II Publications	Mass Storage Unit (MSU II) General Description	2537197-0001
182-Megabyte Disk Drive Vendor Publications	Control Data® WREN™ III Disk Drive OEM Manual, part number 77738216, Magnetic Peripherals, Inc., a Control Data Company	2546867-0001
515-Megabyte Mass Storage Subsystem Publications	SMD/515-Megabyte Mass Storage Subsystem General Description (includes SMD/SCSI controller and 515-megabyte disk drive enclosure)	2537244-0001
515-Megabyte Disk Drive Vendor Publications	515-Megabyte Disk Drive Documentation Master Kit (Volumes 1, 2, and 3), Control Data Corporation	2246129-0002
	Volume 1, General Description, Operation, Installation and Checkout, and Part Data	2246125-0004
	Volume 2, Theory, General Maintenance, Trouble Analysis, Electrical Checks, and Repair Information	2246125-0005
	Volume 3, Diagrams	2246125-0006
1/2-Inch Tape Drive Publications	MT3201 1/2-Inch Tape Drive General Description	2537246-0001
1/2-Inch Tape Drive Vendor Publications	Cipher CacheTape® Documentation Manual Kit (Volumes 1 and 2 With SCSI Addendum and, Logic Diagram), Cipher Data products	2246130-0001
	1/2-Inch Tape Drive Operation and Maintenance (Volume 1), Cipher Data Products	2246126-0001
	1/2-Inch Tape Drive Theory of Operation (Volume 2), Cipher Data Products	2246126-0002
	SCSI Addendum With Logic Diagram, Cipher Data Products	2246126-0003

Printer Publications

Model 810 Printer Installation and Operation Manual	2311356-9701
Omni 800™ Electronic Data Terminals Maintenance Manual for Model 810 Printers	0994386-9701
Model 850 RO Printer User's Manual	2219890-0001
Model 850 RO Printer Maintenance Manual	2219896-0001
Model 850 XL Printer User's Manual	2243250-0001
Model 850 XL Printer Quick Reference Guide	2243249-0001
Model 855 Printer Operator's Manual	2225911-0001
Model 855 Printer Technical Reference Manual	2232822-0001
Model 855 Printer Maintenance Manual	2225914-0001
Model 860 XL Printer User's Manual	2239401-0001
Model 860 XL Printer Maintenance Manual	2239427-0001
Model 860 Xl Printer Quick Reference Guide	2239402-0001
Model 860/859 Printer Technical Reference Manual	2239407-0001
Model 865 Printer Operator's Manual	2239405-0001
Model 865 Printer Maintenance Manual	2239428-0001
Model 880 Printer User's Manual	2222627-0001
Model 880 Printer Maintenance Manual	2222628-0001
OmniLaser™ 2015 Page Printer Operator's Manual	2539178-0001
OmniLaser 2015 Page Printer Technical Reference	2539179-0001
OmniLaser 2015 Page Printer Maintenance Manual	2539180-0001
OmniLaser 2108 Page Printer Operator's Manual	2539348-0001
OmniLaser 2108 Page Printer Technical Reference	2539349-0001
OmniLaser 2108 Page Printer Maintenance Manual	2539350-0001
OmniLaser 2115 Page Printer Operator's Manual	2539344-0001
OmniLaser 2115 Page Printer Technical Reference	2539345-0001
OmniLaser 2115 Page Printer Maintenance Manual	2539356-0001

Communications Publications

990 Family Communications Systems Field Reference	2276579-9701
EI990 Ethernet® Interface Installation and Operation	2234392-9701
Explorer NuBus Ethernet Controller General Description	2243161-0001
Communications Carrier Board and Options General Description	2537242-0001

THE EXPLORER™ SYSTEM SOFTWARE MANUALS

Mastering the Explorer Environment	Explorer Technical Summary	2243189-0001
	Introduction to the Explorer System	2243190-0001
	Explorer Zmacs Editor Tutorial	2243191-0001
	Explorer Glossary	2243134-0001
	Explorer Networking Reference	2243206-0001
	Explorer Diagnostics	2533554-0001
	Explorer Master Index to Software Manuals	2243198-0001
	Explorer System Software Installation Guide	2243205-0001
Programming With the Explorer	Explorer Programming Concepts	2549830-0001
	Explorer Lisp Reference	2243201-0001
	Explorer Input/Output Reference	2549281-0001
	Explorer Zmacs Editor Reference	2243192-0001
	Explorer Tools and Utilities	2549831-0001
	Explorer Window System Reference	2243200-0001
Explorer Options	Explorer Natural Language Menu System User's Guide	2243202-0001
	Explorer Relational Table Management System User's Guide	2243203-0001
	Explorer Grasper User's Guide	2243135-0001
	Explorer Prolog User's Guide	2537248-0001
	Programming in Prolog, by Clocksin and Mellish	2537157-0001
	Explorer Color Graphics User's Guide	2537157-0001
	Explorer TCP/IP User's Guide	2537150-0001
	Explorer LX™ User's Guide	2537225-0001
	Explorer LX System Installation	2537227-0001
	Explorer NFS™ User's Guide	2546890-0001
	Explorer DECnet™ User's Guide	2537223-0001
	Personal Consultant™ Plus Explorer	2537259-0001
System Software Internals	Explorer System Software Design Notes	2243208-0001
	Release Information, Explorer System Software	2549844-0001

CONTENTS

ABOUT THIS MANUAL

Purpose

This document provides a general description of the Texas Instruments (TI) Explorer II processor board and the auxiliary processor options. The information in this document is intended for use by system designers, value-added resellers (VARs), maintenance personnel, system users, and operators.

Contents

This manual is divided into the following three sections:

Section 1: General Information — Provides a general overview of the processor and auxiliary processor options. This overview includes features, specifications, and a list of reference documents.

Section 2: Installation and Operation — Provides detailed information on installation and operation of the processor board and the auxiliary processor options.

Section 3: Equipment Description — Provides a brief general description of the processor board and the auxiliary processor options.

1 GENERAL INFORMATION

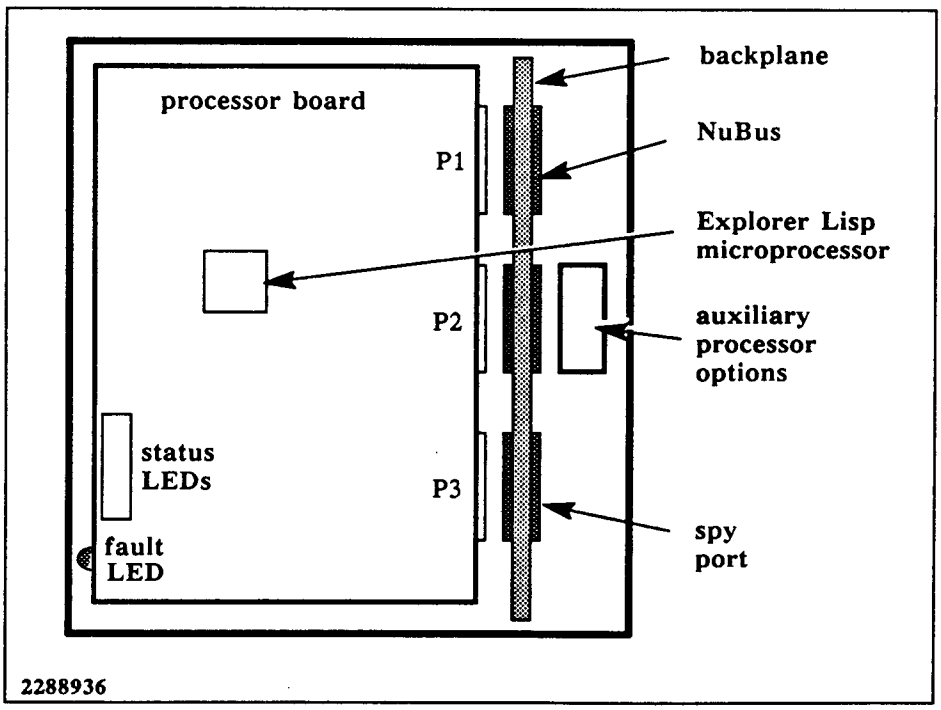
Introduction

1.1 This section provides general information on the Texas Instruments Explorer II processor board and the auxiliary processor options (Figure 1-1). This information is organized under the following topics:

- Features
- Specifications
- Reference documents

The Explorer II processor board is a standard three-high Eurocard board that is used as the Lisp processor in an Explorer 7-slot system enclosure. The processor board interfaces over the NuBus (connector P1) as a master or slave to other elements in the 7-slot system enclosure. The auxiliary processor options interface to the processor board over connector P2. A spy port at connector P3 is provided for an external testing device. Status and fault light-emitting diodes (LEDs) are provided for maintenance information on the processor board and the auxiliary processor options.

Figure 1-1 **Explorer II Processor With Auxiliary Processor Options**



Auxiliary processor options refers to the different option boards that can be associated with the Explorer II processor board. The logic on the Explorer II processor board is arranged to operate with different auxiliary processor option boards with only software changes. The option boards can be installed in the field as they become available.

The Explorer Lisp microprocessor is the principal Lisp processing element on the processor board. The Lisp microprocessor is a very-large-scale-integration (VLSI) microprocessor chip that contains 553,687 transistors and 116,736 bits of random-access memory (RAM). It replaces most of the processor logic that is now located on a two-board processor assembly in the existing TI Explorer computer system.

Features

1.2 The processor board and the auxiliary processor options have the following key features:

- Explorer Lisp microprocessor
- Cache memory logic
- Virtual memory mapping logic
- Microinstruction control store RAMs (32K x 64 bits)
- Spy port for extensive processor board testing and microcode development
- Auxiliary processor options port

Specifications

1.3 Table 1-1 lists the environmental and power specifications for the processor board and the auxiliary processor options.

Table 1-1 **Processor Board and Auxiliary Processor Options Specifications**

Item	Specifications
Power input	
Processor board	+5 volts, 27.5 amperes, 138 watts +12 volts, 50 milliamperes, 600 milliwatts
Temperature	
Operating	10° to 35° C (50° to 95° F)
Nonoperating	-40° to 65° C (-40° to 149° F)
Relative humidity	
Operating	20% to 80% (noncondensing)
Nonoperating	5% to 95% (noncondensing)

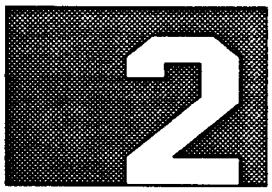
Reference Documents

1.4 The reference documents listed in Table 1-2 provide additional technical information on the Explorer II processor and the auxiliary processor options:

Table 1-2 Reference Documents

Category	Document	TI Part Number
Primary Documents	Explorer System Field Maintenance	2243141-0001
	Explorer System Field Maintenance Supplement	2537183-0001
	Explorer II Processor Board Assembly	2540830-0001
	Explorer II Processor Board Logic Diagram	2540832-0001
	Explorer II Processor Board Specification	2540834-0001
	32-Bit Lisp Microprocessor Specification (Explorer Lisp Microprocessor)	2248114-0001
Secondary Documents	Explorer NuBus System Architecture General Description	2537171-0001
	Explorer Processor General Description	2243144-0001
	NuBus Specification	2242825-0001
	Explorer Backplane Specification (Local Bus & NuBus)	2235539-0001
	System 1500 Backplane Specification (NuBus Only)	2535855-0001
	Explorer I Processor Two-Board Assembly	2243881-0001
	Explorer I Processor Main Board Assembly	2243895-0001
	Explorer I Processor Main Board Logic Diagram	2243897-0001
	Explorer I Processor Auxiliary Board Assembly	2236405-0001
	Explorer I Processor Auxiliary Board Logic Diagram	2236407-0001
	Explorer I Processor Specification	2236414-0001

INSTALLATION AND OPERATION



Introduction

2.1 This section includes information on the installation and operation of the Explorer II processor board and the auxiliary processor options. The installation and operation information is discussed under the following topics:

- TI-installed processor board and auxiliary processor options
- Unpacking the processor board and auxiliary processor options
- Installing the processor board
- Installing the auxiliary processor options
- Processor board and auxiliary processor options operation

NOTE: The following installation and unpacking paragraphs apply to situations where the processor board and the auxiliary processor options are added to an existing Explorer system. If you have purchased a new Explorer system with the processor board and the auxiliary processor options installed, disregard the paragraphs covering installation.

TI-Installed Processor Board and Auxiliary Processor Options

2.2 The following procedure outlines the tasks you must perform before TI installs your Explorer II processor board and the auxiliary processor options:

1. Note the serial number on the box that contained this manual.
2. Call the Field Service Communications Center (FSCC) at 800-572-3300 to schedule a site inspection (if required) and the equipment installation. The following information is required to schedule a TI installation:
   a. System serial number
   b. Customer name
   c. Customer street address and zip code
   d. Name and telephone number of customer personnel to contact
   e. Purchase order number if the installation was not ordered with the equipment

Unpacking the Processor Board and Auxiliary Processor Options

2.3 For Explorer II processor board and auxiliary processor options owners who do their own installation, perform the following steps to unpack the equipment:

1. Visually inspect the shipping container for damage. If the inspection reveals damage to the shipping container, contact the carrier agent for instructions on filing a claim. The carrier, not Texas Instruments, is responsible for damage during shipment. Resolve all problems relating to shipping damage before proceeding with the installation.

2. Note on the delivery receipt any problems that you discover.

3. Be sure that the driver has signed the delivery receipt.

4. Obtain the following tools to unpack the processor board or the auxiliary processor options:

   a. Safety glasses

   b. Knife for cutting the sealing tape

CAUTION: The processor board contains static-sensitive electronic components. To avoid damage to these components, ensure that you are well grounded before handling the processor board.

The recommended method is to use a static-controlled system consisting of a static-control floor or table mat and a static-control wrist strap. These are commercially available. If you do not have a static-control system, you can discharge any accumulated static charge by touching a grounded object prior to handling the processor board. Then, as a further precaution, place the processor board on a grounded surface after removing it from its shipping container.

Before storing or transporting the processor board, return it to its protective package.

---

5. As you unpack the processor board (Figure 2-1) and the auxiliary processor option (Figure 2-2), inspect the equipment for shipping damage. If the inspection reveals damage that you feel is significant, stop the unpacking procedure and contact the carrier agent. After the carrier agent inspects the damage, contact a Texas Instruments Field Service office. Save all the packing material for future use whenever possible.

Figure 2-1 Processor Board Shipping Container

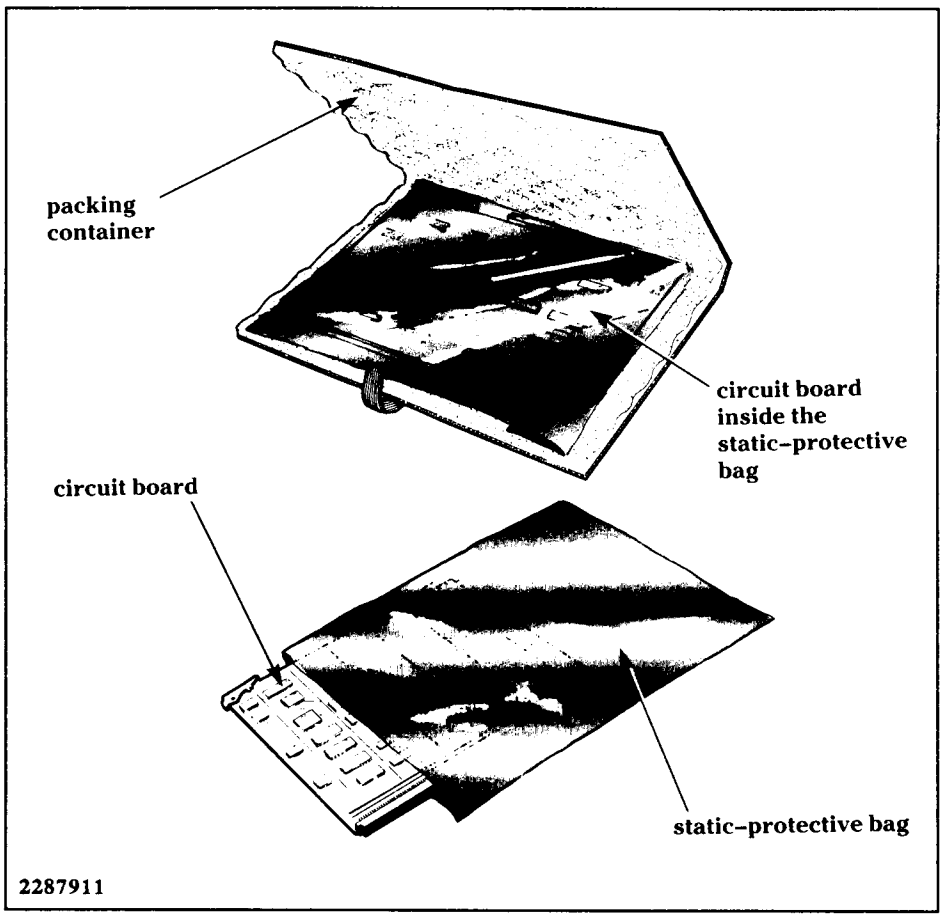
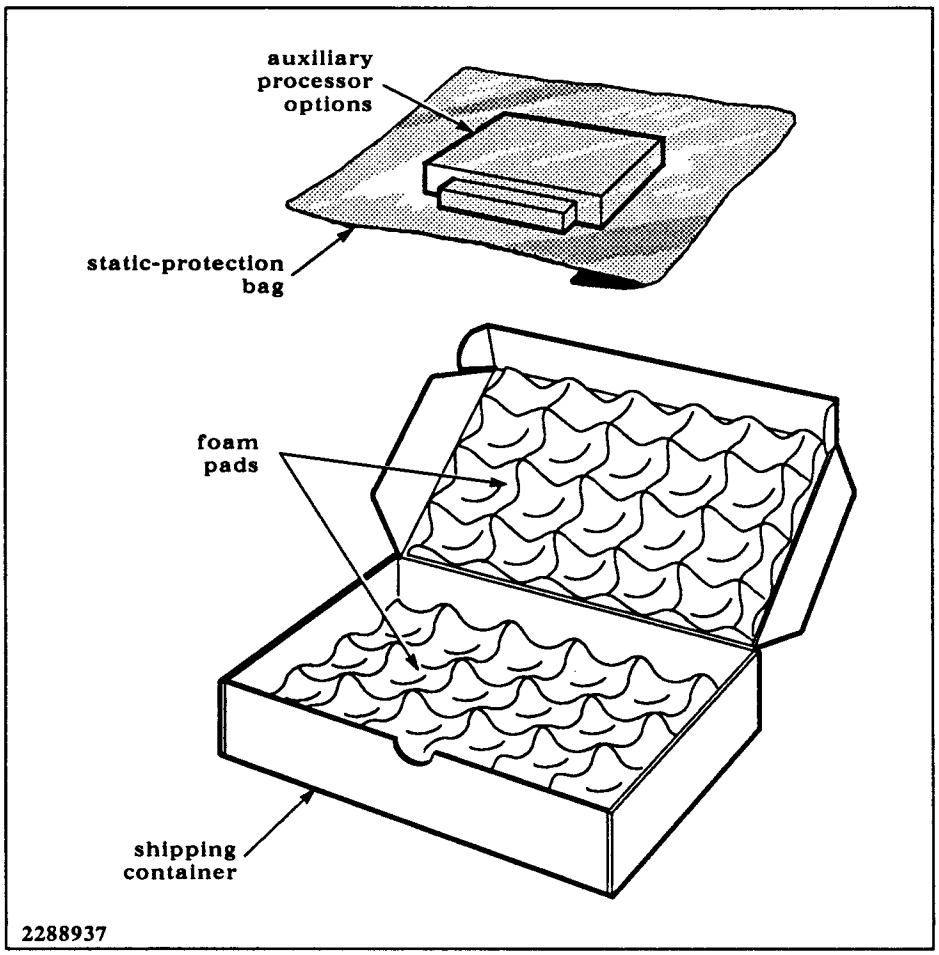


Figure 2-2 Auxiliary Processor Options Shipping Container



Installing the Processor Board

2.4 Perform the following procedure to install the processor board in a standard Explorer system enclosure:

CAUTION: Before you begin this procedure, be sure that Release 3 software is installed on your system. Refer to the *Explorer System Software Installation* manual for instructions on installing the Release 3 software.

NOTE: If you have made any changes to the existing Release 2.X software on your system, you should keep this software so you can put these changes into the new Release 3 software at a later time, if you so desire.

WARNING: To eliminate the possibility of electrical shock during option or upgrade installation, you must isolate the system enclosure from all potential energy sources. To isolate the system enclosure:

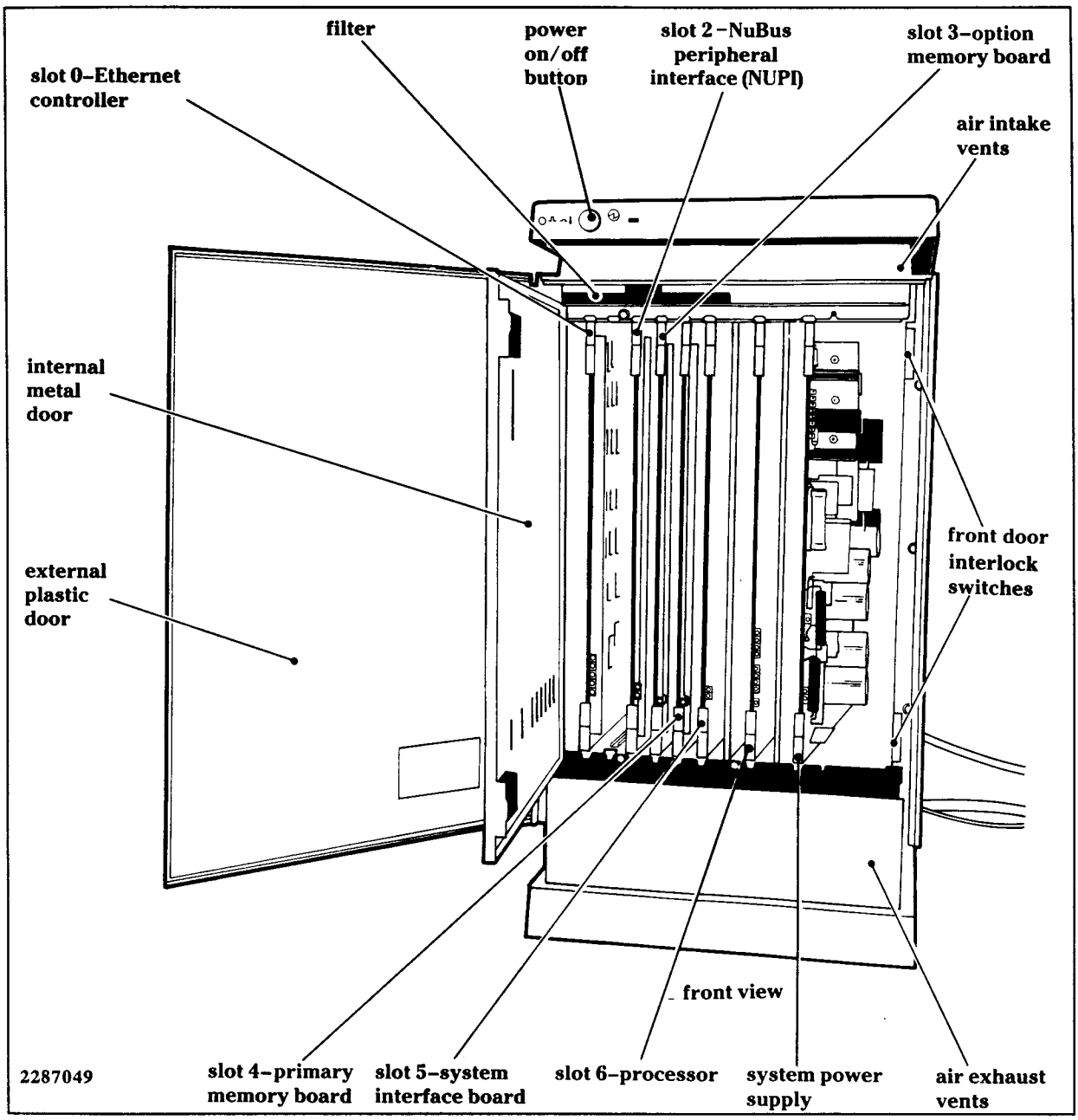
1. **Power off the system enclosure and all peripherals.**
2. **Disconnect the power cable from the wall outlet of all local peripherals connected to the system enclosure.**
3. **Unplug the system enclosure power cable from the wall outlet.**

1. Power off all the equipment as indicated in the above warning.
2. Open the external plastic front door (Figure 2-3) and the inner metal door to gain access to the card cage of the system enclosure.
3. Remove the Explorer I processor two-board assembly from slot six.
4. Position the Explorer II processor board so that the fault LEDs are near the bottom of the 7-slot enclosure; then, insert the board into slot six.
5. Close the inner metal door and the external plastic front door of the system enclosure.
6. Reconnect all cables that were disconnected during the power off procedure in step 1.

NOTE: The inner, metal front door and the rear door of the system enclosure must be closed for the system to be operational.

7. Power up all the equipment that was powered off in step 1. Be sure you run the extended self-tests.
8. Run Explorer standalone diagnostics EXP2 to check the operation of the Explorer II processor board. If the Release 3 software is not on your disk, boot EXP2 from the cartridge tape. Refer to the *Explorer Diagnostics* for instructions on running EXP2.
9. Boot the Lisp system as a final system check. Refer to the *Explorer System Software Installation Guide* for instructions on booting the system.

Figure 2-3 Typical Processor Board Installation



Installing the Auxiliary Processor Options

2.5 The Explorer II processor board must be installed prior to the installation of the auxiliary processor options.

Perform the following procedure to install the auxiliary processor options in an Explorer system enclosure:

WARNING: To eliminate the possibility of electrical shock during option or upgrade installation, you must isolate the system enclosure from all potential energy sources. To isolate the system enclosure:

1. **Power off the system enclosure and all peripherals.**
2. **Disconnect the power cable from the wall outlet of all local peripherals connected to the system enclosure.**
3. **Unplug the system enclosure power cable from the wall outlet.**

---

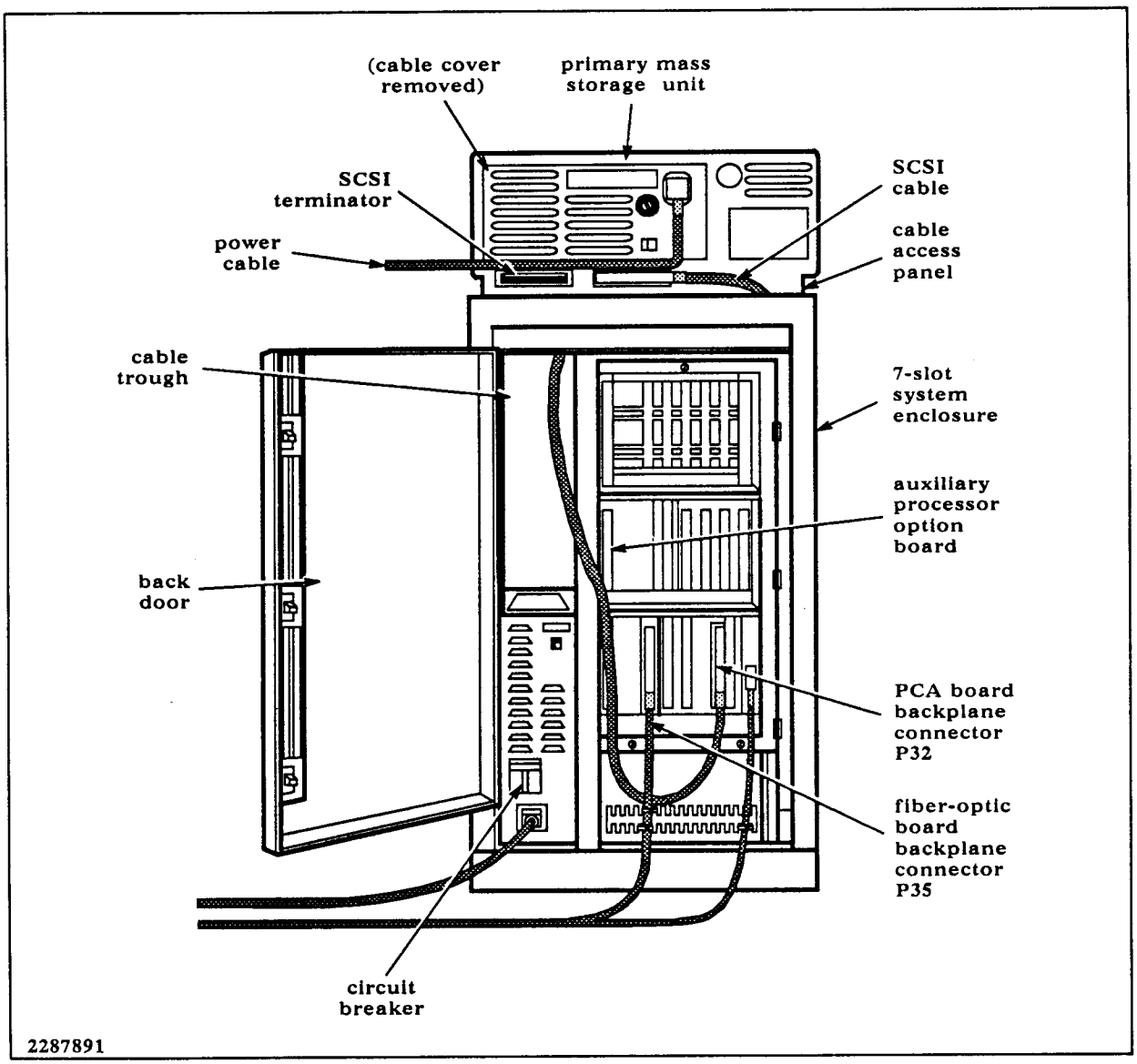
1. Power off all the equipment as indicated in the above warning.
2. Open the plastic rear door (Figure 2-4) to gain access to the adapter guide assembly of the system enclosure.
3. Insert the applicable auxiliary processor options board into the connector on the rear of the backplane that is associated with connector P2 of the Explorer II processor board, which is normally in slot six.
4. Close the plastic rear door of the system enclosure.
5. Reconnect all cables that were disconnected during the power off procedure in step 1.

NOTE: The inner, metal front door and the rear door of the system enclosure must be closed for the system to be operational.

---

6. Power up all the equipment that was powered off in step 1. Be sure you run extended self-tests.
7. Install the software support for the auxiliary processor options using the instructions in the *Explorer System Software Installation* manual.
8. Run Explorer standalone diagnostics EXP2 to check the operation of the Explorer II processor board and the applicable auxiliary processor options board that is installed. If the Release 3 software is not on your disk, boot EXP2 from the cartridge tape. Refer to the *Explorer Diagnostics* for instructions on running EXP2.
9. Boot the Lisp system as a final system check.

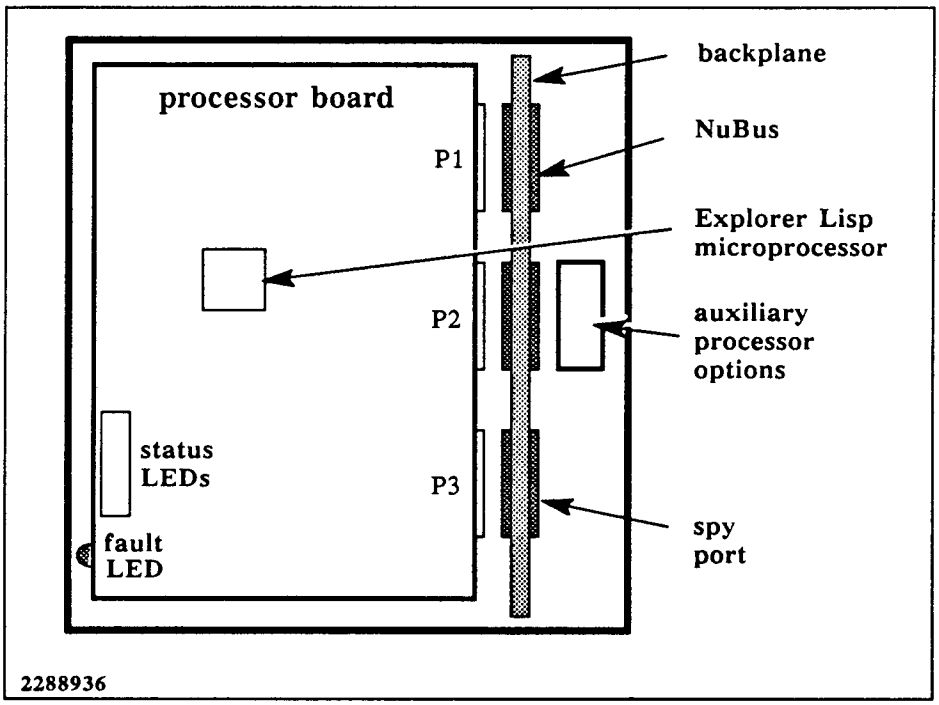
Figure 2-4 Typical Auxiliary Processor Options Board Installation



Processor Board and Auxiliary Processor Options Operation

2.6 The processor board plugs into the backplane as shown in Figure 2-5. Backplane connector P1 connects to the NuBus, which provides the interface to other boards in the system. Connector P2 connects to the auxiliary processor. Connector P3 provides an access point for spy port diagnostic tests. Status and fault LEDs are provided to aid the operator in troubleshooting the processor board and the auxiliary processor options.

Figure 2-5 **Explorer II Processor With Auxiliary Processor Options**



3 EQUIPMENT DESCRIPTION

Introduction

3.1 This section contains a functional description of the Explorer II processor board and the auxiliary processor options. For a more detailed description of this equipment, refer to the reference documents listed in Section 1 of this manual. The information in this section is arranged under the following topics:

- Processor board description
- Auxiliary processor options description

Processor Board Description

3.2 For a physical layout of the processor board, refer to Figure 3-1. A functional block diagram of the processor board is shown in Figure 3-2. Refer to both of these diagrams as appropriate during the following discussions. The processor board description is arranged under the following topics:

- Explorer Lisp microprocessor overview
- Processor board logic overview
- Configuration ROM data
- Interface description

To aid in the execution of a Lisp-orientated virtual machine, Lisp data is stored in main memory in 32-bit quantities called storage quantums or Qs. A Q is divided into three fields. The first is a 2-bit field, Q<31:30>, which is used to store what is called the CDR (a Lisp primitive function) code. The information stored in this two-bit field is used to reduce the amount of storage required for list data. The next field is a 5-bit field, Q<29:25>, which is used to store the Q's DATA TYPE or tag. The remaining field, Q<24:00>, is 25 bits in length and contains either a Pointer (the address of another Q) or immediate data, depending on the Q's DATA TYPE. The 25-bit field is usually called the Q-POINTER.

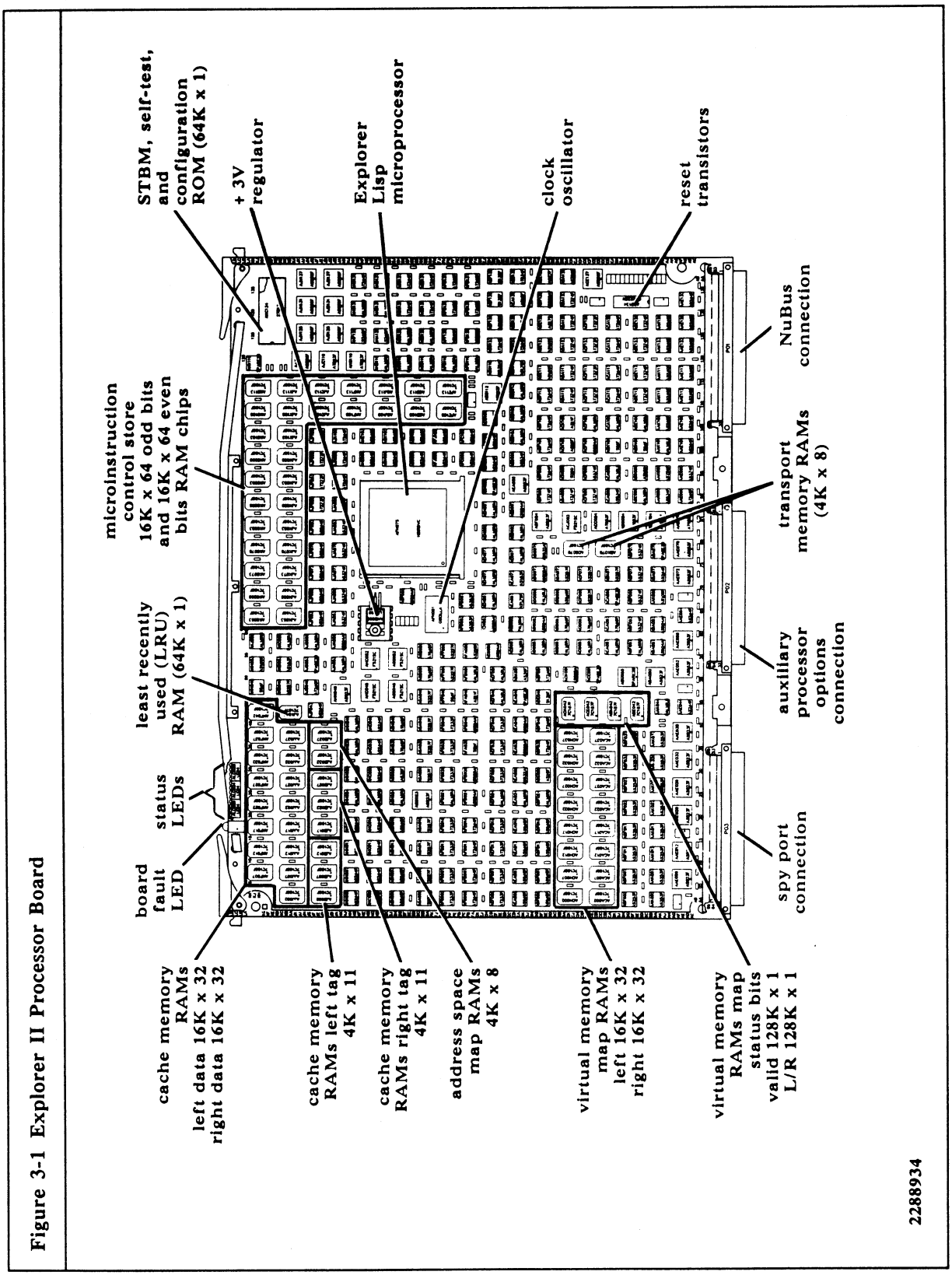
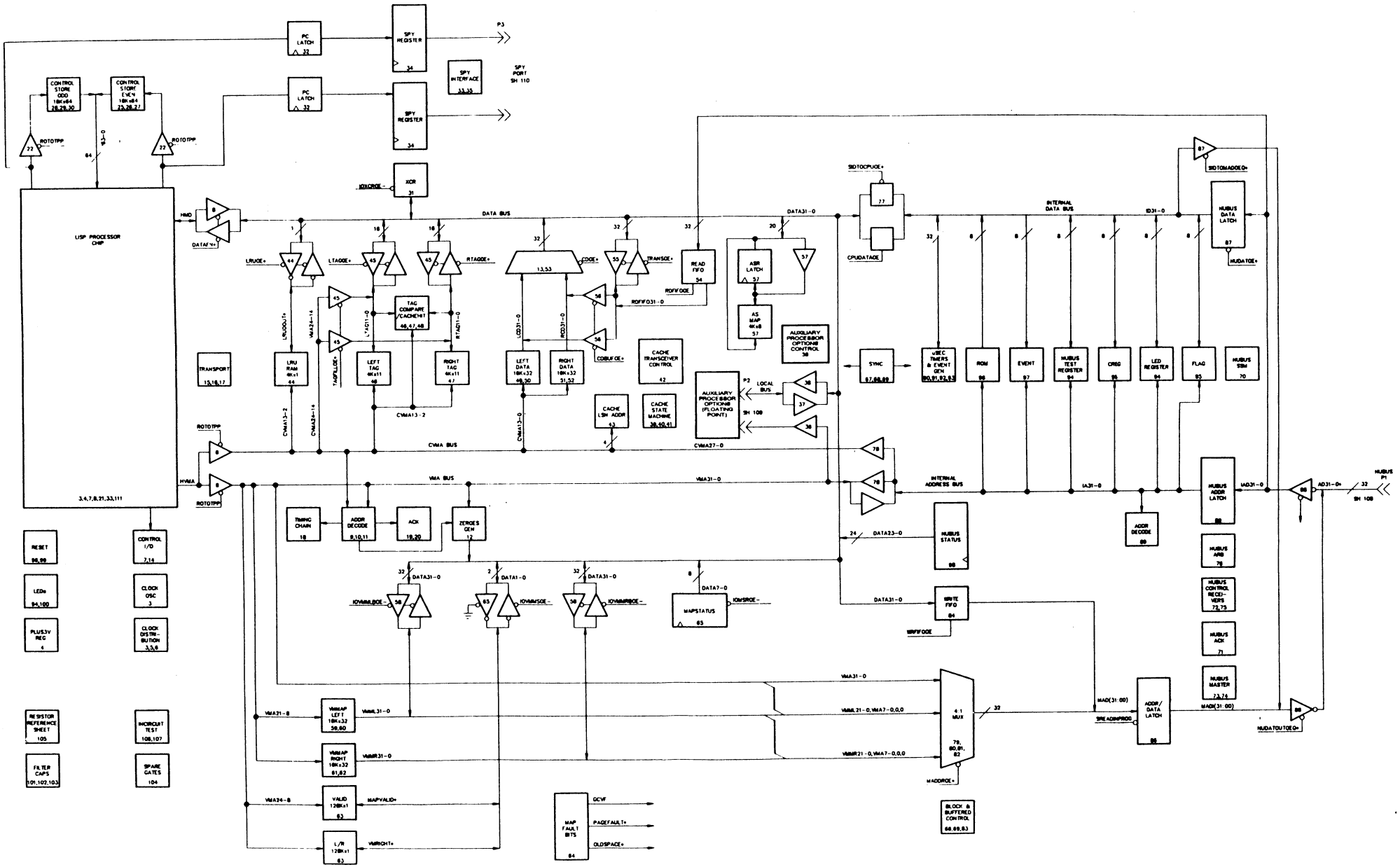


Figure 3-1 Explorer II Processor Board

Figure 3-2 Processor Board Functional Block Diagram



Explorer Lisp Microprocessor Overview

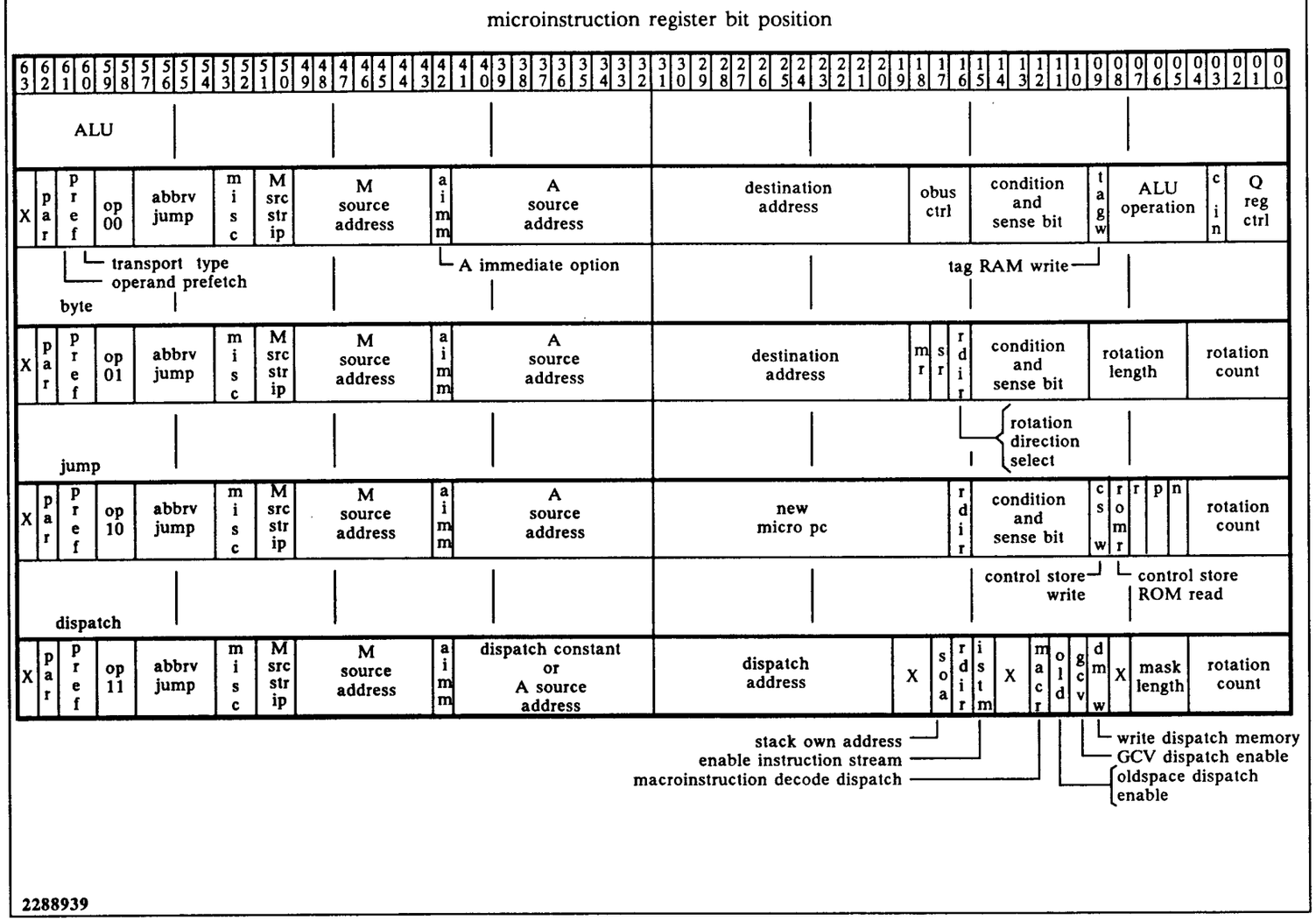
3.2.1 The Lisp microprocessor is a very-large-scale-integration (VLSI) chip that replaces most of the logic on the existing Explorer I processor two-board assembly. A detailed discussion of the Explorer I processor is provided in the existing *Explorer System Field Maintenance* manual.

Many additional features have been added to the Lisp processor chip that are not available on the Explorer I processor. For a detailed discussion of the differences between the Lisp microprocessor and the Explorer I processor, refer to the *Explorer Lisp Microprocessor Specification*. The major added features to the Lisp processor chip are:

- The Lisp microprocessor uses four types of microinstructions (ALU, BYTE, JUMP, and DISPATCH) that are similar to those used in the Explorer I processor. The microinstructions (Figure 3-3) used in the Lisp microprocessor consist of 64 bits as apposed to 56 bits for the Explorer I processor.
- The Lisp microprocessor uses a four-deep microinstruction pipeline that doubles instruction overlap and offers faster throughput than the two-deep pipeline used on the Explorer I processor.
- The Lisp microprocessor interfaces to the processor board over 264 pins.
- The Lisp microprocessor supports the following test strategies:
  - Scan design methodology that allows every nonmemory register on the chip to be read and set after every microinstruction.
  - Read/write access to all on-chip memories for testing.
  - Signature analyzers on the M-bus and O-bus to compress data generated during test micro-subroutines.
  - Control logic for halting and single-stepping the processor clock.
  - A self-test program in the 256-word on-chip control store ROM (IROM).
  - A test loader program in IROM that brings a more extensive self-test program and system loader into control store RAM and enters it.
  - A spy-port interface to support an external software debugging tool.

  For a detailed discussion of the Lisp processor test strategies, refer to the *Explorer Lisp Microprocessor Specification*.
- A number of special programming considerations are discussed in the *Explorer Lisp Microprocessor Specification*. These special programming considerations should be studied before you attempt any microprogramming changes.

Figure 3-3 Explorer Lisp Microinstruction Format



Processor Board Logic Overview

3.2.2 The Explorer II processor logic is built around five interconnecting buses, and four major logic groups called the virtual memory mapper, the cache memory, the microinstruction control store, and the NuBus interface logic. The five buses and four major logic groups are briefly discussed here.

Virtual Memory Address Bus

3.2.2.1 The VMA bus, VMA<31:00>, is a unidirectional 32-bit address bus whose source is the VMA register in the Lisp microprocessor. The VMA bus is connected to the on-board data cache, the virtual memory mapper logic, and through transceivers to the internal address bus.

Data Bus

3.2.2.2 The data bus, DATA<31:00>, is the bidirectional interface to the memory data (MD) register in the Lisp microprocessor. The following logic groups interface to the data bus:

- Internal data bus
- Cache memory logic
- Virtual memory mapper logic
- Automatic transport logic
- External control register
- Zeros generation logic
- Auxiliary processor options logic
- NuBus status register
- Write first-in-first-out (FIFO) memory

Internal Data Bus

3.2.2.3 The internal data bus, ID<31:00>, interfaces to the NuBus through buffer/line drivers and NuBus data latches. Internal data-to-data transceivers form the interface between the data bus and the internal data bus. With the exception of the event and microsecond timers, the same registers and ROMs that interface to the internal data bus also interface to the NuBus. The following registers and ROMs interface to the internal data bus:

- STBM, self-test, and configuration ROM
- Event-posting registers
- Configuration register
- Flag register
- Microsecond timer
- Event-generating timer
- LED register
- NuBus test register

Internal Address Bus

3.2.2.4 The internal address bus, IA<31:00>, is the counterpart to the internal data bus. The internal address bus can be accessed by the NuBus through a buffer/line driver and the NuBus address latch. Internal address-to-VMA transceivers form the interface between the VMA bus and the internal address bus.

Master Address Data Bus

3.2.2.5 The master address data bus, MAD<31:00>, is used by the processor for master write transfers to the NuBus. The mapped or unmapped address is applied to the master address/data bus via an address multiplexer. The write-FIFO memory is the interface between the processor data bus and the master address/data bus. The master address/data bus interfaces to the NuBus through an address/data latch and buffer. As an error-recovery/transfer verification feature, the address and data written to the NuBus is looped back through an interface buffer and stored in the read-FIFO memory. On a master read transfer, data from the NuBus is applied through an interface buffer to the read-FIFO memory (the loopback path on a master write transfer).

Virtual Memory Mapper

3.2.2.6 The memory mapper provides virtual-to-physical address mapping for the processor. Main memory is viewed by the virtual memory system as a 128-megabyte address space that is divided into 128K pages of 1K bytes (256 32-bit words) each. The memory mapper consists of two major blocks of logic: the virtual memory map logic (left and right data, each 16K x 32 RAMs) and the address space (AS) map logic (4K x 8 RAMs).

The storage quantity (or Q) of the virtual memory address bus is applied to the virtual memory map. The Q is divided into three fields: the CDR code, the type field, and the pointer field. The pointer field contains the 25-bit virtual address in the virtual memory space. The virtual address is further divided into a 17-bit virtual page number (VPN) and an 8-bit page offset. The page offset bypasses the map and is not changed.

The VPN is used to index a 128K-by-2-bit, map-entry status RAM. The map-entry status RAM contains a location corresponding to every possible page in the virtual address space. For every page in the virtual address space there are two bits of status stored. The first bit is the valid bit that indicates whether the map contains the virtual-to-physical translation for this page. The second bit is the selector bit that indicates which of the two virtual memory map RAMs (left or right) contains the translation for this page. This second bit has no meaning if the valid bit is not set.

There are two virtual memory map RAMs. Each map entry contains the 22-bit physical address (page frame number) that corresponds to the logical address used to index the virtual memory map RAM. Additionally, the map entry contains the ten map status bits for the addressed page. Five of these status bits are metabits used by the software, two bits are garbage collector volatility (GCV) bits, and two bits are access privilege bits. Since the page frame number is 22 bits wide and the map status bits field is 10 bits wide, each entry in the virtual memory map RAMs is a 32-bit entry.

The virtual memory mapper also contains a block of logic called the address space map. The address space map divides the virtual memory address space into 32-page groups called address space quantums. The address space map logic also contains status bits that apply to the entire address space quantum. The minimum region size is one address space quantum. The address space map is also addressed by the pointer field of the virtual memory address. Since the address space quantum spans 32 pages, only the 12 most significant bits of a Q-pointer value are required to index the address space map RAM. This RAM is eight bits wide and contains three bits of garbage collection volatility status, the old space bit, and four address space metabits. Note that the address space map is connected only to the data bus.

Cache Memory

3.2.2.7 The cache memory is a two-way set-associative cache with 4K blocks of four words each for a total capacity of 128K bytes. The cache is closely coupled to the memory mapper since it relies on map status information in determining if a cache hit has occurred. A cache-option feature on the Explorer II processor board allows the cache to be selectively controlled in specific cases of prefetch cycles, autotransport cycles, instruction fetch cycles, and program data cycles. This cache option feature also allows the total disabling of the cache.

For a memory read, a virtual address is presented to the cache. The cache controller determines if the word is contained in the cache memory and if the map status from the mapper for accessing this word is valid. If so, the word is supplied from the cache memory. If the map status is valid but the cache memory does not contain the required word, the cache controller initiates a four-word block fill for the block containing the word and places the block in the least recently used (LRU) set.

Write operations are similar except that if the word is not contained in the cache memory and the map status is valid, the cache is not updated, and the word is simply written through to main memory. If the cache controller finds the word to be written is already in the cache, the cache data RAM is also updated.

Microinstruction Control Store

3.2.2.8 The microinstruction control store memory is located in two places. A 256-by-64-bit control store loader/self-test ROM is contained within the Lisp microprocessor. 32K-by-64-bit writable control store static RAMs are located on the processor board external to the Lisp microprocessor. The Lisp microprocessor internal control store ROM and the writable control store RAM on the processor board are connected in parallel.

The control store ROM performs a basic self-test and then accesses the self-test ROM on the processor board to load additional self-test and system loader code into the writable control store RAMs. The control store ROM is accessed as a contiguous portion of the control store address space. The control store ROM overlaps the 256 least significant locations of the writable control store RAMs. The control store ROM must therefore be disabled before the 256 least significant locations of the writable control store RAMs can be read. The 256 least significant locations of the writable control store RAMs can be written to with the control store ROM enabled.

The writable control store instructions are implemented at the microinstruction interface of the Lisp microprocessor using two banks of 16K-by-4 static RAM devices (16 devices in each bank) to provide storage for 32K microinstruction words. The writable control store RAMs are organized into two banks to allow the control store memory to be interleaved. The interleaved memory scheme accommodates the slower address access time of the memory devices to the faster instruction rate of the Lisp microprocessor. The microinstruction interface of the Lisp microprocessor consists of a single data bus with two completely separate address and control buses. This allows the interleaving of the banks of memory to cover the odd and even locations in the control store address space.

Configuration ROM Data

3.2.3 The contents of the configuration ROM for the memory board are listed in Table 3-1. For a detailed description of the configuration contents, refer to the *Explorer NuBus System Architecture General Description*.

Table 3-1 Configuration ROM Contents

NuBus Address (Hexadecimal)	Contents	Description
FsFFFFFF—FsFFFFDC	Varies with week, year, and site of manufacture	Serial number
FsFFFFD8—FsFFFFC0	*,FF,FF,FF,FF,FF	Configuration ROM revision level (unblown space for future revisions)
FsFFFFBC—FsFFFFB8	XX,XX	CRC signature
FsFFFFB4	0C	Configuration ROM size (4K bytes)
FsFFFFB0—FsFFFFA4	"TIAU"	Vendor ID
FsFFFFA0—FsFFFF90	00,00,00,05,00	Processor board information
FsFFFF8C—FsFFFF84	"CPU"	Board type
FsFFFF80—FsFFFF44	"00002540830-0001"	Part number
FsFFFF40—FsFFFF38	D0,00,00	Offset to configuration register
FsFFFF34—FsFFFF2C	FF,FF,FF	Offset to device driver (none)
FsFFFF28—FsFFFF20	XX,XX,XX	Offset to diagnostic code

Table 3-1 Configuration ROM Contents (Continued)

NuBus Address (Hexadecimal)	Contents	Description
FsFFFF1C– FsFFFF14	C0,00,00	Offset to flag register
FsFFFF10	27	ROM flags (memory and block moves)
FsFFFF0C	03	Layout byte
FsFFFF08	06	Self-test time (64 seconds)
FsFFFF04	C3	ID byte
FsFFFF00	10	Resource type
FsFFFEFC– FsFFFEF4	FF,FF,FF	NVRAM
FsFFFEF0	00	NVRAM size (none)
FsFFFEEC– FsFFFEE4	E0,00,00	Event registers offset
FsFFFEE0– FsFFFED8	E0,00,08	STBM secondary event offset
FsFFFED4– FsFFFECC	E0,00,04	Restart event offset
FsFFFEC8 FsFFFEAC	FF,FF,FF,FF FF,FF,FF,FF	Sub-board bases (None)
FsFFFEA8– FsFFC000	Additional data included	Interface diagnostics, EPROM checksums, self-test and boot microcode to be loaded into control store

NOTE:

Quotation marks around items in the Contents column indicate the items are in ASCII code.

Interface Description

3.2.4 Tables 3-2 through 3-4 list the interface signals for connectors P1, P2, and P3 on the processor board.

Table 3-2 NuBus Connector P1 Signals

Pin	Row A		Row B		Row C
1	MINUS12V		MINUS12V	(65)	XP1RESET-
2	GND		GND		GND
3	XP1SPV-	(35)	GND		VCC
4	XP1SP- (NC)		VCC		VCC
5	XP1TM1-		VCC		XP1TM0-
6	XP1AD01-		VCC	(70)	XP1AD00-
7	XP1AD03-		VCC		XP1AD02-
8	XP1AD05-	(40)	MINUS5V		XP1AD04-
9	XP1AD07-		MINUS5V		XP1AD06-
10	XP1AD09-		MINUS5V		XP1AD08-
11	XP1AD11-		MINUS5V	(75)	XP1AD10-
12	XP1AD13-		GND		XP1AD12-
13	XP1AD15-	(45)	GND		XP1AD14-
14	XP1AD17-		GND		XP1AD16-
15	XP1AD19-		GND		XP1AD18-
16	XP1AD21-		GND	(80)	XP1AD20-
17	XP1AD23-		GND		XP1AD22-
18	XP1AD25-	(50)	GND		XP1AD24-
19	XP1AD27-		GND		XP1AD26-
20	XP1AD29-		GND		XP1AD28-
21	XP1AD31-		GND	(85)	XP1AD30-
22	GND		GND		GND
23	GND	(55)	GND		XP1PFWP-
24	XP1ARB1-		MINUS5V		XP1ARB0-
25	XP1ARB3-		MINUS5V		XP1ARB2-
26	XP1ID1-		MINUS5V	(90)	XP1ID0-
27	XP1ID3-		MINUS5V		XP1ID2-
28	XP1ACK-	(60)	VCC		XP1START-
29	VCC		VCC		VCC
30	XP1RQST-		GND		VCC
31	GND		GND	(95)	GND
32	PLUS12V		PLUS12V		XP1NUCLK-

NOTES:

1. Connector viewed from the front (connector) side of the backplane.
2. NC indicates no connection.

Table 3-3 Auxiliary Processor Options Connector P2 Signals

Pin	Row A		Row B		Row C
1	XP2ADR00		XP2FPOE- (LTM0-)	(65)	XP2DAT00
2	XP2ADR01		GND		XP2DAT01
3	XP2ADR02	(35)	GND		XP2DAT02
4	XP2ADR03		NC (GND)		XP2DAT03
5	XP2ADR04		VCC		XP2DAT04
6	XP2ADR05		VCC	(70)	XP2DAT05
7	XP2ADR06		VCC		XP2DAT06
8	XP2ADR07	(40)	XP2OPTION3-		XP2DAT07
9	XP2ADR08		XP2MEMREQ-		XP2DAT08
10	XP2ADR09		XP2FPWRT- (LOCK-)		XP2DAT09
11	XP2ADR10		XP2CLK	(75)	XP2DAT10
12	XP2ADR11		GND		XP2DAT11
13	XP2ADR12	(45)	XP2BSO-		XP2DAT12
14	XP2ADR13		XP2MEMACK-		XP2DAT13
15	XP2ADR14		XP2DATOE-		XP2DAT14
16	XP2ADR15		GND	(80)	XP2DAT15
17	XP2ADR16		NC (GND)		XP2DAT16
18	XP2ADR17	(50)	NC (GND)		XP2DAT17
19	XP2ADR18		GND		XP2DAT18
20	XP2ADR19		XP2RESET-		XP2DAT19
21	XP2ADR20		XP2BCLK-	(85)	XP2DAT20
22	XP2ADR21		XP2BERR-		XP2DAT21
23	XP2ADR22	(55)	GND		XP2DAT22
24	XP2ADR23		XP2FAST-		XP2DAT23
25	XP2ADR24		XP2OPTION2-		XP2DAT24
26	XP2ADR25		XP2DECODE-	(90)	XP2DAT25
27	XP2ADR26		XP2OPTION1-		XP2DAT26
28	XP2ADR27	(60)	VCC		XP2DAT27
29	XP2ADR28		NC (GND)		XP2DAT28
30	XP2ADR29		GND		XP2DAT29
31	XP2ADR30		GND	(95)	XP2DAT30
32	XP2ADR31		XP2LTM1-		XP2DAT31

NOTES:

1. Connector viewed from the front (connector) side of the backplane.
2. Signal names within parentheses occur only in slots 3 through 6 of the Explorer I chassis.
3. NC indicates no connection.

Table 3-4 Diagnostic and Testing Connector P3 Signals

Pin	Row A		Row B		Row C
1	XP3LCSE13		NC (GND)	(65)	XP3LCSE14
2	XP3LCSE12		GND		NC
3	XP3LCSE11	(35)	GND		XP3PRA
4	XP3LCSE10		NC (VCC)		NC
5	XP3LCSE09		VCC		XP3BQA
6	XP3LCSE08		VCC	(70)	NC
7	XP3LCSE07		VCC		XP3SPYRESET-
8	XP3LCSE06	(40)	NC (VCC)		XP3TESTMODE-
9	XP3LCSE05		NC (VCC)		XP3OPTION3-
10	XP3LCSE04		NC (VCC)		XP3OPTION2-
11	XP3LCSE03		NC (VCC)	(75)	XP3OPTION1-
12	XP3LCSE02		GND		XP3SSDOUT
13	XP3LCSE01	(45)	NC (GND)		XP3LCSO02
14	XP3LCSO13		NC (GND)		XPELCSO14
15	XP3LCSO12		NC (GND)		XP3LCSO01
16	XP3LCSO11		GND	(80)	NC
17	XP3LCSO10		NC (GND)		XP3SSDIN-
18	XP3LCSO09	(50)	NC (GND)		XP3PSDOUT
19	XP3LCSO08		GND		XP3STEPREQ-
20	XP3LCSO07		NC (GND)		XP3HALT-
21	XP3LCSO06		NC (GND)	(85)	XP3SSCAN-
22	XP3LCSO05		NC (VCC)		XP3PSCAN-
23	XP3LCSO04	(55)	GND		XP3PSLDEN-
24	XP3LCSO03		NC (VCC)		XP3PSADV-
25	NC		NC (VCC)		XP3PSDIN
26	NC		NC (VCC)	(90)	NC
27	NC		NC (VCC)		NC
28	XP3PRB	(60)	VCC		XP3BQB
29	XP3PFA		NC (VCC)		XP3BCSOA
30	XP3PFB		GND		XP3BCSOB
31	XP3PEA		GND	(95)	XP3BCSEA
32	XP3PEB		XP3TEMP- (VCC)		XP3BCSEB

NOTES:

1. Connector viewed from the front (connector) side of the backplane.
2. Signal names within parentheses occur only in slot 6 of the Explorer I chassis.
3. NC indicates no connection.

Auxiliary Processor Options Description

3.3 The logic on the Explorer II processor board is arranged to operate with different auxiliary processor option boards with only software changes. Descriptions of each option board will be provided under this heading as the option boards become available.

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