A LARGE SCALE COMPUTER TERMINAL OUTPUT CONTROLLER

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TABLE OF CONTENTS

I. INTRODUCTION

The purpose of this paper is to describe the design and implementation of a large scale computer terminal output controller which supervises the transfer of information from a Control Data 6400 Computer (1) to a PLATO IV (2) data network.

PLATO IV is a computer-assisted instruction system. In this system up to 4000 remote computer terminals (3), each requiring a nominal 1200 bps channel are connected to a centrally located computer. A block diagram is shown in Figure 1.

Voice grade telephone lines could serve as the 1200 bps communication channels. The intra-state tariffs for leasing such voice grade lines range from 50¢/mile/month for TELEPAK D service (240 channels) to about $4.50/mile/month for a single line. On the other hand, the tariffs for an inter-city educational television channel range from $55/mile/month downward with the number of channels leased. Using such a channel more than 1000 terminals could be provided with 1200 bps service at a per terminal charge of less than 5.5¢/mile/month. (4)

The format of the signals coming out of the Digital Television Transmitter (DTX) must conform to the requirements of the standard (FCC accepted) 525 line raster scan system. The format of the data portion of the video signal is shown in Figure 2. This data word configuration holds two major advantages over other possible data formats.

1) Since error bursts in the received digital television signal have
      a high probability of lasting for less than 1008 bit times, the

PLATO IV Terminals
(1008 maximum)

Figure 1
PLATO IV

$T_0{}^{O}$ $T_1{}^{O}$ $T_2{}^{O}$ ------------------------------------ $T_{83}{}^{O}$

$T_{84}{}^{O}$ $T_{167}{}^{O}$

12 TV lines

Bit 0 for all terminals

$T_{924}{}^{O}$ $T_{1007}{}^{O}$

12 lines

12 lines

Bit 1
Bit 2

Bit 19
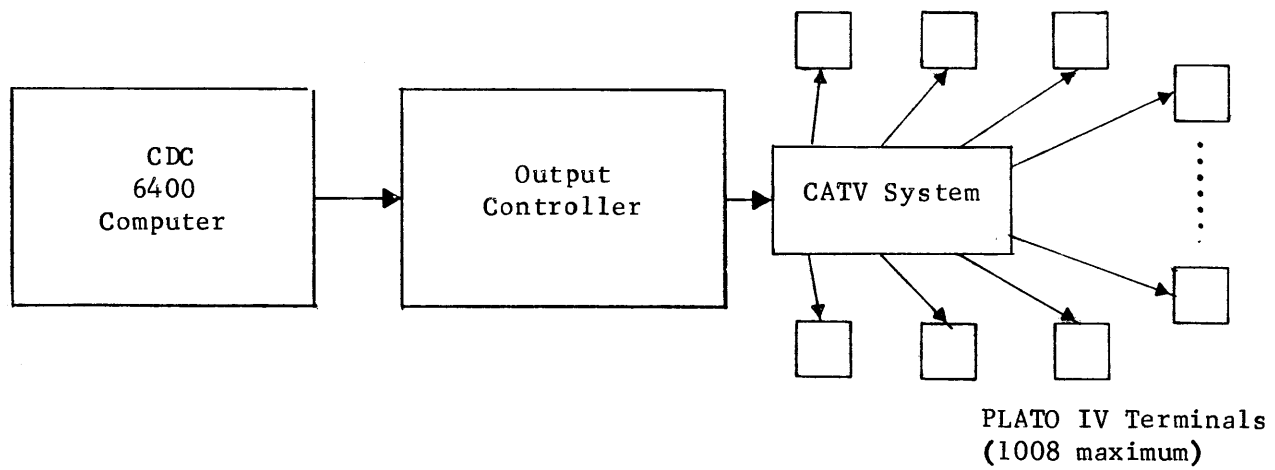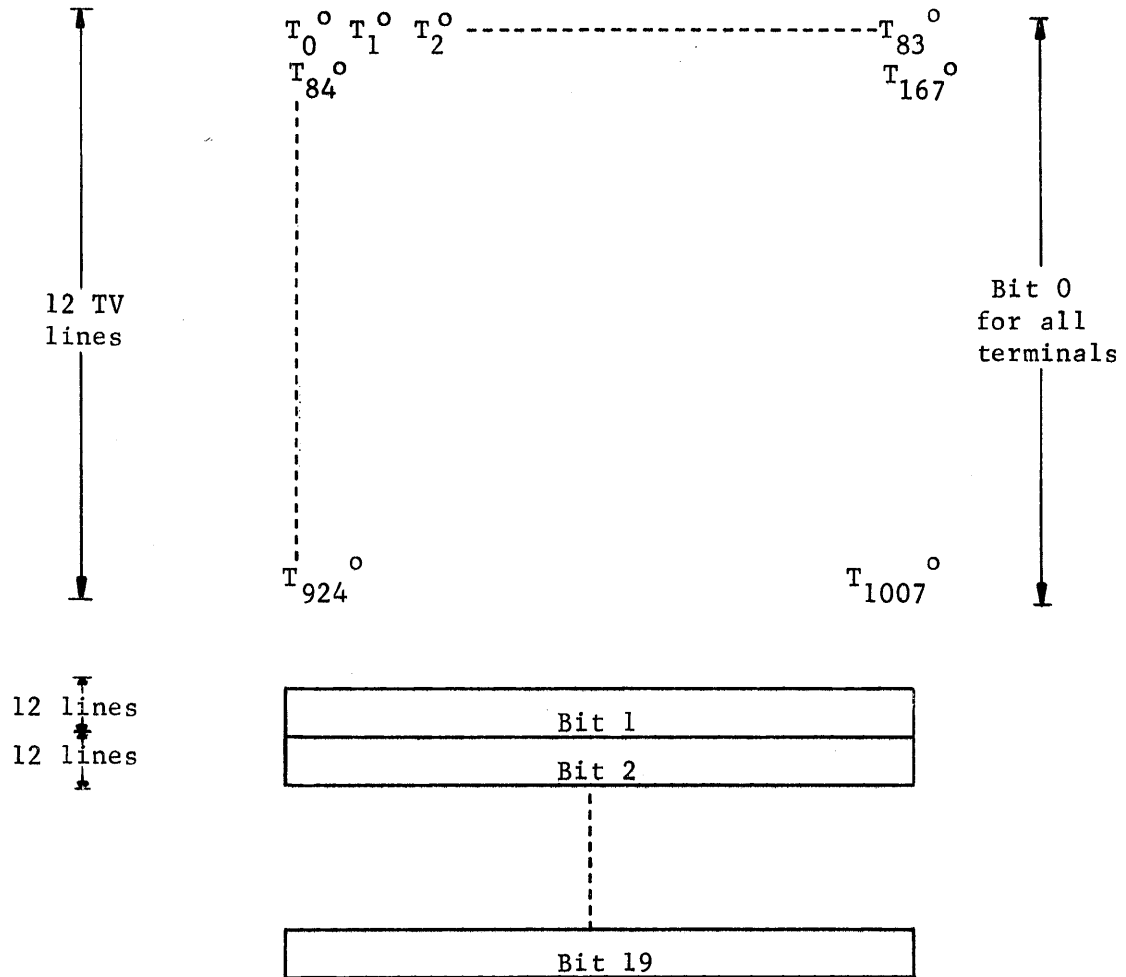
Figure 2
Format of PLATO Data in TV Frame

resulting probability that an error burst could cause two bits of a terminal data word to be erroneous and consequently, not be detected by the parity check is very small.

2) Since the actual terminal data rate is very close to the effective terminal data rate, it is not necessary to store complete 20 bit data words in the Digital Television Receiver in preparation for the conversion to 1200 bps data transmission. The actual terminal data rate in the DTX is one bit per 12 television lines or 21 bits (20 data plus start bit) in 252 television line. This data rate is 1313 bps. The telephone data rate is 1260 bps (21 bits in 1/60 second) and is also the effective terminal data rate.

The bit interval in the Digital Television Transmitter is 635 nanoseconds or 1.575 mbps. Since some of the video field is used for sync and timing information, the effective data rate is 1.2064 mbps.

II. OUTPUT CONTROLLER

The function of the Output Controller is to provide the necessary inter-facing between the computer and the CATV network. This operation consists of storing information as it is sent out from the computer and then outputting that information to the CATV network at the proper time. A complete field of information must be stored prior to the output operation. Since data must be output on every video field, two memories must be used so that one may be loaded with new data while the other is being read and data outputted.

The computer used to control the 1008 terminals through the PLATO IV data network is a Control Data 6400. (1) This computer consists of one central processing unit surrounded by 10 peripherial processing units (PPU) which are used to perform the primary input-output functions. The PPU word size is 12 bits. Each PPU has a maximum data transfer rate of 1 mega-word per second.

A block diagram of the Output Controller is shown in Figure 3. The main sections are: 1) The 6400 I/O Control; 2) A dual 20K bit Metal Oxide Semiconductor (MOS) random access memory; and 3) The DTX I/O Control.

The 6400 I/O Control provides the necessary timing the control circuitry to synchronize data transfer from the 6400 PPU to the Output Controller. In the 6400 I/O Control, the data from the 6400 PPU is prepared for entry into the memory and parity information is generated.

The DTX I/O control interprets the control-timing signals from the DTX and provides the read control necessary to transfer the contents of the memory being read out to the CATV system.
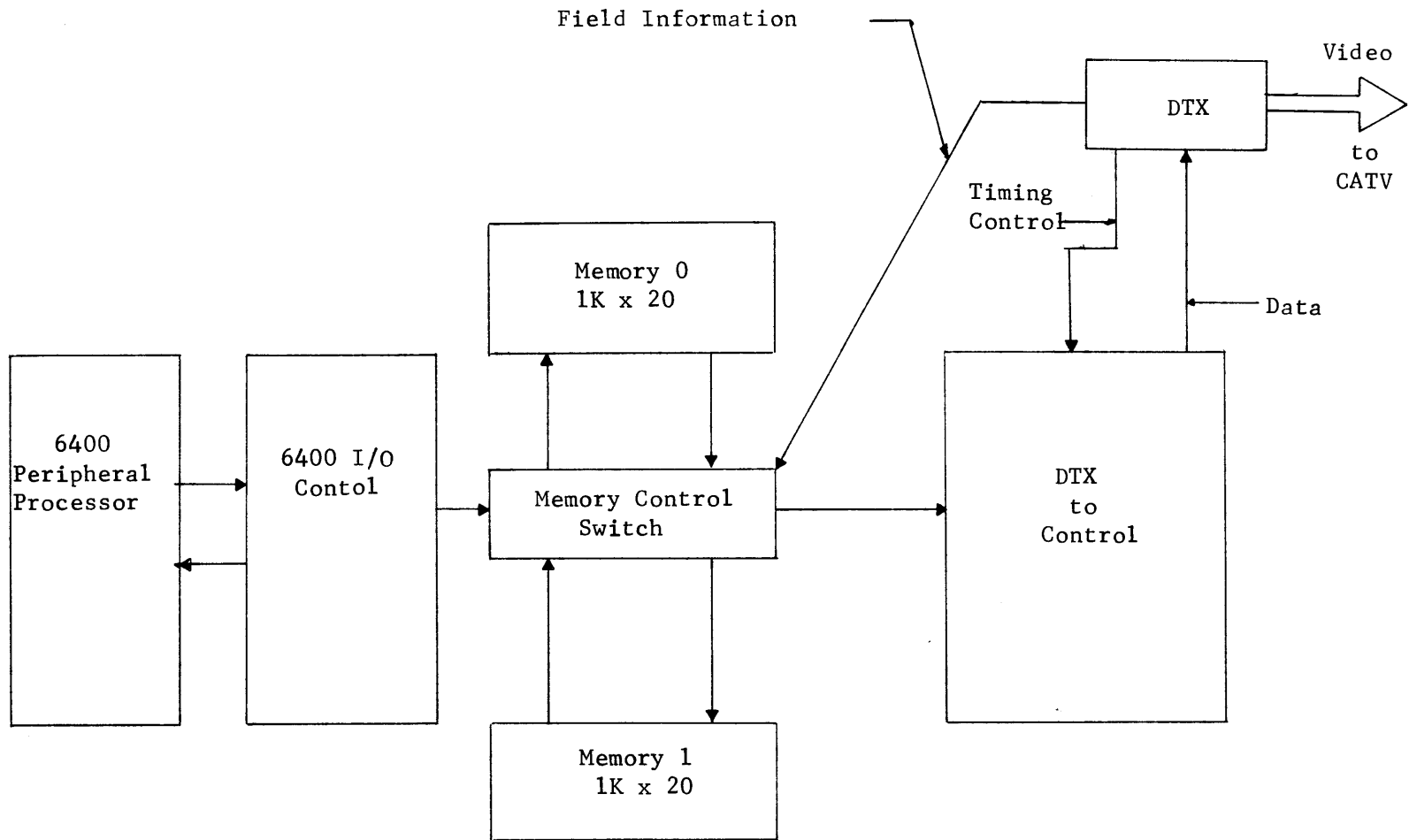
Figure 3
Output Controller

III. DESCRIPTION OF OPERATION

Three PPU words are required to specify a PLATO IV terminal word. In this word triplet, ten bits are used to specify the terminal address, twenty bits are used as terminal data and six bits as control information. The format of this word triplet is shown in Figure 4.

Bit 00   Parity Bit. This bit position is filled by the Output Controller with parity information. Even parity is used for the data portion of the word.

Bits 01-19   Terminal Data

Bits 20-29   Address of terminal for which data is intended.

Bits 10-11 of the three 12 bit words are used as control indications by the Output Controller. They are interpreted as follows:

Bit 11, word 1   This bit, when set to "1", indicates the start of a word triplet.

Bit 10, word 3   This bit, when set to "1", indicates that this word is the address of the last terminal to receive data during the present 1/60 of a second.
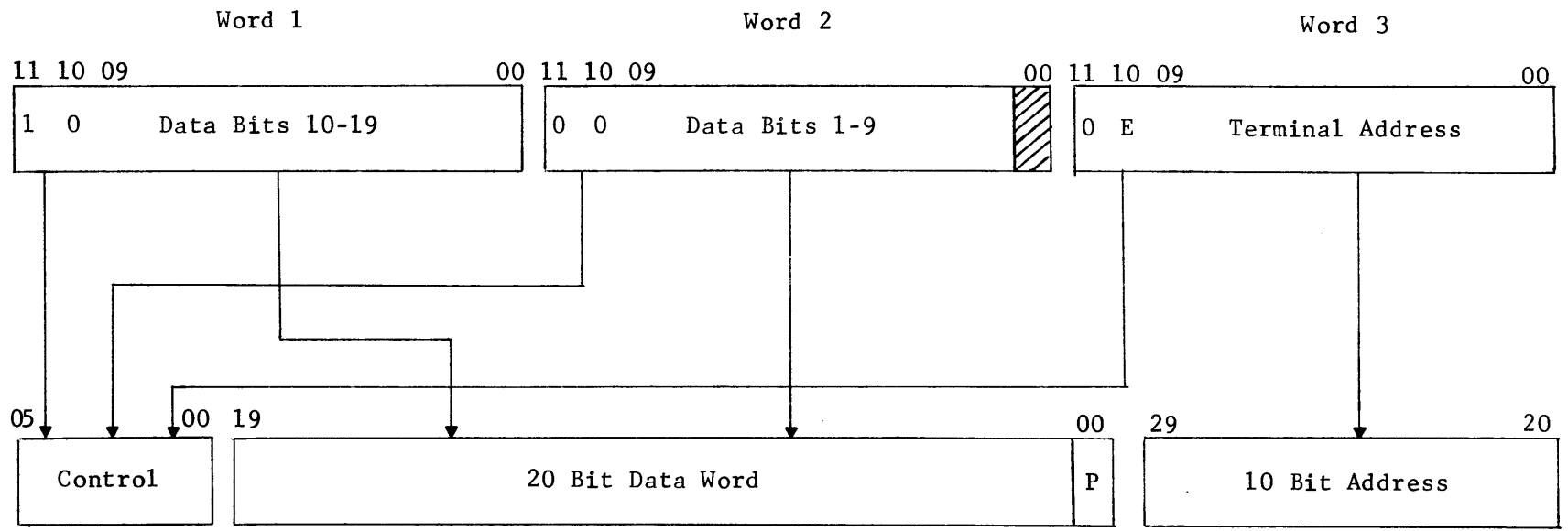
Figure 4
Output Word Format

After a complete word triplet has been received by the Output Controller, the terminal data is loaded into memory at the location specified by the terminal address. In the next video field the entire memory is then read and output. Figure 5 is a flow diagram of the operations necessary to transfer a data word through the Output Controller.

Dynamic, random access, MOS memories were used as the memory module in the Output Controller. It is necessary to arrange the memory in such a manner that successive data bits to be output are not stored in the same package. This is due to the fact that 1) the dynamic memories are organized as 1024 x 1, i.e., 1024 one-bit words per package; 2) only one bit can be read from a chip at a time; 3) the read/write cycle is 600 nanoseconds minimum; and 4) data must be read from successive terminal locations at 635 nanosecond intervals. Otherwise, the necessary cycle time would be 635 nanoseconds which is very close to the minimum.

Figure 6 illustrates the final memory organization adopted. A single bit of all 1008 terminal locations is stored on one card, in one quarter of each of the four packages on that card. Four bits total are stored on a single card. Bits 0-3 of all terminals are stored on card 0, bits 4-7 are stored on card 1, etc. Eight of the terminal address bits (the eight most significant) are used to determine the position within the quadrant that the data is stored. The two least significant address bits are decoded into four lines and used to select the package within the card to be written. Data intended for student $27_{10}(0000011011_2)$ is stored in package P_D on all cards $(11_b=D)$ at location $6_{10}(100000110_2)$ within all quadrants.

```
┌─────────────────┐
│   Generate      │◄──────────────────────────────────┐
│  Word Triplet   │                                    │
└─────────────────┘                                    │
         │                                             │
         ▼                                             │
┌─────────────────┐                                    │
│    Output       │                                    │
│  Word Triplet   │                                    │
└─────────────────┘                                    │
         │                                             │
         ▼                                             │
┌─────────────────┐                                    │
│   Generate      │                                    │
│    Parity       │                                    │
└─────────────────┘                                    │
         │              ┌──────┐                       │
         ◄──────────────│ wait │◄──────┐               │
         ▼              └──────┘        │               │
┌─────────────────┐                    │               │
│    Memory       │──── yes ───────────┘               │
│    Busy?        │                                    │
└─────────────────┘                                    │
         │                                             │
        no                                             │
         ▼                                             │
┌─────────────────┐                                    │
│     Load        │                                    │
│    Memory       │                                    │
└─────────────────┘                                    │
┌─────────────────┐      ┌──────────┐      ┌──────────────┐
│     Field       │─yes─►│  Change  │─────►│    Read      │◄──┐
│    Change       │      │  Fields  │      │   Memory     │   │
└─────────────────┘      └──────────┘      └──────────────┘   │
         │                                        │           │
         │                                        ▼           │
         │                                 ┌──────────────┐  no
         └────────────────────────────────►│    Change    │───┘
                                           │    Field     │
                                           └──────────────┘
                                                  │
                                                 yes
                                                  ▼
                                           ┌──────────────┐
                                           │   Change     │
                                           │   Fields     │
                                           └──────────────┘
```

Figure 5
Read/Write Block Diagram

1024 x 1 Section

P
D C B A D C B A D C B A D C B A D C B A

q_D

q_C

q_B

q_A

8 Memory Address
lines (to all ckts)

Card 4   Card 3   Card 2   Card 1   Card 0

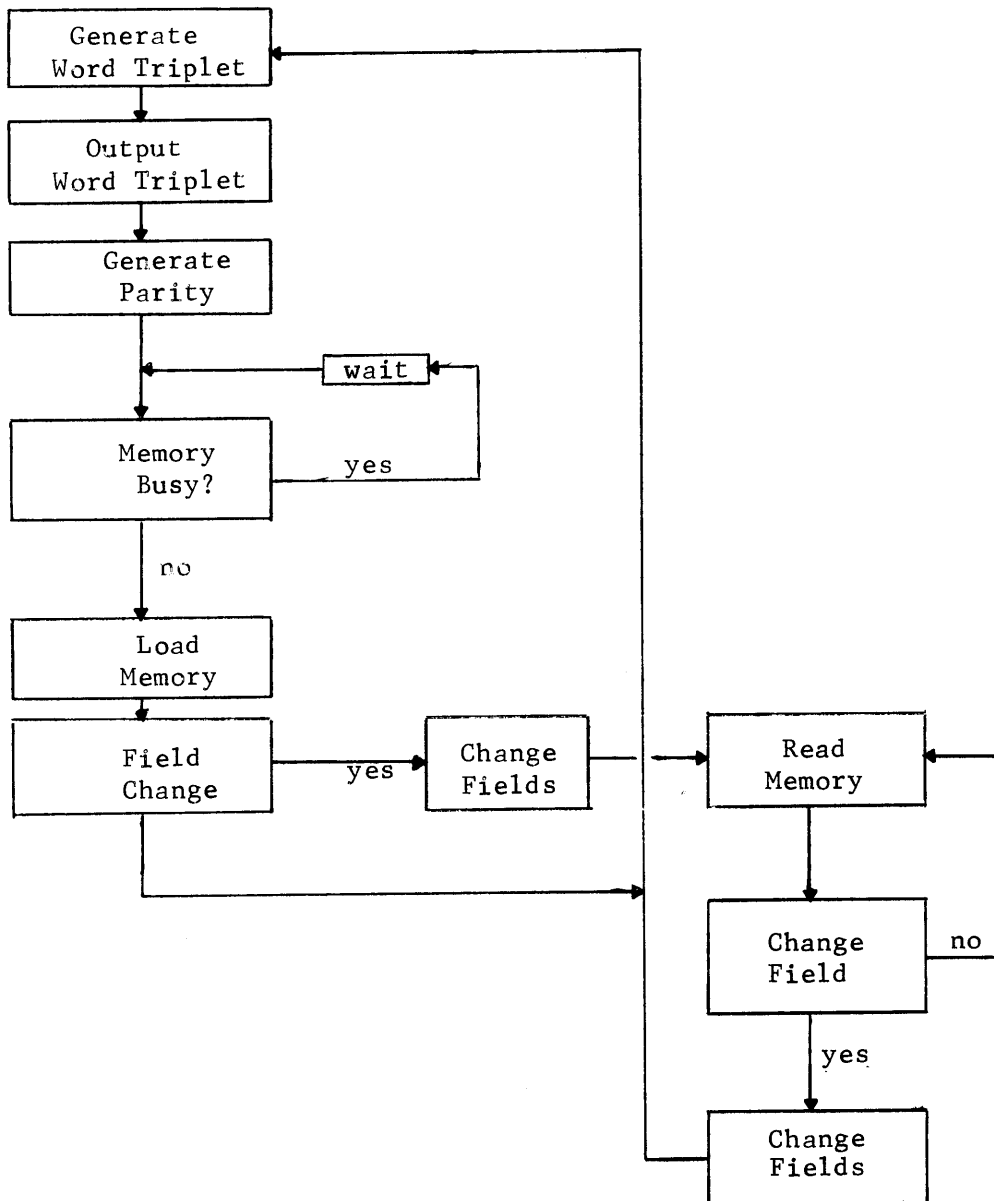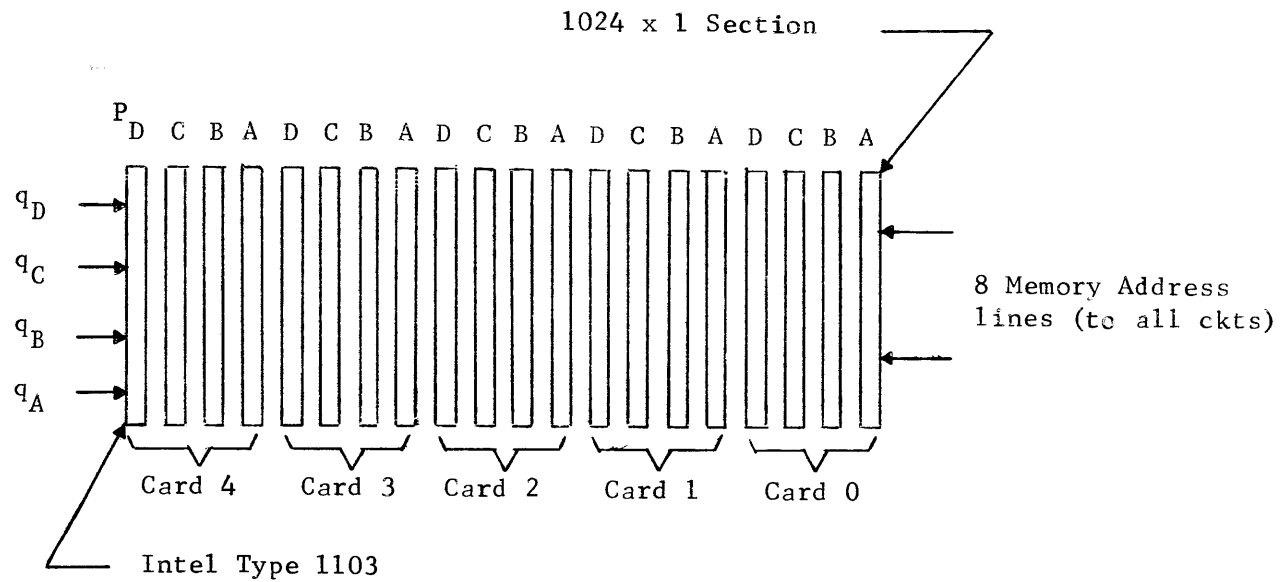Intel Type 1103

Figure 6
Output Controller Memory Organization

Figure 7 is a flow diagram of the sequence of operations used to load data into the memory. Because of the careful positioning of data in the memory when it is written, the unloading may be done in a simple sequential order. Data can be read from four locations simultaneously, thus allowing a 2.6 μsec read cycle time, and avoiding any speed problems. Figure 8 is a flow chart of the read sequence. The address register determines the position within quadrants that is read and the bit group determines both card and quadrant being read. Each time four bits are read from memory they are loaded in a shift register and clocked serially to the CATV system. A logical zero is written in every memory location as it is read in order to generate a NOP (no-operation - a data word, which is ignored by all terminals, consisting of all zero's) for every terminal which the computer does not address in the next field.
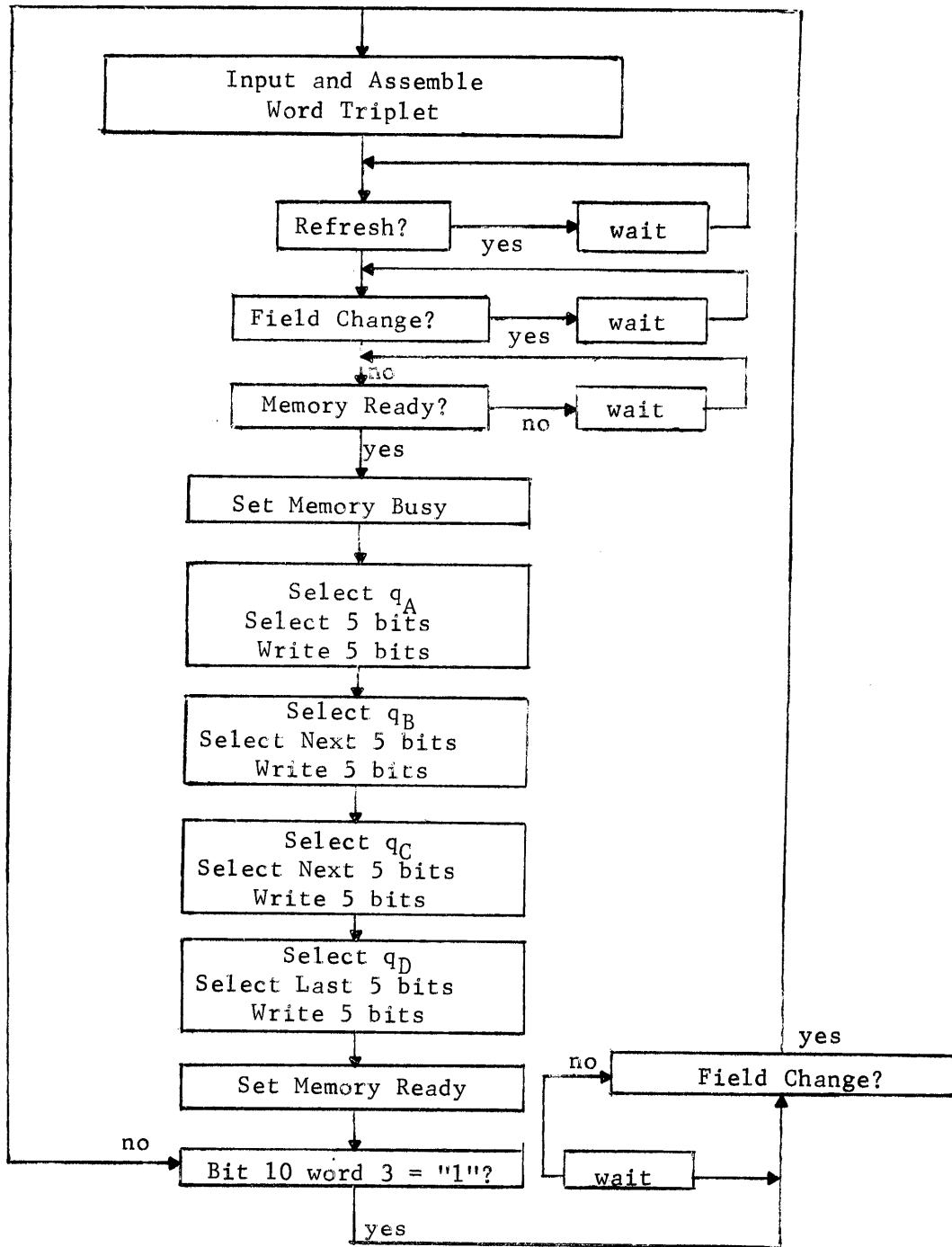
```
┌──────────────────────────────────────────────────────────────────────────┐
│                    ↓                                                       │
│           ┌─────────────────────┐                                         │
│           │  Input and Assemble │                                         │
│           │    Word Triplet     │                                         │
│           └─────────────────────┘                                         │
│                    ↓                          ┌──────────┐                 │
│              ┌──────────┐        yes          │          │                 │
│              │ Refresh? │─────────────────────│   wait   │─────┐           │
│              └──────────┘                     └──────────┘     │           │
│                    ↓                                            │          │
│            ┌───────────────┐      yes          ┌──────────┐    │          │
│            │ Field Change? │───────────────────│   wait   │────┘          │
│            └───────────────┘                   └──────────┘               │
│                    ↓ no                                                    │
│            ┌───────────────┐       no          ┌──────────┐               │
│            │ Memory Ready? │───────────────────│   wait   │               │
│            └───────────────┘                   └──────────┘               │
│                    ↓ yes                                                   │
│           ┌─────────────────┐                                             │
│           │ Set Memory Busy │                                             │
│           └─────────────────┘                                             │
```

Input and Assemble Word Triplet

Refresh? — yes → wait

Field Change? — yes → wait

no

Memory Ready? — no → wait

yes

Set Memory Busy

Select q_A
Select 5 bits
Write 5 bits

Select q_B
Select Next 5 bits
Write 5 bits

Select q_C
Select Next 5 bits
Write 5 bits

Select q_D
Select Last 5 bits
Write 5 bits

Set Memory Ready

no

Bit 10 word 3 = "1"?

yes

Field Change? — no → wait

yes

Figure 7
Load Cycle

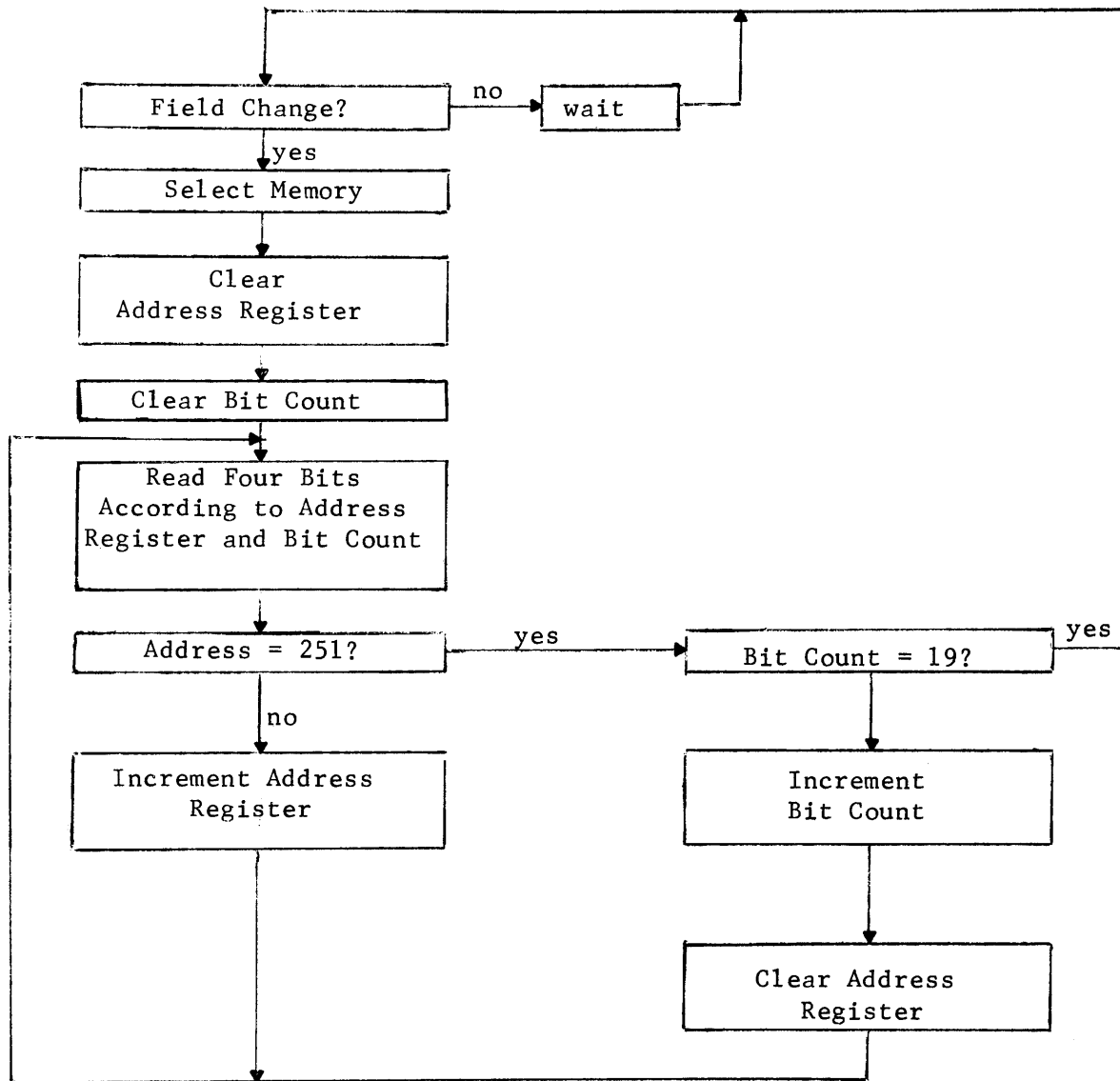Figure 8
Read Sequence

IV. DESIGN CONSIDERATIONS

Dynamic memories were chosen for the Output Controller because of power, size, cost and speed considerations.

Dynamic memories hold a considerable power saving advantage over static memories because the data is charge stored in capacitors in a dynamic memory and consumes no stand-by current. In a static memory, data is stored in an active device flip-flop and consumes continuous current. A 40K bit dynamic memory under full continuous access will dissipate 2.94 watts in the memory and 3 watts in the associated drive circuitry. A static memory, however, under the same conditions would require from 60 to 140 watts in the memory section and 3 watts in the drive circuitry. A 20:1 memory power saving is realized by using dynamic memories.

Dynamic memories are packaged as 1024 bits per package and static memories are 256 bits per package. When dynamic memories were used in the Output Controller, 40 packages were needed to build the memory. Four packages per card is the practical limit and results in a 10 card memory system. Had static memories been chosen, 160 packages and 40 cards would have been needed.

The cost of the dynamic memories priced per bit is approximately 20% lower than static memories. This fact added to the power supply cost savings and printed circuit board cost savings could result in as much as a 35% savings in total memory cost.

The minimum guaranteed cycle times for the dynamic memories is 600 nanoseconds. This rating makes the 1.3 μsec write cycle time used when loading memory comfortably longer than the minimum. The static memories

on the market have a typical cycle time of 1.0 μsec. to 1.4 μsec., depending on circuit type. These rated speeds would come dangerously close to the cycle time used and would require a slow-down of the system.

Intel type 1103 (5) dynamic memories were chosen to be used in the Output Controller.

V. SUMMARY

The Output Controller has been built and installed in the PLATO IV Network Interface.(7) A 6400 simulator was built and used to check out and test the system. The controller has been successfully debugged and is in operation.

The digital transmission system has also been tested. Approximately 80 hours of testing have been conducted. A 180-mile loop facility employing three methods of video transmission was used. Data was recorded using an input signal level of 0 dbmv. An alternating "1"'s and "0"'s pattern was used. Figure 9 is a list of the results of that test. (4)

The Output Controller requires a total volume of 180 cubic inches, and consumes approximately 20 watts and has a total component cost of $2500.

The Output Controller was designed to specifically meet the requirements of the PLATO IV system. However, the controller can easily be adapted to any large-scale computer terminal system.

Total Run Time	78.35 hours
Total Number of Error Bursts	85
Average Time Between Bursts	.92 hours
Shortest Observed Burst	1 bit
Longest Observed Burst	264,009 bits
Average Burst Length[†]	1998 bits
Percent of Bursts Less Than 1008 Bits	88.2%
Bits Transmitted Per Bit in Error[‡]	2.08×10^6

[†]The three longest bursts are excluded from this figure. Including these bursts the average burst length was 10,732 bits.

[‡]The three longest bursts were excluded from this figure. If included, this number becomes 3.74×10^5 bits transmitted per bit in error.

Figure 9
Test Results

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6. J. Stifle, "The PLATO IV Architecture," CERL Report X-20, April, 1971.