UNIVAC

First in real-time Computer systems.

SPERRY RAND

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Printed in U.S.A.

UNIVAC 1110 system

pacesetters of the industry

facts & figures

SPERRY RAND

1110 Facts and Figures

The UNIVAC® 1110 system. Most powerful member of the UNIVAC 1100 series of real-time computers. UNIVAC 1110 systems enable users to move into a system that not only meets many immediate real-time requirements, but also allows for extensive expansion flexibility in any direction. Quickly and economically.

The minimum UNIVAC 1110 configuration . . . minimum only when it's compared to its expansion possibilities . . . is referred to as a "2 x 1" system. This means that the foundation processing section includes two Command/Arithmetic Units (CAU) and one Input/Output Access Unit. And being modular, UNIVAC 1110 systems provide easy expansion with more CAU's, IOAU'S, storage and peripherals. UNIVAC 1110 systems possess tremendous throughput capabilities. They're ideal as a central system for management information, as a medical information system or a scientific and educational tool.

UNIVAC 1110 systems offer the ability to configure for partial or full system back-up. This built-in redundancy feature is your key to a fail-safe operation. Industry will discover that the UNIVAC 1110 system is one of the most profitable investments around.

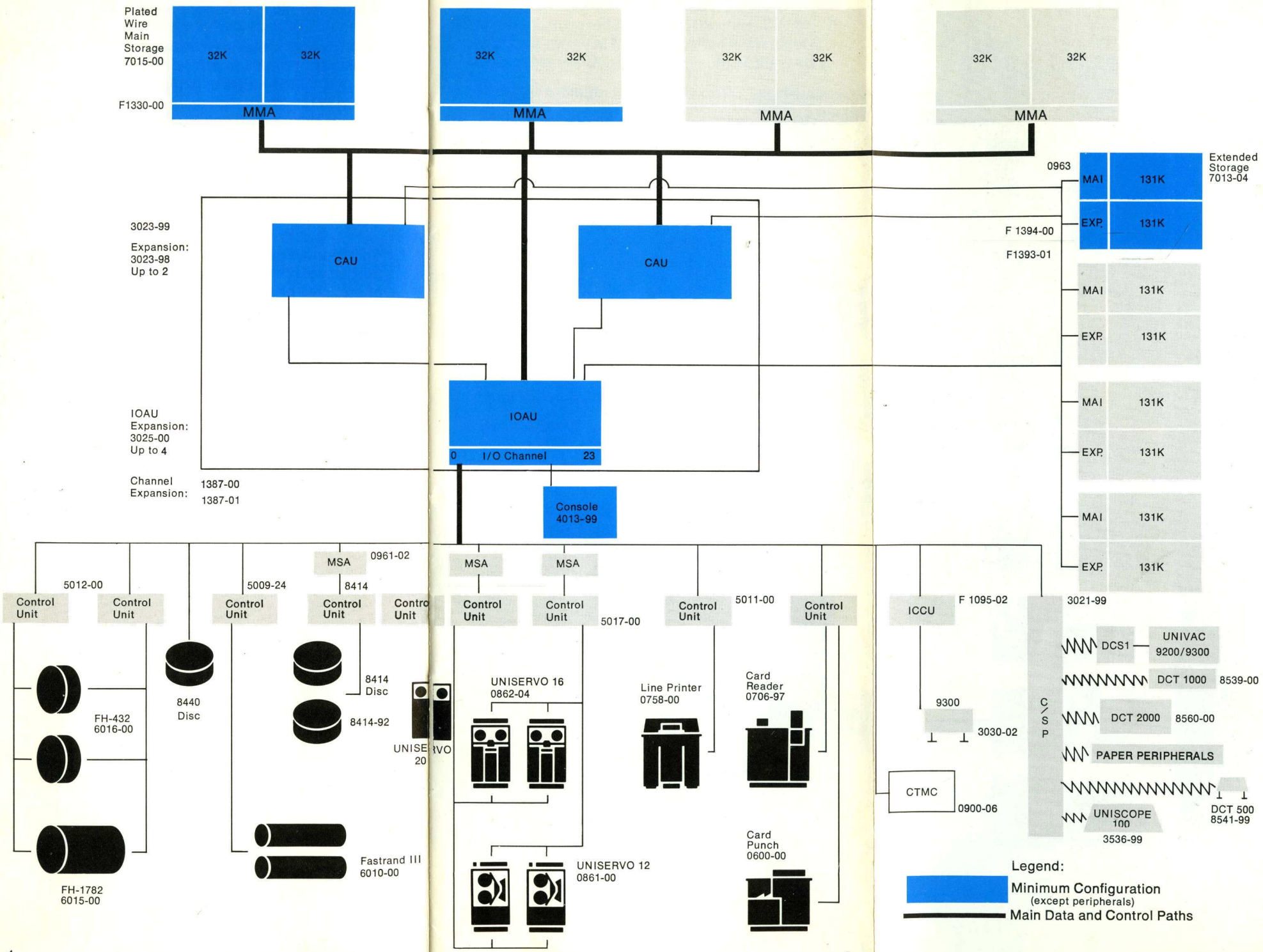
UNIVAC 1110
Modularity with investment protection

UNIVAC 1110 systems provide users with important investment protection in hardware and software. UNIVAC 1110 systems can use most of the standard UNIVAC 1100 series hardware and *all* existing software and peripherals.

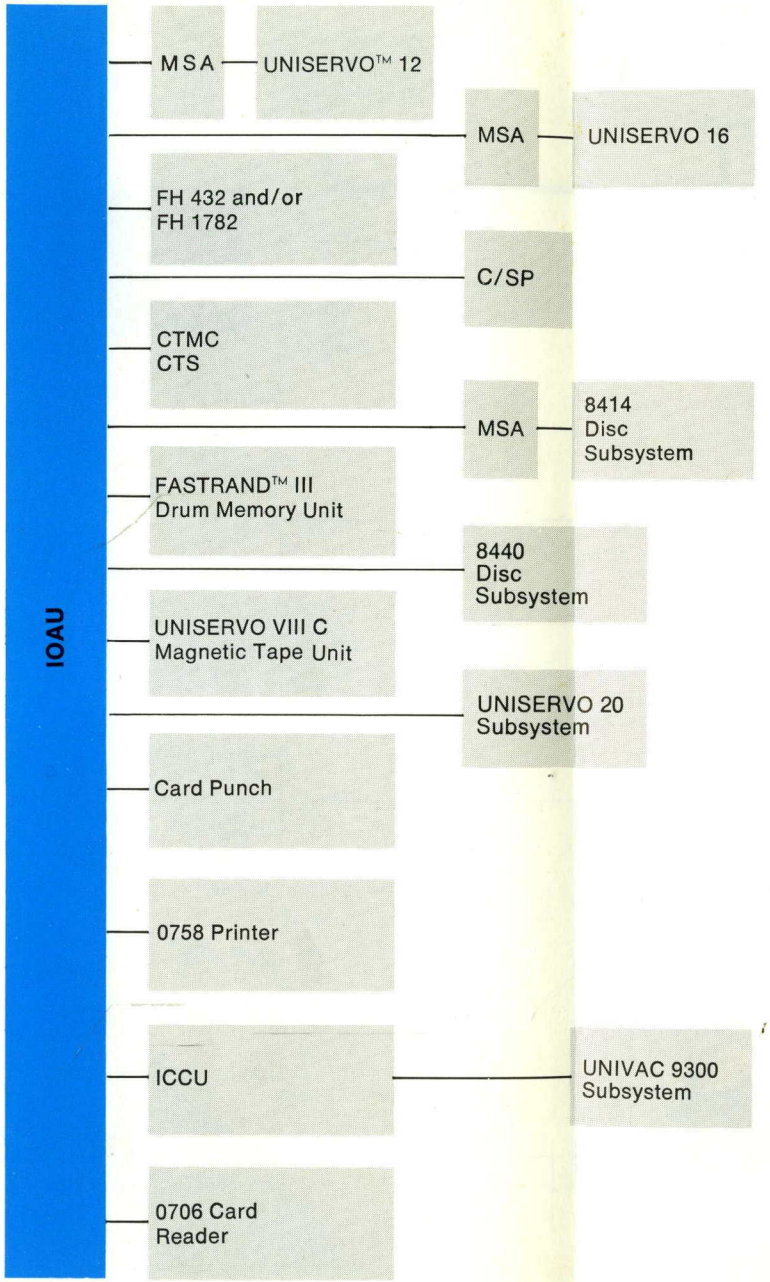
For example, move from the UNIVAC 1108 system . . . upwards . . . to the UNIVAC 1110 system. You just change processors and main storage. There's no change in user software.

An important advantage . . . investment protection felt throughout your entire data processing operation. The kind of security only Univac offers . . . and delivers.

UNIVAC 1110 Processor and Main Storage Configurator



I/O Devices



Processor

The basic UNIVAC 1110 processor consists of three functionally independent units. Two of these are identical CAU's; the third is the Input/Output Access Unit which is shared by the CAU's.

The CAU's control functionally distinct sections.

Address Formation Sections—Accepts the 24-bit absolute address, form the proper request, increments the address, asks for the next request, and generates the operand.

General Register Stack—Consists of 112 arithmetic holding and indexing registers which provide 75 nanosecond internal storage for accumulator storage, indexing, and other special purposes.

Condition Jump Operations—Assures that jumps decisions are made without any arithmetic delay.

Arithmetic Section—Handles shifting through a one cycle matrix as well as all fixed and floating point arithmetic.

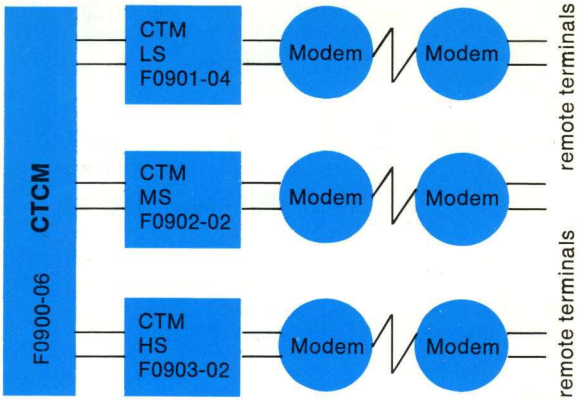
Control Section—Links the operations being performed by the other four sections.

UNIVAC 1110 Local Peripheral Facts

Auxiliary Storage		
FH 432 Drum**	Average Access	4.25 msec.
	Capacity	262,144 words or 1,572,864 Ch.
	Transfer rate	240,000 words or 1,440,000 Ch/Sec.
	Max. Per Subsystem	8
	I/O Channel*	1
FH 1782 Drum**	Average Access	17.0 msec.
	Capacity	2,097,152 words or 12,582,912 Ch.
	Transfer rate	240,000 words or 1,440,000 Ch/Sec.
	Max./Subsystem	8
	I/O Channel*	1
FASTRAND III	Average Access	92 msec.
	Capacity	33,030,144 words or 198,180,864 Ch.
	Transfer rate	39,424 words or 230,400 Ch/Sec.
	Max./Subsystem	8
	I/O Channel*	1
Disc Subsystems		
8414 Disc	Average Access	60 msec.
	Capacity	5.0 million
	Transfer rate	69,333 Wds./Sec.
	Max. Per Subsystem	8
	I/O Channel*	1
8440 Disc	Average Access	35 ms.
	Capacity	114 million Ch.
	I/O Channel*	1
	Transfer rate	138,888 Wds./Sec.
	Subsystem	1-8 drives
Magnetic Tape Subsystems		
UNISERVO VIII C	Transfer rate	32,000 to 120,000 Ch/Sec.
	Recording density	200/556/800 BPI
	Tracks	7 or 9
	Max./Subsystem	16
	I/O Channel	1
UNISERVO 12	Transfer rate	68,320 or 34,160 frames/sec.
	Recording density	Variable (dual)
	Tracks	7 or 9
	Max./Subsystem	16
	I/O Channel*	1
UNISERVO 16	Transfer rate	192,000 or 96,000 frames/Sec.
	Recording density	Variable (dual)
	Tracks	7 or 9
	Max./Subsystem	16
	I/O Channel*	1
UNISERVO 20	Transfer Rate	320,000 frames/sec.
	Recording Density	1600 PPI
	Tracks	9 Track
	Maximum/ Subsystem	16
	I/O Channels*	1
Printer Subsystem (0758)	Print Speed	1200/1600 LPM
	Ch/Line	132
	Ch. Printed	43/63
	Horiz. Spacing	10 Ch/Inch
	Vert. Spacing	6 and 8 Lines/Inch
	I/O Channel	1
Card Subsystem	Card Read	900 CPM
	Card Punch	300 CPM
	I/O Channel	1
UNIVAC 9000 Subsystems	Card Read	600 CPM
	Card Punch	75-200 or 200
	Print Speed	600/1200 LPM
	I/O Channel	1

*Can provide simultaneous dual access using 2 channels.
**May be mixed.
Transfer rates stated apply to 9 track series.

CTMC Configurator



Communications Terminal Module Controller (CTMC)

The function of the UNIVAC Communications Terminal Module Controller (CTMC) is to transmit data between the CTM's and the Central Processor. A CTMC may be connected to any processor I/O Channel, multiplexing up to 16 CTM's to that channel.

Communications Terminal Module (CTM)

The function of the CTM is to provide: (1) a logical and electrical interface, (2) buffering, (3) control circuitry for termination of the communication lines at the CTMC. Each CTM provides termination for a specific number of lines dependent upon the speed of the line and the line control capability required by the user. Lines may operate in simplex, half duplex or full duplex mode.

CTM Low Speed

Line Speed	To 300 BPS
Transmission	Asynchronous 5, 6, 7, 8 level
Lines Terminated	2 In/2 Out

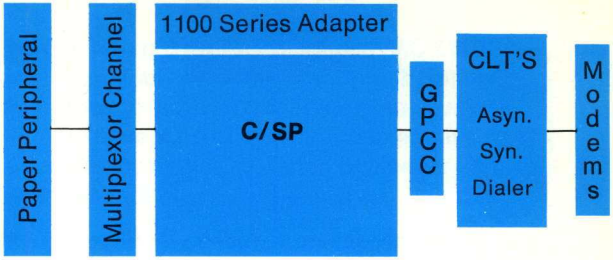
CTM Medium Speed

Line Speed	To 1600 BPS
Transmission	Asynchronous 5, 6, 7, 8 level
Lines Terminated	2 In/2 Out

CTM High Speed

Line Speed	To 4800 BPS
Transmission	Synchronous 5, 6, 7, 8 level
Lines Terminated	2 In/2 Out

Communications/Symbiont Processor (C/SP)



The UNIVAC Communications/Symbiont Processor (C/SP) is a high performance internally programmed communications concentrator/multiplexor and/or a symbiont processor. It provides control for a variety of high and low speed communication lines along with paper peripheral subsystems while interfacing with a general purpose computer.

The C/SP unburdens the processor of the necessity of handling communications and symbiont activity as well as reducing valuable storage requirements.

Asynchronous Communications Line Terminal

Line Speed	45-2400 BPS
Facilities	Pvt. Telegraph, TWX, Telex, Voice Band
Interfaces	EIA RS232C, CCITT, MIL. STD. 188B
Mode	Start-Stop

Synchronous Communications Line Terminal

Line Speed	600-50,000 BPS
Facilities	Voiceband, Broadband, Direct Wire
Interfaces	EIA RS232C, CCITT, MIL. STD. 188B
Mode	Synchronous

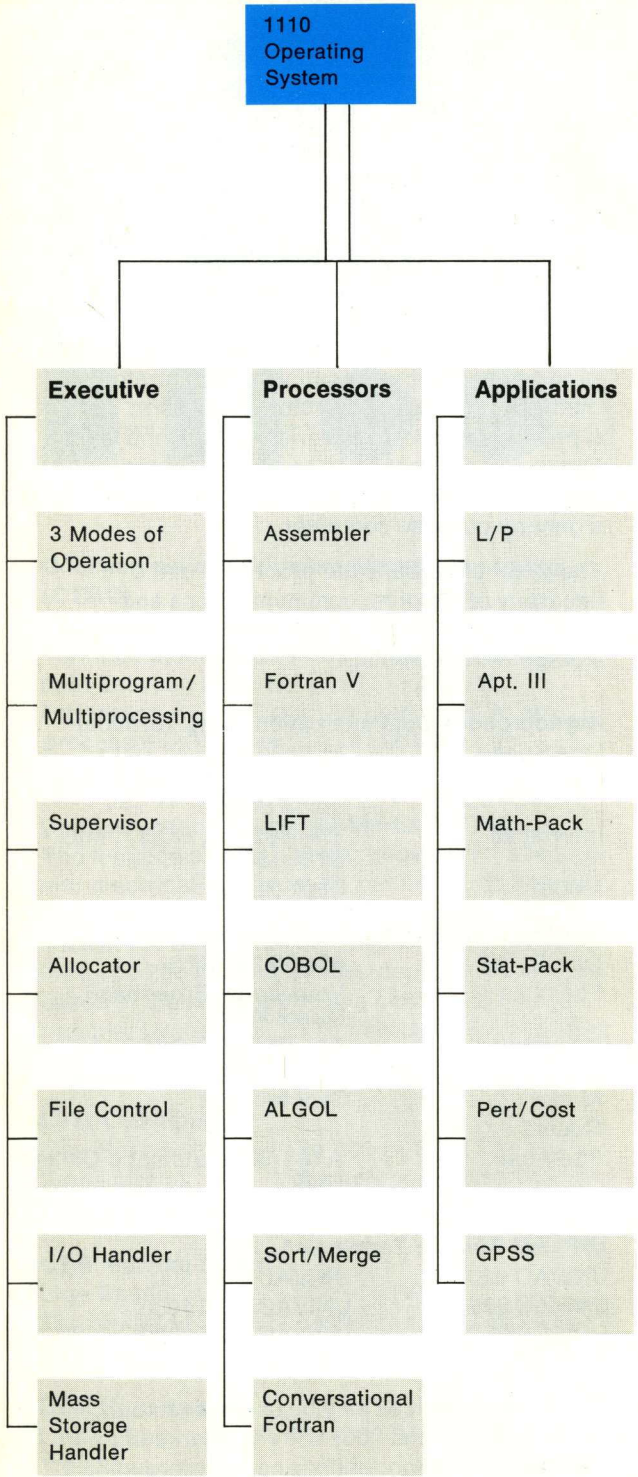
Dialer

Interface	AT&T 801 Automatic Calling Unit

UNIVAC Remote Terminals*

UNIVAC 9200	UNIVAC DCT 500
UNIVAC 9300	UNIVAC DCT 1000
UNISCOPE™ 100	UNIVAC DCT 2000

*Many other devices may be used as remote terminals. Consult your UNIVAC Marketing representative for details, and for information on additional types of CTM's.



UNIVAC 1110 Operating System

The Operating System for the UNIVAC 1110 consists of individual elements which optimize the hardware/software balance of the system. With the exception of the control executive, the various items of the Operating System are independent.

The Operating System encompasses revised industry standard compiler language processors, comprehensive application system support, and total utilization of an 8-bit data base.

Language Processors

Assembler
Translates a symbolic language to machine-language relocatable object coding for the 1110 machine. It allows programmers to generate data words, value or instruction at assembly time.

FORTRAN V
Designed for scientific and engineering computations with all the features of USASI FORTRAN IV plus many valuable extensions.

COBOL
The Univac COBOL compiler provides the complete American Standard COBOL less the report writer.

Any program written to conform to standard specifications can be run using this compiler without the need for conversion.

ALGOL
LIFT—FORTRAN II to FORTRAN V translator

Applications
Linear Programming
SORT/MERGE

APT III
PERT/COST
MATH-PACK
STAT-PACK
GPSS
SIMULA

Instruction Repertoire

The UNIVAC 1110 system,which has basic 320 microsecond read and 520 microsecond write cycle times,uses a four-deep instruction stack. This stacking technique effectively reduces the execution time of most instructions. The execution time is further reduced by the fact that each processor in the system using instruction stacks is available for instruction execution. Therefore, the execution timing of each instruction is peculiar to a given configuration.

Instruction Repertoire

Byte Move with Translate

Byte Translate and Test

Byte Translate and Compare

Byte Compare

Byte to Packed Decimal Convert

Packed Decimal to Byte Convert

Edit

Byte to Binary Single Integer Convert

Byte to Binary Double Integer Convert

Binary Single to Byte Convert

Binary Double to Byte Convert

Byte to Single Floating

Byte to Double Floating Convert

Instruction Repertoire

Single Floating to Byte Convert

Double Floating to Byte Convert

Compress Byte to Binary

Extend Binary to Byte

Compress Byte to Binary Halves

Extend Binary Halves to Byte

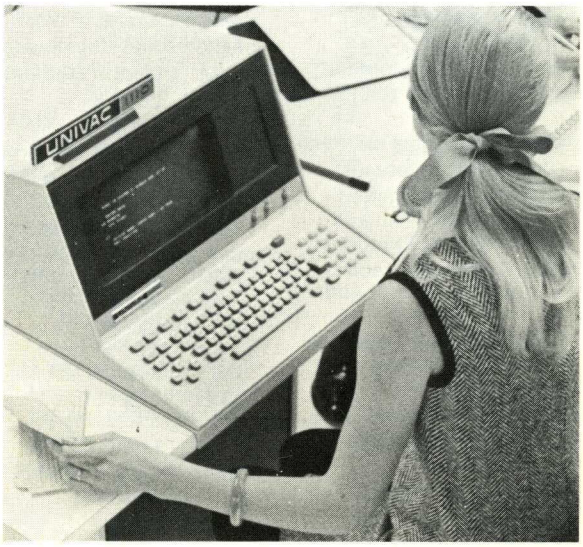
Compress Byte to Binary Long

Extend Binary Long to Byte

Byte Add

Byte Subtract

Byte Move



Operation Code	Description
LA	Load A
LNA	Load Negative A
LMA	Load Magnitude A
LNMA	Load Negative Magnitude A
LR	Load R
LX	Load X
LXM	Load X Modifier
LXI	Load X Increment
DL	Double Load A
DLN	Double Load Negative A
DLM	Double Load Magnitude A
SA	Store A
SNA	Store Negative A
SMA	Store Magnitude A
SX	Store X
SR	Store R
DS	Double Store A
SZ	Store Zero
BT	Block Transfer
AA	Add to A
ANA	Add Negative A
AMA	Add Magnitude to A
ANMA	Add Negative Magnitude to A
AU	Add Upper
ANU	Add Negative Upper
MI	Multiply Integer
MSI	Multiply Single Integer
MF	Multiply Fractional
DI	Divide Integer
DSF	Divide Single Fractional
DF	Divide Fractional
DA	Double Precision Fixed Point Add
DAN	Double Precision Fixed Point Add Negative
AH	Add Halves
ANH	Add Negative Halves
AT	Add Thirds

Operation Code	Description
ANT	Add Negative Thirds
AX	Add to X
ANX	Add Negative to X
FA	Floating Add
FAN	Floating Add Neg.
FM	Floating Multiply
FD	Floating Divide
LUF	Load and Unpack Floating
LCF	Load and Convert to Floating
Double Precision	
DFA	Floating Add
DFAN	Add Negative
DFM	Multiply
DFD	Divide
DFF	Double Load and Convert to Floating
MCDU	Magnitude of Characteristic Difference to Upper
CDU	Characteristic Difference to Upper
FEL	Floating Expand and Load
FCL	Floating Compress and Load
AX	Add to X
ANX	Add Negative to X
LXM	Load X Modifier
LX	Load X
SX	Store X
LXM	Load X Increment
LMJ	Load Modifier and Jump
TLEM	Test Less or Equal to Modifier
JMGI	Jump Modifier Greater and Increment
OR	Logical OR
XOR	Logical Exclusive OR
AND	Logical AND
MLU	Masked Load Upper

Operation Code	Description
SSC	Single Shift Circular
DSC	Double Shift Circular
SSL	Single Shift Logical
DSL	Double Shift Logical
SSA	Single Shift Algebraic
DSA	Double Shift Algebraic
LSC	Load Shift and Count
DLSC	Double Load Shift and Count
LSSC	Left Single Shift Circular
LDSC	Left Double Shift Circular
LSSL	Left Single Shift Logical
LDSL	Left Double Shift Logical
SE	Search for Equal
SNE	Search for Not Equal
SLE	Search for Less or Equal
SG	Search for Greater
SW	Search for Within Range
SNW	Search for Not Within Range
	Masked Search for:
MSE	Equal
MSNE	Not Equal
MSLE	Less or Equal
MSG	Greater
MSW	Within Range
MSNW	Not Within Range
MASL	Masked Alphanumeric Search for Less or Equal
MASG	Masked Alphanumeric Search for Greater
SLJ	Store Location and Jump
LMJ	Load Modifier and Jump

Operation Code	Description
JGD	Jump on Greater and Decrement
DJZ	Double Precision Zero Jump
JPS	Jump on Positive and Shift
JNS	Jump on Negative and Shift
JZ	Jump on Zero
JNZ	Jump on Non-Zero
JP	Jump on Positive
JN	Jump on Negative
JK	Jump on Keys
HKJ	Halt on Keys and Jump
JNB	Jump on No Low Bit
JB	Jump on Low Bit
JMGI	Jump Modifier Greater and Increment
JO	Jump on Overflow
JNO	Jump on No Overflow
JC	Jump on Carry
JNC	Jump on No Carry
JIC	Jump on Input Channel Busy
JOC	Jump on Output Channel Busy
JFC	Jump on Function in Channel
TEP	Test Even Parity
TOP	Test Odd Parity
TLEM	Test Less or Equal to Modifier
TZ	Test for Zero
TNZ	Test for Non-Zero
TE	Test for Equal
TNE	Test for Not Equal
TLE	Test for Less or Equal
TG	Test for Greater
TW	Test for Within Range
TNW	Test for Not Within Range
TP	Test for Positive
TN	Test for Negative
DTE	Double Precision Test Equal
EX	Execute
NOP	No Operation
TS	Test and Set

Instruction Repertoire

Operation Code	Description
LIC	Load Input Channel
LICM	Load Input Channel and Monitor
DIC	Disconnect Input Channel
LOC	Load Output Channel
LOCM	Load Output Channel and Monitor
DOC	Disconnect Output Channel
LFC	Load Function in Channel
LFCM	Load Function in Channel and Monitor
AACI	Allow All Channel External Interrupts
PACI	Prevent All Channels External Interrupts

Operation Code	Description
ER	Executive Return
SCN	Store Channel Number
LPS	Load Processor State Register
LSL	Load Storage Limits Register
III	Initiate Interprocessor Interrupt
SIL	Select Interrupt Locations
LCR	Load Channel Select
LLA	Register/Load Last Address Register
AAIJ	Allow All I/O Interrupts and Jump
PAIJ	Prevent All I/O Interrupts and Jump