PRELIMINARY INFORMATION

ON THE

CONTENT OF REGISTERS OF THE

1103A FLOATING POINT INSTRUCTIONS

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The layout of the "Floating Point Content of Registers" is not the same as that of the fixed point instructions. There are more conditions affecting the final content of A. First, has the NEFF been set or cleared by instruction 05? Second, what is the relative size of (u) and (v)? For these reasons, only the Pack and Unpack commands are in the usual format. Since the arithmetic Floating Point commands do not change (u) and (v), $(u)_f$ and $(v)_f$ are not included in the Contents of Registers of operations 64, 65, 66, 67, 01, and 02.

The binary point of floating point numbers is usually between the twenty-eighth and the twenty-seventh place. After the arithmetic pseudo-normalizing process, the mantissa is in A_L, and the binary point is between A_{63} and A_{62}. It may or may not be normalized. The position of the most significant bit (MSB) indicates what has occurred. If normalized, the MSB will be in A_{62}.

The value of the significant bits depends upon whether rounding has occurred. Rounding in effect adds an extra bit to the value of (a) at A_{35} (unless the addition of the rounding bit carries into A_{62}, in which case the final left shift is omitted and the rounding bit remains added to the value of A_{34}.

The value of $(Q)_f$ will be either (1) the normalized rounded, and packed result (NRP), or (2) the pseudo-normalized result (PN).

NOTE: If A or Q is the v-address of any floating point command other than the pack or unpack command (A) or (Q) will be destroyed by the Unpack (u) sequence before the unpack (v) sequence is reached.

Instruction: Floating Add (FAuv)	Operation: 64

Function: Form in Q the normalized rounded and packed floating point sum of (u) and (v).

NE FF	Arithmetic Conditions		$(A)_f$ MSB	$(A)_f$ Value of significant bits	$(A)_f$ Round	$(Q)_f$ Norm	$(Q)_f$ Value
0	$(u) \geq (v)$		A_{62}	$(u_m).2^{(u_c)-(v_c)+(v_m)}$	yes	NRP	(u) + (v)
	$(u) < (v)$		A_{62}	$(v_m).2^{(v_c)-(u_c)+(u_m)}$	yes	NRP	(u) + (v)
1	$(u) \geq (v)$	$(u_c)-(v_c) \geq 2$	A_{61}	$(u_m).2^{(u_c)-(v_c)+(v_m)}$	no	PN	(u) + (v)
		$(u_c)-(v_c) < 2$	$A_{61}-A_{33}$	$(u_m).2^{(u_c)-(v_c)+(v_m)}$	no	PN	(u) + (v)
	$(u) < (v)$	$(v_c)-(u_c) \geq 2$	A_{61}	$(v_m).2^{(v_c)-(u_c)+(u_m)}$	no	PN	(u) + (v)
		$(v_c)-(u_c) < 2$	$A_{61}-A_{33}$	$(v_m).2^{(v_c)-(u_c)+(u_m)}$	no	PN	(u) + (v)

Instruction: Floating Subtract (FSuv)	Operation: 65

Function: Form in Q the normalized, rounded and packed floating point difference of (u) and (v).

NE	Arithmetic		$(A)_f$			$(Q)_f$	
FF	Conditions		MSB	Value of significant bits	Round	Norm	Value
0	$(u) \geq (v)$		A_{62}	$(u_m).2^{(u_c)} - (v_c)_{-(v_m)}$	yes	NRP	(u) - (v)
	$(u) < (v)$		A_{62}	$(v_m).2^{(v_c)} - (u_c)_{-(u_m)}$	yes	NRP	(u) - (v)
1	$(u) \geq (v)$	$(u_c)-(v_c) \geq 2$	A_{61}	$(u_m).2^{(u_c)} - (v_c)_{-(v_m)}$	no	PN	(u) - (v)
		$(u_c)-(v_c) < 2$	$A_{61}-A_{33}$	$(u_m).2^{(u_c)} - (v_c)_{-(v_m)}$	no	PN	(u) - (v)
	$(u) < (v)$	$(v_c)-(u_c) \geq 2$	A_{61}	$(v_m).2^{(v_c)} - (u_c)_{-(u_m)}$	no	PN	(u) - (v)
		$(v_c)-(u_c) < 2$	$A_{61}-A_{33}$	$(v_m).2^{(v_c)} - (u_c)_{-(u_m)}$	no	PN	(u) - (v)

Instruction: Floating Point Multiply (MPuv)	Operation: 66

Function: Form in Q the normalized rounded and packed floating point product of (u) and (v).

NE	Arithmetic	$(A)_f$			$(Q)_f$	
FF	Condition	MSB	Value of significant bits	Round	Norm	Value
0		A_{62}	$(u_m).(v_m)$	yes	NRP	(u).(v)
1	$(u_m).(v_m) \geq \frac{1}{2}$	A_{61}	$(u_m).(v_m)$	no	PN	(u).(v)
	$(u_m).(v_m) < \frac{1}{2}$	A_{60}	$(u_m).(v_m)$	no	PN	(u).(v)

Instruction: Floating Point Divide (FDuv)	Operation: 67

Function: Form in Q the normalized, rounded and packed floating point quotient of $(u) \div (v)$

ME FF	Arithmetic Condition	$(A)_f$ MSB	$(A)_f$ Value of significant bits	$(A)_f$ Round	$(Q)_f$ Norm	$(Q)_f$ Value
0		A_{62}	$(u_m) \div (v_m)$	yes	NRP	$(u) \div (v)$
1	$(u_m) \div (v_m) \geq 1$	A_{61}	$(u_m) \div (v_m)$	no	PN	$(u) \div (v)$
	$(u_m) \div (v_m) < 1$	A_{60}	$(u_m) \div (v_m)$	no	PN	$(u) \div (v)$

Instruction: Floating Point Polynomial Multiply (FPuv)	Operation: 01

Function: Form in Q the sum of (v) and the product of $(Q)_i.(u)$

(NE FF should be cleared for the execution of this instruction. If it is not the product mantissa will be rounded not with one, but with (A_L).)

NE	Arithmetic	$(A)_f$			$(Q)_f$	
FF	Condition	MSB	Value of mantissa	Round	Norm	Value
0	(Q) (u) $\geq$ (v)	A_{62}	$(Qu)_m.2^{(Qu)c-(vc)+(v_m)}$	yes	NRP	$(Q)_i(u)+(v)$
	(Q) (u) $<$ (v)	A_{62}	$(v_m).2^{(vc)-(Qu)c+(Qu)_m}$	yes		

Instruction: Floating Point Inner Product (FIuv)	Operation: 02

Function: Form in Q the normalized, rounded and packed sum of (Q_i) and the product of (u) and (v).

(NE FF should be cleared for the execution of this instruction; if it is not, the product mantissa will be rounded, not with one, but with (A_L).)

NE FF	Arithmetic Condition	$(A)_f$ MSB	$(A)_f$ Value of significant bits	$(A)_f$ Round	$(Q)_f$ Norm	$(Q)_f$ Value
0	$(Q)_i \geq (u)\ (v)$	A_{62}	$(Qm)_i.2^{(Qc)_i-(uv)_c+(uv)_m}$	yes	NRP	$(Q)_i+(u)(v)$
	$(Q) < (u)\ (v)$	A_{62}	$(uv_m).2^{(uv)c-(Qc)_i+(Qm)_i}$	yes	NRP	$(Q)_i+(u)(v)$

Instruction: Floating Point Unpack (UPuv)	Operation: 03

Function: Unpack (u) replacing (u) with (u_m) and replacing (v_c) with (u_c) or its complement if (u) is negative. The characteristic portion of $(u)_f$ contains sign bits. The sign and mantissa bits of $(v)_f$ are cleared to zero.

Storage Class		Contents of Register & Storage Position After Operation					
		$(MC)_f$ or $(MD)_f$		$(A)_f$			$(Q)_f$
u	v	u	v	MSB	Value of bits	Round	
MC or MD	MD or MC	(u_m)	(u_c)		No change		No change
	A	(u_m)	——	A_{34}	(u_c)	no	No change
	Q	(u_m)	——		No change		(u_c)
A	MD or MC	——	(u_c)	A_{26}	$(A_m)_i$	no	No change
	A	——	——	A_{34}	$(A_c)_i$	no	No change
	Q	——	——	A_{26}	$(A_m)_i$	no	$(A_c)_i$
Q	MD or MC	——	(u_c)		No change		$(Q_m)_i$
	A	——	——	A_{34}	$(Q_c)_i$	no	$(Q_m)_i$
	Q	——	——		No change		$(Q_c)_i$

Instruction: Normalize, Round, & Pack (NPuv)	Operation: 04

Function: Replace (u) with the normalized rounded packed floating point number obtained from the possibly unnormalized mantissa in $(u)_i$ and the biased characteristic in $(v)_c$.

It is assumed that $(u)_i$ has the binary point between u_{27} and u_{26} ($(u)_i$ is scaled 2^{-27}).

Storage Class		Contents of Registers & Storage Position After Operation					
		$(MC)_c$ or $(MD)_f$		$(A)_f$			$(Q)_f$
u	v	u	v	MSB	Value of bits	Round	
MC or MD	MD or MC	NRP(u)+(v_c)	No change	A_{62}	$(u_m)_f$	yes	No change
	A	NRP(u)+(v_c)	——	A_{62}	$(u_m)_f$	yes	No change
	Q	NRP(u)+(v_c)	——	A_{62}	$(u_m)_f$	yes	No change
A	MC	——	No change	A_{34}	NRP$(A_R)_i$+(v_c)	yes	No change
	A	——	——	A_{34}	NRP$(A_R)_i$+$(A_{Rc})_i$	yes	No change
	Q	——	——	A_{34}	NRP$(A_R)_i$+(Q_c)	yes	No change
Q	MD or MC	——	No change	A_{62}	$(u_m)_f$	yes	NRP$(Q)_i$+(v_c)
	A	——	——	A_{62}	$(u_m)_f$	yes	NRP$(Q)_i$+$(A_{Rc})_i$
	Q	——	——	A_{62}	$(u_m)_f$	yes	NRP$(Q)_i$+$(Q_c)_i$

Instruction: Floating Point Normalize Exit (NEj)	Operation: 05

Function: If J=0 clear the normalize exit flip-flop (designated NFF); if j-1 set NFF to 1

(a) The results of setting NFF to 1 is set forth in the "Contents of Registers"

(b) When NFF is set to 1, it will remain set until cleared by another NEj - instruction

(c) NFF must be cleared for FP, FI, and MP instructions