COPY NO. 57

Univac®

LARC CIRCUITRY

SECTION I

STANDARD LOGIC-CIRCUITRY TYPES

Preliminary Edition

FEBRUARY 1960

Remington Rand Univac®
DIVISION OF SPERRY RAND CORPORATION
PHILADELPHIA 3, PENNSYLVANIA

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LARC CIRCUITRY

Section I

ERRATA

(1) The entire content of page 1-29 should be placed between the first and second paragraphs of page 1-33.

(2) The reference to figure 8a in the last line of the first paragraph of page 1-25 should be to figure 10a.

(3) The reference to transistors Q1 and Q5 in the third line of the text on page 1-24 should be to transistors Q1 through Q5.

(4) The arrowhead in the transistor Q2 symbol of figure 1-37 on page 1-85 should be reversed, making Q2 an NPN transistor and agreeing with the note.

SECTION I
STANDARD LOGIC-CIRCUITRY TYPES

1-1. INTRODUCTION

The complete logic design of the Larc computing unit, processor, and main storage is based upon the use of solid-state circuit elements: diodes for AND-OR logic, transistors for amplification, and magnetic cores for fast-access storage. The logical functions are performed throughout the entire system by means of a relatively small number of standard circuit types. All circuit components, excepting those in the clocks and power supplies, are packaged on printed-circuit plug-in cards of uniform dimensions. The number of different card types is held to a minimum.

The following descriptions cover the theory of operation of each of the standard circuit types. Since most of these circuit types have a specific logical application, the object of the description is to relate the circuit operation to its essential logical properties in the system; thus the circuits described here in Section I include all of those shown on the logical diagrams—except those associated with the core storage, which are covered in the manual on core storage.

1-2. GATE INVERTERS

The gate inverter is the most widely used circuit in the Larc system. Known in logic terms as a stroke function, it is designed to perform the dual logical functions of AND and OR gating, and its basic configuration is used in many of the other standard Larc circuits, such as pulseformers and drivers. The gate inverter consists of a diode-gating input circuit and an inverting transistor amplifier. Three different types of gate inverters are used in the system: 1C, 1E, and 1S.

1-3. TYPE-1C CIRCUIT

The type 1C gate inverter circuit is shown in figure 1-1. For this initial description the circuit is duplicated to show clearly the logical significance of the output of the transistor when it is conducting (figure 1-1a) and when it is switched off (figure 1-1b). In the Larc system all information is expressed in combinations of 0 bits and 1 bits,

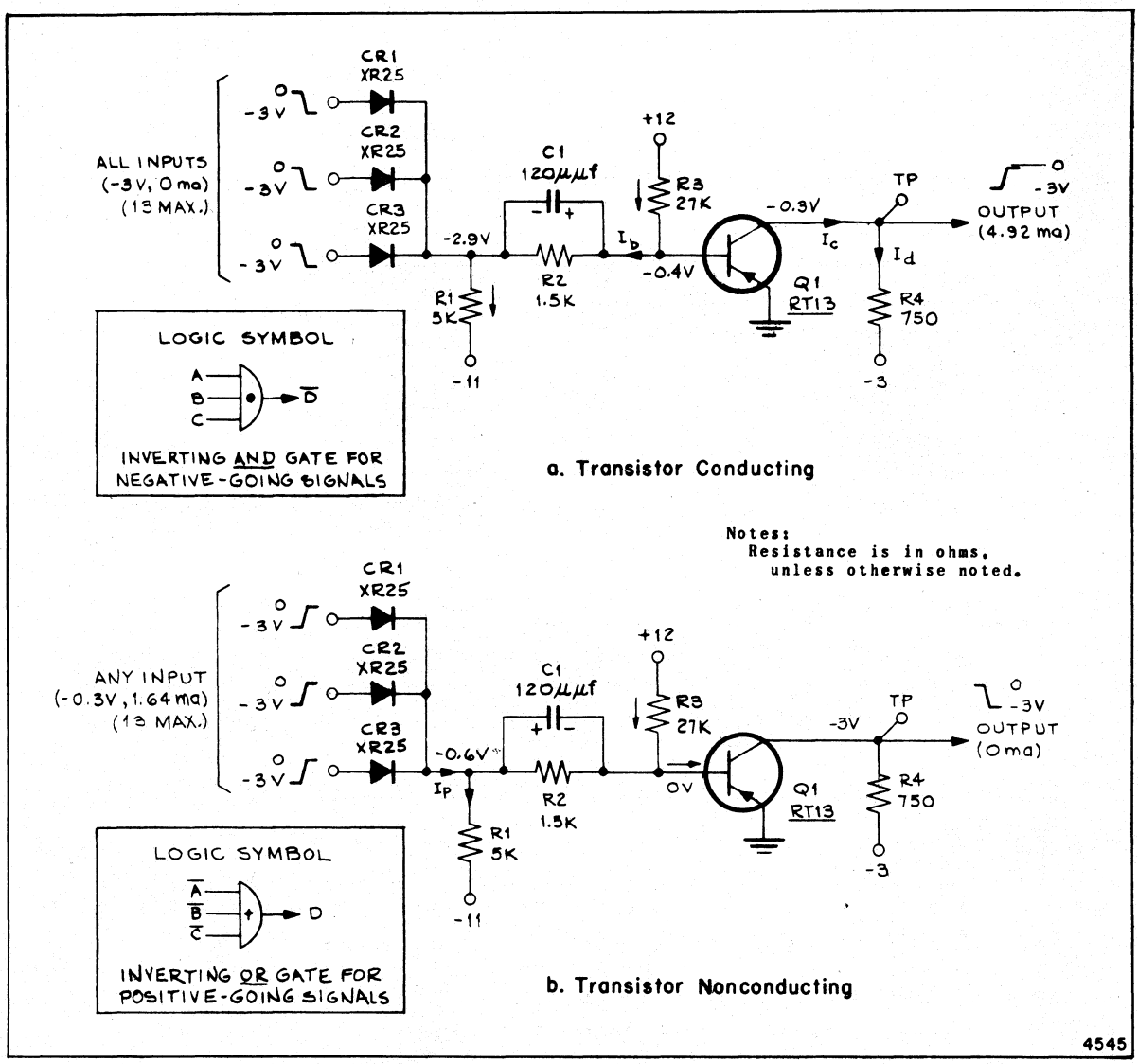


Figure 1-1. Type-1C Gate Inverter

represented electrically as high and low signals. The transistor output-voltage levels shown in figure 1-1 represent typical information in which the signals are close to zero reference level or at some negative potential. A signal at or very close to the zero reference level is a high and a signal at the negative potential is a low.

The type-RT13 transistor, connected so that the base is the controlling electrode, is used in all the basic gate-inverter circuits: 1C, 1E, and 1S. The RT13 is a surface-barrier transistor (Philco type SB100) which permits extremely fast switching functions while it operates at relatively low voltage ratings. However, the RT13 can be considered to operate in essentially the same manner as a conventional PNP junction transistor. Therefore, in order that the transistor be conducting, the base-emitter circuit must be biased in the forward direction by making the base slightly negative with respect to the emitter.

Figure 1-1a illustrates the state of the circuit when the transistor is conducting. This condition is brought about by means of the supply voltages and the constant-current coupling network (R1, R2, R3), provided that all of the input diodes (CR1, CR2, and CR3) are cut off. (Three input diodes (type XR25) are shown in the illustration, although any number of inputs from one to 13 may be connected to a single 1C circuit.) If all the inputs are at the -3-v level, the diodes will be reverse-biased, and the base current (I_b) will be sufficient to operate the transistor. The resulting collector current (I_c) will cause the output potential to rise toward ground. Thus from the logical viewpoint the circuit is acting as an inverting AND gate since the output will be relatively positive or high only if all the inputs are negative-going signals.

The circuit parameters are chosen so that the bias voltage on the base is approximately -0.4 v. This amount of bias will insure the delivery of sufficient base current. The voltage at the top of R1 is set to -2.9 v to provide a reverse bias of 0.1 v on the input diodes. The base current then is limited to the difference between the pull-down current through R1 from the -11-v source and the pull-up current through R3 from the +12-v supply.

While the transistor is conducting, the output potential at the collector will rise from -3 v toward ground but will be negative with respect to ground by an amount equal to the sum of the voltage drops between the emitter and base and between the base and collector. The final collector potential with the transistor fully conducting is called the bottoming potential and should never be more negative than -0.3 v. As indicated in figure 1-1a, the output current available for driving the load is nominally 4.92 ma. In logical terms this amount of current is equivalent to 3 drive units or 9 current units.* Consequently, a 1C circuit operating individually is capable of driving a load consisting of no more than three 1C circuits or the equivalent.

In order to switch the transistor off, a positive-going signal is required at any one of the input diodes. As shown in figure 1-1b, CR1, CR2, and CR3 are all receiving positive-going inputs and therefore will conduct in the forward direction through R1. The increased base drive current (I_p) through R1 will cause the potential at the input to the circuit to rise toward ground. The input potential level actually rises from -2.9 v to about -0.6 v:

Output voltage from preceding collector	-0.3 v
Maximum drop across XR25 diode	-0.3 v
	-0.6 v

As a result of this diode current the base voltage will rise to ground potential or slightly above. In either case the base-emitter diode is biased in the reverse direction and the transistor will be cut off. The

* One drive unit: 1.64 ma, the input required for a 1C circuit.
One current unit: 0.55 ma, the input required for a 1E circuit.

collector output voltage then will drop to the supply level at -3 v. Since the output is negative when any of the inputs becomes relatively positive, the circuit is now acting as a logical inverting OR gate.

The coupling capacitor C1, sometimes called a speed-up capacitor, improves the speed of response of the circuit. When the transistor is to be turned off, the charge stored on the plates of C1 when the transistor was conducting (figure 1-1a) is discharged through the base-emitter circuit, thereby reducing the turn-off time. In addition, the capacitor provides an initial surge of input current when the transistor is changed from the cut-off to the conducting condition. Without the initial surge of input current the output signal would have a slower rise time.

1-4. TYPE-1E CIRCUIT

The 1E circuit is a low-level gate inverter that operates in exactly the same way—and has the same configuration—as the type 1C gate inverter. The 1E circuit operates at a lower current level than the 1C circuit and therefore is used whenever the number of logical loads that must be driven by a 1C circuit is greater than 3. The only difference between the 1E and 1C gate inverters is in the values of the components in the coupling network and the dummy load resistor. As shown in figure 1-2, the resistors in the 1E circuit have all been increased by a factor of roughly 3 over the corresponding parts in the 1C circuit. With the same supply voltages, therefore, the current requirements for operating the RT13 in the 1E circuit are only about one third of those required for the 1C circuit.

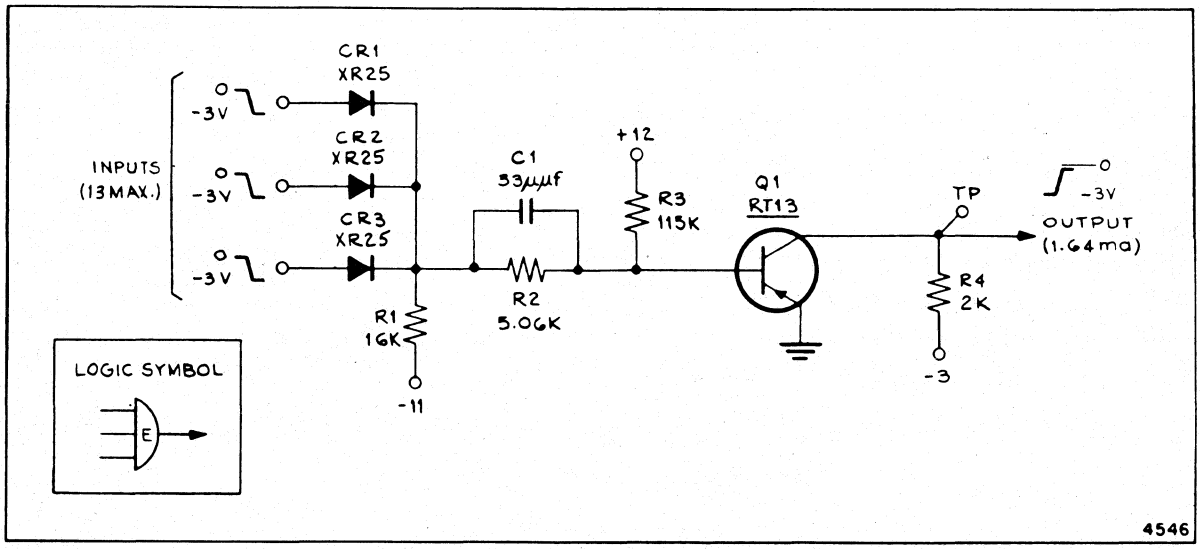


Figure 1-2. Type-1E Gate Inverter

The output collector current from the 1E circuit is equal to 1 drive unit, or 1.64 ma. Consequently a 1E circuit can drive only a single 1C circuit. On the other hand, the input current required to turn the transistor off is only 0.55 ma, and therefore up to nine 1E circuits can be driven simultaneously by one 1C circuit. Operated as either an AND or OR gate inverter, the 1E circuit has slightly longer delay than the 1C. If

the delay of the 1C is taken as standard and made equal to 1, the delay of the 1E circuit is 1.6.*

1-5. TYPE-1S CIRCUIT

The 1S gate inverter is essentially a desensitized version of the 1C circuit. The circuit has been designed to satisfy the need for an inverter, more stable than the 1C type, which can be connected to form a feedback loop and thus be used as a flip-flop in asynchronous logic networks. † There are two versions of the 1S circuit, both of which are relatively immune to noise pulses. The type 1S-A is available for general asynchronous applications; the type 1S-B is a special unit intended for use in the critical self-sprocketing logic of the drum synchronizers. The schematic diagrams of both types of circuits are given in figure 1-3.

* One delay unit, the time required to switch the 1C circuit, varies between 11 and 40 μs. Delay and timing considerations are covered fully under heading 1-9.

† Flip-flop circuit arrangements are covered under heading 1-17.

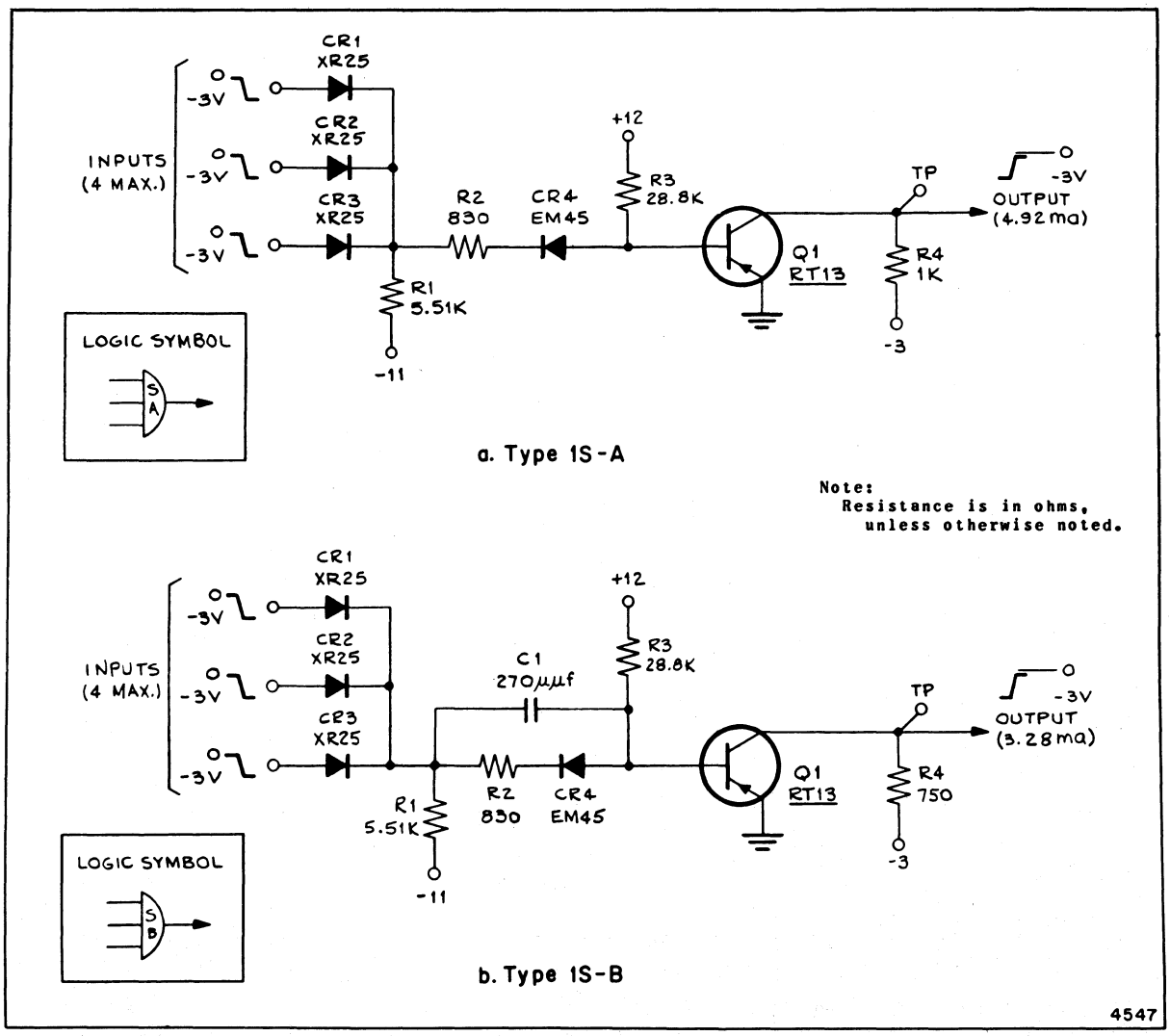


Figure 1-3. Type-1S Gate Inverter

The principle of operation of the 1S circuits is essentially the same as that of the 1C circuit. The increase in stability is achieved by increasing the reverse bias on the input diodes when the transistor is conducting, and by increasing the reverse bias at the base when the transistor is cut off. The larger biases will result in operation of the circuit at higher turn-on and turn-off clipping levels. As shown in figure 1-3a, the 1S-A circuit has been modified from the basic 1C circuit by reducing the value of the coupling resistor R2 (from 1500 to 830 ohms) and by including the voltage step-up diode CR4. In addition, the speed-up capacitor (C1 in figure 1-1) has been eliminated.

The effect of R2 and CR4 is to reduce the input impedance of the coupling network so that the base current will complete its transition from minimum to maximum values over a smaller input-voltage swing. The conducting diode (CR4) acts as a low-impedance voltage source in order to maintain a high step-up voltage from input to base terminals with smaller pull-up current from the 12-v supply. The result of this modification to the input coupling circuit is to provide a nominal reverse bias of 0.56 v on the input diodes, and a reverse bias of 0.28 v on the base of the transistor. With these larger biases the speed of response of the 1S-A circuit is about one third that of the 1C circuit—that is, single-stage delays are about three times greater than the 1C. The input and output drive requirements of the 1S-A are the same as those of the 1C circuit.

The type 1S-B gate inverter (figure 1-3b) is a faster version of the 1S-A circuit and has delay times comparable to the 1C circuit. The increase in speed over the 1S-A circuit is effected by adding the speed-up capacitor (C1) across R2 and CR4, lowering the value of the dummy load resistor (R4), and selecting a faster transistor (grade number 2122). The stable features of the circuit are similar to the 1S-A, but the use of the lower-value load resistor results in an output-current level about two thirds as large as the 1C or 1S-A. The function of the speed-up capacitor is the same as that of the 1C circuit.

1-6. TRANSISTOR SELECTION

The very fast operation of the gate-inverter circuits, as well as of all other standard logic circuit types that employ the RT13 surface-barrier transistor, make it imperative that careful consideration be given to all aspects of transistor performance. The subject of transistor classification and circuit application is very broad, and no attempt is made here to cover the area fully. It is introduced only to give some indication of the problems involved and to explain the coding system for selecting and grading the RT13 units. The most important parameters covered by the selection process are (1) current gain, (2) breakdown voltage, and (3) rise and storage times.

The current gain is measured in terms of the large-signal beta so that the ratio of the peak base-drive current (I_p) to d-c base current (I_b) (figure 1-1b) plus the ratio of the dummy resistor current (I_d) to base currents (figure 1-1a) can be selected to provide optimum circuit speed. The larger the I_p/I_b ratio, the more overdrive there is available to turn the transistor on, thus reducing the delay due to poor driving-pulse fall times. The larger the dummy current, the faster any stray capacitances will be charged and the faster the output step voltage will drop. The

nearer the I_d/I_b ratio is to the value of beta, the less oversaturation there is. Beta, then, must be selected for an optimum value in such a way as to give the required gain and minimum delay.

For a transistor turning on, beta is chosen mainly according to loading conditions. The more loads a single collector drives, the less base drive current (I_p) there is available per load and therefore the harder it is to switch the following stages. The result is longer rise times and delays. The maximum number of loads possible is determined, then, by the minimum beta available. For a transistor turning off, the worst operating condition is minimum loading with transistor beta and storage time a maximum. This condition oversaturates the transistor, thereby producing the maximum hole (minority carrier) storage delay, which is a large portion of the total delay of an RT13 transistor. To sum up broadly: the minimum beta should be as large as possible and the maximum beta as small as possible. A minimum beta of 9 (nominal value: 7.4) is found to be the lowest beta that can be used and still achieve the required circuit speed in a standard IC inverter circuit.

The d-c collector voltage is as large as possible in order to decrease the effects of the collector-to-base feedback capacitance and also because tolerance conditions are harder to satisfy at lower voltages. However, a 3-v swing at the collector is the maximum allowable in view of the breakdown-voltage aging characteristics of the RT13 transistor. A nominal value for the rise time—defined as the time required for the collector current to reach 90 percent of its maximum value—is 17 mμs. Storage time, nominally 54 mμs, is defined here as the period between the completion of base-current flow and the time when the collector current begins to fall. These conditions are but a few of the more important design parameters which must be examined carefully before the RT13 transistor is used in a particular circuit application.

Every RT13 transistor used in the Larc circuit packages is tested thoroughly for conformance with the parametric values mentioned under heading 1-6, paragraph 1 and then is graded accordingly. The grade number consists of a four-digit identification number that specifies the ranges of current gain, breakdown voltage, and rise and storage times applicable to a transistor. Table 1-1 lists the parameters and shows how they are divided

Table 1-1. Grading Code, Type RT13 Transistor

Code Number	Code-Digit Position and Transistor Parameters			
	1	2	3	4
	Current Gain (beta)	Breakdown Voltage	Rise Time (mμs)	Storage Time (mμs)
1	≥5 <7.5	≥6 <10	≥17 =25	≥54 =70
2	≥7.5 <9.5	≥10	≥12 <17	≥46 <54
3	≥9.5 <11		<12	<46
4	≥11 <12			
5	≥12			

into groups with a code number assigned to each group. For example, a transistor coded 3122 would have a current gain between 9.5 and 11, a breakdown voltage between 6 and 10 v, a rise time between 12 and 17 mμs, and a storage time between 46 and 54 mμs.

An additional classification number (from 1 to 5) is assigned to each type 1C and 1S-A gate inverter and is determined solely by the logical application of the circuit. This number appears beside every 1C and 1S circuit shown in the logic diagrams and determines the number of current units (1E drives) required from that circuit under existing loading conditions. This method of classification facilitates the interpretation of current-gain requirements for the individual circuits and enables maximum use to be made of all grades of RT13 transistors. The logical grading code is as follows:

Code No.	Current Units
1	1.0 ... 3.0
2	3.0 ... 4.5
3	4.5 ... 6.0
4	6.0 ... 7.5
5	7.5 ... 9.0

Thus a 1C circuit which is coded with a 2 on the logic diagram must be equipped with a transistor capable of supplying sufficient current for driving up to four 1E circuits independently. It is evident that grading on the logical diagrams of 1E circuits is not necessary since they are permitted to drive only a single 1C circuit. Special applications of the RT13 transistor, such as in the type 1S-B gate inverter and in other circuits described elsewhere in the manual, are not coded on the logical diagrams but are selected according to the parameters given in table 1-1.

1-7. PACKAGING

All the gate inverter circuits (1C, 1E, and 1S) are packaged in a similar manner; each printed-circuit board contains up to ten circuits. Each transistor and its associated gate-inverter circuit is assigned a position number from 0 to 9 on the card. There are 38 available contacts on each card type for use as input or output terminals, as well as ten test positions for making contact to the collector terminals of each of the transistor circuits on a card.

The only differences between the various card types for each kind of gate-inverter package are in the number of circuits on each card and in the number of input diodes provided for each circuit. There is a total of 15 card types for 1C packages (card types CA ... CK, CM ... CO, CR), eight types for 1E packages (EA ... EF, EH, EI), and one each for the 1S circuits (card types SA for 1S-A and SB for 1S-B). Table 1-2 lists all the gate-inverter card types, together with the number of circuits on each card and the number of input connections provided at each of the circuit positions. Card types CM, CN, CO, and CR are for use in the core storage only. Card type DC also contains passive delay elements (heading 1-19).

Table 1-2. Card Types: Gate-Inverter Packages

Card Type	Number of Input Connections Per Circuit Position									
	0	1	2	3	4	5	6	7	8	9
CA	1	1	1	1	12	8	1	1	1	1
CB	3	2	5	2	3	2	4	2	3	2
CC	1	3	2	2	10	2	2	2	2	2
CD	3	3	4	2	4	2	4	2	3	1
CE	7	1	1	1	1	7	1	1	7	1
CF		6	5		6	7			9	
CG	11			5				8	10	
CH	6			6	2		6	6	6	
CI	6	1		1	1	6	6	1	6	1
CJ	6	2	3	2	3	3	3	2	5	
CK	13	1		1	2	1	1	8	1	1
CM	3	2	3	2	3	2	3	2	3	2
CN	1	4	3	2	3	2	3	2	3	2
CO	2	2	2	2	2	2	2	2	2	2
CR	1	1	2	1	2	1	2	1	2	1
EA	3	2	3	3	4	2	3	3	3	2
EB	3	2	4	3	3	1	4	3	3	2
EC	3	2	3	2	3	2	4	2	4	3
ED	3	2	3	2	4	2	4	2	4	2
EE	4		4	3	4	3	4	2	4	1
EF	6	2	3	2	3	2	3	2	3	2
EH	6			6	2		6	6	6	
EI		1	13			9	8	1		1
SA	3	3	4	2	4	2	4	2	3	1
SB	3	3	4	2	4	2	4	2	3	1
DC	5	1	4	1	6	1	4	1	4	1

1-8. PULSEFORMERS

In the logical design of the Larc system, timing is an extremely important consideration, since all operations must be synchronized by the pulses on a central clock bus. In the process of generating the signals needed to perform the various logical functions an information level is conveyed through a path or several paths; each path consists of many stages of transmission units (gate inverters, delay elements, and so forth). No unit can be operated without introducing some delay, which is not constant but varies within a range depending on the tolerances allowed for the passive and active elements used in the unit. Consequently a means must be provided for synchronizing the signals with the central clock pulses of the system so that the output of one stage or logic level reaches some other stage at the correct instant in time. The pulseformer is the standard Larc circuit used to synchronize the changes in information level being propagated throughout the system.

The basic pulseformer circuit is composed of three parts: a gate-inverter-driver, a bidirectional transmission gate, and a flip-flop. (See block-logical diagram, figure 1-4a.) The gate inverter (similar to the

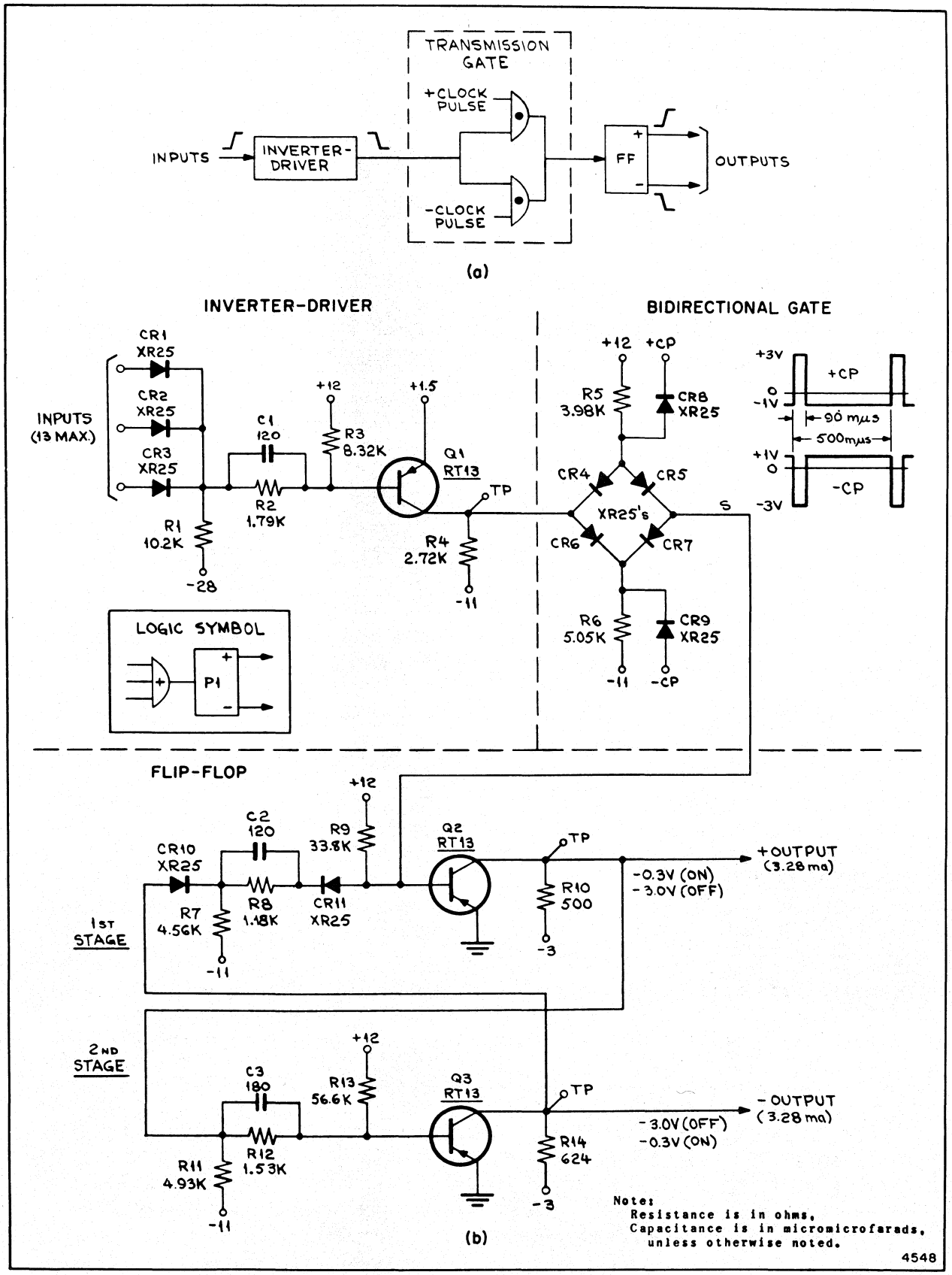


Figure 1-4. Type-P1 Pulseformer

type-1C configuration) performs a logical OR function at the input of the pulseformer and therefore acts as the driving element for the bidirectional gate and flip-flop circuits. The transmission gate consists of a pair of diode AND gates which are capable of handling both polarities of clock pulses as control inputs, and in furnishing a positive or negative pulse as triggering input to the flip-flop. The flip-flop circuits are composed of two or more transistor amplifiers (similar to the type 1C circuit) so that both positive and negative outputs of varying drive levels can be accommodated. The number of transistors used in the flip-flop circuit, and therefore the number and polarity of outputs, is the means for distinguishing between the three types of available pulseformer circuits. The three types of circuits are designated as P1, P2, and P3.

1-9. TYPE-P1 CIRCUIT

The complete schematic diagram of the type P1 pulseformer is given in figure 1-4b. As the logical notation signifies, the input inverter-driver stage is functioning as an OR gate for positive-going input signals; that is, if any input is relatively positive, the driver transistor Q1 will be turned off, and its collector output voltage will drop from a slightly positive value to a slightly negative one. The principle of operation of the driver circuit is similar to the type-1C inverter described under heading 1-3. The circuit parameters have been chosen so that the input requirements are the same as the 1C circuit (switching current: 1.64 ma); the output supplies the correct level and polarity of drive for controlling the bidirectional gate.

Basically the bidirectional gate consists of a positive AND gate (diodes CR4 and CR8) and a negative AND gate (diodes CR6 and CR9) whose function is to sample the output of the driver stage during the 0.1-μs period of the clock pulses. At all other times the gates are logically closed so that no change will take place at the output at S—that is, at the junction of the isolating diodes CR5 and CR7. Thus, if the output of the driver is positive at the time of a clock pulse, the positive clock gate (CR4, CR8) must function so as to give a positive-going output at S. Similarly, if the driver output is negative at the clock-pulse time, the negative clock gate (CR6, CR9) must operate so that the output is negative-going.

The combined operation of the inverter-driver and the diode AND gates can best be described with the aid of figure 1-5, which shows the four possible cases for controlling the trigger input to the flip-flop S. Figure 1-5a illustrates the operation of the circuit for the case where the driver stage is on and the clock pulses are off; in figure 1-4b all the inputs to the driver stage are relatively negative and therefore the transistor is conducting; the positive clock pulses (+CP) are relatively negative (positive clock gate closed) and the negative clock pulses (-CP) are relatively positive (negative clock gate closed). The conducting Q1 causes its collector voltage to rise toward the emitter bias potential of +1.5 v. This voltage actually reaches about +1.2 v, which is applied to the junction of diodes CR4 and CR6 in order to cause CR6 to conduct through R6 while it keeps CR4 cut off. Since the polarities of the clock pulses are such as to cause diodes CR8 and CR9 to be biased in the forward direction, CR8 and CR9 will conduct while diodes CR5 and CR7 are cut off, and the voltage level at point S will not change. Thus the flip-flop will

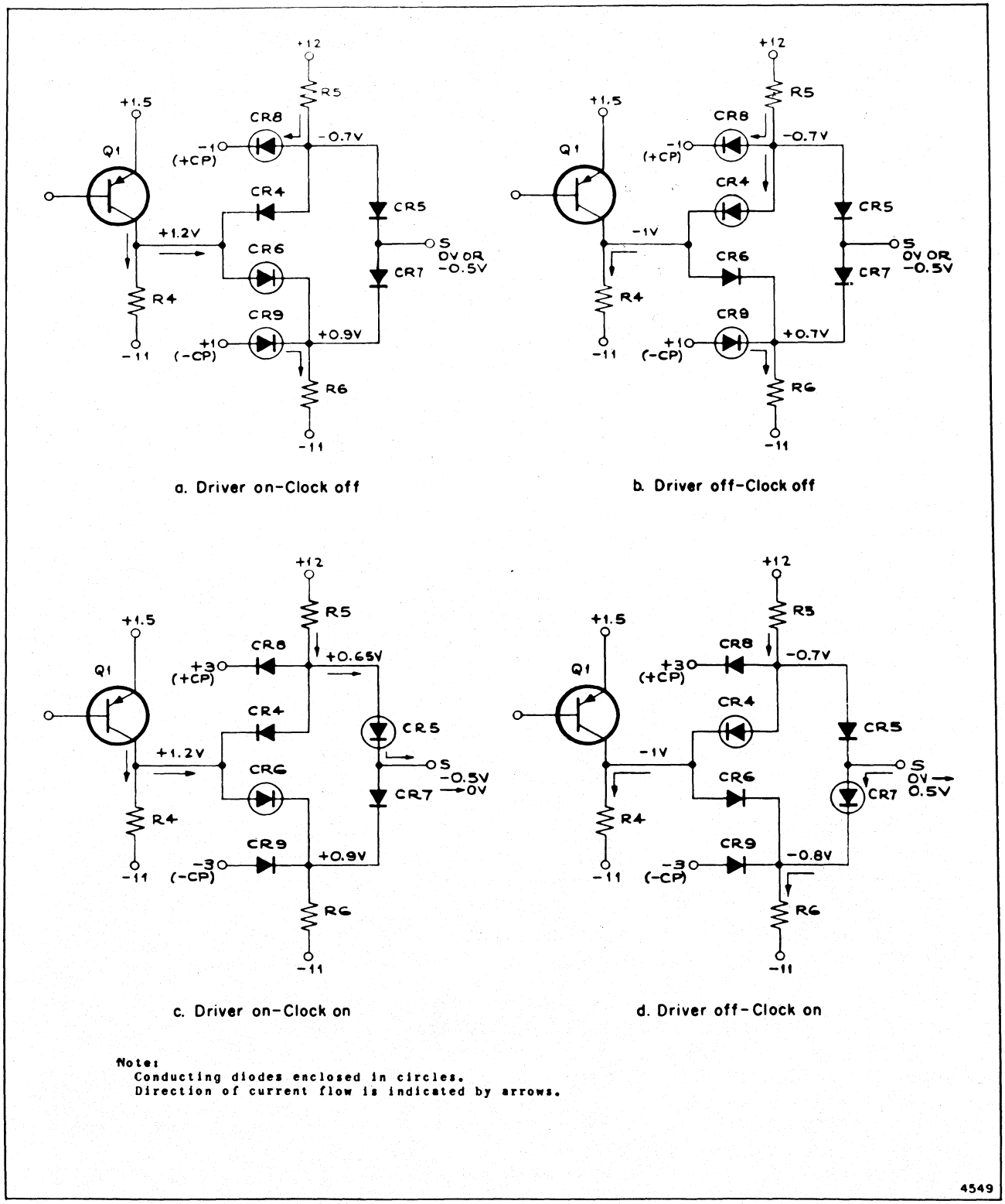


Figure 1-5. Driver-Bidirectional Gate Operation

remain in the state resulting from the previous sampling; that is, the base voltage of transistor Q2 will remain at 0 v if it was last switched off, or at -0.5 v if it was last switched on.

A similar condition exists if the driver stage is switched off, provided that the clock pulses are still off. This condition is shown in figure 1-5b, where a positive-going input to the driver stage has caused Q1 to be cut off. In this case the voltage level at the junction of the positive and negative AND gates (-1 v) will be determined by the current flowing through the path consisting of R5, CR4, and R4. As before, the isolating diodes CR5 and CR7 are biased in the reverse direction, and the voltage at S is unchanged.

Figure 1-5c shows what happens when clock pulses arrive and the driver stage is on. The positive voltage at the collector of Q1 will cause CR6 to conduct and CR4 to be cut off as in the first case in figure 1-5a. However, the presence of the 0.1-μs positive clock pulse (+CP) will cause CR8 to be cut off, and a current will flow through R5 and CR5 to the base of Q2. (Q2 appears on figure 1-4.) This current will cause the output at S to rise and is sufficient to trigger the first stage of the flip-flop from the on state to the off state, or, if Q2 is already off, to keep it off. As indicated in figure 1-5c, the current through CR5 causes the bias voltage on the base of Q2 to rise from its relatively negative value of -0.5 v to ground potential, or to maintain the bias at ground potential if the base-emitter circuit of Q2 was previously biased in the reverse direction.

If a positive input signal is applied to switch the driver stage off, then the first stage of the flip-flop must be triggered from off to on, or kept on. This condition is shown in figure 1-5d, where the voltage at the output of Q1 has dropped to -1 v, turning CR4 on and CR6 off. The coincidence of the negative clock pulse (-CP) will cause CR9 to be cut off so that a current will flow from the base-emitter circuit of Q2 through CR7 and R6. With the negative clock gate open, the output at S will drop to -0.5 v. Thus the base of Q2 will be biased in the forward direction and the first stage of the flip-flop circuit will be in the conducting state. The conducting Q2 (figure 1-4b) will cause its output level to be relatively positive; this output is applied directly to the input circuit of the second stage of the flip-flop. Transistor Q3 then will be cut off and its output will be relatively negative. The output of Q3 is fed back to the input circuit of Q2 so that the circuit remains in this condition even after the clock pulses have passed. Thus it is evident that a positive-going input to the driver stage will cause a negative input to the diode gate, which in turn will function at the next clock time (figure 1-5d) and cause Q2 to be conducting and Q3 to be off. The relative polarities of the input and output signals are then as shown in figure 1-4a. Negative inputs to the driver will reverse the polarities of the outputs of the flip-flop at the next clock time.

The principle of operation of the transistor circuits in the flip-flop stages, (figure 1-4b), including the coupling networks, speed-up capacitors, input diode (CR10), and stabilizing diode (CR11), is essentially the same as that described under heading 1-2 for the gate-inverter circuits. The circuit parameters closely approximate those of the standard IC circuit so that the output current levels will be about the same. The positive output from Q2 and the negative output from Q3, therefore, are both capable of

driving two 1C loads or the equivalent. The third drive unit from each of the two transistors is needed for the feedback loop.

Notice in figure 1-4b that R14, the load resistor of Q3, has a larger value than R10, the load resistor of Q2. The increase in resistance is needed because the current gain (beta) of Q2 has been selected as 10, whereas that of Q3 is 9. These values of beta have been found to be the optimum ones for providing the minimum circuit delays as a function of clock-pulse width. Measurements indicate that the minimum and maximum switching delays of the flip-flop circuit are 4 mμs and 65 mμs, respectively. The minimum switching delay is the time from the occurrence of the clock pulse until the output changes at Q2. The maximum switching-delay value is that from the clock pulse to the output of Q3.

Since the purpose of the pulseformer is to synchronize signals at various points in the logical network, the output of a pulseformer must transmit through no fewer than a certain minimum number of stages and no more than a certain maximum number of stages before it is sampled (retimed by the synchronizing clock pulses) by the next pulseformer. The number of stages allowed between successive pulseformers is determined by the sampling rate (clock-pulse frequency: 2 mc), clock-pulse width (100 mμs maximum), and the maximum and minimum delays of the pulseformer and the intervening transmission units. With the standard unit of delay that of the 1C circuit (minimum unit 11 mμs, maximum unit 40 mμs), the maximum (N_{max}) and minimum (N_{min}) number of stages or levels of circuit logic—in terms of delay units—that can be used between pulseformers is calculated roughly as follows:

$$N_{max} \leq \frac{T - j - D_{max}}{40\ m\mu s} = 8.5$$

$$N_{min} \geq \frac{W + j - D_{min}}{11\ m\mu s} = 5.7$$

Symbol	Meaning	Time (mμs)
T	Clock-pulse period	500
j	Clock-pulse jitter tolerance	10
D_{max}	Maximum delay of pulseformer, plus maximum time by which input to driver must precede clock pulse	150
W	Maximum clock-pulse width	100
D_{min}	Minimum delay of pulseformer, plus minimum overlap allowed between input to driver and clock pulse	47

These figures have been standardized as 8 and 5.6 for the maximum and minimum number of delay units, respectively. If the delay of the input-driver stage of the pulseformer is included, the figures are 9 and 6.6.

The number 6.6 is chosen because the delay of the type-1E gate-inverter circuit is equivalent to 1.6 standard (1C) units. As an example based on the preceding values of delay, the following three combinations of transmission units or their equivalent are the maximum allowed in any path between successive pulseformers:

Combination Examples	Circuit Type	
	1C	1E
1	8	0
2	6	1
3	4	2

1-10. TYPE-P2 AND -P3 CIRCUITS

The P2 and P3 pulseformer circuits differ from the P1 circuit only in output capabilities. These special types of pulseformers are constructed simply by augmenting the P1 circuit with one or two additional stages to produce additional negative outputs. The complete schematic diagrams are given in figures 1-6 and 1-7. Notice that the circuits are identical to the P1 circuit shown in figure 1-4 except for the inclusion of the additional transistors (Q4 in figure 1-6, Q4 and Q5 in figure 1-7) which are connected in parallel with the second stage (Q3) of the standard flip-flop circuit. Consequently the driving power for the additional stages must be supplied by the first stage of the flip-flop (Q2).

In the type-P2 circuit (figure 1-6) transistor Q2 is capable of supplying only 1 drive unit (1.64 ma) from the positive output of the pulseformer because of the input requirements of Q3 and Q4. Transistor Q3 can supply 2 output drive units (3.28 ma) as in the P1 circuit, while the extra stage Q4 can handle a full external load of three 1C circuits or the equivalent. As indicated by the logic symbol, the outputs from Q3 and Q4 are designated as -6 and -9 respectively; the numbers 6 and 9 refer to current units. In the P3 circuit (figure 1-7) the entire output of Q2 is used within the pulseformer to drive transistors Q3, Q4, and Q5, and therefore all the outputs are taken from the negative side of the flip-flop circuit. The amount of drive available from each of the stages follows the same reasoning given for the P2 circuit and is indicated in figure 1-7.

The components in the additional stages (Q4 and Q5) are identical to those in the second stage of the flip-flop (Q3) except for the value of the load resistors (R18 in figures 1-6 and 1-7 and R22 in figure 1-7). The reason for the decrease in the value of load resistance is that the input drive required by Q2 is slightly greater than that needed by standard 1C or equivalent loads.

1-11. TRANSISTOR SELECTION

The testing and grading of the RT13 transistor is no different for the units used in the pulseformer circuits from that described under heading 1-6 for the gate inverters. However, a slightly different system is used on the logical diagrams to specify the grade of each output transistor in the P1, P2, and P3 circuits as compared to the system of grade 1 through

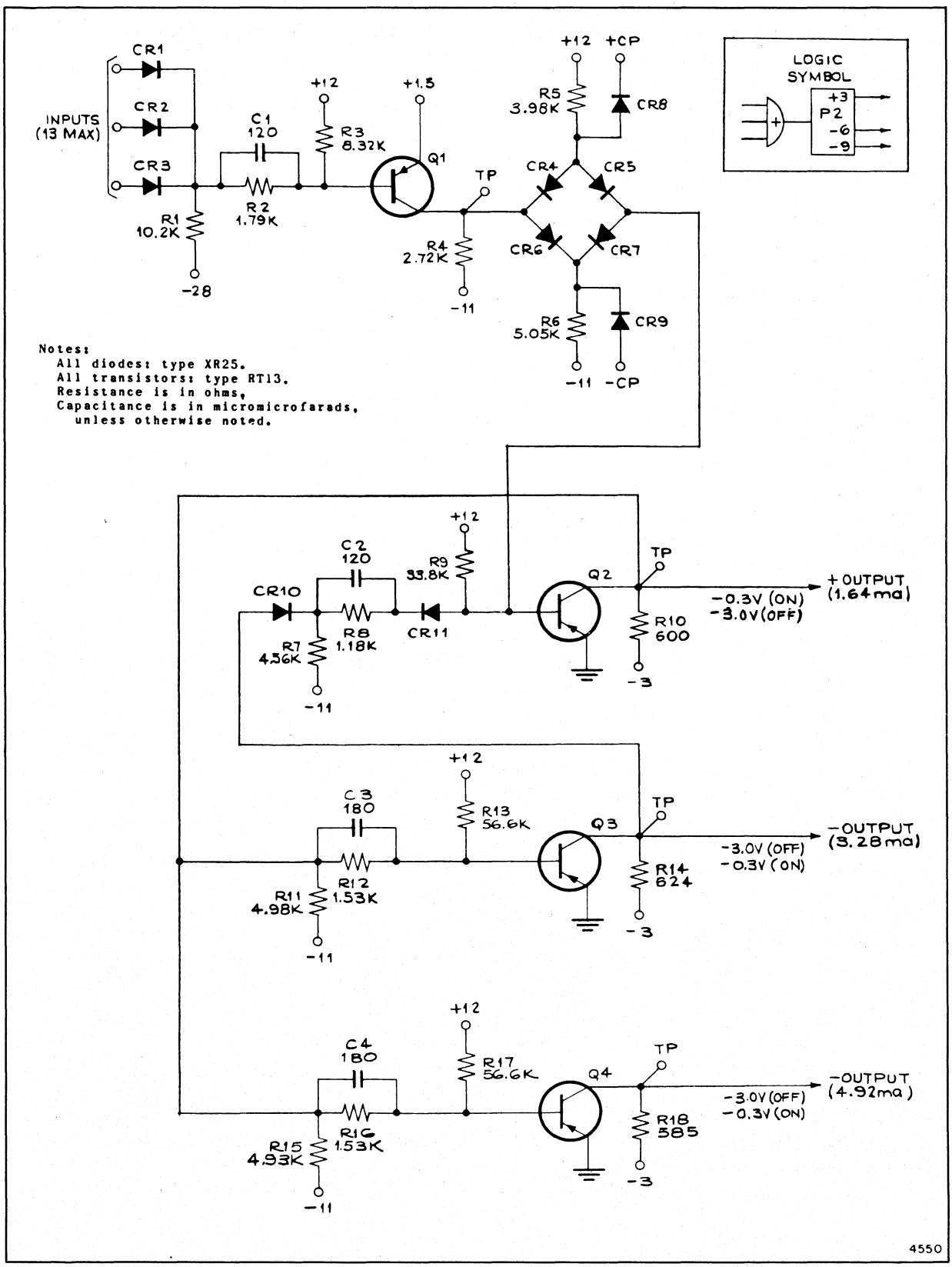


Figure 1-6. Type-P2 Pulseformer

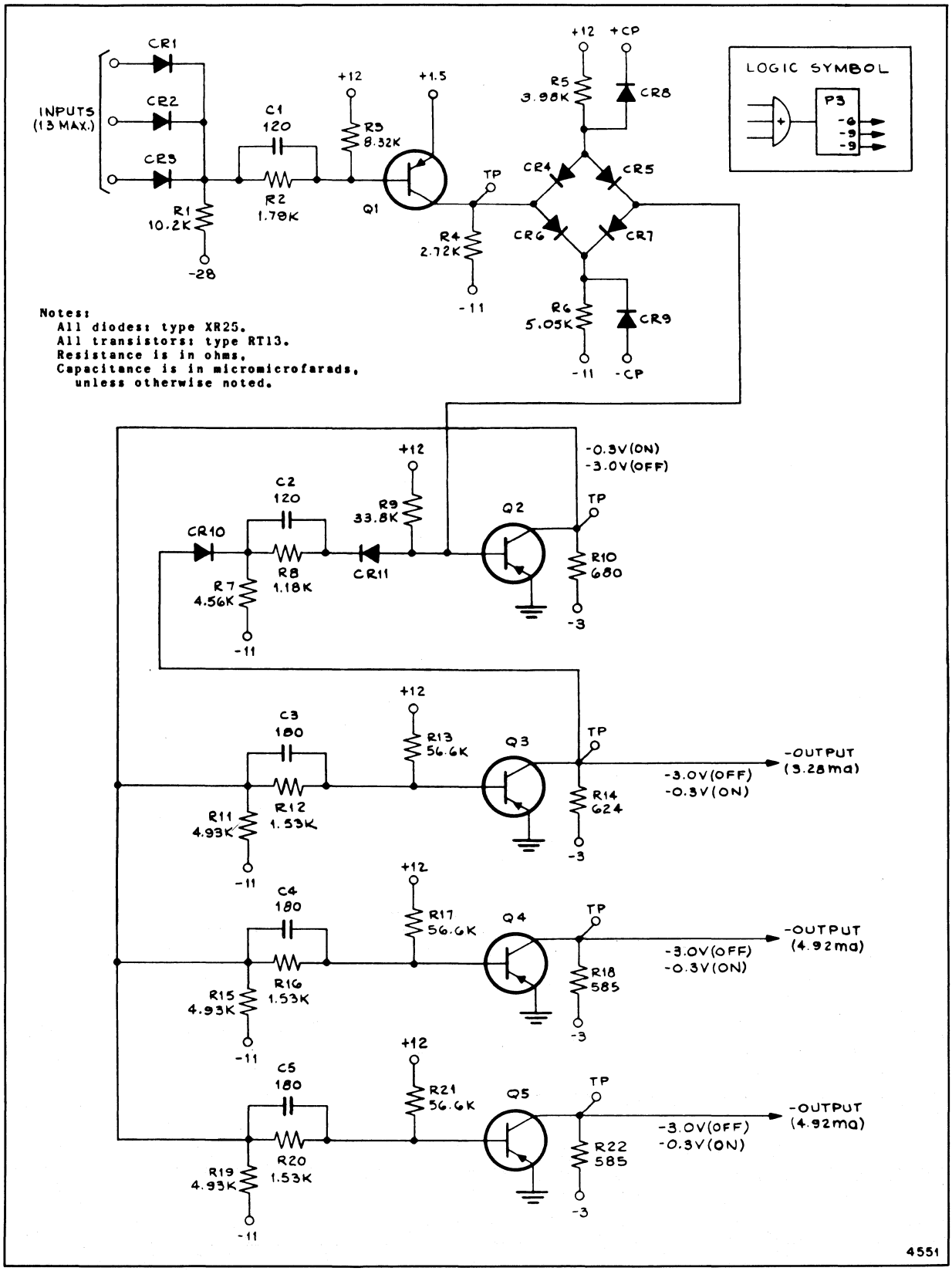


Figure 1-7. Type-P3 Pulseformer

5 for 1C circuits. The number that accompanies each output terminal from a pulseformer unit specifies directly the number of current units (1E drives) needed from the terminal to handle the loading conditions associated with that output. Consequently, the grade number, depending on the current gain of a particular output transistor, can range from 1 to 9, and sometimes can be greater, as in the case of a P2 or P3 circuit.

1-12. PACKAGING

The three basic types of pulseformer circuits are packaged on a total of seven different card types; each card contains two complete circuits. In addition to the three standard pulseformer circuits shown in figures 1-4, 1-6, and 1-7 there are three card types that include a passive-delay element (heading 1-19) at the input to the driver stage of the circuit. These pulseformer circuits with built-in delay also feature a test-jack terminal at the input which may be used to jam the circuit into a particular state for test purposes. Output test terminals are provided for making connections to the collectors of each of the transistors in the circuit. Table 1-3 lists all the pulseformer card types, circuit types, inputs, and the location of each output transistor position. For example, on card type PE the three output transistors associated with each of the two type-P3 pulseformer circuits are located at positions 2 through 7 and the number of input diodes used in each circuit is 11.

Table 1-3. Card Types: Pulseformer Packages

Card Type	Circuit Type	Number of Input Diodes		Output-Transistor Positions									
		Circuit 1	Circuit 2	0	1	2	3	4	5	6	7	8	9
PA	P1	11	11		x	x					x	x	
PC	P2	11	11		x	x	x			x	x	x	
PE	P3	11	11			x	x	x	x	x	x		
PG	P1*	1	1		x	x					x	x	
PK	P2*	1	1		x	x	x			x	x	x	
PP	P3*	1	1			x	x	x	x	x	x		
PV	P1	8	14		x	x					x	x	

*With delay.

1-13. HIGH-POWER AMPLIFIERS

The number of output drive units required of some key signals in the system often exceeds that which is available from the basic gate inverters and pulseformers described under headings 1-2 through 1-12. Low-gain logical amplifiers (such as the 1C circuit) can be pyramided to build up drive, but this method becomes costly when basic amplifier gain is only 3. For example, it would require 14 type-1C stages to deliver the equivalent of 33 (1C) drive units with 3 drive units as input. Consequently the high-power amplifier was developed to provide a fast, high-gain logical circuit with very few additional components.

The basic high-power amplifier circuit consists of two transistors connected to produce what is sometimes called a "transistor pair" or "piggy-back" circuit. The transistor circuit connections are shown in figure 1-8a. The first transistor (Q1) is a low-power unit which is connected to operate as both a common emitter and an emitter-follower stage. The current gain (beta) of this stage from base to collector is equal to β_1 and its gain from base to emitter is $\beta_1 + 1$:

$$\frac{\Delta I_{c1}}{\Delta I_{b1}} = \beta_1 \text{ (common-emitter gain)}$$

$$I_{e1} = I_{c1} + I_{b1}$$

$$\frac{I_{e1}}{I_{b1}} = \frac{I_{c1} + I_{b1}}{I_{b1}} = \frac{I_{c1}}{I_{b1}} + 1$$

$$\therefore \quad \frac{\Delta I_{e1}}{\Delta I_{b1}} = \beta + 1 \text{ (emitter follower gain)}$$

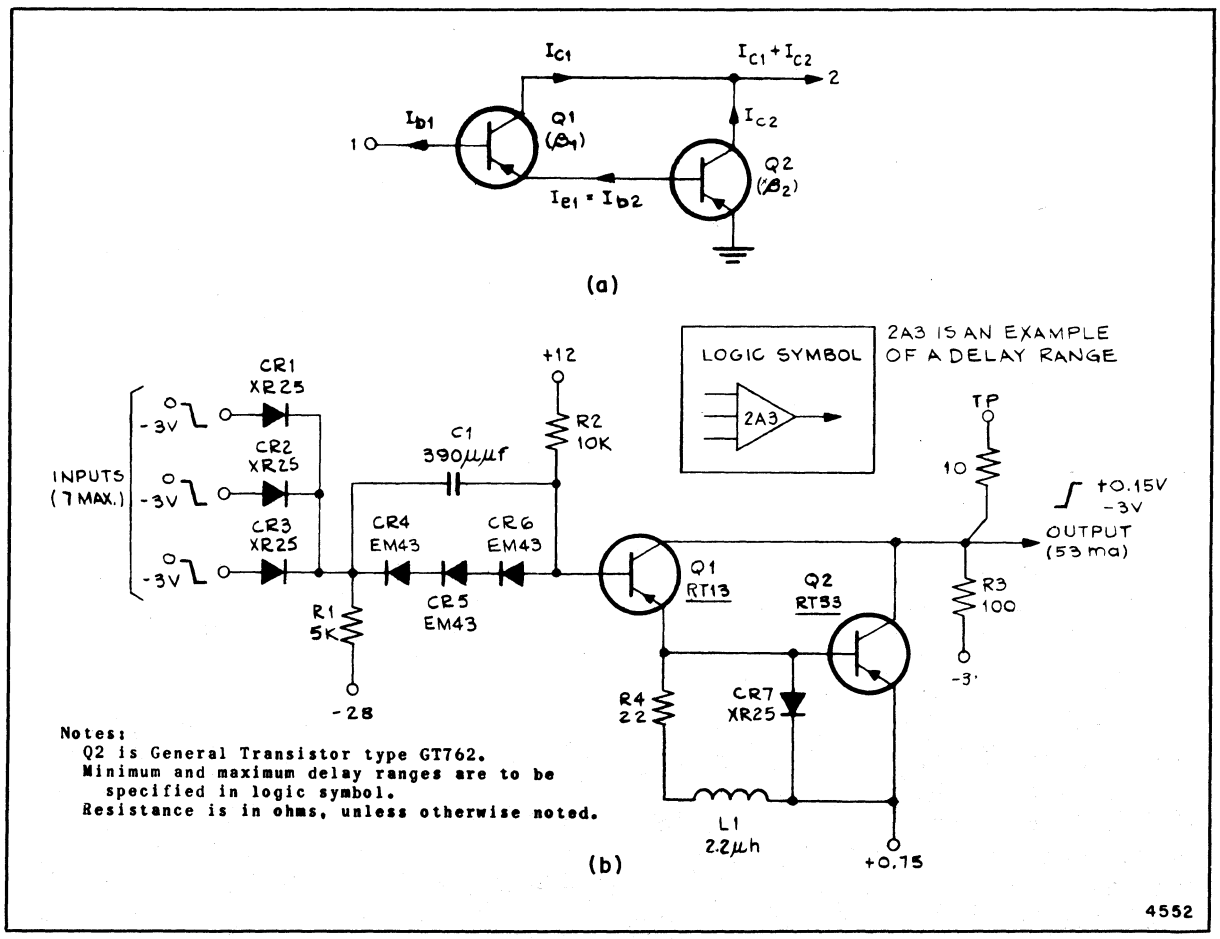


Figure 1-8. High-Power Driver

The emitter current (I_{e1}) of Q1 is also the base current (I_{b2}) of Q2 and therefore it is amplified again by an amount equal to the gain of the high-power second stage β_2. The total current gain of the circuit is the sum of the gains in both paths from input (1) to output (2) figure 1-8a:

$$G_{12} = \beta_1 + (\beta_1 + 1)\beta_2$$

$$= \beta_1 + \beta_2 + \beta_1\beta_2$$

The speed of response of this circuit is somewhat faster than the speed of any other method of cascading two transistors, but the chief advantage of the transistor-pair connection is in its improved turn-off characteristics. Since only the first transistor becomes saturated, it is possible to use a fast, low-gain unit for Q1 (type RT13) because the current level is relatively low. operates at currents much higher than the current level of Q1 (type RT33; General Transistor type GT762) and is therefore inherently slower, but it does not add any hole-storage time to the circuit delay.

A high-power amplifier is used in two standard types of Larc circuits to provide for high output-drive requirements. A high-power driver combines a transistor pair with an input gating arrangement similar to other gate inverters. A high-power pulseformer consists of a high-power driver internally connected to the output of a modified type-P1 pulseformer.

1-14. HIGH-POWER DRIVER

The high-power driver circuit is shown schematically in figure 1-8b. If all the inputs are relatively negative, the gating diodes (CR1, CR2, CR3) will be cut off and the potential level at the base of transistor Q1 will be determined solely by the current flowing in the constant-current coupling network. This network is composed of resistors R1 and R2, coupling capacitor C1, and the voltage step-up diodes CR4, CR5, and CR6. The series-connected diodes help to provide a fairly constant potential difference from input to base terminals with less pull-up current from the 12-v supply. Initially the input impedance of the series transistor bases is high, but the current in the circuit is sufficient to make the base of Q1 negative with respect to the emitter bias supply. As the transistors begin to conduct, the input impedance of the circuit and the forward drops across the biases of Q1 and Q2 become less; the case current of Q1 then is limited to the difference between the pull-down current through R1 and the pull-up current of R2.

The emitter-follower action of Q1 causes the base current of Q2 to increase until it is equalized by the shunting effect of the series R4-L1 circuit across the base of Q2. Initially the shunt-circuit impedance is high and therefore does not reduce the drive to the base of Q2. However, the current through L1 builds up gradually, as determined by the L/R time constant, until it reaches a final value equal to the base-to-emitter drop of Q2 divided by R4. With both transistors conducting, the sum of the collector currents becomes large enough to bring the voltage across the dummy

resistor (R3) and the load to a value slightly negative with respect to the emitter bias supply. Finally, Q1 saturates, but because of the circuit connections Q2 does not saturate.* When the RT33 transistor is not saturated, its voltage drop between collector and emitter is about 0.6 v, and thus the output potential level rises about +0.15 v.

The total current gain of the circuit with both transistors fully conducting is equivalent to the sum of gains of each stage plus their product (heading 1-13). This large total gain results in an output current available for driving the load of about 53 ma (96 current units). Thus the high-power driver is capable of driving a load consisting of up to 32 type-1C circuits of 1 drive unit each or the equivalent.

As with any gate inverter, a positive-going signal is required at any of the input diodes in order to switch the circuit to the off condition. The amount of driving current needed to switch the transistor-pair circuit is necessarily larger than that required by the basic gate inverters and is equal to the full output of a 1C circuit (4.92 ma). When the driving voltage is close to ground potential (-0.3 v maximum), an input diode will conduct in the forward direction through R1. Because of the voltage drops across the forward-biased step-up diodes (CR4, CR5, and CR6), the voltage at the base of Q1 will rise to a value which is slightly positive with respect to the emitter bias supply, and the transistors will begin to cut off. In operation the voltage at the top of R1 rises to about -0.6 v (driving voltage minus drop across XR25 diode). The drop across the type-EM43 silicon diodes with pull-up current from R2 at 1 ma is about 0.6 v for each diode. Thus the voltage at the base will be about +1.2 v.

The driving current through the step-up diodes and coupling capacitor (C1) to the base of Q1 causes the rapid clean-up of the heavily saturated first stage. As the junction currents of the RT13 fall to zero, the field around the inductor (L1) collapses and forces a reverse current through the base-emitter circuit of Q2. Although the second stage was not saturated, reverse base current reduces the fall time of the collector current. Because of the wide range of transistor characteristics that must be accommodated in this circuit, there is usually some current still flowing in the inductor after Q2 is completely off. The bypass diode CR7 prevents this excess current from flowing into the emitter of Q1.

The circuit delay imposed by the high-speed driver is necessarily longer than the basic gate-inverter units (1C, 1E). To facilitate their use in different logic networks, the high-power-driver circuit has been made available in three different ranges of minimum and maximum delay times. These different delay values are a function of the particular transistor characteristics used in the circuit, and they are specified in terms of the standard 1C unit of delay. The minimum-maximum delay ranges available are 2 ... 3, 3 ... 4, and 4 ... 5, where the minimum unit is 11 mμs and the maximum is 40 mμs.

* The collector-to-emitter potential of Q1 is always slightly negative, no matter how hard it is driven. The collector-to-base potential of Q2 must also remain negative, since the emitter of Q1 is tied to the base of Q2, and both collectors are connected together. This is a necessary as well as sufficient condition for insuring that Q2 is not saturated.

1-15. HIGH-POWER PULSEFORMER

The high-power pulseformer combines the functions of a standard pulseformer with a high-power amplifier to provide a retimed high-level output signal. The circuit, shown in figure 1-9, uses the same configurations as the type-P1 pulseformer (figure 1-4) and the high-power driver (figure 1-8). The pulseformer functions, including those of the input driver, bidirectional gate, and flip-flop, are handled in the same way as described for the P1 circuit under heading 1-9. The high-power-driver circuit is connected in parallel with the second stage of the flip-flop and operates in exactly the same way as described under heading 1-14. Thus any positive-going input at CR1, CR2, or CR3 will cause Q1 to be cut off so that Q2 will be conducting at the next clock-pulse time. Q3, Q4, and Q5 then will be switched off, and the output signal from the high-power driver will be negative.

Comparison of the pulseformer circuit of figure 1-9 with the P1 circuit in figure 1-4 shows that the two circuits are identical except that no outputs are taken from the flip-flop stages. In addition, the dummy load resistor has been removed from the collector of Q2 in the high-power unit because of the larger input drive requirements of the high-power output stage. The high-power driver in figure 1-9 is identical to the one in figure 1-8 except for the larger value of the clean-up inductance L1. The power pulseformer can accommodate a longer time constant in the bypass circuit since no signal of shorter duration than 0.5 μs can pass through a pulseformer.

The input drive requirement of the power pulseformer is the same as the P1 (1 drive unit); its output capabilities are the same as for the high-power driver (32 drive units). Because of the output high-power-driver stage the use of the power pulseformer in the logical networks requires that its additional inherent circuit delay be included as part of the total circuit delay between successive pulseformers. The available minimum-maximum ranges for power-pulseformer delay are 2 ... 2 and 3 ... 3, which are specified in terms of the 1C delay unit.

1-16. PACKAGING

The high-power-driver circuit (HPD) is supplied as card types HA and HC. Type HC is intended for use in the core-storage circuits only. The HA card contains two complete high-power-driver circuits plus two standard 1C inverter circuits, with a total of four circuits on each card. The HC card contains only the two high-power drivers. There are seven output test terminals provided on each card, and a total of 35 contacts are available for use as input and output terminals. The number of inputs associated with each circuit position is given in table 1-4.

The high-power pulseformers are packaged in the same manner as the regular pulseformers (heading 1-12) with two complete circuits on each card and provision on some cards for incorporating a passive-delay element and an input test terminal. In addition, the high-power pulseformers are supplied as so-called Z drivers (HPZ) for use in driving the coaxial cables that make up the high-speed bus array. As shown in figure 1-9, the HPZ circuit is exactly the same as the regular power pulseformer except for the

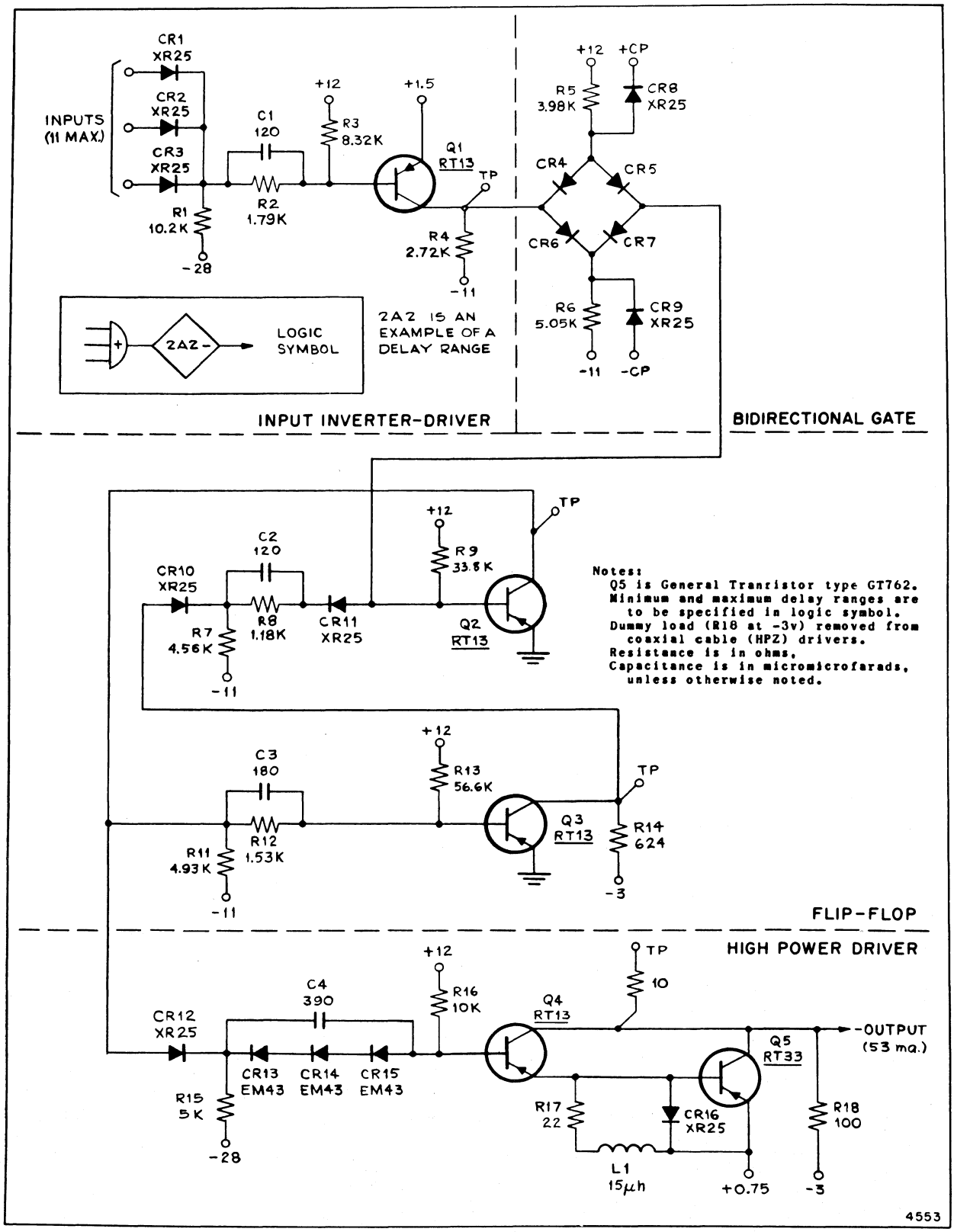


Figure 1-9. High-Power Pulseformer

Table 1-4. High-Power Driver Packages

Card Type	Number of Inputs and Circuit Type for Each Circuit Position						
	0	1	2	3	4	5	6
HA		6 of 1C	6 of HPD		7 of HPD	6 of 1C	
HC			6		7		

output dummy load resistor. Each of the power pulseformer card types has four accessible terminals for use as test points. These test points (figure 1-9) are connected to the collectors of transistors Q1 and Q5. Table 1-5 lists the card types.

Table 1-5. Power-Pulseformer Packages

Card Type	Circuit Type	Number of Inputs for Each Circuit Position			
		0	4	7	9
PR	HP		11	11	
PS	HP*		1	1	
PT	HPZ*		1	1	
PU	HPZ		11	11	

*With delay.

1-17. FLIP-FLOPS

An important required characteristic of computer circuits is that they be able to carry over a signal from one time interval to the next. The flip-flop switching circuit has this characteristic because its output signal depends on its input signal of the preceding time interval. This feature also gives it the attribute of storage. From a purely logical viewpoint, any of the gate-inverter or pulseformer circuits described so far can be connected to form a flip-flop. However, certain considerations limit the type of circuit that can be used and the manner in which it is connected to form a one-bit storage device.

Figure 1-10 shows the basic flip-flop circuit configurations used throughout Larc logic. The gate-inverter arrangement (figure 1-10a) uses two transistors in which the output of Q1 is fed back to control the input to Q2. If the R inputs are all negative, any positive-going signal applied at S_1 or S_2 will cause the reset signal to be relatively positive. Thereafter it does not matter what value (S_1 or S_2) may have since a positive-going signal will always be present at the input to Q1. If any R input becomes relatively positive, the situation will be reversed until an S input again becomes positive. Thus it is possible to set the flip-flop into either one of two stable states until it is changed by the input signals.

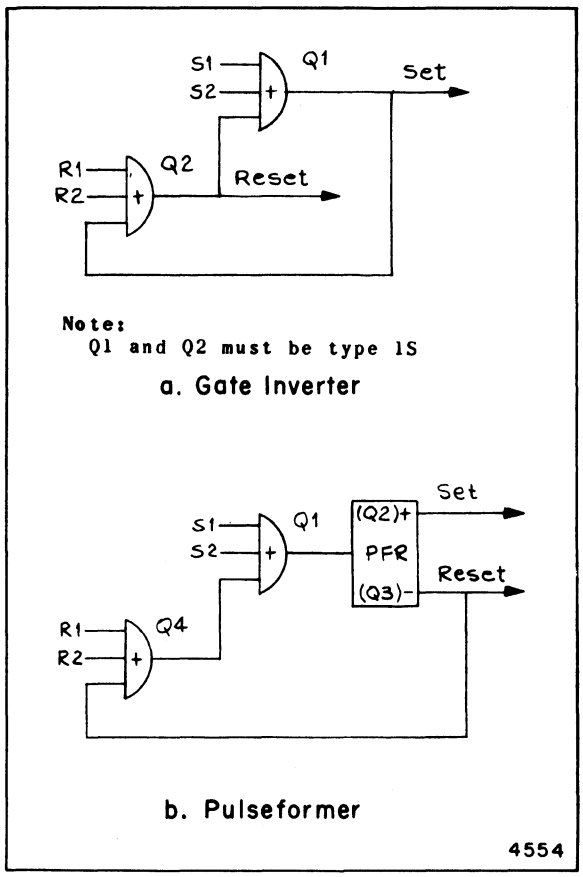


Figure 1-10. Flip-Flop Arrangements

In the designing of the standard gate inverter (type 1C, 1E) the emphasis was placed on fast response. The bias level on the transistor when it is turned off and the bias level on the input diodes when the transistor is conducting are very small. Slight variations in voltage or resistance tolerances can cause the transistor bias to be zero, or the input diodes can remain conducting when they should be cut off. With the connection shown in figure 1-10a transistor Q1 will be conducting while Q2 is cut off, or the reverse. With the assumption of the former condition, a small noise pulse coupled into the emitter of Q2, or a transient originating in the collector supply, may cause the transistor to conduct slightly. This condition will tend to turn Q1 toward the off state since the input-diode bias is very small. The action can become regenerative and reverse the state of the flip-flop. For these reasons the type-1C and -1E gate inverters are not connected to form a feedback loop. As mentioned under heading 1-5, the type-1S gate inverter, with its larger transistor and diode biases, was developed specifically for the purpose of allowing the arrangement of figure 1-8a to be used safely in asynchronous applications.

The pulseformer circuits described under headings 1-8 and 1-13 are used throughout the Larc system to prevent regeneration caused by noise. When equipped with a recirculation path and a reset or clear gate, a pulseformer (PFR) can be used as a one-bit register as shown in figure 1-10b. The function of this circuit is logically similar to that of figure

1-10a but the outputs from transistors Q2 and Q3 can change only once per clock-pulse time. No compensating delay is required to bring the number of stages of delay in the feedback loop to the minimum required between pulseformer inputs if the recirculation path contains an even number of inversions. The coincidence of any positive-going signals at the inputs to Q1 and Q4 will result in the set signals (S_1 or S_2) taking precedence.

1-18. DELAY ELEMENTS

A delay element is used to delay signals a fraction of a clock-pulse period so that pulseformer timing requirements can be more easily met. The delay compensates for the difference between the actual number of levels of logic (in terms of standard (1C) delay units) used in a path between two successive pulseformers, and the total allowable delay (6.6 to 9 standard units). A delay element may be of either the passive or active type, depending on the kind of components used to produce the delay.

The delay circuits described here are used to introduce ranges of delay times of less than a clock-pulse period (delay: < 0.5 μs). Two other types of delay circuits are used in the Larc logic—single-pulser delay and long-delay circuits—to produce delay times greater than 0.5 μs. These special delay elements are used only in the circuits for which they were designed. Therefore the single-pulser delay is described as part of the single-pulser circuit (1-28); the long-delay element, used exclusively in the drum-synchronizer logic, is covered in the section devoted to circuits designed uniquely for use in the drum synchronizers (1-42).

1-19. PASSIVE DELAY

The passive delay element is so called because it consists of passive components only and cannot perform any logical function. The delay is produced by a lumped-constant delay line like the one shown in figure 1-11a. The delay circuit DL is a fairly conventional low-pass filter with mutual inductance between L1 and L2. The tapped coil is of single-layer construction; it contains a powdered-iron core. The mutual inductance and shunt capacitance produce slight overshoot and undershoot effects, thereby improving the rise time of the delay line. The clamping diode CR is used at the output of the delay section to limit the positive portion of the ringing.

The characteristic impedance of the lumped-constant section DL is this:

$$Z_0 = (L_T/C)^{1/2}$$

Cutoff occurs at the frequency at which Z_0 ceases to be resistive and becomes reactive—that is, at

$$\omega_c = \frac{1}{(L_T C)^{1/2}}$$

The delay time of the section, then, is this:

$$T_d = (L_T C)^{1/2}$$

Complete design of a delay line is an advanced problem in filter theory, but some indication of the magnitudes of L and C is given in table 1-6 for the various delay ranges available. As indicated in figure 1-11a, the passive delay line must be terminated in a type-1C inverter circuit. The values of L and C therefore are based on a Z_0 of 1300 ohms, which closely matches the input impedance of the 1C circuit.

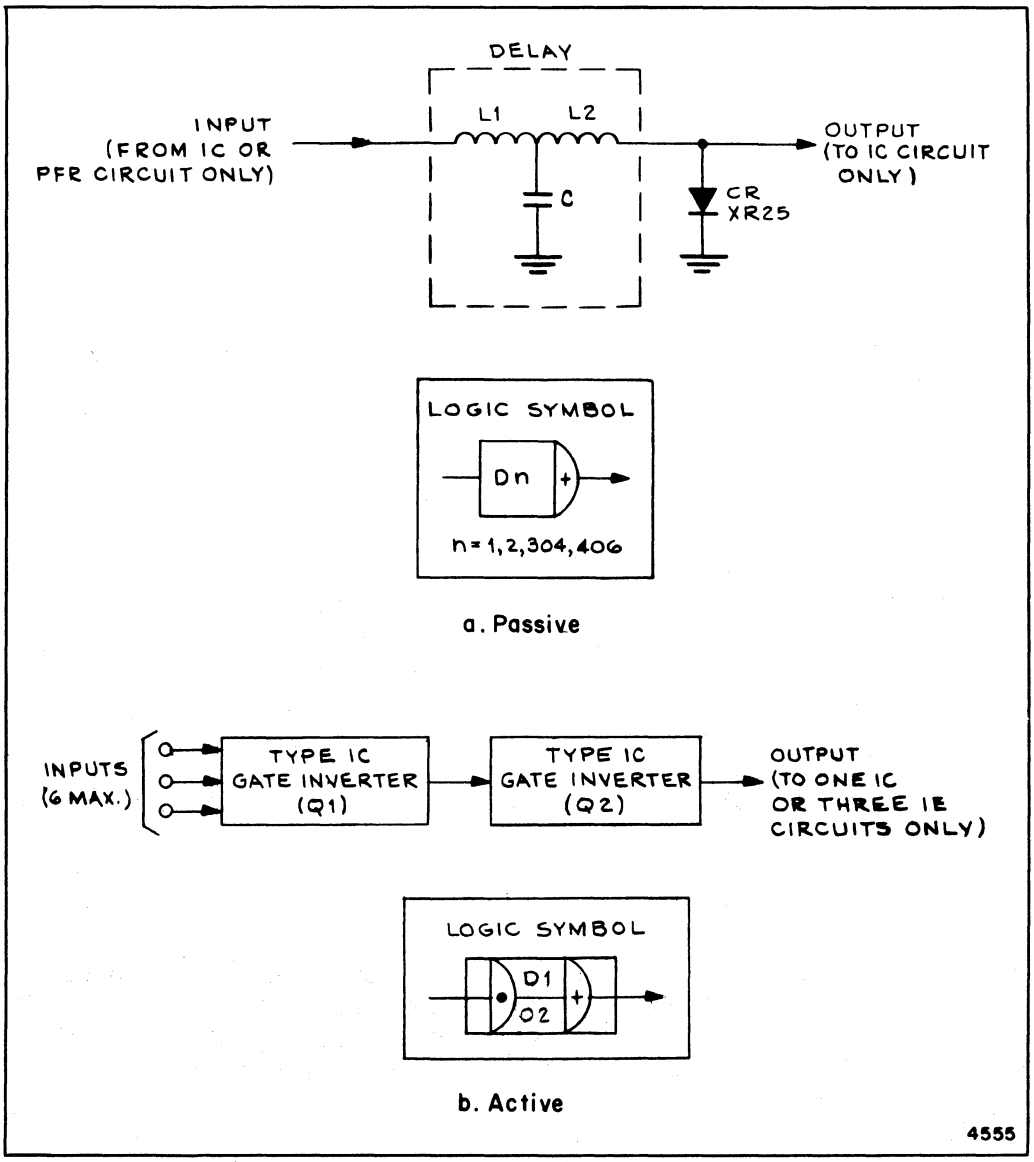


Figure 1-11. Delay Elements

Table 1-6. Characteristics of Delay Units

Delay Element (Dn)	Wire Size (gauge number)	N1 (turns)	L1 (μh)	N2 (turns)	L2 (μh)	L_T (μh)	C (μμf)
D1	HF42	11	1.7	33	9.8	16	10
D2	HF42	18	4.0	54	23	33	33
D304*	HF42	28	7.7	84	42	61	47
D406*	HF46	90	54	90	54	140	68

*D304: D3 through D4.
D406: D4 through D6.

The notation for the type of delay unit (Dn) designates the number of levels of (1C) logic for which the delay compensates, where $1 \leq n \leq 6$. The numeral 0 in the delay value D406 refers to the logical OR function and signifies that the delay element produces delays corresponding to four, five, or six levels of logic. The D304 delay element produces delays corresponding to three or four levels of logic. For example, the D406 element produces a time delay of about 97 mμs, which falls within the ranges of delay spanned by four to six levels of logic (44 ... 160 mμs and 66 ... 240 mμs, respectively). Thus the D406 element may be used in the circuit logic to compensate for either four, five, or six units of delay. Since the passive element can be connected only to a single 1C circuit, and since no logic is permissible at the input to the 1C circuit which the delay element drives, the passive element is always shown in the logic networks as being a combination delay and inverter-amplifier with the same input and output requirements as the 1C circuit, except that no logic functions are allowed at its input.

The passive-delay elements are packaged, along with their 1C circuit terminations, on card type DC. This card contains a total of five delay elements (with the values of the delays specified according to logic requirements) and five 1C circuit terminations, plus five additional 1C circuits with varying numbers of input connections provided. The input connection to the delay element may be obtained directly from the adjacent 1C circuit on the same card or from another card by means of a separate input terminal connection. The number of input connections associated with each of the ten transistor circuit positions is given in table 1-2 under card type DC. The single inputs at positions 1, 3, 5, 7, and 9 refer to the separate delay-element inputs.

1-20. ACTIVE DELAY

An active delay element is required whenever there is the need to combine logic and delay functions at the same point in a circuit. Active delays of from 3 to 6 units can be obtained simply by placing passive delay elements of 1 to 4 units between two 1C gate inverters. An active delay of 2 is obtained more or less automatically by using two 1C circuits alone. An active delay of 1 is all that is necessary to make a complete set of delays from 1 to 6 units available. Thus the only unique active delay circuit required by the logic design is one that will give a delay of 1 unit while it permits more than one signal to be connected to its input.

1-21. RETRIGGERABLE DELAY FLOP

The retriggerable delay flop (RDF) is a form of flip-flop which has only one rather than two stable states, and which will provide storage for a definite rather than an indefinite period. In this sense the RDF is an active delay circuit which generates a linear ramp voltage of fixed time duration after the reception of an input signal. A regenerative switching circuit consisting of a transistor amplifier and transformer feedback loop is used in conjunction with an output R-C timing circuit to produce a ramp voltage of desired amplitude and time duration. In the Larc circuit logic the output from the RDF is restricted to delivery of an input to a Schmitt trigger circuit only—the ST-B or ST-C.* A combination RDF and ST-B circuit produces an output signal which is a delayed representation of the input. Pulse-stretching functions are produced by teaming an RDF with an ST-C circuit.

The retriggerable feature of the RDF circuit enables two kinds of delay action to take place within the circuit, depending on the interval between input signals. These actions are shown in figures 1-12a and 1-12b, where T is the interval between input signals and D is the total circuit-delay time of the RDF. It is evident that if a second input signal occurs before the end of the delay interval of the RDF, no change in output from the ST circuit will take place because of the first input. Thus the total delay of the ST-B output or the pulse width of the ST-C output will be determined either by a single trigger input signal or by the last of a series of retriggering input signals whose period is less than the delay of the RDF.

The RDF circuit has been designed to span a total delay range from 9 μs to 130 ms. (Refer to table 1-7.) The short-delay group is designated as an RDF-A circuit and is capable of producing delays ranging from 9 μs to 3.8 ms. The RDF-A circuit is further classified into eight subrange circuits in which some degree of overlapping of delay times is allowed between adjacent subranges. The long-delay group (RDF-B) includes five subrange circuits which provide delays ranging from 3.2 ms to 130 ms. The tolerance on a delay within any subrange is normally set at ±10 percent; however, a close tolerance of ±3 percent is obtained by adding voltage regulators to the circuit.

The schematic diagram of the complete RDF circuit is given in figure 1-13. The circuit is divided into four parts according to function; they are referred to as the (1) triggering circuit, (2) regenerative switching circuit, (3) timing circuit, and (4) voltage-regulating circuit. As shown by the broken connection lines (jumpers A and B), the voltage-regulating circuit is optional and depends on the degree of tolerance desired. The broad span is achieved by the type of transformer (T1) and transistor (Q2), and components R2, R4, R10, and C, the values of which will vary according to the desired circuit delay—that is, according to the two basic groups referred to as the short-delay group and the long-delay group. (Refer to tables 1-7 and 1-8.)

* Since a total of five different types of Schmitt trigger circuits are used in the Larc circuit logic, the types will be described separately under headings 1-22 through 1-27. However, note that an RDF may be connected only to an ST-B or ST-C type circuit.

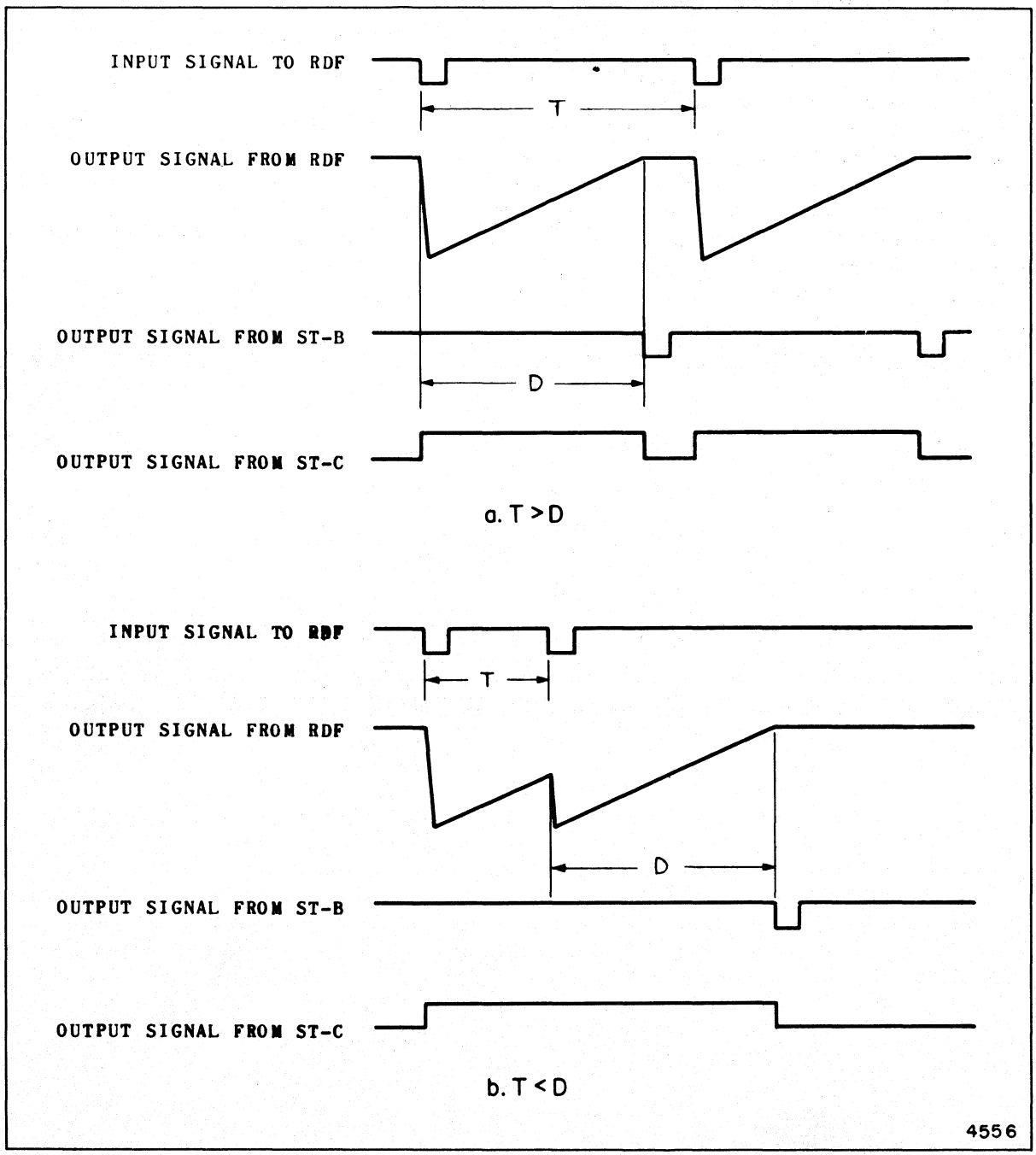


Figure 1-12. RDF Triggering Conditions

The active delay element is shown in block form in figure 1-11b. It is composed of two cascaded type-1C circuits which are exactly the same as the standard gate inverter (figure 1-1). Obviously this circuit can be considered to have a minimum total delay time of 2 units, but special conditions are required to limit the maximum delay to less than 40 mμs across the two circuits. The conditions are these:

(1) Transistors are selected for maximum over-all speed.

Table 1-7. Variation in Values of Components of Retriggerable Delay Flop Circuits

R8, R10: values to be determined by specific delay time (table 1-8)
RDF card: contains two circuits per card and requires two card spaces in backboard

Circuit Types		Delay Range t (μs)		R2 (KΩ)	R4 (Ω)	C (μf)	Q2 (Type 2N247)	T1 Type	RDF Card Type
Tolerance									
±10%	±3%	From	To						
Short-Delay Group (RDF-A)									
A1	A2	9	18	39	22	0.0022	RT53	MT63	RA
B1	B2	15	38	39	22	0.0047	RT53	MT63	RA
C1	C2	32	80	39	10	0.01	RT53	MT63	RA
D1	D2	70	180	39	10	0.022	RT53	MT63	RA
E1	E2	150	380	39	10	0.047	RT53	MT63	RA
F1	F2	320	800	39	0	0.1	RT53	MT63	RA
G1	G2	700	1800	39	0	0.22	RT53	MT63	RA
H1	H2	1500	3800	39	0	0.47	RT54	MT63	RA
Long-Delay Group (RDF-B)									
I1	I2	3200	8000	50	0	1.0	RT53	MT62	RB
J1	J2	7000	16,000	50	0	2.0	RT53	MT62	RB
K1	K2	14,000	32,000	50	0	4.0	RT53	MT62	RB
L1	L2	28,000	64,000	50	0	8.0	RT53	MT62	RB RC*
M1	M2	60,000	130,000	50	0	16.0	RT54	MT62	RB RC*
Special Variable Unit**									
X1	X2	200	100,000	50	0	†	RT54	MT62	RB

* RC circuit contains additional timing capacitors required for use with RDF-B type-L and -M long-delay (over 20 ms) circuits.

** For use as a variable-frequency generator.

† Variable.

(2) Transistors Q1 and Q2 are mounted on the same card so that there is no excessive wiring capacity on the first stage.

(3) Q1 is permitted to drive a constant load.

(4) The maximum load on Q2 is limited to one 1C circuit (or three 1E circuits).

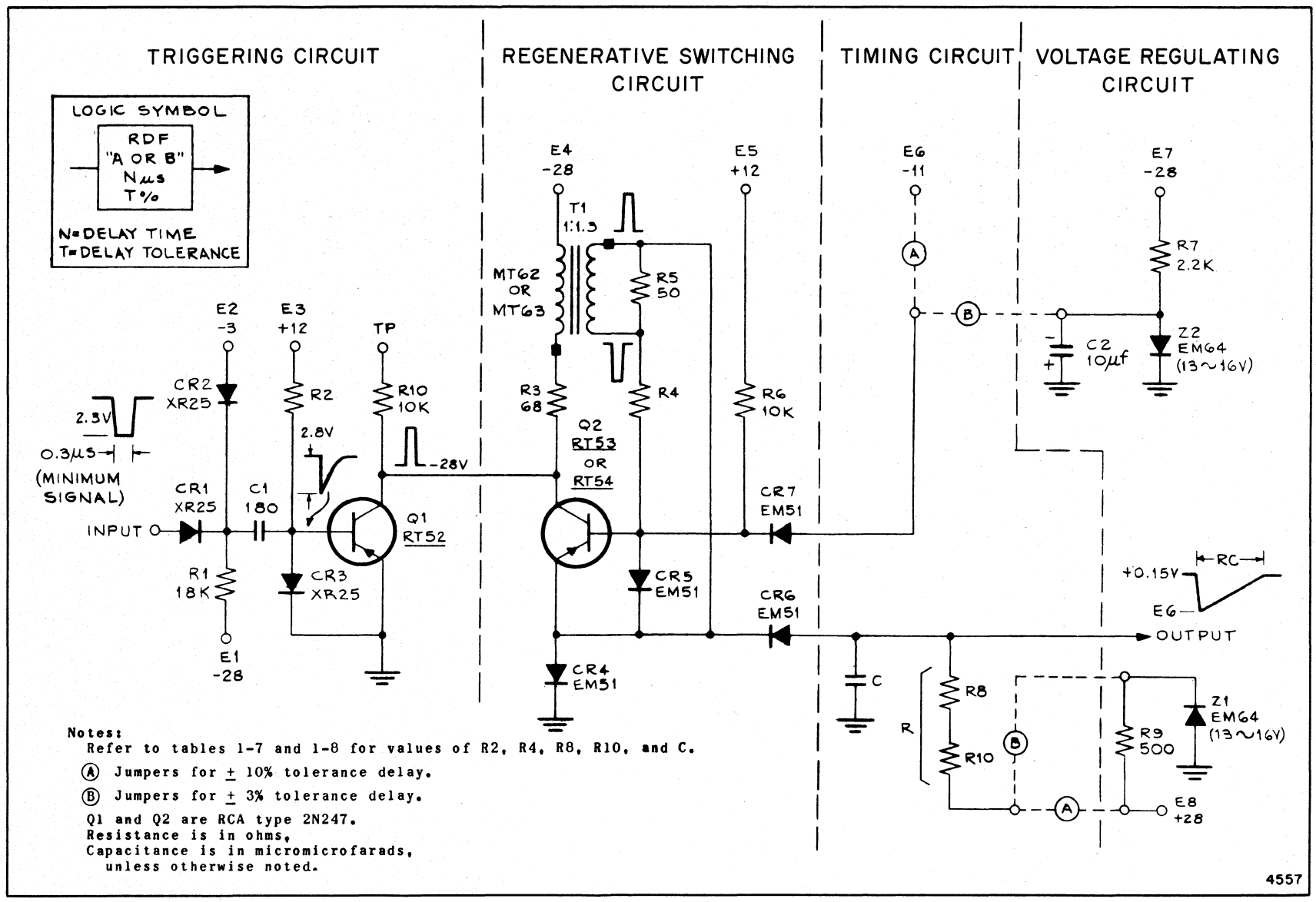


Figure 1-13. Retriggerable Delay Flop

For condition (1) the best results are obtained by combining a fast-rise-time transistor for Q1 with a low-storage-time unit for Q2. Condition (4) is an acceptable logical specification. As indicated by the logic symbol, the active delay element may be counted as 1 or 2 units of delay, and the double-inversion properties of the circuit produce the same signal polarities at the input and output. For logical gating functions up to six inputs may be connected to the input of the first stage.

For the triggering action, transistors Q1 and Q2 both are normally cut off because of the forward drops across diodes CR3 and CR5; CR3 receives current from supply E3 via R2 and the CR5 from E5 via R6, with CR4 serving as a ground return. The drop across CR4 is about 0.6 v, which is sufficient to hold CR6 off; thus the output timing circuit (R8, R10, and C) is disconnected from the switching circuit, and the output voltage will be limited by the set level of the following Schmitt trigger circuit.

A negative-going step or pulse of at least 2.8-v amplitude and 0.3-μs duration will be differentiated by C1 and R2 to cause Q1 to be driven momentarily into the conduction region. This action causes the collector of Q1—and with it the collector of Q2—to rise in a positive direction to a voltage near ground potential. The triggering current flowing in the primary of transformer T1 is fed back to the base-emitter circuit of Q2 by way of the transformer secondary winding so as to bias the transistor in the forward direction. The circuit parameters are chosen so that the action becomes regenerative. The pulse at the base of Q1 is no longer necessary and may be removed with no effect on the cycle of operation.

During the regenerative process Q2 acts as a current-source generator drawing emitter current through C and CR6 since CR4 cannot pass current of this polarity. When the voltage across the capacitor is reduced to the potential level of E6 (or the regulated level established by the zener diode Z2), diode CR7 starts to conduct. The current from CR7 clamps the base of Q2 so that the negatively charging C, which continues to lower the emitter potential of Q2, automatically tends to reverse-bias the transistor, and the regeneration process stops. In addition, current from the clamp reduces the base current of Q2, thus further decreasing the regenerative action. As a result the circuit will return to steady-state conditions with transistor Q2 off and diodes CR5 and CR4 on. Diodes CR6 and CR7 then will open, and the timing circuit again will be disconnected from the switching circuit. The capacitor C now will begin to charge positively through resistors R8 and R10 toward the level of E8 (or the regulated level established by zener diode Z1). When the capacitor voltage again builds up to the set level of the Schmitt trigger circuit, the delay action of the RDF is complete.

The close-tolerance (±3-percent) delay times are achieved by connecting the voltage-regulating circuit across the d-c supplies of the timing circuit. The zener diode Z1 is used to regulate the charging voltage E8 while Z2 regulates the clipping voltage, where the higher E7 supply is substituted for normal supply E6. Diodes Z1 and Z2 are both type-EM64 zener diodes with an initial tolerance on breakdown voltage of between 13 and 16 v; the nominal value is 15 v. With these diodes the regulating circuit is capable of supplying enough current to two RDF circuits; that is, the addition of only one regulating circuit is needed for every two RDF circuits requiring 3-percent tolerances.

The total delay time of the RDF can be approximated by calculating the charging time of capacitor C in terms of the exponential voltage $1 - \varepsilon^{-t/T}$, where t is the delay interval and T the RC time constant (R = R8 + R10). Thus the time required for C to charge from its initial voltage ($E_{initial} = E_6$ or E_{Z2}) toward its steady-state voltage ($E_{supply} = E_8$ or E_{Z1}) is this:

$$\frac{E_{initial}}{E_{supply}} = 1 - \varepsilon^{-t/RC}$$

$$\therefore\ t = (RC)\ \ln\left(\frac{E_{initial} + E_{supply}}{E_{supply}}\right)$$

The values of t and C for each subrange circuit type are given in table 1-7. In the specification of a delay for a particular application, R is calculated from the preceding equation and a pair of suitable resistors (R8 and R10) are selected according to the resistance chart given in table 1-8. For example, the desired delay is 100 μs and the tolerance is to be ±10 percent; according to table 1-7, C will equal 0.022 μf. Therefore

$$R = \frac{t}{(C)\ \ln\left(\frac{11\text{ v} + 28\text{ v}}{28\text{ v}}\right)}$$

$$= \frac{100 \times 10^{-6}}{0.022 \times 10^{-6}\ (0.33)} = \frac{100}{0.00726} = 13.8\text{ K}$$

According to table 1-8, R8 is 5.6 kilohms and R10 is 8.2 kilohms, or 1.8 and 12.0 kilohms.

The other variable components (R2, R4, T1, and Q2) in the circuit are chosen according to whether the RDF is intended for use in the short- or long-delay group. As shown in table 1-7, the bias resistor R2 (at the base of Q1) has a value of 39 kilohms for the short-delay group and 50 kilohms for the longer-delay group. The larger resistance is needed because of the lower transistor-power dissipations encountered with the larger input-signal intervals of the longer delays. R4, T1, and Q2 are chosen to provide optimum operating parameters for the regenerative switching circuit.

Table 1-8. Resistance-Combination Totals for Two Series Resistors (R8, R10) in Timing Circuit of Retriggerable Delay Flop*

Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)	Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)
3.3	1.5	1.8	5.0	2.5	2.5
	1.3	2.0		2.0	3.0
3.4	1.2	2.2	5.1	1.8	3.3
				1.2	3.9
3.5	1.3	2.2			
	1.0	2.5	5.2	2.2	3.0
	1.5	2.0		2.5	2.7
				1.3	3.9
3.52	0.82	2.7			
			5.3	2.0	3.3
3.6	1.8	1.8			
			5.4	2.7	2.7
3.7	1.0	2.7		1.5	3.9
	1.2	2.5			
	1.5	2.2	5.5	2.5	3.0
				2.2	3.3
3.8	1.8	2.0			
	1.3	2.5	5.52	0.82	4.7
3.82	0.82	3.0	5.7	2.7	3.0
				1.8	3.9
3.9	1.2	2.7		1.0	4.7
4.0	2.0	2.0	5.8	2.5	3.3
	1.8	2.2			
	1.5	2.5	5.82	0.82	5.0
	1.3	2.7			
	1.0	3.0	5.9	2.0	3.9
				1.2	4.7
4.12	0.82	3.3			
			6.0	3.0	3.0
4.2	2.0	2.2		2.7	3.3
	1.5	2.7		1.3	4.7
	1.2	3.0		1.0	5.0
4.3	1.8	2.5	6.1	2.2	3.9
	1.3	3.0			
	1.0	3.3	6.2	1.5	4.7
				1.2	5.0
4.4	2.2	2.2			
			6.3	3.0	3.3
4.5	2.0	2.5		1.3	5.0
	1.8	2.7			
	1.5	3.0	6.4	2.5	3.9
	1.2	3.3			
			6.42	0.82	5.6
4.6	1.3	3.3			
			6.5	1.5	5.0
4.7	2.2	2.5		1.8	4.7
	2.0	2.7			
			6.6	3.3	3.3
4.72	0.82	3.9		2.7	3.9
				1.0	5.6
4.8	1.8	3.0			
	1.5	3.3	6.7	2.0	4.7
4.9	1.0	3.9	6.8	1.8	5.0
	2.2	2.7		1.2	5.6

* $R8 + R10 = R = \frac{t}{C \cdot \ln\left(\frac{E_{initial} + E_{supply}}{E_{supply}}\right)}$

Table 1-8. Resistance-Combination Totals for Two Series Resistors (cont.)

Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)	Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)
6.9	3.0	3.9	9.5	3.9	5.6
	2.2	4.7		2.7	6.8
	1.3	5.6		2.0	7.5
				1.3	8.2
7.0	2.0	5.0			
			9.7	4.7	5.0
7.1	1.5	5.6		2.2	7.5
				1.5	8.2
7.2	3.3	3.9			
	2.5	4.7	9.8	3.0	6.8
	2.2	5.0			
			10.0	5.0	5.0
7.4	2.7	4.7		2.5	7.5
	1.8	5.6		1.8	8.2
7.5	2.5	5.0	10.1	3.3	6.8
7.6	2.0	5.6	10.2	2.7	7.5
				2.0	8.2
7.62	0.82	6.8			
			10.3	4.7	5.6
7.7	3.0	4.7			
	2.7	5.0	10.4	2.2	8.2
7.8	3.9	3.9	10.5	3.0	7.5
	2.2	5.6			
	1.0	6.8	10.6	5.0	5.6
8.0	3.3	4.7	10.7	3.9	6.8
	3.0	5.0		2.5	8.2
	1.2	6.8			
			10.8	3.3	7.5
8.1	2.5	5.6			
	1.3	6.8	10.82	0.82	10.0
8.3	3.3	5.0	10.9	2.7	8.2
	2.7	5.6			
	1.5	6.8	11.0	1.0	10.0
8.32	0.82	7.5	11.2	5.6	5.6
				3.0	8.2
8.5	1.0	7.5		1.2	10.0
8.6	3.9	4.7	11.3	1.3	10.0
	3.0	5.6			
	1.8	6.8	11.4	3.9	7.5
8.7	1.2	7.5	11.5	4.7	6.8
				3.3	8.2
8.8	2.0	6.8		1.5	10.0
	1.3	7.5			
			11.8	5.0	6.8
8.9	3.9	5.0		1.8	10.0
	3.3	5.6			
			12.0	2.0	10.0
9.0	2.2	6.8			
	1.5	7.5	12.1	3.9	8.2
9.02	0.82	8.2	12.2	4.7	7.5
				2.2	10.0
9.2	1.0	8.2			
			12.4	5.6	6.8
9.3	2.5	6.8			
	1.8	7.5	12.5	5.0	7.5
				2.5	10.0
9.4	4.7	4.7			
	1.2	8.2			

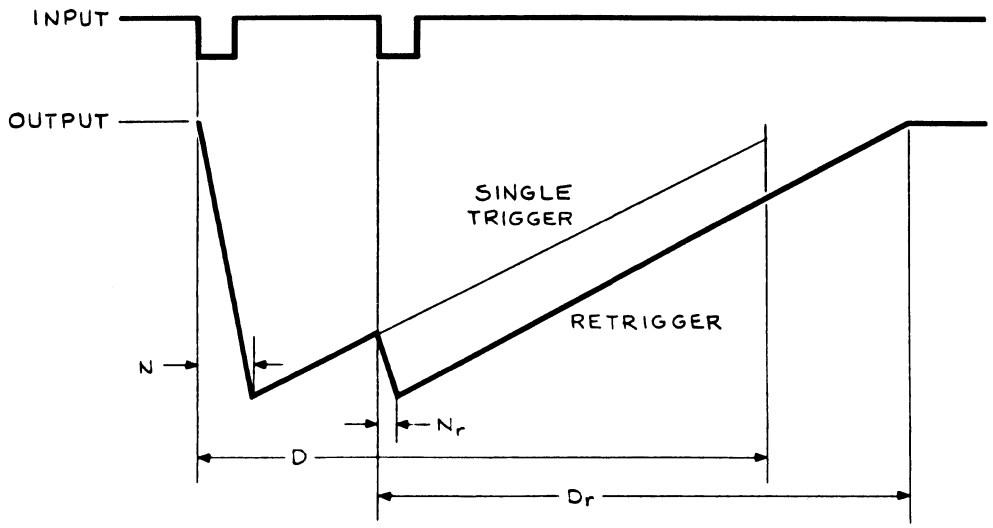
Table 1-8. Resistance-Combination Totals for Two Series Resistors (cont.)

Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)	Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)
12.7	2.7	10.0	16.0	3.0	13.0
				1.0	15.0
12.82	0.82	12.0			
			16.2	1.2	15.0
12.9	4.7	8.2			
			16.3	3.3	13.0
13.0	3.0	10.0		1.3	15.0
	1.0	12.0			
			16.4	8.2	8.2
13.1	5.6	7.5			
			16.5	1.5	15.0
13.2	5.0	8.2			
	1.2	12.0	16.7	4.7	12.0
13.3	3.3	10.0	16.8	6.8	10.0
	1.3	12.0		1.8	15.0
13.5	1.5	12.0	16.9	3.9	13.0
13.6	6.8	6.8	17.0	5.0	12.0
				2.0	15.0
13.8	5.6	8.2			
	1.8	12.0	17.2	2.2	15.0
13.82	0.82	13.0	17.5	7.5	10.0
				2.5	15.0
13.9	3.9	10.0			
			17.6	5.6	12.0
14.0	2.0	12.0			
	1.0	13.0	17.7	4.7	13.0
				2.7	15.0
14.2	1.2	13.0			
	2.2	12.0	18.0	5.0	13.0
				3.0	15.0
14.3	6.8	7.5			
	1.3	13.0	18.2	8.2	10.0
14.5	2.5	12.0	18.3	3.3	15.0
	1.5	13.0			
			18.6	5.6	13.0
14.7	4.7	10.0			
	2.7	12.0	18.8	6.8	12.0
14.8	1.8	13.0	18.82	0.82	18.0
15.0	7.5	7.5	18.9	3.9	15.0
	6.8	8.2			
	5.0	10.0	19.0	1.0	18.0
	3.0	12.0			
	2.0	13.0	19.2	1.2	18.0
15.2	2.2	13.0	19.3	1.3	18.0
15.3	3.3	12.0	19.5	7.5	12.0
				1.5	18.0
15.5	2.5	13.0			
			19.7	4.7	15.0
15.6	5.6	10.0			
			19.8	6.8	13.0
15.7	7.5	8.2		1.8	18.0
	2.7	13.0			
			20.0	10.0	10.0
15.82	0.82	15.0		5.0	15.0
				2.0	18.0
15.9	3.9	12.0			

Table 1-8. Resistance-Combination Totals for Two Series Resistors (cont.)

Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)	Total Resistance (KΩ)	R8 (KΩ)	R10 (KΩ)
20.2	8.2	12.0	23.5	1.5	22.0
	2.2	18.0			
			23.6	5.6	18.0
20.5	7.5	13.0			
	2.5	18.0	23.8	1.8	22.0
20.6	5.6	15.0	23.9	3.9	20.0
20.7	2.7	18.0	24.0	12.0	12.0
				2.0	22.0
20.82	0.82	20.0			
			24.2	2.2	22.0
21.0	3.0	18.0			
	1.0	20.0	24.5	2.5	22.0
21.2	1.2	20.0	24.7	4.7	20.0
	8.2	13.0		2.7	22.0
21.3	3.3	18.0	24.8	6.8	18.0
	1.3	20.0			
			25.0	12.0	13.0
21.5	1.5	20.0		10.0	15.0
				5.0	20.0
21.8	6.8	15.0		3.0	22.0
	1.8	20.0			
			25.3	3.3	22.0
21.9	3.9	18.0			
			25.5	7.5	18.0
22.0	10.0	12.0			
	2.0	20.0	25.6	5.6	20.0
22.2	2.2	20.0	25.9	3.9	22.0
22.5	7.5	15.0	26.2	8.2	18.0
	2.5	20.0			
			26.7	4.7	22.0
22.7	4.7	18.0			
	2.7	20.0	26.8	6.8	20.0
22.82	0.82	22.0	27.0	12.0	15.0
				5.0	22.0
23.0	10.0	13.0			
	5.0	18.0	27.5	7.5	20.0
	3.0	20.0			
	1.0	22.0	27.6	5.6	22.0
23.2	8.2	15.0	28.0	10.0	18.0
	1.2	22.0			
			28.2	8.2	20.0
23.3	3.3	20.0			
	1.3	22.0	28.8	6.8	22.0

The time required to charge capacitor C negatively depends on the circuit parameters and the triggering conditions. The variation in this charge time, and therefore the circuit delay, is related to the triggering input conditions as shown here.



N : NEGATIVE CHARGE
D : TOTAL DELAY
D > Dr
Dr and Nr : RETRIGGERED CONDITIONS

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The preceding drawing shows the input and output waveforms of the RDF timing circuit and the variations in total delay time due to triggering conditions. In order to minimize the variations, the timing capacitor must be charged in the negative direction as fast as possible; that is, making $(D - N) >> N$ and $(D_r - N_r) >> N_r$ causes the variation in delay with triggering conditions to be small. For the shorter delays the leakage inductance of T1 is a controlling factor in the rise time of the negative charge current from C. For the longer delays (larger capacitors) the negative charge time is controlled more by C than by the leakage inductance, provided that the magnetizing inductance of T1 is large enough to prevent saturation of the transformer during the longer charge time. Consequently, a different transformer is provided for the two delay groups. The short-delay unit (type MT63) has low-leakage inductance to give maximum speed and stability to the circuit, whereas the long-delay unit (type MT62) has been designed for maximum effective magnetizing inductance.

Transistor TR2 is an RT53 unit (type 2N247) with a current gain of 10, and is satisfactory for most of the RDF circuit types. However, for the longest-delay units in each delay group a higher beta unit, RT54 ($\beta = 15$), is needed to counteract the current loss in the magnetizing inductance of T1.

For the long-delay group which has larger capacitors in the timing circuit the conducting period of Q2 is long enough to allow the magnetizing current to reverse from its steady-state direction determined by the drop

across CR5; thus, when the regeneration process stops, the recovery of T1 automatically reverse-biases Q2. However, for the shorter delays the conducting period is not long enough to reverse the magnetizing current, and as a result the transformer recovery tends to keep the transistor conducting. To prevent this from happening, resistance R4 is connected between the base of Q2 and the secondary of T1 in the shorter-delay circuits.

As indicated in table 1-7, a special variable RDF unit (type X) is available for use as a variable-frequency generator. This circuit provides a delay range from 200 to 100,000 μs by making the value of the timing capacitor variable over a series of steps.

The RDF printed-circuit-card types are designated RA for the short-delay group (logic symbol: RDF-A) and RB for the long-delay group (RDF-B). Because of the size of the transformer (T1) and some of the capacitors, an RDF card requires two card spaces in the backboard. Each card type contains two basic RDF circuits, as shown in figure 1-13, with provisions for adding one voltage-regulating circuit and for removing the timing-circuit components (R8, R10, and C).

Also as indicated in table 1-7, the type-RC circuit is mounted on a separate card and contains extra timing capacitors for use with two of the RDF long-delay circuits (type L and M), where the required delay is greater than 28 ms. Each RC circuit (two circuits per card) contains three 4-μf capacitors, so that additional timing capacity totaling 4, 8, or 12 μf may be connected in parallel with capacitor C on an RB card.

1-22. SCHMITT TRIGGERS

The Schmitt trigger circuit is used to convert signals which are not in digital form into a suitable d-c level or rectangular pulse as required by the circuit logic. Basically a Schmitt trigger (ST) is a bistable circuit which has this property: an output of constant peak value is obtained for the period during which the input waveform exceeds a specific voltage. As used here, the circuit detects the fact that a positive-going sinewave or linear ramp voltage at its input has reached, or is very close to, the level of ground potential. At this point the circuit is set and will produce a significant output pulse or level. Subsequent changes in output cannot take place until the variable input signal has swung in a negative direction below the reset level of the Schmitt trigger.

A simplified block diagram of the Schmitt trigger circuits used in the logic networks is shown in figure 1-14. The first two stages are transistor switching circuits that form a conventional bistable Schmitt-trigger arrangement. The first stage (Q1) is conducting with the following stage (Q2) off when the input is below the reset level. When the positive-going input ramp or sinewave reaches the set level, Q1 is cut off, and Q2 starts to conduct. The output current from Q2 is fed into the impedance-coupling network (Z), which drives the output stage Q3. Depending on whether Z is an a-c or d-c device, the normally conducting Q3 will be cut off for a very short time to produce a negative-going output pulse, or for a longer time to produce a d-c level proportional to the time that the circuit is set.

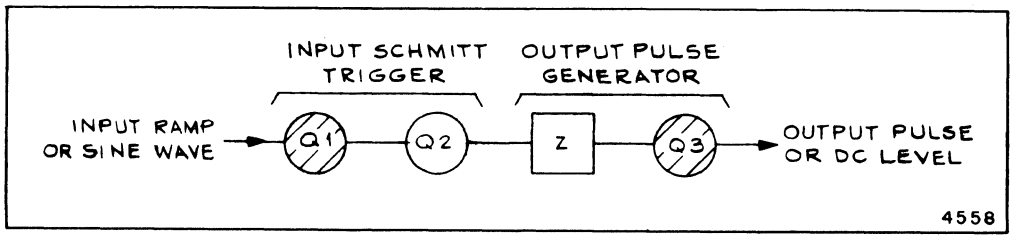


Figure 1-14. Schmitt Trigger, Block Diagram

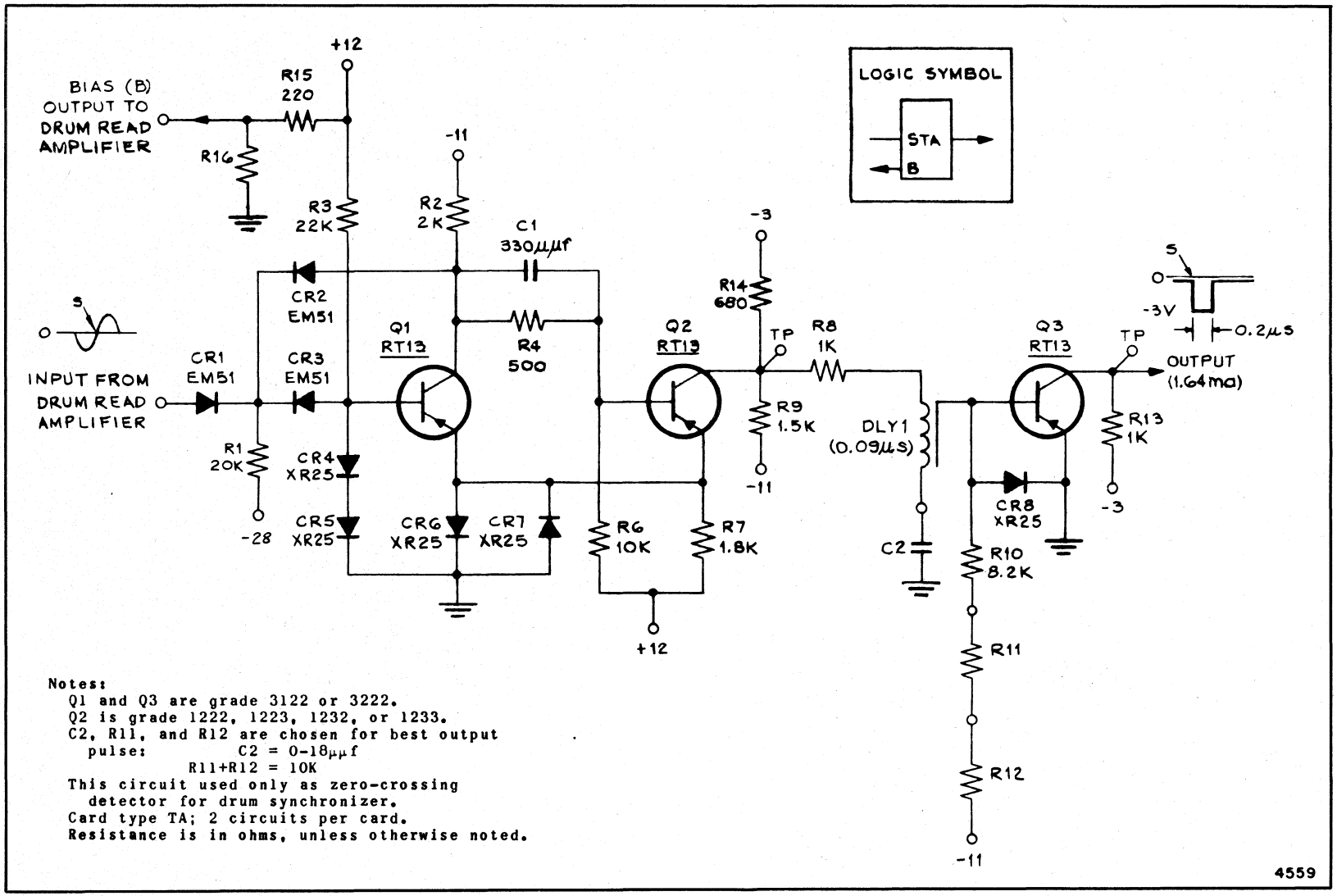
The ST circuits are used to convert sinusoidal inputs from drum and tape read amplifiers, or ramp signals from retriggerable delay flops, into the 3-v levels of the Larc logic. However, input and output signal requirements for the various applications are such that a total of five different types of ST circuits are used in the system (ST-A, -B, -C, -D, and -E). The principles of operation of each of the circuit types are basically the same, and therefore only the first (ST-A) will be described completely in detail. The descriptions of the other types will cover only the differences in the circuit as compared with type ST-A. The schematic diagrams, including information on transistor grades* and card types for each of the circuits, are given in figures 1-15 through 1-19.

1-23. TYPE-ST-A CIRCUIT

The ST-A Schmitt trigger type circuit is used only in the self-sprocketing logic of drum synchronizers to convert the sinusoidal output of a drum read amplifier to a carefully timed 0.2-μs negative output pulse. An output pulse is produced by the ST-A circuit to set an asynchronous (type-1S) flip-flop each time the input sinewave crosses the zero axis in a positive direction. For this reason the circuit is also known as a zero-crossing detector. The coupling impedance between the input Schmitt trigger circuit and the output pulse generator is an a-c device in the form of an open-circuited delay line. The schematic diagram is given in figure 1-15.

Input stages Q1 and Q2 form the Schmitt trigger portion of the circuit. Q1 is normally biased to the conduction state, in which the base current is limited to the difference between the pull-down current through R1 and the pull-up current through R3. A biasing potential (B) for the drum read amplifier is fed back from the ST-A through the voltage divider consisting of R15 and R16. This biasing voltage originates in the ST-A circuit so that the output waveform from the drum read amplifier can be centered around the trigger or set level (S) of the ST-A. In operation the value of R16 is selected to give the best results for a particular amplifier-Schmitt-trigger combination. With Q1 conducting, its collector voltage will be positive, keeping Q2 off. Because of the open circuit (for dc) presented by the delay line DLY 1, the steady-state output of Q2 will have no effect on the base of Q3. Since Q3 is biased on, the output level will be high (-0.3-v); the circuit is in the reset state. These

* All transistors used in the Schmitt trigger circuits, except the input stage of ST-D, are the surface-barrier type RT13 (Philco type SB100). Grade numbers refer to speed and gain selection groups.



Notes:
Q1 and Q3 are grade 3122 or 3222.
Q2 is grade 1222, 1223, 1232, or 1233.
C2, R11, and R12 are chosen for best output pulse: C2 = 0-18μμf
R11+R12 = 10K
This circuit used only as zero-crossing detector for drum synchronizer.
Card type TA; 2 circuits per card.
Resistance is in ohms, unless otherwise noted.

Figure 1-15. Type-ST-A Circuit

conditions will prevail with no input signal or for the negative alternations of the sinewave input.

When a positive-going input signal from the drum read amplifier approximates the zero reference level, input diode CR1 will conduct, and the resulting positive potential will cause Q1 to cut off. This action corresponds to the setting of the Schmitt trigger and occurs whenever a positive-going signal attains a potential in the range of -0.25 to +0.15 v (called the set band). Resetting occurs for negative-going signals in the range of -0.45 to -0.85 v (the reset band). The two bands are not independent, however; to insure setting and resetting, a level shift of at least 0.75 v is required, although in some instances this may occur within a difference as small as 0.40 v.

When Q1 reaches cutoff, the collector-to-emitter voltage swings negative and Q2 conducts. The emitter voltage swing of the two transistors is limited and controlled by clamping diodes CR6 and CR7. The internal voltage drops across these diodes determine the emitter voltage swing and the limits of the set and reset bands; therefore it is desirable to maintain the current in each above a minimum level so that any variation in drop is held within a reasonably small range. The resistance of R7 is chosen according to the minimum current condition in CR6 (about 1 ma) when Q1 is conducting; R14 and R9 are chosen similarly for minimum CR7 current when Q2 is conducting.

Diodes CR1 and CR3 effectively decouple the input signal from the base of Q1, while the series-connected diodes CR4 and CR5 limit the reverse-bias voltage at the base. Nonlinear feedback is provided by diode CR2 in order to reduce variations in delay in the operation of the circuit. The coupling circuit between Q1 and Q2 uses type-RT13 transistors and is designed for optimum switching speed without excessive power dissipation. On this basis the collector currents of Q1 and Q2 are about 5 ma and 10 ma, respectively. The required gains for the two stages, then, are about 9 for Q1 (beta selection group 3 transistor) and about 5 for Q2 (group 1 transistor).

The output stage (Q3) is normally conducting by means of the forward current through R10. When Q2 suddenly switches on, its collector voltage swings in a positive direction such that a reverse current is forced into the base of Q3. The output stage will then be cut off for a period equal to twice the delay time (0.09 μs) of the distributed-parameter delay line DLY 1.* Thus an output negative-going pulse with a duration of about 0.2 μs will be generated at the collector of Q3.

Resistance R8, in conjunction with the voltage divider of R9-R14, terminates the input of the delay line so that secondary reflections do not occur. Diode CR8 maintains a low load impedance on the delay line while Q3 is cut off thus allowing the full input swing to be across the delay line rather than across the transistor. The equivalent voltage of the R9-R14 divider is about -5.5 v, which should be present at the test point (TP) at the collector of Q2 when the circuit is in the reset state (Q2 off). The same point will be near ground potential when the circuit is triggered on.

* The total delay from the time of the step voltage output of Q2 until Q3 returns to the conducting state is equal to the rise time of the delay line plus the equivalent fall time (2 x 0.09 = 0.18 μs).

The width of the output pulse from the ST-A is critical. Because of component tolerances it is necessary to have a means available for adjusting the width of the 0.2-μs pulse to an accuracy of ±5 percent. As shown in figure 1-15, resistors R11 and R12 and capacitor C2 are selected for making the adjustment. If the values of these components are changed within the ranges indicated, the base current of Q3 will vary sufficiently to cause an effective variation in width of output pulse of approximately 14 percent. In operation the values of resistors R11 and R12 are selected (up to a maximum total of 10 kilohms) to produce the pulse width within the ±5-percent tolerance with a single type 1S-B gate inverter load connected to the output. (The maximum load current of the ST-A is 1 drive unit: 1.64 ma.) Small values of capacitance (up to 18 μμf) can be added in the C2 position to increase the amplitude of the pulse if it falls below -2.7 v. The presence of the extra capacity on the open end of the delay line causes to take place additional reflections which tend to increase the effective pulse width. Further, a small positive-going blip is created in the center of the output pulse because C2 presents a very low terminating impedance to the line when the input transient first arrives. The value of C2 must be such that this blip does not exceed 0.5 v in amplitude.

Since the Schmitt trigger is used in asynchronous logic only, inherent circuit delays are not relevant to the logical design of the system. However, for checking the transient response of these circuits, the total delay from an input zero crossing to the -1.2-v point on the output pulse should fall within the range of 30 mμs to 220 mμs.* The minimum delay condition for each circuit type should be measured with a 500-kc, 48-v peak-to-peak sinewave input and a fully loaded output. Maximum delay is measured at 250 kc, 6-v peak-to-peak sinewave and no load.

1-24. TYPE-ST-B CIRCUIT

The type-ST-B Schmitt trigger is shown in figure 1-16. It is evident that this circuit is essentially the same as the ST-A circuit described in detail under heading 1-23. In fact, the principle of operation of the entire circuit is exactly the same, and therefore only the slight modifications are covered here.

The ST-B circuit is intended to work only in combination with an RDF circuit (heading 1-21) to produce a negative-going output pulse which is a delayed representation of the RDF input. When the RDF is triggered on, the input to the ST-B drops below the reset level; the output remains high (-0.3 v). When the charging voltage across the timing capacitor in the RDF reaches the set point of the ST-B, the ST-B is triggered and a negative output pulse (3 v) is produced. The width of the output pulse is nominally 0.8 μs, but the tolerance is ±20 percent. For this reason the delay line DLY 1 has a rise time of 0.4 μs, and no fine pulse width adjustments (C2, R11, and R12, as in ST-A) are provided. The output-current level from Q3 (3.28 ma) is capable of driving two type-1C or -1S-A loads. For most applications, however, the RDF—ST-B delay network will be connected to a single pulser circuit (heading 1-28) to produce eventually a synchronized 0.5-μs pulse.

* This range of minimum-maximum delay times pertains to all circuit types except ST-A. Because of the presence of feedback diode CR2 (figure 1-15), the maximum delay of the ST-A should not be greater than 180 mμs. Refer to footnote of paragraph 6 under heading 1-23.

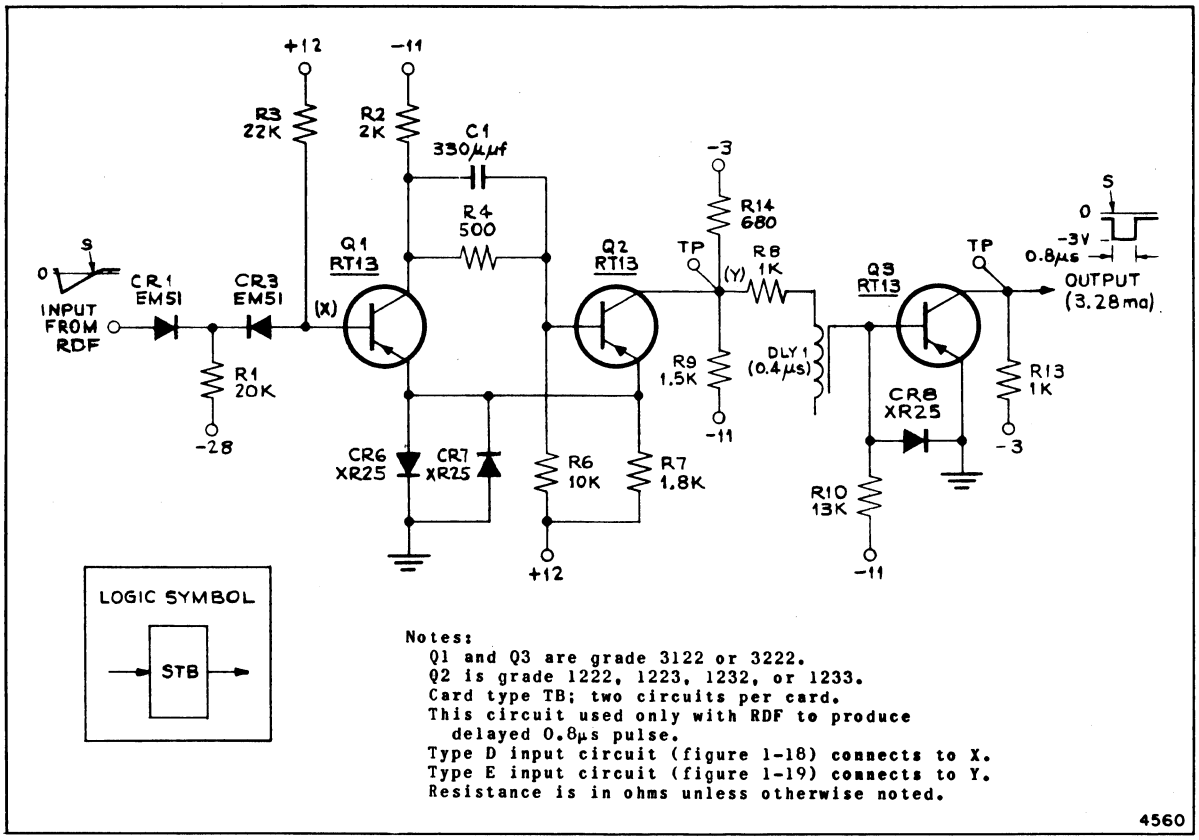


Figure 1-16. Type-ST-B Circuit

1-25. TYPE-ST-C CIRCUIT

The over-all purpose of the type-ST-C Schmitt trigger circuit is similar to the ST-B in that it is intended to work only in conjunction with an RDF. However, a combination RDF and ST-C produces a d-c level for an output which is effectively a widening of the input trigger pulse of the RDF (heading 1-21). As shown in figure 1-17, the Schmitt trigger portion of the circuit (Q1 and Q2) is identical to the ST-B, with the output transistor (Q3) d-c-coupled to Q2. This arrangement is similar to the conventional gate inverter (1C, 1E); therefore, when Q2 is not conducting, Q3 will be conducting, and the reverse. In fact, the entire output stage in the ST-C is practically the same as the standard 1C inverter (figure 1-1a). The series resistor (R8 in figure 1-17) is higher because of the higher driving voltage from Q2 in the ST-C circuit (-5.5 for ST-C as compared to -2.9 v for 1C). The output drive level, with 750-ohm dummy-load resistor R13, is also the same as the 1C: 3 drive units (4.92 ma).

In operation a negative trigger pulse at the input to the RDF will reset the ST-C circuit, producing a high output from Q3. The duration of this signal is equal to the delay time (D) of the RDF. At the end of this time the ST-C is set, Q3 is cut off, and the output drops to -3 v. The circuits remain in this state until another negative triggering pulse is received at the input to the RDF.

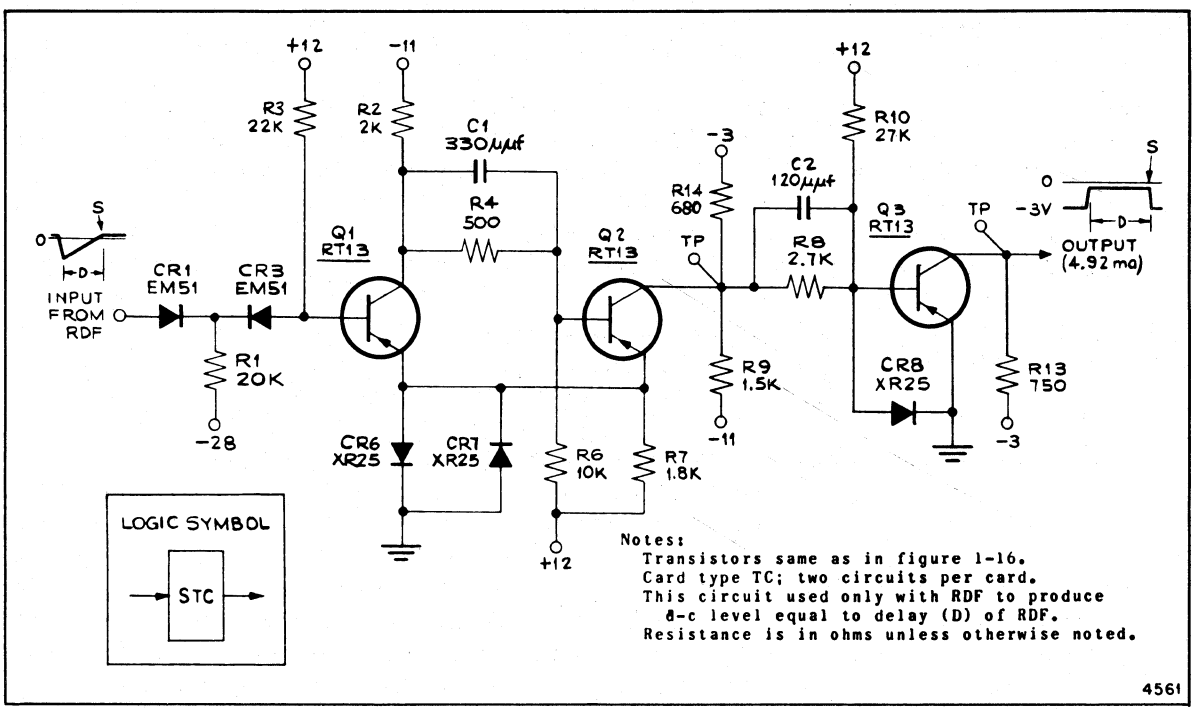


Figure 1-17. Type-ST-C Circuit

1-26. TYPE-ST-D CIRCUIT

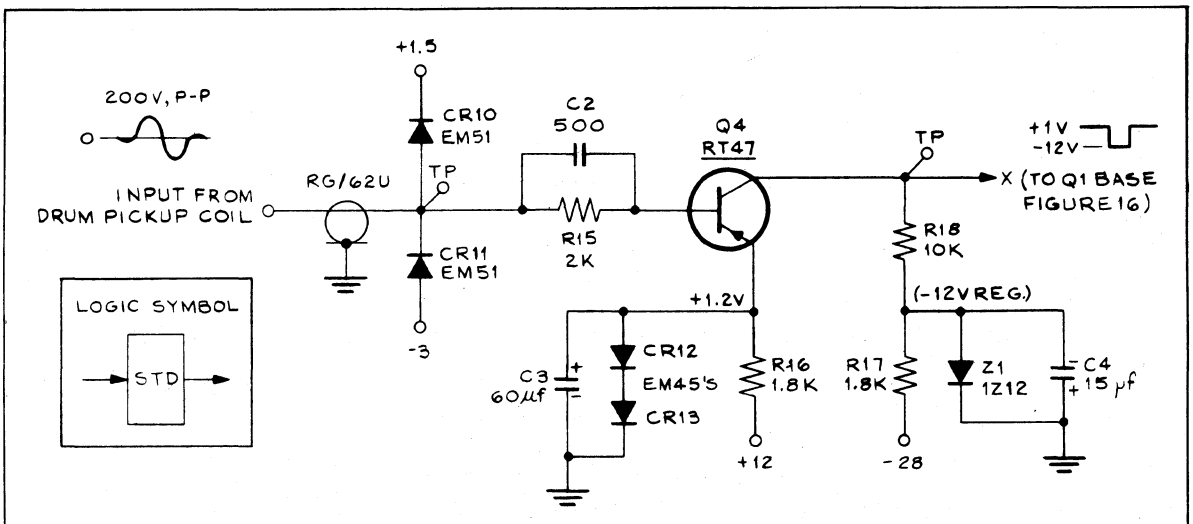
Another Schmitt trigger circuit that is used only in the drum synchronizer logic is the type ST-D. This circuit has been designed specifically to convert the once-per-revolution waveform from a drum into a negative-going pulse of fixed duration. The drum waveform is generated each time a permanent magnet imbedded in the drum end surface passes under a fixed pickup coil, and thus is used as a reference pulse to indicate each complete revolution of the drum. This arrangement is for use only during the write-sector-address mode of operation for the drum connected to the synchronizer.*

The required output from the ST-D circuit is a 3-v, negative-going, 0.8-μs pulse for each input reference waveform from the drum. Consequently the Schmitt trigger and output stages of this circuit are the same as those of the ST-B. However, an additional stage is included at the input of the ST-D to improve the over-all triggering characteristics of the circuit. This input stage is shown in figure 1-18. The input waveform from the pickup coil is transmitted over a coaxial cable which may be connected to any one of the drums in the system. The polarity of this signal is such that the positive-going portion will precede the negative. The pickup coil in the drum is specified as a 48-v cross-bar actuator coil, which has an impedance, at the frequency of the pulse output (2 kc), of about 20 kilohms.

* The write-sector-address mode of operation is implemented chiefly through drum write synchronizer 3. Consequently there is only one type of ST-D circuit in the entire system.

The input stage (Q4) of the ST-D uses a type RT47 transistor as a clipping amplifier. Q4 is normally conducting in the absence of an input signal by virtue of a positive emitter bias of about +1.2 v developed across diodes CR12 and CR13. The use of the diodes provides for better voltage regulation at the emitter than is obtained directly through R16 from the +12-v supply. With Q4 on, the output at the collector will be a d-c level of about +1 v. Thus the ST-B input circuit connected to point X will be in the set state. (The input coupling circuit of ST-B is eliminated because the output voltage swing of Q4 is within the ratings of the RT13.) Q1 is cut off while Q2 is conducting (figure 1-16). However, with no input from the drum Q3 is unaffected, and the output signal is near ground potential.

With the arrival of the positive-going input waveform from the drum, Q4 will be cut off and the potential at point X will drop to the level established by zener regulating diode Z1. The Schmitt-trigger portion of the circuit then will change state, and the transient current in the delay line (DLY 1, figure 1-16) will trigger off the output stage (Q3) to produce the negative-going 0.8-μs pulse. The clamp diodes, CR10 and CR11 limit the input voltage swing at the base of Q4 to 4.5 v. The voltage regulation provided by zener diode Z1 at the collector, and by diodes CR12 and CR13 at the emitter, help keep the drifts of the -28- and +12-v supply voltages well below the normal 4-percent level. It is necessary to maintain a close tolerance on the supply voltages in order to insure that the jitter figure for the output signal is low. The jitter problem results from the poor rise time of the signal waveform at both the input and output of the



Notes:
Q4 (RT47) is Raytheon type 2N428.
Remainder of circuit connects to X and is exactly the same as type B shown in figure 1-16.
Card type TD; one circuit per card but requires two card spaces in backboard.
This circuit used only to produce 0.8μs pulse from drum reference signal.
Coaxial input cable has maximum length of 150' and may be connected to any one of the 12 drums.
Capacitance is in micromicrofarads unless otherwise noted.

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Figure 1-18. Type-ST-D Input Stage

clipping amplifier. The large electrolytic capacitors C3 and C4 are shunted across the regulator circuits to attenuate further the supply-voltage noise, and to average out loading effects by the circuit.

1-27. TYPE-ST-E CIRCUIT

The ST-E circuit is modified from the ST-B to work in conjunction with a tape read amplifier. The circuit will convert a sinewave input from the amplifier into an 0.8-μs negative output pulse at 2 units of drive. It is used in both the tape read and on-line printer synchronizers to detect positive-going near-zero crossings of the input-signal waveforms. The term "near zero" is used to differentiate from the other Schmitt trigger circuits, since the ST-E circuit is biased so that the nominal set voltage occurs at about -0.2 v rather than at zero reference level. Consequently the tolerances on the set and reset bands for the ST-E are these:

Set band	-0.45 to -0.05 v
Reset band	-0.65 to -1.05 v

The input circuit of the ST-E is shown in figure 1-19. The output from the second stage (Q2) drives the delay line and output stage (Q3) of figure 1-16 as indicated at point Y in the two figures. The input coupling circuit of Q1 uses larger values of resistances than the corresponding parts of the ST-B circuit because of the larger signal voltages encountered at the output of the tape read amplifier. In addition, blocking input is provided (diode CR10) to insure that the ST-E is not set prematurely. The high blocking input must be applied continuously to the ST-E before the arrival of the tape-read signal waveforms so as to prevent spurious hash pulses from being interpreted as information signals.

The voltage divider consisting of R15 and R16 across the -3-v supply provides the offset (-0.2 v) bias at the emitter of Q1 so that triggering occurs below zero level. This offset bias level serves to stabilize the reset triggering time when high-resolution input signals are received from the tape. As shown in figure 1-19, this has the effect of moving the reset point (R) further down on the slope of the negative-going portion of the input waveform. Notice that two separate and distinct bias voltages are used to supply diodes D6 and D7.

1-28. SYNCHRONIZED SINGLE PULSER

The synchronized single pulser is a circuit configuration which is capable of converting an asynchronous input signal of any duration to a single 0.5-μs output pulse synchronized to the Larc clock. The circuit consists of two standard pulseformers (type P1) connected to each end of a special single-pulser delay element. The logical circuit arrangement is shown in figure 1-20a.

The nonsynchronous input from a pushbutton switch or delay flop is usually fed through a Schmitt trigger circuit (type ST-B or ST-C) to reset the first pulseformer; the positive output is low, and the negative high.

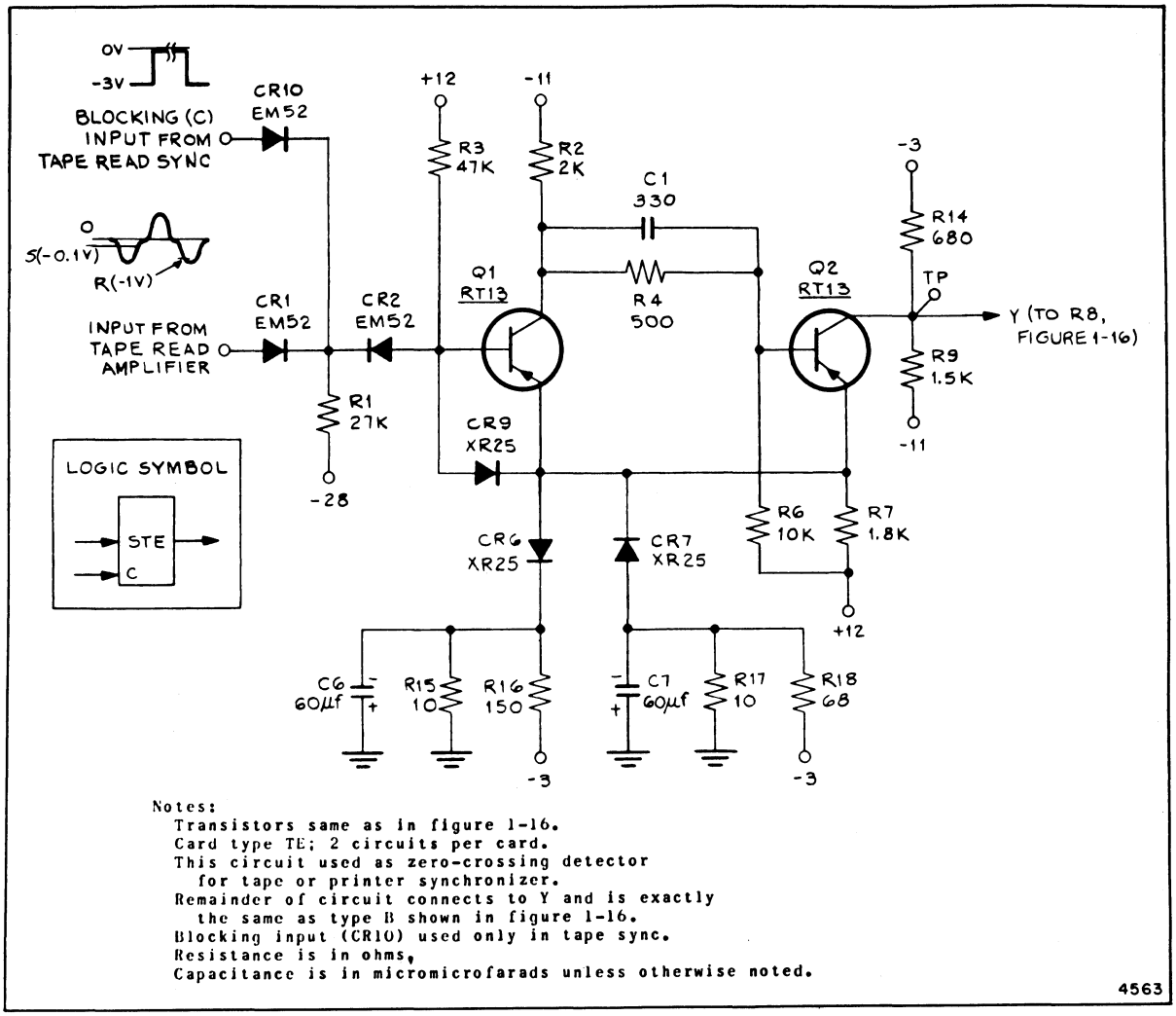


Figure 1-19. Type-ST-E Input Circuit

The output signals of opposite polarity are applied to the two parallel delay lines of D406 and D13, which are of about 0.3- and 0.7-μs duration, respectively. The shorter delay is a standard 1C-terminated delay element (type D406); the longer delay is a type DB single-pulser delay element which is terminated by a 1E inverter circuit. The outputs from the delay lines then are gated to reset the second pulseformer and thereby produce the desired synchronized output. The accompanying timing chart (figure 1-20a) shows the signal levels at points A through G and illustrates the operation and timing of the circuit. It is evident that the two different delays allow low inputs to the second pulseformer gate in only one clock-pulse time.

The only new circuit used in the complete single-pulser arrangement is the type-DB delay circuit shown in figure 1-20b. The delay line DLY is a distributed-constant type with a characteristic impedance (Z_0) of 2000 ohms and a delay time (T_d) of 0.59 μs. The delay line is a passive element, and therefore, in order to perform logical functions at the input

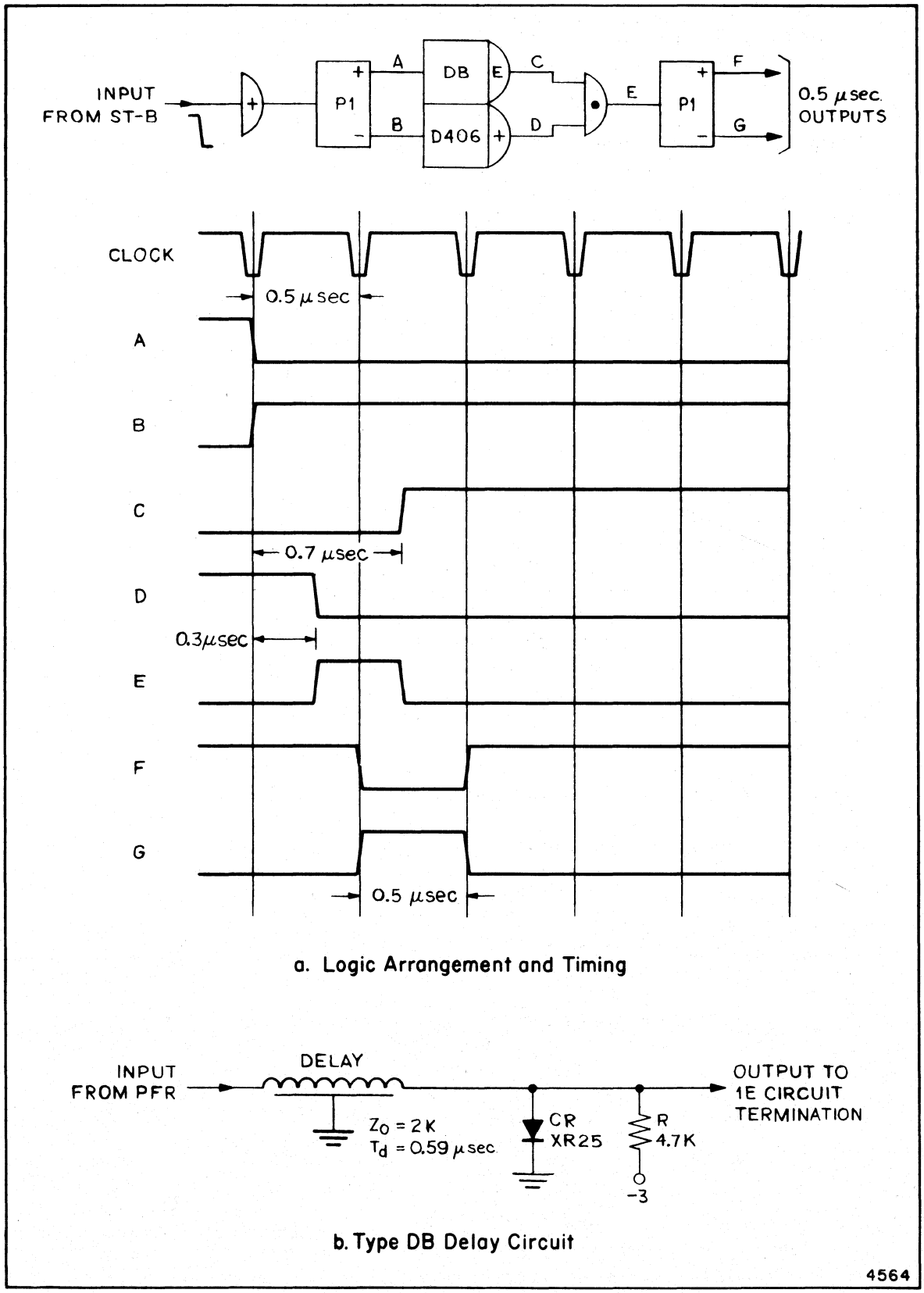


Figure 1-20. Synchronized Single Pulser

to the second pulseformer, it must be terminated in a gate-inverter circuit. Since a low-level 1E circuit (figure 1-2) is used to terminate the line (input impedance ≈ 5000 ohms), the parallel 4700-ohm resistor R is used to give a close impedance match to Z_0. The clamp diode CR limits the positive portion of ringing at the output of the line. Thus the total delay of the DB and 1E circuits (from A to C in figure 1-20a) is approximately 0.7 μs.

The shorter delay section uses a standard passive-delay element of the type described under heading 1-18. The total delay in the parallel path (B to D in figure 1-20a), then, is that of the type-D406 delay element and its 1C termination circuit—about 0.3 μs.

The single-pulser delay element is supplied as card type DB with two circuits per card—that is, two DB lines with two IE terminations, and two D406 lines with two 1C terminations. The outputs from the four transistors connect to another card for logic applications.

1-29. OUTPUT DRIVERS

Several different types of output driving circuits have been devised for amplifying the relatively low-power signals used in the logical circuits to the higher-power signals needed to drive such output control devices as magnets, solenoids, and vacuum tubes, and neon and incandescent indicator lamps. The differences between the types of drivers depend mainly on the kind of output device being driven and on the repetition rate of output signal. In general the drivers consist of a cascaded two-stage switching circuit which uses high-power transistors in one or both stages. Among the output drivers are (1) three low-speed units, types R1, R2, and R3, (2) a neon-indicator driver, type L, and (3) two vacuum-tube drivers, types VT and VC. Other output drivers have been developed specifically for use in the tape and printer synchronizers and are covered in the descriptions of these circuits.

1-30. TYPE-R1 AND -R3 LOW-SPEED DRIVER CIRCUIT

The types-R1 and -R3 circuits are so-called low-speed drivers used in applications in which the output current requirements are not in excess of 60 ma. The circuit for each, shown in figure 1-21, is capable of amplifying the 3-v input signals from the logic networks to a 48-v output level for driving relays, solenoids, or incandescent lamps. For the safe operation of the type-R1 circuit the repetition rate of the input signals must be limited by the logical-design application so that the interval between inputs to the driver is at least 25 ms.

It is convenient, in certain applications, to limit the input repetition rate to the low-speed driver by circuit modification instead of using logical means. The type-R3 circuit incorporates the necessary modification in the form of the 5-μf capacitor (C1) connected to the transistor base of the input stage. The bypass action to ground provided by this capacitor effectively limits the input rate to about 20 pulses per second, which is well within the region of safe operation. Except for C1, the type-R1 and -R3 circuits are identical.

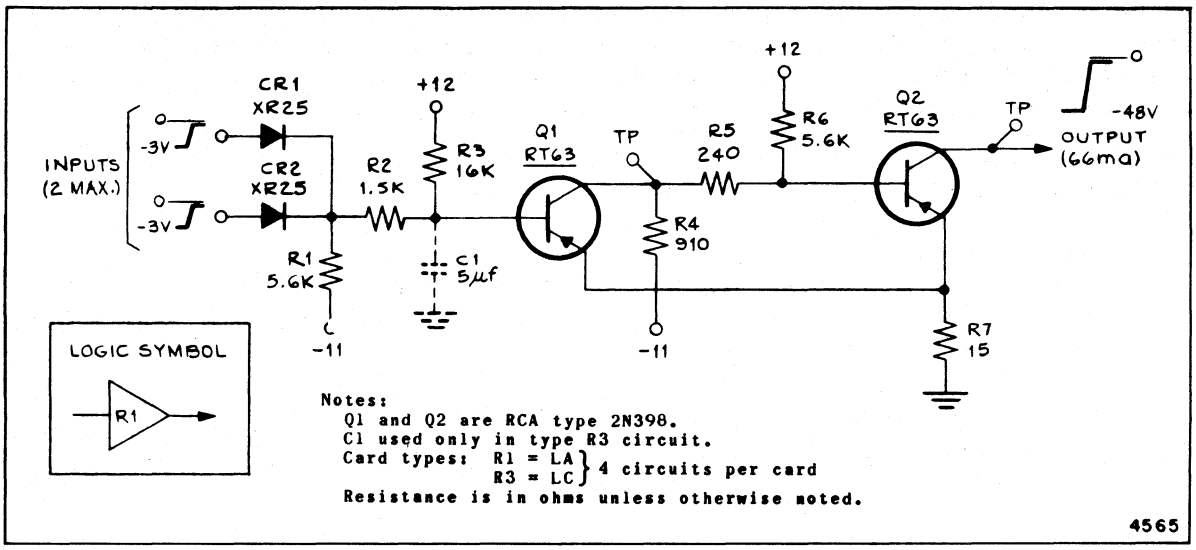


Figure 1-21. Type-R1 and -R3 Low-Speed Driver Circuit

The operation of the circuit is similar to previously described inverter circuits. The circuit parameters in the constant-current (PNP) coupling networks are chosen so that, with low input signals present, the first stage Q1 is conducting (base-to-emitter voltage: -0.35 v) and Q2 is nonconducting. As shown in figure 1-21, the output potential level for all the devices to be driven by a type-R1 or -R3 unit is at -48 v. A positive-going signal of 1 drive unit (1.64 ma) at input diode CR1 or CR2 will cause Q1 to cut off and Q2 to conduct (base-to-emitter voltage: -0.9 v) so that the output will rise toward the level of ground potential. (Q2 bottoms at about -0.3 v.) The use of type-RT63 high-voltage junction transistors (RCA type 2N398) in both stages provides for an output driving signal of up to 66 ma at the 48-v swing of the second collector supply. The common-emitter resistor R7 introduces a small amount of negative feedback into the circuit and thereby improves the stability of operation with marginal input signals.

When the type-R1 or -R3 driver is used to furnish power for operating incandescent lamps, special precautions must be taken to limit the transient current from the collector of Q2, or damage to the transistor will result. Current limiting is needed because of the wide variation in the thermal time constants of the transistor and the incandescent lamp. In most of the Larc applications a 1500-ohm thermistor is connected in series with the incandescent lamp (GE type 1835) to provide the protection from current surge for the RT63 transistor in the low-speed driver. The negative temperature coefficient of resistance of the thermistor causes the major portion of the initial-output step voltage from the driver to be applied across it. As the lamp filament and thermistor heat up, the thermistor resistance decreases and the output voltage is gradually transferred to the lamp.

The type-R1 circuit is supplied as card type LA, and the R3 circuit is supplied as card type LC. Each of the two card types contains four driver circuits. (See figure 1-21.)

1-31. TYPE-R2 LOW-SPEED DRIVER

The circuit for the type-R2 low-speed driver is shown in figure 1-22. Except for higher-power output capabilities this circuit is essentially the same as the type-R1 circuit of the preceding section. The input stage Q1 uses the same type-RT63 junction transistor as the R1 circuit, but Q2 is a type-RT62 high-power alloy unit (RCA type 2N301-A). With the type-RT62 transistor as the output amplifier, the R2 circuit is capable of delivering up to 500 ma of load current at the collector supply voltage of -48 v. The input current required to switch the circuit is about 2 drive units (3.28 ma).

The coupling circuits in both stages have been changed from the R1 circuit to include the silicon step-up diodes CR3 and CR4. The use of the diodes reduces the input impedance of each stage so that minimum required base-current conditions can be more easily met. In addition, current feedback (R7 in figure 1-21) has been eliminated from the circuit. The R2 circuit is supplied as card type LB with four complete circuits per card.

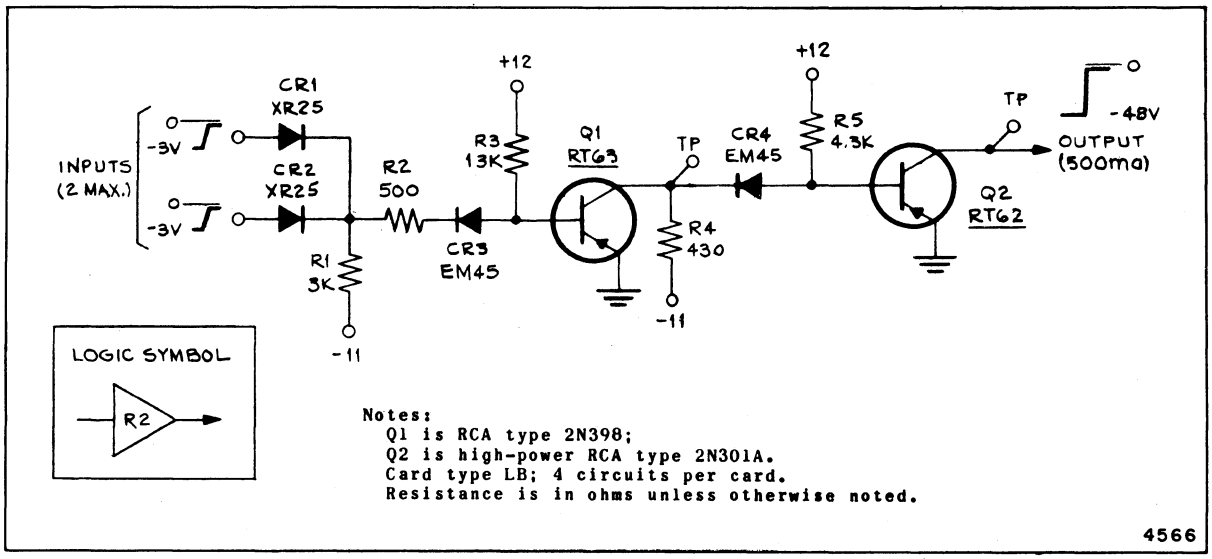


Figure 1-22. Type-R2 Low-Speed Driver Circuit

1-32. TYPE-L NEON-INDICATOR DRIVER

The type-L neon-indicator driver is used in any application where it is desirable to provide a continuous visual indication of a signal state at some point within the logic networks. The circuit card must be situated near the logical circuitry to be monitored in order to minimize wiring capacitance effects, but the neon-indicator bulb may be placed at any convenient location since lead length from the driver output is insignificant. The circuit is illustrated in figure 1-23 and consists of a single-stage amplifier with only one input and one output connection allowed. The operating conditions are such that, when the input signal is low (-3 v), diode CR1 is reverse-biased, the transistor is conducting, and the externally packaged neon-indicator bulb is on. If the input signal goes high, Q1 cuts off, and the neon bulb is extinguished.

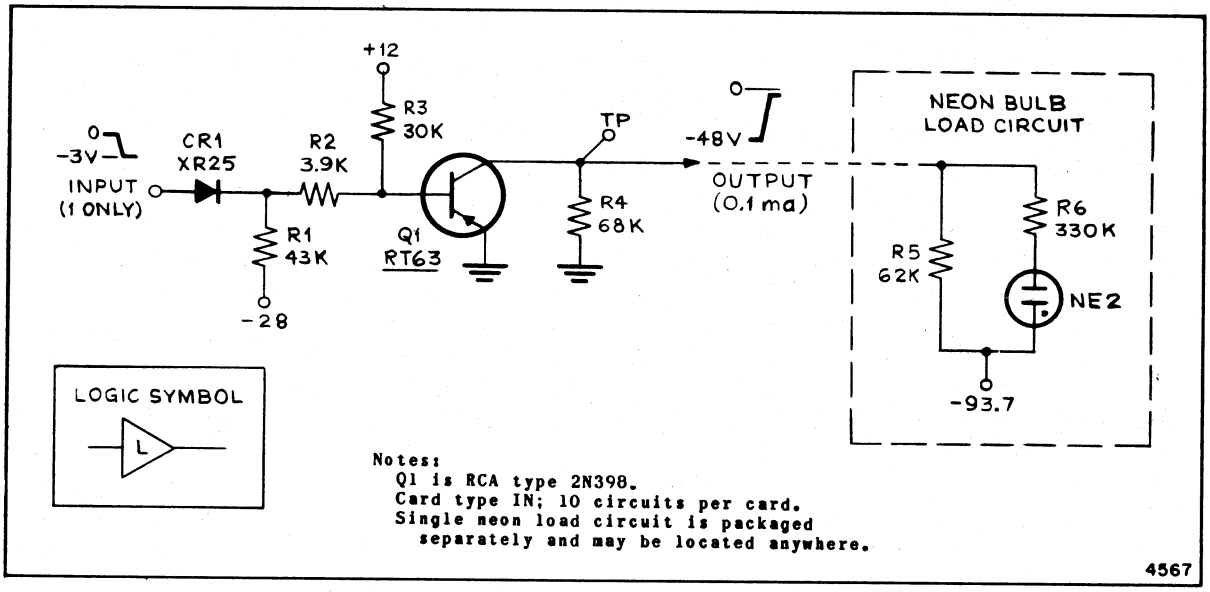


Figure 1-23. Type-L Indicator-Driver Circuit

The input circuit uses a standard resistive voltage step-up coupling network. The single input diode is needed (no logic allowed) to isolate the stage and prevent loading down of the input signal when it is at -3 v. Without the isolation provided by CR1, other gate-inverter circuits (1C, 1E) driven by the same input signal would require an additional current gain of 1. The transistor is a high-voltage RT63 unit, and the required input switching current is only 0.55 ma; that is, the loading effect of the circuit is the same as a type-1E low-level gate inverter.

In the output circuit the -93.7-v load-return voltage is required to fire the neon bulb. This voltage is selected on the basis of a maximum firing potential for type-NE2 neon bulbs of 86 v plus allowances for a 0.3-v transistor bottoming voltage, 0.7 v for wiring and ground voltage drops, and a $\pm$5-percent supply tolerance. In operation the nominal drop across a bulb is about 60 v, and excellent results in terms of brightness level and life of the bulb are obtained at a current of only 100 μa. The resistance R6 in series with the neon bulb limits the current to this value.

In order to extinguish the neon bulb it is only necessary to reduce the voltage across it to less than 62 v. The values of the resistances in the voltage divider R4 and R5 are chosen so as to cause the collector-to-emitter potential to be between 45 and 50 v when the transistor is switched off. Consequently the collector will swing from about -48 v to -0.3 v from the conducting to the nonconducting state.

The neon indicator circuit, sometimes referred to as the 1C indicator circuit, is supplied as card type IN. (Up to ten circuits can be mounted on a type-IN card.) As mentioned earlier, the card will contain only the transistor and its input coupling circuit. The neon-bulb load circuit is packaged separately.

1-33. TYPE-VT TUBE DRIVER

The type-VT output circuit is a low-frequency unit which is similar to the type-R1 low-speed driver. The VT circuit differs from the R1 type in that it provides an output-signal voltage that swings positive as well as negative with respect to ground, a requirement which is most often found in tube-operated switching circuits. The circuit is shown in figure 1-24 and is designed specifically for amplifying the 3-v signals of the tape- and printer-synchronizer logic to the 50-v (peak-to-peak) levels needed to drive control tubes in the Uniservos and on-line printer.

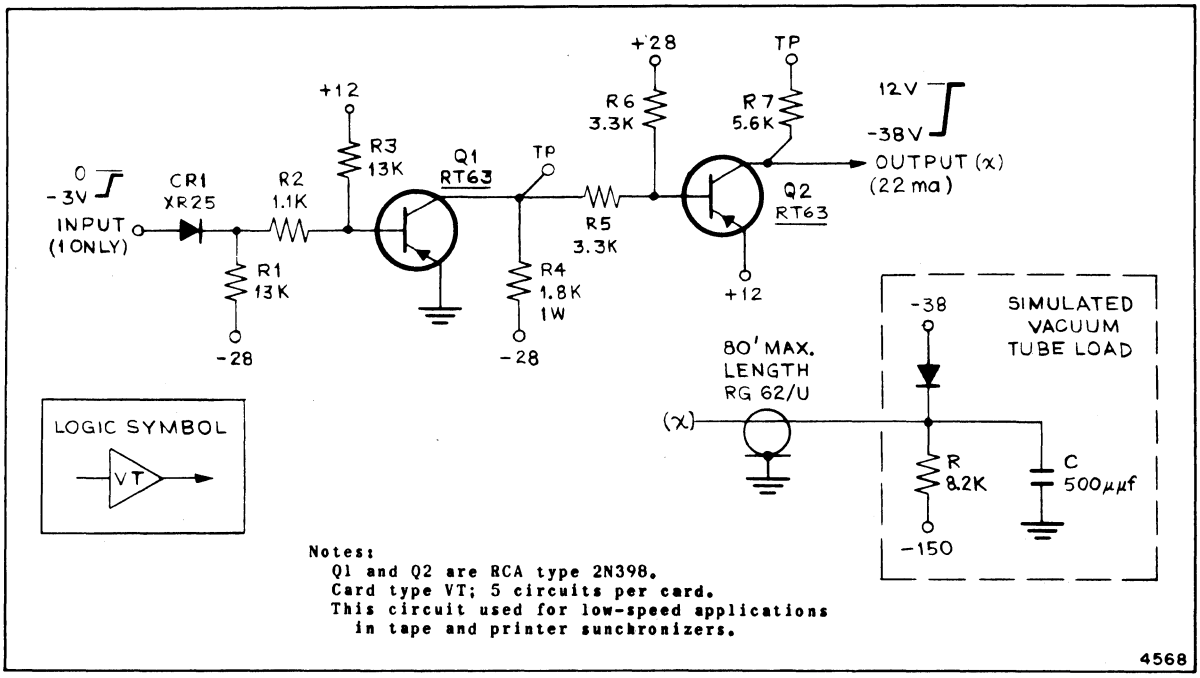


Figure 1-24. Type-VT Tube-Driver Circuit

The circuit consists of two resistance-coupled inverting amplifiers using type-RT63 transistors in both stages (the same as the R1 circuit). With a low input Q1 is conducting while Q2 is nonconducting, and the level of the output potential is at its most negative value. Notice that only one input and one output connection is allowed and that the output signal is carried by coaxial cable of up to 80 feet in length to the output device where it is clamped externally to -38 v. A high input signal of 1 drive unit (1.64 ma) will be coupled by diode CR1 to cut off Q1 and turn on Q2. The level of the output potential then will rise to the second emitter-return potential of +12 v. Consequently the input signal at the base of the Q2 must be more positive than 12 v when Q1 is conducting. The resistive voltage step-up network composed of R4, R5, and R6 performs this function.

In operation the voltage at the collector of Q1 varies from -0.3 to -15 v from the on to the off state, while the output at the collector of Q2 will swing from -38 to +12 v, as shown in figure 1-24. The maximum collector current from Q2 with the simulated load shown is about 22 ma.

The 5.6-kilohm resistor R7 in series with the output test point is used as a safety precaution to prevent damage to the circuit from accidental grounding. For test purposes, with a IC circuit for input drive and the simulated load shown in figure 1-24, the bottoming voltage for Q2 (measured from the +12-v supply to the output point at x) must be less than 0.3 v. The transient response of the circuit (measured from input to output terminals with a 100-μs test pulse) must not exceed 60 μs for maximum delay, plus rise time.

1-34. TYPE-VC TUBE DRIVER

The type-VC tube driver is a high-speed output circuit which has been designed specifically for driving vacuum-tube loads in the electronic page recorder. The circuit is similar to the VT unit in that it consists of a two-stage switching amplifier, but it includes additional components for improving the frequency response (figure 1-25). The requirements of the circuit are that it be able to amplify a 3-v input signal of 1 drive unit to an output signal which will swing between -28 and +12 v with a delay time in the range of 1 μs.

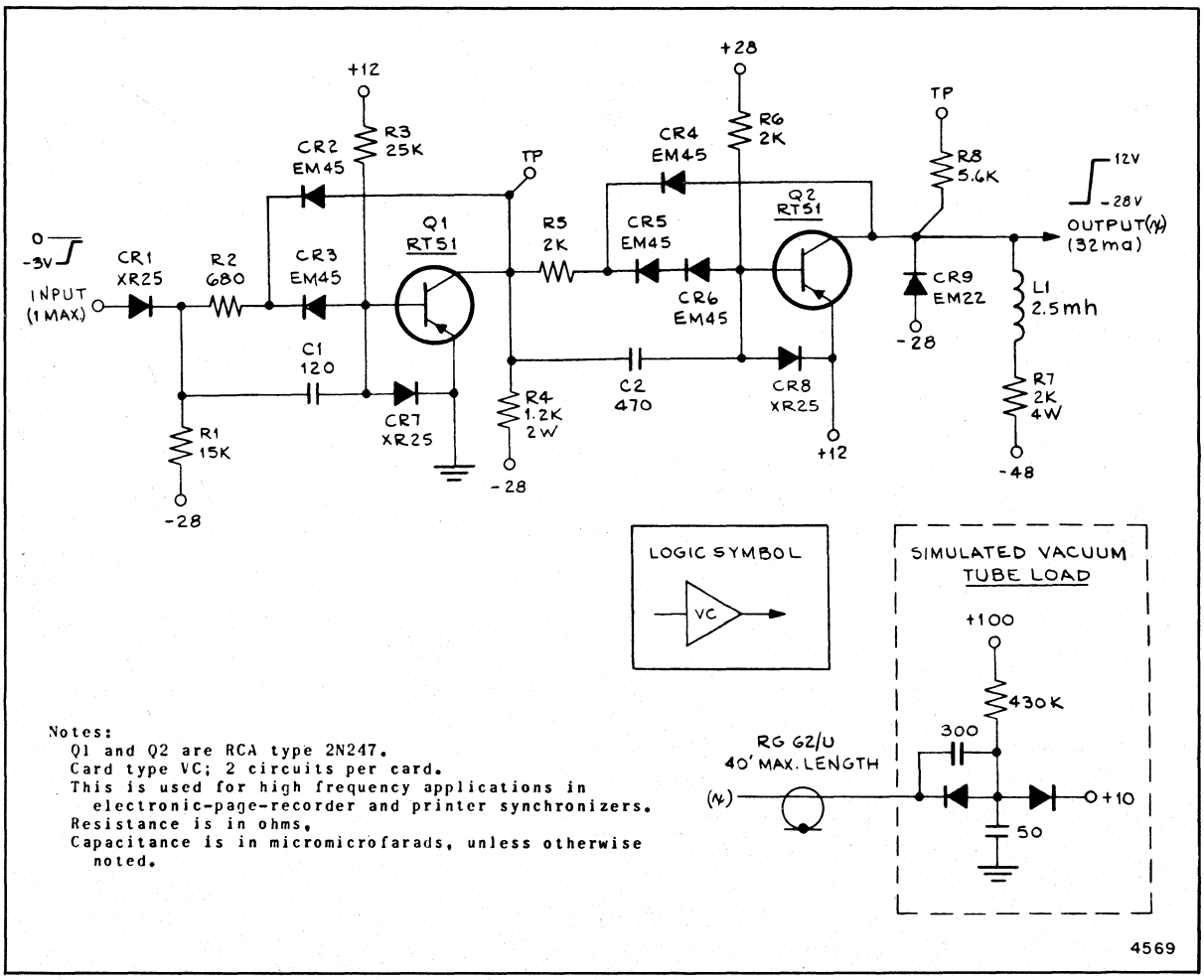


Figure 1-25. Type-VC Tube-Driver Circuit

Both transistors in the circuit, Q1 and Q2, are type-RT51 high-frequency drift units (RCA type 2N247) which are capable of handling the 40-v output collector voltage at the required switching speeds.* As compared to junction transistors, the drift units are characterized by (1) shorter transit time for the injected carriers in the base region, (2) lower collector capacitance, and (3) lower base resistance. With these transistors, however, circuit precautions must be taken to guard against excessive storage delays due to loss of the drift field. For the type-RT51 unit the drift field will be lost if the bottoming potential becomes lower than about 1 v. As shown in figure 1-25, feedback diodes from collector to base are used in both stages to limit the saturation current. This action takes place as follows.

Diodes CR2 and CR4, functioning as clamping diodes, restrict the swing of the collector potential in the positive direction. The following relationship, covering the output stage Q2, at which the collector voltage rises to the value of the clamping potential E_c, holds true:

$$E_c = E_{be} + E_s - E_f$$

At this point diode CR4 begins to conduct; therefore the transistor collector voltage is maintained at the value of E_c. In the preceding equation E_{be} is the base-to-emitter drop of the conducting Q2, E_s is the sum of the forward drops of CR5 and CR6, and E_f is the drop across CR4. With the use of type-EM45 silicon diodes the solution is this:

$$E_c = 0.6 + 1.5 - 0.73$$

$$= 1.37 \text{ v}$$

Thus the collector-to-emitter potential of Q2 will always be greater than 1.37 v. An added benefit of the use of clamping diodes is the degenerative action of the clamp circuit itself, which minimizes the effect of overdrive and allows a faster current response during switching.

Other speed-up features of the circuit are the coupling capacitors (C1 and C2) and the peaking components at the output collector (L1 and R7). The output-load circuit consisting of the coaxial cable capacitance paralleled by R7 and L1 is underdamped with the values shown, but ringing effects are eliminated by the clamping of the output signal at -28 v and the effective clamping action of the transistor at +12 v.

In operation the circuit functions in a manner similar to that described under heading 1-33 for the type-VT tube driver. Tests are also conducted in the same way with a 1C circuit used for input drive and a

* The RT51 transistor has an impurity distribution in the base region which is very high at the emitter and decreases exponentially to low values at the collector. This distribution produces a constant electric drift field parallel to the diffusion direction in the base region.

simulated load circuit as shown in figure 1-25. For the type-VC circuit the measured bottoming voltage for Q2 must be between 1.2 and 2.0 v; the transient-response times, measured with a 5-μs test pulse, must not exceed the following values by more than 10 percent:

Transient Response	Waveform (Percent)	Time (μs)
Rise delay	0 ... 10	0.50
Rise time	10 ... 90	0.34
Fall delay	100 ... 90	0.30
Fall time	90 ... 10	0.94

Because of the large number of components and high wattage of resistors, only two circuits are packaged on a standard card (type VC). In addition, each VC card requires two card spaces in the backboard because of transistor size and power dissipation.

Another point that must be considered in the operation of the tube-driver circuits (both types VT and VC) is the need for voltage sequencing during power turn-on and turn-off. In both cases +12 v must be applied before and removed after -28 v, in order to prevent excess voltage on the collector of the first stage (Q1). The collectors of the second stage also must be protected by the application of the clamp voltages (-38 v for VT, -28 v for VC) before the higher output-load return voltages are turned on.

1-35. COUPLING NETWORKS

Various types of coupling circuits are needed to couple signals from the input-output equipment, or from the operator and engineer consoles, into the computer-processor logic circuitry at the correct d-c levels. In this sense the coupling circuits serve primarily as voltage attenuators so that signals at different potential levels will be introduced into the system at the standard 3-v logic levels. For coupling signals between the input-output equipment and the processor the type-CNC, -CNE, and -CNR circuits are available; a special filter unit (type F) couples signals from switches on the consoles or other equipment into the logic circuitry. The type-CNC and -CNE circuits are used only in specific circuit applications in the tape and printer synchronizers; the CNR circuit has a unique application in the drum-write synchronizer. These circuits, therefore, will be described in the following paragraphs devoted to synchronizer circuits.

The type-F filter circuit is shown in figure 1-26 and consists of a shunting capacitor (C) connected across the signal line. The capacitor diminishes pick-up noise on interconnecting cable wires which results from the opening and closing of the switch contacts. With the switch open, the -3-v level will be applied to the load side of the circuit through resistor R, and the capacitor will be charged to 4.5 v. When the switch is closed, the capacitor will discharge rapidly through the switch, and the output

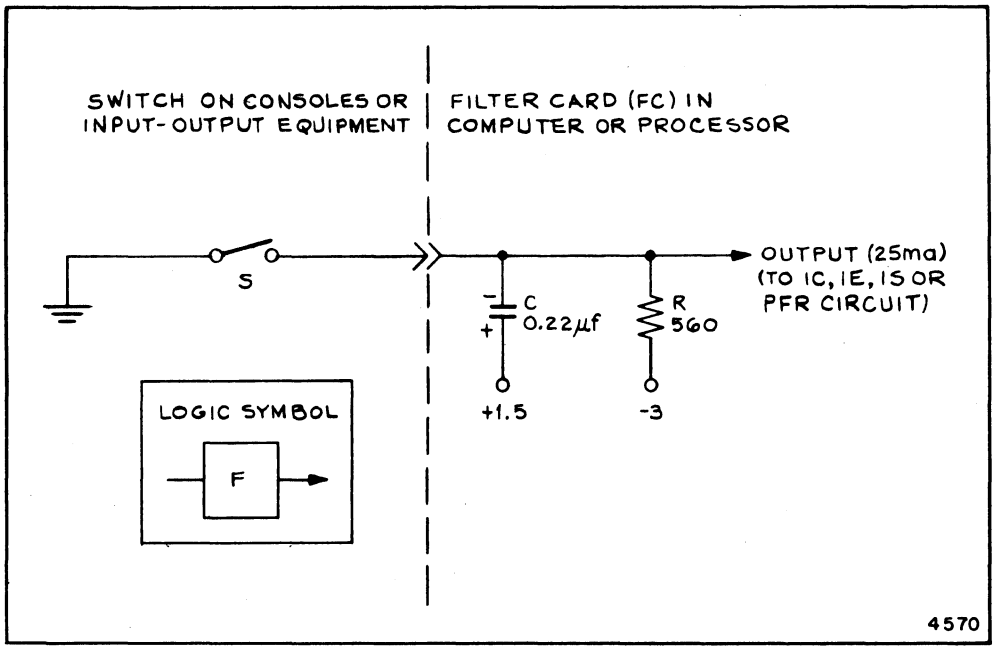


Figure 1-26. Type-F Filter Circuit

voltage will rise to the level of ground potential. The discharge current from C is sufficient for driving a load of up to 15 type-1C circuits or the equivalent (about 25 ma). Heavier loads can be accommodated simply by connecting additional filter elements in parallel across the output signal line. The filter circuit is supplied as card type FC with 20 circuits on a card.

1-36. DRUM-SYNCHRONIZER CIRCUITS

Several special circuit types have been developed for use in the drum read and drum write synchronizers. They include those needed for generating the write-current waveforms for driving the magnetic head in a drum, as well as those required to carry out the functions of the self-sprocketing readback system. Among the logic circuit types used only in the drum synchronizers to implement these functions are the following:

(1) Type DU-DW Drum write amplifier

(2) Type DP Drum read preamplifier

(3) Type DR-DS Drum read amplifier

(4) Type ST-A Schmitt trigger

(5) Type LD Long-delay element

(6) Type 1S-B Gate inverter

The Schmitt trigger and gate-inverter circuits are described in the sections devoted to these circuits. (Refer to headings 1-5 and 1-23 for details of 1S-B gate-inverter and ST-A Schmitt trigger circuits.) Detailed descriptions of the other circuits mentioned in the preceding list are given here. However, a general description of the overall drum read-write system is presented first so that the application of these special circuit types in the drum synchronizer logic will become more evident. Also covered here is a special coupling circuit (type CNR) that has a unique application in the drum write synchronizer.

1-37. DRUM READ-WRITE SYSTEM: GENERAL DESCRIPTION

A drum write synchronizer contains a group of five write-current generating circuits (one for each bit of a digit) which produce the required phase-modulated current waveforms for writing on a drum. In the phase-modulation method of recording the significance of a 1 or a 0 is determined by the direction of the write-current transient as it crosses the zero axis at a particular phase of each write cycle. In order to write a pattern in which all bits are the same, it is clearly necessary to recross the zero axis at some other part of the write cycle. The read-back circuits must be able to distinguish between these two kinds of transients.

The convention adopted for use in the Larc system is based on the polarity of the waveform at the output of the write-current generators in the synchronizer. The output circuits of the generators are push-pull circuits driving a twin-conductor, balanced-to-ground output cable. The outputs of the twin conductor are labeled + and — on the logic diagrams.

Convention for Writing a 1

The direction of the write-current transient at the time of significant zero crossing is

(1) From positive to negative when it is observed at the output marked +, or

(2) From negative to positive when it is observed at the output marked -.

Convention for Writing a 0

The direction of the write-current transient at the time of a significant zero crossing is

(1) From negative to positive when it is observed at the output marked +, or

(2) From positive to negative when it is observed at the output marked -.

The synchronizer must control the frequency of the write-current generators so as to maintain the correct bit density on the recorded drum surface. The bit repetition rate chosen for this purpose is 500 kc.

Timing pulses TO and T4 are used to phase the generators so that significant zero crossings will occur at these times. Even with no input information the output will change state every TO and T4, producing a 250-kc waveform which will be interpreted as alternate 1's and 0's. (See waveform 1, figure 1-27.)

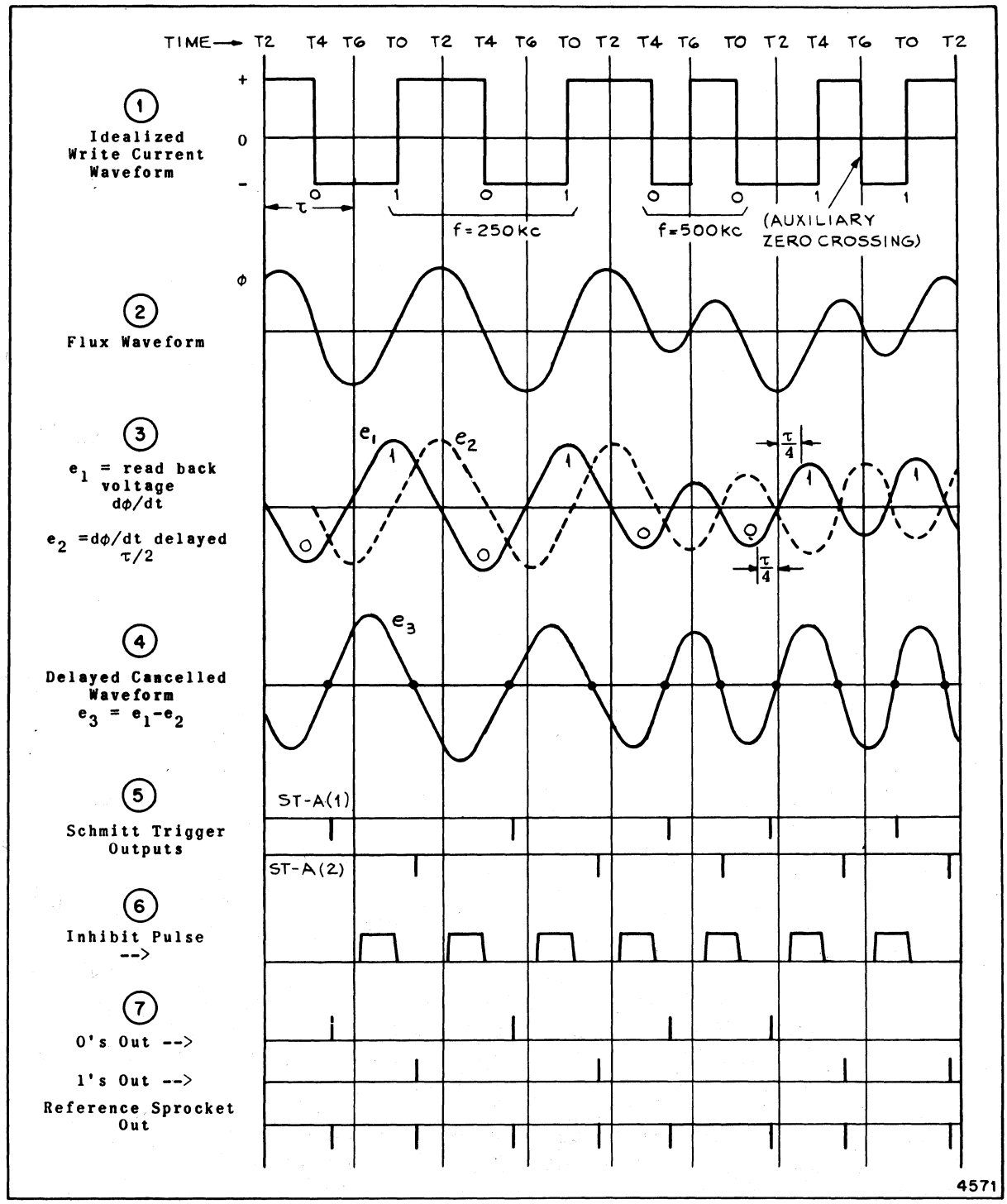


Figure 1-27. Drum Read-Write System, Waveforms

Under control of the synchronizer, output information from the main core storage is transferred to the input of the write-current generators at times T2 and T6. At these times the positive output is made high in preparation for writing a 1, or low in preparation for writing a 0, if it is not already in the desired state. Thus, the significant crossing, which occurs 1 microsecond later, will be of the correct polarity. An extra write-current transient will occur each T2 or T6 only if the bit to be recorded is the same as the last bit recorded in the same channel. Such transients are termed auxiliary zero crossings and must be recognized as such in the read-back circuits.

The recorded flux pattern on the surface of the drum is essentially proportional to the write current, except for two factors. All transients are slower than the write current, and the 500-kc constant-frequency segments are approximately one half the amplitude of the 250-kc constant-frequency segments. (See waveform 2, figure 1-27.)

The read-back voltage waveform e_1 (waveform 3, figure 1-27) is proportional to the slope of the flux waveform, with peaks corresponding to the zero crossings of the flux and write current waveforms. To select only the significant peaks (information) from a signal, the usual method is to generate synchronous sampling pulses by means of a sprocket or timing track. The requirement concerning accuracy of ideal synchronization is that the interrogation must take place within one quarter bit cell ($\tau/4$) of the significant peaks. If a sample pulse is not generated within the tolerance of $\tau/4$, the significance of the information may be misinterpreted that is, the wrong polarity of signal could be read beyond the limit of $\tau/4$ as shown on waveform 3 of figure 1-27.

In the case of the Larc drum system it is not feasible to meet the $\tau/4$ maximum tolerance. If an individual sprocket track were assigned to each band of five information tracks, the permissible skew of the head could have an arc of only a few minutes. It is particularly difficult to meet this limit in the case of a movable-head system such as that of Larc. Therefore it is desirable to derive the sprocket pulses from the information signal itself.

A self-sprocketing system for phase-modulated signals must provide an output corresponding only to the significant peaks of the read-back voltage. However, since zero crossings are easier to detect than peaks, the peaks are converted back to zero crossings. A delayed-cancellation operation is performed in which the read-back signal is delayed approximately one half bit cell ($\tau/2$) and is subtracted from the original signal. The result is waveform 4, figure 1-27. Peaks are converted to zero crossings delayed approximately $\tau/4$, and the relative signal amplitudes for consecutive like bits and unlike bits are more nearly equal than in the read-back waveform. The zero crossings of the cancelled waveform are spaced nearly $\tau/2$ and τ units apart, and roughly correspond to the zero crossings of the write-current waveform.

It is now necessary to detect the zero crossings of the cancelled waveform and generate three outputs: the 1's, 0's, and sprocket pulses. This is carried out by two Schmitt trigger circuits (type ST-A) whose output pulses correspond to zero crossings with opposite slopes in the cancelled waveform, and special circuit logic built around the type-LD

long-delay element and a flip-flop arrangement which uses type-1S-B gate inverters. As drawn in the remaining waveforms of figure 1-27, the technique consists of detecting the 1's and 0's of the significant zero crossings, inhibiting the auxiliary zero crossings, and deriving the sprocket pulses. Note that the inhibit pulse relies on the fact that the largest spacing between a significant zero crossing and an auxiliary zero crossing is always less than the smallest spacing between two significant zero crossings.

1-38. WRITE-CURRENT GENERATION. The write-current generators consist of a group of five pulseformer-type flip-flops that are connected as binary counters. The outputs from the flip-flops will change at a basic frequency under control of the recurring timing pulses from the processor cycling unit. As shown in the logic diagram of figure 1-28a for one of the channels (channel X*), the outputs from each side of the generator circuit are connected through a pair of control gates to the + and - inputs of the drum write-amplifier unit DU. The DU unit represents the first stage of the drum write amplifier and is packaged on the same card with gates G1 and G2. The amplifier output stages are packaged on a DW unit capable of driving the write bus that carries the output-current waveforms to the read-write head in a drum.

Timing pulses T0 and T4 control the basic operating frequency of the generators. During writing, additional driving signals are applied to the inputs of the generators at the recurring times T2 and T6 to modulate the output signal. As indicated in figure 1-28a, the driving signals (1's and the reset pulse) will write 1's or 0's, depending on whether the driving signals set or reset the flip-flop in the generator.

In figure 1-28a is a timing chart of the various current waveforms which shows the times at which the levels from the generator pulseformer (P1) and amplifier (DW) change in accordance with the timing and other driving signals from the synchronizer. These waveforms indicate that the direction of a waveform at the time of a significant zero crossing depends on the point in the circuit at which the waveform is examined.

A positive information pulse will occur at time T2 (or T6) if a 1 is to be recorded. A reset pulse will also occur at T2 and T6 as long as information is being transferred from the main core storage. The information pulse will override the reset pulse to set the flip-flop (if it is not already set) and produce a negative output at point 1. This action will open gate G1 to provide a positive output on the + line of the write bus. At the time of the next driving signal, T4 (or T0), the flip-flop will be reset, and gate G2 will open to produce a positive output on the — line of the write bus.

If a 0 is to be recorded, there will be no information pulse at time T2 or T6. The reset pulse then will reset the flip-flop at this time (if it is not already reset) to produce a negative output at point 2. This action will open gate G2 to provide a positive output on the — line of the write bus. At the time of the next driving signal, T4 or T0, the flip-flop will be set, and gate G1 will open to produce a positive output at the + line of the write bus. The flip-flop, therefore, will invariably change state at T0 and T4, but will change state at T2 or T6 only as required by information received from the main core storage.

* Channel X: channels A ... E.

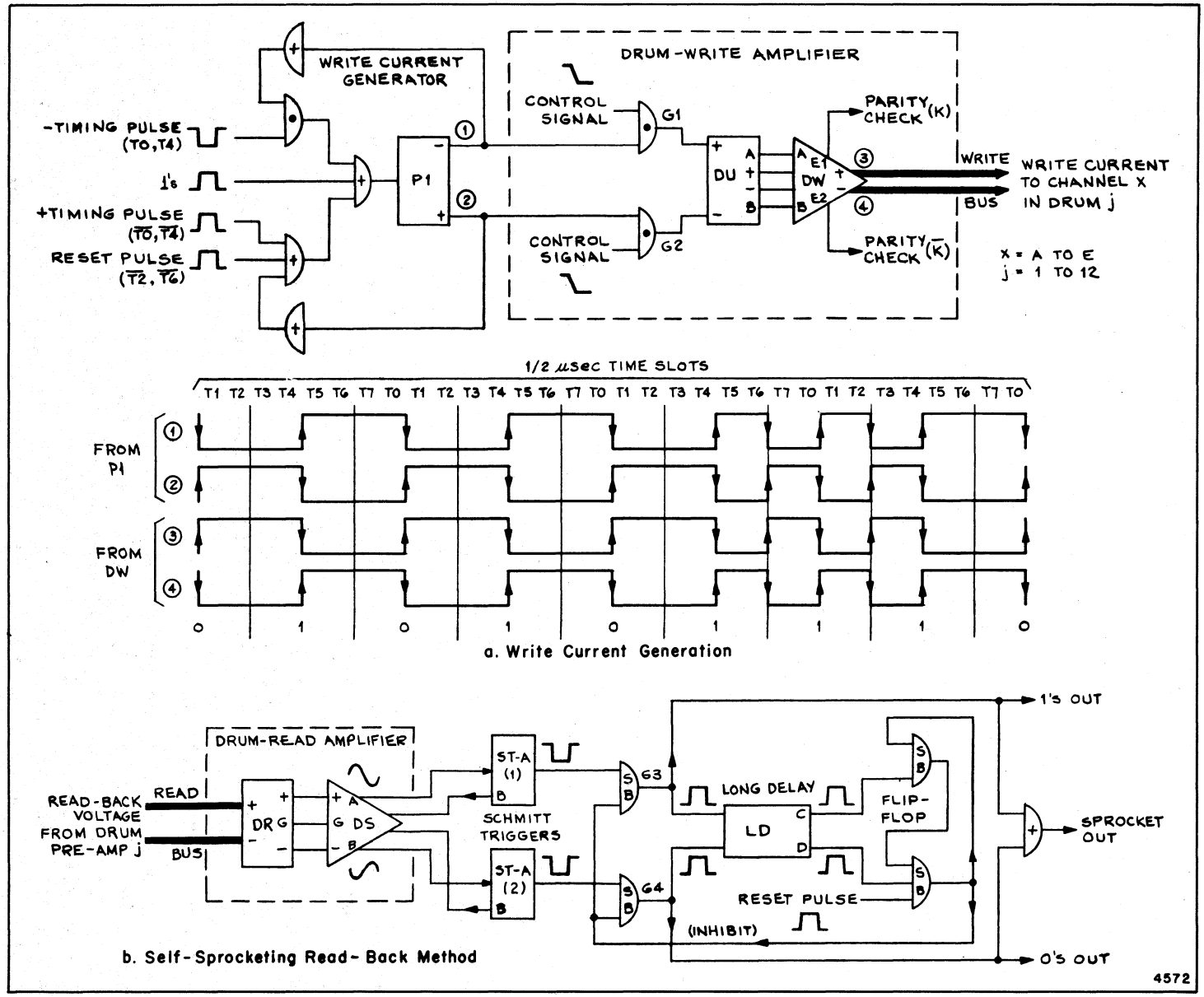


Figure 1-28. Drum Read-Write System (One Channel)

The sequence in figure 1-28a illustrates the signals that are used to write the bits 0 1 0 1 0 1 1 1 0 on one of the channels. The outputs taken from terminals E1 and E2 on the amplifier unit DW (signals K and $\bar{K}$, respectively) are sent to the error-detection circuits in the synchronizer and are used to provide a parity check on the output information.

1-39. SELF-SPROCKETING READ-BACK METHOD. The information signals from the magnetic head in the drum are fed into the synchronizer through a preamplifier and a relay switching package located in the drum, and through the drum-read bus. As shown in figure 1-28b, the input drum read amplifier is packaged on two card types, DR and DS. Each card type consists of a two-stage balanced amplifier. The output from the amplifier unit is a sinewave whose zero crossings correspond to peak voltages picked up from the drum. The + and — outputs are 180 degrees out of phase. The output from each side of the DS unit triggers a corresponding Schmitt-trigger, A-type circuit (ST-A). The Schmitt circuit provides a negative pulse of fixed duration starting from a positive-going zero crossing at its input.

The outputs from the ST-A circuits are negative-going 0.2-μs pulses which open gates G3 and G4. Depending on whether the input signal represents a 1 or a 0, gates G3 or G4 will open and produce a corresponding 1 or 0 information signal which is fed to the self-sprocketing and other synchronizer circuits. For the self-sprocketing operation gates G3 and G4 are controlled by the output from the flip-flop. As shown in figure 1-28b, the flip-flop is reset initially by a pulse so that gates G3 and G4 will be alerted to pass the first information pulses from the drum.

The output from gate G3 or G4 is connected to the type-LD long-delay element. After a delay of approximately 0.33 μs, a positive output is obtained from terminal C of the LD unit, which sets the flip-flop. After a much longer delay of 1.35 μs, an output is obtained from terminal D, which resets the flip-flop. During the time that the flip-flop is set, gates G3 and G4 are inhibited. The timing of the inhibit pulse is arranged to span the possible times of any auxiliary zero crossings—that is, zero crossings that result from writing two or more consecutive like bits (heading 1-37).

1-40. DRUM WRITE AMPLIFIER

The complete schematic diagram of the drum write amplifier is shown in two parts in figures 1-29 and 1-30. Figure 1-29 shows the type-DU card, which contains the input control gates and the first stages of the amplifier for both sides of the balanced circuit. The amplifier output stages, which are shown in figure 1-30, constitute the type-DW card. The inputs to the DU unit are obtained from the write-current generator and other circuits in the drum write synchronizer. The outputs from the DW unit are connected through the write cable to a termination circuit located in the drum. Figure 1-31a illustrates the termination network for one channel.

The input gating arrangement of the drum write amplifier consists of conventional 1C inverter circuits, Q1 and Q4, in which four input diodes are connected to each side of the circuit. As shown in figure 1-29, diodes CR1 and CR11 couple the outputs of opposite polarity from each side of a write-current generator so that Q1 and Q4 will always conduct on an alternating basis. Similarly, the remaining stages in the amplifier will

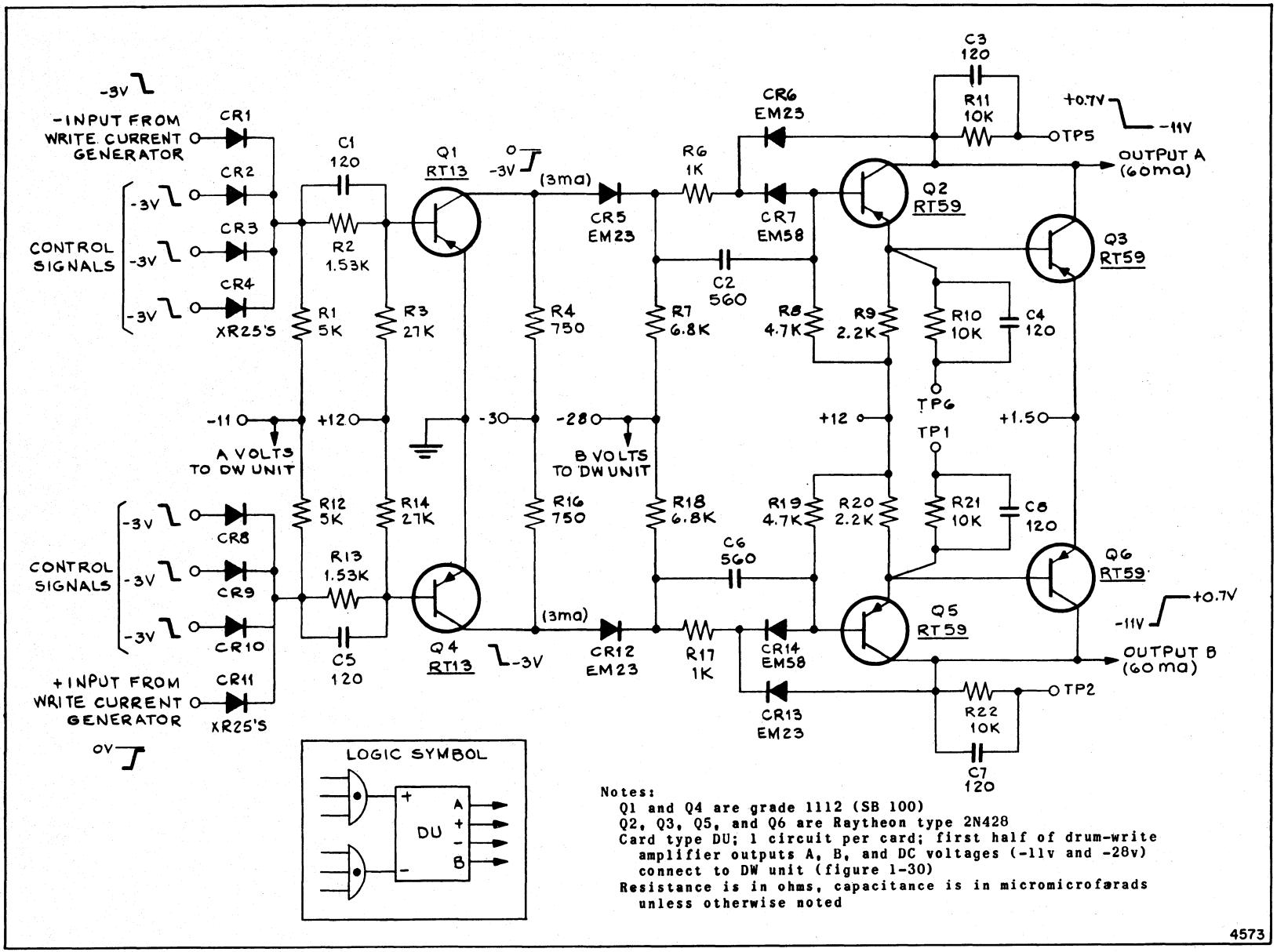


Figure 1-29. Drum Write Amplifier. Part 1

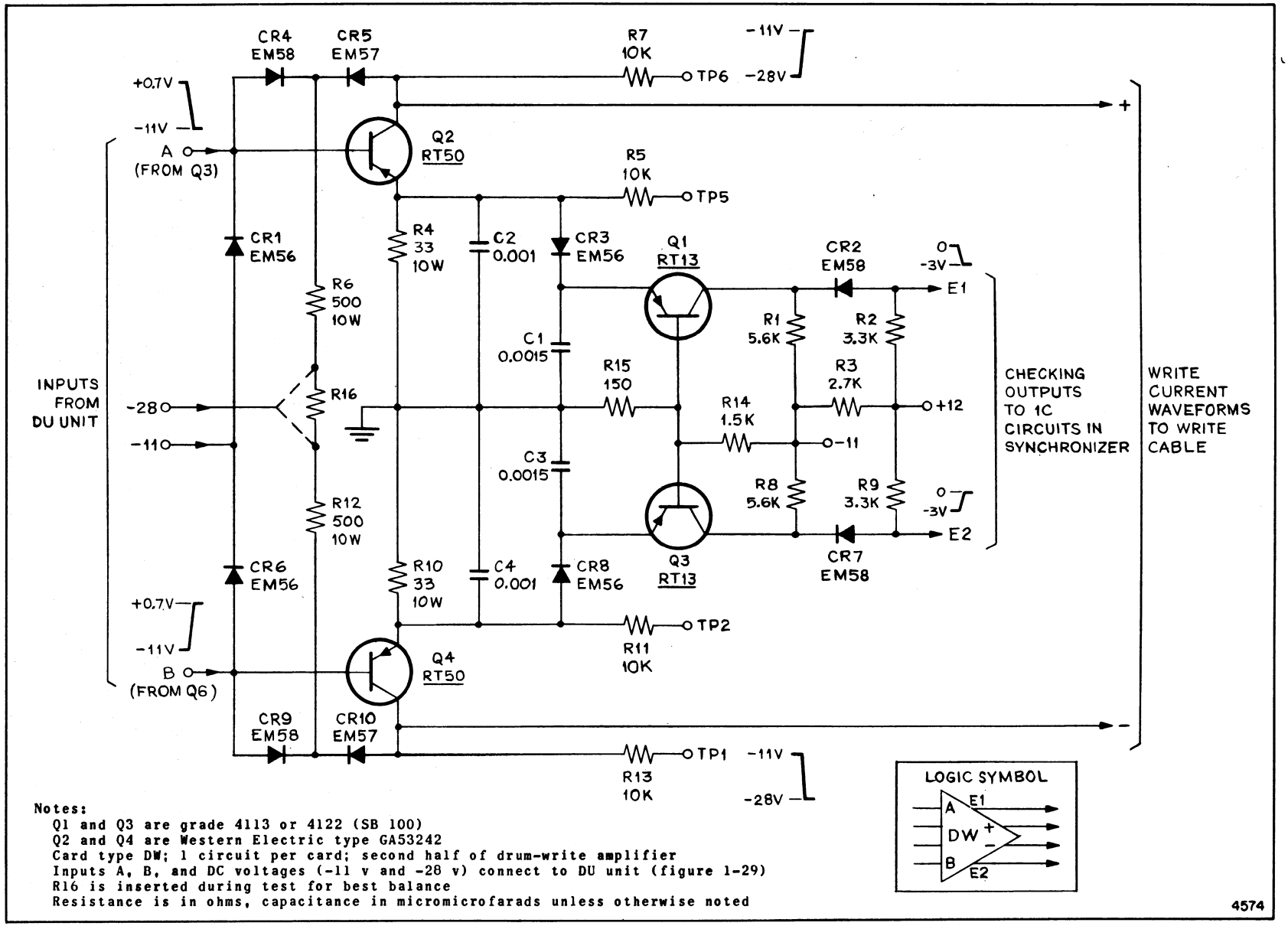


Figure 1-30. Drum Write Amplifier. Part 2

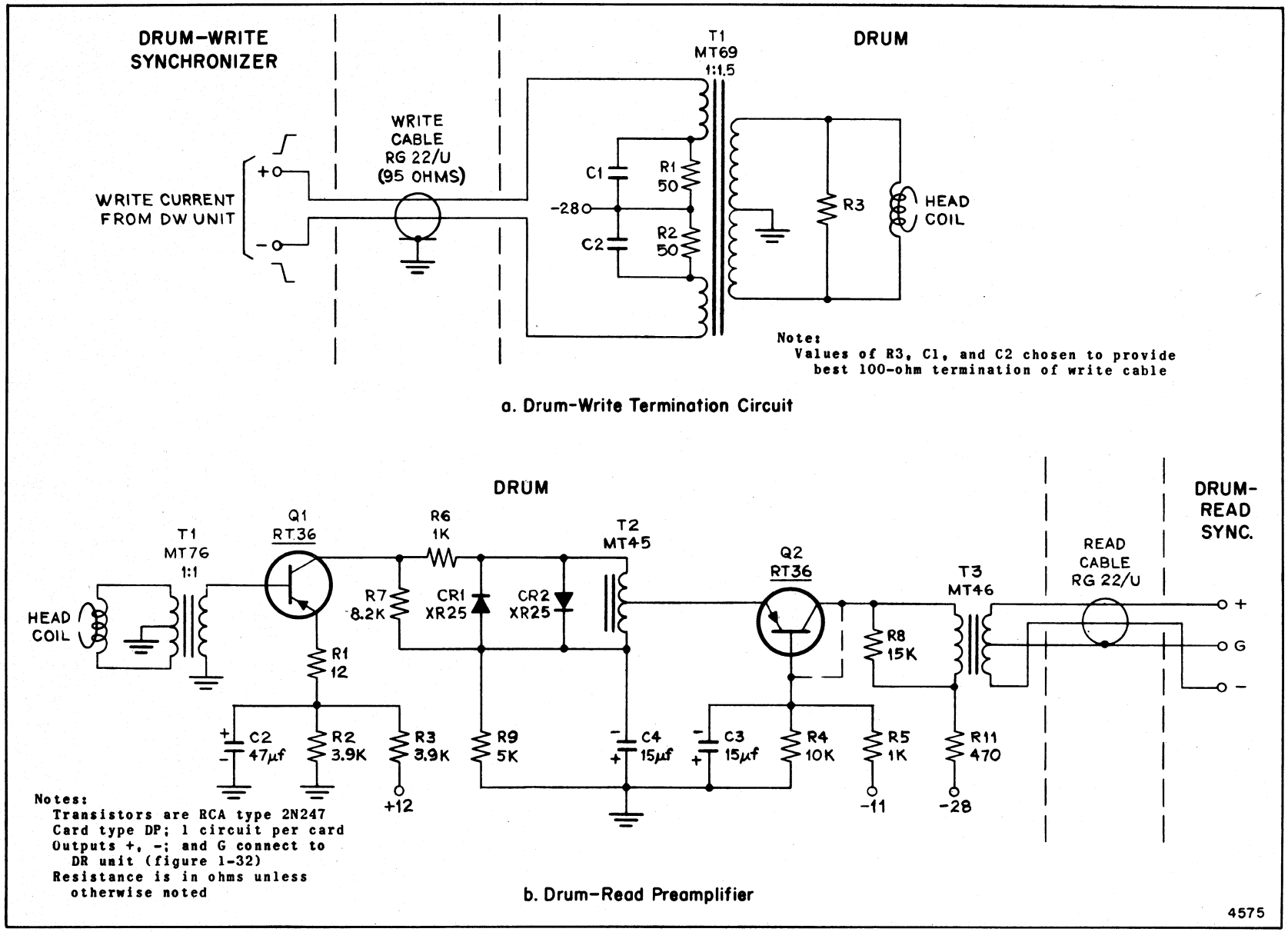


Figure 1-31. Read-Write Circuits in Drum

function on signals of opposite phase; therefore a description of one side of the circuit serves to explain the principle of operation of the entire circuit.

If Q1 is conducting, a current of about 3 ma is coupled through diode CR5 to cut off the next stage of the amplifier, Q2 and Q3. These two transistors are connected in piggy-back fashion to provide high driving power for switching the output stage on the DW card. Q2 is functioning as both an emitter-follower and common-emitter circuit similar to the high-power logical amplifier circuit described under heading 1-13. This stage also contains diode feedback (CR6) to limit the saturation current and thereby improve the speed of response of the stage. The d-c collector supply voltage for Q2 is obtained from the DW card (figure 1-30) through resistor R6 and the forward-biased diode CR4.

Outputs A and B from the DU card connect directly to the bases of Q2 and Q4 through inputs A and B on the DW card. With the driving-stage transistors Q2 and Q3 cut off (figure 1-29), the input voltage at the base of Q2 (figure 1-30) will drop to the clamping level of -11 v established by diode CR1 on the DW card. The output stage then will conduct to provide writing current to the drum.

The + and — outputs from the DW card are connected through the write cable to the primary of the output transformer T1 (figure 1-31a), which terminates the line and provides an impedance match for the head coil in the drum. The d-c collector potential (-28 v) for the output stages in the synchronizer is obtained through the primary of the output transformer and the interconnecting cable. As shown in figure 1-30, outputs are also taken from the emitters of the output stages to drive a pair of low-power, common-base stages, Q1 and Q3. The purpose of these stages is the providing of a parity-check output as close to the writing head as possible. For example, if the emitter signal of Q4 is high, the signal will be coupled through diode CR8 to the emitter of Q3. The conducting Q3 then will provide a positive-going output signal through diode CR7 which is fed back to type-1C logic circuits within the synchronizer for checking purposes.

To refer back to figure 1-29: whenever the transistor-pair stage is conducting, Q2 and Q3 (or Q5 and Q6) will be driven almost to saturation. It is desirable to have a low-impedance output and low collector voltage while these stages are conducting, but the storage-time problem accompanying saturation is not desirable. To satisfy these conflicting requirements, the feedback diode CR6 (or CR13) is connected between the common collectors and the input base. The diode, however, will not conduct until the collectors are within a few tenths of a volt of the base, thereby allowing a larger current to discharge the capacitive effects of the collector load. In the worst case the collector current at output A or B of the DU unit will rise toward a limit value of about 120 ma, provided the collectors are more negative than the base by as much as 1 v or more. This action tends to speed up the transient response of the stage without causing carrier storage to delay the turn-off transient.

In operation the output current from the DU card will vary between 50 and 66 ma, while the collector-to-emitter potential will not exceed +0.7 v. When this stage is not conducting, the maximum collector output voltage at A or B will be limited to -11 v by the clamping diode CR1 or CR6 at the base of the output stage on the DW card (figure 1-30).

When either of the output stages of the amplifier (Q2 or Q4) is turned on, the amplifier is presented with an essentially resistive load of 50 ohms because of the balanced cable termination located in the drum. About 40 percent of the -28-v source (-11.2 v) will appear therefore across the 33-ohm emitter resistor R4 (or R10) if the transistor saturates. Diode CR1 or CR6 normally limits the base drive so that emitter potential is of slightly less value than -11.2 v during conduction, and feedback diode CR5 or CR10 limits the base drive just short of saturation if the available load current is slightly less than the output is capable of delivering. The minimum output current is therefore determined when the base drive is most negative and the -28-v collector supply least negative, and will be about 270 ma; maximum output current is limited by the emitter resistor to less than 355 ma. These current and voltage values will provide a peak-to-peak head current for the drum of at least 270 ma and leave 30 ma for the magnetizing current in T1. With the use of high-power RT50 transistors in the output stages of the DW card with a minimum beta of 11, the required base current is about 25 ma.

Any unbalance in the circuit due to tolerance variations in components is compensated for by means of resistor R16 (figure 1-30) in the base circuits of Q2 and Q4. The value of this resistor is selected during the testing of the circuit, and the variable connection is made to either one end of the resistor or the other to obtain the best balanced drive to the bases of the output transistors.

In order to handle the large output writing currents at a safe power-dissipation level, the output transistors Q2 and Q4 (Western Electric type GA53242) are each supplied with a 3 in. x 3 in. x 1/16 in. aluminum heat sink.

The primary winding of the output transformer (figure 1-31a) is split, and each half is returned to -28 v through a 50-ohm resistor (R1, R2). Each resistor is shunted by a capacitor (C1, C2) chosen so that the R-C time constant is approximately the same as the L/R time constant across the transformer secondary at 500 kc. The exact values of C1, C2, and R3 are selected during the testing of the circuit to provide for a constant 100-ohm termination of the output stages. This arrangement makes the collector load impedance more nearly independent of frequency and appreciably reduces the worst-case dissipation of the output transistors. Other advantages of the termination circuit in the drum are these:

(1) It terminates the write cable to prevent either ringing or reflected pulses, or both.

(2) It provides a fail-safe arrangement by leaving the RT50 output transistors without collector voltage in the event of a broken write cable.

(3) It enables the DW card type to be tested with a resistive dummy load (50 ohms to -28 v).

1-41. DRUM-READ AMPLIFIER

The drum-read amplifier circuitry is divided into two parts—a drum-read preamplifier associated with each recorded channel in the drum, and a main read amplifier in a drum read synchronizer. The purpose of the

preamplifier is the improvement of the signal-to-noise ratio of the signal distributed on the read cable, which is subject to interference from stray noise pulses before it reaches the read synchronizer. To reduce noise pickup further, signal leads between the head coil and the preamplifier are balanced to ground; so is the read cable which connects a selected preamplifier to one of the drum read synchronizers.

1-42. PREAMPLIFIER. The drum-read preamplifier (figure 1-31b) performs several functions in addition to amplifying the signal. It provides a balanced-to-ground input to the head coil through a 1:1 transformer (T1) whose centertapped primary eliminates the need for a centertap on the head coil. It limits the output to the read cable to about 2.5 v peak-to-peak by diode clipping (CR1, CR2) when the signal input exceeds about 50 mv peak-to-peak. It recovers from a severe overdrive (approximately 300 mv input) to a 5-mv input to produce an undistorted output in less than 20 μs. It has sufficient power gain to drive a 95-ohm terminated line with a signal voltage approximately 50 times as large as that measured across the head coil under open circuit conditions.

Three transformers are used in the preamplifier: input (T1), interstage (T2), and output (T3). For maximum gain the interstage transformer has as large a turns ratio as possible since it couples between the collector of one transistor and the emitter of the other. The upper limit on the turns ratio is set by leakage inductance, which resonates with various distributed capacitances which would produce severe phase distortions at the high end of the desired pass band. To minimize this effect, transformer T2 is designed to have the shortest L/R time constant of the three, allowing a lower magnetizing inductance and a correspondingly larger turns ratio for the same limiting value of leakage inductance. The interstage transformer therefore limits the low-frequency gain and determines the low-frequency 3-db-down point.

The input transformer must be wide-band so as not to affect the head termination. This is not difficult to effect since impedance levels are low and the turns ratio is set at 1:1. The remaining transformer (T3), which couples the second-stage collector to the 95-ohm output read cable, limits the high-frequency response so that the amplitude response will be considerably reduced before high-frequency resonance of the interstage leakage reactance starts to disturb the phase response.

This method of separating the elements which limit the amplitude response at the high- and low-frequency ends of the pass band also reduces phase shift, since at the 3-db points only one stage has very much phase shift to contribute. The preamplifier therefore has an amplitude response which is flat (±0.1 db) from 200 kc to 500 kc, less than 1 db down at 75 kc and 1200 kc, and less than 3 db down at 35 kc and 2200 kc.

1-43. MAIN AMPLIFIER. As with the drum-write amplifier, the main read amplifier in a drum-read synchronizer is packaged on two separate card types, DR and DS. The first two stages of this balanced amplifier (four transistors) constitute the DR unit (figure 1-32), and the output stages (four transistors) constitute the DS unit (figure 1-33). The inputs to the DR unit are obtained from the preamplifier in the drum by way of the read cable, and the output of this unit is transformer-coupled to the DS card. The outputs from the DS card are connected to Schmitt trigger (type-A) circuits in a drum-read synchronizer.

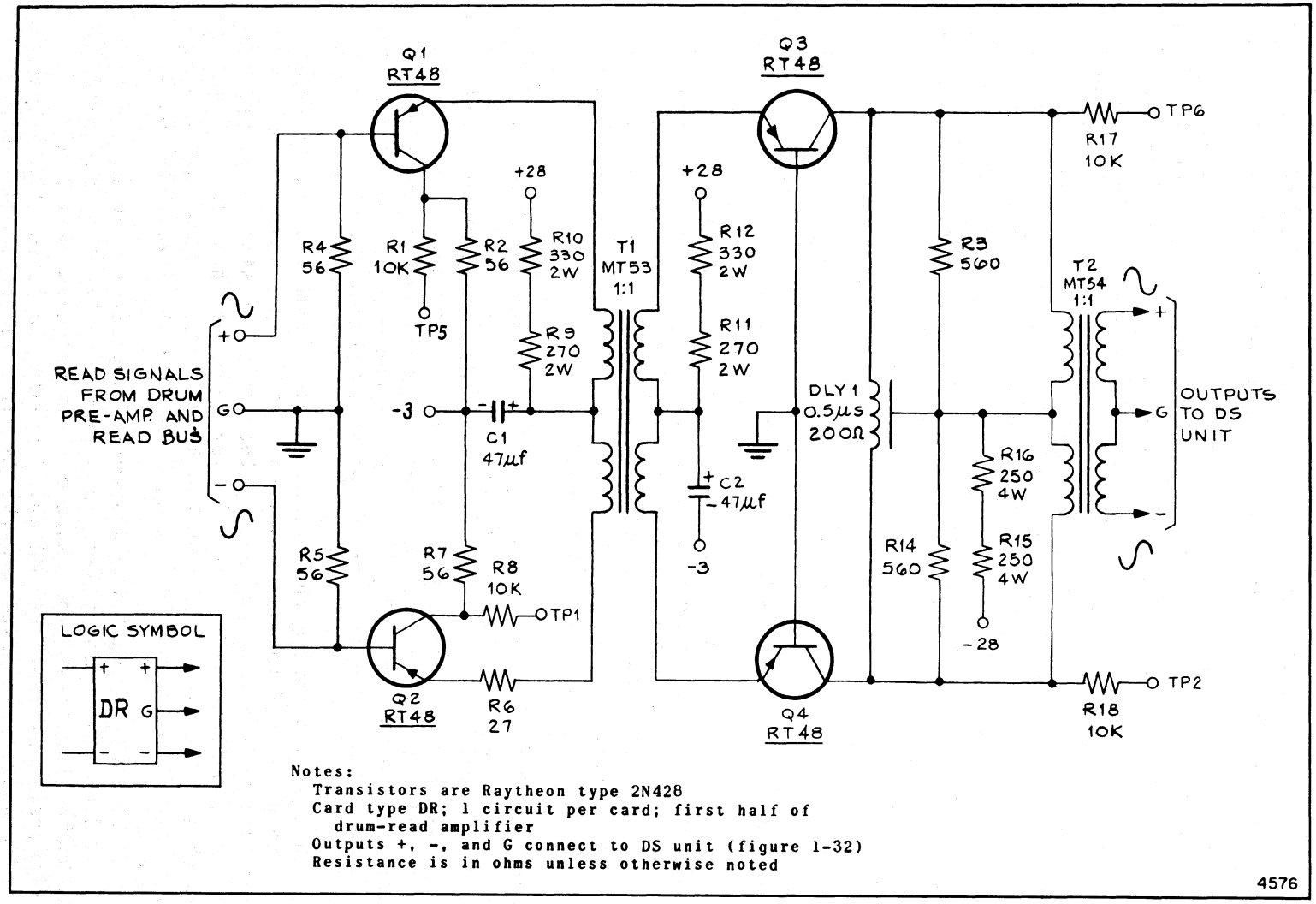
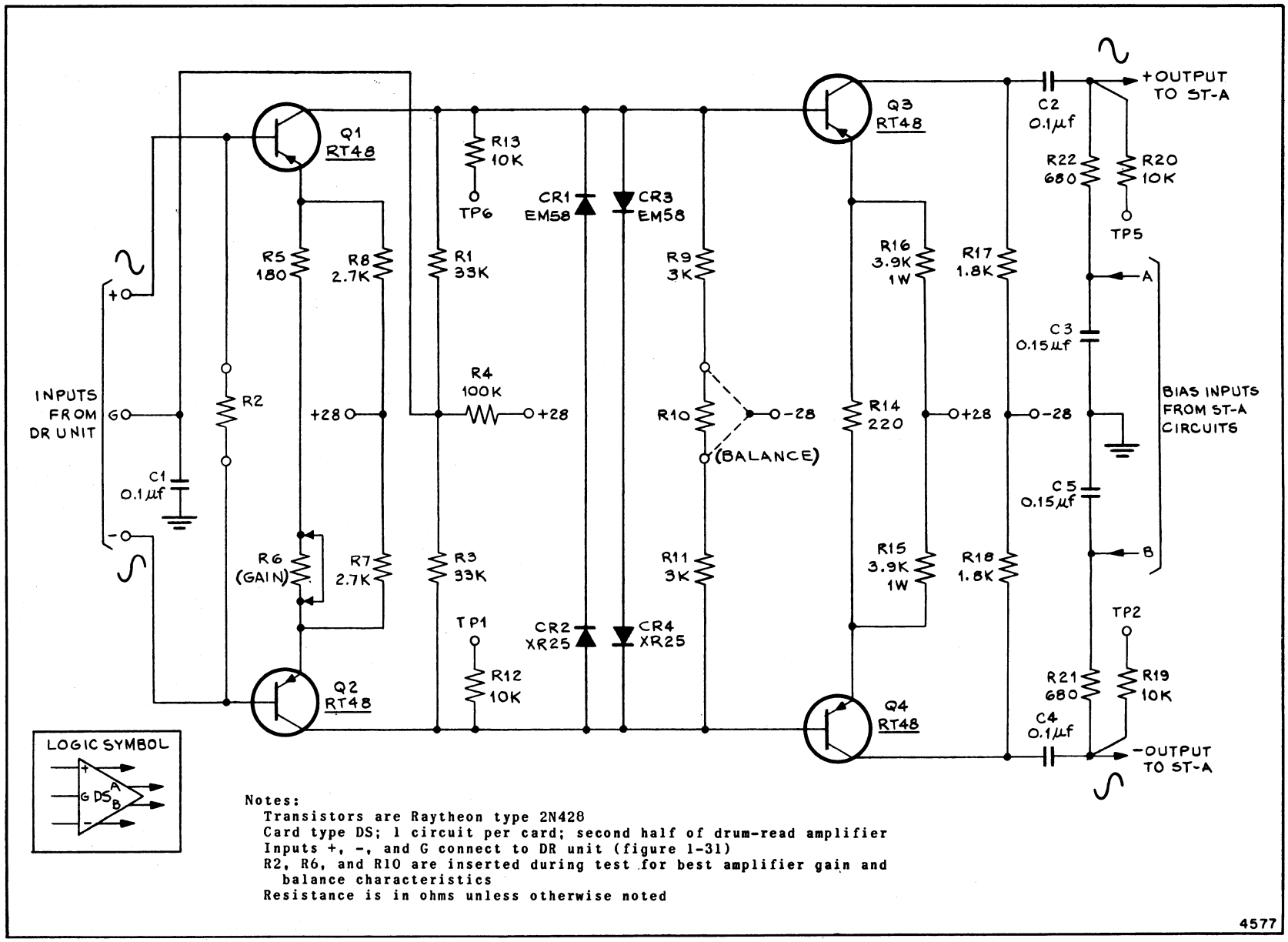


Figure 1-32. Drum Read Amplifier. Part 1



Notes:
Transistors are Raytheon type 2N428
Card type DS; 1 circuit per card; second half of drum-read amplifier
Inputs +, -, and G connect to DR unit (figure 1-31)
R2, R6, and R10 are inserted during test for best amplifier gain and balance characteristics
Resistance is in ohms unless otherwise noted

Figure 1-33. Drum Read Amplifier. Part 2

The inputs to each single-channel amplifier in a drum-read synchronizer can be switched to the output of a preamplifier on a corresponding channel in any one of the drums. The read bus is terminated at a drum-read synchronizer and a relay switching package is designed to minimize the length of unterminated stubs. It is important to keep these stubs very short compared to the wavelength at signal frequency (500 kc) so that their total effect will be a slight increase of capacitive loading on the preamplifier output. Since the read cable is balanced to ground, the synchronizer input is similarly balanced. If possible, the read cable shield should be grounded only at the read synchronizer, as indicated at terminal G in figures 1-31b and 1-32. At preamplifier output is the transformer winding of T3, which can float with respect to the preamplifier ground without inducing spurious signals, but the synchronizer input transistors (Q1 and Q2) could be saturated by ground currents which might carry their bases negative by 1 or more with respect to synchronizer ground.

Since the balanced read cable makes two phases of a drum read-back signal available at the DR input, and two phases of output are required to drive the Schmitt trigger circuits, a balanced structure is continued throughout the main read amplifier. The two phases of the signal are transformer-coupled up to the point where they are clipped, with each transformer driven push-pull and the secondary load balanced to ground. This arrangement affords a linear amplifier response to large signal swings and helps to maintain the correct phase of peaks and zero crossings.

Two transformers (figure 1-32) are used on the DR unit with a 1:1 turns ratio, and in each the primary and secondary are wound together as two strands of bifilar wire. Maximum coupling is obtained between primary and secondary, and the large capacitance between windings is not significant since it is not charged or discharged by signal currents.

The first transformer (T1) couples the emitter circuits of the first two transistors (Q1 and Q2) on each side of the balanced circuit. The two input transistors drive the primary in push-pull while the two second-stage transistors (Q3 and Q4), which are operated with bases grounded, provide a balanced load to the transformer secondary. The centertap of the primary is bypassed to ground through C1 but is presented with a relatively high d-c impedance, which sets the d-c operating point of the input transistors. The secondary centertap is bypassed, through C2, and has an equally high d-c impedance so that at zero signal the two second-stage transistors have essentially the same emitter current as the two input transistors.

The input transistors have their collectors returned to -3 v through small 56-ohm resistors (R2, R7), an arrangement which reduces the transistor collector dissipation. The 10-kilohm resistors (R1, R8) at the collectors of Q1 and Q2 provide isolated points at which the signal can be observed. The emitters drive approximately 27 ohms in series with the grounded-base input impedance of the second stage. This impedance is necessary to achieve the desired dynamic range, and it also reduces the variability of input impedance.

The second-stage collectors drive a push-pull coupling transformer (T2) and a delay line (DLY 1). The centertap of the transformer primary

is returned to the -28-v supply through two 250-ohm resistors (R15, R16). Any noise or distortion which is in phase at the opposite ends of the transformer primary appears as a voltage drop across these resistors, and only the undistorted signal reaches the delay line or the secondary winding. The delay line is connected from end to end to the transformer primary with its ground returned to the centertap. Both ends are terminated by the effective load across the transformer. Impedance variations of the third-stage transistor inputs (on the DS unit, figure 1-33) are damped by the shunt resistors across transformer, T2 (R13, R14). The push-pull drive provides equal signals of opposite phase at opposite ends of the delay line.

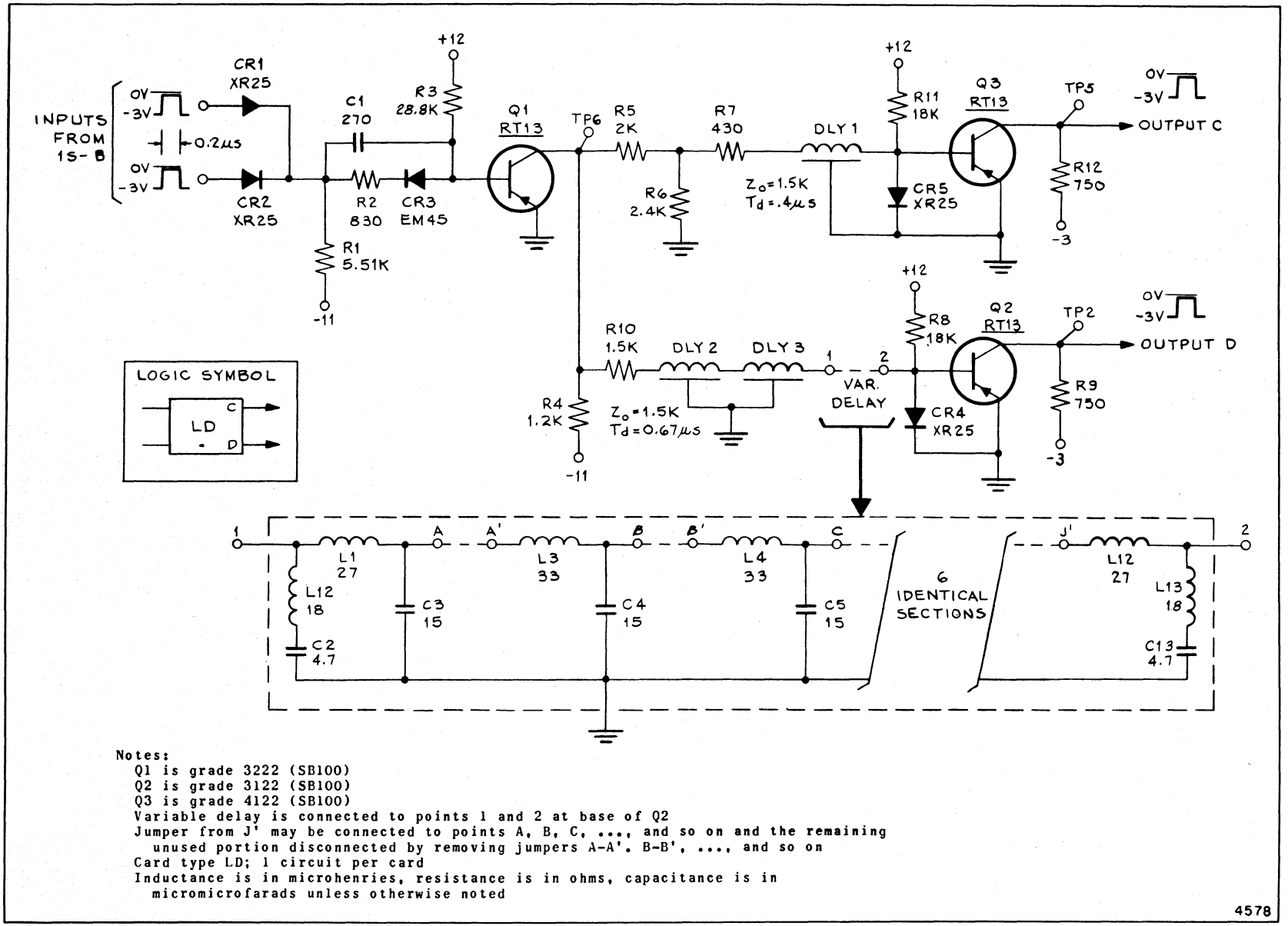
The output voltage from the delay-line load drives a pair of third-stage transistors (Q1 and Q2, figure 1-33) whose function is to amplify and limit the waveform. At this point the signal information is carried by the phase and timing at the zero crossings, and the shape of the remainder of the waveform can be safely disregarded. It is essential, however, that the portion clipped from the waveform by the limiters always center on the zero voltage line. This is achieved by cross coupling the collector circuits of Q1 and Q2 with diodes (CR1 ... CR4), so that the collector circuit impedance is high only when the third-stage collectors are within about 1.25 v of each other.

Since the two third-stage transistors are driven by opposite ends of the centertapped transformer winding of T2 (figure 1-32), the base potentials are equal only when the voltage across the transformer is zero. The two transistors are operated as a differential amplifier so that their collector voltages are equal when the base voltages are equal. A balancing adjustment (R10) is placed in the collector circuit to adjust for initial parameter differences. As indicated in figure 1-33, the value of resistor R10 is selected during the testing of the circuit, and a connection is made to one end of the resistor or the other to obtain the best balanced drive to the bases of the output transistors. This adjustment can be made by zeroing the d-c voltage difference between collectors of Q1 and Q2 under no-signal conditions, and it will be unaffected by subsequent drifting of supply voltages. Drift of other circuit parameters will not unbalance the circuit if both sides drift in the same direction.

A manual gain control is provided so that the system can be marginally checked by reducing gain during a maintenance period. This control (R6 in figure 1-33) varies the coupling resistance between the emitters of the differential amplifier (Q1-Q2). Normal gain setting is made by shorting out resistor R6 with a jumper. Subsequent changes in gain characteristics can be obtained by selecting suitable values for resistors R6 or R2, or both.

The d-c current-feedback arrangement (R1, R3, R4) (figure 1-33) is used to prevent too great a shift of the average collector-voltage level in the differential amplifier stage. The d-c component does not appear in the amplifier output signal, but it must be sufficiently controlled to avoid cut-off or saturation of individual transistors and to limit collector dissipation.

The fourth stage of the amplifier consists of another balanced pair of transistors (Q3 and Q4). Their emitters are coupled by a small fixed



Notes:
Q1 is grade 3222 (SB100)
Q2 is grade 3122 (SB100)
Q3 is grade 4122 (SB100)
Variable delay is connected to points 1 and 2 at base of Q2
Jumper from J' may be connected to points A, B, C, ..., and so on and the remaining unused portion disconnected by removing jumpers A-A', B-B', ..., and so on
Card type LD; 1 circuit per card
Inductance is in microhenries, resistance is in ohms, capacitance is in micromicrofarads unless otherwise noted

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Figure 1-34. Long-Delay Circuit

resistor (R14) to provide a low d-c impedance, while the d-c current is supplied by a high-impedance source for stability. Two separate outputs (+ and -) are supplied, each with approximately 500 ohms a-c impedance, to provide signals of opposite polarity to drive type-A Schmitt trigger circuits. Each output is coupled to a variable-bias voltage so that the output waveform can be centered around the set level of the associated Schmitt trigger. The d-c impedance of the bias network is always less than 800 ohms.

1-44. LONG-DELAY ELEMENT

The type-LD long-delay element provides two accurately delayed signals to meet the requirements of the self-sprocketing logic of the synchronizer. As shown in figure 1-28b, the long-delay element receives two positive-going inputs from type-1S-B gate inverters. It delivers a positive-going output signal to each side of an asynchronous flip-flop circuit, which uses two 1S-B inverter stages. The circuitry within the long-delay element consists of an input gate inverter similar to type 1S-B, two delay lines, and two output driver stages capable of driving a 1S-B circuit. For switching the circuit, therefore, 3 drive units (1.64 ma) are required at each input and output terminal of the delay element. Figure 1-34 is a schematic diagram of the complete circuit.

The input buffer stage (Q1) is similar to the standard 1S-B inverter circuit described under heading 1-5 (figure 1-3). The narrow input pulses (0.2 μs) generated in the preceding type-A Schmitt triggers are coupled through diode CR1 or CR2 to cause Q1 to cut off. As a result, a negative-going pulse will be applied to each delay line. The output stages Q2 and Q3 then will conduct to provide positive-going 3-v signals at outputs C and D. Because of delay line DLY 1 the output at C will be delayed about 0.4 μs with respect to the input at CR1 or CR2. Delay lines DLY 2 and DLY 3 and the variable delay will cause the output at D to be generated about 1.34 μs after an input.

The delay time from the input to the output at D is highly critical since it is during this time interval that the inhibit pulse (figure 1-28) is generated to block the unwanted (auxiliary) zero-crossing pulses. For this reason the variable lumped-parameter delay line is placed in series with the two distributed-parameter lines DLY 2 and DLY 3 so that tolerance variations can be more easily met. As shown in figure 1-34, the variable delay consists of nine constant-k T sections plus two half-π matching end sections. The delay presented by the variable portion of the line can be adjusted with jumpers to a value between about 25 and 225 mμs. Consequently the optimum circuit delay through the lower path will be 1.34 μs (2 x 0.67 μs = total delay of DLY 2 and DLY 3) $\pm$5 percent (variation supplied between points 1 and 2).

All the delay lines have a characteristic impedance of 1500 ohms and they are terminated at the input ends by resistors, so that any reflections from the output end (short-circuited by the bases of Q2 and Q3) will be absorbed. The short-delay path is terminated by the attenuator network composed of R5, R6, and R7; the long-delay path is terminated by R10. The diodes CR4 and CR5 across the base-emitter circuits of Q2 and Q3 keep the load impedance on the delay lines low even when these stages are biased in the reverse direction.

The resistive network (R5, R6, R7) in series with the short-delay line (DLY 1) is a constant-impedance attenuator which assures that the amplitude of the signal at output D will always be greater than the output at C for very narrow (spike) inputs. If a sneak pulse were to be propagated through to output C with less attenuation than the corresponding signal from output D, the flip-flop in the self-sprocketing logic circuit (figure 1-28) would be set but would not reset again and would block all further inputs to the long-delay circuit. The amount of attenuation provided by the resistive network guarantees that the peak value of the spike at output C will not exceed -1.5 v when the peak value of output D is set to -1.2 v and both output transistors have equal betas and rise time.

1-45. TUNE-UP PROCEDURE FOR SELF-SPROCKETING LOGIC CIRCUITS

The correct functioning of the self-sprocketing circuits in the drum synchronizers is highly dependent on the relative timing and position of the pulses at various points in the logic network. The following procedure outlines the measurement technique for adjusting the circuit to optimum operating conditions. Use a Tektronix 546 type oscilloscope.

This procedure goes on the assumption that all necessary card types are in place in the synchronizer, as shown in the block diagram of figure 1-28b. For a driving source use a sinewave oscillator connected to a type-MT54 transformer. The transformer is needed to supply the required balanced input waveforms to the circuit, as shown in the figure. This is the procedure for adjusting the circuit:

(1) Eliminate the first stages of the drum-read amplifier by removing the type-DR card from the circuit.

(2) Connect outputs from the oscillator-transformer combination to the + and — inputs of the second part of the drum read amplifier on the card type DS.

(3) Synchronize the oscilloscope by connecting the output from one of the two Schmitt triggers (ST-A) to the external synchronization terminal on the oscilloscope.

(4) Use alternate oscilloscope sweeps to display both the sinewave input to the DS amplifier card and the ST-A output pulse.

(5) Adjust output from the oscillator for a small input-signal amplitude to the amplifier, but not too small that it will fail to trigger the Schmitt trigger. In addition, the use of a low-frequency input signal of about 7500 cps minimizes the effect of variation of delay through the circuits.

(6) Adjust the bias-level output (B) from the ST-A(1) card so that the negative-going output pulse from the ST-A circuit occurs at the same time as the positive-going zero crossing of the input sinewave at the DS input of the drum read amplifier. The bias level is adjusted by selecting a suitable value for resistor R16 (figure 1-15) in the ST-A circuit.

(7) Repeat step (6) for the ST-A(2) circuit.

(8) Use alternate oscilloscope sweeps to display the ST-A output pulse (either ST-A(1) or ST-A(2)) and the output inhibit pulse from the 1S-B circuit of the flip-flop.

(9) If the output signal observed from the flip-flop remains high, reset the flip-flop circuit manually.

(10) Observe and measure the interval between the leading edge of the ST-A output pulse and the trailing edge of the inhibit pulse from the flip-flop. The optimum delay interval is 1.605 μs.

(11) If the delay is not optimum, remove the type-LD long-delay card and select a suitable tap on the adjustable portion of the variable delay line (figure 1-34) to get the optimum delay. The sinewave oscillator should be set to a frequency of about 150 kc for this adjustment.

1-46. TYPE-CNR COUPLING CIRCUIT

The type-CNR circuit is a special coupling circuit that has a unique application in the drum write-synchronizer logic. As shown in figure 1-35, the circuit is used for coupling the large-signal output from a type-R1 low-speed driver unit to a type-1S gate-inverter circuit. Resistors R1, R2, and R3 form a constant-current coupling network between isolating diode CR and the input to the following stage.

When the input signal rises toward the zero reference level, CR conducts in the forward direction through R1 and the input voltage at the top of R1 rises from about -6 v to about -0.6 v. The voltage step-up through R2 then causes the output to rise to about -0.3 v, which is the normal input level for switching the following 1S circuit to the off state.

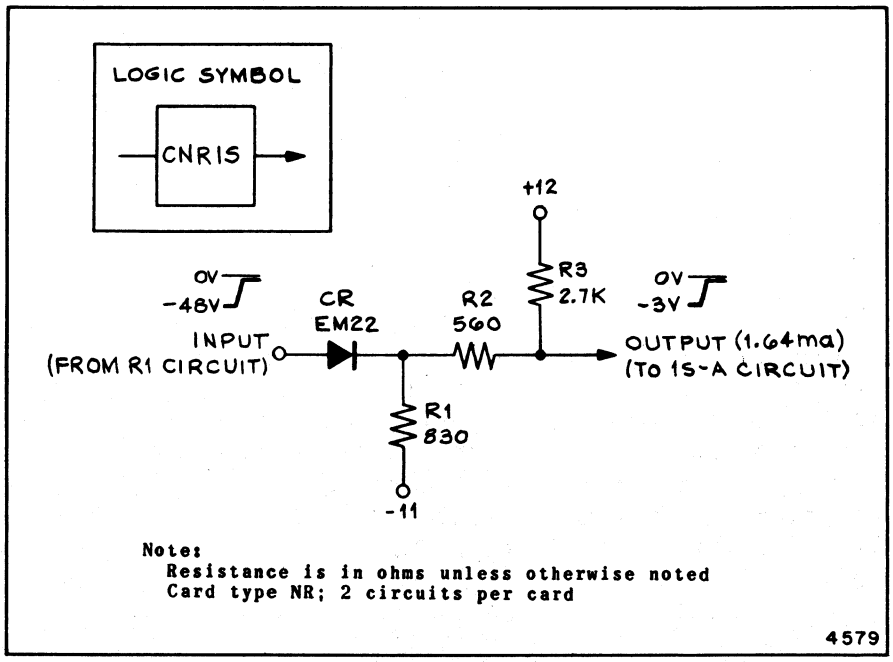


Figure 1-35. Type-CNR Coupling Circuit

The CNR circuit is supplied as card type NR, which contains two coupling circuits per card. However, since this circuit only provides a testable signal for use within a drum write synchronizer, there is only one such circuit in the entire basic system.

1-47. TAPE-SYNCHRONIZER CIRCUITS

The tape synchronizer contains several unique circuit packages for use in controlling the operation of the Uniservo II magnetic-tape unit. Among these circuits are (1) output drivers for writing on tape, (2) input, trigger, and gain-control amplifiers for reading from tape, (3) a tape-motion-control circuit, (4) a logic-checking circuit, and (5) various coupling networks. The special circuit types that have been developed for use in the tape read-write synchronizer logic are listed here. Most of them are in the processor card library. (The second half—the output stage—of the tape write amplifier and the centerdrive-control circuit are located in the Uniservo power-supply cabinet.)

Type-TW tape write amplifier

Type-TR tape read amplifier*

Type-GN gain-control network

Type-ST-E Schmitt trigger*

Type-CDC centerdrive-control circuit

Type-NS tape-selector checker

Type-VT tube driver*

Type-CNC and -CNE coupling networks*

* These circuits are also used in the line-printer synchronizer.

After a brief description of the tape read-write system each of the preceding circuit types is described in detail (headings 1-49 through 1-54), except the Schmitt trigger circuit (ST-E) (heading 1-27) and the tube-driver circuit (heading 1-33).

1-48. TAPE READ-WRITE SYSTEM: GENERAL DESCRIPTION

The standard recording method used in the Larc application of the Uniservo II magnetic-tape unit is the return-to-zero system. In this system a 1 is represented by a small saturated area of the magnetic material on the tape in one direction; a 0 is represented by a similar area in the opposite direction. The recording current is always returned to—or allowed to remain in—zero polarity before the end of each bit cell—that is, before the end of the interval allowed for recording each information bit.

Each of the eight channels†† in the Uniservo head assembly independently writes or reads information in an associated track on the moving tape.

†† Seven information channels for Univac code, and one sprocket channel.

A separate erase head saturates the entire width of magnetic material on the tape in the zero polarity before the tape passes the recording head on a write operation. In addition to producing the correct recording polarity, this arrangement insures the removal of all residual magnetism from the tape before writing.

The tape synchronizer must control all reading and writing operations on a tape unit so that they will be synchronized to the information flow within the processor. For output write operations the synchronizer contains a group of eight tape write amplifiers (one for each track on the tape) that produce the required write-current waveforms for recording on a tape. Figure 1-36a shows a simplified diagram of the output write circuit for one channel. Operation of the other seven channels is identical to, and occurs in parallel with, the sample channel.

A negative-going information pulse from an output pulseformer-type flip-flop is inverted by a 1C circuit and applied as a high signal (representing a 1) to the type-TW tape write amplifier. The first stage of this amplifier is located on a standard printed-circuit card in the synchronizer module of the processor card library. The second (output) stage of the TW unit, however, is located in the Uniservo power-supply cabinet. As shown in figure 1-36a, the two parts of the amplifier are connected by a coaxial cable of not more than 60 feet in length. The positive-going output from the second stage then is connected through another coaxial cable to the Uniservo, where it is applied to the head coil for writing on the associated channel.

The Uniservo can accommodate either high-quality plastic tape or the metal tape which was developed especially for the Univac system. Plastic tape requires a lower recording current than metal tape does. When plastic tape is used, a metal-plastic single-throw switch on the Uniservo is closed and the write current passes through a 150-ohm current-attenuating resistor in series with the head coil (figure 1-36a). This operation is implemented by the controlling of a relay which has a set of eight normally closed contacts. For a plastic-tape operation the switch is closed and the relay contacts open to allow current to pass through the resistor. For a metal-tape operation the switch is open and the relay contacts are closed in order to bypass the resistor.

For use in the Larc and other systems the tape synchronizer is capable of controlling the tape recording density so that information may be written at either 100 or 200 pulses per inch. Since the tape is driven at a constant speed of 100 inches per second, the pulse repetition rate (PRR) for recording and reading will be either 10 kc or 20 kc, depending on the program-controlled density parameter.

Figure 1-36c shows a typical series of write-current pulses and readback voltage waveforms for the two recording rates. Notice that the output current from the tape write amplifier has a nominal peak-to-peak value of 100 ma for metal tape. For plastic tape the head current is reduced about 40 percent to 60 ma peak-to-peak. At the 20-kc rate the period for each bit cell is 50 μs with a 50-percent duty cycle used for recording information. For the lower density (PRR: 10 kc) a pulse of 50-μs duration is needed to record information. As mentioned four paragraphs earlier, these pulse times are controlled by the synchronizer logic circuitry in response to instruction signals from the processor.

To summarize: in the absence of an output pulse that represents a 1 (low input to TW unit) a head channel writes zero or erase polarity in its associated channel of the tape. To record a 1 a reverse-current pulse is applied to the read-write coil. The pulse reverses the direction of polarization of the magnetic tape and the current returns to zero polarization before the time for recording the next bit.

For input read operations the synchronizer contains a group of eight tape read amplifiers and associated Schmitt trigger circuits. These circuits amplify and convert the readback-voltage waveforms from the head coils in the Uniservo to the standard 3-v d-c levels of the synchronizer logic. Also associated with the input circuits of the synchronizer is a group of three gain-control networks that provide for the variable-gain feature of the tape read amplifier. A single-channel diagram of the read circuit is given in figure 1-36b.

Magnetized areas on each track of the tape induce small voltages in the head coil which are proportional to the time derivative of the flux pulses on the tape. The voltage waveforms therefore vary directly with the strength of magnetization and tape speed. The strength of magnetization in turn depends on conditions present during recording. A 1 in the return-to-zero system therefore is read out as a series of two voltage pulses of opposite polarity. (See waveforms 2 and 4, figure 1-36c.) The time between the broken lines corresponds to one bit of information and is only a function of pulse repetition rate. The space between the two halves of the voltage waveform is a function of the pulse-packing density on the tape.

On a read operation the head coil is connected through a gain-control potentiometer to a shielded cable which connects the read signal to the synchronizer input. The cable is a twisted-pair of conductors with low capacity, and is not more than 100 feet in length. A relay-switching network (not shown in figure 1-36) is also used to connect the outputs from different Uniservos to the read amplifiers. Since the head coil is an integral part of each Uniservo head assembly, the gain adjustment is provided at the source to compensate for individual tolerances associated with each channel. The gain is varied with a 100-ohm potentiometer and a 1000-ohm resistor, which are connected in series across the head coil. The potentiometer is adjusted initially against a standard calibration tape which allows for widest possible tolerances.

The input signal to the synchronizer is fed through the type-TR tape read amplifier where it is amplified from 600 to 3200 times, depending on gain requirements. The TR unit is a direct-coupled, four-stage, variable-gain amplifier that employs negative feedback for improved stabilization. As indicated in figure 1-36b, the nominal peak-to-peak signal from the read cable is 5 mv for plastic tape and 10 mv for metal tape. The nominal output from the amplifier will range between 6 v peak-to-peak and 16 v (peak-to-peak), which is sufficient to trigger the following type-ST-E Schmitt trigger circuit. As described under heading 1-27, the ST-E circuit functions on the positive-going portion of the readback-voltage waveform from the TR amplifier to produce an accurately-timed, negative-going, 3-v pulse, which is applied to an input asynchronous-type flip-flop in the synchronizer logic circuitry.

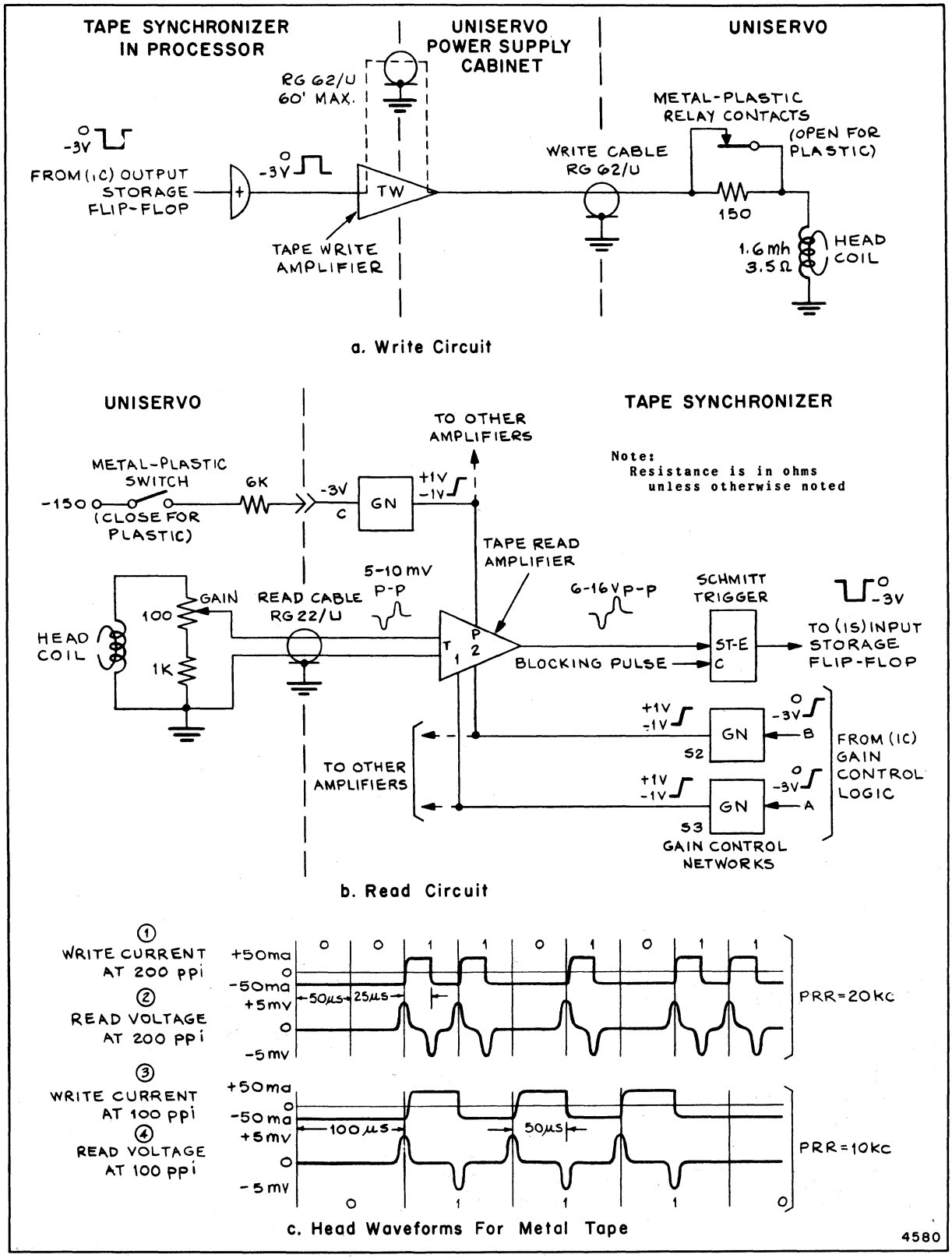


Figure 1-36. Tape Read-Write System (One Channel)

The wide variation in gain in the read amplifier is obtained with the help of the type-GN gain-control networks, which are connected between the gain-control logic circuits of the synchronizer and special input terminals (P, 1, and 2) on the TR read amplifier. Information signals fed into the tape synchronizer are always checked for errors. If an error is indicated, the gain of the read amplifier will be changed automatically from normal to a higher or lower setting to provide output levels at one eighth or one third of the standard signal amplitude. For normal gain the output level is set for one fifth of the standard signal amplitude. At this level the amplifier safely passes all normal signals and blocks out noise pulses of average amplitude. At the low-gain setting the level is set to one third of the standard signal amplitude so as to pass normal information but block above-average noise. The high gain conditions establish the output level at one eighth of standard amplitude and thereby enable the amplifier to pass low-level information signals but still discriminate against average noise.

Whether the tape read amplifier operates at a normal-, high-, or low-gain setting is a program-controlled parameter which is implemented by gain-control logic circuits in the synchronizer. As indicated in figure 1-36b, the signals from the (1C) gain-control logic are coupled to the inputs of two GN gain-control networks that employ emitter-follower-type transistor circuits. The outputs from the GN units are connected in parallel to terminals 1 and 2 of the eight read amplifiers. The amplifiers will operate in the normal-, high-, or low-gain mode in accordance with the relative polarities of the signals received from the gain-control networks.

Another factor which enters into the over-all gain of the read amplifier is the use of plastic tape. Since the output signals received from plastic tape are of smaller amplitude than those from metal tape, additional gain must be provided in the amplifier when plastic tape is used. The additional gain is manually obtained by means of the metal-plastic switch on the Uniservo. For plastic-tape operations the switch is closed to provide a low signal to the input P terminal of the tape read amplifier. In this case the signal is fed through a purely resistive-type gain network in order to supply the correct voltage levels to the amplifier. Consequently the total combination of different gains available through the read circuit is six: three (low, normal, high) for metal tape and three for plastic tape.

1-49. TAPE WRITE AMPLIFIER

Figure 1-37 is a schematic diagram of the type-TW tape write amplifier. As mentioned in paragraph 4 under heading 1-48, the two stages of the amplifier are physically divided: the first stage is in the tape-synchronizer module of the processor and the output stage is in the Uniservo power-supply cabinet. The input stage Q1 is a conventional inverting amplifier which uses a medium-power PNP junction transistor (Philco type 2N597). The transistor is normally biased to the conducting state by means of the resistive voltage step-up network consisting of R1, R2, R3, and the supply voltages. Thus, with no input signal present, diode CR1 is reverse-biased and Q1 is conducting. This action is similar to previously described constant-current, base-input coupling circuits (types 1C, P1, and R1).

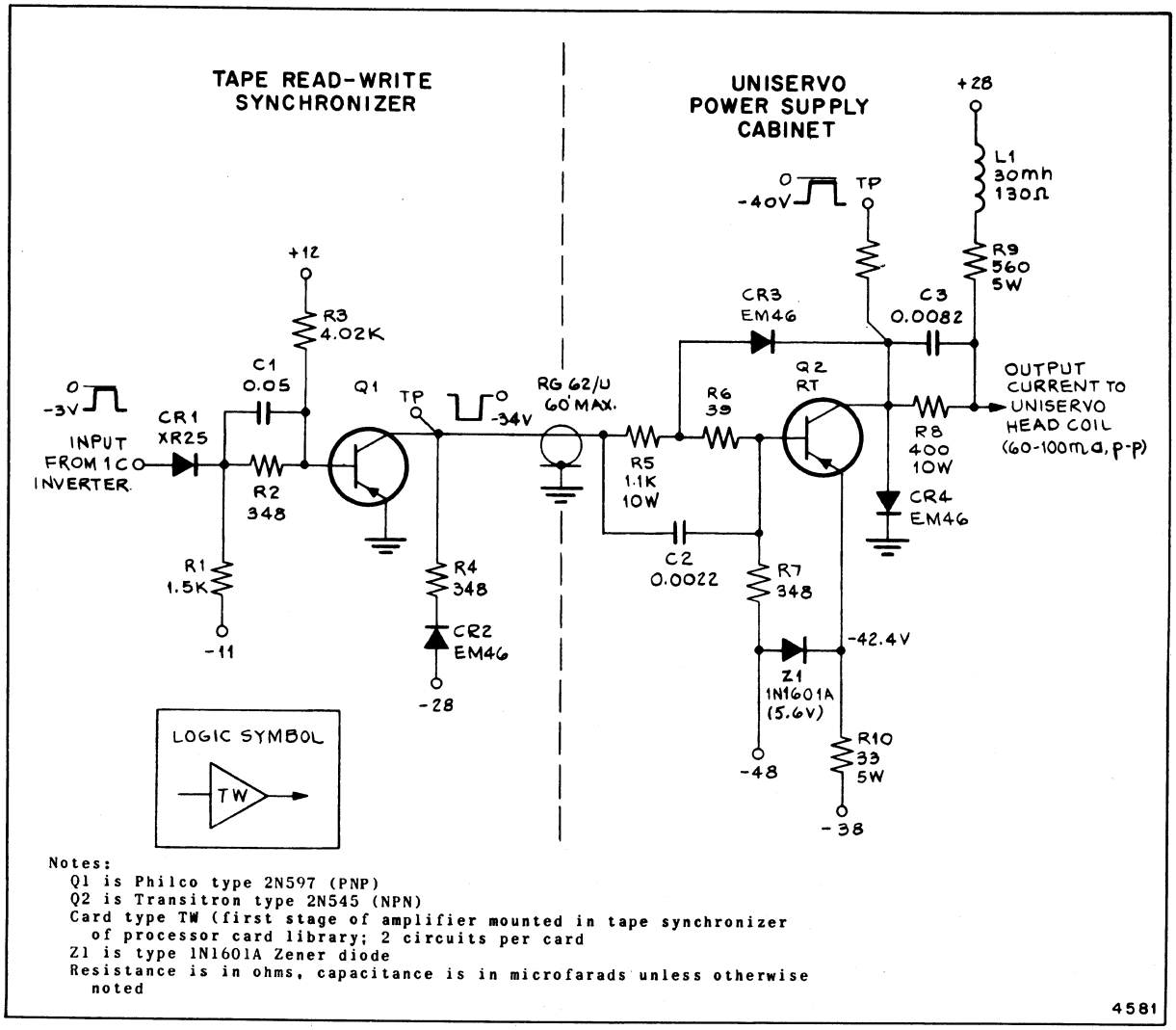


Figure 1-37. Tape Write Amplifier

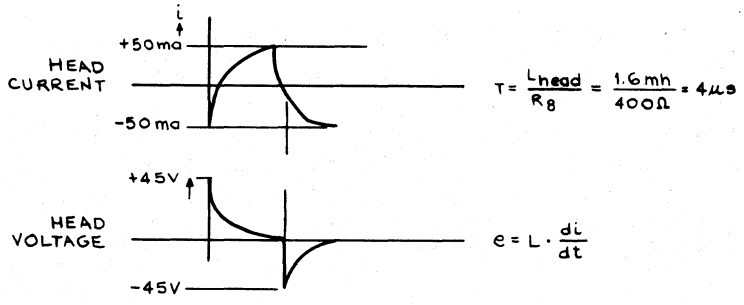
With Q1 conducting, the collector output potential will rise toward the level of ground potential to provide a relatively positive input to the second stage of the amplifier, Q2. The output stage uses an NPN junction transistor (Transitron type 2N545) because of the availability of relatively large negative d-c voltage supplies. Consequently, with Q1 conducting, the base of Q2 will be slightly positive with respect to the emitter so that Q2 will also be conducting. This action will cause a relatively negative signal to be present at the collector output terminal of Q2.

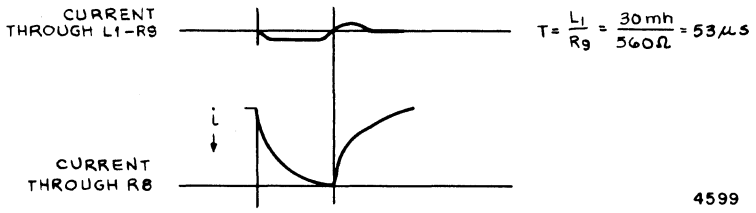
The voltage level at the output of the amplifier will be approximately -40 v. This level is established mainly by the zener regulating diode Z1 connected across the base-emitter circuit of Q2. Z1 is a type-1N1601A zener diode. It has an initial tolerance on breakdown voltage of between 5 and 6 v; the nominal value is 5.6 v. As indicated in figure 1-37, this diode is connected to the -48-v source so as to establish a potential of -42.4 v at the emitter of Q2. The single zener diode is capable of supplying enough current for the output stages of the eight tape write amplifiers.

When Q2 is conducting, current flows from the -38-v source to ground, through the read-write head coil in the Uniservo (figure 1-36a), and back to the collector-emitter circuit of Q2 through the write cable and resistor R8. The bottoming potential of Q2 and the drop across R8 will limit the voltage swing at the collector to about -40 v. The feedback diode CR3, connected from collector to base, limits the saturation current of Q2 and thereby improves the response during switching. This action is similar to that of other circuits—type-VC tube driver (heading 1-34) and -DS drum read amplifier (heading 1-41). Capacitor C3 also speeds up the transient response of the output waveform by providing an initial surge of output current when the transistor is switched to the conducting state. Without this initial surge of output current the output signal would have a slower rise time.

When circuit conditions are as just described, the direction of the current through the head coil is such that it saturates the tape in the erase or 0 direction. In order to record a 1, both transistors in the TW unit must be switched to the cut-off state. The output waveform will change to a positive-going pulse with a duration equal to the duration of the input information pulse from the synchronizer. A positive-going signal from the 1C inverter circuit will cause CR1 to conduct through R1. The increased input current will result in raising the potential at the base of Q1 toward ground so that the base-emitter circuit will be biased in the reverse direction. Q1 will be cut off, and its output collector potential level will drop to about -34 v, as established by means of the path to the -48-v source in the power-supply cabinet.

The negative-going pulse from Q1 is coupled through the coaxial line (type RG62/U) to the input base circuit of Q2 and cuts off the output stage. In this case the input voltage change causes the base to become slightly more negative than the emitter so that the base-emitter diode is reverse-biased, and conduction through the transistor stops. When Q2 is off, an output current will flow from the +28-v supply through L1 and R9 to the head coil in the Uniservo, and back through ground. The collector voltage is limited to about the level of ground potential by the clamping diode CR4. The series inductance-resistance network (L1-R9) in the collector return circuit has a time-constant which is about 14 times as large as the time constant of R8 and the head coil inductance of 1.6 mh. The current through the L1-R9 path is about 50 ma and can be considered to be constant because of the large time constant. Therefore, both rise and fall times of the current through the head are determined by the time constant (L head/R8) and both are about 4 μs. (See the following waveforms.) Capacitor C3 helps the switching characteristics of the output signal by discharging rapidly through the head coil and emitter-collector circuit of Q2, thereby reducing appreciably the turn-off time.





1-50. TAPE READ AMPLIFIER

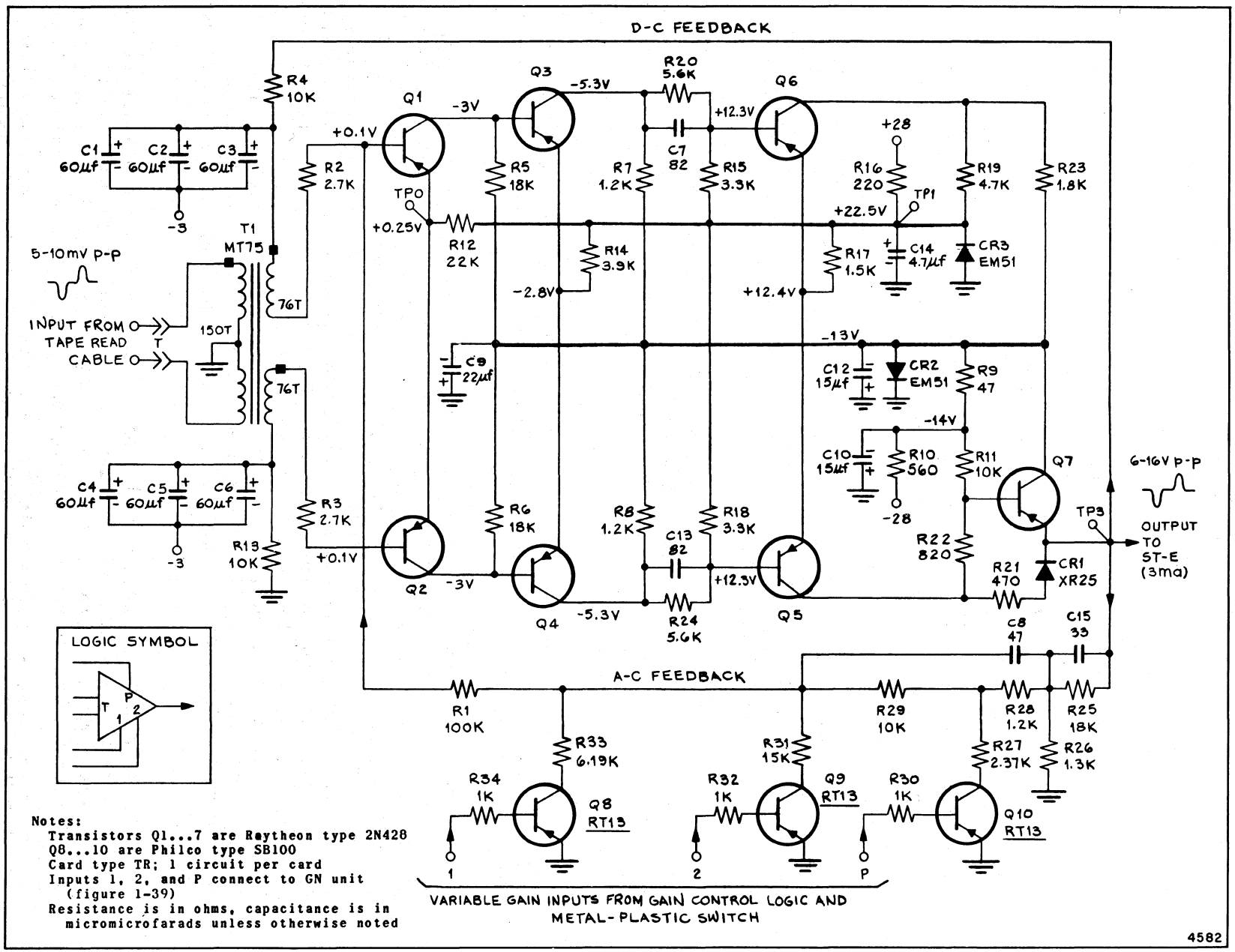
The tape read amplifier (figure 1-38) uses a direct-coupled push-pull circuit design which includes both d-c and a-c feedback paths for stabilization and variation of the gain setting. The amplifier is packaged as card type TR; the complete schematic diagram of the card is given in figure 1-38. The circuit is direct-coupled throughout in order to provide the best low-frequency response. Good response at the low end of the passband is necessary because in the return-to-zero recording system some of the channels on the tape can remain idle for appreciable lengths of time. The high-frequency response is relatively flat out to 125 kc, which is more than adequate for amplifying-frequency components up to the fifth harmonic of the highest basic tape-signal frequency of 20 kc.

The main amplifier consists of the three-stage push-pull circuit which uses transistors Q1 ... Q6 and which provides a gain of approximately 50 in each stage. This high amplification is obtained by using Raytheon type-2N428 transistors (beta > 60) throughout the amplifier. Thus the over-all open-loop current gain of 125,000 will be more than sufficient for supplying the highest required closed-loop gain of 3200, which occurs at the high gain setting for plastic tape. Push-pull circuits are used to obtain a minimum amount of delay through the amplifier and also to permit a simpler method for stabilizing the output.*

Other features of the circuit are the low-impedance emitter-follower output stage Q7, the d-c feedback path which provides for a d-c reference point for stabilizing the output to that required by the following Schmitt trigger stage, and the a-c feedback path which includes the resistive ladder network controlled by transistors Q8, Q9, and Q10. This network provides the variable-gain feature of the amplifier by switching more or less resistance in parallel with the feedback path. For example, if the inputs to the bases of Q8, Q9, and Q10 are all high so as to cut off the three transistors, there will be minimum shunt resistance in the feedback circuit. This minimum resistance will allow maximum negative feedback current to be applied at the input of the amplifier so that it will operate at the lowest gain.

The two phases of input signal from the balanced read cable are coupled to the bases of the first-stage transistors (Q1 and Q2) through the 1:1 input transformer T1. The first stage functions as a stabilizing amplifier since the base of Q1 is returned through one half of the secondary of T1 to

* Push-pull connections reduce the discharge time of the interelectrode capacitances within the transistors because the RC time constant of the collector-emitter circuit is much shorter than the collector-base time constant of a single-end stage.



Notes:
Transistors Q1...7 are Raytheon type 2N428
Q8...10 are Philco type SB100
Card type TR; 1 circuit per card
Inputs 1, 2, and P connect to GN unit (figure 1-39)
Resistance is in ohms, capacitance is in micromicrofarads unless otherwise noted

Figure 1-38. Tape Read Amplifier

the d-c feedback loop from the output, while the base of Q2 is returned through the lower half of the secondary of T1 to ground. Thus any deviation at the amplifier output from the ground reference point established at the base of Q2 will be automatically corrected by means of the negative feedback signal at the base of Q1. Ground is used as the d-c reference point to coincide with the near-zero crossing point (-0.1 v) at which the following Schmitt-trigger stage is set.

The d-c feedback resistor R4 is selected at 10,000 ohms to provide a compromise value which does not overload the amplifier output while it limits the voltage drop across it, in accordance with the minimum base current required by the first stage. The nominal base current of the high-gain transistors in the first stage is about 8 μa, which results in an 80-mv drop across the feedback resistor. Under the worst operating conditions, the maximum error at the output of the amplifier (offset tolerance from ground reference) due to base current and base-to-emitter potential variations is about ±70 mv. The large electrolytic capacitors (C1 ... C6) connected across the base circuits of Q1 and Q2 are used for decoupling and determine the low-frequency roll-off characteristics of the amplifier. Because of the potential variations just indicated, all the capacitors are returned to -3 v to insure that correct polarization is maintained across them.

The outputs from the collectors of Q1 and Q2 are directly coupled to the bases of the second stage of the push-pull arrangement. The emitters of Q3 and Q4 are returned through a common 3900-ohm resistor R14 to the +22.5-v supply to provide sufficient current for driving the voltage-divider network to the next stage. The voltage dividers are used to bring the bases of the third-stage transistors Q5 and Q6 up to a quiescent voltage of +12.3 v from the negative level at the collectors of Q3 and Q4. Speed-up capacitors C7 and C13 are added for minimum delay through the circuit.

The final push-pull stage is connected to provide a single driving source for the emitter-follower output stage Q7. The collector current from Q5 is divided by R21 and R22 between the emitter and the base-return resistor R11 of Q7. R21 and R22 keep this current independent of the output load current so that a constant current is maintained through the common emitter resistor R17 of the last push-pull stage. This action also tends to provide a constant positive clipping level of about +11 v which is independent of the load. Base resistor R11 is returned to a source that is 1 v more negative than the collector of Q7 in order to supply enough base current for sharp negative clipping. The nominal value of the negative clipping level is -13 v.

Diode CR1 is an isolating device that limits the current drained from the base of Q7 when the transistor is saturated. The output at the collector of Q6 of the last push-pull stage is dissipated in the voltage-divider resistances consisting of R19 and R23. These resistors are chosen so that the output from the driving transistor Q5 will cut off before Q6 saturates. The current for the positive alternations of the output-signal waveform is supplied by the collector of Q5, while the negative alternations are handled by the emitter current from Q7. As indicated in figure 1-38, the nominal peak-to-peak output-signal amplitude will vary from 6 to 16 v at an average current of 3 ma, and the d-c output impedance will always be less than 100 ohms.

The over-all closed-loop gain of the amplifier is controlled by the a-c feedback network connected between the emitter output of Q7 and the base input of Q1. The three gain switching circuits (Q8, Q9, and Q10) are connected across a resistive ladder network to control the magnitude of the feedback current. The bases of Q8 and Q9 are respectively the number 1 and 2 input terminals of the amplifier that are fed from the gain-control networks in the synchronizer.* Q10 is coupled from input terminal P through another gain-control circuit to the plastic-metal tape-selector switch in the Uniservo (figure 1-36b). The input level at each transistor base is either +1 v or -1 v; it depends on whether the output from the associated gain-control network is high or low. If the level is at +1 v, the transistor will be cut off and more current will be fed back to the input of the amplifier to give less over-all gain. Conversely, a negative input voltage will allow the transistor (type RT13) to conduct so as to present a low impedance and thereby divert some of the feedback current to ground. With less negative feedback, the gain of the amplifier will increase proportionately. Table 1-9 lists the relative and absolute gains of the amplifier for both metal and plastic tape operations. In addition, the table shows the reset level of the Schmitt trigger circuit (fraction of the amplifier-output peak-signal amplitude) at high, normal, and low relative gain settings, the feedback factor (F) for the gain-control ladder network, and the logical significance of the outputs of the type-GN gain-control networks in the synchronizer.*

Table 1-9. Gain Settings for Tape Read Amplifier

Tape	Relative Gain	Absolute Gain	Reset Level of ST-E	Level at Input 1†	Level at Input 2†	Level at Input P†	F††
Plastic	High	3200	1/8	Low	High	Low	0.011
	Normal	2000	1/5	High	Low	Low	0.018
	Low	1200	1/3	High	High	Low	0.034
Metal	High	1600	1/8	Low	High	High	0.023
	Normal	1000	1/5	High	Low	High	0.037
	Low	600	1/3	High	High	High	0.068

† Logical significance of the outputs of the type-GN gain-control networks in the synchronizer.

†† $F = V_f/V_o$

F: Feedback attenuation factor
V_f: Voltage at output of feedback network
V_o: Voltage at output of amplifier

The design of the feedback network is facilitated by making the open-loop gain of the amplifier as large as possible; in fact, for purposes of calculation the gain can be considered infinite. To prevent excessive loading of the circuit, the feedback resistor R1 is much larger in value than any other resistor in the ladder network. The gain switching transistors (Q8, Q9, and Q10) also must be either fully conducting or completely off to insure correct operation of the network. For this condition the type-GN gain-control networks are used as coupling circuits between the synchronizer logic circuits and the feedback loop in the amplifier. Since the output voltage can swing both positive and negative, the bias voltage at the bases of the gain switching transistors must also be capable of

* The type-GN gain-control networks are described under heading 1-51.

going above ground. Thus the purpose of the gain-control coupling network is to convert from standard levels (-3 v to ground) to levels of ±1 v (figure 1-36b).

In operation the feedback current from the output of the amplifier is divided first by the permanent voltage divider consisting of R25 and R26. The current then is further divided by an amount that depends on how many of the gain switching transistors are conducting. The purpose of capacitors C8 and C15 across the divider resistors is to balance out any stray capacitances that exist between the feedback network and ground. Such compensation will aid in maintaining maximum stability of the output signal.

1-51. GAIN-CONTROL NETWORK

The schematic of the type-GN gain-control network is shown in figure 1-39. The schematic represents the complete GN card type, which is a composite of the three GN circuits associated with each tape read-write synchronizer—that is, a total of three GN circuits is used in the synchronizer logic circuitry (figure 1-36), and the three circuits, two alike and one different, are packaged on the same card. Although the tape synchronizer logic drawings indicate three similar GN circuit types, the one that couples the output from the metal-plastic selector switch is different from the others. The difference is easily identified in figure 1-39, where emitter-follower transistor stages Q1 and Q2 are used to couple from the gain-

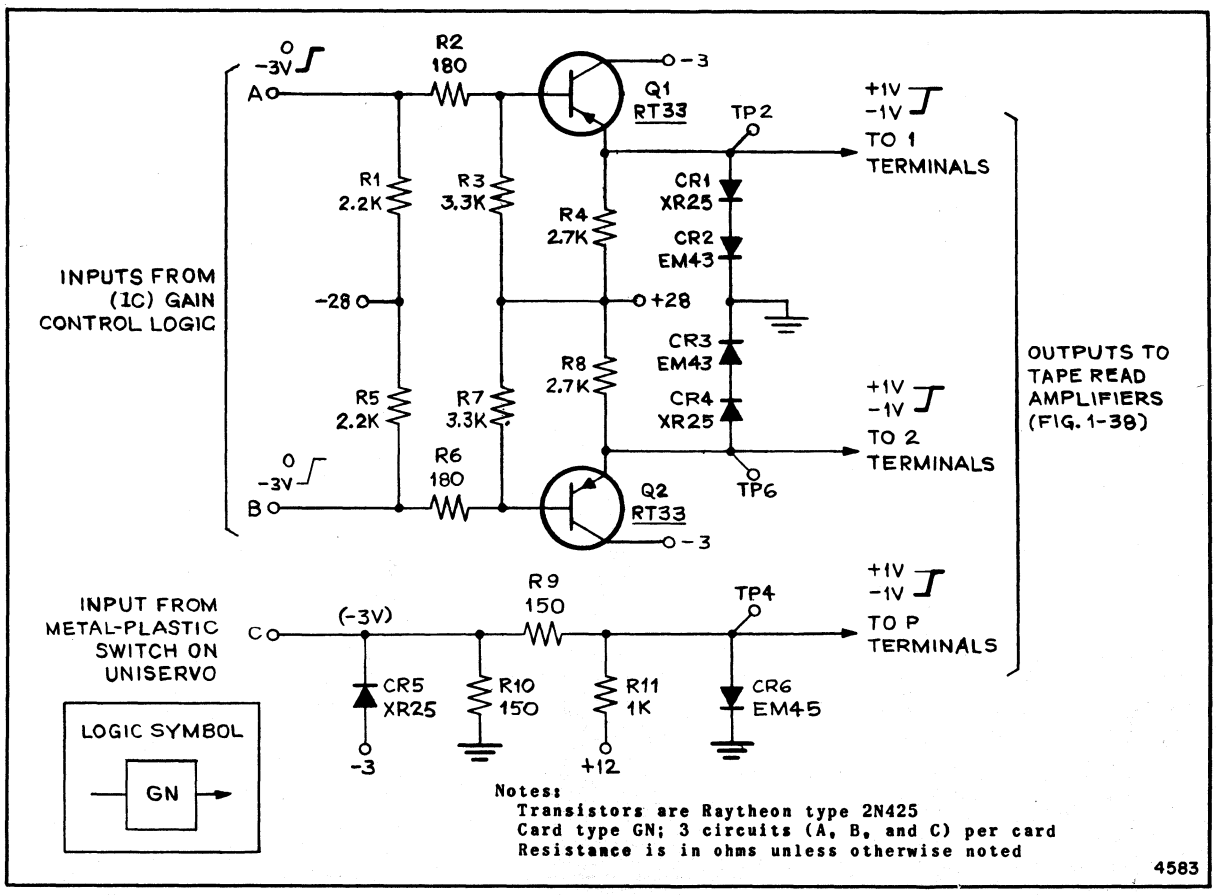


Figure 1-39. Gain-Control Network

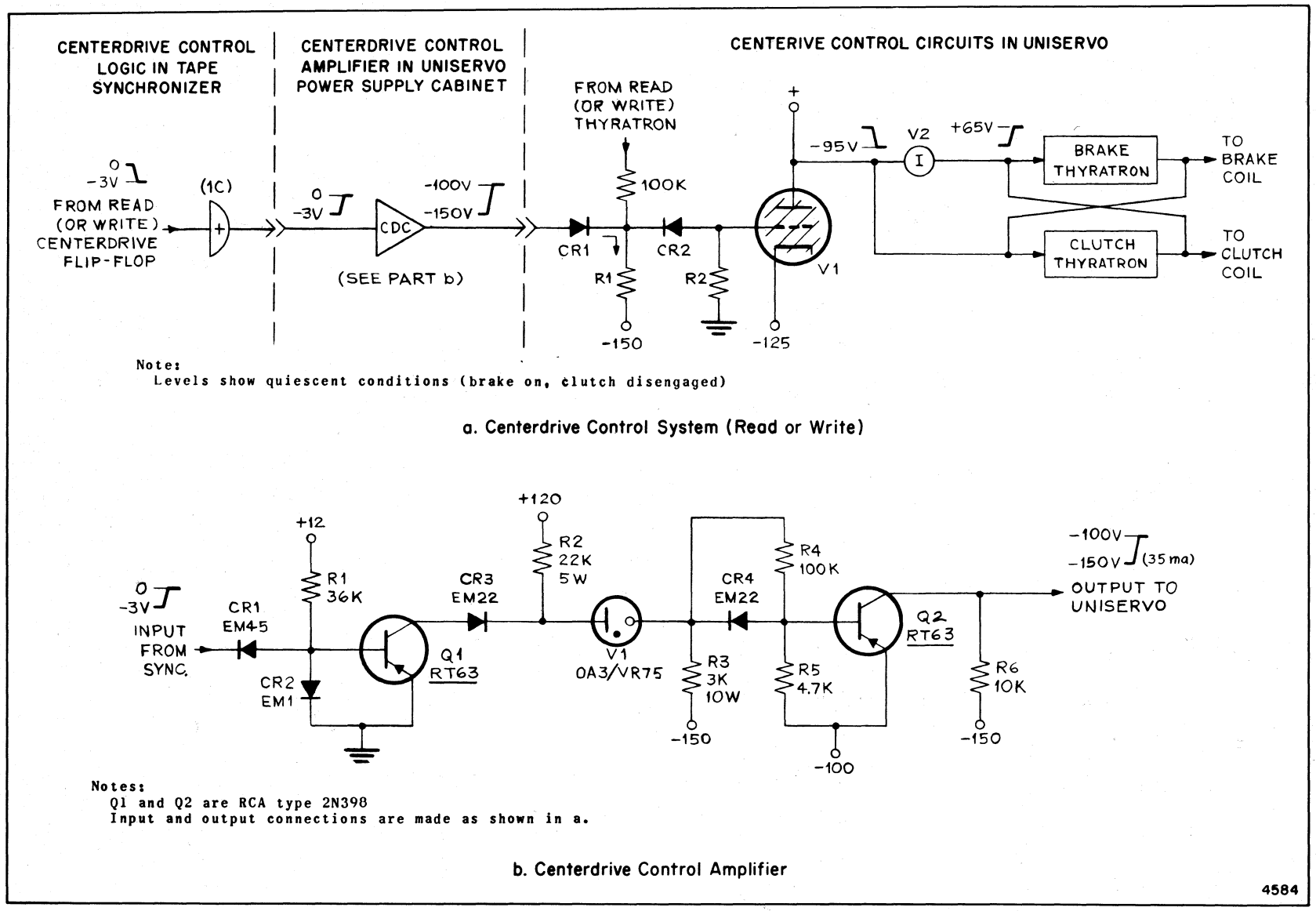


Figure 1-40. Centerdrive-Control Circuit

control logic circuitry to input terminals 1 and 2 of the eight tape read amplifiers. For coupling between the metal-plastic switch cable and terminal P of the amplifiers, a resistive-type network is used because sufficient current can be supplied through the closed switch to drive all the gain-control transistors (Q10 in figure 1-38) in the group of eight amplifiers.

As mentioned under heading 1-50, the purpose of the gain network is to convert from the standard 3-v level to a voltage level that swings positive as well as negative with respect to ground. The circuits at inputs A and B are similar and use conventional constant-current (PNP) coupling networks. The circuit parameters are chosen so that, with the input level at -3 v, the voltage at the base of Q1 (or Q2) will be about -1.2 v. Consequently the transistor will conduct (base-to-emitter voltage $\approx$ 0.2 v), and the output level at the emitter will be about -1 v. If the input signal changes to the level of ground potential, Q1 (or Q2) will be cut off, and the output signal will rise toward the emitter return potential of +28 v. The series-connected diodes across the output, however, clamp the output signal to +1 v. (The drop across the type-XR25 diode is about 0.3 v, while that across the type-EM43 diode is about 0.7 v.)

The third circuit at C produces the $\pm$1-v output level, depending upon the position of the manually operated metal-plastic selector switch on the Uniservo. For metal tape operations the switch is open and the input at C is floating (figure 1-36b). A current of about 8 ma then will flow out to the P terminals of the eight tape read amplifiers (collective load resistance is one eighth of 1000 ohms, which is 125 ohms) from the +12-v supply and R11 to cut off transistor Q10 (figure 1-38) in each amplifier. Diode CR6 clamps the output level at +1 v. The switch on the Uniservo is closed for plastic-tape operations so that the input level at C will be set to -3 v, as clamped by diode CR5. The voltage divider consisting of R9 and R11 then will divide the current so that the output level will drop to about -1 v. The negative level will allow Q10 in each of the eight amplifiers to conduct in order to provide the correct gain setting for plastic-tape operations.

1-52. CENTERDRIVE-CONTROL CIRCUIT

The function of the centerdrive-control system (figure 1-40a) is to control the movement of tape in the Uniservo in accordance with signals that originate in the tape read-write synchronizer. The centerdrive consists of a motor coupled to a capstan by an electromagnetic clutch-brake device; the clutch-brake device is operated by a pair of thyratron output tubes. The output from one thyratron energizes the clutch coil to engage the clutch and rotate the capstan; the output from the other thyratron energizes the brake coil to stop the capstan. The clutch and brake thyratrons are cross-coupled to provide feedback loops and thereby insure that only one tube will conduct at a time. The states of the thyratrons are controlled directly by signals from the centerdrive control logic in the synchronizer. The diagram of the system shown in figure 1-40a is simplified. (Actually there are two centerdrive control circuits in the synchronizer logic: one for read and one for write operations. However, the two circuits are identical in operation.)

The centerdrive-control and thyratron circuits are normally in the state that energizes the brake. This quiescent condition is illustrated by the levels shown in figure 1-40a. The read (or write) centerdrive-control signal from a flip-flop circuit in the logic circuitry is off in order to provide a low signal (-3 v) to the output circuit (1C) of the synchronizer. The inverted output from the 1C circuit then is fed to the special centerdrive-control amplifier unit (CDC) in the Uniservo power-supply cabinet. This unit, explained in detail under heading 1-54, is a transistor amplifier which is designed to amplify the 3-v level from the synchronizer to the high d-c voltages needed to drive the vacuum-tube control circuits in the Uniservo. As indicated in figure 1-40a, the output from the CDC unit swings from -150 to -100 v and is fed to the clutch and brake thyratrons through a diode switch and tube-driver network.

With the output from the CDC circuit at -100 v, diode CR1 will conduct in the forward direction through R1. Diode CR2 will also conduct from its ground return path through R2 so that the grid of tube V1 will be positive (-100 v) with respect to its cathode (-125 v). The plate voltage of the conducting V1 will drop to about -95 v and cause the clutch thyratron to be extinguished. At the same time tube V2 will invert the signal from V1 to fire the brake thyratron. These actions send a current through the brake coil to stop the tape motion or keep it stopped.

If a read (or write) centerdrive-control signal is generated in the synchronizer (high output to 1C circuit), conditions in the system will be reversed from those described in the preceding paragraph. In this case the output level from the CDC amplifier will be at -150 v to cut off CR1 and V1. The clutch thyratron will conduct to start or keep the capstan in motion.

Coaxial cable is used to connect the CDC unit to the output from the synchronizer module in the processor, as well as to the centerdrive circuits in the Uniservo.* The remainder of this section deals with the CDC amplifier shown on the tape-synchronizer logic drawings and mounted separately in the Uniservo power-supply cabinet.

The complete schematic of the centerdrive-control amplifier is given in figure 1-40b. The input stage Q1 is normally held nonconducting by the +12-v potential supplied through R1 to the base. The nonconducting state will prevail when the input-driving signal from the synchronizer is high (ground potential) or when it is disconnected from the CDC input. The disconnection is necessary because, when Q1 is off, the output stage Q2 is conducting to provide the correct level of voltage (-100 v) for operating the brake. Since the CDC input can be connected to one of several different 1C-driving stages through a plugboard, Q1 must remain in the nonconducting state if the input should be disconnected. The condition of keeping Q1 off imposes the constraint that all turn-on current for Q1 must be supplied through the 750-ohm dummy load resistor (R4) returned to -3 v in the 1C driving stage (figure 1-1). Under these conditions the most efficient coupling method to the base of Q1 is provided by a constant-voltage source such as that supplied by the series-connected diode CR1. This diode (type EM45) has an average voltage drop of about 0.6 v which is more than enough to insure that Q1 will be biased in the reverse direction when the input from the 1C circuit reaches its least positive value of -0.3 v. The clamp diode CR2 is needed to protect the base of Q1 from excessive reverse bias when the input is disconnected.

* Refer to Uniservo II manual, as corrected December 1958, heading 4-44 (U-1630.2).

The coupling circuit between Q1 and Q2 (figure 1-40b) uses a resistive step-up network in series with the voltage-regulator tube V1. The use of the VR tube (type 0A3/VR75) insures the delivery of sufficient current to the base of Q2 for efficient operation with the available supply voltages. Q2 will conduct without the VR tube in the circuit if its emitter return voltage is reduced, but its doing so would result in a higher collector-to-emitter voltage at the output. Resistor R2 is chosen to provide for a minimum current through V1 at all times and thereby improve the stability of operation. Diode CR3, in series with the collector of Q1, enables the anode of V1 to be returned to a positive potential so that the tube will fire when power is first applied.

With Q1 off, the second stage will conduct so that the output will rise toward the -100-v level of the emitter supply. The output stage is capable of driving a minimum load resistance of about 1500 ohms, a condition which occurs in the case of a fully expanded system of ten Uniservos connected to a single CDC amplifier. Under some conditions, such as that produced by a general-clear instruction, the output stage may be required to hold up the entire load for a short period. Thus transistor Q2 is normally operated in a heavily saturated condition and is capable of supplying an output current of about 35 ma.

Although the operating speed is very low, the dummy load resistor R6 has been added across the collector of Q2 to aid in discharging the capacitance of the coaxial cable which connects the CDC output to the Uniservo inputs.

1-53. TAPE-SELECTOR CHECKER

The type-SC tape-selector checker is a special gating circuit that detects the presence of two or more Uniservo-select signals at the same time. The circuit is designed to operate in conjunction with a full complement of Uniservos connected to the tape read-write synchronizer. Consequently 11 inputs are provided on the card which correspond to the maximum of ten Uniservo-select lines and one dummy-select line. Each of the 11 lines is driven from a type-VT tube driver to provide a large signal input (voltage swing: -12 v to about +38 v). The output from the circuit supplies a standard -3-v level at 0.55 ma to drive a single 1E circuit. The checker is packaged as card type NS and contains two full checking circuits (22 inputs) per card. The schematic is given in figure 1-41.

Logically the circuit will provide a low output (-3 v) if only one or no input-select line is active—that is, the output current will be 0 if not more than one input is at +12 v. However, if two or more input lines are positive, the circuit will function to produce a high output (+0.2 v) at 0.55 ma. By detection of the absence of a high output when a Uniservo-select line is energized, and by subsequent detection of the presence of a high output when the dummy-select line is also energized, it is possible to make sure that one and only one Uniservo is selected.

If all the input signals are at the -38-v level in operation, the gating diodes (CR1 ... CR11) will be biased in the reverse direction and the output level will be clamped to -3.3 v by the current flow from the -3-v supply through CR12 to the -48-v supply. If the level on one input line rises to +12 v, the diode associated with the input line will conduct

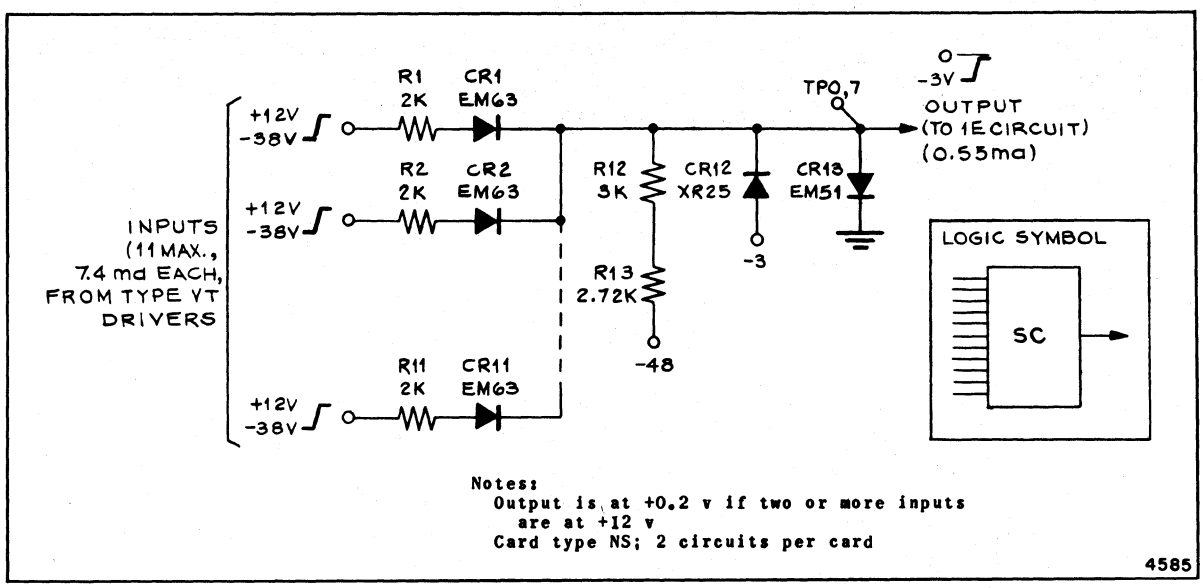


Figure 1-41. Tape-Selector Checker Circuit

in the forward direction from the 2-kilohm series resistor through resistors R12 and R13 to -48 v. The voltage division here is such that 15 v will be dropped across the 2-kilohm resistor so that the output level will remain at approximately -3 v. (The resistance ratio is 1:4, and 60 v/4 = 15 v.) If two or more input diodes conduct, the resistance ratio in the voltage-divider network will decrease proportionately so that the voltage drop across the input circuit will always be less than 10 v (voltage drop for two inputs: 9 v). Consequently the output will rise to about the level of ground potential, as clamped by diode CR13.

1-54. TYPE-CNC AND -CNE COUPLING CIRCUITS

The type-CNC and -CNE circuits are used to couple high-potential signals from the Uniservos into the logic circuitry of the tape synchronizer. The CNC circuit is connected to a type-1C gate inverter; the CNE circuit is connected only to a 1E circuit. Except for these output load requirements the CNC and CNE are the same. The circuit for each and the respective logic symbols are given in figure 1-42.

The output signal from a Uniservo is connected through coaxial cable to the input of the coupling network, where it is applied across the voltage divider consisting of resistances R1 and R2. The lower end of R2 is returned to a source of positive or negative potential which depends on the circuit application. The values of R1 and R2 will also vary with the particular circuit application, depending primarily upon the input-signal level and output-drive requirement. CR1 and CR2 are clamping diodes which restrict the output-voltage swing to about 3 v. In operation the voltage drop across the type-EM45 silicon diode (CR2) is about 0.7 v while the drop across the type-XR25 diode is about 0.3 v. The output-voltage swing then will range from about +0.7 v to -3.3 v, thereby enabling the circuit to reject small-amplitude noise signals.

The CNC and CNE circuits are supplied as card types NC and NE, respectively, and each card contains ten coupling circuits. The specific applications of all these circuits (including voltage levels and resistance values) in the tape synchronizer are illustrated in figure 1-43.

The first three circuits (write forward, read backward, and read forward) are CNC types in which the outputs to the 1C circuits are normally low because of conduction from -3 v through R2 to -11 v. If the read or write relay contacts are closed in conjunction with the centerdrive relay, a positive level of about +14 v will appear at the input to the CNC voltage divider to give a high output of +0.7 v. The next five circuits are interlock test circuits in which type-CNE coupling units are used and which function in the same manner as the CNC circuits. The isolation tube diodes prevent interaction among signals from different Uniservos.

The read and write photocell signals are connected from the output stage of the photocell amplifier and appropriate relay contacts in the Uniservo to CNC circuits in the synchronizer. The second half of the 6SN7 tube is normally in the conducting state, and the constant voltage level at its plate will be about +80 v. The output from the CNC circuit will then be -3.3 v, as described two paragraphs back. If a bad spot is detected, the 6SN7 will be cut off abruptly; its plate voltage will rise to +120 v. This positive pulse has a duration of about 1.2 ms and will be coupled through the 0.01-μf capacitor to cause a high output from the CNC circuit.

The last two circuits (write test and write-clutch test) operate in a similar manner to produce outputs from the CNE circuits that are normally high; that is, the write and clutch thyratrons are extinguished (anode voltages: +230 and +600 v) so that the isolation diodes are cut off. If the thyratrons are fired, the cathodes of the isolation diodes will be negative and the output levels from the CNE circuits will drop to -3.3 v.

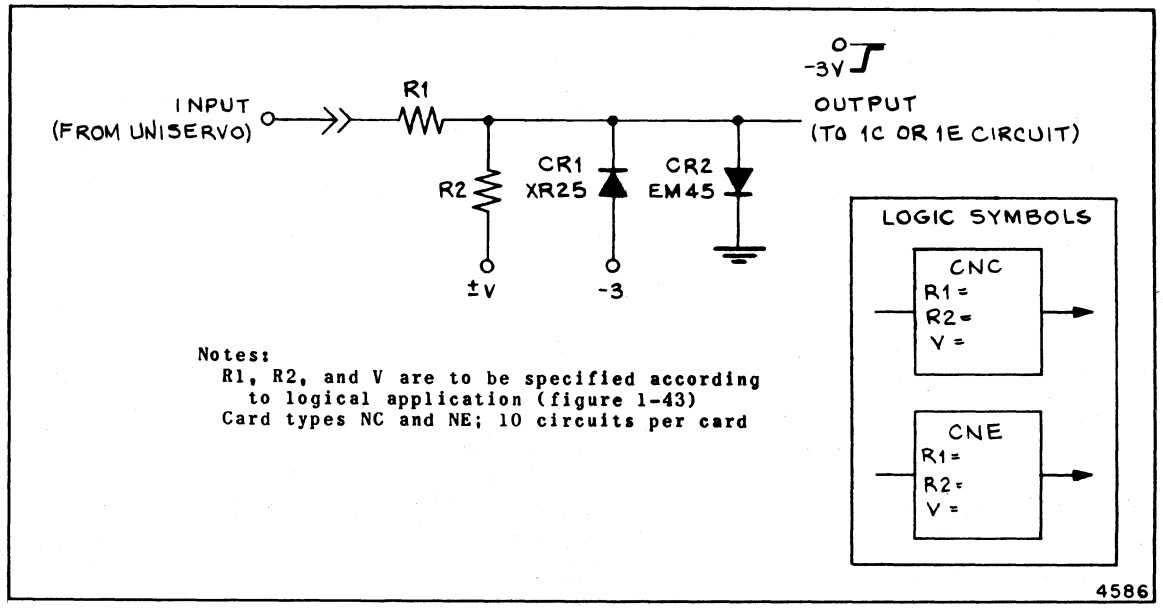


Figure 1-42. Type-CNC and -CNE Coupling Circuits

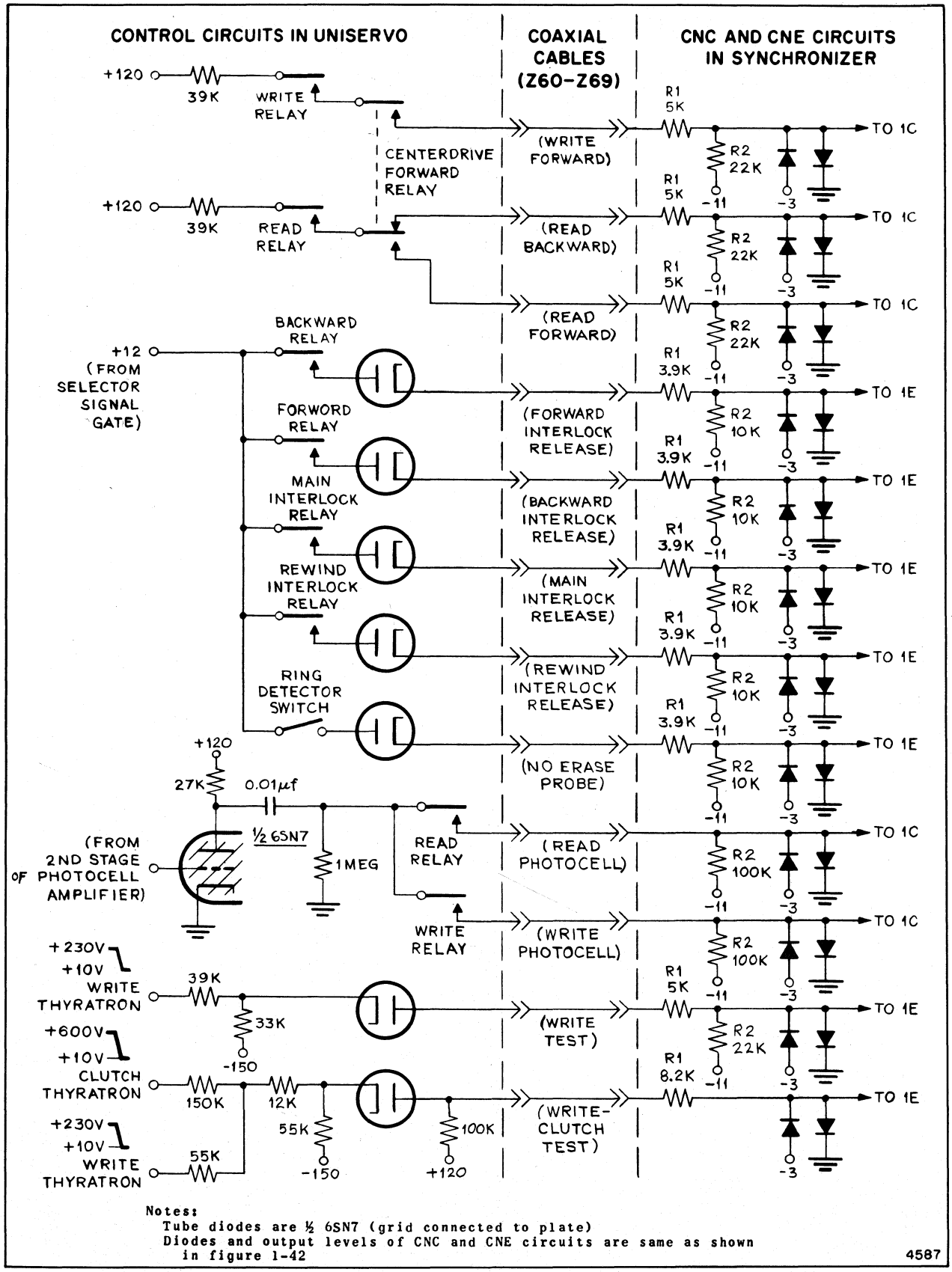


Figure 1-43. Uniservo Coupling Networks

1-55. PRINTER-SYNCHRONIZER CIRCUITS

A few special circuit types have been developed for use in the line-printer synchronizer. There are three output driver types (PC1, PC2, and PC3) used exclusively to supply the correct levels of drive for operating the magnetic-core-storage matrix in the printer. These driver circuits are designed to produce sufficient current for setting and sampling selected cores in the matrix and, as such, are referred to as write-in drivers (PC1), read-out drivers (PC3), and select drivers (PC2). A detailed description of each of the driver packages is given under headings 1-57 and 1-58. However, a brief description of the over-all printer core-storage system is presented first so that the application of these special driver circuits in the printer synchronizer will be clear. Also covered under headings 1-59 and 1-60 are the code drum amplifier, which is the same as the type-TR tape read amplifier, and the circuit applications of the types-CNC and -CNE coupling networks. As mentioned under headings 1-33 and 1-47, the type-VT tube driver is also used in the printer-synchronizer circuitry as an output driver.

1-56. PRINTER CORE-STORAGE SYSTEM: GENERAL DESCRIPTION

Output information to be printed is compared in the synchronizer for identity with signals fed back from the code drum in the printer which represent sequential character positions around the circumference of the print wheels. When identities occur, print-select signals are generated and stored in the synchronizer and are fed back to the printer in groups of five to control eventually the movement of the printing mechanism. As shown in figure 1-44a, the printer contains a magnetic-core matrix arranged in a 5 x 13 array. Up to five cores, depending on the polarity of the five signals derived from the type-PC1 write-in drivers, may be set (written in) at one time.

The output from each PC1 driver is connected in parallel to a column of 13 cores, but only one core in the column is capable of being set during the 12-μs pulse time allowed for write-in. This condition is effected by applying a coincident 12-μs select signal from the type-PC2 select driver associated with the currently selected row of five cores; the 13 PC2 drivers are excited sequentially by signals derived from a 13 counter in the synchronizer. The excitations for the five PC1 drivers and the single PC2 driver are synchronized by the logic circuitry in the synchronizer so that the setting of cores will take place in groups of five. Thus the minimum output current required from each PC1 unit is that needed to switch one core (20 ma), plus the current for a total of 13 resistors in parallel (14.3 ma) (R4 in figure 1-44b). Required from a PC2 unit is the current drawn by a common load-return circuit for all five cores in a row (189 ma maximum).

The read-out process is carried out in essentially the same manner, as far as switching the cores is concerned. In this case seven higher-power type-PC3 drivers are used to supply a 20-μs read-out signal to each of the 65 cores in the matrix; six of the PC3 units drive ten cores in parallel, and the seventh drives the remaining five. Except for the larger current requirements (246 ma), the PC3 drivers are the same as the PC1 units. Therefore the select signals from the PC2 drivers must also be applied

simultaneously to effect a read-out from the cores. As indicated in figure 1-44a, the signals from the PC2 units are applied for the full 20-μs sampling time, and all 13 rows are selected in parallel.

The output line from each of the 65 cores is connected to the control grids of a pair of thyratron-gate tubes so that those cores which have been set will alert the appropriate actuator-control circuits. In operation one of the polarities of magnetization of the cores is identified with a 1 and the other with 0. To determine which magnetization is present, the read-out (sampling) pulse from the PC3 driver is applied to a winding in the direction to restore the core to the 0 state. If the 0 polarization is present (core not originally set by PC1 signals), only a very small flux change occurs along the hysteresis loop of the core. Thus only a very small voltage appears at the output winding. However, if the polarization corresponding to a 1 is present (core set by 12-μs pulse from PC1 unit), the read-out pulse changes the flux density by twice its saturation value, and this large flux change produces a large voltage in the output winding.

The core-storage circuit for one unit is illustrated in figure 1-44b. To set the core, the write-in line from the PC1 unit supplies a positive-going pulse of 15-v amplitude while the select line from the PC2 driver supplies a coincident negative-going pulse. Both pulses are 12 μs in duration and, with the indicated polarities, diode CR4 will conduct in the forward direction. Thus the current from the PC1 unit will flow up through one half of the primary winding of the core unit and out through R3 to -29 v. The direction of this current sets the core to the 1 state. Notice that the presence of the select pulse enables this current to flow by cutting off diodes CR3 and CR5 and causing the top of R3 to be at about +1 v. In the absence of a write-in pulse CR4 will be cut off and no current will flow through the core winding. To insure that the voltage at the top of R3 is always more positive than +15.5 v in the absence of a select signal, diodes CR3 and CR5 are returned to a clamping level of +15.5 v.

The read-out process functions in exactly the same manner as write-in except that the current from the PC3 driver flows through the upper half of the core primary winding and has a duration of 20 μs. If the core is in the 1 state, a large flux change will take place and a voltage will be induced in the secondary winding of the core. The positive voltage at the top of the output winding then will be coupled through diode CR5 to overcome the bias on the control grids of the thyratron-actuator drivers. Coincident signals from other circuits (odd-even row circuits) in the synchronizer on the shield grids of the thyratrons will complete the print operation.

1-57. TYPE-PC1 AND -PC3 PRINTER CORE DRIVERS

The type-PC1 and -PC3 circuits are very similar and provide the printer core write-in and read-out signals, respectively. The circuit configuration shown in figure 1-45 is the same for type-PC1 and -PC3 core drivers and is capable of amplifying 3-v input signals from the synchronizer logic circuits to 15-v output signals for driving the magnetic cores in the printer storage matrix.

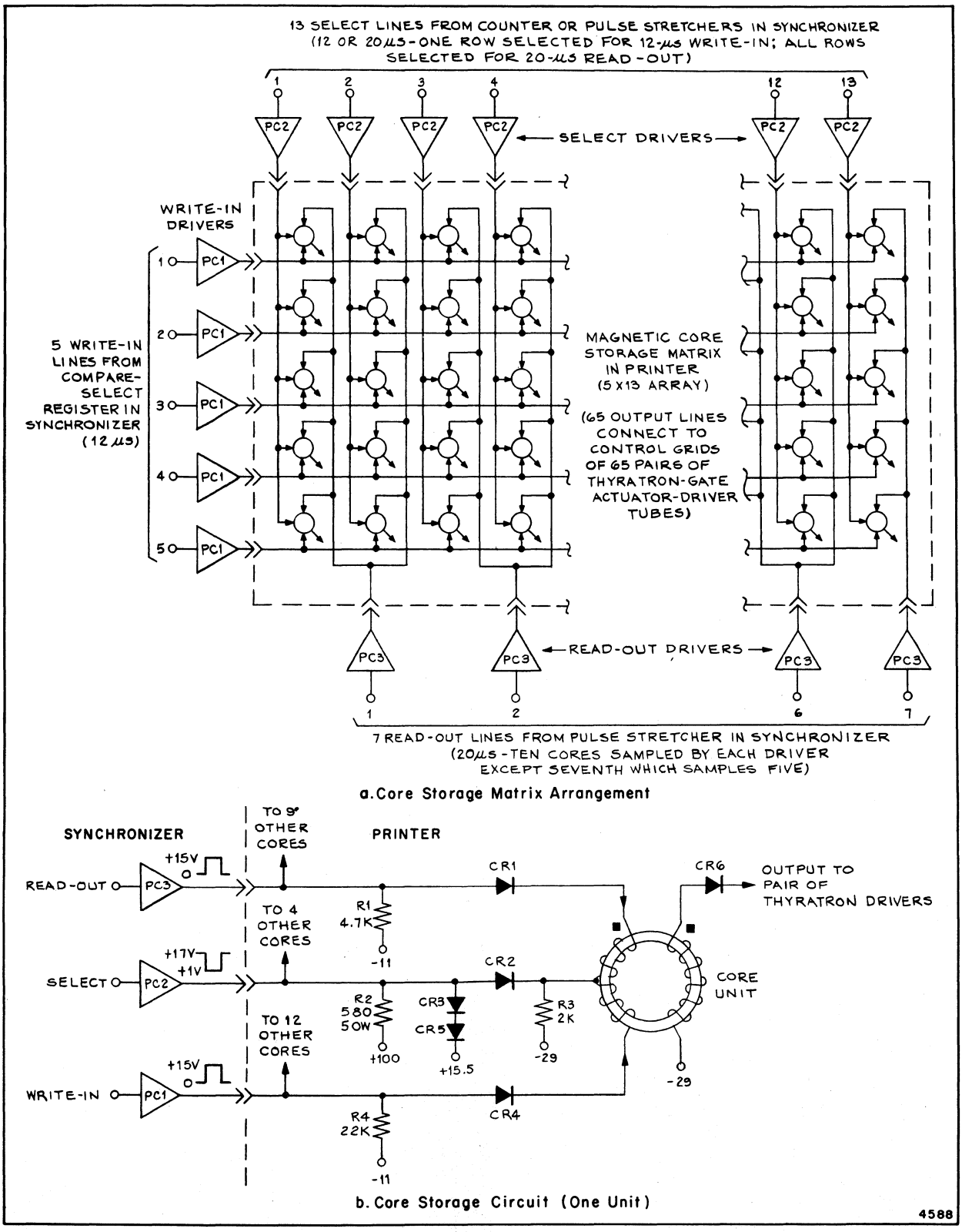
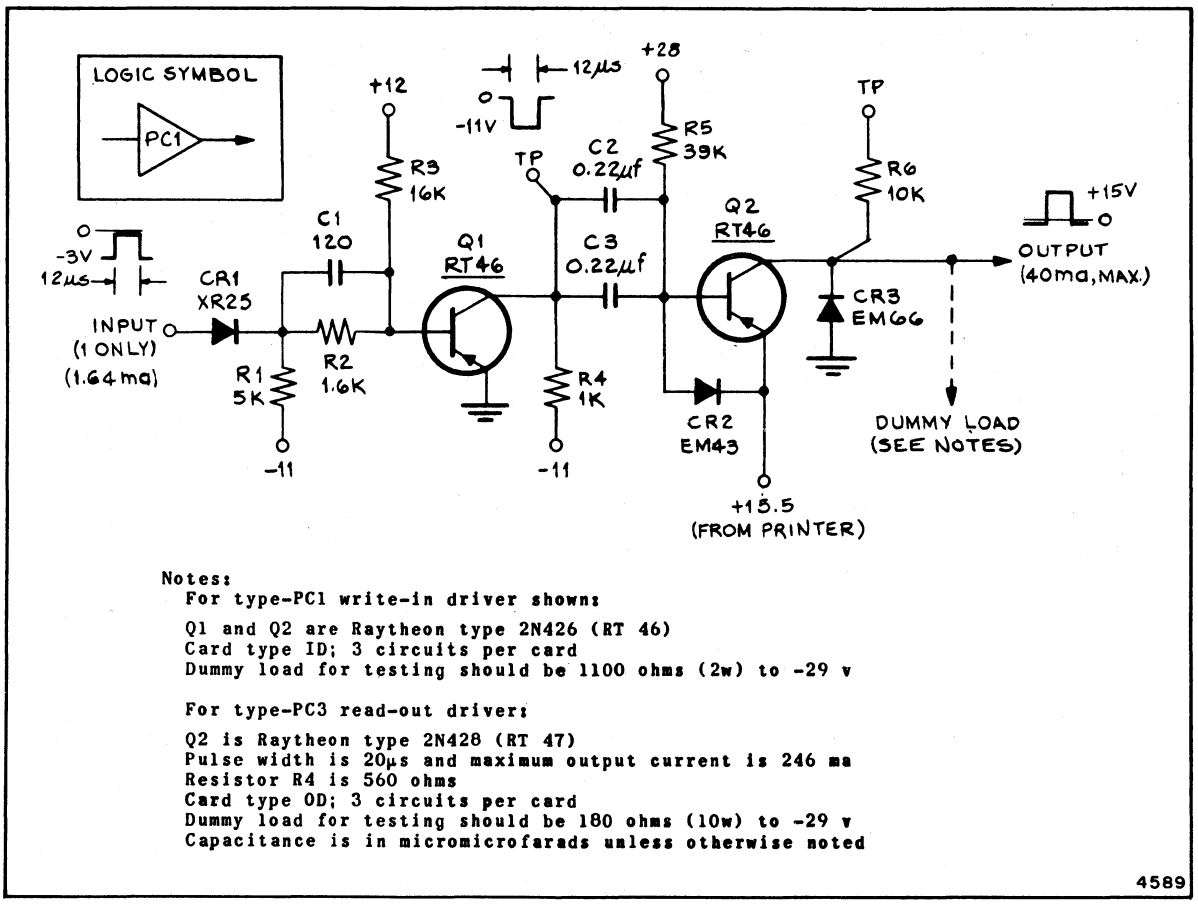


Figure 1-44. Line-Printer Core-Storage System



Notes:
For type-PC1 write-in driver shown:

Q1 and Q2 are Raytheon type 2N426 (RT 46)
Card type ID; 3 circuits per card
Dummy load for testing should be 1100 ohms (2w) to -29 v

For type-PC3 read-out driver:

Q2 is Raytheon type 2N428 (RT 47)
Pulse width is 20μs and maximum output current is 246 ma
Resistor R4 is 560 ohms
Card type OD; 3 circuits per card
Dummy load for testing should be 180 ohms (10w) to -29 v
Capacitance is in micromicrofarads unless otherwise noted

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Figure 1-45. Type-PC1 and -PC3 Printer Core Drivers

The differences between the PC1 circuit shown in the schematic and the PC3 circuit are outlined in the notes accompanying the figure. The following description pertains to the PC1 circuit and the modifications for the PC3 driver are explained afterward.

The operation of the circuit is similar to previously described inverter circuits; in fact, the input stage Q1 is practically the same as a type-1C circuit with one input diode. Thus Q1 is normally conducting (input level: -3 v; base-to-emitter voltage: -0.25 v) and the collector output will be near the level of ground potential. The coupling circuit between Q1 and the output stage Q2 uses the parallel-connected capacitors C2 and C3 to eliminate bias difficulties, since a relatively high voltage is required at the emitter of Q2. Consequently, Q2 is held in the off state by means of the current from the +28-v supply, through R5 and the clamp diode CR2 to +15.5 v, which makes the base about 0.6 v more positive than the emitter. As shown in figure 1-44b, the 22-kilohm load resistor (R4) in the printer is returned to -11 v but the output at the collector of Q2 (figure 1-45) is clamped near to ground by diode CR3 (maximum drop: 0.7 v).

A positive-going signal of 1 drive unit (1.64 ma) at input diode CR1 (figure 1-45) will cause Q1 to cut off. The negative-going pulse at the collector will be coupled through C2-C3 to enable Q2 to conduct so that the

output will rise toward the emitter return potential of +15.5 v. (Saturation voltage of Q2 is about 0.4 v.) The 15-v level was chosen because of the limiting factor of the breakdown-voltage rating of the type-RT46 transistor. However, this transistor (Raytheon type 2N426) provides for a maximum output current of 40 ma, which is adequate for carrying the load of 13 core circuits (17 ma), and also provides switching current for one core (20 ma).

The major differences between the PC1 write-in driver and the type-PC3 read-out driver is in the output load requirements. The PC3 circuit is required to supply switching current for 20 μs to as many as ten cores at a time. Thus the collector current from Q2 can be a maximum of about 246 ma. For this reason the output stage of the PC3 circuit uses a type-RT47 higher-current-gain and faster-switching transistor (Raytheon type 2N428) which has an end-of-life base-current amplification factor of at least 20.* The larger output-current requirements also necessitate an increase in the end-of-life current gain of the first stage (RT46) from 17 to 30, with a corresponding reduction in the value of the collector load resistor R4 from 1000 to 560 ohms.

As indicated in figure 1-45, the type-PC1 circuit is supplied as card type ID; the PC3 circuit is supplied as card type OD. Each of the two card types contains three driver circuits.

1-58. TYPE-PC2 PRINTER CORE DRIVER

The circuit for the type-PC2 printer core driver is shown in figure 1-46. Except for signal polarities the function of this circuit is essentially the same as that described under heading 1-57. In order to produce a negative-going output pulse of the required amplitude and power level, an emitter-follower output stage Q3, which uses a type-RT47 transistor, has been added to the basic driver circuit. The input stage Q1 is identical to the one used in the PC1 and PC3 circuits. The second stage, however, is biased to the conducting state by returning the base-load resistor to a source which is negative (+15.5 v) with respect to the emitter (+20 v). Q3 will be held to the cut-off state in the absence of an input signal. Thus the quiescent conditions for the select driver are these:

(1) A high (ground) steady-state input will hold Q1 off.

(2) Q2 is biased on so that its collector voltage will be high (+20 v) to hold Q3 off.

(3) The output level then will be fixed at about +17 v by means of the clamp diodes (CR3 and CR5 in figure 1-44b) in the printer load circuit.

(4) With the +17-v level present at the centertap of the core primary winding, diodes CR4 in the write-in circuit and CR1 in the read-out circuit will be biased in the reverse direction, and core switching is prevented.

* Of the seven required read-out units, each of six units drives ten cores in parallel and the seventh drives five cores in parallel in the core-storage circuitry. Therefore a maximum output current of only 246/2 ma = 123 ma is required of the seventh unit. Though not necessary, the gain (beta) of the output transistor of this unit need only be half of the other six. However, all transistors are usually selected to be identical so that the cards are interchangeable.

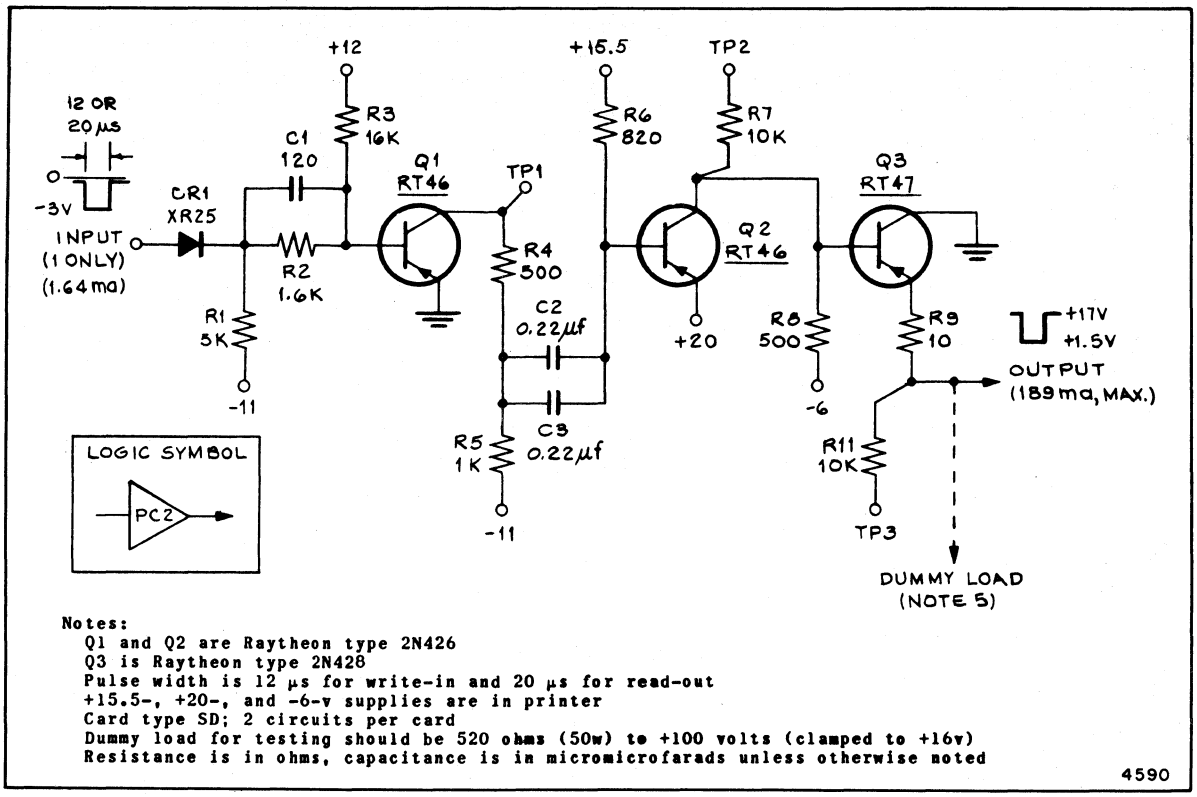

Figure 1-46. Type-PC2 Printer Core (Select) Driver

A negative-going select pulse at the input of the PC2 circuit will cause diode CR1 to cut off and Q1 to turn on. The rise in collector voltage of Q1 toward ground level will be coupled through capacitors C2-C3 to cause Q2 to be cut off for 12 or 20 μs corresponding to the duration of the input pulse. With Q2 off, the emitter-base circuit of Q3 will be biased in the forward direction, and an output current will flow from the +100-v supply in the printer through dropping resistor R9 and the emitter-collector circuit of Q3. Consequently the output level will drop to near ground potential, and diodes CR3 and CR5 (figure 1-44b) will be cut off. With a low level established at the centertap of the core winding, the magnetic flux of the core can be switched by a positive-going pulse from either the PC1 or PC3 circuit.

Resistor R9 in the emitter circuit of Q3 (figure 1-46) is used to insure that the output level from the PC2 circuit is always slightly more positive (+1.5 v) than the output level from the PC1 or PC3 driver in the absence of a write-in or read-out pulse. This will insure that diodes CR1 and CR4 (figure 1-44b) will be cut off at the correct times. The circuit conditions are such that the common load resistor for all five cores connected to each PC2 circuit (R2 in figure 1-44b) has a value of only 580 ohms. The RT47 output transistor Q3 (figure 1-46) then will carry a maximum collector current of about 190 ma. Because of a dissipation of about 12 watts, R2 consists of four 120-ohm 10-watt wire-wound resistors and one 100-ohm one in series.

The coupling circuit between Q1 and Q2 in the PC2 circuit includes the voltage-divider network consisting of R4 and R5 in order to reduce the most

positive bias voltage present at the base of Q2 during the period in which this stage is cut off. The circuit parameters are chosen so that the initial base-to-emitter voltage of Q2 of about 2.6 v gradually drops to 1.5 v, as determined by the RC time constant of the coupling circuit. The values of the components in the circuit (R4, R5, R6, C2, and C3) are such that the time constant of 535 μs is short enough to allow the coupling capacitor to charge up again to its initial value in the time between select pulses.

The PC2 driver is supplied as card type SD, which contains two complete circuits per card. The power supplies for +15.5, +20, and -6 v are physically located in the line-printer equipment, and the three potentials are carried to the printer synchronizer module of the processor card library by power cables (figure 1-46).

1-59. CODE-DRUM AMPLIFIER

The code drum in the printer, which is attached and keyed to the same shaft as the revolving print wheels, consists of a magnetically coated cylinder on which are recorded ten channels of coded information. This information consists of nine-bit code and sprocket signals which are continually read by a magnetic head assembly and transferred by RG22/U cables to the synchronizer input circuitry. The code-drum amplifiers amplify the low-level output from the read head in the printer to a level sufficient to energize Schmitt trigger circuits; the Schmitt trigger circuits, in turn, drive standard asynchronous logic circuits in the synchronizer. Thus the code-drum read system is very similar to the tape read system used in the tape-synchronizer circuits (figure 1-36b) and the code-drum amplifier is the same as the type-TR tape read amplifier. A logic type diagram of the code-drum amplifier is given in figure 1-47.

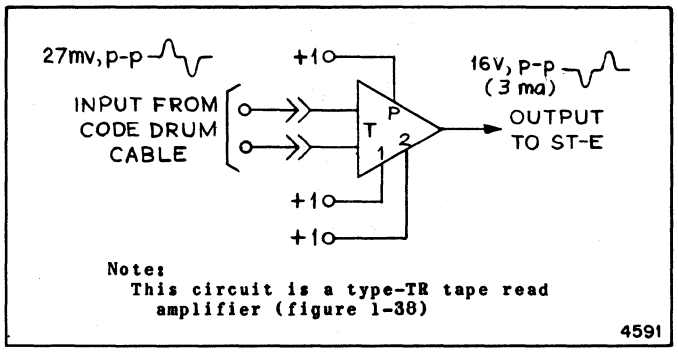

Figure 1-47. Code Drum Amplifier

The average peak-to-peak input from the code-drum cable is 27 mv. The nominal zero-to-peak output from the code-drum amplifier needed to set the following type-ST-E Schmitt trigger circuit is 8 v. Therefore the over-all closed-loop gain of the code-drum amplifier should be about 593.* It is evident that this amount of gain is very close to that obtained from the tape read amplifier when it is set to its minimum gain setting (table 1-9)

* The input signals from the code drum can vary between 15 mv and 40 mv to produce corresponding zero-to-peak outputs from the amplifier of 4.5 v to about 12 v. However, these levels are within the clipping range of the TR circuit.

—that is, at a gain of 600, which is the low gain setting for metal tape. As described under heading 1-50, minimum amplifier gain is achieved when the a-c feedback loop provides for maximum feedback current. Maximum feedback current occurs when all three gain-control transistors (Q8, Q9, and Q10 in figure 1-38) are cut off and the shunt resistance in the ladder network is effectively out of the circuit. Thus the amplification for the printer signals is obtained as shown in figure 1-47. The three gain-control transistors are cut off to give a fixed closed-loop gain of about 600. This is brought about by simply applying +1 v from a fixed d-c source to the three gain-control input terminals (1, 2, and P) of the amplifier.

1-60. COUPLING CIRCUITS

The coupling networks consist of five type-CNC circuits and one type-CNE circuit that are used to couple high-potential signals from the line printer into the logic circuitry of the printer synchronizer. The operation of these circuits is exactly the same as that described for the tape-synchronizer coupling circuits under heading 1-54 (figure 1-42). The specific application of the six coupling networks (including voltage levels and resistance values) in the printer synchronizer are illustrated in figure 1-48.

The first four circuits (no paper, no ribbon, paper-feed error, and carriage out) are CNC types in which the outputs to the 1C circuits are normally low because of conduction from -3 v through R2 to -11 v. If any one of the four relay-switch contacts is closed, a positive level of about +15 v will appear at the input to the CNC voltage divider. This will cause a high signal of about +0.7 v to be generated at the output of the circuit, and thereby indicate the appropriate malfunction.

The charge test circuit drives a 1E inverter to produce an output that is high during the time that the actuator capacitors across the printer-thyratron-driver circuits are in the process of being charged—that is, during the 10-ms interval required to charge the capacitors up to +750 v. At all other times the charge test signal will be low to indicate that a steady-state condition exists across the capacitor circuit. The action is implemented as follows. The output emitter-follower transistor (Q1) in the printer is an NPN type; when the +750-v supply is on, the transistor will conduct in the forward direction from base to emitter and provide a high positive potential at the input to the CNE circuit. This result will produce the usual high input signal (+0.7 v) to the 1E circuit. When the charging voltage is removed, a negative bias is applied across the base-emitter circuit of Q1 and the transistor is cut off. The output from the CNE circuit will drop to the clamping level at -3 v.

The bias check circuit is an OR gate arrangement which indicates the absence of one or both of two critical bias voltages in the printer. If both the -50 and -30-v bias voltages are present, the voltage division across the resistive network is such as to keep the anodes of the isolation diodes more negative (-9 v) than the cathodes, and the output from the CNC circuit will be at -3 v (figure 1-48). However, if either or both of the bias voltages are removed, one or both of the diodes will conduct and cause a positive output from the CNC circuit.

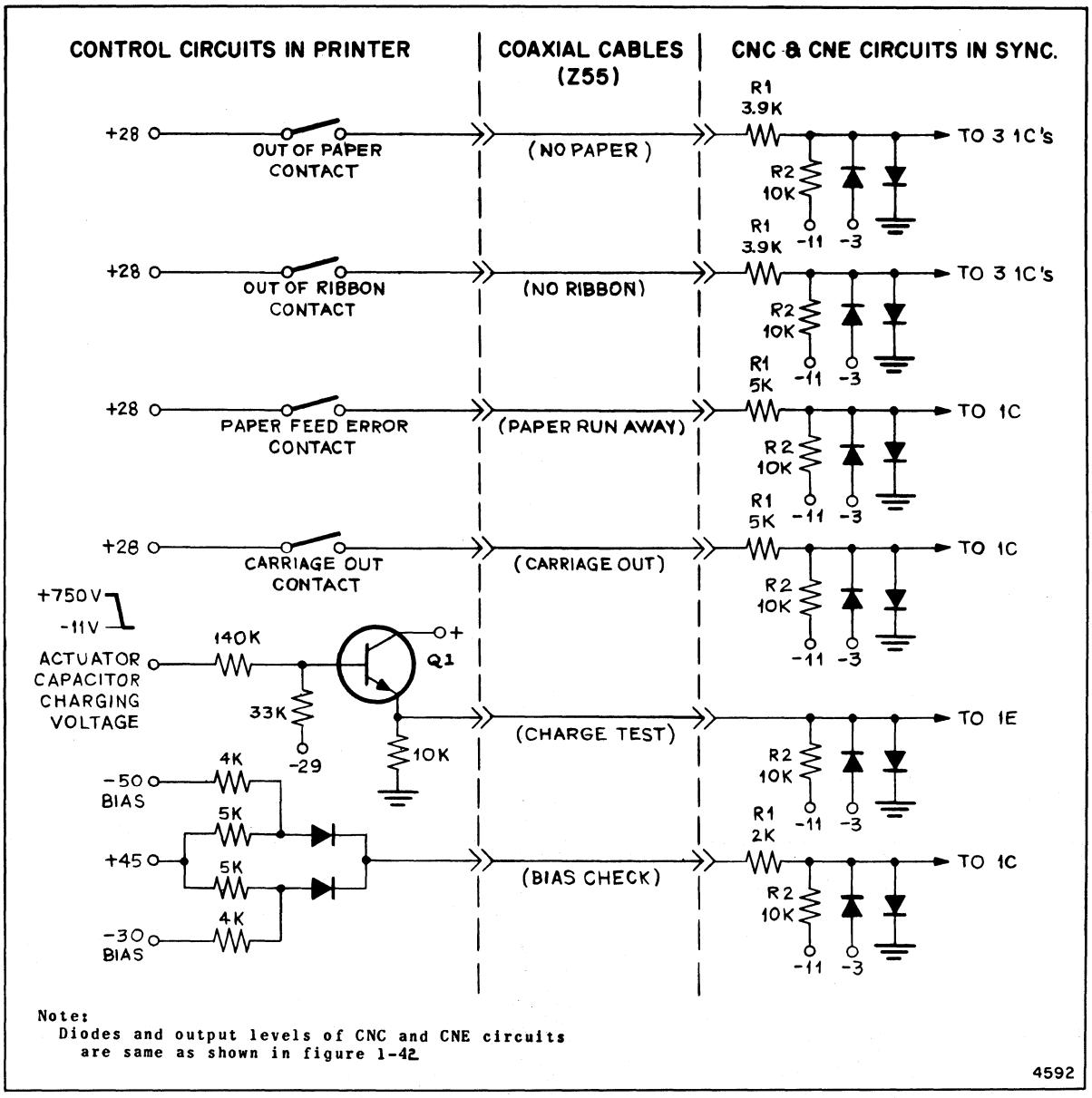

Figure 1-48. Line-Printer Coupling Networks

1-61. FAST-REGISTER CIRCUITS

The computing unit and processor each contain several fast-operating storage registers composed of magnetic-core matrices. The matrices use type-1011 tape-wound Ferractor® cores that have a switching time of only 1 microsecond for a complete read-write cycle. The fast registers in the computing unit are the 26 one-word A-B registers operated completely in parallel. The A-B registers consist of two core matrices in which each is arranged in a 26 x 30 array. Consequently, to transfer a word to or from one of these registers, there must be a switching of corresponding rows of 30 cores in each of the two matrices.

In the processor there are several fast registers located in the synchronizer-dispatcher. The synchronizer address register is similar to the

A-B registers except that the cores are arranged in a single 7 x 25 array. The smaller size is used because only the five-digit memory address is stored for each of the seven input-output synchronizers included in the basic system. The other fast registers are the input and output buffer registers associated with each of the synchronizers. The buffer registers are similar to the other types in that they use the same circuit components throughout. However, these registers do not operate completely in parallel because their function is to provide temporary storage for data being transferred between the input-output equipment and the main storage. Thus the configuration of the buffer register is such as to provide for serial-to-parallel data conversion if the buffer register is an input buffer, or parallel-to-serial if it is being used as an output device. Serial data transfer here means parallel-digit or five bits at a time. ('Parallel' refers to a complete 60-bit word transfer at one time.)

Both the input- and output-buffer registers consist of eight one-word storage registers constructed in the form of two 8 by 30 matrices. The total of eight registers is for the basic system; the size of any of the fast-register matrices for any expanded system must be increased proportionately. The interconnections between the cores are arranged to provide the appropriate read-out and write-in switching configurations. The logical significance of the interconnections among the buffer registers, as well as other relevant connection data on these and the address and A-B registers, will be found in descriptions of Larc logic. Headings 1-62 through 1-68 present a general description of the over-all fast-register operation and detailed descriptions of each of the standard circuit types.

1-62. FAST-REGISTER OPERATION: GENERAL DESCRIPTION

Figure 1-49 is a simplified diagram of a fast-register system. The connections shown in this illustration are for parallel operation of the matrix as used in the A-B registers of the computer and the address register in the synchronizer-dispatcher. Each of the magnetic cores in the matrix stores one bit of information. In operation one of the polarities of magnetization of the cores represents a 1 information bit and the other a 0. For determining which state of magnetization is present a read-out pulse is applied to a winding on the core in the direction to restore the core to the 0 state. If the 0 polarization is present, only a very small flux change occurs along the hysteresis loop of the core, and very little voltage change appears at the output winding. However, if the polarization corresponding to a 1 is present, the read-out pulse changes the flux density by almost twice its saturation value, and this large flux change produces a large voltage in the output winding.

As shown in the Ferractor insert in figure 1-49, each core has three windings: a read winding, a write winding, and an output winding. The read windings in a row of cores are all connected in series (up to a maximum of 30 cores: $n \leq 30$) and are driven by a single read driver circuit. The read driver consists of an input transistor stage (gate inverter) and a series-pulse magnetic amplifier which uses a type-1003 Ferractor core element. Reading or clearing a row of cores requires a 1-μs negative-going pulse at the input to the read driver from an address information line. The negative-going signal causes the input transistor to conduct; the conduction of the transistor in turn sets the magnetic

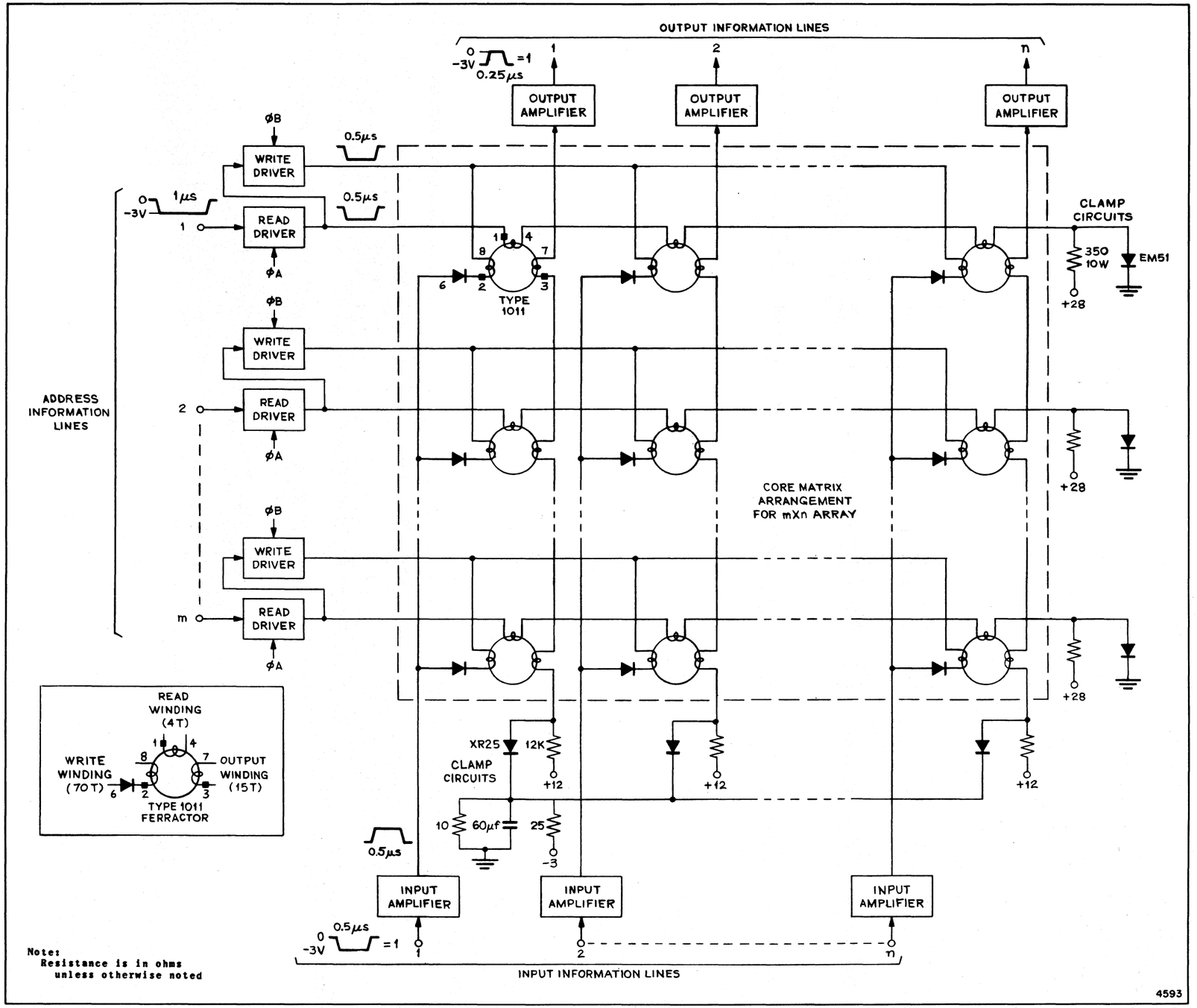

Figure 1-49. Fast-Register System for Parallel Operation

amplifier so that, when the series-fed power pulse is applied, the cores will be switched to (or left in) the 0 state. As shown in the illustration, the read-out pulse is a negative-going pulse of 0.5-μs duration and is generated by the A-phase clock pulse (φA), which is applied in series with the output winding of the read magnetic amplifier (heading 1-64). A-phase designates that the negative halves of the 0.5-μs squarewave clock pulses coincide with the odd time slots of the logic timing intervals (T1, T3, T5, T7). B-phase clock pulses are negative during the even time-slot periods (T0, T2, T4, T6).

The magnitude and significance of the voltage appearing on the output windings as a result of the read-out pulse depend on the previous state of the core. The result of the storage of a 1 by any core will be the generation of a positive-going output pulse in the output winding. This pulse is fed to a corresponding output amplifier in the matrix. The characteristics of the output amplifier are such that up to 13 core output windings may be connected in series to a single amplifier input. In the case of the A-B registers an additional input diode circuit to the amplifier (figure 1-52) is provided for the remaining 13 core output windings in the 26 x 30 array ($m \leq 26$).

The output amplifier consists of a two-stage transistor amplifier and delay circuit which produces a 3-v output information signal (positive-going for 1's) at 1 drive unit (1.64 ma). The amplifier delay characteristics are needed to provide synchronization with the next pulseformer clock period of the logic circuitry. The rules for establishing the delay period are covered under heading 1-67 and in the timing chart of figure 1-53, which shows relative signal polarities and specific timing information on the operation of A-B registers.

The write-in operation of the cores is implemented by the application of opposite-polarity signals to the write windings connected in parallel. The write-driver circuit supplies a 0.5-μs negative-going pulse to one end of the write winding while a coincident 0.5-μs pulse is supplied to the other end from an input amplifier. The latter pulse is an information pulse which is positive for 1's. Thus the isolating diodes connected to the selected windings will conduct in the forward direction and switch the cores from the 0 to the 1 state. If the input amplifier signal is negative, no current will flow through the write winding and the core will remain in the cleared or 0 state.

The write-driver circuit varies according to the fast-register application. For parallel operation (figure 1-49) it is driven directly by the read driver output and consists only of a type-1012 magnetic-amplifier core circuit operating during the B-phase of the clock periods. With this arrangement a read-out operation is always followed by a write-in operation 0.5 μs later. Depending on the logic control signals, either the same information is regenerated or new information is stored in the register. In the input and output buffer registers, however, the write-driver circuit is identical to the read-driver unit and contains a cascaded transistor amplifier and type-1003 magnetic amplifier. This arrangement allows the write circuits to be addressed independently of the read-driver circuits and thereby enables the serial-to-parallel (or parallel-to-serial) conversion properties of the buffer registers to be used.

An input amplifier is connected in parallel to each of the cores in a column and consists of a single-stage transistor inverting amplifier. The circuit is designed so that 1 drive unit of input power holds the stage in the nonconducting state. A negative-going 0.5-μs input pulse will allow the positive output signal to be generated to drive the lower end of the selected write winding.

The clamp circuits connected to the ends of the series of read and output windings are included in figure 1-49 to show the termination networks for all the windings in the core matrix. The operation of these clamps, as well as of the voltage divider in the circuit of the output windings, is covered under headings 1-63 through 1-67.

1-63. TAPE-WOUND CORES

The magnetic cores used in all of the fast-register storage matrices are fast-switching alloy units of tape-wound construction. (These cores are further identified as type-1011 memory Ferractor cores.) The core consists of four wraps of type-4-79 molybdenum-permalloy tape, 1/32-inch wide, 1/8-mil thick, wound on a 50-mil (inside diameter) stainless-steel bobbin. The molybdenum-permalloy core material has a rectangular hysteresis-loop characteristic that requires a relatively low magnetizing force to switch the core at the 0.5 μs switching speeds of the fast registers. Therefore it requires minimum energy from the read and write drivers—a fact which is the principal criterion of design in building the core matrix.

The number of wraps of tape used to make the core is a compromise value for producing a high-squareness ratio in the core hysteresis-loop characteristic, which increases with an increase in the number of wraps, and a fast switching time, which decreases with more wraps. With four wraps of tape of the dimensions given in the preceding paragraph, and on the assumption of a saturation flux density of about 7500 gauss for the core material, the total flux change which occurs when the core is switched is about 1.5 maxwells.

The read, write, and output windings on the core are made with No. 43 high-frequency wire and are wound to provide the relative polarities shown in the insert in figure 1-49. The number of turns in the output winding is based on the total flux change of 1.5 maxwells. On the assumption that the minimum required output pulse is 0.5 v and the switching time is 0.5 μs, the minimum number of turns is about 16:

$$N = \frac{V\Delta t}{\Delta\phi} \times 10^8$$

$$= \frac{(0.5)\ (0.5 \times 10^{-6}) \times 10^8}{1.5}$$

$$= 16 \text{ (turns)}$$

The number of turns on the output winding must be kept to the minimum value for several reasons:

(1) The air inductance of the winding increases as the square of the number of turns. Since up to 13 output windings can be connected in series, the inductance must be kept to a low value.

(2) When a register is selected for read-out, those cores which store a 0 will exhibit some flux change as the core is driven from remanence to saturation because of the lack of squareness of the hysteresis loop. This flux change will cause a small output sneak voltage to be induced in the output winding. So that the amplitude of this voltage remains at a minimum, the number of turns in the output winding should be no greater than necessary.

(3) The current required by the output amplifier must flow through all the output windings in series. To keep any of the unselected cores from switching, the magnetizing force established by the output current through the output windings of the unselected cores must be less than the coercive force. Therefore the number of turns in the output winding must be limited. In addition, the capacitive loading on the write driver is a function of the number of cores in a register and the capacitance between the write and output windings of the core. One way to minimize this capacitance is to minimize the number of turns in the output winding.

The number of turns used in the read and write windings is based on the amount of magnetizing current needed to switch the core in the allotted time. This magnetizing current is supplied by the A-phase or B-phase clock power through the output windings of the read or write magnetic-amplifier drivers. Although the pulse width of the clock is 0.5 μs, an allowance of 0.125 μs is made for clock rise and fall time, a delay due to the lack of squareness of the hysteresis loop of the driver core, and rise time due to the inductance of the output winding of the driver core. Thus an average pulse width of 0.375 μs is available to switch the core in the storage matrix. With an experimentally derived curve of switching time as a function of magnetizing force, 1.15 oersted of magnetizing force (H) is required to switch the core in 0.375 μs. Based on this value of H, the ampere-turn product (NI) for the read and write windings is 0.425.

For the read-out process, the amount of current delivered to the series-connected read windings from the read driver is about 107 ma. Therefore the minimum number of turns on the read winding is this:

$$\frac{0.425\ NI}{0.107\ I} = 4 \text{ turns}$$

The number of turns is kept at 4 in order to minimize clock voltage requirements. If more turns were used in the read winding, a correspondingly higher clock voltage would be needed; this in turn would require either more turns on the output winding of the read driver or more wraps of tape on the read driver core. In either case optimum design parameters would be affected.

The number of turns in the write winding is based on the capacity of the write driver to deliver approximately 110 ma to the parallel-connected write windings. The maximum number of write windings that can be connected to a single write driver is 30 (heading 1-62). In consideration of the fact that the memory code is such that only three out of five cores will be switched (written in) at any one time, the current available for each write winding is 110/18 = 6.1 ma. Therefore the minimum number of turns in the write winding is this:

$$\frac{0.425 \quad NI}{0.006 \quad I} = 70 \text{ (turns)}$$

1-64. READ DRIVER

Figure 1-50a shows the schematic diagram of the complete read driver circuit. This circuit is used in all the fast registers to produce the read-out or clear pulse for the storage cores. The driver consists of an input inverting-amplifier stage and a magnetic amplifier which uses a tape-wound core similar in construction to that described under heading 1-63. The magnetic amplifier is powered by series-fed A-phase clock pulses so that an output will be produced during time T1, T3, T5, or T7. This timing is determined by the main-storage timing requirements and is used in the A-B, address, and input-buffer registers. Read drivers that operate during the A phase of the clock are designated type RA. (See logic symbol.) However, the read drivers in the output-buffer registers, which operate during the B phase and produce outputs during time T0, T2, T4, or T6, are designated RB.

In the absence of an input address signal the input stage Q1 is held in the nonconducting state by means of a high (ground) signal at diode CR1. In this situation CR1 conducts through R1 to produce a d-c voltage at the junction of R1 and R2 of about -0.6 v. The drop across the forward-biased CR2 causes the base voltage to be at ground potential so that the transistor is cut off. With Q1 off, the output voltage will be set at about -7 v, as established by the constant-current clamp circuit at the other end of the input winding of the magnetic amplifier. All the read driver circuits in the fast registers are driven by single IC stages; since each of the registers is divided into two equal sections, there is an average of 1-1/2 drive units (2.46 ma) available for holding each input stage off.

A 1-μs input signal at -3 v will cause CR1 to cut off and Q1 to conduct. The reverse bias on CR1 is about 0.1 v. The use of the step-up diode (CR2) allows the base current to complete its transition from minimum to maximum values over a smaller input-voltage swing. The amount of current delivered by the type-XT76 transistor (Philco type 2N501: micro-alloy diffused transistor) when it is fully conducting is close to 50 ma. This current switches the state of the core in the read magnetic amplifier and is described in the following paragraphs.

The tape-wound core used as the read magnetic amplifier is designated type 1003 and contains three windings: input, output, and bias. The core material is the same as the type-1011 storage core under heading 1-63. The inside diameter of the bobbin is 100 mils instead of 50, and the number

of turns on the three windings and number of wraps of tape is changed because of the different functions performed by the core and its external circuits. In order to produce a high-saturation flux density of about 14,000 gauss, the total number of wraps of tape is 23. The number of turns required on the input winding is 46 and is based on a minimum input current of 33 ma and a magnetizing force of about 1.4 oersted. For the output winding the rate of change of voltage for switching the core depends on the magnitude and width of the clock pulse; the total flux change which occurs when the core is switched is about 7.5 maxwells. The number of turns on the output winding is 81, on the assumption that the maximum clock voltage will drive the core 95 percent of the way up the hysteresis loop. The 10-turn bias winding is used to inhibit the core from switching when an input pulse is absent.

The operation of the magnetic amplifier is based on the relative polarities of the windings, which are arranged so that a negative clock pulse will switch the core toward positive saturation. The amplitude of the clock pulse and the number of turns on the output winding are such that under worst tolerance conditions (maximum amplitude variation and minimum core coercivity) the core will barely switch from negative remanence to positive saturation in the clock-pulse half cycle. High-limit cores, low-limit power pulses, or combinations of the two result in the incomplete driving of the core toward saturation. In either instance the core is never driven to saturation; therefore the output winding remains at high impedance throughout the clock-pulse interval, and no change in output occurs. During the positive half cycle of the clock-pulse period the output is disconnected by diode CR7, while the current in the bias winding switches the core down its hysteresis curve from positive to negative saturation. Thus with each clock cycle the core is switched up and down along the entire hysteresis loop.

The magnetizing current flowing in the output winding is supplied by the constant-current clamp consisting of diodes CR5 and CR6 and resistor R5. The 1100-ohm resistor and the +28-v return voltage are chosen to guarantee a small surplus of current over the required magnetizing current so that CR6 will remain conducting and no signal will appear at the output. Diode CR6 must have a larger voltage drop (EM82: 1.3 v minimum) than the clamp diode connected to ground at the end of the series of read windings in the storage matrix (EM51 of figure 1-49: 0.5 v) in order to prevent any magnetizing current from flowing through the read windings. The sneak-suppressor action of the combination makes the output winding act like a true open circuit to the output load, since no current flows to the load during its high-impedance condition.

When the input stage Q1 (figure 1-50a) is cut off, a positive-going pulse is applied to the input winding at the end of the negative clock interval. This pulse causes a current to flow during the entire positive clock period in a direction to overcome the bias current and insure that the core is put into a state of positive saturation. Therefore a very low impedance is presented by the core during the following negative clock period, and full output current (107 ma) will be coupled through diode CR7 to the read windings of the core matrix.

A smaller number of turns are used on the input winding so that under worst tolerance conditions (minimum current from Q1 and maximum core coer-

civity) the amplifier will be driven completely to positive saturation by the end of the input period. Normally saturation will be reached before the end of the half cycle, a fact which causes the input to act as a short circuit to its driving source. Constant-current clamp CR4-R4, like that on the output, is designed to remain conducting for normal magnetizing currents but to limit the current when the normal value is exceeded. Shorting of the input, therefore, will only slightly affect the loading on the driving source, for the current through R4 increases only slightly when the signal voltage is added to the relatively high d-c voltage already across it.

The bias winding (figure 1-50a) is connected in series with the bias windings of other read drivers to a constant-current d-c source of +28 v. Potentiometer R7 adjusts the bias current to nominal value of 45 ma, which can be measured conveniently at jack J1.

1-65. WRITE DRIVER

There are two versions of the write driver used in the various fast registers; which of the two depends on the logical application of the matrix. One type is identical to the read driver circuit described under heading 1-64 and is used exclusively in the input and output buffer registers of the processor. In these applications the write driver is addressed independently of the read driver and is powered by B-phase clock pulses in the input buffer registers and by A-phase pulses in the output buffer. In the parallel-operated A-B and address registers, however, the write driver is always driven by the output from the read driver, and it requires a modified form of magnetic-amplifier circuit, which is illustrated in figure 1-50b.

The core element is of the same construction and size as the one in the read driver. The only difference is in the number of turns on the input and output windings and in the direction of polarization of the windings. The change in polarization is dictated by the fact that the driving signal from the read driver is negative-going. In addition, the write drivers used in the parallel mode of operation are always powered by the B phase of the clock pulses and produce an output pulse 0.5 μs after the read driver output, at time T0, T2, T4, or T6.

The tape-wound core is type 1012, with 21 turns on the input winding and 92 turns on the output (figure 1-50b). With 20 wraps of tape the total flux change which occurs when the core is switched is about 6.4 maxwells. The input signal must produce this flux change in 0.375 μs; to do so requires a magnetizing force of about 2.1 oersted and an input current of 75 ma. The number of turns required on the output winding to supply the necessary number of volt-seconds is 92, on the assumption that the maximum 0.5-μs clock voltage will drive the core 95 percent of the way down the hysteresis loop. The bias winding on the write driver has ten turns and is energized in the same way as in the read driver (figure 1-50a).

In operation the negative clock pulse switches the core from a state of positive remanence to one of negative saturation. During the switching period the core presents a high impedance and no output is produced. The positive half cycle of the clock pulse is blocked by diode CR3, but at this

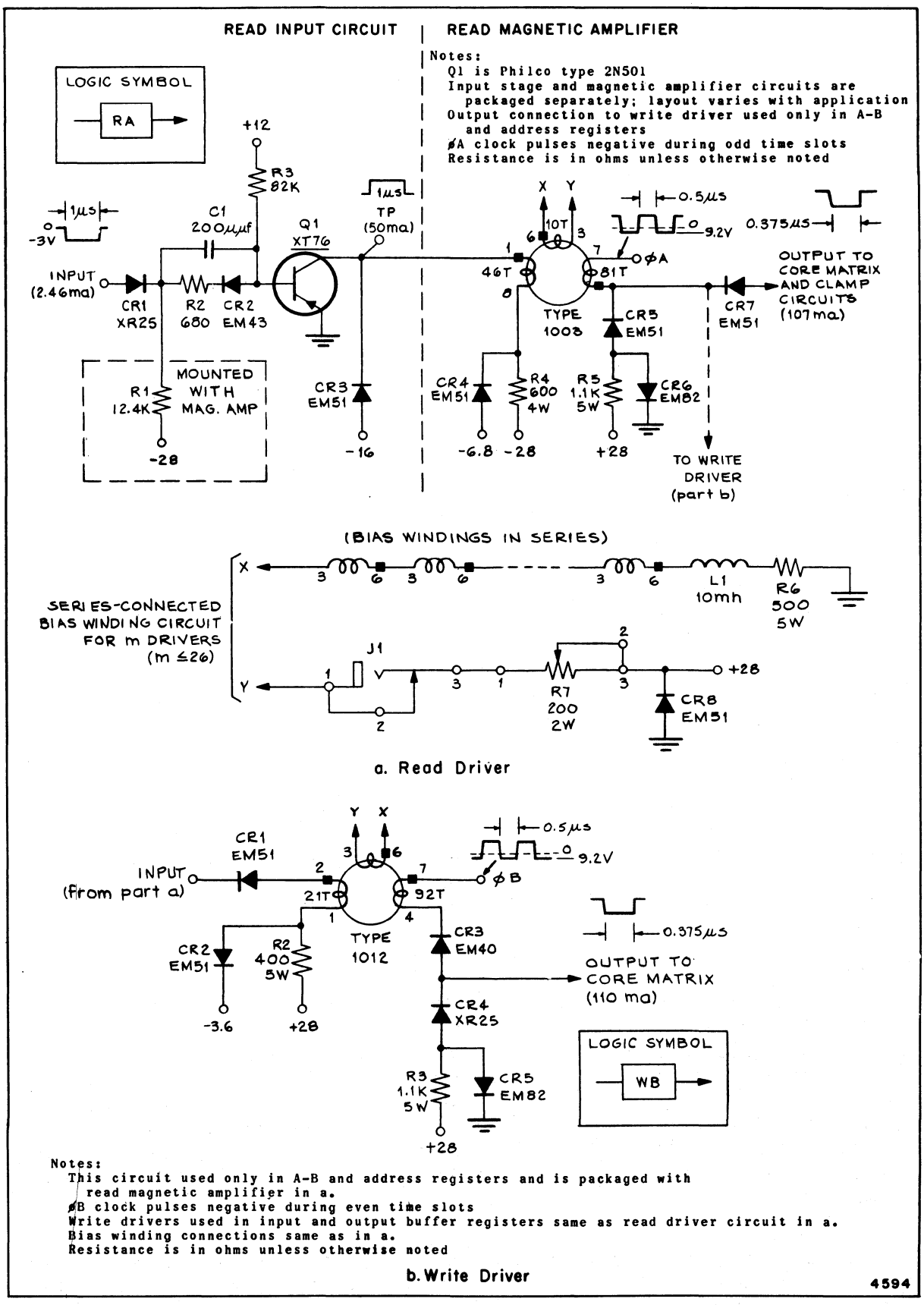

Figure 1-50. Read-Write Driver Circuits

time the bias current resets the core back to positive remanence. Now, with a negative signal from the read driver at the input winding, the bias current is overcome and the core is left in a state of negative remanence during the positive halves of the B-phase clock pulses (negative halves of the A-phase pulses). Consequently, with the arrival of the negative B-phase clock pulses the core will present a very low impedance, and an output current of about 110 ma will be coupled through CR3 to the load. The clamp components and other features of the circuit are similar to those described for the read driver under heading 1-64.

1-66. INPUT AMPLIFIER

The input amplifier operates in conjunction with the write driver to write information into the cores of the matrix. As described under heading 1-62, the coincidence of a negative-going pulse from the write driver and a positive-going pulse from the input amplifier at opposite ends of the write windings will cause the core to be switched from the 0 to 1 state. If no output pulse is received from the input amplifier at the time of the write driver pulse, the core will remain in the 0 state. Thus the input amplifier converts a negative-going 3-v information signal from the logic networks to a 0.5-μs positive-going output signal close to the level of ground potential, and thereby completes the current path through the write winding. The circuit schematic is given in figure 1-51.

The operation of the circuit is quite similar to the read input circuit described under heading 1-64 and also to other gate inverters. A high (ground) input will cause CR1 to conduct, Q1 will be cut off (base-to-emitter voltage: +0.3 v), and the output voltage will be low (-11 v). When the input swings negative (representing a 1 information pulse), CR1 cuts off and Q1 conducts (V_{be} = -0.25 v). The output current at the collector will cause the level of the output signal to rise toward ground. The clamp circuit in the emitter of Q1 is used to limit this current after the core in the matrix is completely switched.

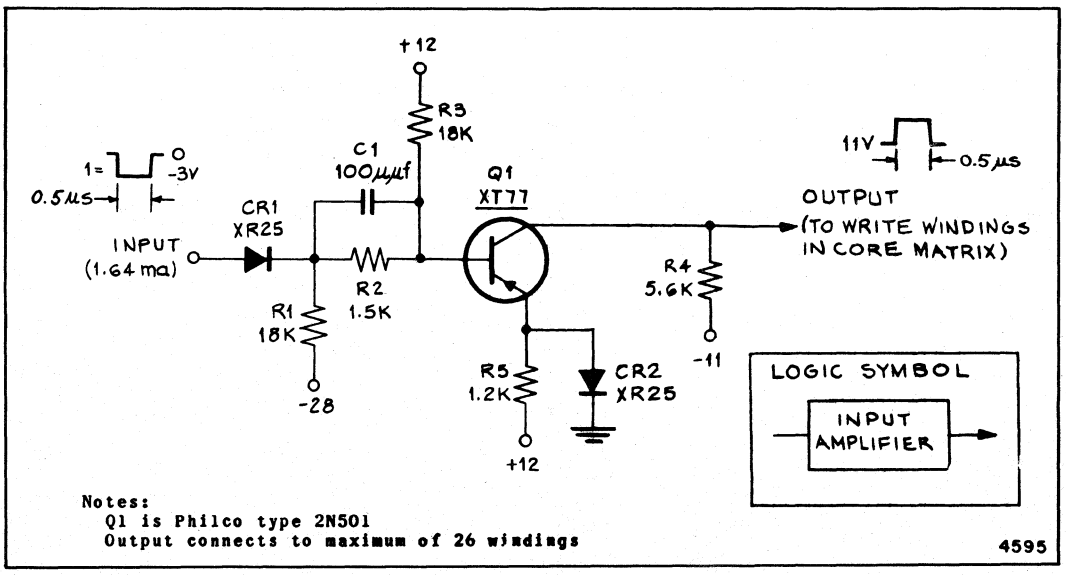

Figure 1-51. Input-Amplifier Circuit

1-67. OUTPUT AMPLIFIER

The output-amplifier circuit is shown in figure 1-52. Whenever a storage core is switched during the read-out process, a positive-going pulse of about 0.25-μs duration is induced in the output winding of the core. This pulse is amplified and delayed by the output amplifier so that it will enter the logic networks at the correct level and timing. The input stage Q1 is normally held in the conducting state by means of the base current furnished by the -11-v supply through R1. With Q1 on, the second stage Q2 will be cut off and cause a low output from the amplifier (-3 v).

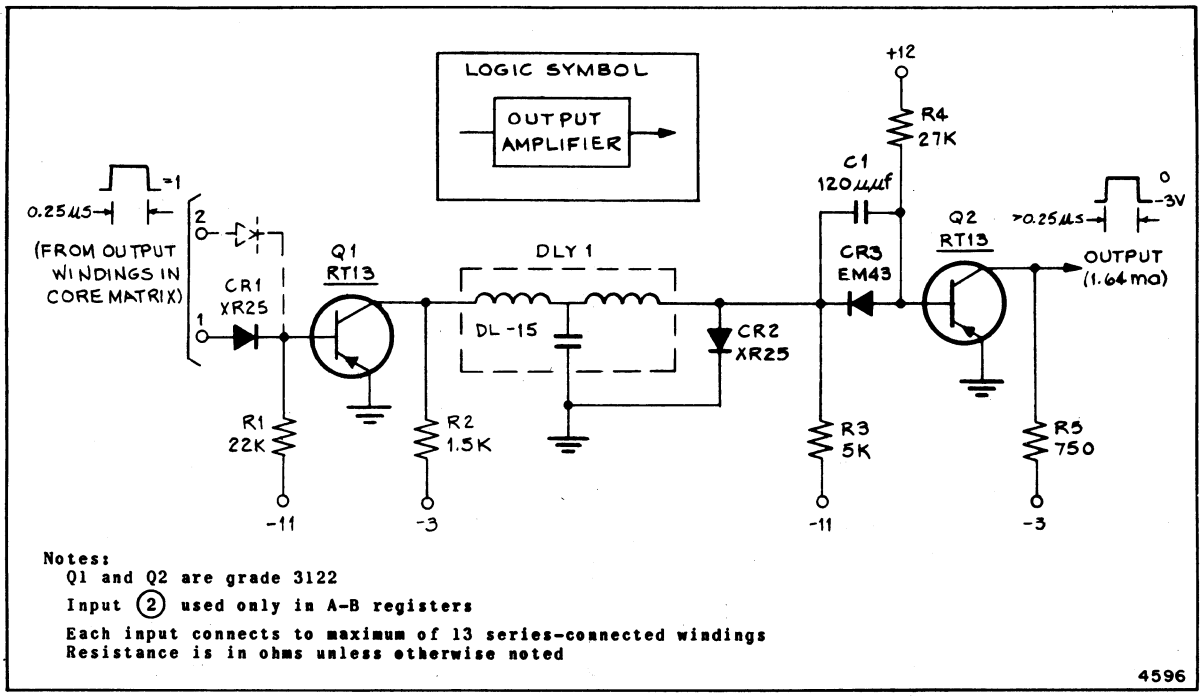

Figure 1-52. Output-Amplifier Circuit

The input to the amplifier (figure 1-49) is connected to a series of output core windings: up to 13 in series may be connected to each input diode of the amplifier. The lower end of the series of windings in the matrix is returned to a clamp and voltage-dividing network. The voltage divider (10- and 25-ohm resistors to -3 v)* causes to be present at the lower end of the windings a negative voltage which is more negative than the base-to-emitter drop (-0.5 v) of Q1 in the output amplifier. This action will insure that the isolating diode (CR1 in figure 1-52) is biased in the reverse direction during the time when the core is not switched. The clamp circuit (12,000-ohm resistor and the XR25 diode: figure 1-49) is needed to limit the current through the windings so that only half the coercive force is applied to the cores. This will help to insure that the cores are not switched by the output current.

A positive signal appearing at any one of the series-connected output windings will cause CR1 to conduct in the forward direction (figure 1-52). The current flowing from the clamp circuit will replace the base current

* The resistances in the clamp circuit (given as 25 ohms and 12 kilohms) are varied according to the matrix application.

from the transistor, and Q1 will cut off. The negative-going output from the collector will allow Q2 to conduct so that the output signal will rise toward the level of ground potential. The second stage uses practically the same components as the type-1C gate inverter. The only difference is that the transfer element here is a type-EM43 diode instead of the usual coupling resistor. The diode reduces the required input-voltage swing and effectively widens the output pulse. Thus a positive-going output signal representing a 1 will be generated at the collector of Q2 at 1 unit of drive (1.64 ma) for application to the logic circuitry.

The transistors used in the output amplifier are of type RT13 with a grade rating of 3122. The delay line DLY 1 used between stages is designated as type DL-15. It is a passive, lumped-constant line similar to that described under heading 1-19 and produces a delay of about 70 mμs. The minimum allowed delay from the collector of Q1 to the input of the next pulseformer driver stage in the logic networks is 170 mμs. (See the timing chart, figure 1-53. This timing chart is specific for the A-B registers only and is based on the fact that there are two levels of logic between the output of the output amplifier, which is the collector of Q2, and the input of the pulseformer buffer.) This minimum value insures that the narrowest 1 information pulse will reach the pulseformer in time to be transmitted even in the case of the worst pulseformer clock tolerance. The maximum allowed delay of 235 mμs functions in the opposite direction to insure that 0 information from the output amplifier does not reach the pulseformers at the time of the next clock pulse.

1-68. PACKAGING

The fast registers are packaged entirely separate from the other logic-circuit types. Each of the groups of registers is mounted in a self-contained framework assembly positioned vertically in a large area of the computer and processor card libraries. The complete complement of 26 A-B registers is packaged on two frames, of which each contains two 13 x 30 core-matrix assemblies mounted back to back, with their associated read and write drivers, input and output amplifiers, and clamp circuits. Similarly, the input and output buffer registers in the processor are each packaged on two frame assemblies; the address register, because of its smaller matrix, is completely within one two-sided frame.

A fast-register frame assembly consists of 32 printed-circuit cards, of which 16 are mounted on each side of the frame. The cards are stacked vertically in two rows of eight cards each, on both sides. They are consecutively numbered from top to bottom, as one faces the card library:

Cards	Side
1, ... 8*	Right rear
9, ... 16	Right front
17, ... 24*	Left rear
25, ... 32	Left front

* Plug-in cards

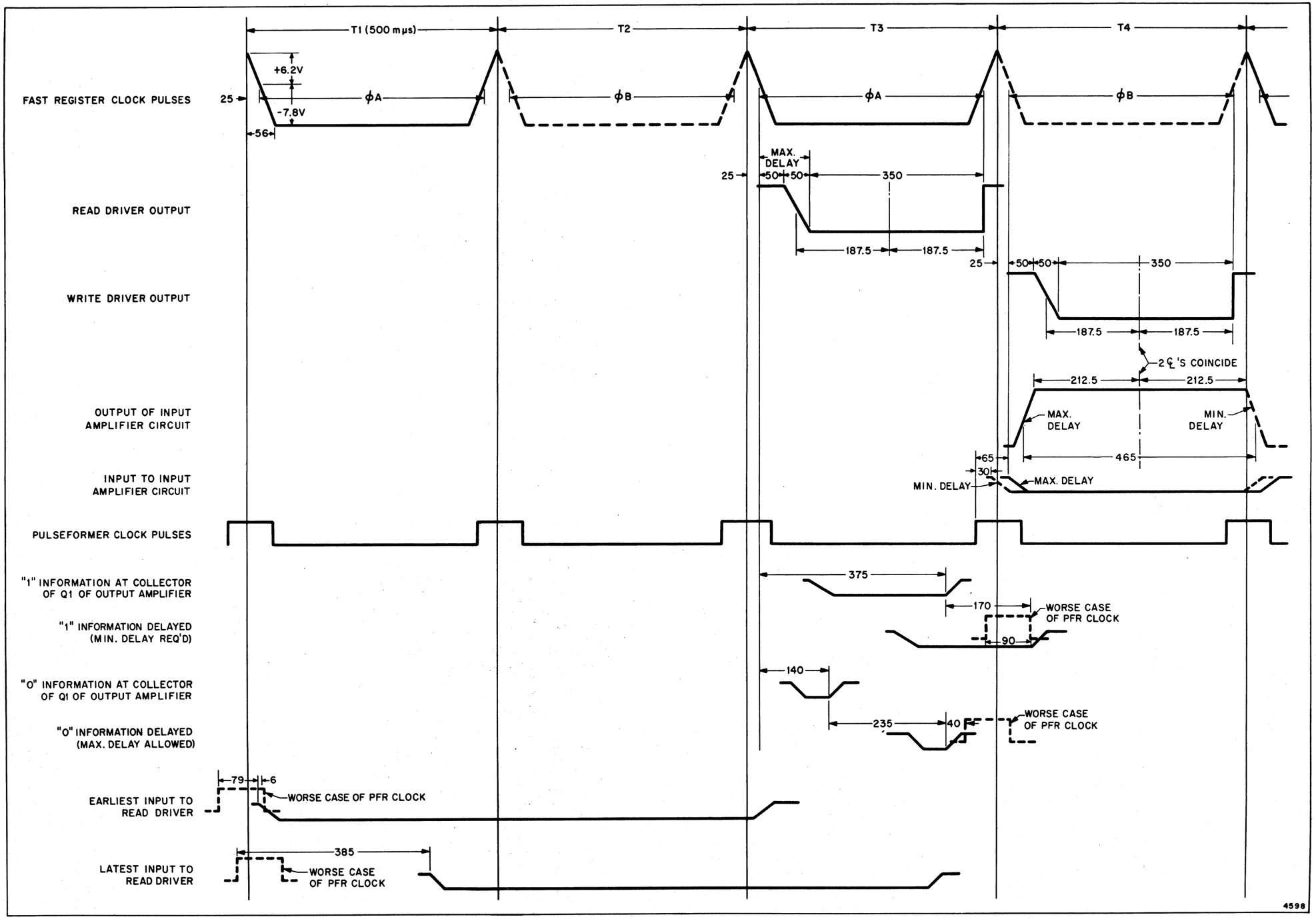

Figure 1-53. Timing Chart, A-B Register

Tables 1-10 through 1-13 give some information on the configurations of each of the fast-register frame assemblies. Each table lists the cards of the register frame, their contents, and their function in the circuit. The functions of the different circuits on the cards correspond to the schematics shown in figures 1-49 through 1-52. Note again that more data on interconnections between the circuit types will be supplied in the descriptions of Larc logic.

Table 1-10. A-B Register Frame: Inventory of Printed-Circuit Cards

Card Numbers	Contents of Card and Circuit Function
1, 17	13 read input circuits
2, ... 7	5 output amplifiers
8, 16	13 clamp circuits
9, 25	13 read and write drivers*
10, ... 15	5 x 13 core matrix
18, ... 23	5 input amplifiers
24, 32	13 clamp circuits
26, ... 31	5 x 13 core matrix

* Magnetic-amplifier circuits.

Table 1-11. Address-Register Frame: Inventory of Printed-Circuit Cards

Card Numbers	Contents of Card and Circuit Function
2, ... 6	5 output amplifiers
17	7 read input circuits
18, ... 22	5 input amplifiers
25	7 read and write drivers*
26, ... 30	5 x 7 core matrix
31	7 clamp circuits

* Magnetic-amplifier circuits.

Table 1-12. Input-Buffer-Register Frame: Inventory of Printed-Circuit Cards

Card Numbers	Contents of Card and Circuit Function	Card Numbers	Contents of Card and Circuit Function
1	13 read input circuits (for 8 read drivers and 5 write drivers)	16	8 clamp circuits
		17	13 read input circuits (for 13 write drivers)
2, ... 7	5 output amplifiers		
8	1 voltage-divider circuit	18, ... 23	5 input amplifiers
		25	13 write drivers*
9	8 read drivers* 5 write drivers*	26, ... 31	5 read input circuits 5 write drivers
10, ... 15	5 x 8 core matrix (for drum read and tape synchronizers)	32	2 bias-control circuit components

* Magnetic-amplifier circuits.

Table 1-13. Output-Buffer-Register Frame: Inventory of Printed-Circuit Cards

Card Numbers	Contents of Card and Circuit Function	Card Numbers	Contents of Card and Circuit Function
1	13 read input circuits (for 10 read drivers and 3 write drivers)	15	14 clamp circuits
		16	10 clamp circuits
2, ... 6	5 output amplifiers	17	13 read input circuits (for 13 read drivers)
7	8 clamp circuits	18, ... 23	5 input amplifiers
8	6 clamp circuits	24	2 bias-control circuit components
9	10 read drivers 3 write drivers*	25	13 read drivers*
10, ... 12	5 x 12 core matrix (for drum write and tape synchronizers)	26, 27, 29 ... 31	5 read input circuits 5 read drivers
13, 14	5 x 6 core matrix (for printer and page-recorder synchronizers)	28	5 read input circuits 5 write drivers
		32	10 clamp circuits

* Magnetic-amplifier circuits