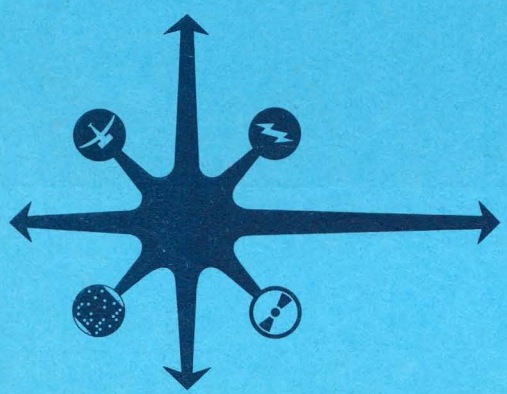
THE CP-642B COMPUTER

. . . . . a technical description



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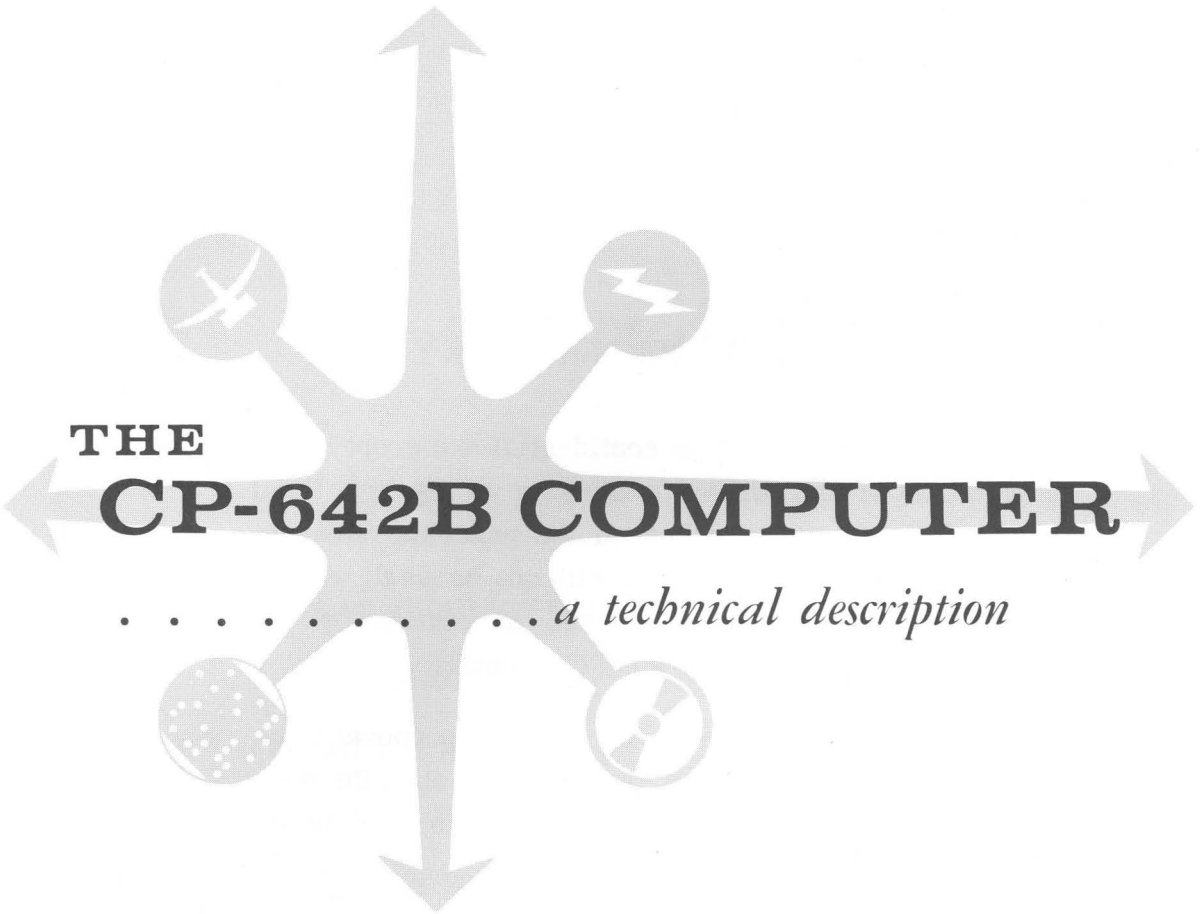

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If this document forms a portion of a proposal to an agency of the United States Government, then the provisions of ASPR 3-109 (March 1958) apply to the entirety of this document.

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PHYSICAL CHARACTERISTICS

Size:

38" wide x 32" deep x 72" high

Weight:

2400 pounds

Operating Temperature:

0° – 50° C

Cooling:

Water–6.3 gallons/minute at 70° ±5° F

Air–approximately 650 cfm at 80° F max. input

Power:

115 VAC, 3 phase, 400 cycle, 2.5 KVA (Regulated)

115 VAC, 3 phase, 400 cycle, 2 KW (Unregulated)

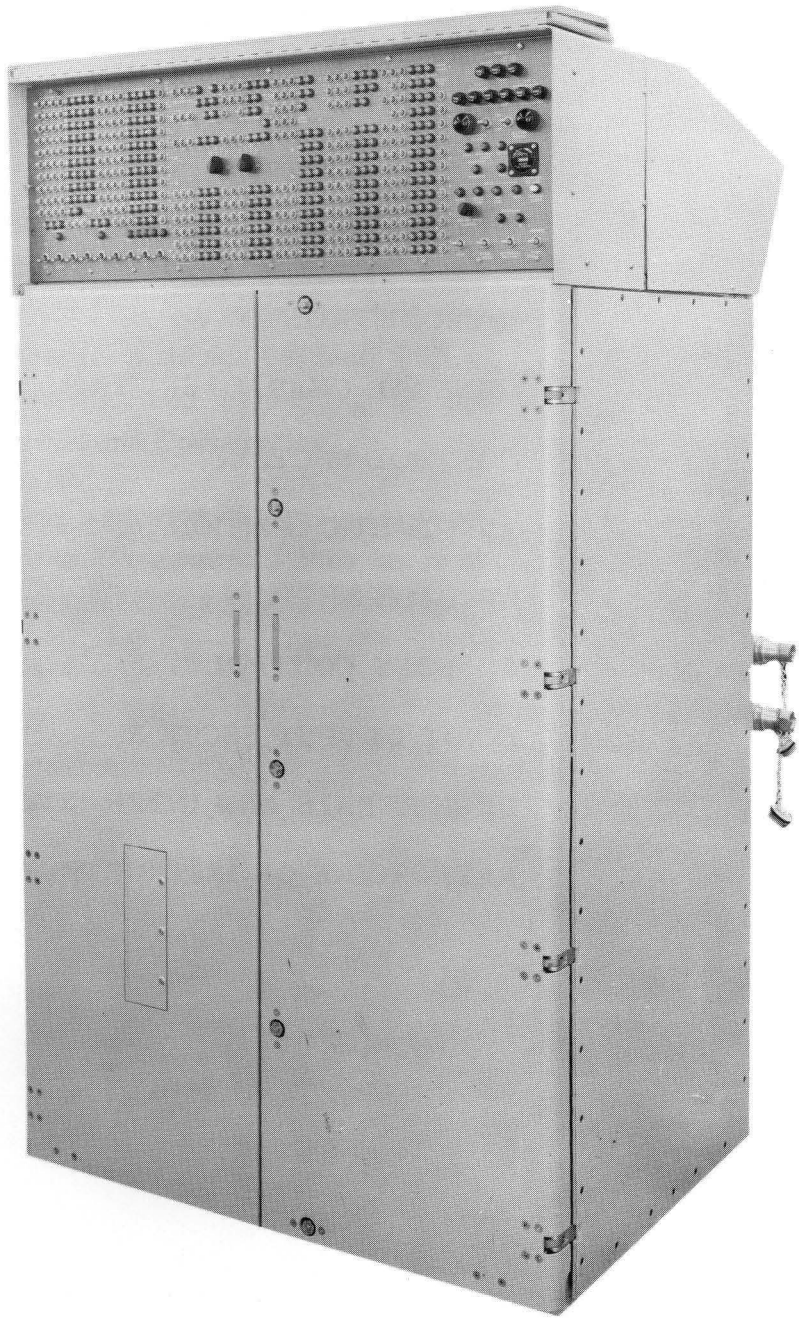


Figure 1. CP-642B Computer

THE CP-642B COMPUTER

INTRODUCTION

The CP-642B Computer is a general-purpose, stored-program machine capable of rapidly processing a large quantity of complex data. It is designed for compatibility with the AN/USQ-20 data set of the Naval Tactical Data System (NTDS). Principal features of the computer include the following:

- Internal high-speed storage with a cycle time of four microseconds and a capacity of 32,672 words;
- Control storage employing magnetic, thin film memory with a cycle time of 2/3 microsecond and a capacity of 64 words;
- Repertoire of 62 instructions, most of which provide for conditional program branches;
- 30-bit word length;
- Optional operation with 15-bit half-words;
- Internally stored program;
- Programmed checking of data parity;
- Parallel, ones' complement, subtractive arithmetic;
- Single address instructions with provisions for address modifications via seven index registers;
- Internal seven-day, real-time clock for initiating operations at desired times;
- Provision for connecting external real-time clock;
- Optional number of input and output channels of 4, 8, 12, or 16 for rapid data exchanges with external equipment or for communicating with other computers without program attention;

- Option of two interfaces; one of the NTDS interface and the other a higher speed interface for faster peripheral equipment. This option may be exercised in four-channel increments.
- Two 32-word nondestructive-readout (NDRO) memories, each with a cycle time of 2/3 microsecond, for storage of critical instructions and constants. These memories provide facility for Automatic Recovery in event of temporary program or system failure and for automatic initial loading of programs.

The following specifications were used as the basis for the design and construction of the CP-642B.

General Electronic Equipment. (Reliability, Simplicity, Material, Workmanship, Production and Central Inspection, Ease of Operation and Maintenance)	MIL-E-16400D (3)
Enclosure	MIL-STD-108D
Technical Manual	MIL-M-16616 (1)
Drawings	MIL-D-70327 (1)
Preparation for Delivery	MIL-E-17555
Radio Interference	MIL-I-16910A (2)
Vibration	MIL-STD-167

GENERAL CHARACTERISTICS

A. Organization

The CP-642B Computer is especially suitable for such real-time applications as missile guidance, range safety, process monitoring, and tactical control and display. Relative to other general purpose systems, the computer emphasizes rapid communication with external devices and large, randomly accessible, internal storage.

Single address instructions are employed most of which have an execution time of 8-12 microseconds. Instruction words are 30 bits; data words can be either 15 or 30 bits.

Internal storage of the computer consists of a 32,672-word, ferrite-core main memory. Each word may be interpreted either as a single 30-bit word, or as two 15-bit words individually addressed. A computer cycle for storage of a 30-bit word requires four microseconds.

An additional storage area, designated as Control Memory, provides 64 addressable locations with a read-restore cycle time of 2/3 microsecond. Fifty-six of these locations are special purpose and provide storage for Input Buffer Control words, Output Buffer Control words, Output Command Buffer Control words, the Real Time clock, and seven index registers. The other eight memory locations are used for data storage. Instructions cannot be run from the control memory, however, input/output transfers can take place to or from this memory, and any operand reference can be accomplished.

Arithmetic and logical operations are performed in the parallel binary mode. For most operations, the result appears in a 30-bit accumulator register. Arithmetic is ones' complement, subtractive, with a modulus $(2^{30}-1)$.

Computer operation is controlled by a stored program capable of self-modification. Each program instruction contains a function code (6 bits), an instruction operand designator (15 bits), and three execution modifiers (3 bits each). Execution modifiers provide for address incrementation, operand interpretation, and branch-point designation. The operand may be increased by the amount contained in any one of seven index registers. The operand specified by the execution address may be interpreted as a 30-bit quantity, or as a 15-bit half-word with or without sign extension. The next sequential program step may be skipped as it is under control of the content of either the Accumulator or the Q register.

Communication between the computer and its associated external equipment is normally accomplished by a buffered transfer of data, with timing under control of the external device. Operating asynchronously with the main computer program, such transfers of data have independent access to storage. The number of data words transferred is under program control by specifying the first and last memory address in the buffer.

The input/output section of the computer is capable of communicating with other CP-642B computers, with the CP-642A computer; with the UNIVAC 1218 computer; with NTDS peripheral equipments; and with other military and commercial peripheral equipments.

A communication path is established by a sequence of request and response signals between external equipment and computer. The request signal may originate in either the computer or the external device. External request signals interrupt the main computer program and cause the computer to establish a communications channel. Once the communication link has been created, the computer returns to the main program sequence and transfer of input or output data proceeds without program reference until completed.

Sixteen-input and 16-output channels are provided in the computer; each channel consists of 30 parallel data lines plus control lines. Two different types of interfaces are employed and a group of four channels may be converted from Type I to Type II and vice versa by simply changing plug-in, printed-circuit cards within the channel circuitry.

- Type I input/output chassis is capable of communication with peripheral equipment only. (Either fast or slow interface may be used, depending upon the type of I/O amplifiers plugged into the chassis.)
- Type II input/output chassis is capable of communicating with either another computer or, by changing printed-circuit jumper cards, with peripheral equipment. (Either fast or slow interface may be used, depending upon the type of I/O amplifiers plugged into the chassis.)

In addition to data words, output channels carry External Function words to the external equipment. These words specify the function that the external device is to perform. Control of the External Function signal is accomplished in block transfers. This feature allows the computer to continue engaging

an external device after the completion of each function. An External Function Word to a tape control unit, for example, may specify "Rewind Tape Unit 2". When Tape Unit 2 has informed the computer that the tape has been rewound, the computer may immediately respond by transmitting another External Function Word, for example, "Write on Tape Unit 1" without program interruption. Acceptance of input data is controlled by Priority and Access Control logic.

The Priority and Access Control circuitry assigns access to control and core memory. If two or more requests for access to memory are received simultaneously, the priority and access circuitry evaluates the requests and assigns function priority according to an established sequence as follows:

- Advance Real-Time Clock
- External Function
- Output Request
- Input Request
- External Interrupt
- External Function Monitor Interrupts
- Output Monitor Interrupt
- Input Monitor Interrupt

If two or more channels simultaneously request the same type of access, the priority and access circuitry assigns channel priority in descending order of channel numbers.

B. Construction

The computer (Figure 1) is housed in a single cabinet, 37-inches deep, 38-inches wide, and 72-inches high. Thirteen chassis trays (viz., seven of logic, one of control memory, and five of main memory) are horizontally arrayed within the cabinet (Figure 2). Logic modules (Figure 3) are encapsulated printed-circuit cards which plug into the trays (Figure 4). Maintenance test points at the front of the trays are readily accessible.

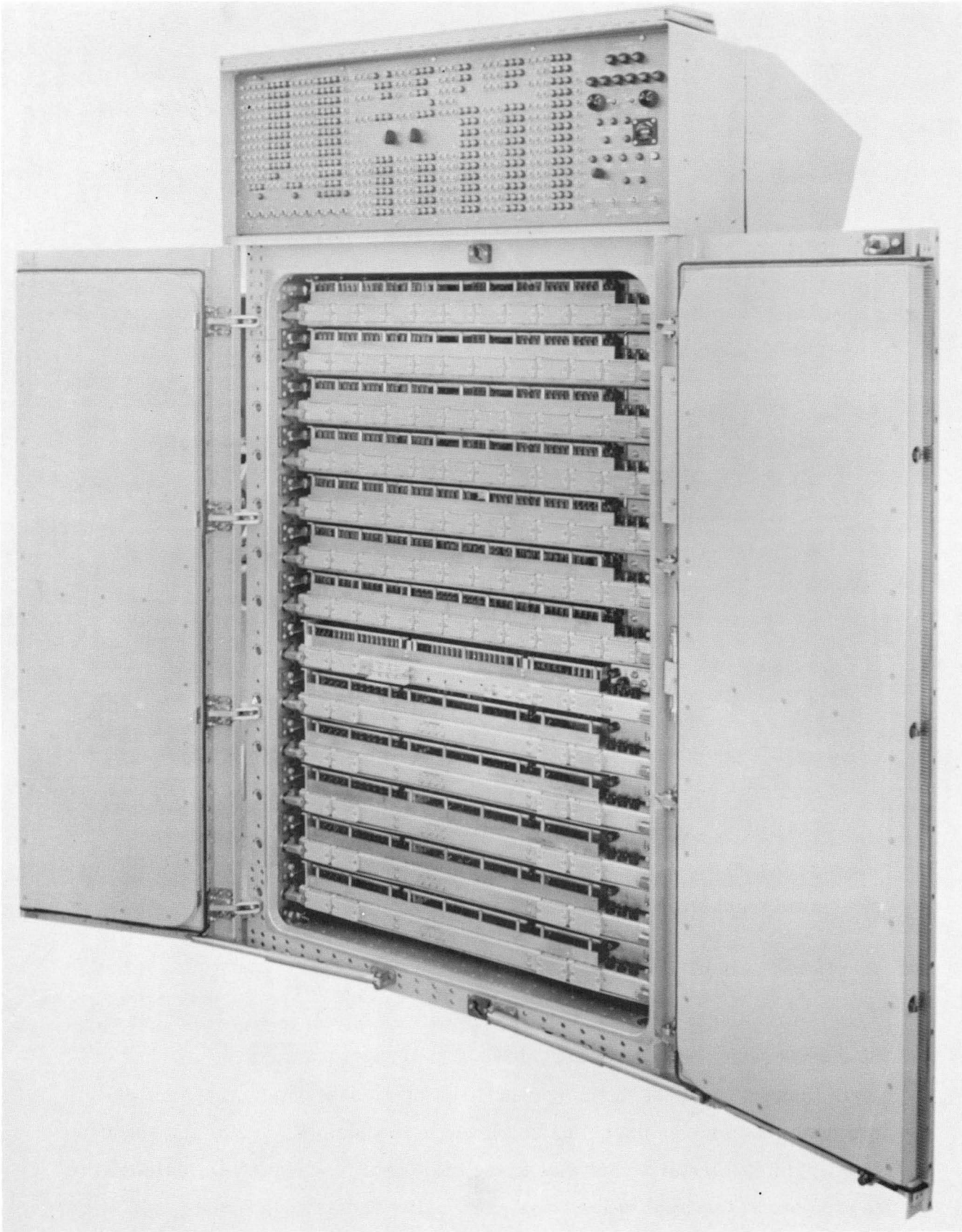


Figure 2. Computer Cabinet Interior

Computer cabinet doors, closed during normal operation, can be opened for maintenance. The maintenance and control panel, built into the upper part of the cabinet, contains register indicators, set and clear pushbuttons, and operating switches.

Primary power to the computer is provided from a motor-alternator that has a 60-cycle input and a 400-cycle output. The alternator, in addition to converting frequency, isolates the computer from the main power source. A maximum of 3.0 kilowatts input to the alternator is required for the computer.

The standard computer is equipped with a water-cooled heat exchanger but a plenum which uses ambient air as a coolant is available as an option. Inter-equipment cabling enters the computer at the top of the cabinet and may be run either overhead or through floor ducts.

The computer is designed and constructed to withstand severe shock and vibration. It may be installed aboard ship or in a trailer without modification.

CONTROL SECTION

The CONTROL SECTION (see Figure 5) consists of those registers and circuits necessary to procure, modify, and execute the instructions of the program.

The U-register (30 bits) is the program control register. It holds the instruction word during execution of an instruction. The function code and the various execution modifiers are translated from appropriate sections of the register. The lower-order 15 bits of the U-register have additional properties, modulus $2^{15}-1$.

The 15-bit B-registers, B_1 thru B_7 store the quantities used for address modification. These B-registers, also called index registers, occupy the lower 15 bits of the Control Memory addresses.

The R-register (15 bits) has counting properties to increase the contents of a selected B-register. The output of this register is made available to the control adder for modifying the lower 15 bits of the U-register.

The B-register (15 bits) is a nonaddressable control communications register. It holds the quantity added to the lower-order 15 bits of the U-register during address modification (i.e., the contents of the selected B-register).

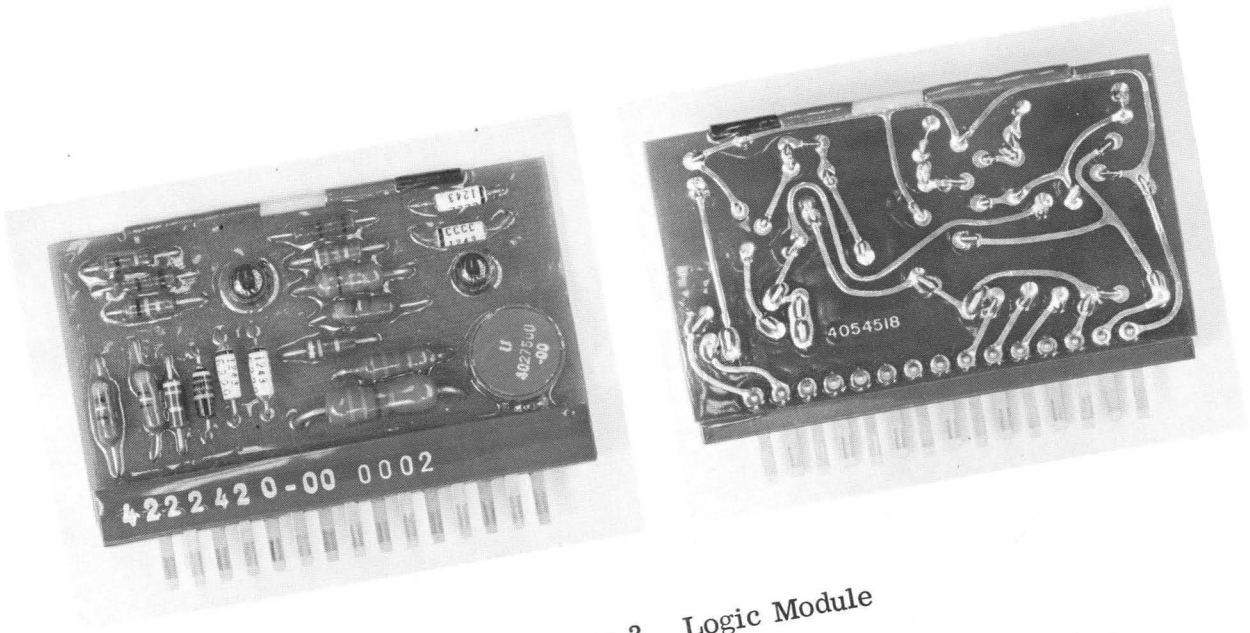


Figure 3. Logic Module

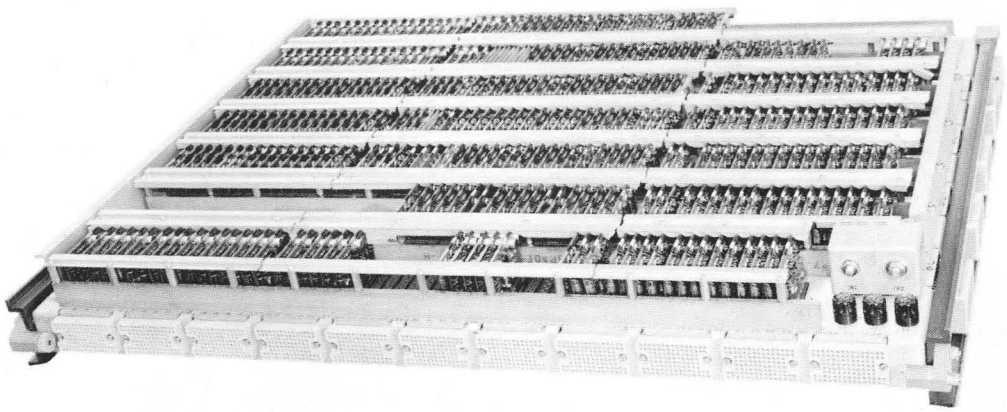


Figure 4. Tray Assembly

The P-register (15 bits) holds the memory address of a computer instruction word — that of the current instruction or a new instruction (e.g., as a result of a jump condition).

The S-register (15 bits) holds the storage address during memory references. At the beginning of a storage access period, the address is transferred to the S register. The contents of the S-register are then translated to activate the storage selection system.

The S_ϕ-register (seven bits) acts in the same manner as the S-register except that it holds the address for Control Memory during the memory cycle time.

The K-registers (K_1, K_2 and K_3) function as a shift counter for all arithmetic operations that involve shifts. Other instructions employing the K registers are Multiply, Divide, and Square Root.

ARITHMETIC SECTION

The ARITHMETIC SECTION performs numeric and logical calculations. Though greatly simplified, Figure 5 shows the important components of the Arithmetic Section: The A-, D-, Q-, X-, and W-registers and the add network.

The A-register (30 bits) may be thought of, for programming purposes, as a conventional accumulator. Because of the logic employed, however, the A-register is actually only the main rank of the accumulator; the D-register serves as a second rank.

The ADD operation is typical of the relationship between the A and D registers: the augend and addend are initially contained in the A and D. Before the addition is performed, the contents of the A-register are transmitted to the X-register. The values of X and D are combined by the add network to form the sum of the two numbers in a parallel manner and placed in the A-register.

The Q-register (30 bits) is used principally during multiply and divide operations. The contents of both A and Q may be shifted left or right, either individually or as one double-length 60-bit word.

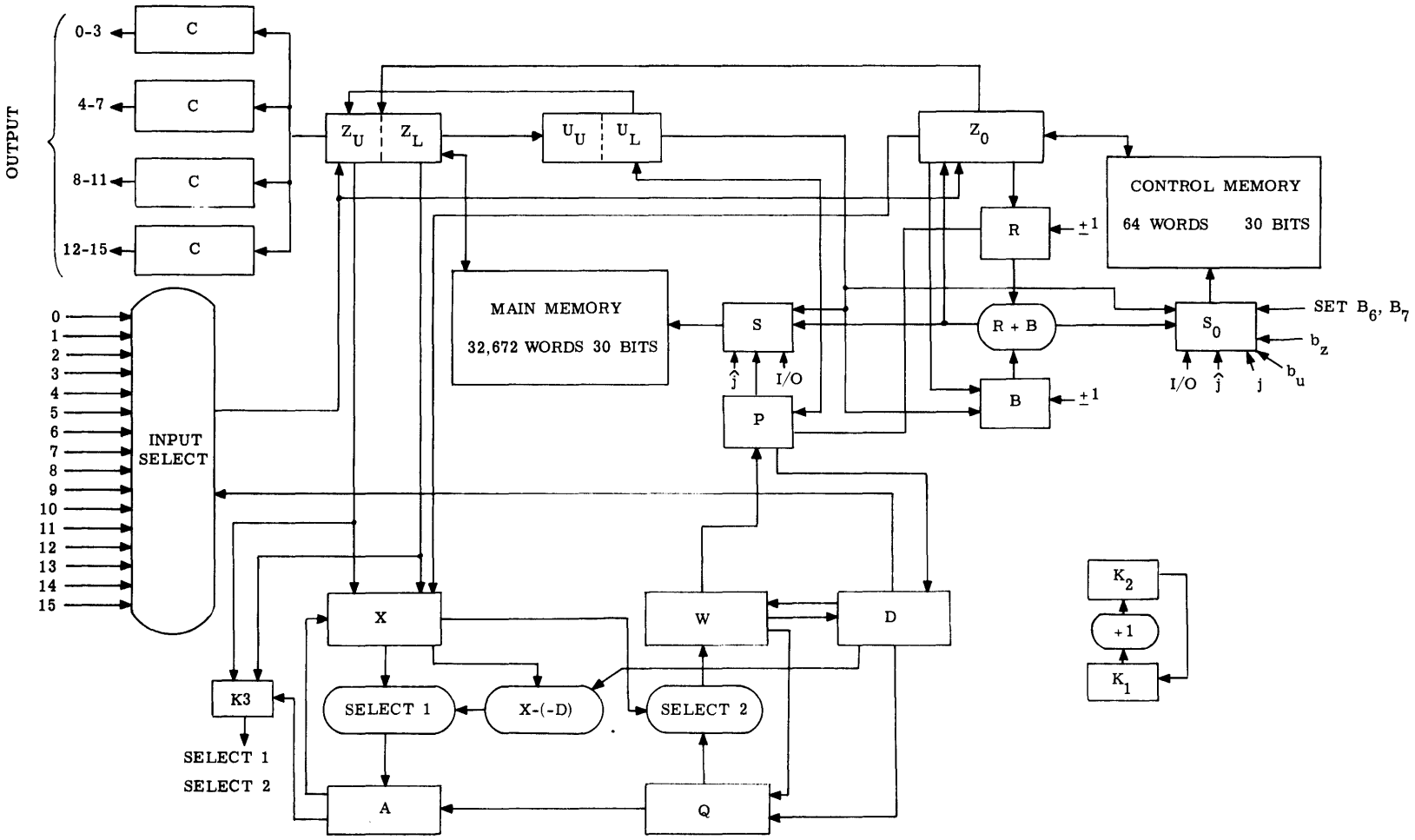


Figure 5. Simplified Block Diagram of CP-642B Computer

The X-, D-, and W-registers are 30-bit, non-addressable registers. These registers are used primarily either for the exchange of data within the arithmetic section or for communicating with the remaining sections of the computer. The W-register is not displayed on the control panel of the computer; the A-, Q-, X-, and D-registers do have indicators which allow the operator to inspect the contents of these registers during debugging operations.

STORAGE SECTION

The STORAGE SECTION consists of three basic memories. These are:

- The Main Storage section constructed of modular arrays of ferrite cores.
- The Control Memory constructed from the magnetic thin-film elements.
- The Bootstrap Memory, a nondestructive readout type, which utilizes the UNIFLUXOR type of storage.

The Main Storage section has a capacity of 32,672 words of 30 bits each. It is coincident-current driven, and is addressed via the address translator. Contents of the location specified by the address is read into the 30-bit, Z-register. Because of optional use of 15-bit half-words, Z is split into two 15-bit sections termed Z-upper (Z_u) and Z-lower (Z_L).

The memory operates in the destructive readout mode. Time required for the read/restore cycle is four microseconds.

The Control Memory can store 64 words of 30 bits each. This memory stores the seven B-indexing registers, the control words for the Input/Output section, and the Real-Time Clock. Address locations of the Control Memory are numbered from 00100 to 00177 and may be referenced to obtain any operand. No instruction can be run from control memory; if this is attempted, the computer will fault.

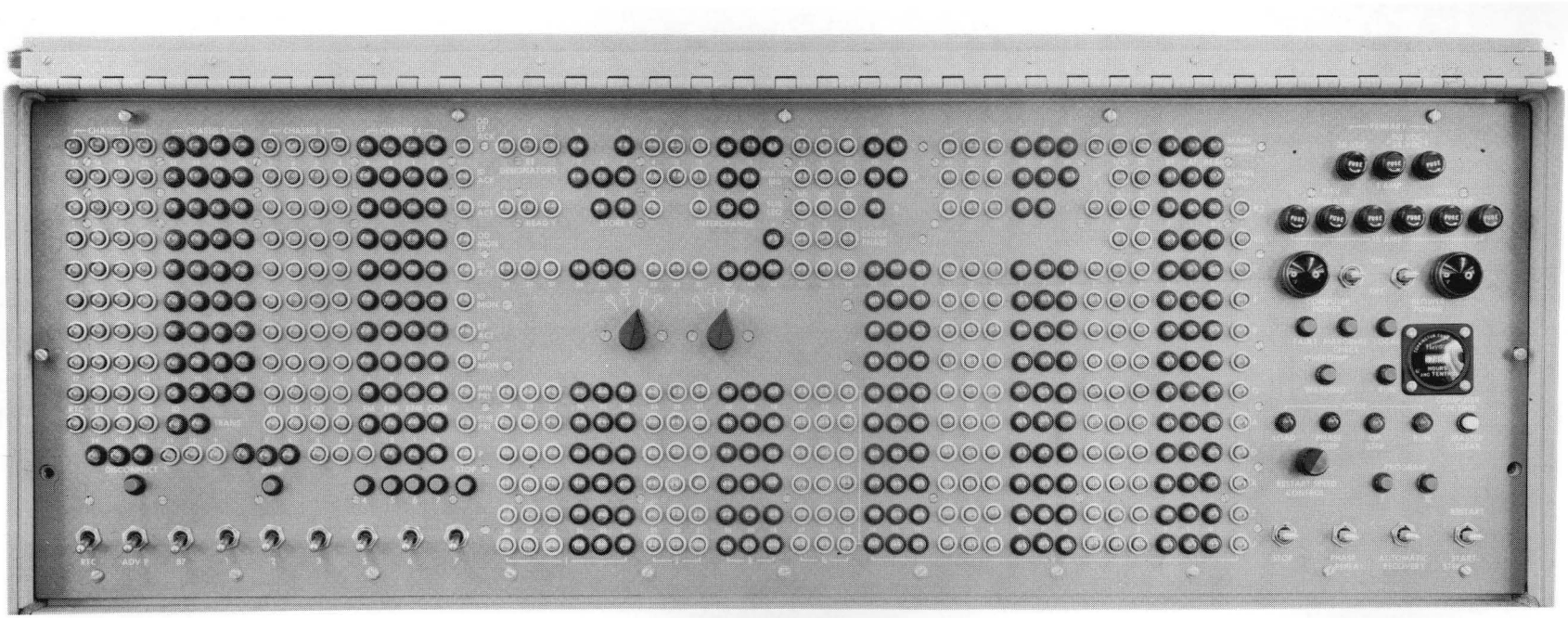


Figure 6. Maintenance Panel of CP-642B Computer

The magnetic thin-film memory is the fastest form of memory yet developed for computer use. The storage media consists of spots of a permalloy ferro-magnetic material, deposited upon a substrate such as a thin glass plate. The permalloy spots are 50 mils in diameter and 1,000 angstroms thick. The geometry of these spots permits the magnetic state of a spot to be switched in billionths of a second with only a small amount of power applied. Since these spots have only two stable states of magnetization, they can readily store binary information.

The cycle time for read/restore of data in the control storage is 667 nanoseconds (2/3 microsecond). This rapid access to the memory increases the usefulness of applications of the computer.

The UNIFLUXOR storage is a nondestructive-readout (NDRO) type of memory used in the computer for automatic program recovery (i.e., in bootstrap programs). This storage area is capable of reading 64 words with a read cycle time of 2/3 microsecond per word. Either one of the two 32-word bootstrap programs in the UNIFLUXOR storage may be selected by a switch. The UNIFLUXOR memory may be entered from any point in a program, and an exit from this memory area requires no special instruction.

The control and UNIFLUXOR memories are referenced by the S_{ϕ}-register; the data is received by the Z_{ϕ}-register.

CONSOLE CONTROL

The maintenance and control panel (see Figure 6), located on the upper front of the computer, includes indicator lamps which display a detailed report of the internal status of the computer, and controls to permit manual initiation of various operations. It is not necessary during normal operations, however, to monitor the maintenance panel or console.

Each register is represented on the maintenance panel by a row of display lamps each of which can be used to manually enter a "one" into the corresponding bit-position, and a Clear button which can be used to enter zeros manually into all bit-positions of the register. Many of the registers are involved only in the mechanics of executing instructions, and are not directly accessible to the program.

B. Special Modes

The maintenance and control panel provides manual controls for selecting the following special modes of operation:

- Execution of one program instruction for each depression of a switch.
- Execution of consecutive program instruction at a low controllable rate.
- Execution of one master clock phase each time a switch is depressed.
- Execution of consecutive master clock phases at a low, controllable rate.
- Operation that is normal except that the computer does not stop for a programmed STOP instruction. (Such operation is called abnormal high-speed operation.)

The console provides manual controls that may be used either to disable the real-time clock, to inhibit the decrementing of the B-7 register, or to inhibit incrementing of the program address (P) register. These options enable the operator to suspend normal operation temporarily without affecting such operation when it is subsequently resumed. Such suspensions could include stopping the computer or temporary operation in one of the special modes.

INPUT/OUTPUT SECTION

A. General

Communication with the CP-642B Computer is carried on in a 30-bit, parallel mode over the input/output channels. Each computer is equipped with 16 channels (numbered 0 through 15). These channels are implemented on four chassis, each of which contains four identical input/output channels. Two different types of chassis can be used with the CP-642B Computer. Type I communicates with peripheral equipment. Type II communicates either with peripheral equipment or with another computer. The conversion from a peripheral equipment channel to an inter-computer channel on Type II chassis involves the changing of one plug-in jumper card per channel.

Either of the two types of chassis can be provided with a fast or slow interface. The slow interface provides communications transfer rates of up to a nominal 40 KC per channel. The CP-642A/USQ-20 provided transfer rates up to a nominal 30 KC per channel. The fast interface will provide transfer rates of up to 125 KC per channel.

In the CP-642A Computer, the transfer of input and output data words is asynchronous with the computer program, but the program maintains synchronous control over the issuance of External Functions. In the CP-642B Computer, transmission of External Functions will be handled the same as data transmission. The peripheral equipment will set a line indicating it is capable of accepting a control word from the buffer. Therefore the transmission of the word is not synchronous with the computer program. Provision has been made, however, to achieve synchronization of program and I/O control to be compatible with existing peripheral equipments.

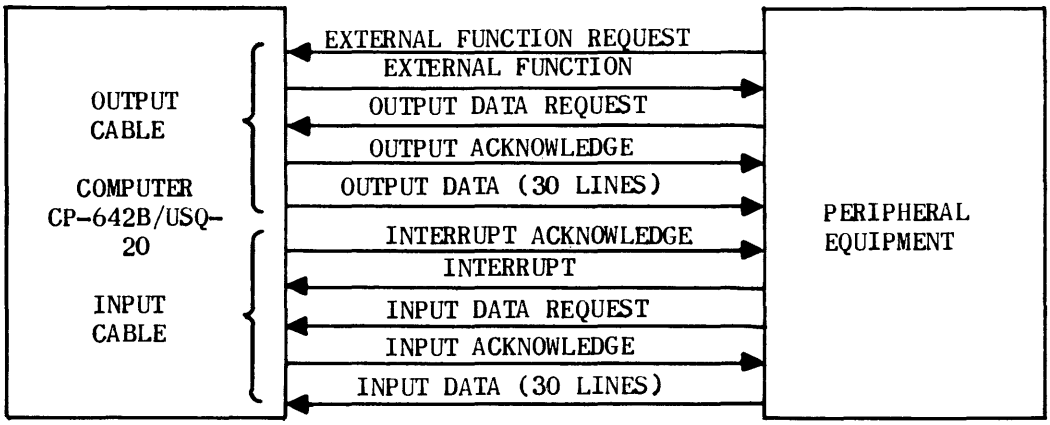


Figure 7. Computer to Peripheral Equipment Interface

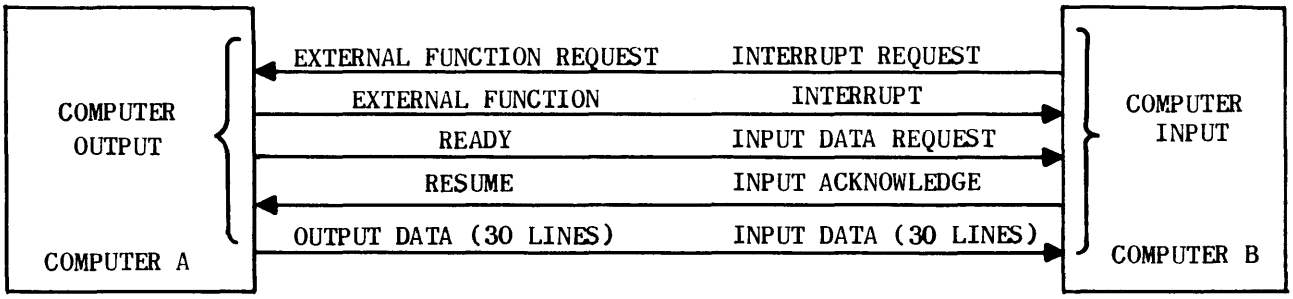


Figure 8. Computer to Computer Interface

All external equipment must adequately resynchronize all control signals (i.e., signals other than data). Resynchronization includes sensing the transition from the "zero" to the "one" state and gating the generated signal against a steady "one" state of the control signal to guard against false triggering on noise pulses.

> NOTE: All references to input and output are made with the standpoint of the computer; that is, 'input' is input to the computer and 'output' is output from the computer.

B. Control Communication

The CP-642B Computer is designed to use a d-c level input/output system. Signals are d-c levels which may be changed upon interchange of control information. Signals may exist for microseconds or for days, depending upon the nature of the particular task.

It should be noted that the control lines are carried in the same cables as the data lines and have the same voltage levels. Hence, delay times, rise and fall times, and storage times are similar.

C. Computer to Peripheral Equipment Interface

1. DATA AND CONTROL SIGNALS

The 16-input channels and 16-output channels each have an associated cable (32 possible cables), and each cable has 30 data lines plus four control lines. Table 1 compares control line designations in the CP-642A/USQ-20 and the CP-642B Computers.

The interface between the CP-642B Computer and various peripheral equipments is illustrated in Figure 7. The functions of three of the control lines on each cable are the same as in CP-642A/USQ-20 operation; however,

TABLE 1. CONTROL SIGNALS IN NORMAL PERIPHERAL EQUIPMENT CHANNELS

Signal Origin	Functional Name (CP-642B)	Equivalent Signal in CP-642A/USQ-20
P E	External Function Request	(None)
C	External Function	External Function
P E	Output Data Request	Output Data Request
C	Output Acknowledge	Output Acknowledge
C	Interrupt Request	(None)
P E	Interrupt	Interrupt
P E	Input Data Request	Input Data Request
C	Input Acknowledge	Input Acknowledge

P E = Peripheral Equipment; C = Computer

an additional control signal has been added to implement an improved technique for the handling of control words between computer and equipment. Note the direction of information flow. The Data Request signals are always sent from the peripheral equipment to the computer. The Acknowledge signals are always sent from the computer to the peripheral equipment.

2. SEQUENCE OF EVENTS

The sequence of events for each of the four cases of communication between the computer and peripheral equipment is given below.

Normal output sequence for data transfer from computer to peripheral equipment (buffer mode):

a) Computer initiates output buffer for given channel.

b) Peripheral equipment sets the Output Data Request Line indicating that it is in a condition to accept data.

c) Computer detects Output Data Request.

d) Computer (at its convenience) places information on the 30 data lines.

e) Computer sets the Output Acknowledge line, indicating that the data is ready for sampling.

f) Peripheral equipment detects the Output Acknowledge.

g) Peripheral equipment may drop Output Data Request any time after detecting Output Acknowledge.

h) Peripheral equipment samples the 30 data lines.

i) Computer drops Output Acknowledge and data lines.

Steps b) through i) of this sequence are repeated for every data word until the number of words specified in the output buffer have been transferred.

Sequence for transmitting an External Function code from computer to peripheral equipment.

a) Peripheral equipment sets the External Function Request line when it is ready to accept an External Function code.

b) Computer detects External Function Request.

c) Computer places the External Function code on the data lines (if its External Function buffer is active).

d) Computer sets the External Function line to indicate that the External Function code is ready for sampling.

e) The External Function clears the External Function request at the peripheral equipment.

f) Peripheral equipment samples the External Function code.

g) Computer drops the External Function line and the External Function code.

h) The sequence is repeated when the peripheral equipment is ready to accept another External Function code.

Normal input sequence for data transfer to computer from peripheral equipment (buffer mode):

a) Computer initiates input buffer for given channel.

b) Peripheral equipment places data word on 30 data lines.

c) Peripheral equipment sets the Input Data Request line to indicate that it has data ready for transmission.

d) Computer detects the Input Data Request.

e) Computer samples the 30 data lines at its own convenience.

f) Computer sets the Input Acknowledge line, indicating that it has sampled the data.

g) Peripheral equipment senses the Input Acknowledge line.

h) Peripheral equipment drops the data lines and the Input Data Request line.

Steps b) through h) of this sequence are repeated for every data word until the number of words specified in the input buffer has been transferred.

Sequence for transmitting an Interrupt from peripheral equipment to the computer.

a) Computer sets the Interrupt Request when it is ready to accept an External Interrupt.

b) Peripheral equipment detects the Interrupt Request.

c) Peripheral equipment places the Interrupt word on the data lines.

d) Peripheral equipment sets the Interrupt line to indicate that the External Interrupt word is on the data lines.

e) Computer detects the Interrupt signal and, at its convenience, accepts the Interrupt word.

f) Computer drops the Interrupt Request.

g) Peripheral equipment detects the drop of the Interrupt Request and clears the Interrupt line and the data lines.

NOTE: The Input Acknowledge of an interrupt will be initiated at the same time that the Interrupt Request is cleared. The simultaneous occurrence of these conditions should be used by peripheral equipment to differentiate between an Interrupt Acknowledge and a Data Acknowledge.

D. Computer to Computer Interface

1. DATA AND CONTROL SIGNALS

Since all input/output channels of the CP-642B Computer can be converted to intercomputer communication channels, it is possible for a computer to communicate with 16 other computers. The control signals governing intercomputer communication are shown in Table 2.

TABLE 2. CONTROL SIGNALS IN SPECIAL INTERCOMPUTER CHANNELS

Output Cable	Input Cable
External Function Request	Interrupt Request
External Function	Interrupt
Ready	Input Data Request
Resume	Input Acknowledge

Note that the control signals in the input cable are the same for intercomputer communication as for communication with peripheral equipment. In the output cable, Ready and Resume signals are used to control the intercomputer transfer of data.

Figure 8 illustrates the interface between two CP-642B Computers. Computer A is transmitting to Computer B.

2. SEQUENCE OF EVENTS

The sequence of events for each of the two cases of intercomputer communication appears below.

Intercomputer command word transfer from Computer A to Computer B:

a) Computer B sets the Interrupt Request when it is ready to accept a command word from Computer A.

b) Computer A recognizes the Interrupt Request as an External Function Request and places the External Function code on the data lines.

c) Computer A sets the External Function to indicate that the External Function code is on the data lines.

d) Computer B recognizes the External Function as an Interrupt and accepts the command word.

e) Computer B clears the Interrupt Request line and sets the Input Acknowledge line.

f) Computer A recognizes the Input Acknowledge as a Resume and clears the External Function line.

NOTE: In the event that Computer A sets the External Function line while the Interrupt Request line is cleared (this is possible when an External Function with Force instruction is used), all communications on the associated group of output channels in A will be suspended until Computer B acknowledges receipt of the External Interrupt or until an intercomputer Time-Out Interrupt in A permits A to resolve the problem.

Intercomputer data transfer from Computer A to Computer B:

a) Computer B initiates an input buffer and Computer A initiates an output buffer for the required channel.

b) Computer A places data on the data lines.

c) Computer A sets the Ready line to indicate that the data is on the lines.

d) Computer B recognizes the Ready signal as an Input Data Request signal and, at its convenience, accepts the data word.

e) Computer B sets the Input Acknowledge.

f) Computer A recognizes the Input Acknowledge as a Resume signal and clears the Ready and data lines.

g) The cycle is repeated for each word to be transferred.

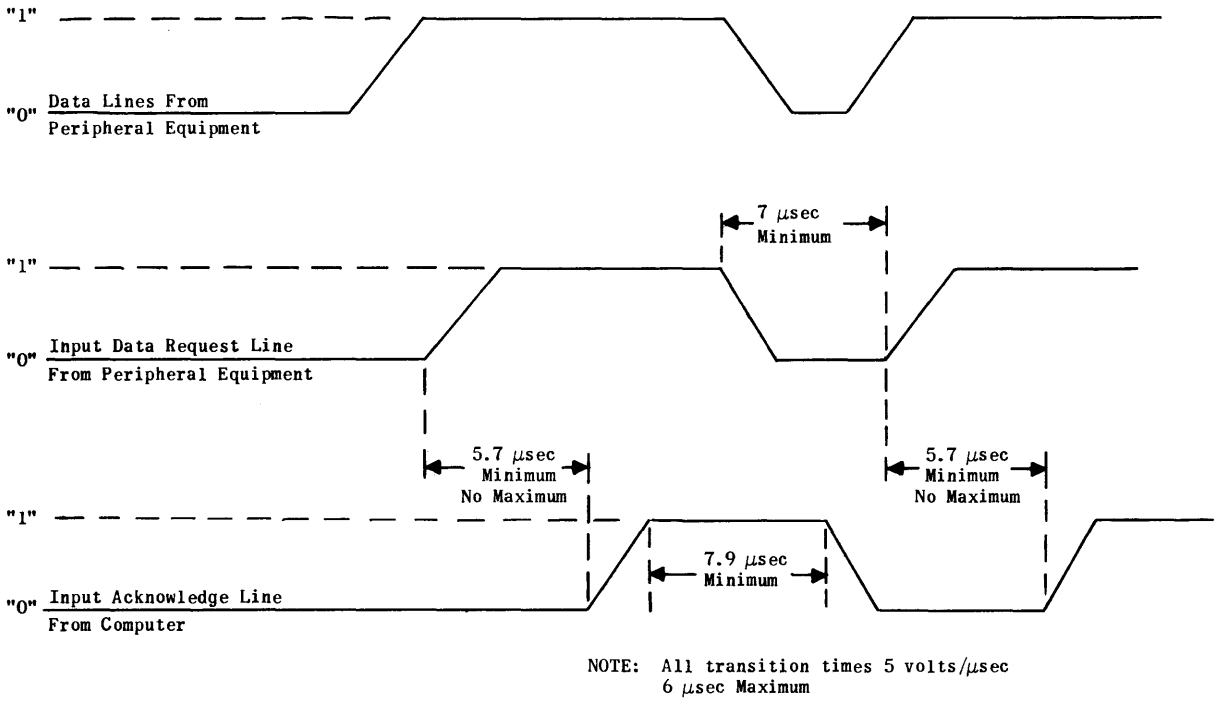
E. Timing - Slow Interface

When transmitting data from computer to equipment, data lines must be stable before being sampled. Hence a time delay exists between the computer's loading of an output register and the energizing of the Output Acknowledge or of the External Function signal.

1. INPUT DATA TIMING CONSIDERATIONS

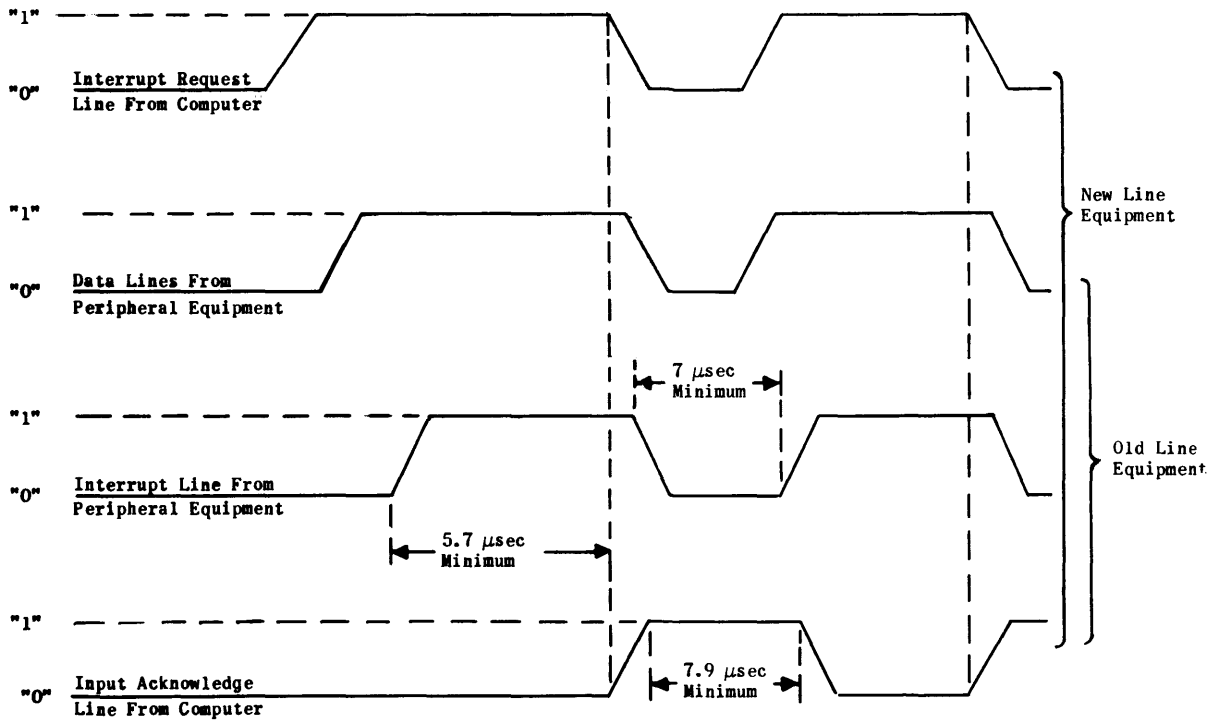
The Input Data Request signal indicates to the computer that data has been placed on the 30 Input Data Lines. To ensure that the data will be accepted, the Input Data Request must be maintained on the lines until an answering Input Acknowledge is received. As shown in Figure 9, there is a 5.7 microsecond minimum delay between the setting of the Input Data Request and its answering Input Acknowledge. There is no maximum limit stated for the delay, since its value for any particular cycle is determined by the interaction with the computer program and the other input/output channels. The data lines must remain stable as long as the Input Data Request is set.

The Input Acknowledge indicates to peripheral equipment that the computer's 30 data lines have been sampled. The Input Acknowledge signal is set for a fixed time interval. The peripheral equipment must be capable of detecting as an Input Acknowledge, a signal which may exist in the stable "one" state for as little as 7.9 microseconds. The Input Data Request line



NOTE: All transition times 5 volts/μsec
6 μsec Maximum

Figure 9. Timing of Input Data Signals - Slow Interface



NOTE: All transition times 5 volts/μsec minimum
6 μsec maximum

Figure 10. Timing of External Interrupt Signals - Slow Interface

and data lines may be dropped to the "zero" state any time after detecting the Input Acknowledge. The Input Data Request cannot be reset immediately to indicate readiness of a second data word because the computer will not recognize the second Input Data Request unless a minimum time delay of seven microseconds is allowed between the start of the dropping of the first Input Data Request and the start of the setting of the second Input Data Request. The timing allows peripheral equipment requiring a maximum data transmission rate to legitimately set the Input Data Request to the "one" state for the second time before the first Input Acknowledge has dropped to the "zero" state. (See Figure 9.) This will not affect operation of the cycle however since a 5.7 microsecond minimum delay will again be required between the setting of the second Input Data Request and the setting of the second Input Acknowledge.

2. EXTERNAL INTERRUPT TIMING CONSIDERATIONS

Two different methods are used to control the transmission of External Interrupts from peripheral equipment to the CP-642B Computer. Two methods are necessary because the computer employs new and improved input/output techniques for a new line of peripheral equipments while maintaining compatibility with the existing peripheral equipments. Figure 10 shows the signals employed in the two methods of control.

When connected to the new items of peripheral equipment, the computer sets the Interrupt Request to indicate that it is able to receive an Interrupt. When sending an Interrupt, the peripheral equipments may either place the Interrupt code on the data lines first and then set the Interrupt line; or they may simultaneously place the Interrupt code on the data lines and set the Interrupt line. While the Interrupt line is set, the data lines must not be changed. The computer accepts the Interrupt code (at its convenience) and drops the Interrupt Request. To ensure that the Computer will accept the

Interrupt code, the peripheral must maintain the Interrupt signal until the Computer simultaneously drops the Interrupt Request and sets the Input Acknowledge. As shown in Figure 10, there is a 5.7 microsecond minimum delay between the setting of the Interrupt line and the dropping of the Interrupt Request. No maximum limit is placed on this delay since for any cycle its value is determined by the interaction between the computer program and the other input/output channels. The dropping of the Interrupt Request indicates to the peripheral equipment that the computer is no longer able to accept Interrupts on that input channel.

When the computer drops the Interrupt Request signal it also sets the Input Acknowledge signal to inform the peripheral equipment that it has accepted the Interrupt code. Note that the existing peripheral equipments can initiate an Interrupt transfer without monitoring the Interrupt Request line from the computer. This characteristic does not alter the timing sequence since the computer will accept the Interrupt code at its own convenience.

3. OUTPUT DATA AND EXTERNAL FUNCTION TIMING CONSIDERATIONS

The timing involved in the transfer of both data words and External Function words is discussed in the following paragraphs.

Peripheral equipment must first set the Output Request line or EF Request line indicating that it is in a condition to accept a data or EF word from the computer. This is necessary because the word will be available to the peripheral equipment in a stable state for an interval that, if the computer is performing output operations at the maximum rate, may be as short as 17.0 microseconds. Data lines will not necessarily be cleared to the "zero" state before being reset to the "one" state. The minimum time interval between the Output or EF Request signal and the placement of answering data on the lines is 5.7 microseconds. The maximum time interval depends upon the computer program, the priority of the particular channel, and the data request rates of the other peripheral equipment.

The Output Acknowledge or External Function signal indicates to the peripheral equipment that the requested word is nowpresent on the data lines and that the lines should now be sampled. As shown in Figure 11, the Output Acknowledge or External Function signal will be sent a minimum of 3.7 microseconds after the data has been placed on the lines. The peripheral equipment must be capable of recognizing, as an Output Acknowledge or an EF, a signal which may exist in the stable "one" state for as short a time as 7.9 microseconds. The computer will maintain stable data on the lines for a minimum of 3.9 microseconds after it starts to drop the Output Acknowledge or EF.

The Output or EF Request may be dropped to the "zero" state any time after detecting the Output Acknowledge or the EF. The Output or EF Request cannot be reset immediately to indicate readiness of the peripheral equipment to accept a second word because the computer will not recognize the second Output or EF Request unless a minimum time delay of seven microseconds is allowed between the start of the dropping of the first Output or EF Request and the start of the setting of the second Output or EF Request. Figure 11 shows that the timing would allow any peripheral equipment that wishes to receive data from the computer at a maximum rate, to legitimately set the Output or EF Request to the "one" state for the second time before the first Output Acknowledge or EF has dropped to the "zero" state. However, this will not affect operation of the cycle since a 5.7 microsecond minimum delay will again exist between the setting of the second Output or EF Request and the availability of the second word on the data lines.

4. OUTPUT TIMING CONSIDERATIONS FOR EXTERNAL FUNCTIONS WITH FORCE

External Functions with Force are unique in that no request is sent by the peripheral equipment. The computer places the External Function code

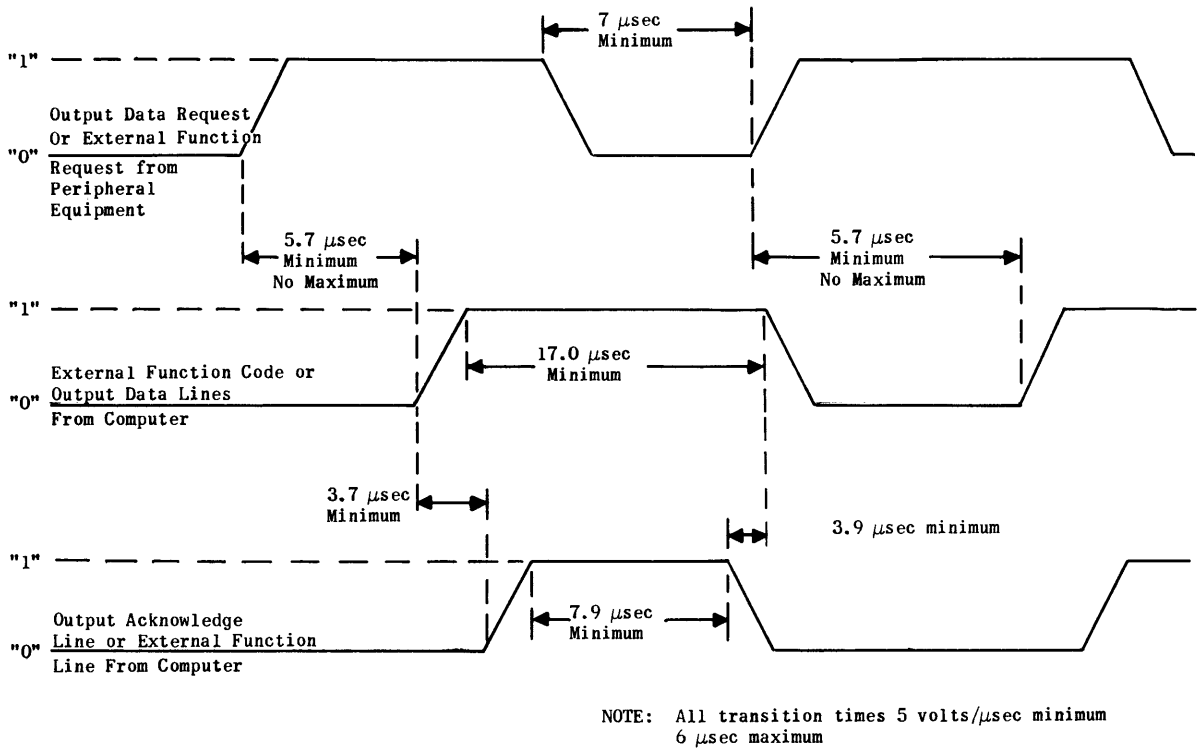


Figure 11. Timing for Normal Output Signals - Slow Interface

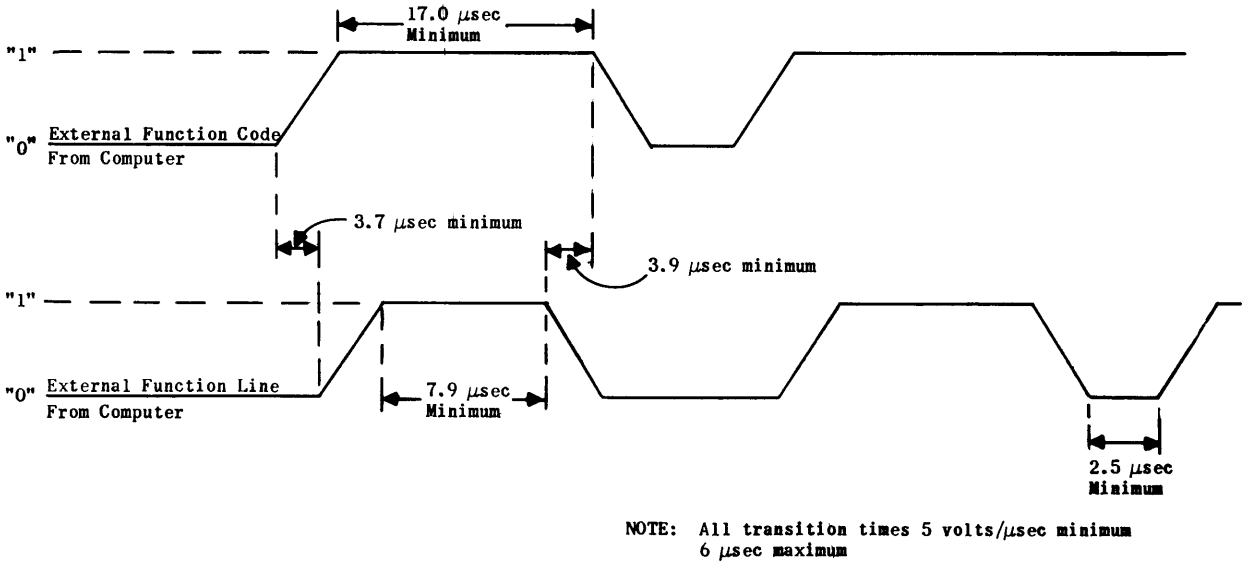


Figure 12. Timing for External Functions with Force - Slow Interface

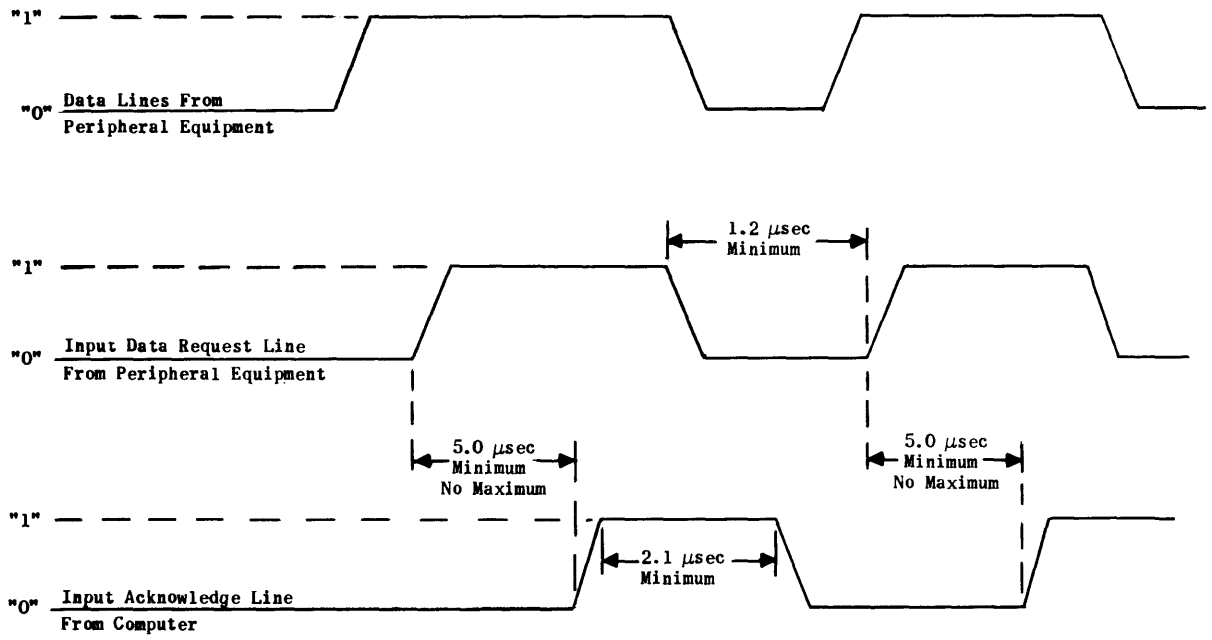
on the 30 output data lines, and a minimum of 3.7 microseconds later energizes the External Function Line. The External Function signal indicates to the peripheral equipment that an EF code is present on the data lines, which should now be sampled. The External Function line will remain in the stable "one" state for an interval which may be as short as 7.9 microseconds. The EF code will remain on the data link for a minimum of 3.9 microseconds after the External Function signal begins to drop.

The peripheral equipment has no control over the rate at which External Functions with force are sent. If two External Functions with force to the same peripheral equipment are executed consecutively, the result will appear as in cycles 2 and 3 depicted by Figure 12. The External Function line will drop to the "zero" state for an interval which may be as short as 2.5 microseconds. If the peripheral equipments cannot accept External Functions at this rate, restrictions must be made in the programming of External Function instructions to the equipment. It should be noted that, since the existing peripheral equipments have no provision for sending an External Function Request signal, all External Functions to existing peripheral equipment must be sent as External Function with force.

F. Timing - Fast Interface

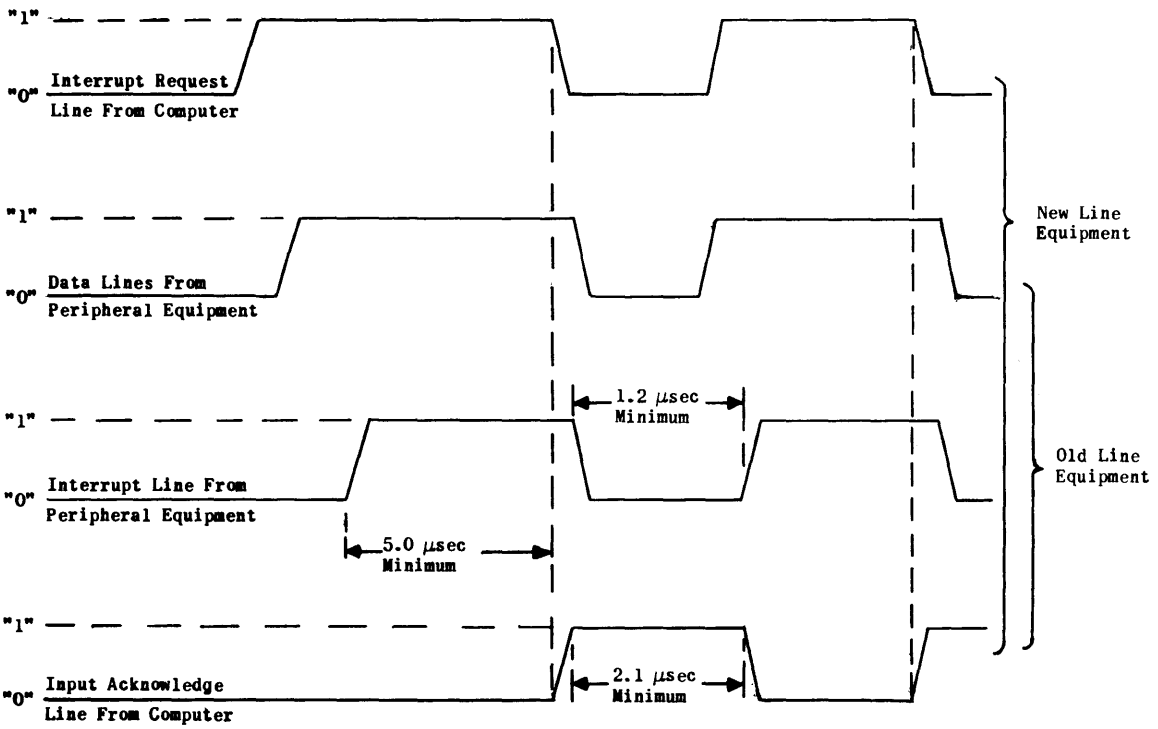
1. INPUT DATA TIMING CONSIDERATIONS

The Input Data Request signal indicates to the computer that data has been placed on the 30 data lines. The Input Data Request must be maintained on the lines until an Input Acknowledge is received. Under emergency conditions, when data loss is of secondary importance, the Input Data Request may be dropped and the Interrupt or another Input Data Request raised a minimum of 10 microseconds later. As shown in Figure 13, there is a 5.0 microsecond minimum delay between the setting of the Input Data Request and its answering Input Acknowledge. There is no maximum limit on the



NOTE: All transition times are 0.4 μsec maximum.

Figure 13. Timing of Input Data Signals - Fast Interface



NOTE: All transition times are 0.4 μsec maximum.

Figure 14. Timing of External Interrupt Signals - Fast Interface

duration of the Input Data Request since its value for any particular cycle is determined by the interaction with the computer program and the other input/output channels. The data lines must remain stable as long as the Input Data Request is set.

The Input Acknowledge indicates to the peripheral equipment that its 30 data lines have been sampled. The Input Acknowledge signal is set for a fixed time interval. The peripheral equipment must be capable of detecting as an Input Acknowledge, a signal which may exist in the stable "one" state for as little as 2.1 microseconds, allowing for a rise time of no greater than 0.4 microseconds. Upon sensing the Input Acknowledge, the Input Data Request may be dropped to the "zero" state anytime, but it must be dropped at least 1.2 microseconds before another Input Data Request can be initiated. It should be noted that the time relationships are such that the peripheral equipment desiring to send data at a maximum rate could legitimately reset the Input Data Request before the previous Input Acknowledge has been dropped to the "zero" state; however, the Input Acknowledge will always be returned to the "zero" state before being reset to the "one" state. This will not affect operation of the cycle since a 5.0 microsecond minimum delay will occur between each Input Acknowledge.

2. EXTERNAL INTERRUPT TIMING CONSIDERATIONS

As previously stated in Section E, there are two methods of controlling the transmission of External Interrupt. The first method, used with existing peripheral equipment, used the Interrupt and Input Acknowledge lines only. The new method uses the Interrupt Request line, Interrupt, and Input Acknowledge lines. New line peripheral equipment may use the Interrupt Request line to sense if their Interrupt will be accepted by the computer. The Interrupt Request line will drop at the same time the Input Acknowledge is sent, but will not be reset until the computer program enables it. Figure 14 shows the timing relationships involved.

3. OUTPUT DATA AND EXTERNAL FUNCTION TIMING CONSIDERATIONS

The peripheral equipment must set the Output Request line or EF Request line indicating that it is in a condition to accept a data or EF word from the computer. There is a 5.0 microsecond minimum delay between the setting of the Output Data Request or EF Request and the placing of data on the line. The maximum time depends upon the computer program, the priority of the particular channel, and the data rates of the other peripheral equipment. Data lines will not necessarily be cleared to the "zero" state before being reset to the "one" state.

The Output Acknowledge or External Function signal indicates to the peripheral equipment that its requested word is now present on the data lines which should now be sampled. As shown in Figure 15, the Output Acknowledge or External Function will be sent a minimum of 0.3 microsecond after the data has been placed on the lines. The peripheral equipment must be capable of recognizing, as an Output Acknowledge or an EF, a signal which may exist in the stable "one" state for as short a time as 2.1 microseconds. The computer will maintain stable data on the lines for a minimum of 3.2 microseconds after it starts to drop the Output Acknowledge or EF. The Output or EF request may be dropped to the "zero" state anytime after detecting the Output Acknowledge or the EF. The Output or EF Request cannot be reset immediately to indicate readiness of the peripheral equipment to accept a second word because the computer will not recognize the second Output or EF Request unless a minimum time delay of 1.2 microseconds is allowed between the start of the dropping of the first Output or EF Request and the start of the setting of the second Output or EF request. Figure 15 shows that the timing would allow peripheral equipment, which wishes to receive data from the computer at a maximum rate, to legitimately set the Output or EF request to the "one" state for the second time before the first Output Acknowledge

or EF has dropped to the "zero" state. However, this will not affect operation of the cycle since a 5.0 microsecond minimum delay will again exist between the setting of the second Output or EF Request and the availability of the second word on the data lines.

4. OUTPUT TIMING CONSIDERATIONS FOR EXTERNAL FUNCTIONS WITH FORCE

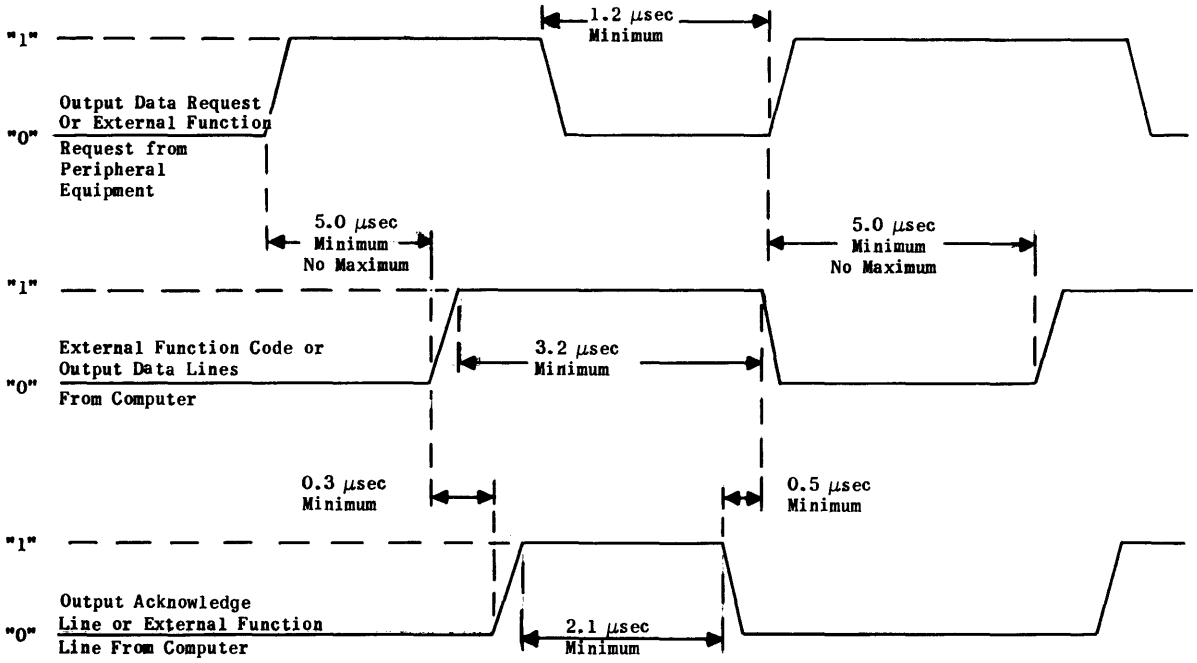
The same considerations apply as in 4 of Section E. Figure 16 shows the timing relationship involved. The computer places the External Function code on the 30 output data lines, and a minimum of 0.3 microseconds later energizes the External Function line. The External Function signal indicates to the peripheral equipment that an EF code is present on the data lines, which should now be sampled. The External Function line will remain in the stable "one" state for an interval which may be as short as 2.1 microseconds. The EF code will remain on the data lines for a minimum of 0.5 microseconds after the External Function signal begins to drop. After each External Function is sent, the line will drop to the "zero" state for an interval which may be as short as 4.7 microseconds.

G. Circuitry Specifications

1. GENERAL

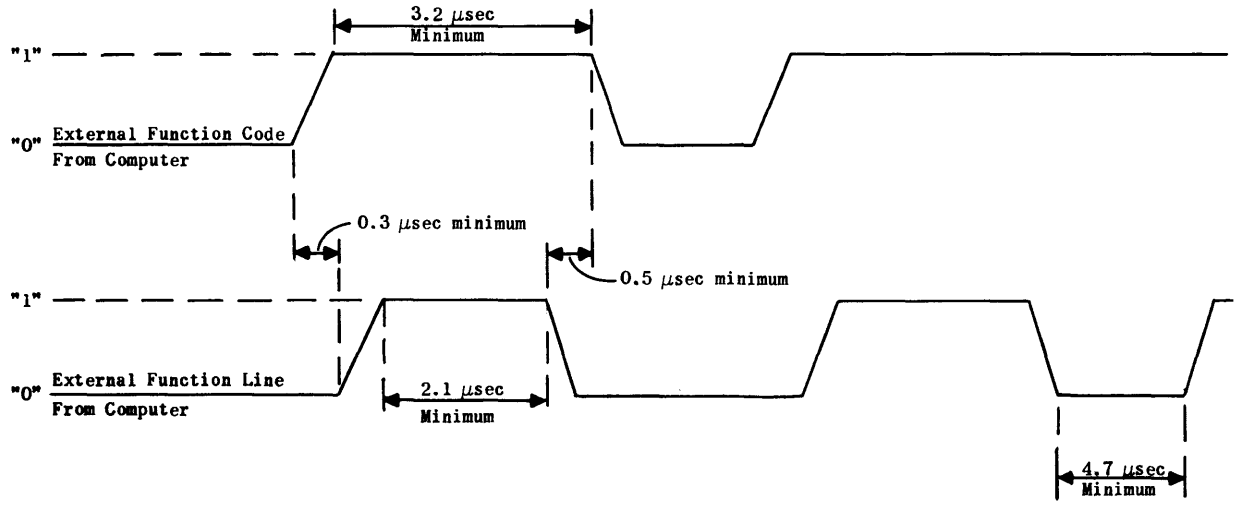
A minimum data transfer time consistent with good engineering practice and moderate hardware requirements is afforded by the CP-642B I/O devices.

The binary "zero" and "one" voltage levels are measured at the output terminals of the computer and the output terminals of peripheral equipment, with the currents specified in the following paragraphs. Rise and fall (transition) times are measured from 10 percent to 90 percent amplitude. The maximum d-c resistance of the ground return for any cable is 0.5 ohm.



NOTE: All transition times are 0.4 μsec maximum.

Figure 15. Timing for Normal Output Signals - Fast Interface



NOTE: All transition times are 0.4 μsec maximum

Figure 16. Timing for External Functions with Force - Fast Interface

For the purposes of this discussion, an output circuit is defined as any circuit in the computer or in the peripheral equipment that applies data or control information to an intercommunication cable. An input circuit is any circuit in the computer or in the peripheral equipment that receives data or control information from an intercommunication cable. Computer output circuits are connected to peripheral equipment input circuits, and computer input circuits are connected to output circuits located in the peripheral equipment.

Because of the rigorous timing restrictions in operating with the "fast" interface, it is strongly recommended that designers of equipment interfacing with this version of the computer use the output circuits and input circuit shown in Figures 17, 18 and 19 respectively. If it is absolutely necessary to design new circuits for these applications, the restrictions of paragraphs 4 and 5 following must be considered by such new circuits.

2. OUTPUT CIRCUITS (Slow Interface)

The binary "one" state of an output amplifier is 0 volt $\pm$ 1.5 volts at the terminals of the equipment under all conditions. The binary "zero" state of an output amplifier is -13.5 volts + 3.5 volts, -4.0 volts at the terminals of the equipment under all conditions. In the binary "one" or "zero" state, an output circuit (located in the computer or peripheral equipment) need supply no more than four milliamperes steady state to any one input circuit in another equipment.

The waveform that any output circuit applies to any line has the following characteristics:

- The transition slope is not greater than five volts per microsecond.
- The maximum transition time is six microseconds.

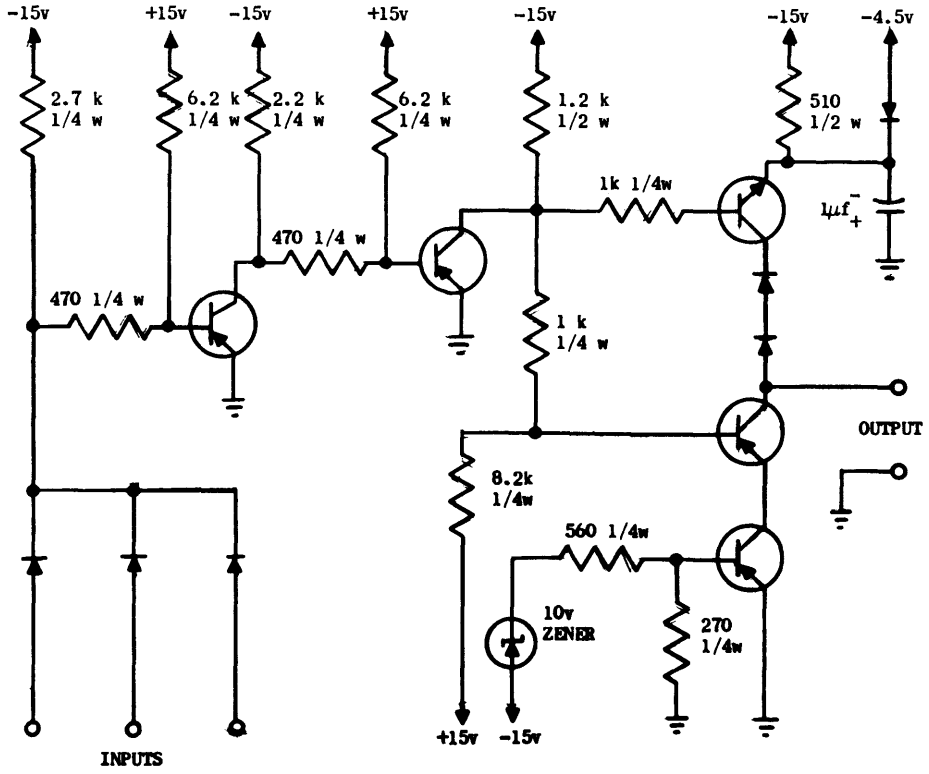


Figure 17. Output Control Line Driver

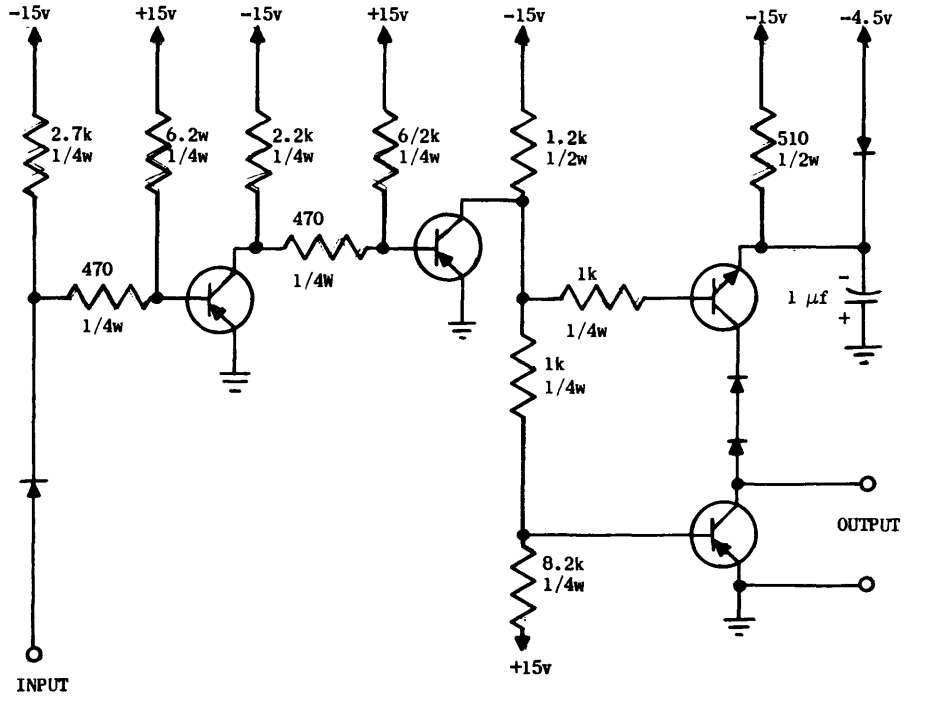


Figure 18. Output Data Line Driver

An output circuit is capable of producing such a waveform when loaded by the capacitance of the cabling separating the output circuit from one or more input circuits. An output circuit used in the computer, in duplexed and non-duplexed peripheral equipment, maintains the waveform under various loading conditions.

The design of output circuits used for control signals provides for an impedance of 100,000 ohms or more to the line when power has been removed, to avoid falsely placing a "one" on the control lines. Data and control signals within the same cable have the same "zero" and "one" levels within 1.0 volt.

3. INPUT CIRCUITS (Slow Interface)

The maximum steady-state current drawn from a line by an input circuit does not exceed four milliamperes. The input circuit is such that if the input wire is disconnected, the effect will be as though a "zero" were present at the input. The threshold level distinguishing the "one" state from the "zero" state is -6 volts $\pm$ 1.5 volt at the input terminals. The input circuit provides an integration delay of 1.5 microseconds $\pm$ 0.5 microsecond to a step function of 15 volts applied to the input. The current drawn from a line by an input circuit during the transition from a "zero" to a "one" or from a "one" to a "zero" will not exceed the steady state value. Phase relations between data signals, and between data and computer Output Acknowledge and Input Data Request signals, are preserved through input circuits connected to the same cable - except as they are affected by the tolerance allowed for integration delay.

4. OUTPUT CIRCUITS (Fast Interface)

The binary "one" state of an output amplifier under all conditions is zero volt to -0.5 volt at the terminals of the equipment. Similarly, the binary "zero" state of an output amplifier is -3.0 to -4.5 volts at the terminals of

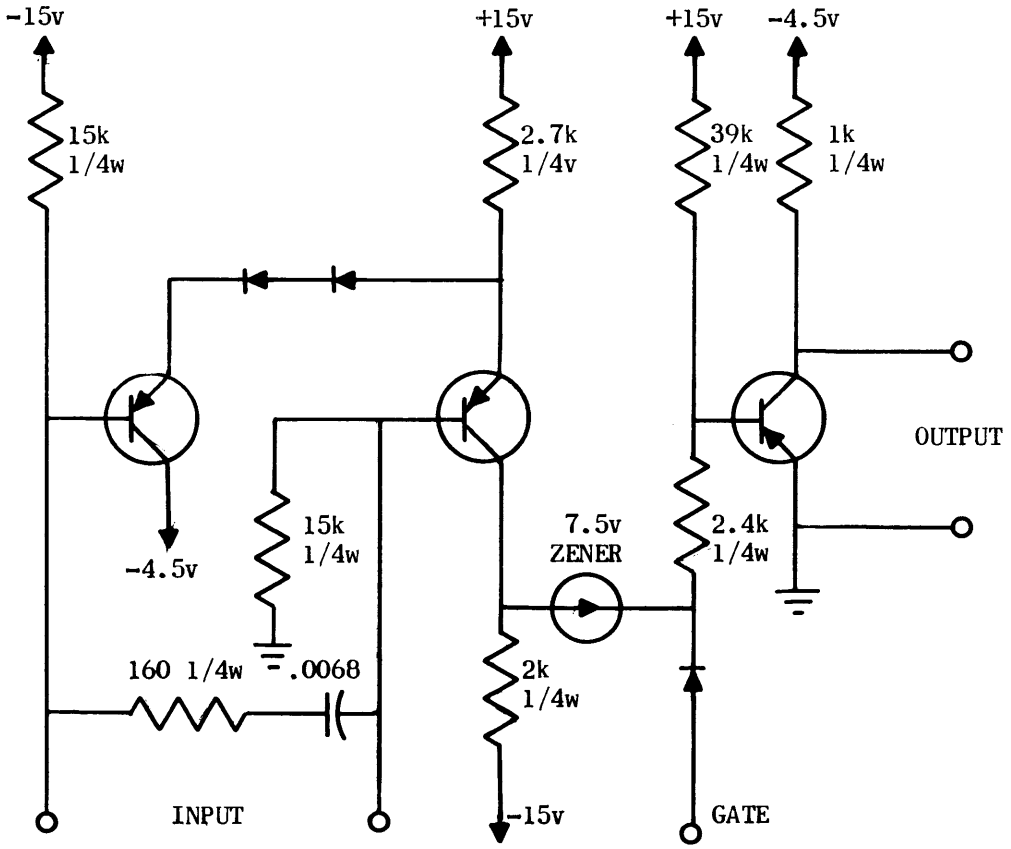


Figure 19. Differential Input Amplifier

the equipment. When the output circuit is in a steady state "one" condition, it is capable of furnishing at least 6.0 milliamperes to the line. When the output is in a steady state "zero" condition, the current drawn from the line is a maximum of 0.3 milliampere.

The total wiring capacity that an output circuit must drive may vary from 0 to 9,000 micro-microfarads if the maximum cable length of 150 feet is used. If less cable is employed, capacity driving requirements may be reduced proportionately.

The output circuits used for control signals are designed so that they present an impedance of 100,000 ohms or more to the line when power has

been removed, to preclude the false placing of a "one" on the control lines. When loaded by a cable and an input circuit the output circuit produces a waveform whose transition time is no greater than 0.4 microsecond. This is predicated on the use of a balanced, twisted-pair, shielded cable of approximately 160 ohms characteristic impedance and no more than 150 feet in length.

5. INPUT CIRCUITS (Fast Interface)

The maximum steady state current drawn from a line by an input circuit will not exceed 1.3 milliampere, when the input is between zero and -0.5 volt. The input circuit is designed so that if the input wire is disconnected, the effect will be as though a "zero" were present at the input. The threshold level distinguishing the "one" state is a voltage level at the input more positive than -1.1 volts. The threshold level distinguishing a "zero" state is a negative level of less than -1.9 volts. The equivalent circuit as seen across the input line appears in Figure 20. The signal must be balanced to ground for noise rejection.

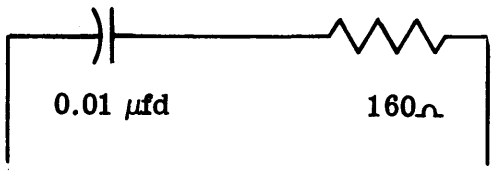


Figure 20. Equivalent Circuit

Phase relationships between data signals and between data and control signals are preserved through input circuits connected to the same cable. The type of input circuit to fulfill these requirements provides for common mode noise rejection.

6. SYSTEM CABLING REQUIREMENTS

The sum of the lengths of all cables connecting an output circuit with an input circuit never exceeds the following limits:

- With the slow interface, the length must not exceed 300 feet of "NTDS-spec" cable (i.e., having a maximum capacitance of 20 mmf per foot between wires of a pair, and between adjacent pairs). If any other cable is used, a maximum length of 150 feet may be used with the slow interface.
- With the fast interface, the length must not exceed 150 feet of "NTDS-spec" cable. If any other cable is used, the maximum length for the fast interface must not exceed 75 feet.

It is recognized that in certain special cases, cables longer than 300 or 150 feet will be required and also that in special cases a very low data transfer rate is necessary. In such instances certain of the considerations outlined above are subject to modification. In any event, however, voltages on the data lines must be stable before data is gated from the lines into the storage elements.

PERIPHERALS AND INTER-COMPUTER CAPABILITY

The CP-642B Computer may be connected simultaneously to a variety of military-qualified or commercial peripheral equipments. These include:

- Teletype Printer Units
- Magnetic Tape Units
- High-Speed Printer Units
- Card Read/Punch Units
- Display and Display Interface Equipment
- Radar and Radar Adaption Interfaces
- Paper Tape Units
- Manual Entry Devices

REPERTOIRE OF INSTRUCTIONS

Since the CP-642B Computer was developed out of the highly successful CP-642A Computer program, in terms of logic, organization, and repertoire, the two machines are quite similar. The CP-642B, however, has a gain factor of two in speed, and of four in total input/output transfer rate.

The CP-642B is a self-modifying, stored program, single-address computer. Although only one reference or address is provided for the execution of an instruction, this reference can be modified automatically during a programmed sequence. Instructions to the computer are 30-bit instruction words that are stored sequentially in the magnetic core memory. The computer executes each instruction sequentially unless an instruction alters the sequence.

Each computer instruction word completely defines a computer operation by means of five designators. The highest-order six bits of an instruction word constitutes the function code designator, f. There are sixty-two function codes each of which corresponds to a machine instruction. The balance of the upper half of the instruction word contains, in the order indicated, the designators j, k. b. The lower half of the word contains the operand designator, y.

The expression $Y = y + (B^b)$ relates to the b- and y-designators. The three bits of b specify (the address of) the B-register whose contents increment y; for b = 0, Y = y. The precise meaning of Y, for a given instruction word depends upon the function code designator and the value of the operand interpretation designator, k.

Normally, the j- and k-designators are three bits each; however, the input-output instructions provide four j-designator bits to specify one of the sixteen channels.

CP-642B REPERTOIRE OF INSTRUCTIONS

FUNCTION CODE	MACHINE INSTRUCTION	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	INSTRUCTION EXECUTION TIME: MICROSECONDS		
			EXECUTION	ABORT	REPEAT
00	Fault Interrupt				
01	RIGHT SHIFT Q	Shift (Q) right by Y	8-12	4	4-8
02	RIGHT SHIFT A	Shift (A) right by Y	8-12	4	4-8
03	RIGHT SHIFT AQ	Shift (AQ) right by Y	8-12	4	4-8
04	COMPARE A, Q, AQ	*Sense j; $(A)_i = (A)_f$	8	4	4
05	LEFT SHIFT Q	Shift	8-12	4	4-8
06	LEFT SHIFT A	Shift (A) left by Y	8-12	4	4-8
07	LEFT SHIFT AQ	Shift (AQ) left by Y	8-12	4	4-8
10	ENTER Q	$Y \rightarrow Q$	8	4	4
11	ENTER A	$Y \rightarrow A$	8	4	4
12	ENTER B^n	$Y \rightarrow B^j$	8	-	-
13	OUTPUT COMMAND ON C^n	Enable Channel j	8	-	-
14	STORE Q	$(Q) \rightarrow Y$	8	4	4
15	STORE A	$(A) \rightarrow Y$	8	4	4
16	STORE B^n	$(B)^j \rightarrow Y$	8	-	4
17	STORE C^n or TEST OCB	$(C)^j \rightarrow Y$	8-12	-	-
20	ADD A	$(A) + Y \rightarrow A$	8	4	4
21	SUBTRACT A	$(A) - Y \rightarrow A$	8	4	4
22	MULTIPLY	$(Q)\ Y \rightarrow AQ$	32-48	4	32-48
23	DIVIDE	$(AQ)\_Y \rightarrow Q$; Remainder A	48	4	48
24	REPLACE A + Y	$(A) + Y \rightarrow Y$ & A	12	0	8
25	REPLACE A - Y	$(A) - Y \rightarrow Y$ & A	12	0	8
26	ADD Q	$(Q) + Y \rightarrow Q$; $A_i = A_f$	8	4	4
27	SUBTRACT Q	$(A) - Y \rightarrow Q$; $A_i = A_f$	8	4	4

FUNCTION CODE	MACHINE INSTRUCTION	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	INSTRUCTION EXECUTION TIME: MICROSECONDS		
			EXECUTION	ABORT	REPEAT
30	ENTER Y + Q	$Y + (Q) \rightarrow A$	8	4	4
31	ENTER Y - Q	$Y - (Q) \rightarrow A$	8	4	4
32	STORE A + Q	$(A) + (Q) \rightarrow Y \& A$	12	0	8
33	STORE A - Q	$(A) - (Q) \rightarrow Y \& A$	12	0	8
34	REPLACE Y + Q	$(Y) + (Q) \rightarrow Y \& A$	12	0	8
35	REPLACE Y - Q	$(Y) - (Q) \rightarrow Y \& A$	12	0	8
36	REPLACE Y + 1	$(Y) + 1 \rightarrow Y \& A$	12	0	8
37	REPLACE Y - 1	$(Y) - 1 \rightarrow Y \& A$	12	0	8
40	ENTER LOGICAL PRODUCT	$L[Y(Q)] \rightarrow A$	8	4	4
41	ADD LOGICAL PRODUCT	$L[Y(Q)] + (A) \rightarrow A$	8	4	4
42	SUBTRACT LOGICAL PRODUCT	$L[Y(Q)] - (A) \rightarrow A$	8	4	4
43	COMPARE MASKED	$(A) - L[Y(Q)]$; sense j; $(A) + L[Y(Q)]$; $A_i = A_f$	8	4	4
44	REPLACE LOGICAL PRODUCT	$L[(Y)(Q)] \rightarrow Y \& A$	12	0	8
45	REPLACE A + LP	$L[(Y)(Q)] + (A) \rightarrow Y \& A$	12	0	8
46	REPLACE A - LP	$(A) = L[(Y)(Q)] \rightarrow Y \& A$	12	0	8
47	STORE LOGICAL PRODUCT	$L[(A)(Q)] \rightarrow Y$; $(A)_j = (A)_f$	8	4	4
50	SELECTIVE SET	Set $(A)_n$ for $Y_n = 1$	8	4	4
51	SELECTIVE COMPLEMENT	Complement $(A)_n$ for $Y_n = 1$			
52	SELECTIVE CLEAR	Clear $(A)_n$ for $Y_n = 1$	8	4	4
53	SELECTIVE SUBSTITUTE	$Y_n \rightarrow A_n$ for $(Q)_n = 1$	8	4	4
54	REPLACE SELECTIVE SET	Set $(A)_n$ for $Y_n = 1$; Y & A	12	0	8
55	REPLACE SELECTIVE COMPLEMENT	Complement $(A)_n$ for $Y_n = 1$; Y & A	12	0	8
56	REPLACE SELECTIVE CLEAR	Clear $(A)_n$ for $Y_n = 1$; Y & A	12	0	8

FUNCTION CODE	MACHINE INSTRUCTION	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	INSTRUCTION EXECUTION TIME: MICROSECONDS		
			EXECUTION	ABORT	REPEAT
57	REPLACE SELECTIVE SUBSTITUTE	$(Y)_n(A)_n$ for $(Q)_n = 1$; Y & A	12	0	8
60	JUMP (ARITHMETIC)	Jump to Y per special Interpretation of j	8	-	-
61	JUMP (MANUAL)		8	-	-
62	JUMP ON C^n ACTIVE INPUT BUFFER	Jump to Y if channel j has active Input/Output buffer	8	-	-
63	JUMP ON C^n ACTIVE OUTPUT BUFFER		8	-	-
64	RETURN JUMP (ARITHMETIC)	Store address of next (or current) inst. in Y_L and jump to Y + 1 per special interpretation of j	12	-	-
65	RETURN JUMP (MANUAL)				
66	TERMINATE C^n INPUT BUFFER OR ENABLE, DISABLE INTERRUPTS	Terminate input/output buffer on channel j	4	-	-
67	TERMINATE C^n OUTPUT BUFFER ON ALL BUFFERS				
70	REPEAT	Execute next inst. Y times	8	-	-
71	BSKIP ON B^n	$(B^j) = Y$, skip next instruction and clear B^j $(B^j) \neq Y$, advance B^j and execute next instruction	8	0	-
72	B JUMP ON B^n	$(B^j) = 0$, execute next instruction $(B^j) \neq 0$, decrease B^j and jump to Y	8	-	-
73	INPUT BUFFER ON C^n (without monitor)	Initiate input buffer without monitor on channel j	8	-	-
74	OUTPUT BUFFER ON C^n (without monitor)	Initiates output buffer without monitor on channel j	8	-	-
75	INPUT BUFFER ON C^n (with monitor)	Initiate input buffer with monitor on channel j	8	-	-
76	OUTPUT BUFFER ON C^n (with monitor)	Initiate output buffer with monitor on channel j	8	-	-
77	FAULT INTERRUPT				