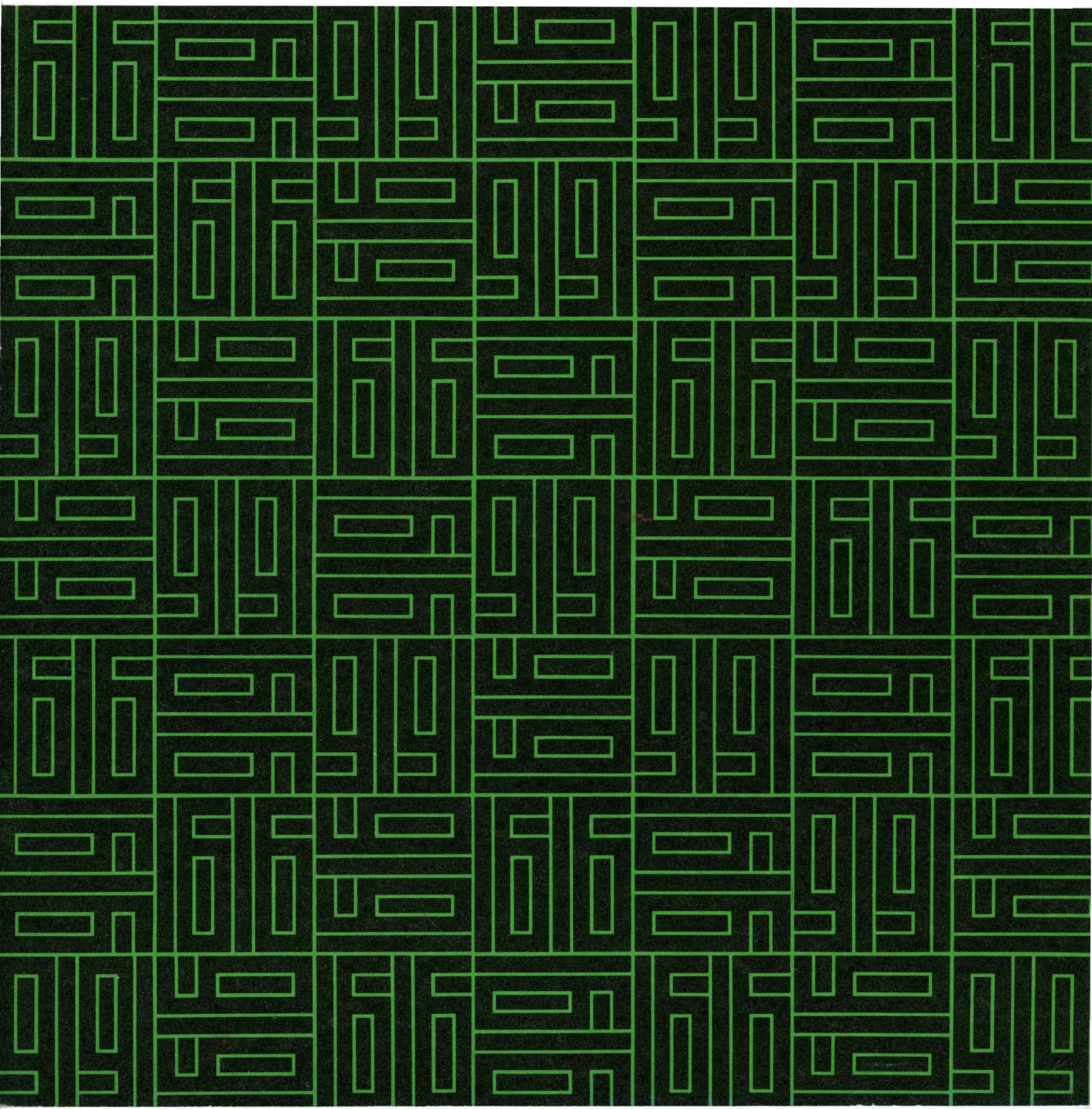
SPERRY RAND

i/o description UNIVAC 1616



SPECIFICATIONS

SUMMARY

Characteristics
General-purpose, 16-bit digital computer
Real-time capability
Physically and functionally modular and expandable
MSI (medium scale integration) elements
Integral cooling blowers and power supplies

Environment
Industrial
Militarized – MIL-E-16400 (Ship-Shore)

CENTRAL PROCESSOR

Standard Features
Two's complement arithmetic
8-bit byte, 16-bit and 32-bit operands
16 high-speed general purpose registers
Program status register
Single bus functional interface
Direct addressing capability to 65K words or 131K bytes
4 Level interrupt processing (hardware serviced)
16-bit and 32-bit instructions – in any mix
Basic instructions – 4 formats

Add	750 nanoseconds
Multiply	4.15 microseconds
Divide	4.15 microseconds

Indexing via general registers
Load and store multiple registers
Processor – peripheral channel
    Up to 16 control units
    Up to 16 external devices/per control unit

Optional Features
Up to 4 sets of 16 general registers
Real-time clock and breakpoint registers (with related instructions)
Status register No. 2
Instructions
    Square Root
    Reverse register
    Scale factor shift
    Count ones
    Set, clear and test bit
Memory protection via lock and key (lockout)
Processor – memory parity checking
Memory interface with separate address, read data and write data lines
NDRO memory (192 words)
Built in Confidence test and initial load program
Up to 4 processor-peripheral channels
Processor-peripheral channel parity checking
Up to 4 separate input/output controllers (16 channels each)

MAIN STORAGE

Standard Features
Expandable – 4K to 65K words in 4K increments
16-bit words
Independently accessible memory banks
Read/restore cycle time – 750 nanoseconds is optimal
Asynchronous timing – request and acknowledge signals

Optional Features
Optional memory types – core, plated wire, film, etc.
Parity
Priority multiplexer – multi-port option

INPUT-OUTPUT CONTROLLER (1 to 4 OPTIONAL)

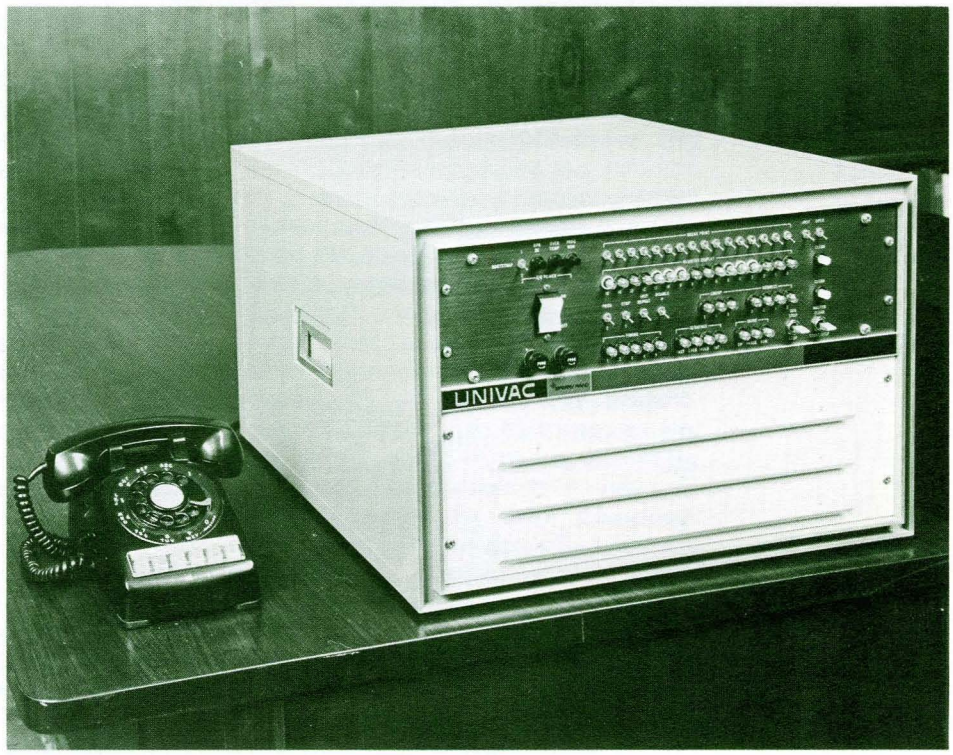
Sync/asynchronous Operation (Serial Transfers)
Asynchronous Operation (Parallel Transfers)
Processor initiated program chain
10 instructions, format same as for CP
IC buffer control memory (64 words)
4 input and output channel groups (1 to 4 groups)
Parallel 16-bit channel interface
    8 bit byte, 16-bit word or 32-bit dual-channel transfer
Interface voltage levels - 4 channel groups
Power supplied by Central Processor (100 watts maximum)
Data parity checking – optional

POWER SUPPLY

CP and IOC
115V, 1 phase, 47 Hz to 500 Hz input
Regulated dc output to CP and IOC

Memory
115V $\pm$ 10V, 1 phase, 60 Hz $\pm$ 2 Hz input
Regulated dc outputs to memory

Optional Features
Power loss protection
    Power fault interrupt to CP
    Automatic master clear
    Automatic restart



Fast processing speeds and short memory cycle times are common features of today's computers. Few, however, have the input/output capability to interface with the wide mix and quantity of peripheral equipment normally found in complex computer systems – or to effect data transfers efficiently at low software overhead and at rates which utilize their processing powers to maximum advantage.

The UNIVAC® 1616 is different. Designed by the Univac Division of Sperry Rand Corporation to meet and satisfy a wide variety of system control and communication applications. Its logic architecture, modular construction and choice of envrionmental enclosures allow it to be configured and adapted to serve wherever computational loads are heavy and fast data throughput and accurate data handling and manipulation is required.

The information presented in this brochure is designed to acquaint you with the full range of the UNIVAC 1616's input/output capabilities. Use it to evaluate the 1616 against your intended application – check our specifications closely, then make your decision.

We feel that you will agree with us that the UNIVAC 1616 offers you one of the most adaptable and efficient computers available today – in any size – anywhere – and at any price.

GENERAL INPUT/OUTPUT CHARACTERISTICS

Input/output (I/O) options provide the means for tailoring the UNIVAC 1616 to serve a wide variety of real-time data processing applications. The computer is designed to handle two distinct types of communication transfers: programmed I/O and buffered I/O, Programmed I/O transfers are accomplished via 8-bit bit-parallel words; a separate program instruction is required for each datum transfer. In contrast, buffered I/O transfers are accomplished via either bit-serial or bit-parallel 16-bit words. This mode permits performing one or more sequential datum transfers wherein there is no program involvement after the input/output operation is initiated. For example, execution of code 35 by the processor is all that's needed to initiate high-speed input or output buffered transfers. An additional feature, command chaining, permits a number of sequential bufferes to be executed with no direct command involvement by the computer during the buffering process. This means that once the buffers have been prepared and initiated, the central processor is free to concentrate on other tasks and software overhead is minimized.

Figure 1 illustrates the relation of the computer to the external devices with which it communicates. Communications are referenced to the computer. "Input" refers to those signals transmitted to the computer and "output" identifies those signals transferred from the computer to the external devices.

The term "external devices" refers to all types of peripheral equipment used in computer systems. These may be the conventional machine-operator or slow speed peripherals such as typewriters, keyboards, printers, punched card units, and magnetic storage devices such as tapes, disc, and drums, etc. Other external devices are those that either provide continuous information in real-time or require continually up-dated information or control commands in order to function properly – such as in the case of sensor-based systems or data acquisition and control systems. In these systems, the computer might be processing raw radar video received from the radar antenna while simultaneously issuing commands to the antenna control section in order to maintain proper tracking of the target.

COMPUTER ARCHITECTURE

The UNIVAC 1616 computer architecture is organized around a common data bus. All transfers of data between the various functional sections are accomplished via the bus. This design approach gives great flexibility to the UNIVAC 1616 and enables it to be easily configured to handle your particular application – whether it be signal processing, data acquisition, command and control, process control, message switching, programmable communications front-ends to large data processing machines, or any of the other numerous functions associated with today's data processing systems.

The basic UNIVAC 1616 computer consists of the central processor, its associated optional capabilities and one 8K memory bank. These are identified in black in Figure 2. The basic input/output and optional memory functions are identified in color.

Memory Interface

Programmed I/O transfer functions are performed by the processor-peripheral channel (P/P Channel). Since programmed I/O functions are normally accomplished at relatively low rates and are under direct control of the central processor, all references to memory are accomplished under the processor's control. The situation is different, however, for buffered I/O functions which are

performed by the input/output (I/O) and/or the communications oriented (CO) controllers. Since they are often called upon to perform block data transfers in high-speed real-time, they have need for direct access to memory for storing and/or retrieving data without interruption. This ability is provided by the memory interface section. Located functionally within the central processor, the memory interface enables the controller to share memory time with the central processor. The interface priority scheme is such that priority is always given the controller whenever it and the central processor request memory access simultaneously.

Memory may be expanded in 8K increments to a total capacity of 65K 16-bit words. Multiple memory banks not only increase the storage capacity but also increase the processor's efficiency and overall processing operating speed by making possible memory overlapping, thus eliminating processing degradation due to memory contention. This is accomplished by adding a memory interface to the controller and a priority multiplexer to each memory bank as shown in Figure 3. Now, any waiting for memory is eliminated since the controller can work with one or more memory banks while the central processor is working with the others. In cases of simultaneous requests to the same memory bank, the priority multiplexer honors the user of the higher priority port first, which as stated before for this case, would be the controller.

Additional controllers can be added for expanding the UNIVAC 1616 to its full input/output capacity. Memory priorities are determined by the order in which the additional controllers are connected to the ports in the priority multiplexers serving the individual memory banks.

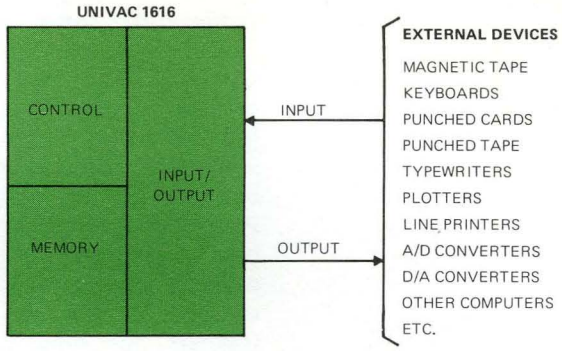


Figure 1. Computer to External Devices Relationship

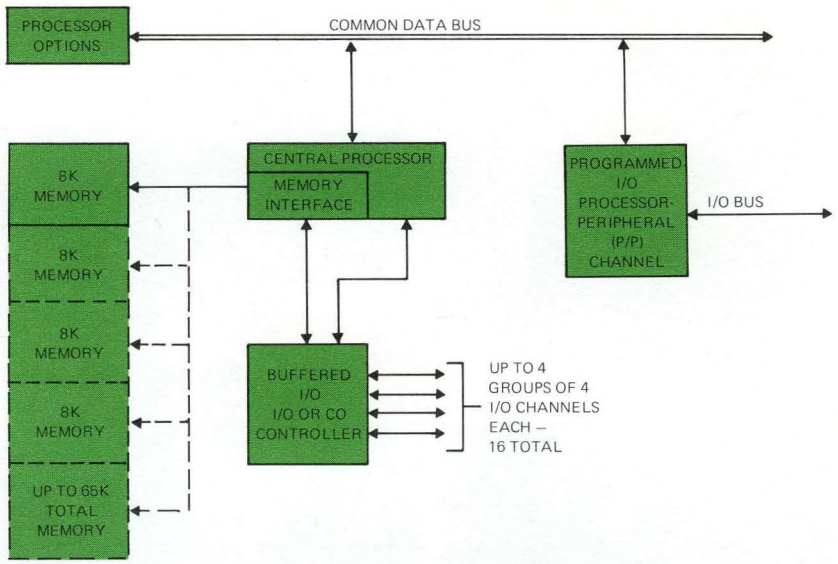


Figure 2. Basic Functional Diagram

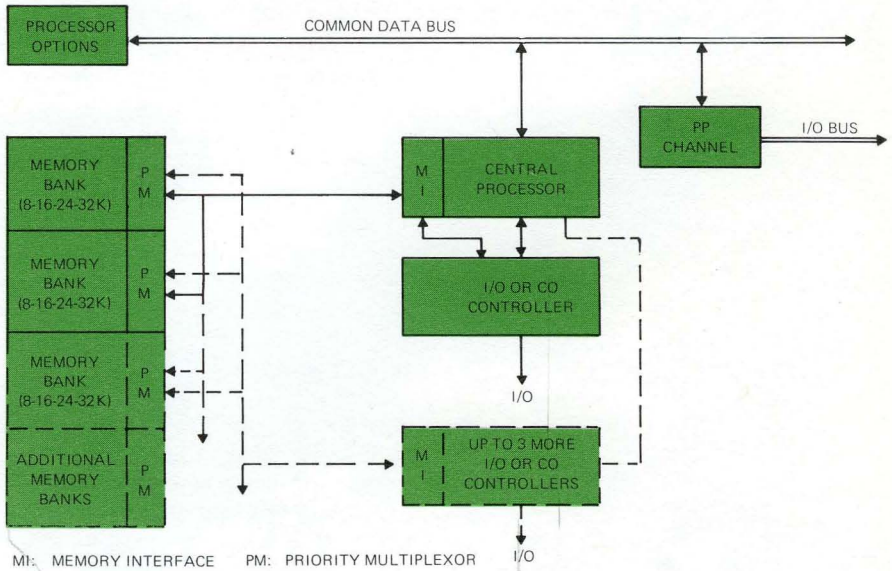


Figure 3. Multi-Controller, Multi-Port Memory Configuration

Buffered I/O Control

Communications to external devices operating in real-time utilize the buffered I/O capabilities of the computer. Maximum word transfer rates possible with buffered I/O are shown in Table 1. Parameters defining the rates are: the type of controller, the number of controller channels, the interface signal voltage levels, and in the case of bit-serial transfers, the input/output clock rate selected for the channel.

The central processor exerts primary control of all buffered I/O operations; however, by using chain commands stored in main memory, a controller may operate independently of the central processor once an input or output datum transfer chain has been initiated. Chain commands not only direct the transfer sequence but they also provide a means of monitoring the end of a buffer sequence, thus giving the programmer a means of checking for certain conditions occurring within a data transfer.

Buffered I/O bit-parallel communications may use 8, 16, or 32-bit word formats; double length 32-bit words are transferred via the dual channel mode wherein two parallel I/O channels (n & n+4) are used. When operating in the dual channel mode, channel n controls the double length transfers; the channel n+4 control is disabled. Bit-serial transfers occur via 16-bit words wherein data are sequenced over a single coaxial cable in the order of bit position zero (0) through fifteen (15).

A maximum of four controllers of any combination can be used with the computer. Controllers can handle up to four groups of four channels each (4, 8, 12, or 16 channels per controller). Each group must be equipped to handle the same type of signal voltage levels and transfer mode (serial or parallel). In addition, each group must be selected for communicating either with peripheral equipment only, or with another computer.

Each channel group contains an input and an output buffer register for temporary storage of information during datum transfers. Peripheral devices used with the UNIVAC 1616 must have similar buffer registers for holding information on the input lines to the computer until the controller can service the channel. In addition, they must contain the proper interface logic for interpreting the commands and information received from the computer and for assembling, in the proper format, all data and corresponding communication codes intended for transfer to the computer.

Programmed I/O Control

Programmed I/O data transfers are accomplished via 8-bit bytes; 8-bit, parallel words are always used, although some data transfers may not make use of all eight bits. The byte-oriented interface is a relatively low performance type interface when compared to the buffered IOC interfaces. However, the capability expands the versatility of the UNIVAC 1616 by providing the means to communicate, via one 8-bit parallel channel interface, with up to a maximum of sixteen peripheral control units. The control units provide the signal recognition, data manipulation, formatting and transmission services necessary for adapting the external devices to the channel interface. Each control unit can service up to sixteen low performance external devices. Thus a theoretical maximum of 256 external devices such as typewriters could be connected to the channel. High performance devices may be used providing they are limited in number so as not to degrade the processor's computational capabilities.

Byte transfers are normally initiated via the channel polling process whereby each of the attached control units is periodically polled in a predetermined order of priority. Providing no unit of higher priority captures the channel first, the selected control unit, when polled, will capture the channel and the transfer process will start. This polling process precedes each transfer of information, including those occurring when transferring blocks of data to external devices such as disc or magnetic tape units. To prevent the control unit from losing the channel to a higher priority control unit during the polling intervals occurring within the block transfer sequences, a burst mode operation is provided which enables the control unit to hold the channel until the block transfer is completed, at which time control is relinquished to the channel.

PROGRAM PRIORITIES

Real-time data processing requires that the processing functions be identified in order of their importance within the system. All programmed I/O input status transfers are initiated via program interrupts which require the processor to interrupt its current operation and turn its attention to directing the datum transfer.

Buffered I/O data transfers operate with a minimum of program intervention. In any event, whenever either internal or external events warrant an intervention of the current program in progress, an interrupt will be issued to the central processor. Program control is then transferred to the stored interrupt routine corresponding to the event that caused the operation.

The UNIVAC 1616 interrupt priority is shown in Table 2. Once an interrupt has been issued, the computer stores its status and the data it was manipulating and turns to the proper interrupt routine. These routines are located in assigned memory locations and direct the central processor in the proper manner for handling the particular type of interrupt condition which initiated the interrupt notice. This routine may be interrupted by a higher-order interrupt should it occur. In all cases, the computer selects the branch of operation for solving the problem requiring the most urgent attention. Program control options allow selecting which interrupts will be honored and which may be ignored. After the interrupt routine has been completed, control is returned to the program which was interrupted and it resumes operation from the point of interruption.

TABLE 1. BUFFERED I/O TRANSFER RATES

Controller Type	Interface & Voltage Type	Spec. (Univac)	Number of Channels* Transfer Rates in K Words/Sec.				
			1	2-4	5-8	9-12	13-16
I/OC	-15V (NTDS)	DS4772	41.6	41.6	83.3	124.4	166.6
I/OC	-3V (NTDS) and 3.5V (ANEW)	DS4772	190.0	250.0	500.0	750.0	1000.0
I/OC	-3V (1108A)	SA00600	667.0	1300.0	1300.0	1300.0	1300.0
COC (Bit-Parallel) Channels	-15V (NTDS)	DS4772	41.6	41.6	83.3	–	–
COC (Bit-Serial) Channels	MIL-STD-188C or RS.232C		Data rates available: 75 to 9600 bits per second.				

*NOTE: The specified transfer rates shown for the I/OC and COC bit-parallel I/O channels are the maximum for the specified number of active input channels or output channels. The combined transfer rates (both input and output active) are twice the rates specified but not greater than 1,300 K words/second.

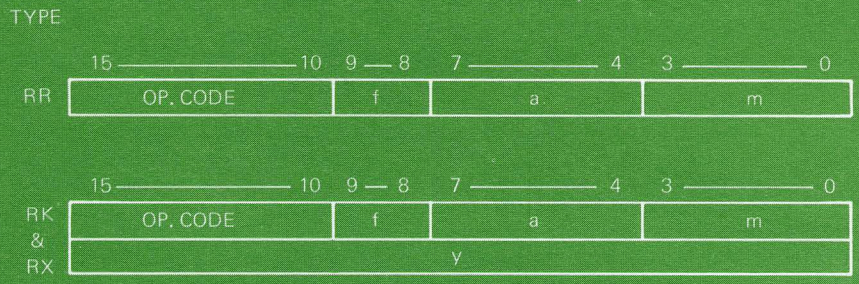
TABLE 2. INTERRUPT PRIORITY

Class	Priority Within Class	Interrupt	Binary Interrupt Code Generated
Class I Hardware Errors	1	Power Fault	000
	2	CP Memory Resume Error	001
	3	CO Parity Error*	010
Class II, Software Interrupts	1	CP Instruction Fault	000
	2	Privileged Instruction Error	001
	3	Memory Lock and Key Error*	010
	4	Executive Call	011
	5	RTC Overflow*	100
	6	Interrupt Clock*	
Class III, I/OC Interrupts	1	External Interrupt	000
	2	Chain	001
Class IV, Proc./Periph. Interrupts	1	Status In Request	000

*Optional

TABLE 3. INSTRUCTION REPERTOIRE

Operation Code and Format	Instruction and Type		Execution Time (Memory Cycles)
	Command	Chaining	
70 RR	Channel Control	Channel Control	1
70 RX	N/A	Initiate Transfer	4
71 RK	Initiate Chain	Load Control Memory	2
71 RX	Load Control Memory	Load Control Memory	3
72 RX	Store Control Memory	Store Control Memory	3
73 RR	N/A	Halt/Interrupt	1
73 RX	N/A	Set/Clear Flag	3



DEFINITION OF FIELDS:

OP. CODE	Code specifying the operation
f:	Format Designator
f = 00	Format RR Register - Register
f = 01	Format RI Register - Intermediate Memory
f = 10	Format RK Register - Literal Constant
f = 11	Format RX Register - Indexed Address or Constant
a:	General Register or Subfunction Designator
m:	General Register or Subfunction Designator
y:	Address or Arithmetic Constant

Figure 4. Instruction Word Formats

15	14	13	12	11 — 0	LOCATION
TM		*	B	BUFFER WORD COUNT	0
BUFFER ADDRESS POINTER					1
CHAIN ADDRESS POINTER					2
UNASSIGNED					3

*UNUSED

Figure 5. Control Memory Locations For One Channel

BUFFERED I/O OPERATION

Buffered I/O channels are used for transferring control commands and data between external devices and memory with no program involvement on the part of the central processor after the transfer has been initiated.

I/O Instructions

Buffered I/O operations are initiated upon execution of a code 35 RR instruction by the central processor. Prior to this, however, the central processor will have loaded pre-assigned locations in memory with the proper data as well as with the appropriate chain instruction for carrying out the I/O operation. Table 3 identifies the special I/O instructions which are recognized by the I/O and CO controllers. Figure 4 defines the instruction word formats.

Control Memory

Buffer control resides within the controller's control memory which has, for each of its sixteen channels, reserved in its memory four memory locations dedicated for storing:

Location 1. The buffer function word
Location 2. The buffer address pointer
Location 3. The chain address pointer
Location 4. Unassigned.

The control memory locations for one channel are illustrated in Figure 5.

The buffer control word (BCW) is stored in location 0. The bit fields within the sixteen bit word provide the primary control information necessary for directing the controller during the I/O buffer operation:

- B (Byte Pointer): The byte pointer (recognized when performing 8-bit (byte transfers) specifies which byte of the memory location specified by the BCW shall be used for the next transfer. After each byte transfer the condition of the byte pointer bit changes state.
- TM (Transfer Mode): This 2-bit field specifies the I/O channel word length for external function, input data and output data transfers.

- Buffer Word Count: This field specifies the number of single length words to be transferred during the selected input data, output data or output external function operations. The buffer word count is decreased by one for each word count. The maximum number of transfers in any one buffer is 4096.

The buffer address pointer is stored in location 1 and specifies the memory address for the next input data, output data or output external function transfer. The contents are increased by one whenever the byte pointer bit changes from 1 to 0. For each 16-bit word transferred, the contents are increased by one.

The chain address pointer is stored in location 2 and specifies the address of the next chaining instruction to be executed for that channel. When a chaining instruction is obtained from memory, the controller increases the chain address pointer by one for single length instructions and by two for double length instructions. When the operations required for the current chaining instruction are completed, the controller automatically retrieves the next chaining instruction from the memory location indicated by the up-dated chain address pointer. The controller then interprets the instruction and performs the operation indicated.

The controller performs channel related functions according to channel priority first and function priority second. The order of priority is channel zero (0) lowest and channel 15 highest. Controller functions are assigned priority as follows:

- Command instructions in response to request of the central processor (not channel related).
- External interrupt input (channel related).
- Input data, output data, output external function or chaining instruction depending on established activity of the chain for a channel.

I/O Interface

Bit-parallel communications between the I/O and CO Controllers and external equipment are carried on in a parallel mode over the input/output channels (Figure 6). Bit-serial transfers are made via a single coaxial cable.

Input Channels

The input channels carry both data and external interrupt information from external equipment to the computer. Input data information transfers are controlled by buffer control words in the controller's control memory. External interrupt information originates at the external equipment and usually informs the computer of a necessary real-time transfer or of an abnormal condition such as tape breakage or incorrect parity.

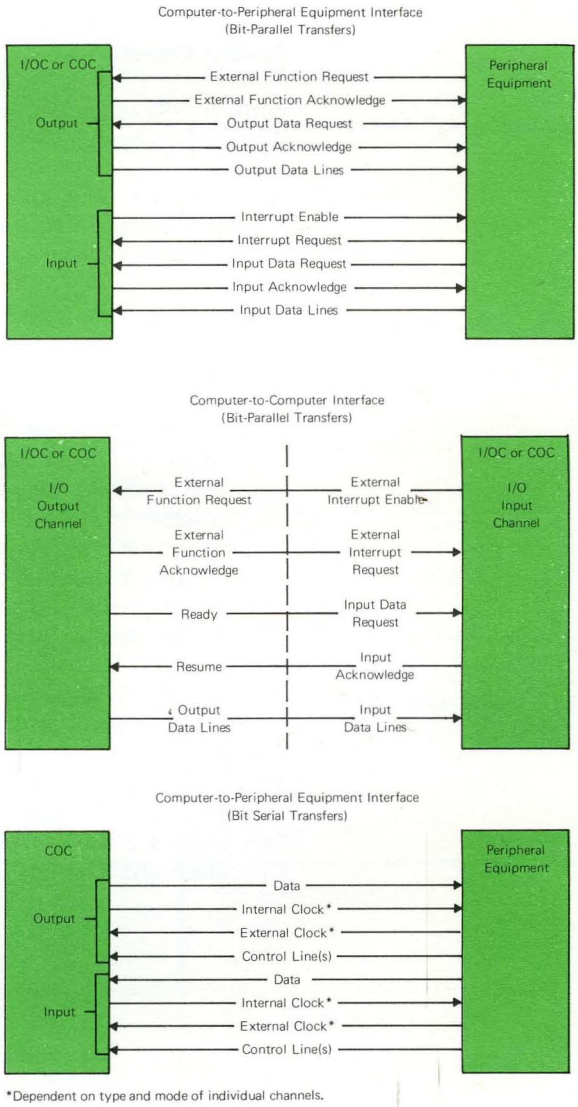


Figure 6. Buffered I/O Interface Structures

Output Channels

The output channels are used to transmit data, and external function code and commands from the computer to external equipment. Both types of transfers are controlled by buffer control words stored in control memory. External functions, transmitted through the data lines, are used for external equipment control such as turn off reader, rewind tape, or turn on typewriter. Only one output mode, output buffer or external function buffer, can be active at one time. Initiating an output buffer will cancel any external function buffer on the same channel, and initiating an external function mode will cancel any active output buffer on the same channel.

Transfer Operation

Buffered I/O operations are initiated by the central processor's executive program. Each time the executive program is called upon to initiate an input or output buffer it must command the controller to execute a chain of instructions that:

- Activates the selected channel and defines the buffer area in main memory.
- Commands the external device connected to the channel to perform the operations required for accomplishing the specified type of transfer.
- Stops the chain (terminate chaining action) and/or interrupts the processor upon completion of the buffer (buffer monitor interrupt).

For example, to illustrate the interaction between the central processor, controller and memory during a buffered I/O operation, assume that a buffer output data transfer is to be initiated via the controller's channel 2. Refer to Figure 7 during the following discussion.

Prior to initiating any transfer action, the processor's executive program must first place the current commands, chain instructions and data in the proper locations in memory. Four memory locations, referred to as command cells, are assigned in memory for each of the possible four controllers. The command cell addresses hold the first instruction which the controller will execute when initiating a data transfer.

As shown in Figure 7, the memory addresses of the command cell for controller 0 in this example, are 140 through 143. The executive program loads cell locations 140 and 141 with the double-length Initiate Chain instruction (code 71 RK, a=2, m=0). The a designator of the first word (location 140) specifies channel 2; the contents of y (in location 141) is the chain address pointer and it specifies the address of the first instruction (in main memory) of the program chain for channel 2.

For this example, assume that the program chain contains the following instructions:

```
y:   70 RX a=2 (EF)
y+1: BW 10  1 word
y+2: EF word address
y+3: 70 RX a=0 (Input data)
y+4: 0 W 01  50 words (80 bytes)
y+5: Input word address
y+6: 73 RR a=1 (Interrupt)
y+7: 73 RR a=0 (Terminate chain)
```

To initiate the buffer transfer, the processor's executive program issues a code 35 instruction which specifies controller 0 and sets its command line.

- Controller 0 reads its command cell in memory. The stored double length code 71 RK instruction (Initiate Chain) specifies the controller's input/output channel (2 - specified by the a designator) and the chain address pointer, y.
- Controller transfers the chain address pointer y to the channel 2 control memory location 2 and activates the chain for channel 2.
- The controller reads the instruction from location y (code 70 RX, Initiate Transfer, double length). The contents of y+1 and y+2 are transferred to the controller's

memory locations 0 and 1 which are assigned for channel 0. Location 0 contains the buffer control word and location 1 specifies the memory address of the first buffer word (this will be an external function word). When the contents of y+1 and y+2 have been transferred to control memory, the channel 2 external function buffer (a=2) is activated. At this time, the chain address pointer will have been advanced by three (3).

- Channel 2 is now ready to perform the first transfer when enabled by the priority scan circuits. When priority is granted, the buffer transfers the first 16-bit word from the external function address specified by the buffer address pointer.
- When the word is transferred, the chain pointer (having been advanced by three, addresses y+3 which specifies input data. The instruction in y+3 instructs the controller to transfer the contents of y+4 and y+5 to the control memory locations 0 and 1 respectively and activates the data input buffer on channel 2. (Location 0, the buffer control word, specifies the transfer mode, whether byte transfer, and the word count.
- The chain stops until all input words are transferred. Since byte transfers were initially indicated, the B-bit in location 0 is toggled and the word count is decreased by one each time B changes from 1 to 0. When the word count reaches zero, the buffer terminates.
- When the buffer terminates, the channel 2 chain is reactivated and the controller reads out the instruction from y+6 (Instruction Halt/ Interrupt 73 RR, a=1). Since a=1, the controller sends an Interrupt to the processor stating, in this case, that the buffer has been completed.
- The controller then reads instruction code 73 RR, a=0, from location y+7. Since a=0, the controller terminates the chain.

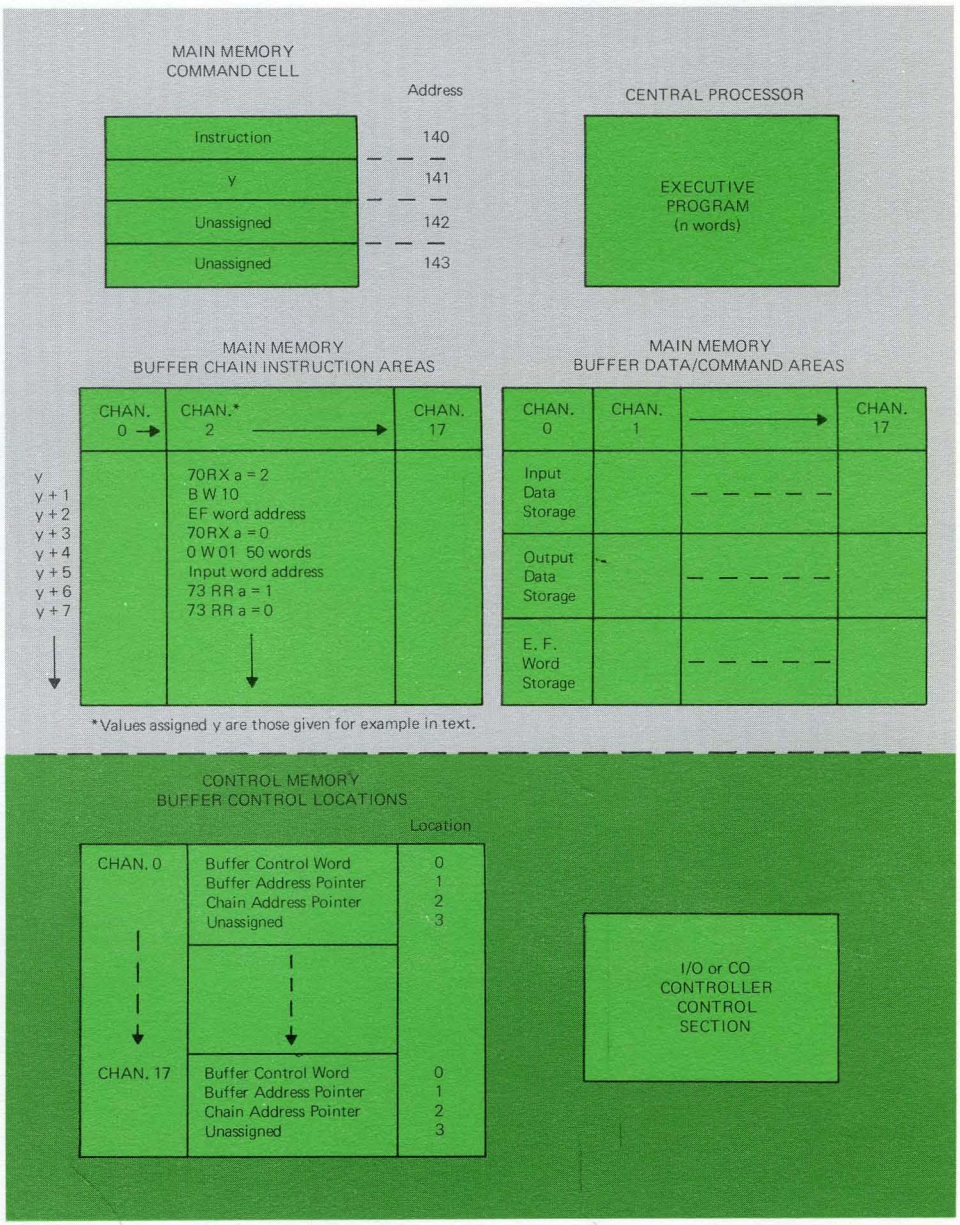


Figure 7. Main Memory and Control Memory Storage Areas

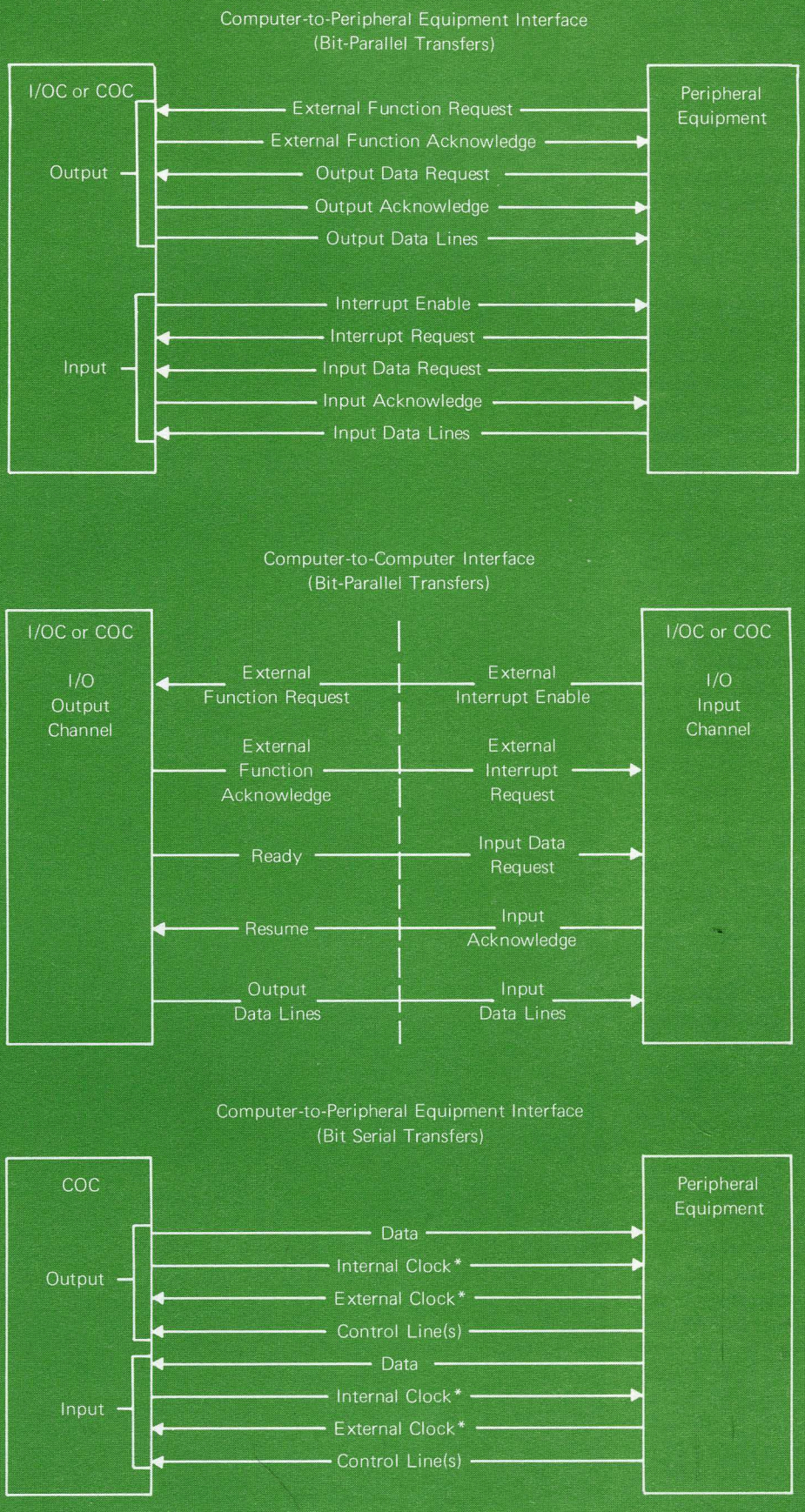


Figure 6. Buffered I/O Interface Structures

Computer to Peripheral I/O Sequences

The sequence of events for the two cases of bit parallel communication between the computer and peripheral equipment is given below. The order of steps a. and b. may be interchanged when an input/output or external function buffer is initiated.

Data Input

Normal input sequence for data transfer to the computer with peripheral equipment is as follows:

a. Controller initiates input data buffer for given channel;
b. Peripheral equipment places a word of data on the Input Data lines;
c. Peripheral equipment sets the Input Data Request line to indicate that a word of data is on the Input Data lines;
d. Controller detects the setting of the Input Data Request line;
e. In accordance with internal priorities, the controller reads the data word which is on the Input Data lines;
f. Controller sets the Input Acknowledge line indicating that it has read the data word on the Input Data lines;
g. Peripheral equipment detects the setting of the Input Acknowledge line;
h. The peripheral equipment may clear the Input Data Request line any time after detecting the setting of the Input Acknowledge line, but it must clear the Input Data Request before the controller will recognize the next Input Data Request;
i. Controller clears the Input Acknowledge line before it reads the next word on the Input Data lines.

Steps b. through i. of this sequence are repeated for every data word until the number of words specified in the input buffer have been transferred.

Figure 6 also indicates similar sequences for External Function and Interrupt transfers.

Data Output

A normal output sequence for data transfer from computer-to-peripheral equipment (buffer mode) is as follows:

a. Controller initiates output data buffer for given channel;
b. Peripheral equipment sets the Output Data Request line when it is in a condition to accept data;
c. Controller detects the setting of the Output Data Request line;
d. In accordance with internal priorities, the controller places a word of data on the Output Data lines;
e. Controller sets the Output Acknowledge line to indicate that a word of data is on the Output Data lines;
f. Peripheral equipment detects the setting of the Output Acknowledge line;
g. Peripheral equipment may clear the Output Data Request line any time after detecting the setting of the Output Acknowledge line but it must clear the Output Data Request line before the controller will recognize the next Output Data Request;
h. Peripheral equipment reads the data word which is on the Output Data lines;
i. Controller clears the Output Acknowledge line before it places the next word on the Output Data lines.

Steps b. through i. of this sequence are repeated for every data word until the number of words specified in the output buffer have been transferred.

Computer to Computer Communications

Since many input/output channels of the computer can be intercomputer channels, it is possible for the UNIVAC 1616 to communicate with a number of other computers. The control signals and lines governing intercomputer communication shown in Figure 6 illustrate the interface between two computers.

The control signals in the input cable are the same for intercomputer communication as for communication with peripheral equipment. In the output cable, Ready and Resume signals are used to control intercomputer transfer of data.

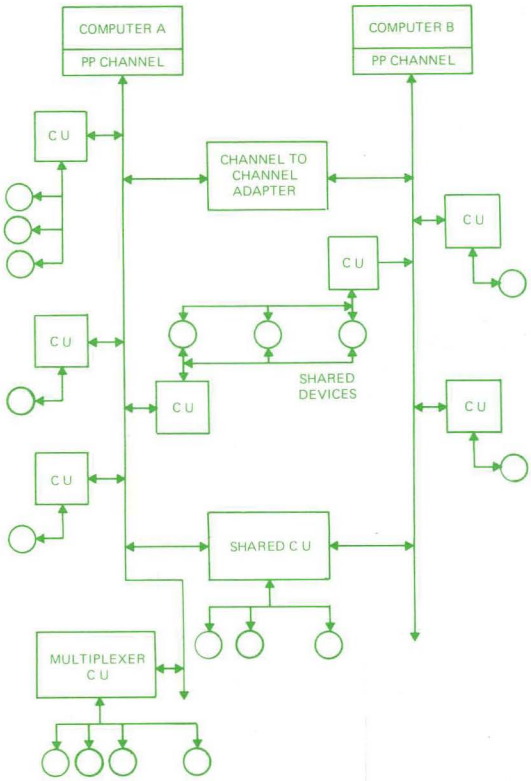


Figure 8. Processor-Peripheral Channel Interface

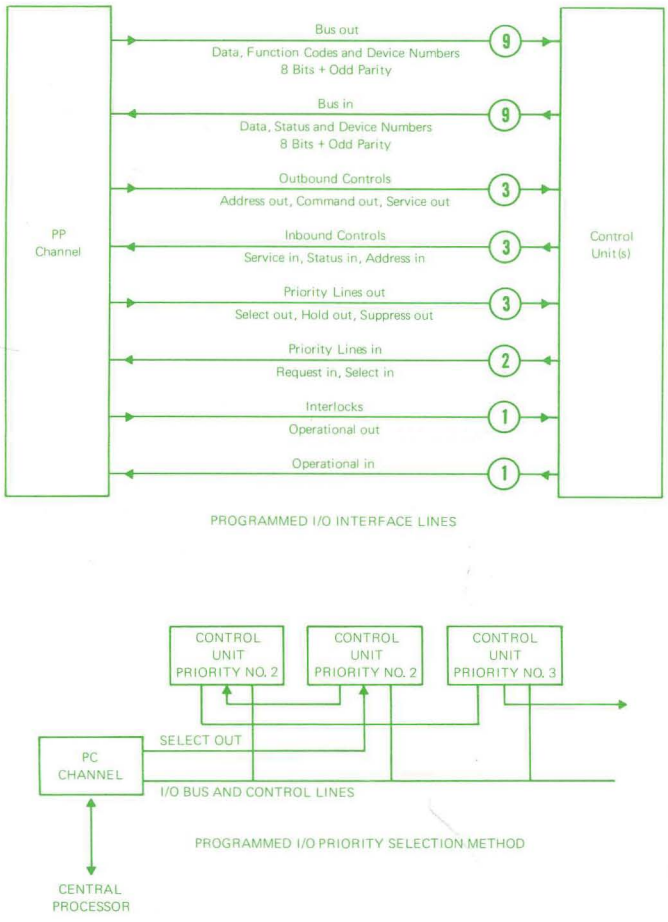


Figure 9. Programmed I/O Interface Structure

PROGRAMMED I/O

Programmed input/output operations require direct central processor involvement for each datum transfer. The byte-oriented I/O transfers are handled by the Processor-Peripheral (PC) Channel which functions as a part of the central processor.

I/O Interface

The channel interface shown in Figure 8 provides the central processor with the capability of communicating with a maximum of 256 external devices via a maximum of sixteen control units. The control units perform the necessary command interpretations and data manipulation necessary for allowing the central processor and the external devices to communicate with each other. The channel also permits two central processors to communicate with each other via a channel-to-channel adapter. When a system requires two central processors, the channel permits sharing of either the control units and/or, sharing of the external devices as shown in Figure 8.

Figure 9 illustrates the channel interface signal lines. With the exception of the Select Out line, no lines are unique to any control unit. The Select Out line is different in that it is looped through the attached control units in serial order and in a sequence conforming to the channel's priority scheme. Channel priority is operative during channel polling when the Select Out is proportional through the control units one by one. The unit which first recognizes the signal and which has a need for communicating with the channel will capture the interface and make its request known to the channel. Thus time-sharing, or multiplexing, of the lines is utilized so that communications may be carried on with more than one control unit.

Transfer Operation

All data transfers of the central processor are buffered, utilizing main memory locations for buffer control, the channel interrupts the central processor program and requests that it service the channel. When the transfer is completed, the control unit relinquishes the channel and the polling process is repeated. As mentioned previously, a burst mode is provided wherein the control unit is allowed to retain channel control during transmission of a block of data.

EPILOGUE

Change generates change, and in no other area is this more evident that in the field of electronic data processing. Here, as our skills increase, our needs multiply and our systems grow in technological complexity.

Changing world conditions create new problems which require new solutions. A large part of Univac's reputation is based upon its ability to detect customer needs long before they become apparent – and to react to them in a timely manner. Univac has always supported a strong internal research and advanced development activity within its walls. As a result, Univac has acquired the knowledge and experience necessary for responding to changing requirements in the field and to create the new equipment necessary for controlling the situation. The UNIVAC 1616 computer reflects this corporate committment; it is designed for you – the ultimate user.

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