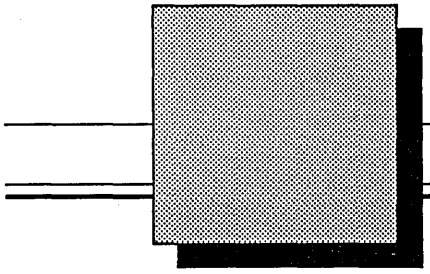


Library Reference Manual

Volume I

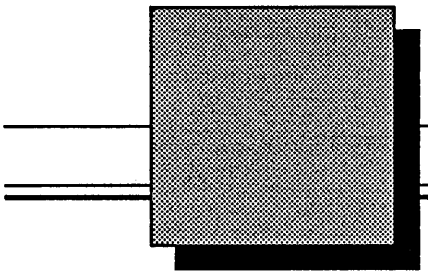
October 1, 1989

P/N: 900-00733

Valid Logic Systems, Incorporated
2820 Orchard Parkway
San Jose, California 95134
(408) 432-9400 Telex 371 9004
FAX (408) 432-9430

MANUAL REVISION HISTORY

Rev	Date	Software Release	Reason for Change
A	3–10–86	Library Release 7.3	Initial release.
B	6–30–86	Library Release 7.6	Updated libraries to include releases 7.4 and 7.6; added VAXstation II support.
C	10–10–86	Library Release 7.8	Updated libraries to include release 7.8.
D	4–6–87	Library Release 8.4	Updated libraries to include releases 8.0, 8.2, and 8.4; updated PIN_NUMBER property and added platform–specific information for the Sun Workstation.
E	10–1–89	Library Release 9.0	Updated all libraries to include releases 8.6, and 9.0; updated logic array libraries to include release 9.3; added ECL 10KH, ECL ANSI 10KH, FACT, and RCACMOS libraries; added DECstation support.



Preface

The *Library Reference Manual* lists the contents of all libraries supplied by Valid and shows an example of each part contained in each library. Version 1 of each component is shown on the left of or above the other body versions. Note the following information in the library examples:

(SIZE) Means that the body can by given a SIZE property in GED.

(OFF GRID) Means that the output pin is off grid (0. 1). Start a wire from the output pin with the blue cursor button so the wire automatically snaps to the pin. Use the white cursor button to adjust the shape of the wire, if necessary.

Table of Contents
Volume I

Section 1: Valid Standard Libraries 1-1

STANDARD Library 1-3
PHANTOM Library 1-13
The Phantom Gate 1-14
TIME Library 1-17
SIM Library 1-25
TUTORIAL Library 1-35

Section 2: 74 Series Libraries 2-1

LSTTL and ANSI LSTTL Libraries 2-3
LSTTL Library 2-15
ANSI LSTTL Library 2-39
STTL and ANSI STTL Libraries 2-69
STTL Library 2-73
ANSI STTL Library 2-81
ASTTL and ANSI ASTTL Libraries 2-91
ASTTL Library 2-97
ANSI ASTTL Library 2-107
ALSTTL and ANSI ALSTTL Libraries 2-119
ALSTTL Library 2-125
ANSI ALSTTL Library 2-137
HCMOS and ANSI HCMOS Libraries 2-153
HCMOS Library 2-165
ANSI HCMOS Library 2-181

FAST and ANSI FAST Libraries 2-201
FAST Library 2-213
ANSI FAST Library 2-237
TTL and ANSI TTL Libraries 2-267
TTL Library 2-275
ANSI TTL Library 2-283
FACT Library 2-293
RCACMOS Library 2-309

Table of Contents
Volume II

Section 3: 54 Series Libraries 3-1

54LSTTL and ANSI 54LSTTL Libraries 3-3
54LSTTL Library 3-13
ANSI 54LSTTL Library 3-31
54STTL and ANSI 54STTL Libraries 3-53
54STTL Library 3-57
ANSI 54STTL Library 3-63
54ASTTL and ANSI 54ASTTL Libraries 3-71
54ASTTL Library 3-75
ANSI 54ASTTL Library 3-81
54ALSTTL and ANSI 54ALSTTL Libraries 3-89
54ALSTTL Library 3-97
ANSI 54ALSTTL Library 3-109
54HCMOS and ANSI 54HCMOS Libraries 3-125
54HCMOS Library 3-137
ANSI 54HCMOS Library 3-153
54FAST and ANSI 54FAST Libraries 3-171
54FAST Library 3-175
ANSI 54FAST Library 3-183
54TTL and ANSI 54TTL Libraries 3-193
54TTL Library 3-197
ANSI 54TTL Library 3-201

Section 4: Miscellaneous Libraries 4-1

CMOS Library 4-3
DISCRETE Library 4-23
MEMORY and ANSI MEMORY Libraries 4-29
MEMORY Library 4-35
ANSI MEMORY Library 4-49
MM74C Library 4-71

Section 5: ECL Libraries 5-1

10K Library 5-3
10KH and ANSI 10KH Libraries 5-15
10KH Library 5-19
ANSI 10KH Library 5-21
100K Library 5-23

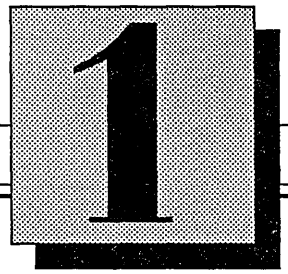
Section 6: The LOGIC ARRAY Libraries 6-1

Programmable Logic Devices User's Guide 6-3
Modeling Programmable Logic Devices 6-4
Implementing Programmable Logic Devices 6-5
Fusemap file 6-5
PLD description file 6-5
User Interface 6-7
Makepld 6-7
Genpld 6-9
Rempld 6-10

Programmable Logic Devices and Scald Software .. 6–11
Graphics Editor 6–11
Compiler 6–12
Simulator 6–12
Timing Verifier 6–13
Packager 6–13
PLD Description File Format 6–14
Design Flow 6–16
Installation 6–17
NEWPAL20 Library 6–19
NEWPAL24 Library 6–27
ADVPAL Library 6–39
IFL Library 6–45

Additional Libraries A–1

Index I–1

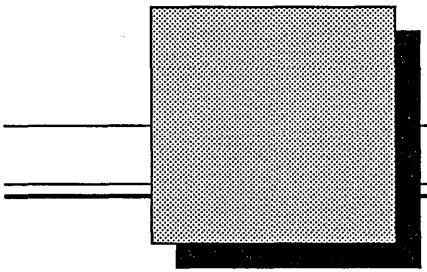


Valid Standard Libraries

This section describes the individual libraries that make up the Valid Standard libraries.

Contents

STANDARD Library 1–3
PHANTOM Library 1–13
TIME Library 1–17
SIM Library 1–25
TUTORIAL Library 1–35



The STANDARD Library

The STANDARD Library requires approximately 253 Kbytes of disk storage.

The STANDARD Library contains parts that have no logic function or physical meaning. These parts are used either to convey design information to the Compiler, Timing Verifier, Simulator, and Packager, or to make the schematic more concisely represent the design. Each part in this library is a body that can be added to a drawing of any type (.LOGIC, .BODY, etc.)

The release level of the STANDARD Library is 9.0.

The following 30 parts (bodies) are in the Standard Library:

A SIZE PAGE

An A–size page border that can be placed around a drawing. The border provides a space for the engineer's name, the date, and notes. The border has no other significance and is not required.

B SIZE PAGE

A B–size page border that can be placed around a drawing. The border provides a space for the engineer's name, the date, and notes. The border has no other significance and is not required.

DEFINE

Used to define text macros which are specified as properties of this body. The property name is the text macro name and the value is its definition.

DRAWING

Used to attach properties to the entire drawing.

FLAG

Flag bodies can be added to interface signals to indicate the physical pins of a design. Flag bodies are usually not required. They are required as Packager output by some physical design systems.

MERGE/DEMERGE

The merge/demerge bodies are used to combine a number of separate signals into a single vectored signal, or to separate a vectored signal into a number of separate signals. This allows you to draw the vectored signal (the bus) as a single wire in parts of the drawing, and to draw it as several signals in other parts of the drawing. For example, an address bus called ABUS<15..0> could be made up of ABUS<8..0> connected to a memory device, and ABUS<10..9>, ABUS<12..11>, and ABUS<15..13> connected to decoders and other control devices.

Using a 4MERGE merge body lets you draw each of the four signals separately on part of the drawing, and then merge them into a single signal in another part of the design. This merge function is performed by synonyming the single signal name with the concatenation of the other signal names.

Each merge body has four versions, two for merges and two for demerges. Versions 1 and 2 have inputs on 0.2–inch centers and versions 3 and 4 have inputs on 0.1–inch centers. Each merge body accepts a different number of input signals to be con catenated together. The merge bodies provided in the Valid libraries are:

2 MERGE
3 MERGE
4 MERGE
5 MERGE
6 MERGE
7 MERGE
8 MERGE

Other merge bodies can be defined. The definition of the merge body is found in a .LOGIC drawing that contains only a SYNONYM body.

The versions of the 2, 4, 6, 8, and 10 merge bodies having inputs on 0.1–inch centers have outputs off grid. To connect a wire to these points, use the blue button on the puck or the right hand button on the mouse. For additional information on wiring, see the *ValidGED User's Manual.*

MSB TAP, LSB TAP, and BIT TAP

The TAP bodies are used to extract, or "break out," a single bit from a vectored signal. There are three TAP bodies:

- The MSB TAP extracts the most significant bit from the signal.
- The LSB TAP extracts the least significant bit from the signal.
- The BIT TAP extracts any single bit from a bus.

For the MSB TAP and the LSB TAP, the width of the signal to be extracted is specified by the SIZE property.

For the BIT TAP, the body property BIT must be changed to select any single bit from bit number 0 to bit number <bus size>–1.

NOT

The NOT body supports the Bubble Checker feature of the Compiler. The NOT body is seen only by the Bubble Checker. It does not change the assertion of a signal. If the Bubble Checker is turned off (by the Compiler directive), the signals on either side of the NOT body are synonymed together and the NOT body is otherwise simply ignored.

This body is used to convert a signal from one assertion to the other for the Bubble Checker without a logical inversion taking place. The NOT body definition is found in NOT.LOGIC. It consists of nothing more than a SYNONYM body to which the two NOT body signals are connected.

ORIGIN

The Graphics Editor automatically uses this body to indicate the origin of any body. The ORIGIN body is not added manually to a drawing. When you edit a .BODY drawing, an origin body (a small X) appears at the center of the screen.

PIN NAMES

The PIN NAMES body is used in hierarchical design and in library development. The PIN NAMES body is added to an unused area of a .LOGIC drawing; the Graphics Editor automatically attaches the names of the pins on the .BODY drawing to the PIN NAMES body on the .LOGIC drawing and appends a \I suffix (scope = interface) to each signal name. The signal names can be moved and reattached to the hierarchical body and the PIN NAMES body then deleted. The use of the PIN NAMES body eliminates the need to retype the signal names and reduces the chances of mislabeling signal names or omitting the local scope (\I) signal property.

REPLICATE

The REPLICATE body is used when making models for sizable parts. This body is used by library developers and is usually added to .TIME and .SIM drawings. It is not usually added to a .LOGIC drawing.

SIGN EXTEND

The SIGN EXTEND body is used to extend an n-bit signal to a SIZE-bit signal by replicating the sign bit. The SIZE property is attached to the body. The MSB (the most significant bit) of the signal is always extended.

SLASH

A SLASH body may be added to a vectored signal to provide a visible note of the signal width. It is also used to check the width of the parent signal. When

you attach a SLASH body you change the value of the SIZE property attached to the body to the correct value. The Compiler checks that the value of the SIZE property for the SLASH body matches the width of the signal. If the two do not match, an error is generated.

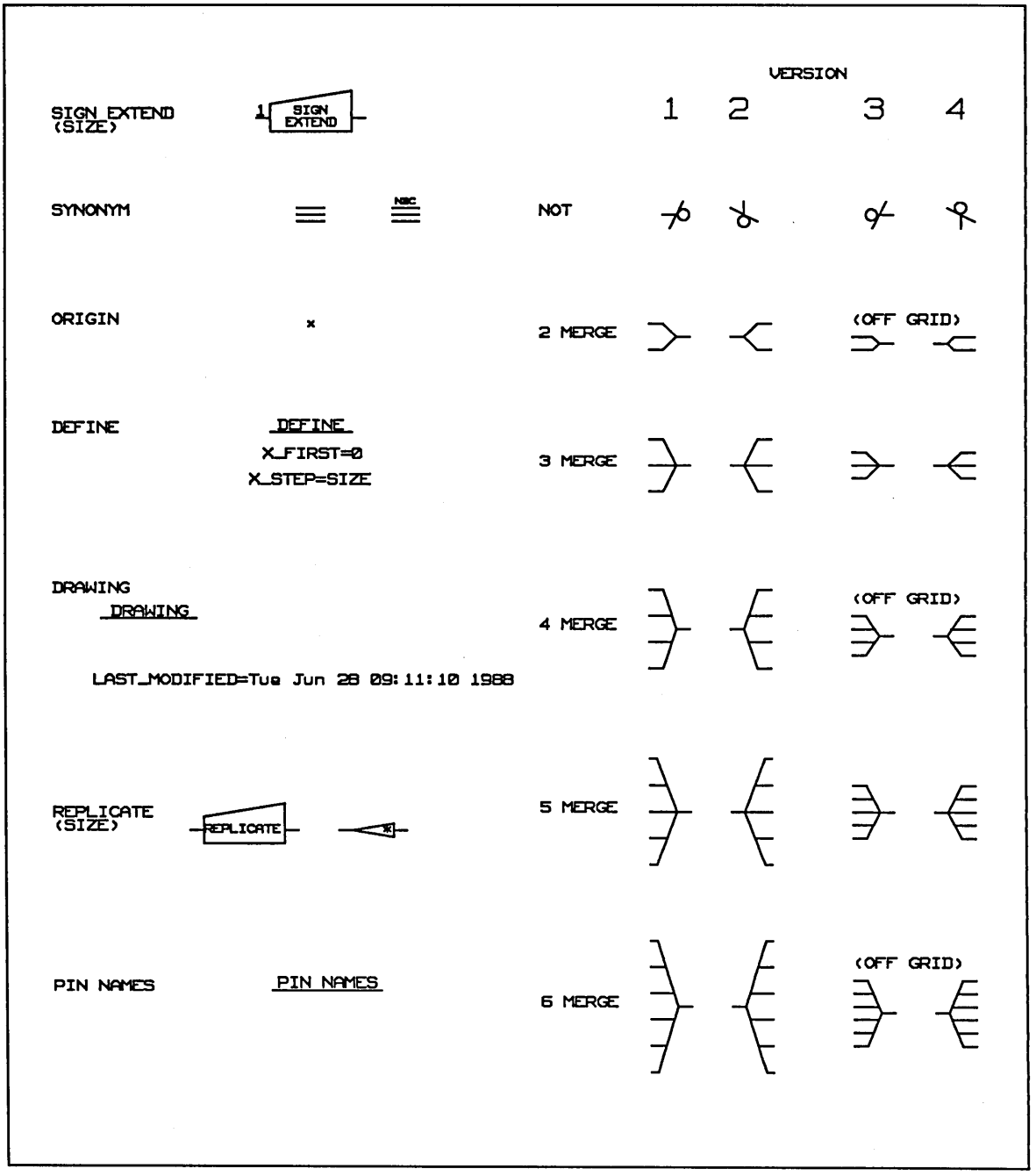
SYNONYM

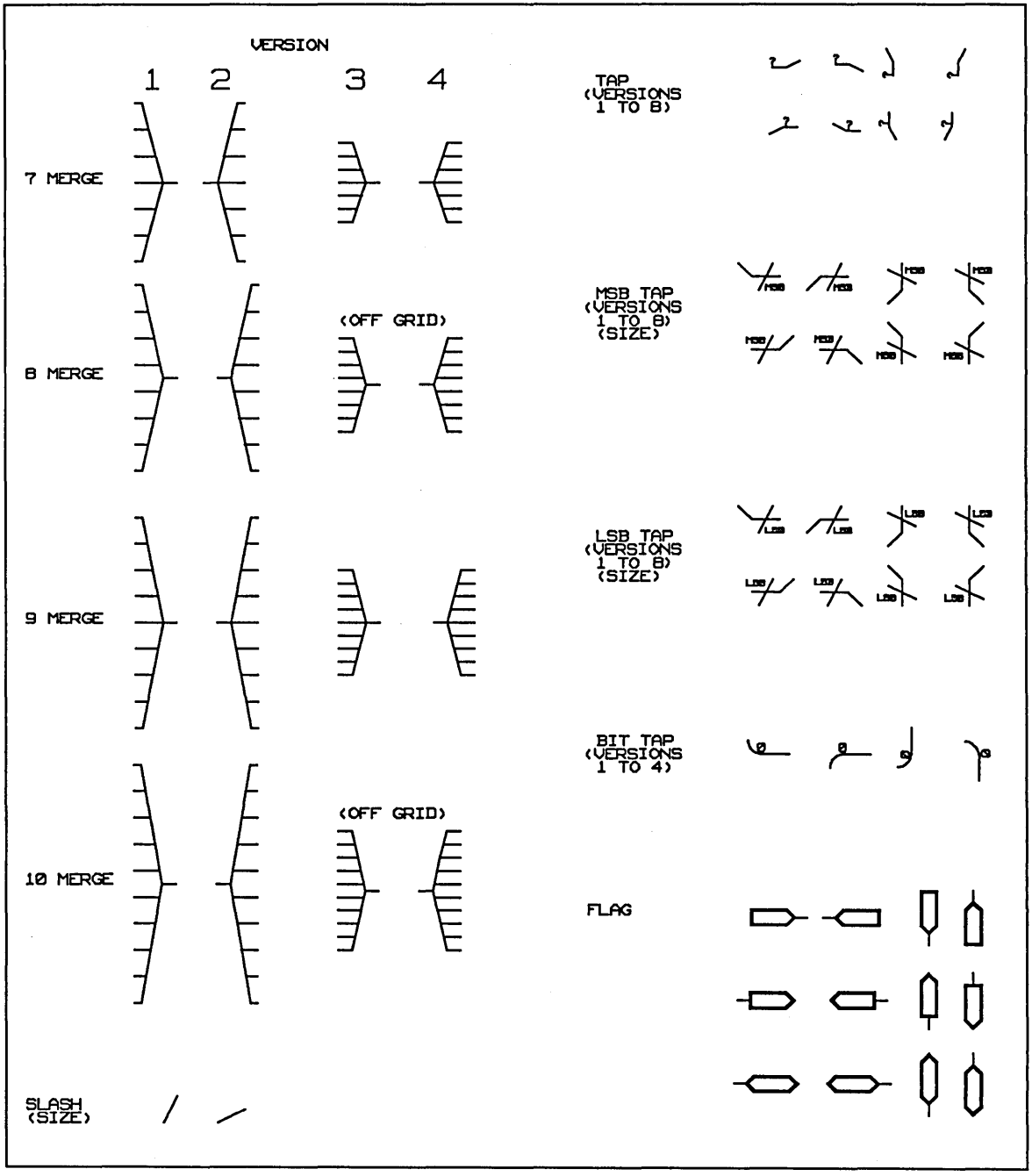
The SYNONYM body is a body with two pins of the same name. Add the synonym body in a corner of the drawing, and use the SIGNAME command to give each of the two pins of the synonym body the name of one of the signals to be synonymed. The assertions of the two signals must match and the signals must have the same width. The synonym body has a definition found in SYNONYM.LOGIC. It is empty. There is a property on the DRAWING body of this drawing that allows this (it is normally not permitted). The property TERMINAL=TRUE tells the Compiler that this is a terminal drawing and does not have to be expanded.

When signals are synonymed together they become aliases for each other. Both names refer to the same physical signal (net). When a signal has a very long name it is convenient to give it a shorter name with a SYNONYM body.

The Compiler performs the synonym function. Two signals are synonymed when the signal names are each connected to a pin of the SYNONYM body, or when the signal names are connected to the same pin of any body. The latter condition should be avoided. Bus-through pins are also implemented by the Compiler synonym function. Two distinct pins

	on the body are given the same name and the signals connected to them are therefore synonymed together.
TIME_DIRECTIVES	This body is used to pass directives to the Timing Verifier. Properties attached to this body are Timing Verifier directives. This body is used infrequently.
SIM_DIRECTIVES	This body is used to pass directives to the Simulator. Properties attached to this body are Simulator directives. This body is used infrequently.
VALID A SIZE PAGE	An A-size page border that can be placed around drawings. The border includes the Valid logo and copyright statement. The border has no other significance and is not required. The border is used for Valid-supplied models and drawings.
VALID B SIZE PAGE	A B-size page border that can be placed around drawings. The border includes the Valid logo and copyright statement. The border has no other significance and is not required. The border is used for Valid-supplied models and drawings.


VERSION
1
2
3
4
SIGN EXTEND (SIZE)
1
SIGN EXTEND
SYNONYM
NOT
ORIGIN
2 MERGE
(OFF GRID)
DEFINE
DEFINE
X_FIRST=0
X_STEP=SIZE
3 MERGE
DRAWING
DRAWING
4 MERGE
(OFF GRID)
LAST_MODIFIED=Tue Jun 28 09:11:10 1988
REPLICATE (SIZE)
REPLICATE
5 MERGE
PIN NAMES
PIN NAMES
6 MERGE
(OFF GRID)


VERSION
1
2
3
4
7 MERGE
8 MERGE
(OFF GRID)
9 MERGE
10 MERGE
(OFF GRID)
SLASH
(SIZE)
TAP
(VERSIONS
1 TO 8)
MSB TAP
(VERSIONS
1 TO 8)
(SIZE)
LSB TAP
(VERSIONS
1 TO 8)
(SIZE)
BIT TAP
(VERSIONS
1 TO 4)
FLAG

TIME_DIRECTIVES

TIMING VERIFIER DIRECTIVES

```
CLOCK_PERIOD=100.0
CLOCK_INTERVALS=8
CLOCK_SKEW=0.0
PREC_CLOCK_SKEW=0.0
DOT_TYPE=DOT_OR
LIST=NOUNNAMED
MAX_ERRORS=10
MAX_EXP_ERRORS=0
MAX_EVAL_PASSES=200
PRINT_WIDTH=132
RISE_FALL_ANAL=ON
RISE_FALL_MODELS=ON
TIMING_DIAGRAMS=OFF
TS_BUS_TYPE=DOT_TS
WIRE_DELAY=0.0-0.0
```

SIM_DIRECTIVES

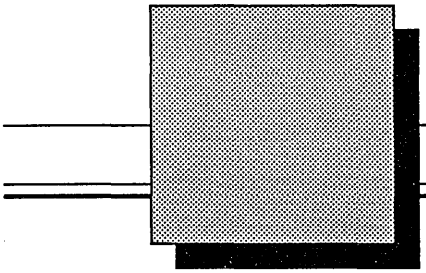
SIMULATOR DIRECTIVES

```
CLOCK_PERIOD=100.0
CLOCK_INTERVALS=8
COMPILER_OUTPUT='CMPEXP.DAT'
COMMAND_FILE='TEST.CMD'
MEM_STATE=4
OUTPUT=LIST,COMMAND_LOG
SESSION_LOG=ON
SYNONYM_FILE='CMPSYN.DAT'
TERMINAL=VT100
```

OTHER BODIES IN THE STANDARD LIBRARY

```
A SIZE PAGE  -  'A' SIZE BORDER FOR A DRAWING
B SIZE PAGE  -  'B' SIZE BORDER FOR A DRAWING
C SIZE PAGE  -  'C' SIZE BORDER FOR A DRAWING
D SIZE PAGE  -  'D' SIZE BORDER FOR A DRAWING

VALID A SIZE PAGE  -  VALID'S STANDARD A SIZE PAGE
VALID B SIZE PAGE  -  VALID'S STANDARD B SIZE PAGE
```



The PHANTOM Library

The PHANTOM Library requires approximately 202 Kbytes of disk storage; there are 14 components in the library.

The release level of the PHANTOM Library is 9.0.

The Phantom Gate

Phantom gates are used when designing with parts using either OPEN COLLECTOR or OPEN EMITTER technology. The TTL family of parts uses OPEN COLLECTOR technology, for example. These two technologies permit outputs to be wired together. The wired outputs act as a logic gate, a so-called wire-gate. In the case of OPEN COLLECTOR technology, the wire-gate performs an AND function, and in the case of OPEN EMITTER technology the wire-gate performs an OR function. Phantom OR-gates and phantom AND-gates are both provided in this library. All phantom gates have a circle at the center so they can be easily distinguished from real logic gates.

Phantom gates are used for OPEN COLLECTOR and OPEN EMITTER connections, but not for TRI_STATE connections.

Instead of joining output wires with a T-junction or a dot, the appropriate phantom body can be added to the drawing and the output wires wired to the input pins of the phantom body. This procedure makes the logic function of the wire-gate visible on the drawing while clearly showing (with a circle on the phantom gate) that the logic function is not performed by a real gate.

The Packager removes the phantom bodies before creating a physical net list. For more details on phantom bodies, see the *ValidPACKAGER Reference Manual* and the *SCALD Language Manual.*

In order to make the phantom gates perform as desired, the WIRE_GATE property is attached to each body on the library drawing for the phantom library (this drawing is named PHANTOM LIBRARY). This property informs the Packager to remove the body before creating a physical net list.

PHAN AND

The Phantom AND body is used where connecting outputs together forms an AND function. This is the case for OPEN COLLECTOR. There are two versions of each body. The bodies are:

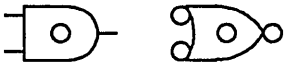
PHAN 2 AND
PHAN 3 AND
PHAN 4 AND
PHAN 5 AND
PHAN 6 AND
PHAN 7 AND
PHAN 8 AND

PHAN OR

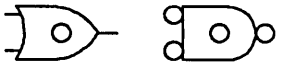
The Phantom OR body is used where connecting outputs together forms an OR function. This is the case for OPEN EMITTER. There are two versions of each body. The bodies are:

PHAN 2 OR
PHAN 3 OR
PHAN 4 OR
PHAN 5 OR
PHAN 6 OR
PHAN 7 OR
PHAN 8 OR

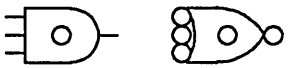
PHAN_2 AND
(SIZE)



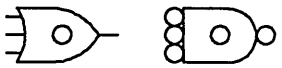
PHAN_2 OR
(SIZE)



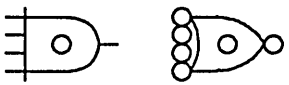
PHAN_3 AND
(SIZE)



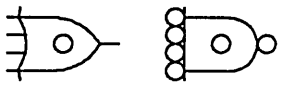
PHAN_3 OR
(SIZE)



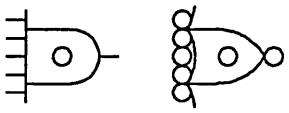
PHAN_4 AND
(SIZE)
(OFF GRID)



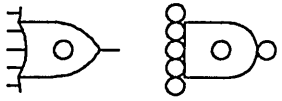
PHAN_4 OR
(SIZE)
(OFF GRID)



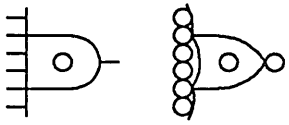
PHAN_5 AND
(SIZE)



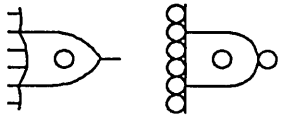
PHAN_5 OR
(SIZE)



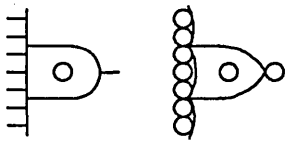
PHAN_6 AND
(SIZE)
(OFF GRID)



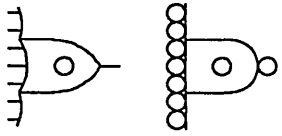
PHAN_6 OR
(SIZE)
(OFF GRID)



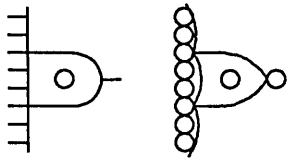
PHAN_7 AND
(SIZE)



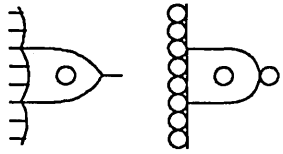
PHAN_7 OR
(SIZE)

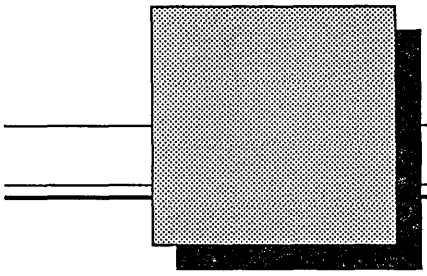


PHAN_8 AND
(SIZE)
(OFF GRID)



PHAN_8 OR
(SIZE)
(OFF GRID)





The TIME Library

The TIME Library requires approximately 237 Kbytes of disk storage; there are 43 components (primitives) in the library.

The TIME Library contains all the Timing Verifier primitives. These primitives are used to build timing models (.TIME drawings) for all of the parts in the Valid libraries. Timing Verifier primitives can only be added to a .TIME drawing. They cannot be added to a .LOGIC drawing.

The release level of the TIME Library is 9.0.

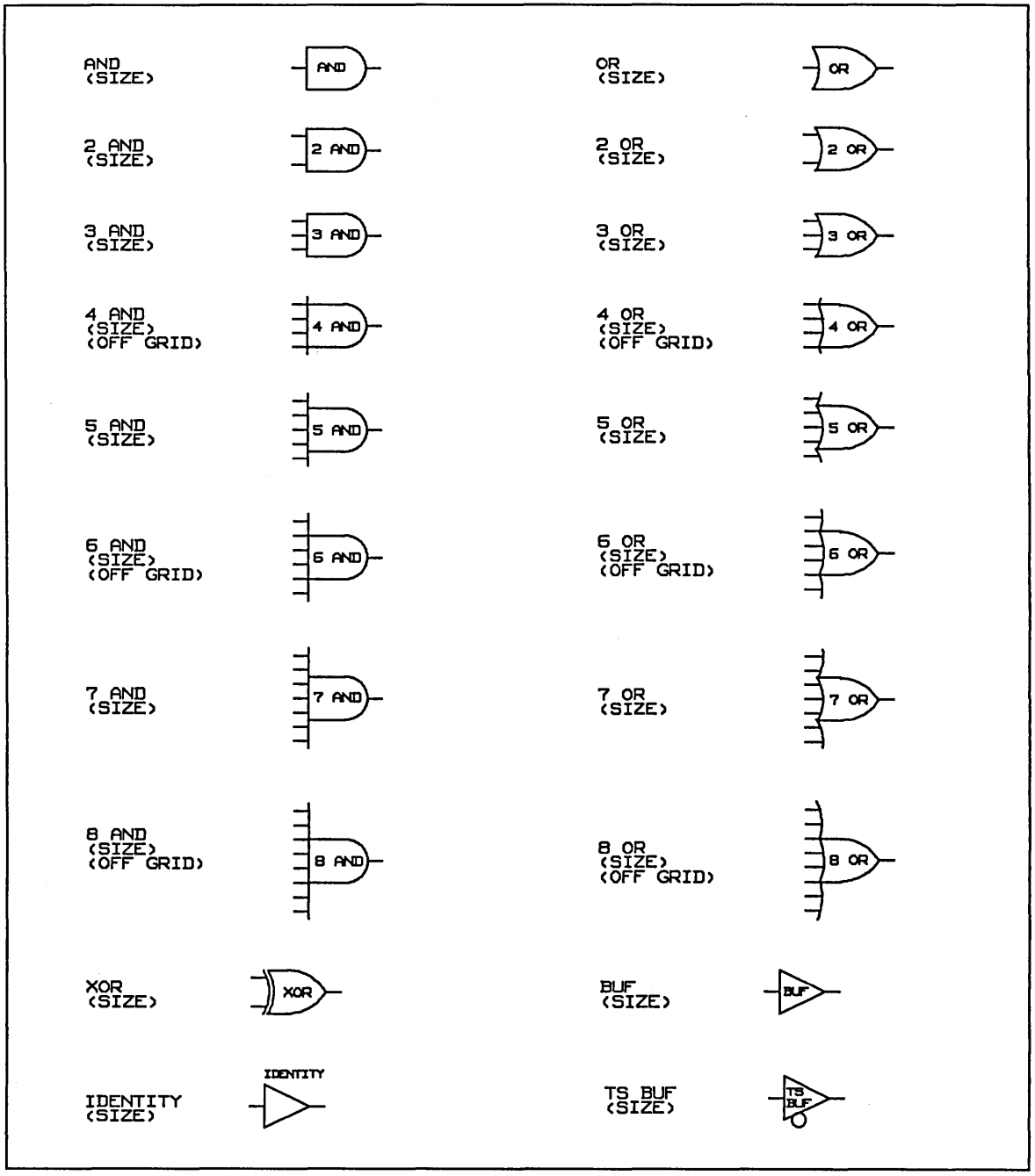
Each Timing Verifier primitive consists of a body and a .PRIM drawing. Every pin of each body can be bubbled individually. This is quite different from the bubbling capability of physical parts. There is only one version of each of the Timing Verifier primitives because each primitive pin can be bubbled individually. See the *Timing Verifier Reference Manual* for a detailed description of each Timing Verifier primitive.

The following primitives are included in the TIME library:

AND	SIZE inputs to single bit output AND gate
2 AND	2-input SIZE-wide AND gate
3 AND	3-input SIZE-wide AND gate
4 AND	4-input SIZE-wide AND gate
5 AND	5-input SIZE-wide AND gate
6 AND	6-input SIZE-wide AND gate
7 AND	7-input SIZE-wide AND gate
8 AND	8-input SIZE-wide AND gate
OR	SIZE inputs to single bit output OR gate
2 OR	2-input SIZE-wide OR gate
3 OR	3-input SIZE-wide OR gate
4 OR	4-input SIZE-wide OR gate
5 OR	5-input SIZE-wide OR gate
6 OR	6-input SIZE-wide OR gate
7 OR	7-input SIZE-wide OR gate
8 OR	8-input SIZE-wide OR gate

CHG	SIZE inputs to single bit output CHANGE gate
2 CHG	2-input SIZE-wide CHANGE gate
3 CHG	3-input SIZE-wide CHANGE gate
4 CHG	4-input SIZE-wide CHANGE gate
5 CHG	5-input SIZE-wide CHANGE gate
6 CHG	6-input SIZE-wide CHANGE gate
7 CHG	7-input SIZE-wide CHANGE gate
8 CHG	8-input SIZE-wide CHANGE gate
XOR	2-input SIZE-wide XOR gate
BUF	1-input SIZE-wide BUFFER gate
THRESHOLD	1-input SIZE-wide threshold gate
IDENTITY	1-input SIZE-wide identity gate
RES	1-input SIZE-wide resistor
TS	BUF SIZE-wide tristate driver with enable
LATCH	SIZE-wide latch with enable
LATCH RS	SIZE-wide latch with enable and asynchronous set and reset
REG	SIZE-wide rising-edge triggered register
REG RS	SIZE-wide rising-edge triggered register with asynchronous set and reset
2 MUX	SIZE-wide 2-input multiplexer
4 MUX	SIZE-wide 4-input multiplexer
8 MUX	SIZE-wide 8-input multiplexer

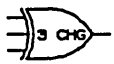
SETUP HOLD	SIZE-wide rising-edge setup and hold checker
SETUP RISE HOLD FALL	SIZE-wide rising-edge setup and falling-edge hold checker
EDGE TO EDGE	SIZE-wide rising-edge to rising-edge skew checker
MIN PULSE WIDTH	SIZE-wide minimum pulse width checker
TRANSMISSION GATE	SIZE-wide bidirectional transmission gate
UNI TRANS GATE	SIZE-wide uni-directional transmission gate


AND
(SIZE)
AND
OR
(SIZE)
OR
2 AND
(SIZE)
2 AND
2 OR
(SIZE)
2 OR
3 AND
(SIZE)
3 AND
3 OR
(SIZE)
3 OR
4 AND
(SIZE)
(OFF GRID)
4 AND
4 OR
(SIZE)
(OFF GRID)
4 OR
5 AND
(SIZE)
5 AND
5 OR
(SIZE)
5 OR
6 AND
(SIZE)
(OFF GRID)
6 AND
6 OR
(SIZE)
(OFF GRID)
6 OR
7 AND
(SIZE)
7 AND
7 OR
(SIZE)
7 OR
8 AND
(SIZE)
(OFF GRID)
8 AND
8 OR
(SIZE)
(OFF GRID)
8 OR
XOR
(SIZE)
XOR
BUF
(SIZE)
BUF
IDENTITY
(SIZE)
IDENTITY
TS BUF
(SIZE)
TS
BUF

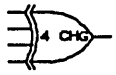
CHG
(SIZE)

2 CHG
(SIZE)

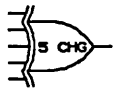
3 CHG
(SIZE)



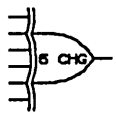
4 CHG
(SIZE)
(OFF GRID)



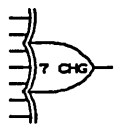
5 CHG
(SIZE)



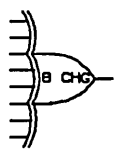
6 CHG
(SIZE)
(OFF GRID)



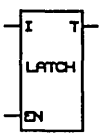
7 CHG
(SIZE)



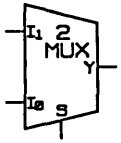
8 CHG
(SIZE)
(OFF GRID)

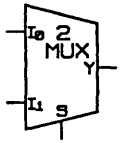


LATCH
(SIZE)

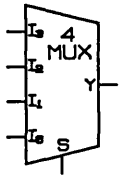


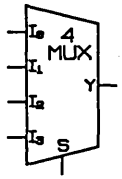
2 MUX
(SIZE)



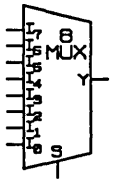


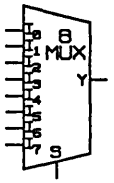
4 MUX
(SIZE)



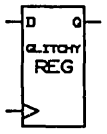


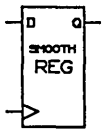
8 MUX
(SIZE)



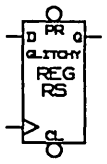


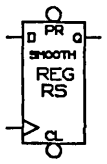
REG
(SIZE)



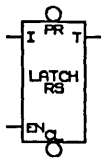


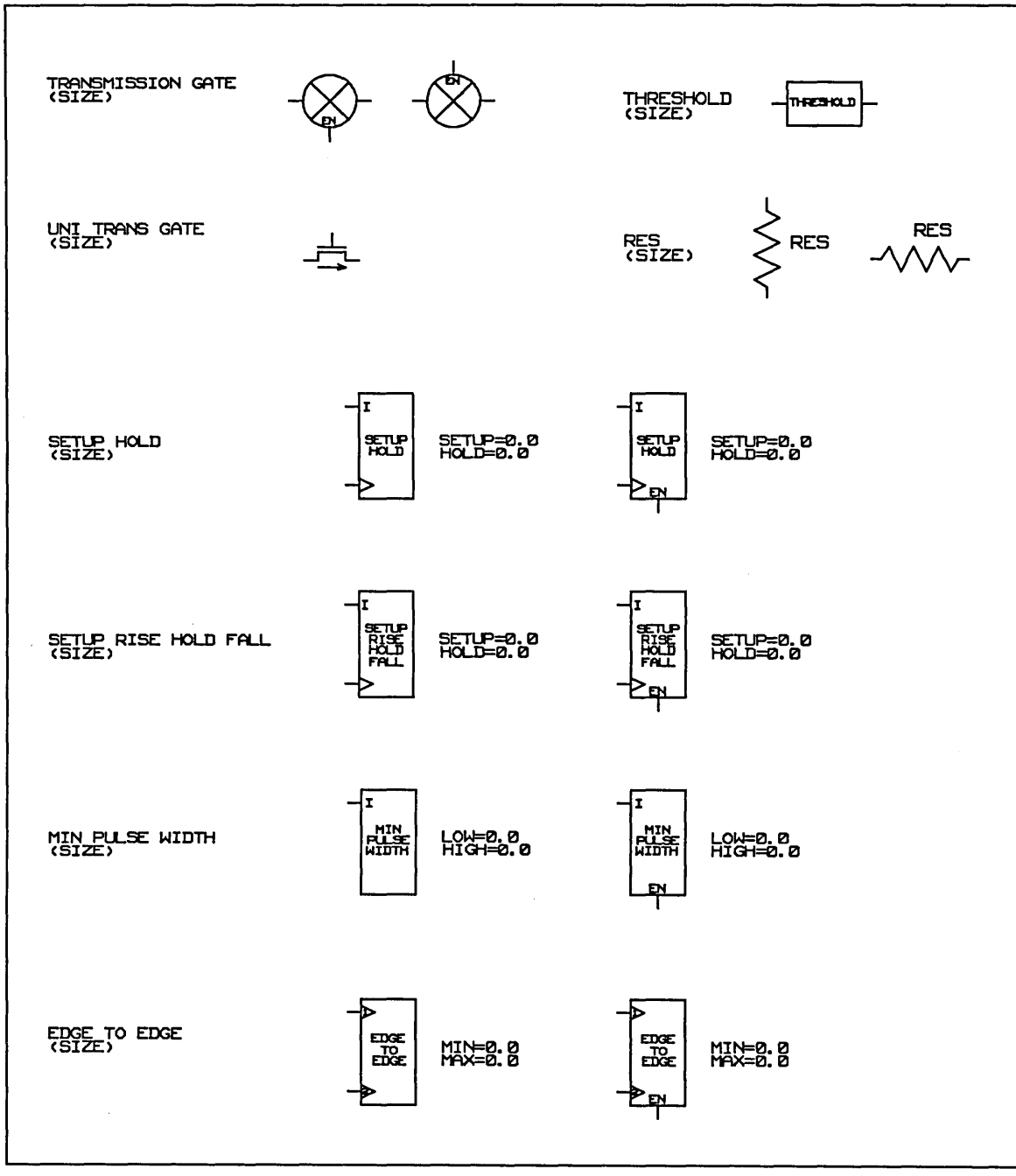
REG RS
(SIZE)

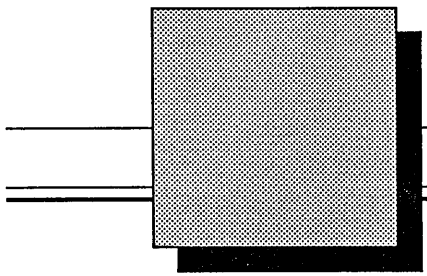




LATCH RS
(SIZE)




TRANSMISSION GATE
(SIZE)
EN
EN
THRESHOLD
(SIZE)
THRESHOLD
UNI_TRANS GATE
(SIZE)
RES
(SIZE)
RES
RES
SETUP_HOLD
(SIZE)
I
SETUP
HOLD
SETUP=0.0
HOLD=0.0
I
SETUP
HOLD
EN
SETUP=0.0
HOLD=0.0
SETUP_RISE_HOLD_FALL
(SIZE)
I
SETUP
RISE
HOLD
FALL
SETUP=0.0
HOLD=0.0
I
SETUP
RISE
HOLD
FALL
EN
SETUP=0.0
HOLD=0.0
MIN_PULSE_WIDTH
(SIZE)
I
MIN
PULSE
WIDTH
LOW=0.0
HIGH=0.0
I
MIN
PULSE
WIDTH
EN
LOW=0.0
HIGH=0.0
EDGE_TO_EDGE
(SIZE)
EDGE
TO
EDGE
MIN=0.0
MAX=0.0
EDGE
TO
EDGE
EN
MIN=0.0
MAX=0.0



The SIM Library

The SIM Library requires approximately 354 Kbytes of disk storage; there are 51 components (primitives) in the library.

The SIM Library contains all the Logic Simulator primitives. These primitives are used to build simulation models (.SIM drawings) for all of the parts in the Valid libraries. Simulator primitives can only be added to a .SIM drawing. They cannot be added to a .LOGIC drawing.

The release level of the SIM Library is 9.0.

Each Simulator primitive consists of:

- A body
- A .PRIM drawing

Every pin of each body can be bubbled individually. This is quite different from the bubbling capability of physical parts. There is only one version of each of the Simulator primitives because each primitive pin can be bubbled individually.

See the *ValidSIM Reference Manual* for a detailed description of each Simulator primitive.

AND

There are several different AND primitives, each with a different number of inputs:

2 AND
3 AND
4 AND
5 AND
6 AND
7 AND
8 AND

OR

There are several different OR primitives, each with a different number of inputs:

2 OR
3 OR
4 OR
5 OR
6 OR
7 OR
8 OR

XOR

Exclusive-OR primitive

BUF	Buffer primitive
TS BUF	3-state buffer primitive
MUX	Several multiplexer primitives are provided: **2 MUX** **4 MUX** **8 MUX**
REG, REG RS, REG RS COMP, REG RS COMP 2	Register primitives
LATCH, LATCH RS, LATCH RS COMP, SCAN LATCH, SCAN LATCH RS	Latch primitives
JK	JK flip-flop primitive
RES	Resistor primitive
PASS TRANSISTOR	Pass transistor primitive
UNI PASS TRANSISTOR	Uni pass transistor primitive
COUNTER SHIFT REGISTER	Counter/shift register primitive. This is equivalent to the ECL 100136 part.
IDENTITY	The identity primitive. This primitive is similar to the BUF primitive except that it outputs 'Z' if the input is 'Z' (the BUF primitive outputs a 'U' if its input is 'Z').
FLAG	Flag bodies can be added to interface signals to indicate the physical pins of a design.

TIMING CHECKERS

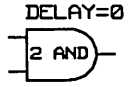
SETUP HOLD SIZE	Wide rising-edge setup and hold checker
SETUP RISE HOLD FALL	SIZE-wide rising-edge setup and falling-edge hold checker
EDGE TO EDGE	SIZE-wide rising-edge to rising-edge skew checker
MIN PULSE WIDTH	SIZE-wide minimum pulse width checker

MISCELLANEOUS

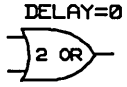
The following primitives are also available:

1 OF 8 DECODER
8-BIT DECODER
PRIORITY ENCODER
8-BIT PRIO ENCODER
ALU
ADDER
CARRY SAVE ADDER
COMPARATOR
LOOKAHEAD
MEMORY
PARITY

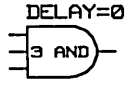
2 AND
<SIZE>



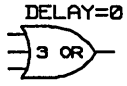
2 OR
<SIZE>



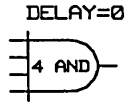
3 AND
<SIZE>



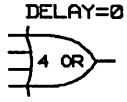
3 OR
<SIZE>



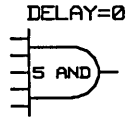
4 AND
<SIZE>
<OFF GRID>



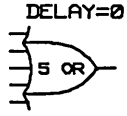
4 OR
<SIZE>
<OFF GRID>



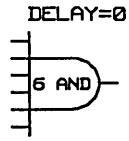
5 AND
<SIZE>



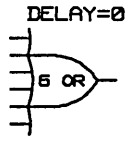
5 OR
<SIZE>



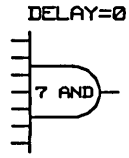
6 AND
<SIZE>
<OFF GRID>



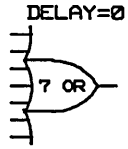
6 OR
<SIZE>
<OFF GRID>



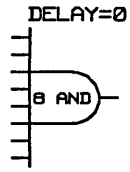
7 AND
<SIZE>



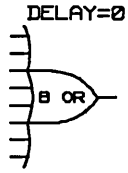
7 OR
<SIZE>



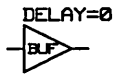
8 AND
<SIZE>
<OFF GRID>



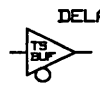
8 OR
<SIZE>
<OFF GRID>



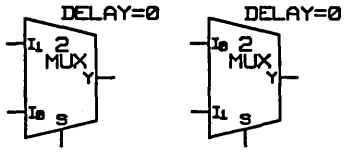
BUF
<SIZE>



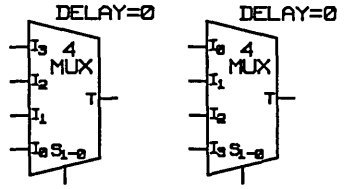
TS_BUF
<SIZE>



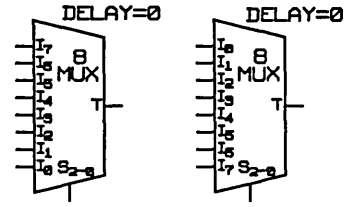
2 MUX
(SIZE)



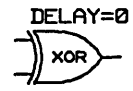
4 MUX
(SIZE)



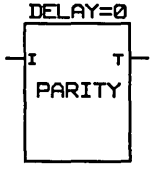
8 MUX
(SIZE)
(OFF GRID)



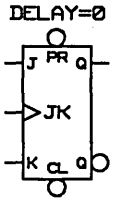
XOR
(SIZE)



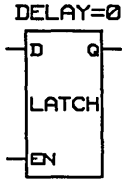
PARITY
(SIZE)



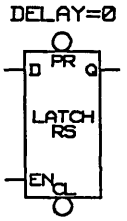
JK
(SIZE)



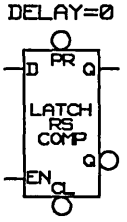
LATCH
(SIZE)



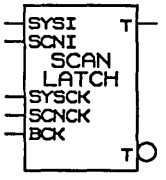
LATCH RS
(SIZE)



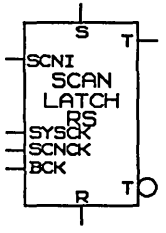
LATCH RS COMP
(SIZE)



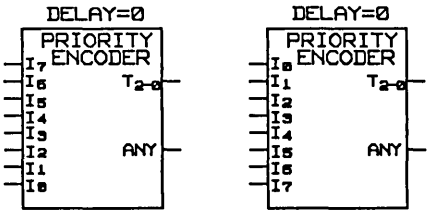
SCAN LATCH
(SIZE)



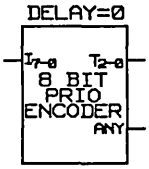
SCAN LATCH RS
(SIZE)



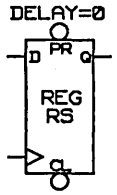
PRIORITY ENCODER



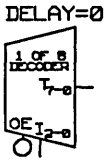
8 BIT PRIO ENCODER



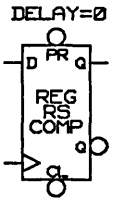
REG RS
(SIZE)



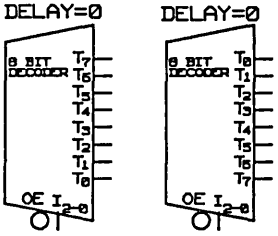
1 OF 8 DECODER



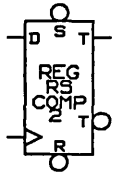
REG RS COMP
(SIZE)



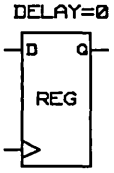
8 BIT DECODER



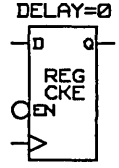
REG RS COMP 2
(SIZE)



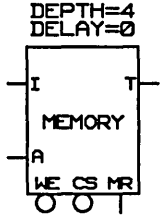
REG
(SIZE)



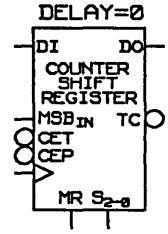
REG CKE
(SIZE)



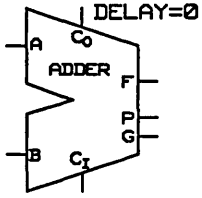
MEMORY
(SIZE)



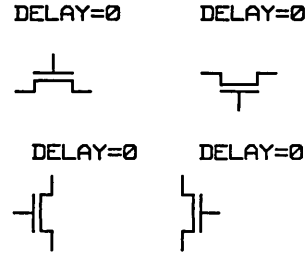
COUNTER SHIFT REGISTER
(SIZE)



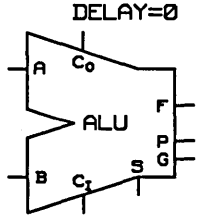
ADDER
(SIZE)



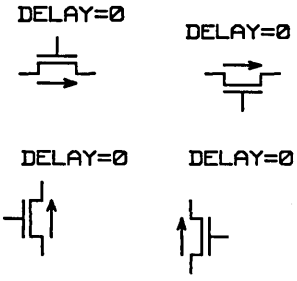
PASS TRANSISTOR
(SIZE)



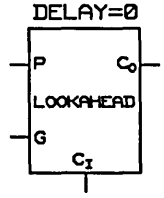
ALU
(SIZE)



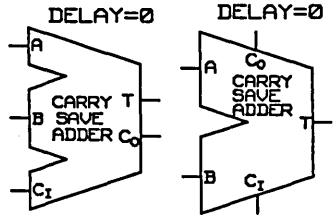
UNI PASS TRANSISTOR
(SIZE)



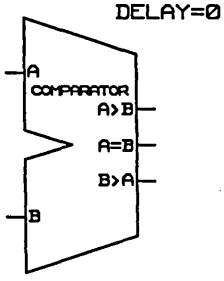
LOOKAHEAD
(SIZE)



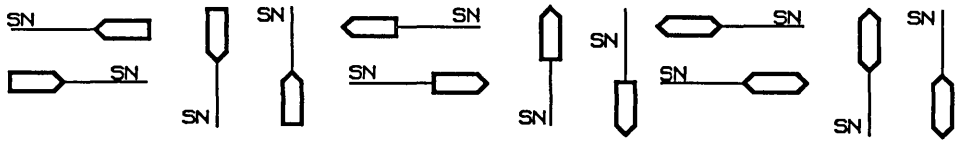
CARRY SAVE ADDER
(SIZE)



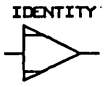
COMPARATOR
(SIZE)



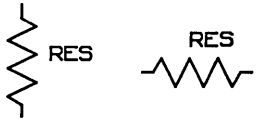
FLAG



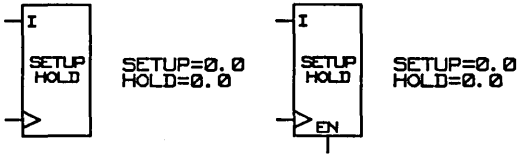
IDENTITY
(SIZE)



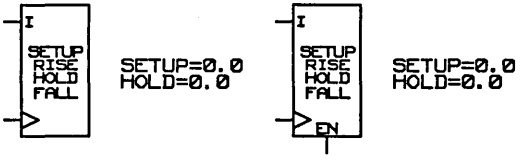
RES
(SIZE)



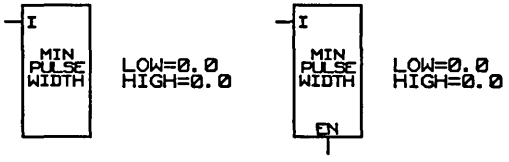
SETUP HOLD
(SIZE)



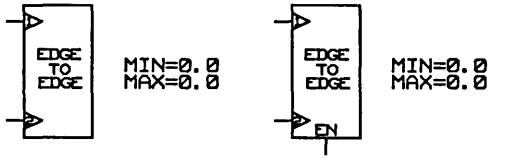
SETUP RISE
HOLD FALL
(SIZE)

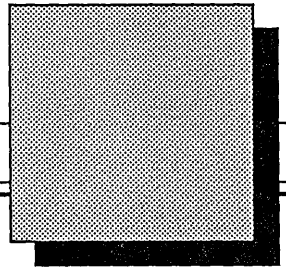


MIN PULSE WIDTH
(SIZE)



EDGE TO EDGE
(SIZE)





The TUTORIAL Library

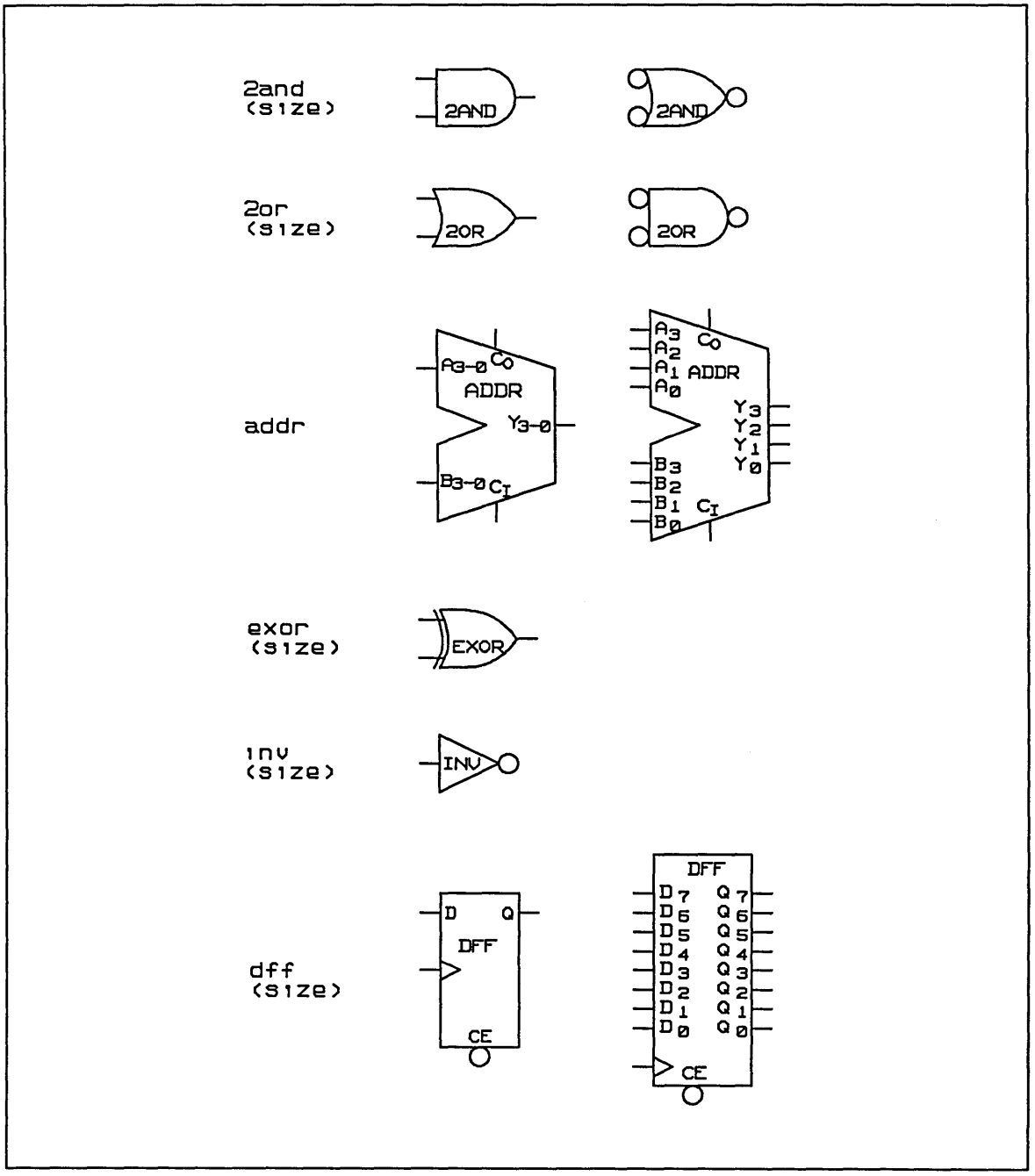
The TUTORIAL Library requires 115 Kbytes of disk storage. This library is included for use with the SCALD tutorials (Tutorial I and Tutorial II) for the various platforms.

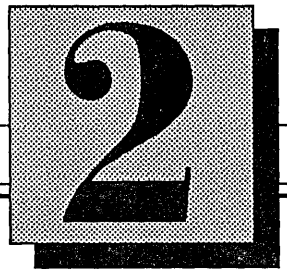
Tutorial I is a step–by–step guide to the Graphics Editor, the Compiler, and the Packager; Tutorial II is a guide to the Simulator and Timing Verifier analysis tools and to the structured and hierarchical design methodologies.

The release level of the TUTORIAL Library is 9.0.

The Tutorial Library is based on the LSTTL library and contains body drawings and physical, timing, and simulation models for the following six components:

INV	Hex inverter
2AND	Quad 2-input AND
2OR	Quad 2-input OR
EXOR	Quad 2-input exclusive-OR
ADDER	4-bit binary full-adders
DFF	Octal D-type flip-flops with enable


2and
(size)
2AND
2AND
2or
(size)
2OR
2OR
addr
A3-0
CO
ADDR
Y3-0
B3-0
CI
A3
A2
A1
A0
ADDR
CO
Y3
Y2
Y1
Y0
B3
B2
B1
B0
CI
exor
(size)
EXOR
inv
(size)
INV
dff
(size)
D
Q
DFF
CE
DFF
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CE

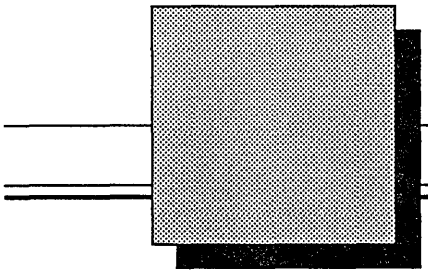


74 Series Libraries

This section describes the individual libraries that make up the 74 series libraries. Note that both standard and ANSI body styles are available for all libraries and that the same components are available in each library. The body style selected is determined by the first library name encountered in the library search path or by the last **library** command.

Contents

LSTTL/ANSI LSTTL Libraries 2-3
STTL/ANSI STTL Libraries 2-69
ASTTL/ANSI ASTTL Libraries 2-91
ALSTTL/ANSI ALSTTL Libraries 2-119
HCMOS/ANSI HCMOS Libraries 2-153
FAST/ANSI FAST Libraries 2-201
TTL/ANSI TTL Libraries 2-267
FACT Library 2-293
RCACMOS Library 2-309



The LSTTL and ANSI LSTTL Libraries

The LSTTL Library requires approximately 8837 Kbytes of disk storage, and the ANSI LSTTL Library requires approximately 8746 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*lsttl.lib* or *a74lsttl.lib*).

The release level of the LSTTL and ANSI LSTTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 219 components:

LS00	Quad 2-input NAND
LS01	Quad 2-input open-collector NAND
LS02	Quad 2-input NOR
LS03	Quad 2-input open-collector NAND
LS04	Hex inverter
LS05	Hex open-collector inverter
LS08	Quad 2-input AND
LS09	Quad 2-input open-collector AND
LS10	Triple 3-input NAND
LS11	Triple 3-input AND
LS12	Triple 3-input open-collector NAND
LS13	Dual 4-input NAND Schmitt trigger
LS14	Hex Schmitt-trigger inverter
LS15	Triple 3-input open-collector AND
LS18	Schmitt-trigger positive-NAND gate with totem-pole outputs
LS19	Schmitt-trigger inverter with totem-pole outputs
LS20	Dual 4-input NAND
LS21	Dual 4-input AND
LS22	Dual 4-input open-collector NAND
LS24	Quad 2-input Schmitt-trigger NAND
LS26	Quad 2-input NAND
LS27	Triple 3-input NOR
LS28	Quad 2-input NOR
LS30	8-input NAND
LS31	Delay element

LS32	Quad 2-input OR
LS33	Quad 2-input NOR
LS37	Quad 2-input NAND buffer
LS38	Quad 2-input open-collector NAND buffer
LS40	Dual 4-input NAND
LS42	4-to-10-line decoder
LS47	BCD-to-7-segment decoder/driver
LS48	BCD-to-7-segment decoder/driver
LS51	2-wide 3-input, 2-wide 2-input AND-OR-invert
LS54	4-wide AND-OR-invert
LS55	2-wide 4-input AND-OR-invert
LS73	Dual JK flip-flops with clear
LS74	Dual positive-edge-triggered D flip-flop
LS75	4-bit bistable latch
LS76	Dual JK flip-flop with preset and clear
LS78	Dual JK flip-flop with common clock and clear
LS83	4-bit binary full-adders with fast carry
LS85	4-bit magnitude comparator
LS86	Quad 2-input exclusive-OR
LS90	Decade counter
LS91	8-bit shift register
LS92	4-bit divide-by-12 counter
LS93	4-bit binary counter
LS95	4-bit shift register
LS96	5-bit shift register

LS107	Dual JK flip-flops with clear
LS109	Dual JKbar positive-edge-triggered flip-flop
LS112	Dual JK negative-edge-triggered flip-flop
LS113	Dual JK negative-edge-triggered flip-flop with preset
LS114	Dual JK negative-edge-triggered flip-flop with preset, common clear, and clock
LS122	Retriggerable monostable multivibrator with clear
LS123	Dual retriggerable monostable multivibrators with clear
LS125	Quad bus buffers with three-state outputs
LS126	Quad bus buffers with three-state outputs
LS132	Quad 2-input positive-NAND Schmitt triggers
LS133	13-input positive-NAND gate
LS136	Quad 2-input exclusive-OR
LS137	3-to-8 line decoders/multiplexers with address latch
LS138	3-to-8 line decoders/multiplexers
LS139	Dual 2-to-4 line decoders/multiplexers
LS145	BCD-to-decimal decoders/drivers for lamps, relays, MOS
LS147	10-line decimal to 4-line BCD priority encoder
LS148	8-line to 3-line octal priority encoder
LS151	1-of-8 data selectors/multiplexers
LS152	1-of-8 data selectors/multiplexers

LS153	Dual 4-to-1-line data multiplexer
LS154	4-to-16 line decoders/demultiplexers
LS155	Decoder/demultiplexer
LS156	Decoder/demultiplexer
LS157	Quad 2-to-1-line non-inverting multiplexer
LS158	Quad 2-to-1-line inverting data multiplexer
LS160	4-bit synchronous decade counters with direct clear
LS161	4-bit synchronous binary counters with direct clear
LS162	4-bit synchronous decade counters with synchronous clear
LS163	4-bit synchronous binary counters with synchronous clear
LS164	8-bit parallel output serial shift register
LS165	Parallel-load 8-bit shift registers
LS166	8-bit shift registers
LS169	4-bit synchronous binary up/down counters
LS170	4 by 4 register files
LS173	4-bit D-type registers with 3-state outputs
LS174	Hex D-type flip-flops
LS175	Quad D-type flip-flops
LS181	Arithmetic logic units/function generators
LS182	Look-ahead carry generators
LS183	Dual carry-save full adders
LS189	64-bit random-access memory
LS190	Synchronous BCD up/down counter
LS191	Synchronous binary up/down counter
LS192	Synchronous BCD up/down dual clock counters

LS193	Synchronous binary up/down dual clock counters
LS194A	4-bit bidirectional shift register
LS195	4-bit parallel-access shift registers
LS196	Presettable decade/bi-quinary counters/latches
LS197	Presettable binary counters/latches
LS219	64-bit random access memory
LS221	Dual monostable multivibrators
LS222	16 x 4 asynchronous first-in first-out memories
LS224	64-bit FIFO memories
LS227	64-bit FIFO memories
LS228	64-bit FIFO memories
LS240	Octal inverting 3-state bus transceiver
LS241	Octal non-inverting 3-state bus transceiver
LS242	Quad inverting 3-state bus transceiver
LS243	Quad non-inverting 3-state bus transceiver
LS244	Octal non-inverting 3-state bus transceiver
LS245	Octal non-inverting 3-state bus transceiver
LS247	BCD-to-7-segment decoder/driver with ripple blanking
LS248	BCD-to-7-segment decoder/driver with internal pull-up
LS249	BCD-to-7-segment decoder/driver with open collector
LS251	3-state data multiplexer
LS253	Dual data selectors/multiplexers
LS257	Quad 3-state non-inverting data multiplexer
LS258	Quad 3-state inverting data multiplexer
LS259	8-bit addressable latches

LS260	Dual 5-input NOR
LS261	2-bit by 4-bit parallel binary multiplier
LS266	Quad 2-input exclusive-NOR gates with open collector
LS273	Octal D-type flip-flops
LS279	Quad SR latches
LS280	9-bit odd/even parity generators/checkers
LS283	4-bit binary full adders
LS290	Decade counter
LS293	4-bit binary counter
LS295	4-bit bidirectional universal shift register
LS298	Quad 2-input multiplexers with storage
LS299	8-bit bidirectional 3-state shift/storage register
LS321	Crystal-controlled oscillator
LS322	8-bit shift register with sign extend
LS323	8-bit bidirectional universal shift/storage registers with 3-state outputs
LS347	BCD-to-7-segment decoder/driver with open collector
LS348	8-line to 3-line priority encoder
LS352	Dual 4-line to 1-line data selector/multiplexer
LS353	Dual 4-line to 1-line data selectors/multiplexers
LS354	8-line to 1-line data selector/multiplexer/ transparent registers

LS355	8-line to 1-line data selector/multiplexer/ transparent registers with open collectors
LS356	8-line to 1-line data selector/multiplexer/ edge-trigger registers
LS357	8-line to 1-line data selector/multiplexer/ edge-trigger registers with open collectors
LS363	Hex bus drivers
LS364	Hex bus drivers
LS365	Hex non-inverted 3-state bus drivers
LS366	Hex inverted 3-state bus drivers
LS367	Hex bus drivers
LS368	Hex bus drivers
LS373	Octal 3-state D-latch with common enable
LS374	Octal 3-state positive-edge-triggered D register
LS375	4-bit bistable latches
LS377	Octal D-type flip-flops with enable
LS378	Hex D-type flip-flops
LS379	Quad D-type flip-flops with enable
LS381	Arithmetic logic unit/function generator
LS382	Arithmetic logic unit/function generator
LS385	Quad serial adders/subtractors
LS386	Quad 2-input exclusive-OR gates
LS390	Dual decade counters
LS393	Dual 4-bit binary counters
LS395A	4-bit universal shift register
LS396	Octal storage register
LS398	Quad 2-input multiplexer with storage
LS399	Quad 2-input multiplexer with storage

LS422	Retriggerable monostable multivibrators
LS423	Retriggerable monostable multivibrators
LS445	BCD-to-decimal decoder/driver
LS446	Quad bus transceivers with direction control
LS447	BCD-to-7-segment decoder/driver
LS448	Quad tridirectional bus transceivers with open collectors
LS449	Quad bus transceivers with direction control
LS465	Octal buffers with three-state outputs
LS466	Octal buffers with three-state outputs
LS467	Octal buffers with three-state outputs
LS468	Octal buffers with three-state outputs
LS490	Dual decade counters
LS533	8-bit latch with inverting outputs
LS534	8-bit register with inverting outputs
LS540	Octal buffers and line drivers with 3-state outputs
LS541	Octal buffers and line drivers with 3-state outputs
LS569	4-bit up/down counters with 3-state outputs
LS590	8-bit binary counters with output registers
LS591	8-bit binary counter with output registers with open collectors
LS592	8-bit binary counter with input registers
LS593	8-bit binary counter with input registers
LS595	8-bit shift register with output latches
LS596	8-bit shift register with output latches with open collectors
LS597	8-bit shift register with input latches
LS598	8-bit shift register with input latches

LS604	Octal 3-state 2-input multiplexed register
LS605	Octal open collector 2-input multiplexed register
LS606	Octal 3-state 2-input multiplexed register
LS607	Octal open collector 2-input multiplexed register
LS620	Octal bus transceiver with 3-state outputs
LS621	Octal bus transceiver with open collector
LS622	Octal bus transceiver with open collector
LS623	Octal bus transceiver with 3-state outputs
LS624	Voltage-controlled oscillator
LS625	Voltage-controlled oscillator
LS626	Voltage-controlled oscillator
LS627	Voltage-controlled oscillator
LS628	Voltage-controlled oscillator
LS629	Dual voltage-controlled oscillator
LS640	Octal 3-state inverting bus transceiver
LS641	Octal open-collector non-inverting bus transceiver
LS642	Octal open collector inverting bus transceiver
LS645	Octal 3-state non-inverting bus transceiver
LS652	Octal 3-state bus transceiver and register
LS668	Synchronous 4-bit up/down counters
LS669	Synchronous 4-bit up/down counters
LS670	4 x 4 register files with 3-state outputs
LS671	4-bit 3-state universal shift register/latch
LS672	4-bit 3-state universal shift register/latch
LS674	16-bit shift registers

LS684	8-bit magnitude comparators
LS693	Synchronous counters with output registers and multiplexed 3-state outputs
LS699	Synchronous up/down counters with output registers and multiplexed 3-state outputs
LS793	8-bit latch/register with readback

Application Notes

Monostable Multivibrators

The LS122, LS123, LS221, LS422, and LS423 models fully support the simulation and timing behavior of a retrigerrable multivibrator – infinite retriggering edges and external resettability at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

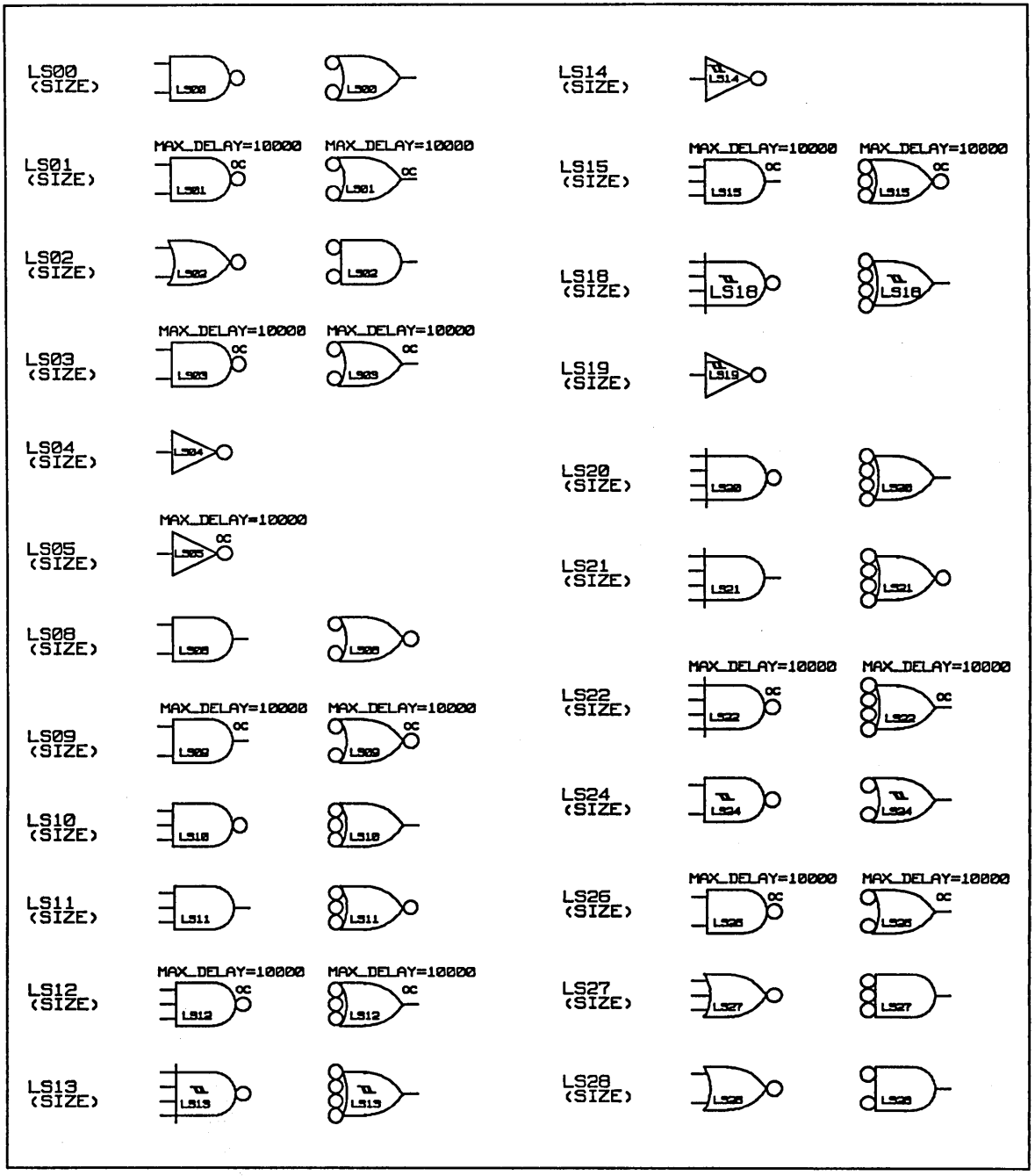
  ```
  LATCH_ERR_MODEL CLOSED;
  ```

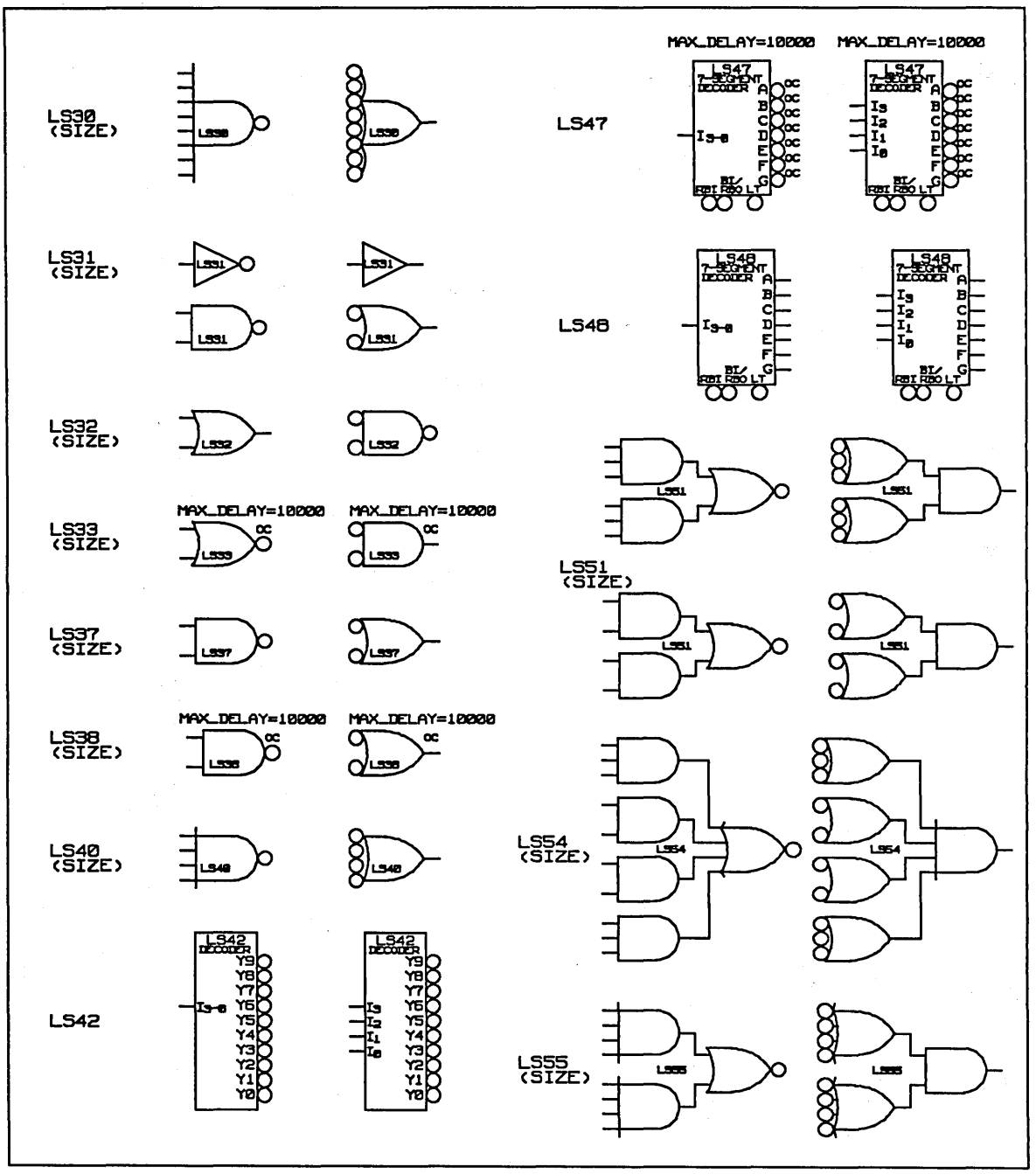
- The first trigger edge must occur after 'PULSE_WIDTH' ns.

- The maximum trigger frequency is

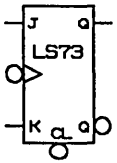
  ```
  2 * RETRIG_DIV2 -1
  ```

  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6-1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.

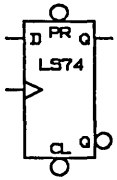

LS00 (SIZE)
LS01 (SIZE)
LS02 (SIZE)
LS03 (SIZE)
LS04 (SIZE)
LS05 (SIZE)
LS08 (SIZE)
LS09 (SIZE)
LS10 (SIZE)
LS11 (SIZE)
LS12 (SIZE)
LS13 (SIZE)
LS14 (SIZE)
LS15 (SIZE)
LS18 (SIZE)
LS19 (SIZE)
LS20 (SIZE)
LS21 (SIZE)
LS22 (SIZE)
LS24 (SIZE)
LS26 (SIZE)
LS27 (SIZE)
LS28 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
OC


LS30
(SIZE)
LS31
(SIZE)
LS32
(SIZE)
LS33
(SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
LS37
(SIZE)
LS38
(SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
LS40
(SIZE)
LS42
LS42
DECODER
I3-0
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
LS47
MAX_DELAY=10000
MAX_DELAY=10000
LS47
7-SEGMENT
DECODER
I3-0
A
B
C
D
E
F
G
BI/RBO
RBI
LT
LS48
LS48
LS51
(SIZE)
LS54
(SIZE)
LS55
(SIZE)

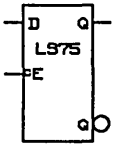
LS73
(SIZE)



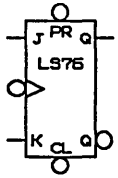
LS74
(SIZE)



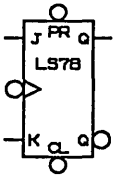
LS75
(SIZE)



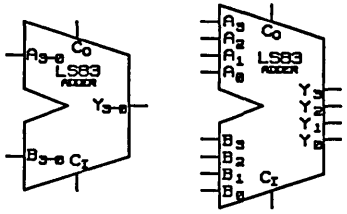
LS76
(SIZE)



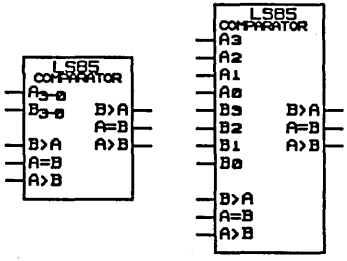
LS78
(SIZE)



LS83

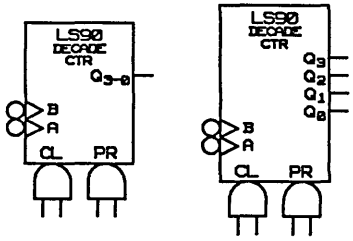


LS85

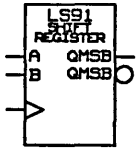


LS86
(SIZE)

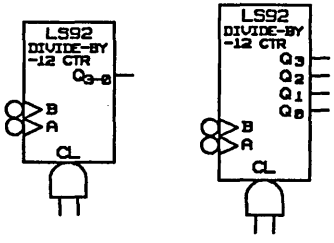
LS90



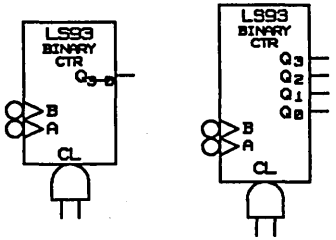
LS91



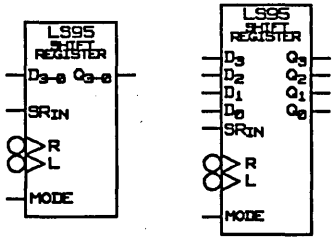
LS92



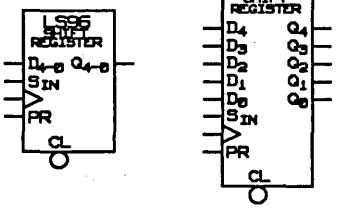
LS93



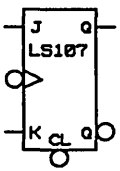
LS95



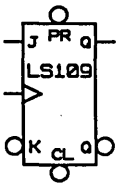
LS96



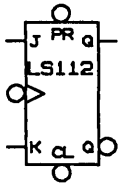
LS107
(SIZE)



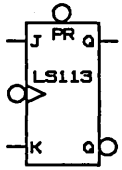
LS109
(SIZE)



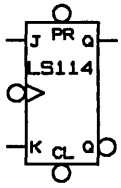
LS112
(SIZE)



LS113
(SIZE)

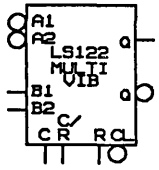


LS114
(SIZE)



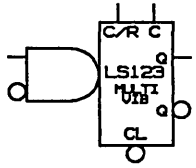
PULSE_WIDTH=10000

LS122

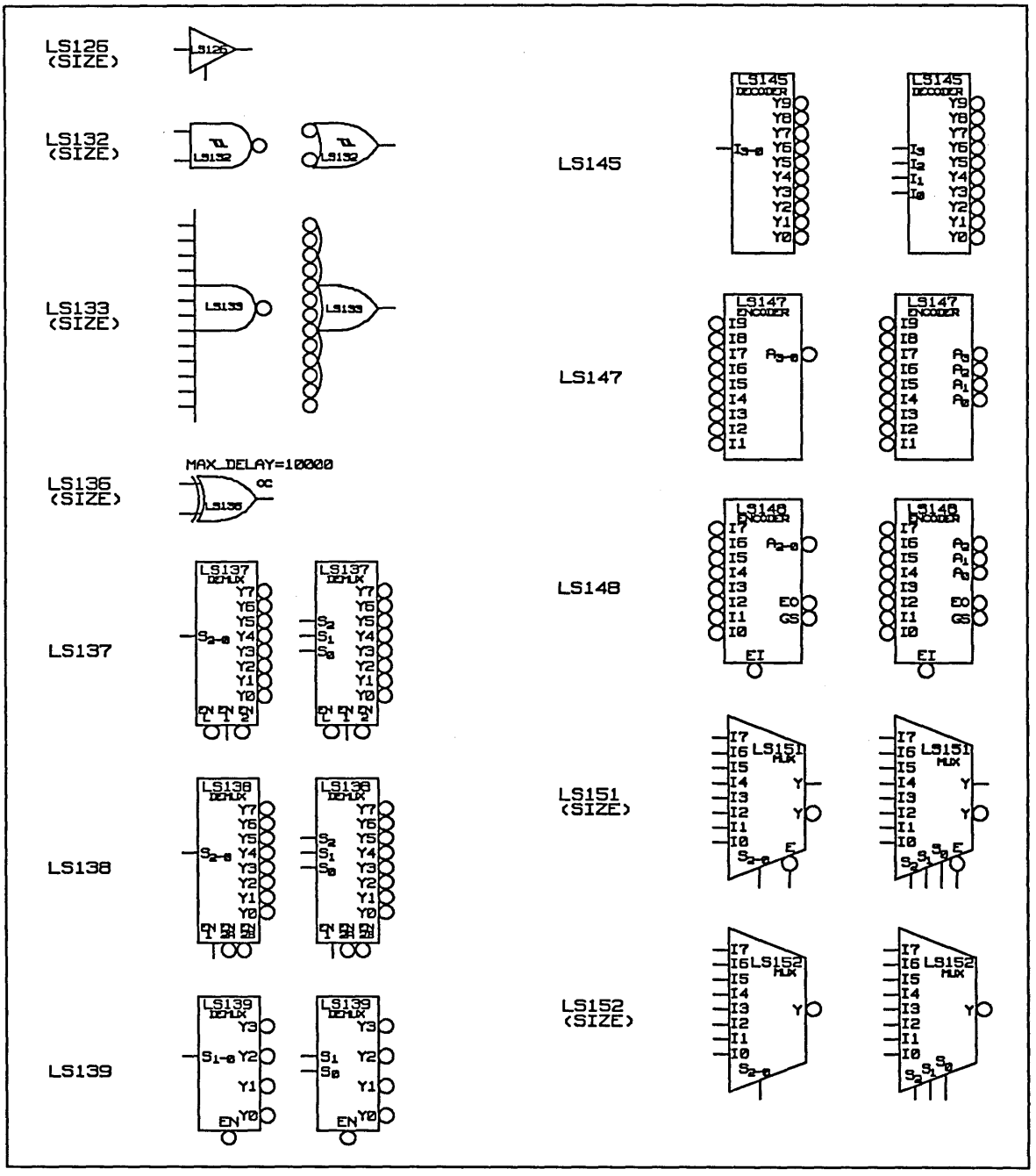


PULSE_WIDTH=10000

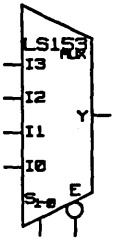
LS123

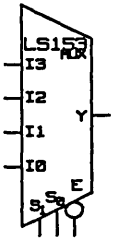


LS125
(SIZE)

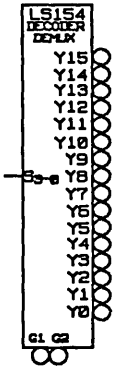

LS126
(SIZE)
LS132
(SIZE)
LS133
(SIZE)
LS136
(SIZE)
MAX_DELAY=10000
LS137
LS138
LS139
LS145
LS147
LS148
LS151
(SIZE)
LS152
(SIZE)

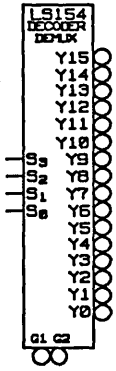
LS153
(SIZE)



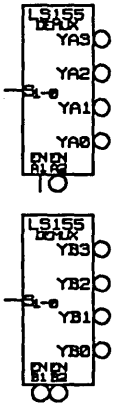


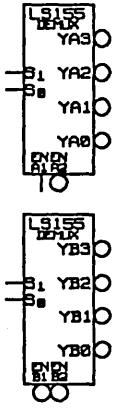
LS154





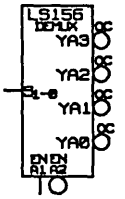
LS155



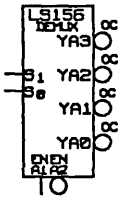


LS156

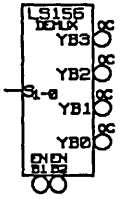
MAX_DELAY=10000



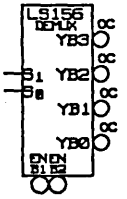
MAX_DELAY=10000



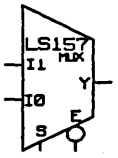
MAX_DELAY=10000

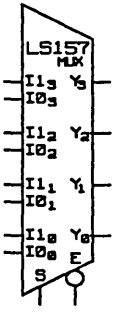


MAX_DELAY=10000

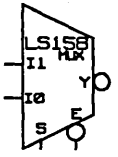


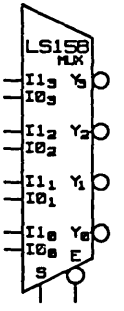
LS157
(SIZE)

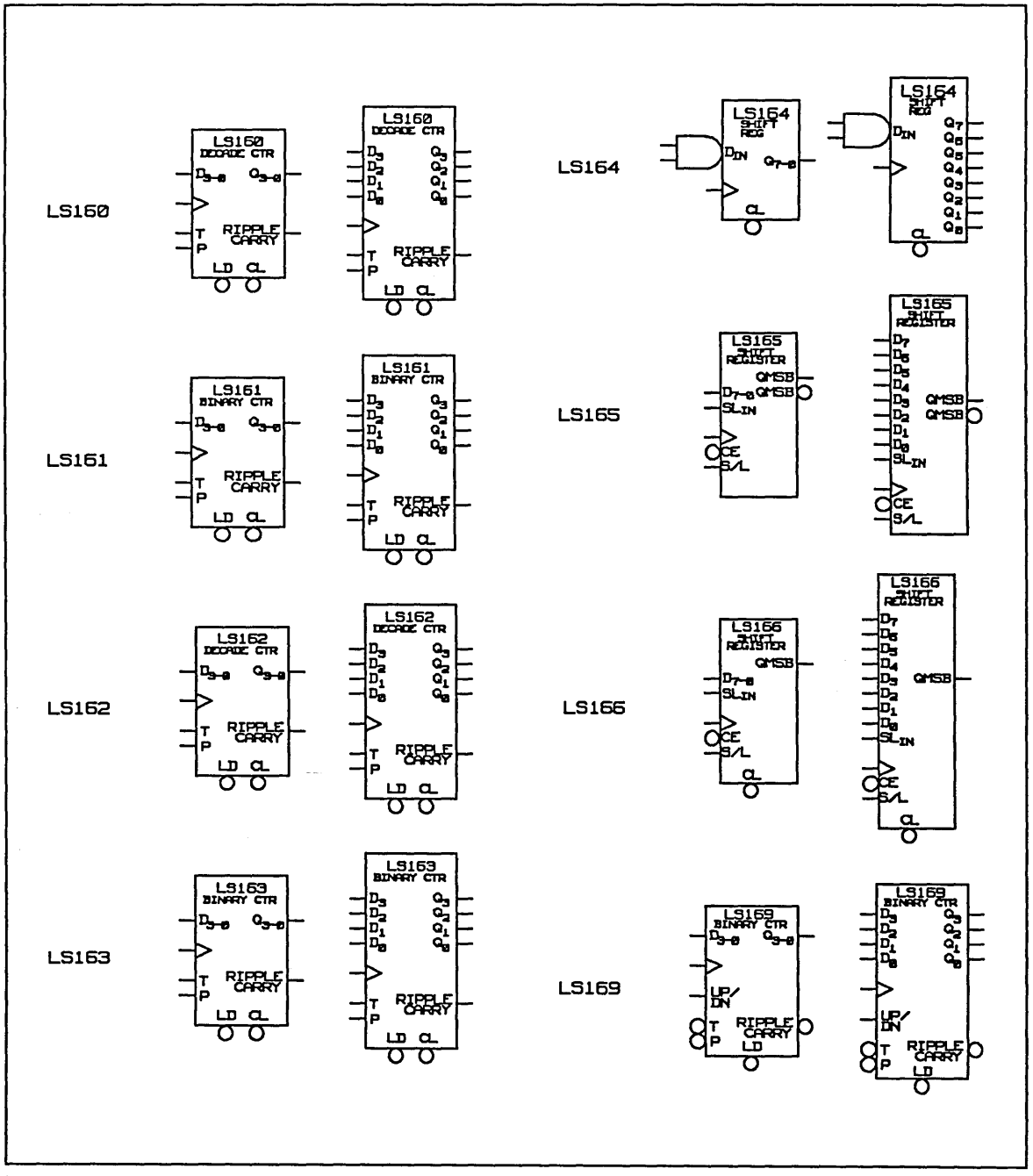


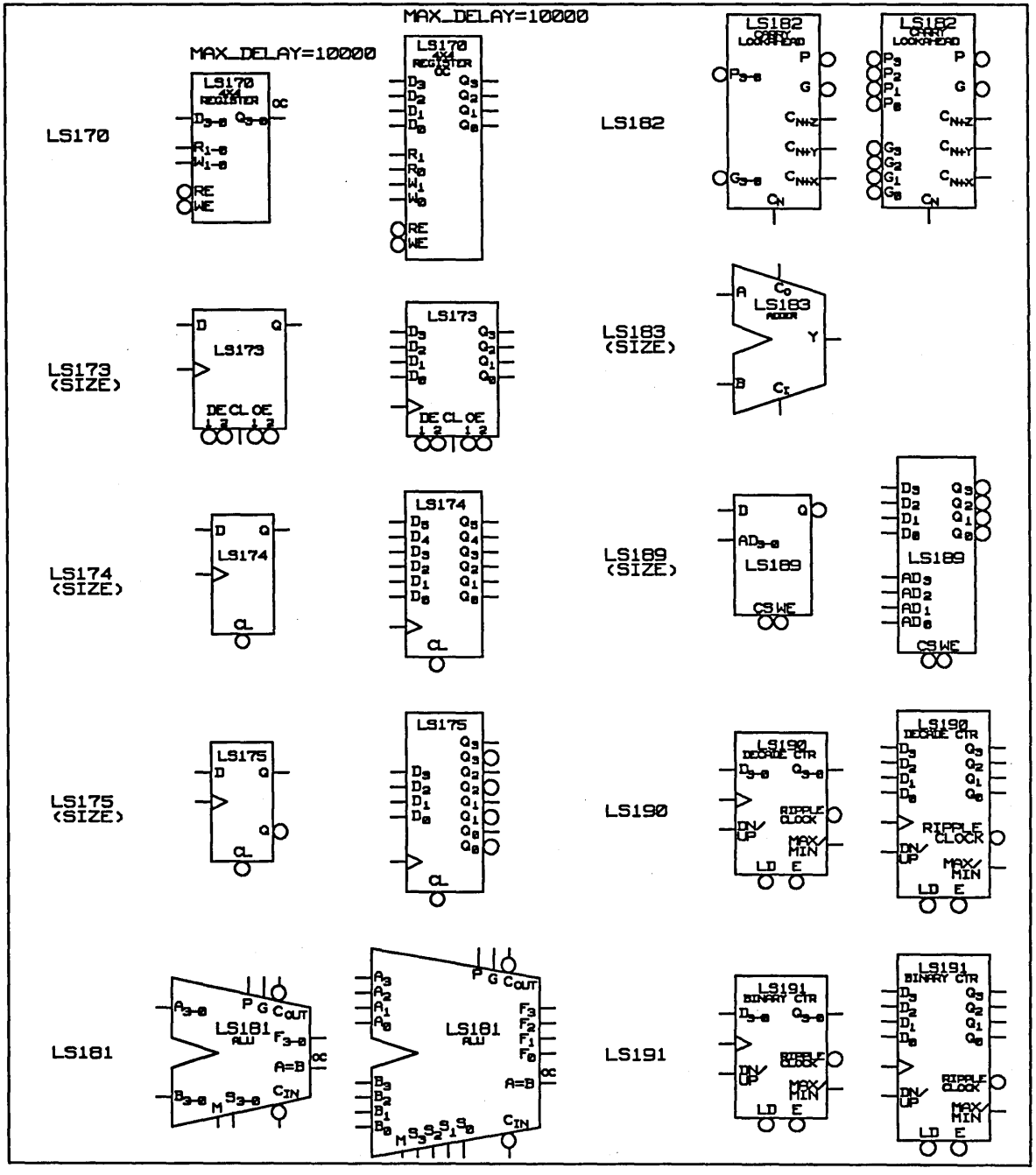


LS158
(SIZE)

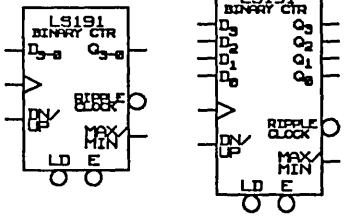




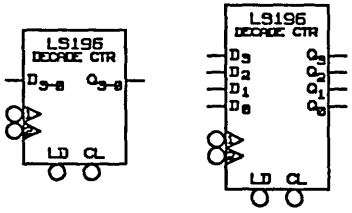

LS160
LS160
DECADE CTR
RIPPLE CARRY
LS161
LS161
BINARY CTR
RIPPLE CARRY
LS162
LS162
DECADE CTR
RIPPLE CARRY
LS163
LS163
BINARY CTR
RIPPLE CARRY
LS164
LS164
SHIFT REG
LS165
LS165
SHIFT REGISTER
LS166
LS166
SHIFT REGISTER
LS169
LS169
BINARY CTR
RIPPLE CARRY


MAX_DELAY=10000
LS170
LS170
LS182
LS173
(SIZE)
LS173
LS183
(SIZE)
LS174
(SIZE)
LS174
LS189
(SIZE)
LS175
(SIZE)
LS175
LS190
LS181
LS181
LS191

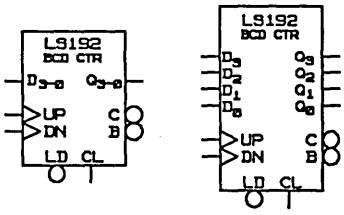
LS191



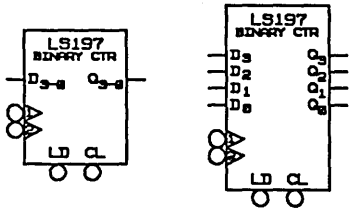
LS196



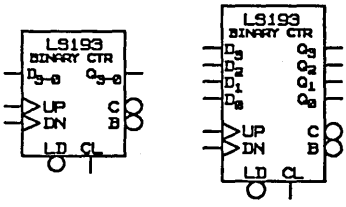
LS192



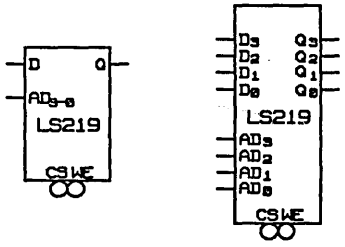
LS197



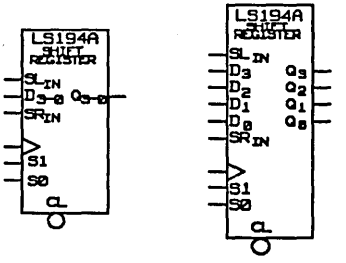
LS193



LS219
(SIZE)

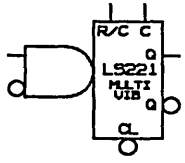


LS194A

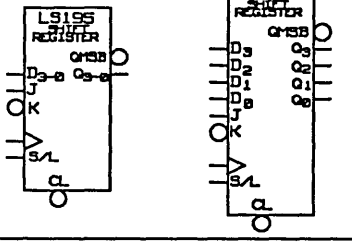


PULSE_WIDTH=10000

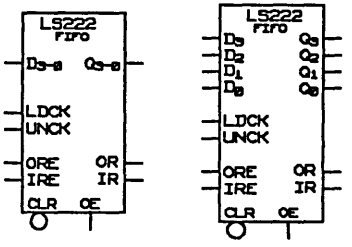
LS221



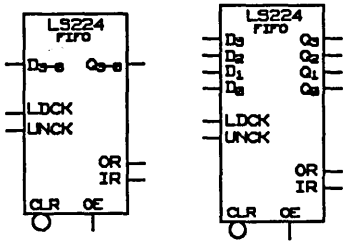
LS195



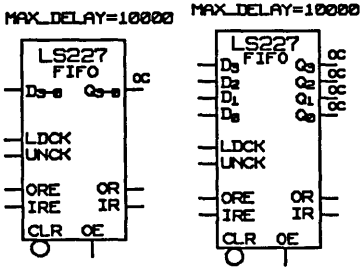
LS222



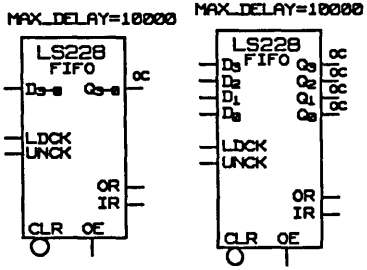
LS224



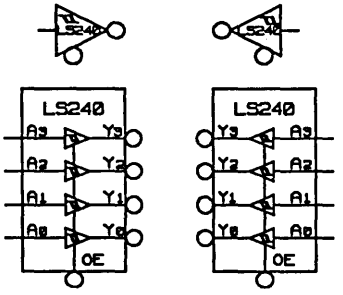
LS227



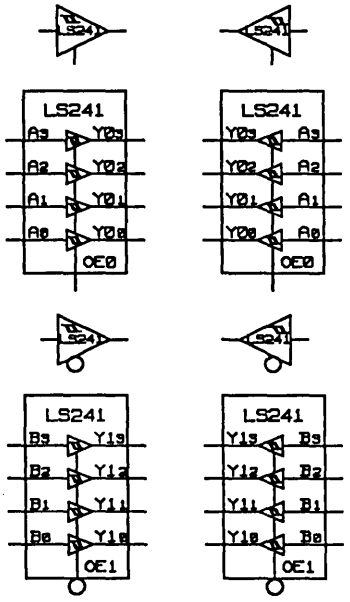
LS228



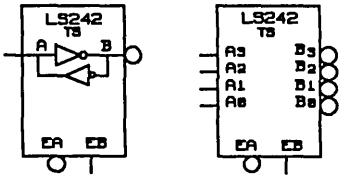
LS240
(SIZE)



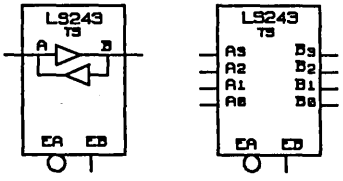
LS241
(SIZE)



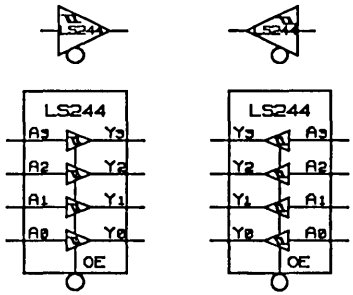
LS242
(SIZE)



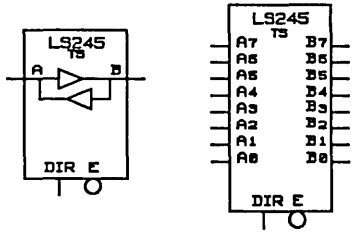
LS243
(SIZE)



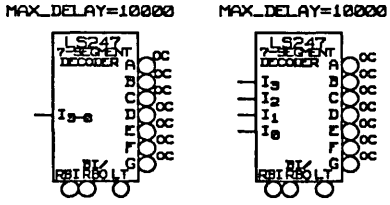
LS244 (SIZE)



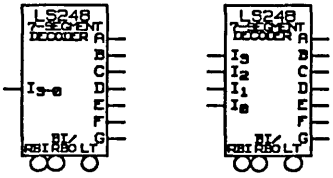
LS245 (SIZE)



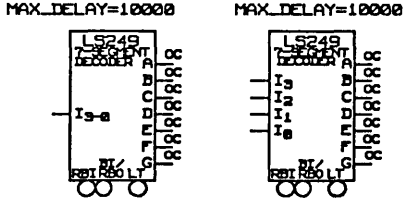
LS247



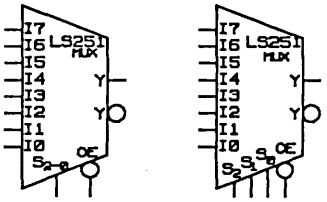
LS248



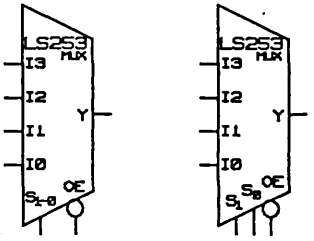
LS249



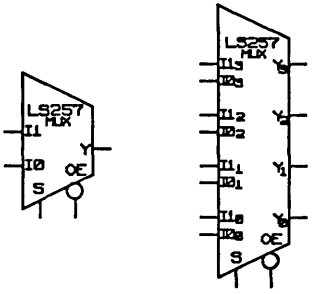
LS251 (SIZE)



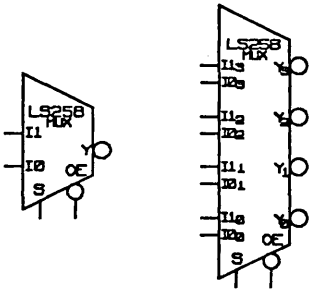
LS253 (SIZE)



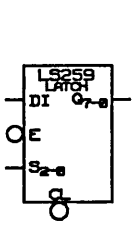
LS257 (SIZE)

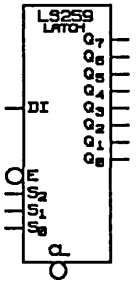


LS258 (SIZE)

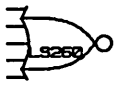


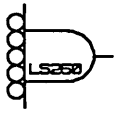
LS259



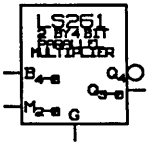


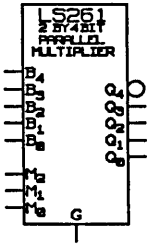
LS260
(SIZE)



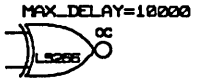


LS261

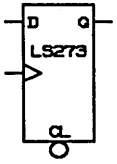


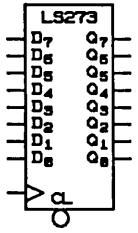


LS266
(SIZE)

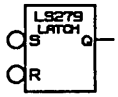


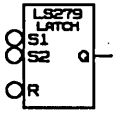
LS273
(SIZE)



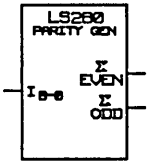


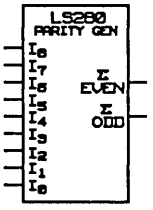
LS279
(SIZE)



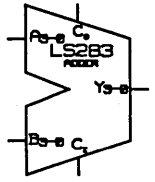


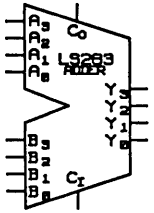
LS280



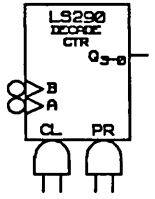


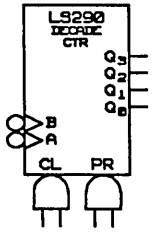
LS283



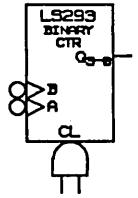


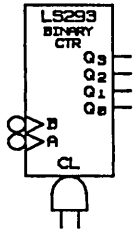
LS290



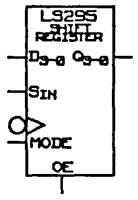


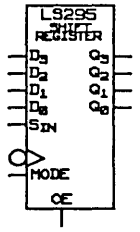
LS293



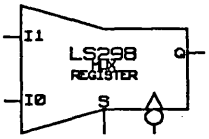


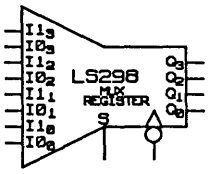
LS295



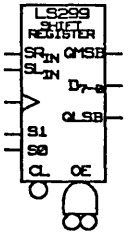


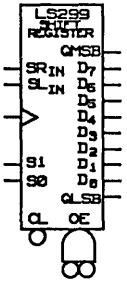
LS298
(SIZE)





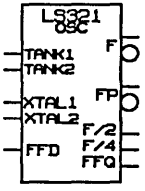
LS299



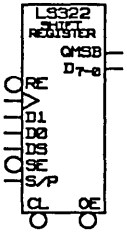


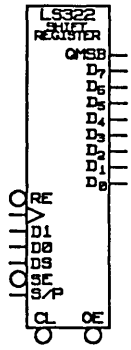
HALF_PERIOD=1000

LS321

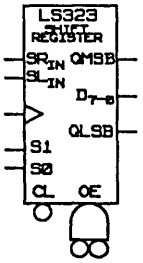


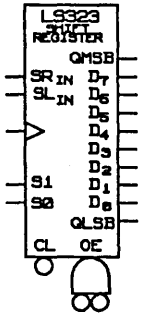
LS322





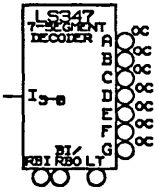
LS323



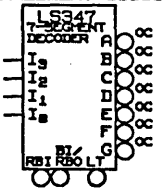


MAX_DELAY=10000

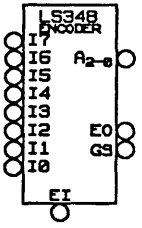
LS347

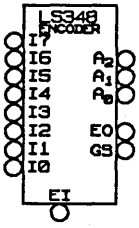


MAX_DELAY=10000

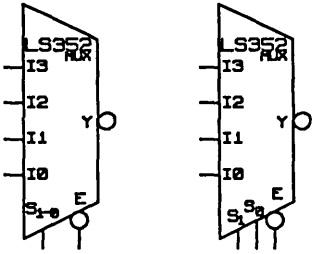


LS348

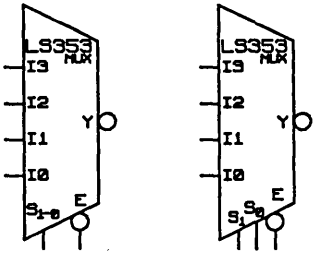




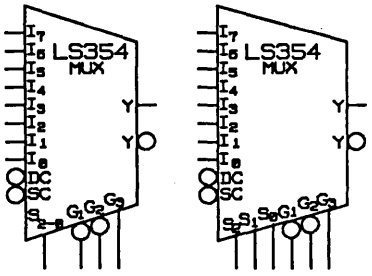
LS352 (SIZE)



LS353 (SIZE)



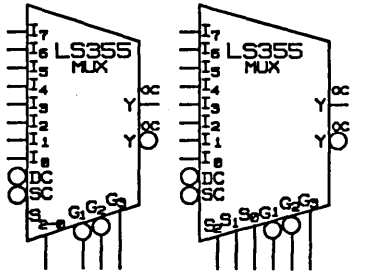
LS354 (SIZE)



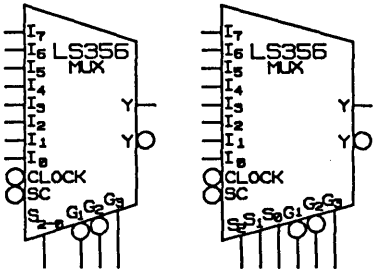
LS355 (SIZE)

MAX_DELAY=10000

MAX_DELAY=10000



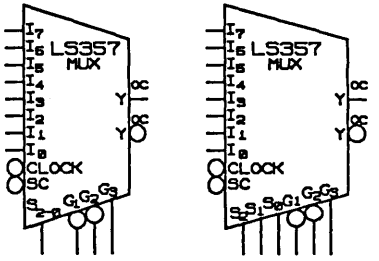
LS356 (SIZE)



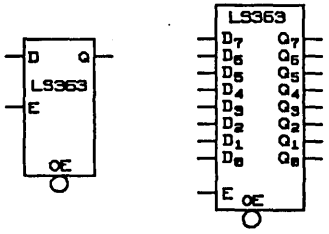
LS357 (SIZE)

MAX_DELAY=10000

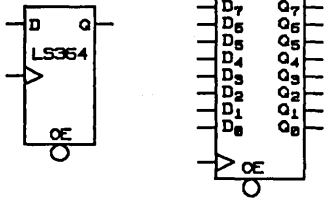
MAX_DELAY=10000

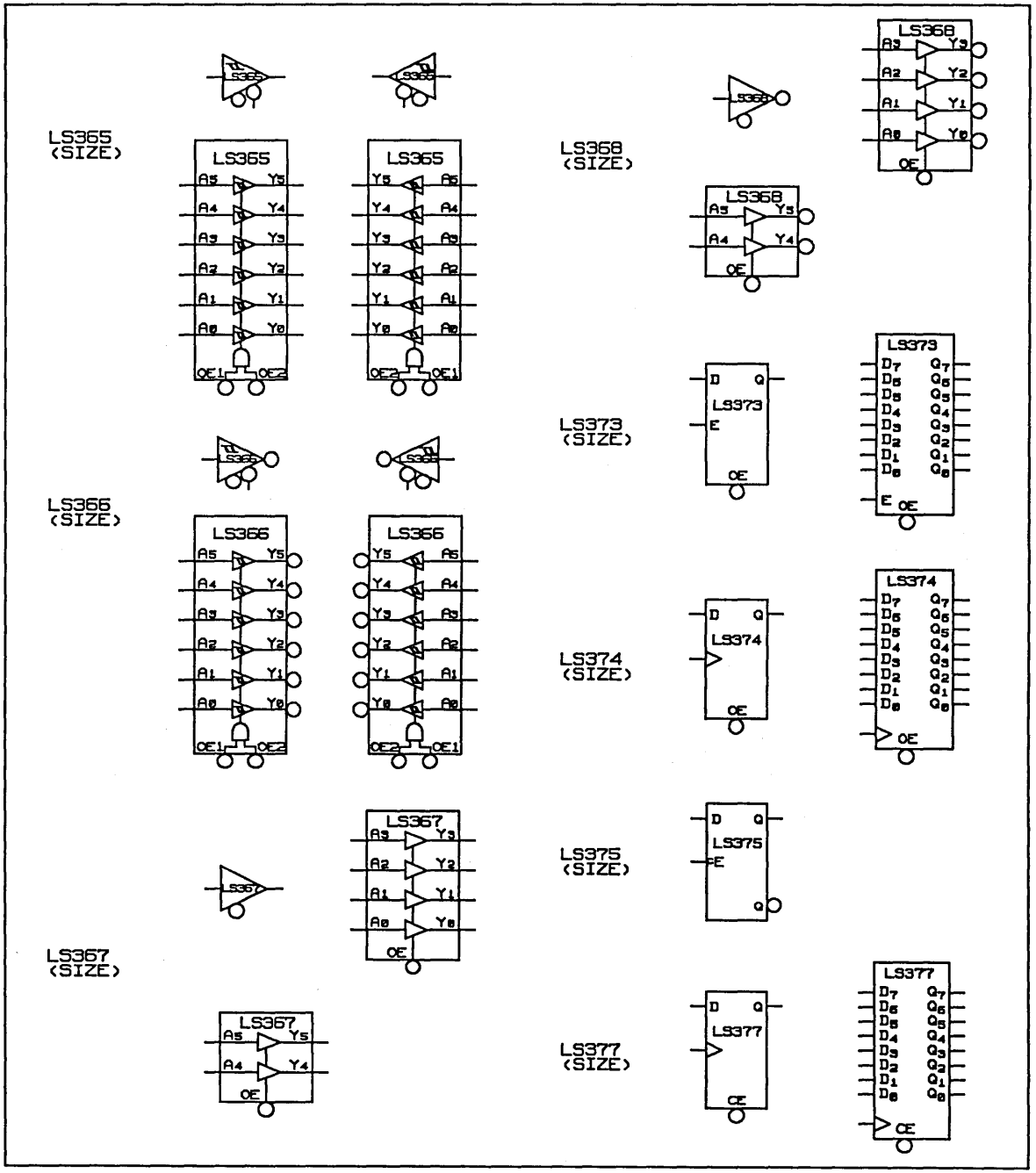


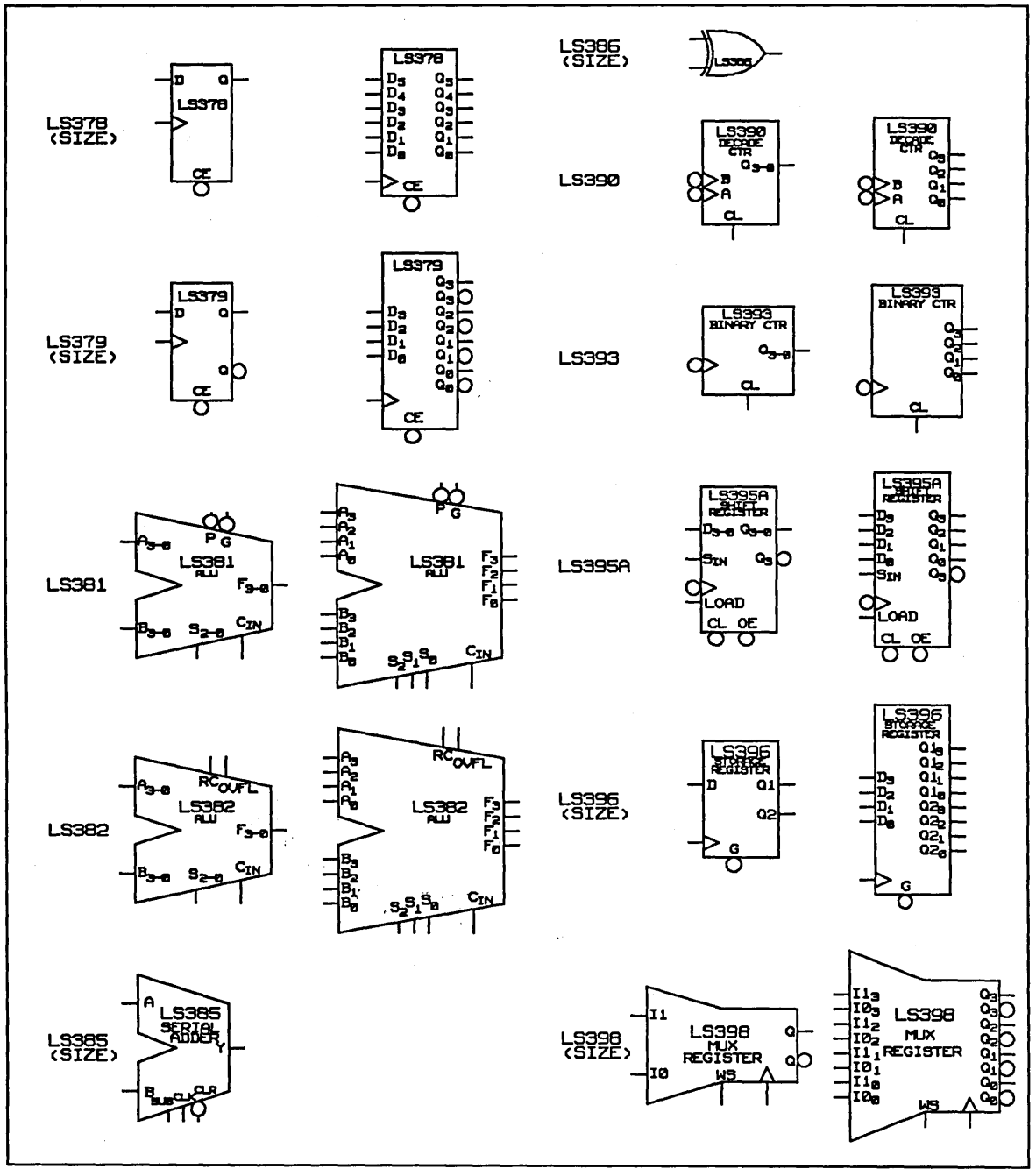
LS363 (SIZE)



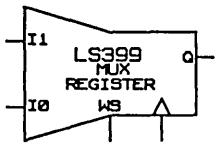
LS364 (SIZE)

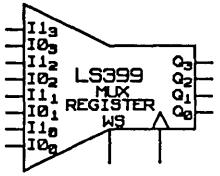



LS365
(SIZE)
LS366
(SIZE)
LS367
(SIZE)
LS368
(SIZE)
LS373
(SIZE)
LS374
(SIZE)
LS375
(SIZE)
LS377
(SIZE)
LS365
LS366
LS367
LS368
LS373
LS374
LS375
LS377

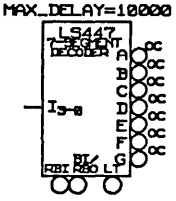

LS378
(SIZE)
LS378
LS379
(SIZE)
LS379
LS381
LS381
LS382
LS382
LS385
(SIZE)
LS385
SERIAL ADDER
LS386
(SIZE)
LS390
LS390
LS393
LS393
LS395A
LS395A
LS396
(SIZE)
LS396
LS398
(SIZE)
LS398
MUX REGISTER

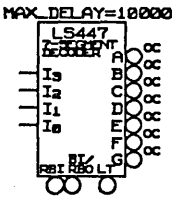
LS399 (SIZE)



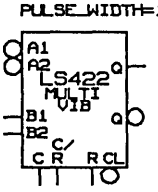


LS447

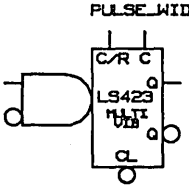




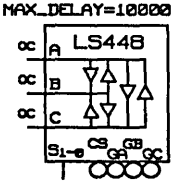
LS422

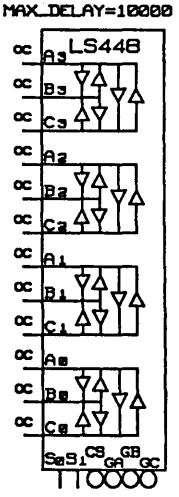


LS423

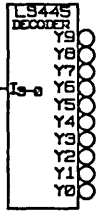


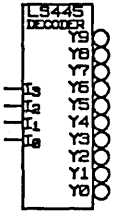
LS448 (SIZE)



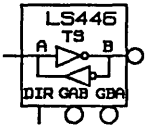


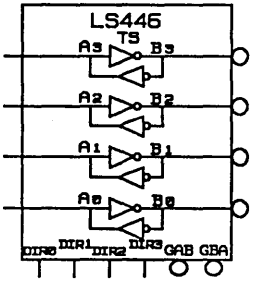
LS445



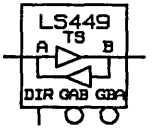


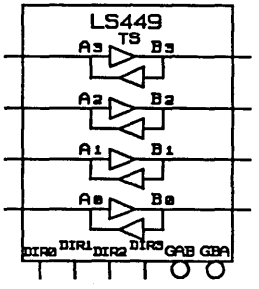
LS446 (SIZE)

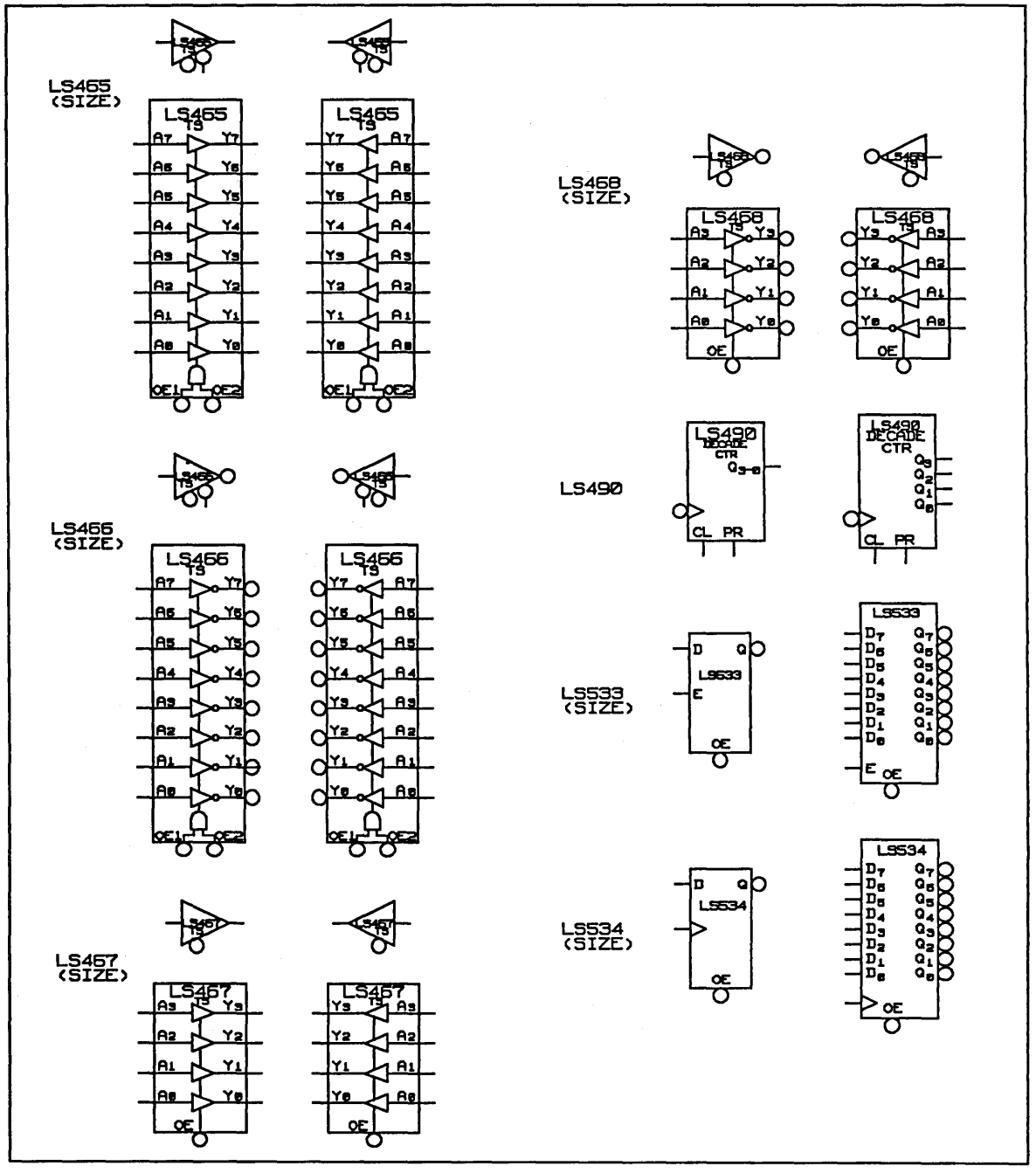


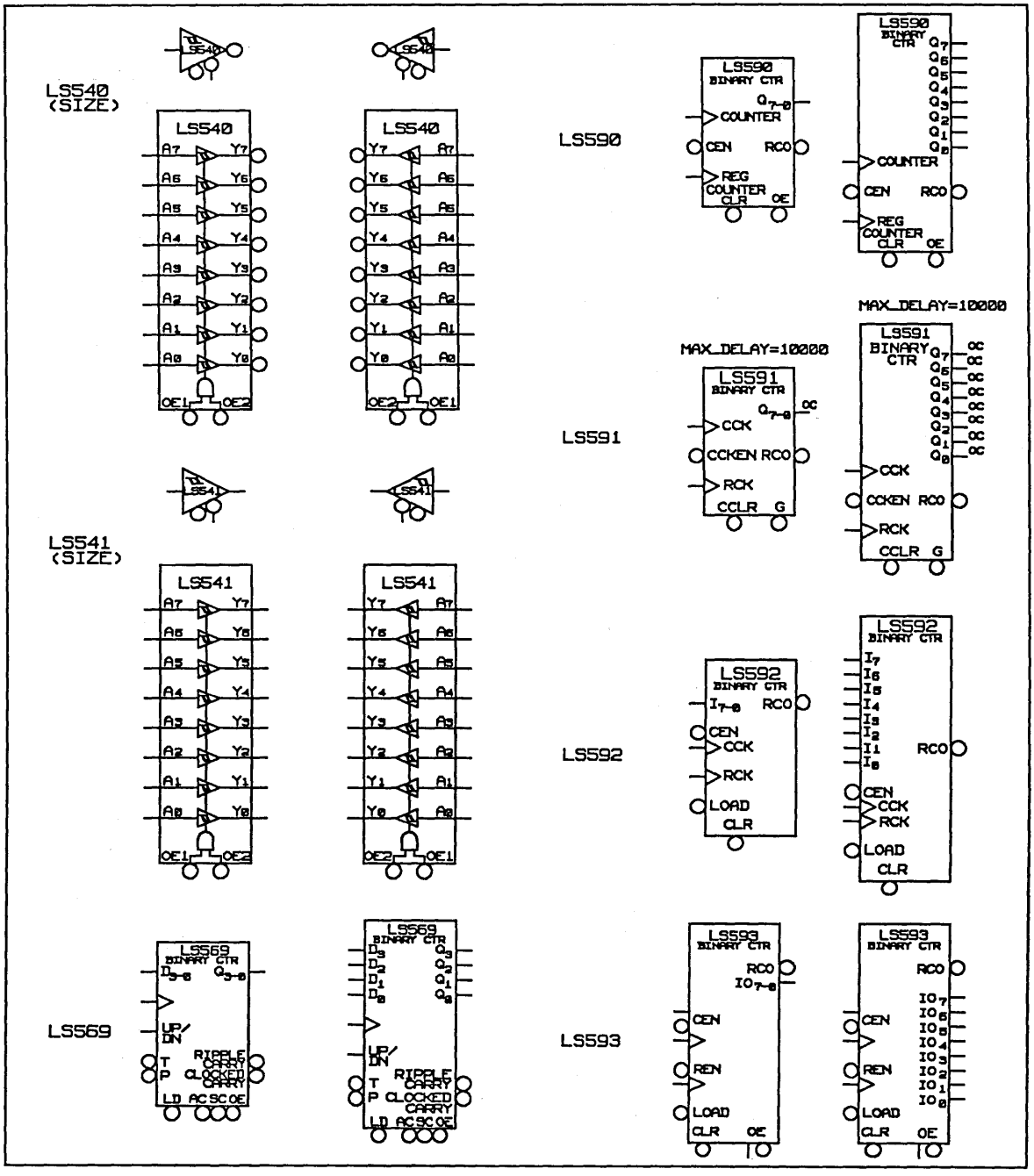


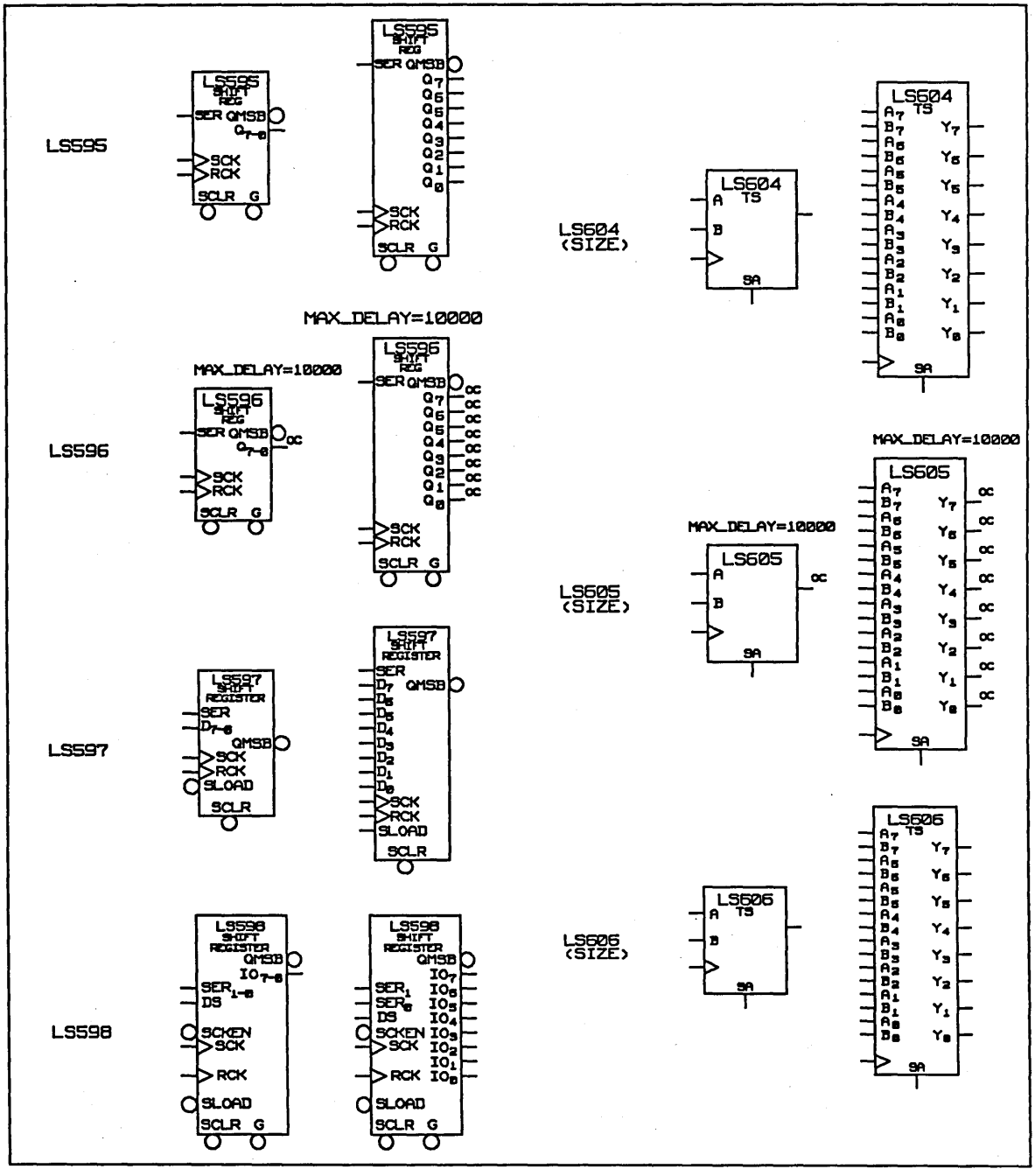
LS449 (SIZE)

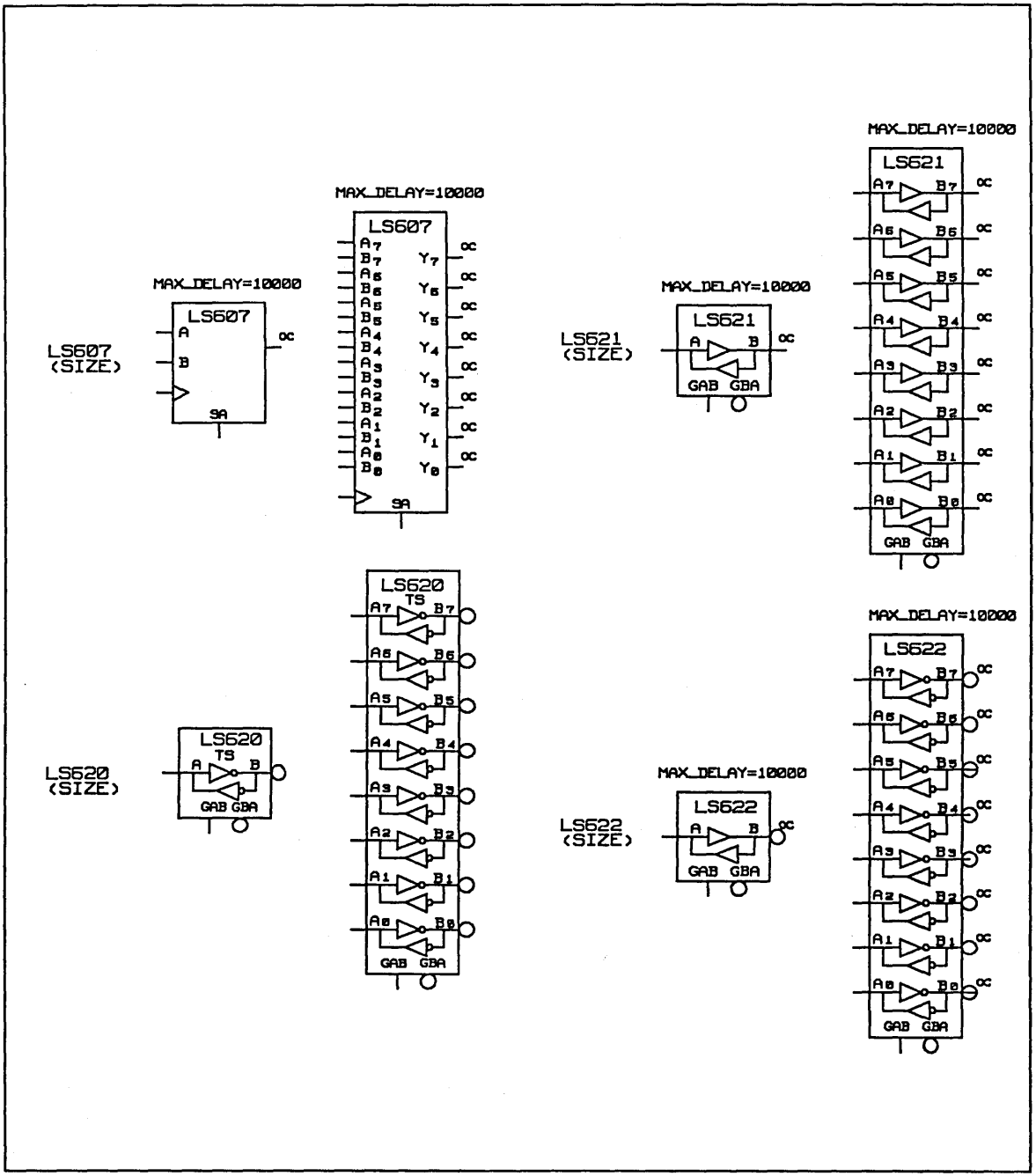


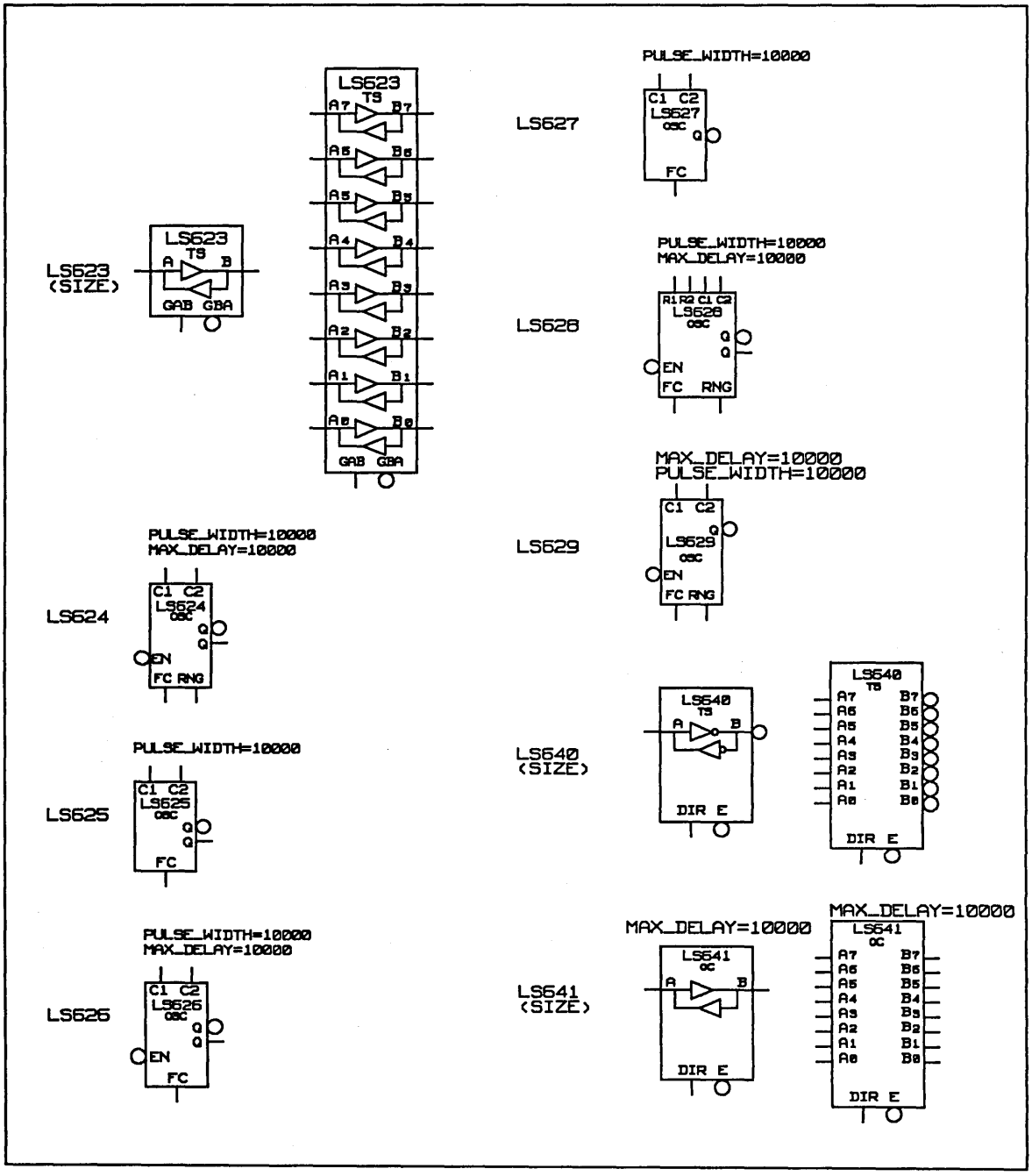


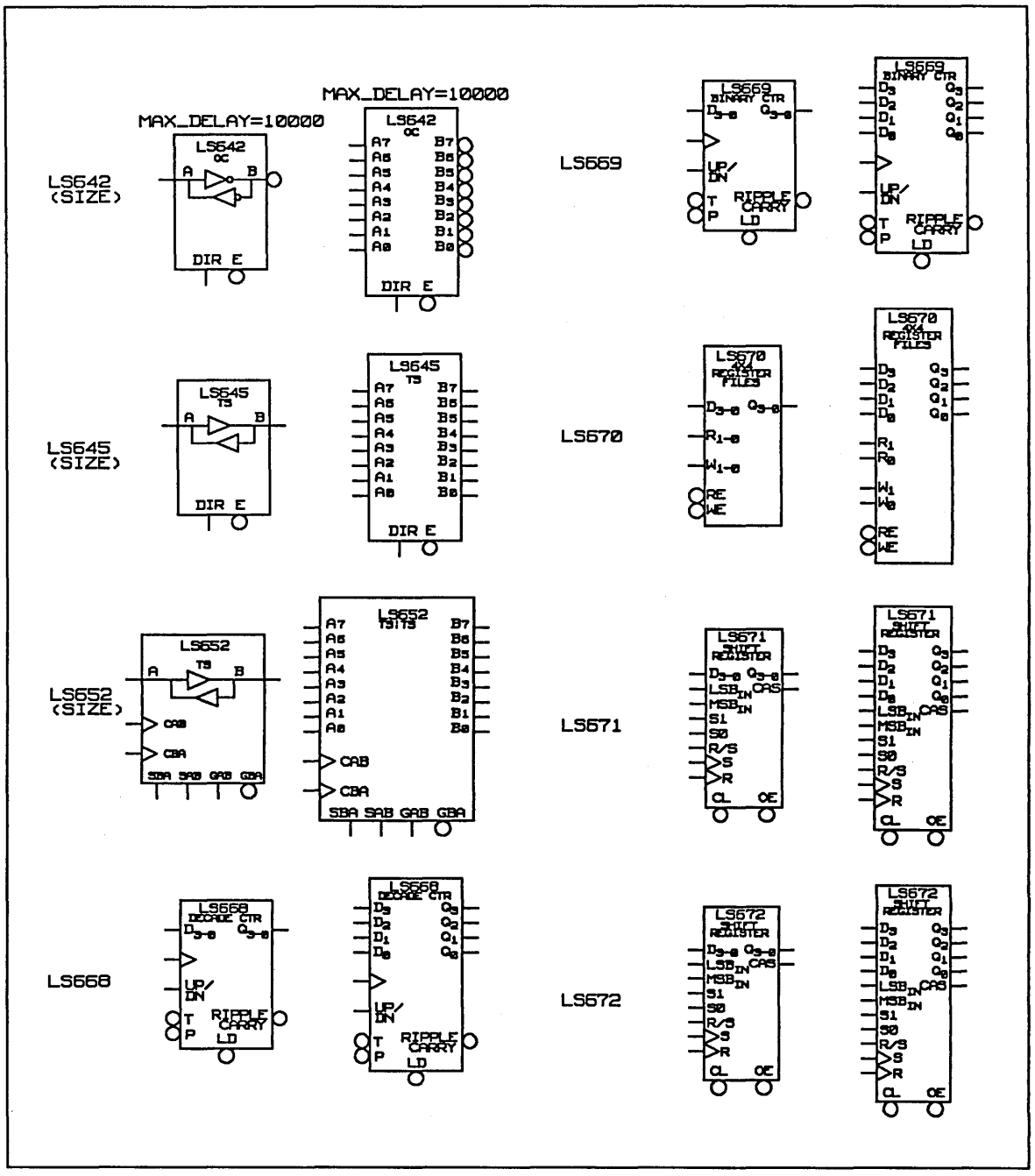

LS465
(SIZE)
LS466
(SIZE)
LS467
(SIZE)
LS468
(SIZE)
LS490
LS533
(SIZE)
LS534
(SIZE)
LS490
DECADE
CTR
LS533
LS534

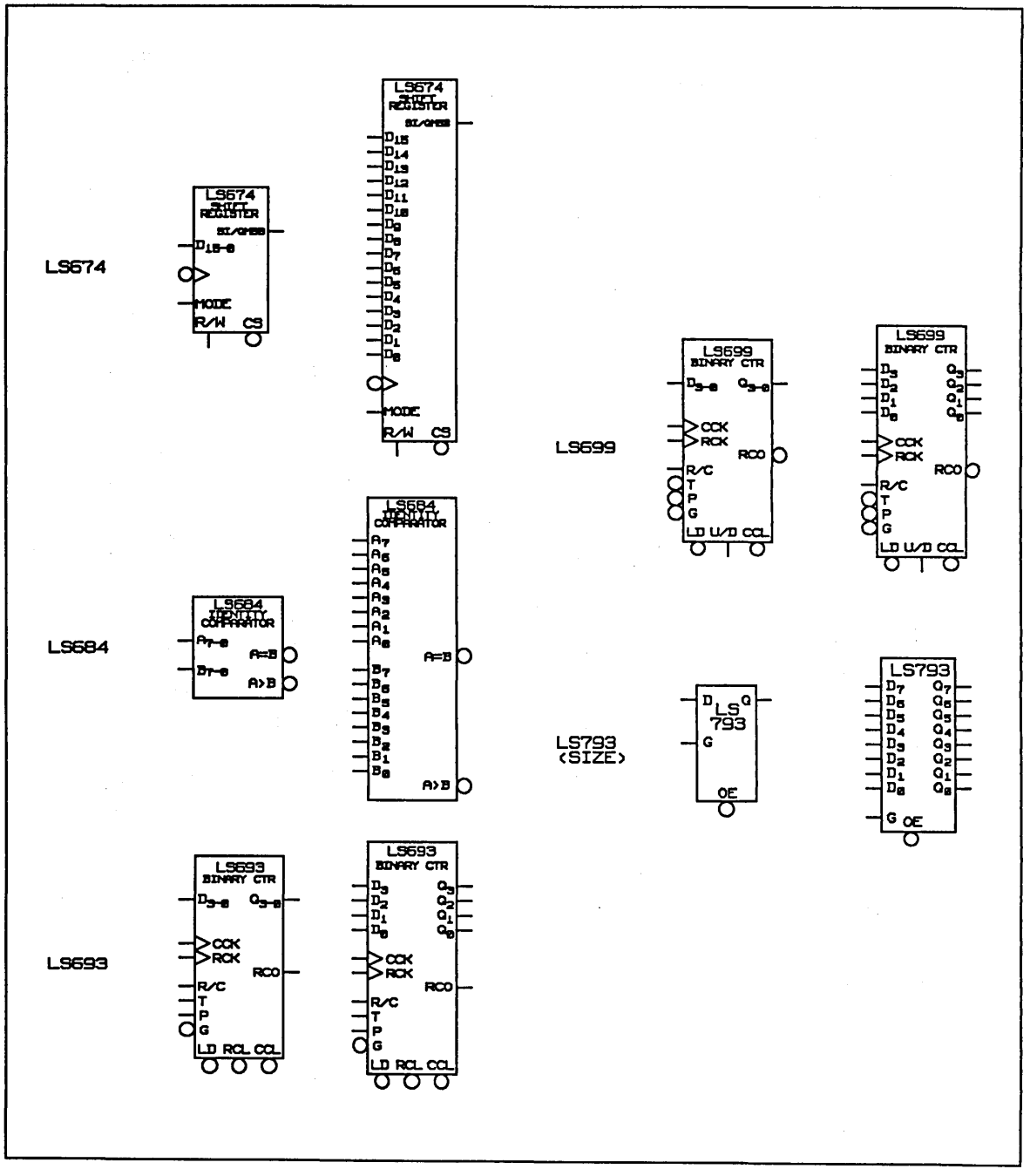

LS540
(SIZE)
LS540
LS540
LS590
LS590
LS590
LS591
LS591
MAX_DELAY=10000
MAX_DELAY=10000
LS541
(SIZE)
LS541
LS541
LS592
LS592
LS569
LS569
LS593
LS593

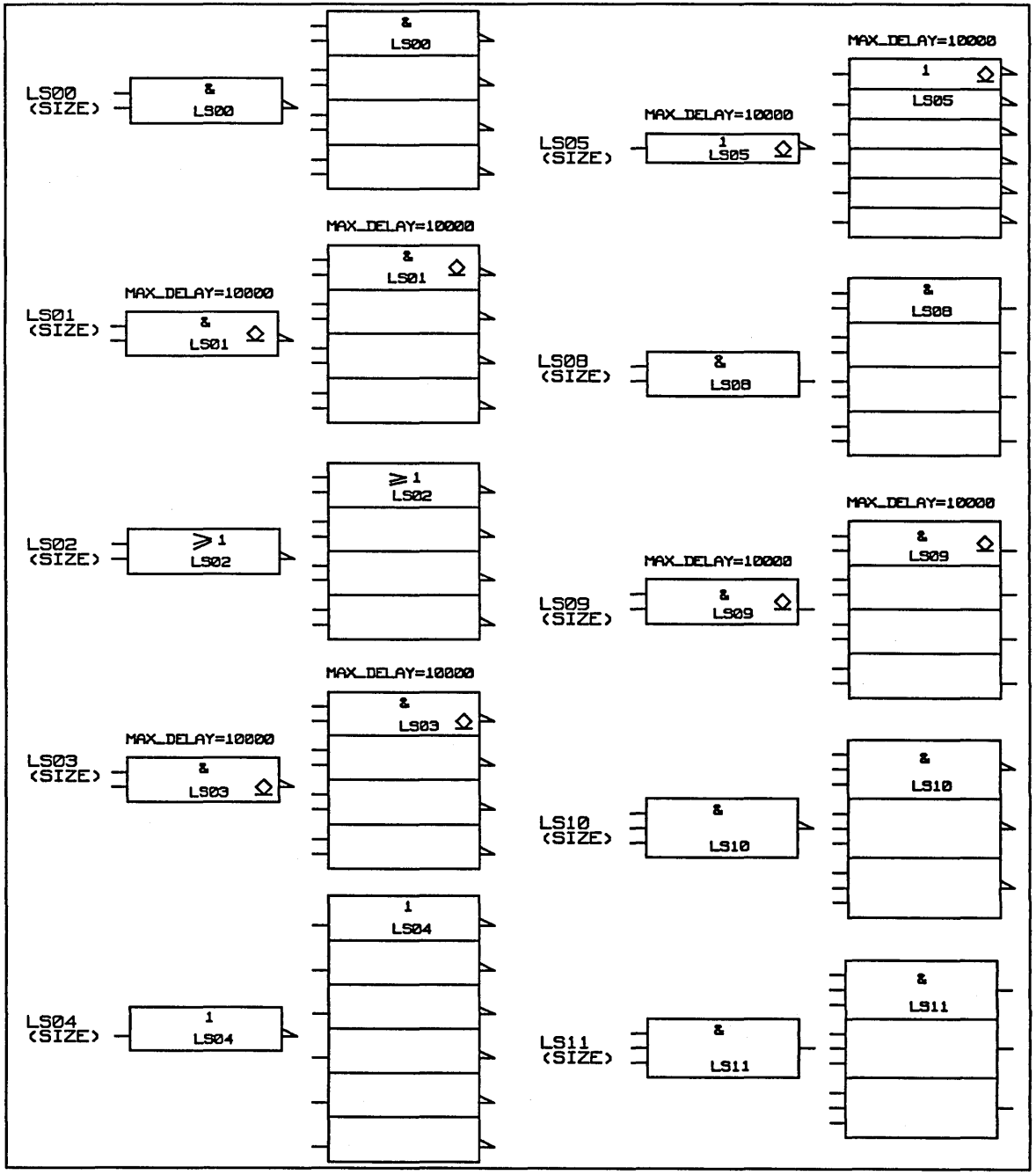

LS595
LS596
LS597
LS598
MAX_DELAY=10000
LS604
(SIZE)
LS605
(SIZE)
LS606
(SIZE)

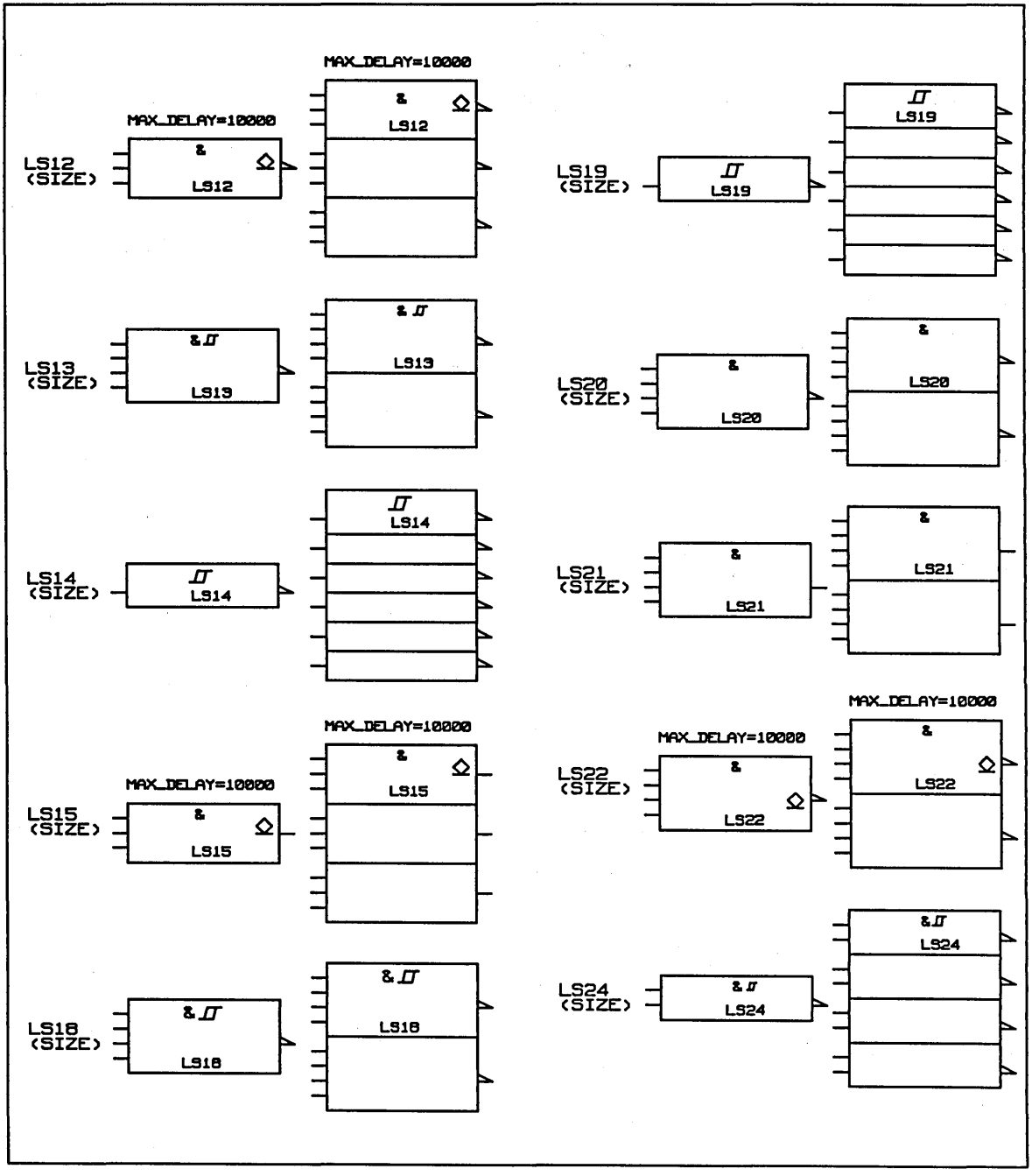

LS607
(SIZE)
MAX_DELAY=10000
LS607
A
B
OC
SA
MAX_DELAY=10000
LS607
A7 B7 A6 B6 A5 B5 A4 B4 A3 B3 A2 B2 A1 B1 A0 B0
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
OC
SA
LS621
(SIZE)
MAX_DELAY=10000
LS621
A
B
OC
GAB GBA
MAX_DELAY=10000
LS621
A7 B7 A6 B6 A5 B5 A4 B4 A3 B3 A2 B2 A1 B1 A0 B0
OC
GAB GBA
LS620
(SIZE)
LS620
TS
A
B
GAB GBA
LS620
TS
A7 B7 A6 B6 A5 B5 A4 B4 A3 B3 A2 B2 A1 B1 A0 B0
GAB GBA
LS622
(SIZE)
MAX_DELAY=10000
LS622
A
B
OC
GAB GBA
MAX_DELAY=10000
LS622
A7 B7 A6 B6 A5 B5 A4 B4 A3 B3 A2 B2 A1 B1 A0 B0
OC
GAB GBA

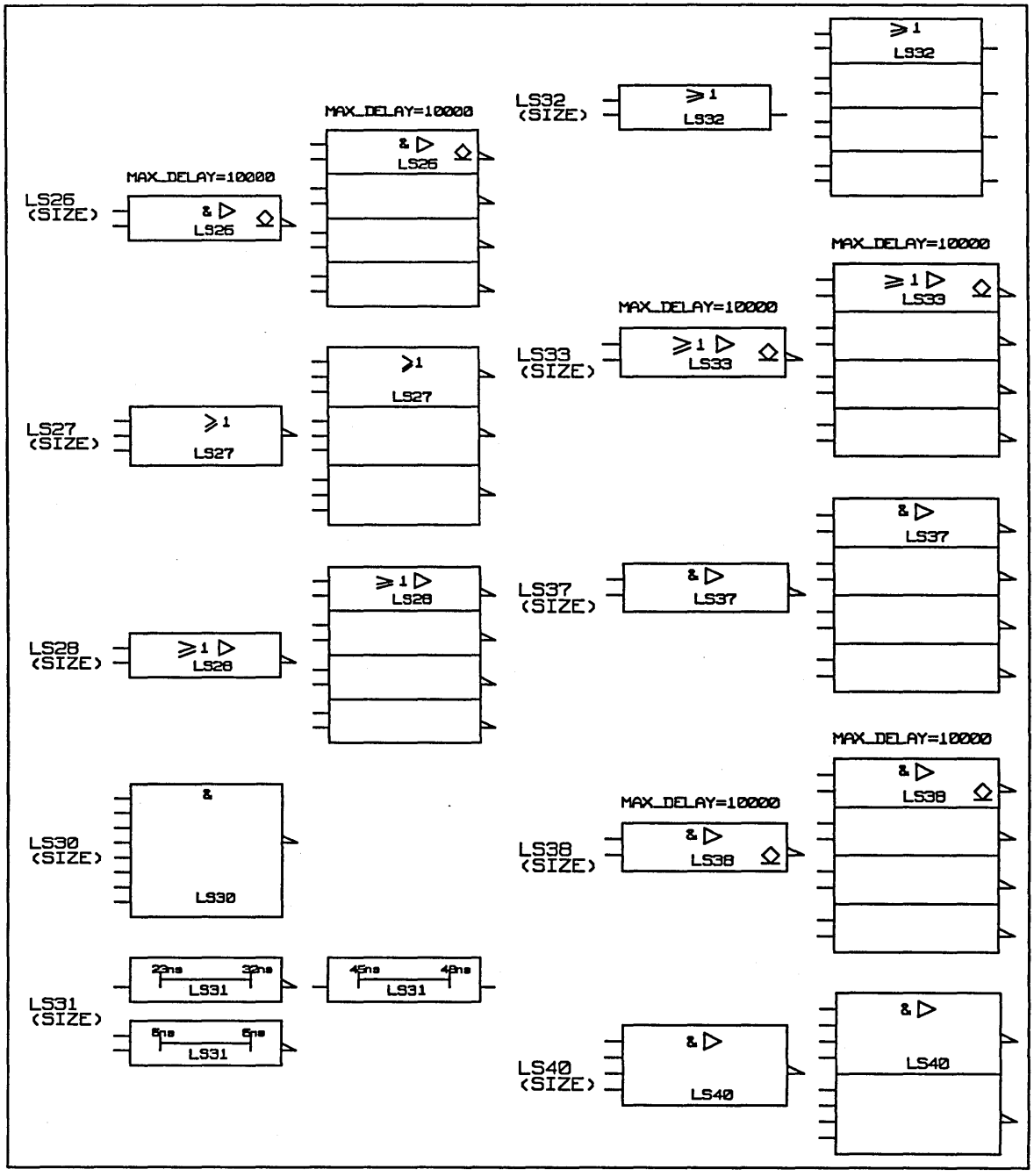

LS623
(SIZE)
LS623
TS
A
B
GAB GBA
LS623
TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
GAB GBA
LS624
PULSE_WIDTH=10000
MAX_DELAY=10000
C1 C2
LS624
OSC
Q
Q
EN
FC RNG
LS625
PULSE_WIDTH=10000
C1 C2
LS625
OSC
Q
Q
FC
LS626
PULSE_WIDTH=10000
MAX_DELAY=10000
C1 C2
LS626
OSC
Q
Q
EN
FC
LS627
PULSE_WIDTH=10000
C1 C2
LS627
OSC
Q
FC
LS628
PULSE_WIDTH=10000
MAX_DELAY=10000
R1 R2 C1 C2
LS628
OSC
Q
Q
EN
FC RNG
LS629
MAX_DELAY=10000
PULSE_WIDTH=10000
C1 C2
Q
LS629
OSC
EN
FC RNG
LS640
(SIZE)
LS640
TS
A
B
DIR E
LS640
TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR E
LS641
(SIZE)
MAX_DELAY=10000
LS641
OC
A
B
DIR E
MAX_DELAY=10000
LS641
OC
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR E

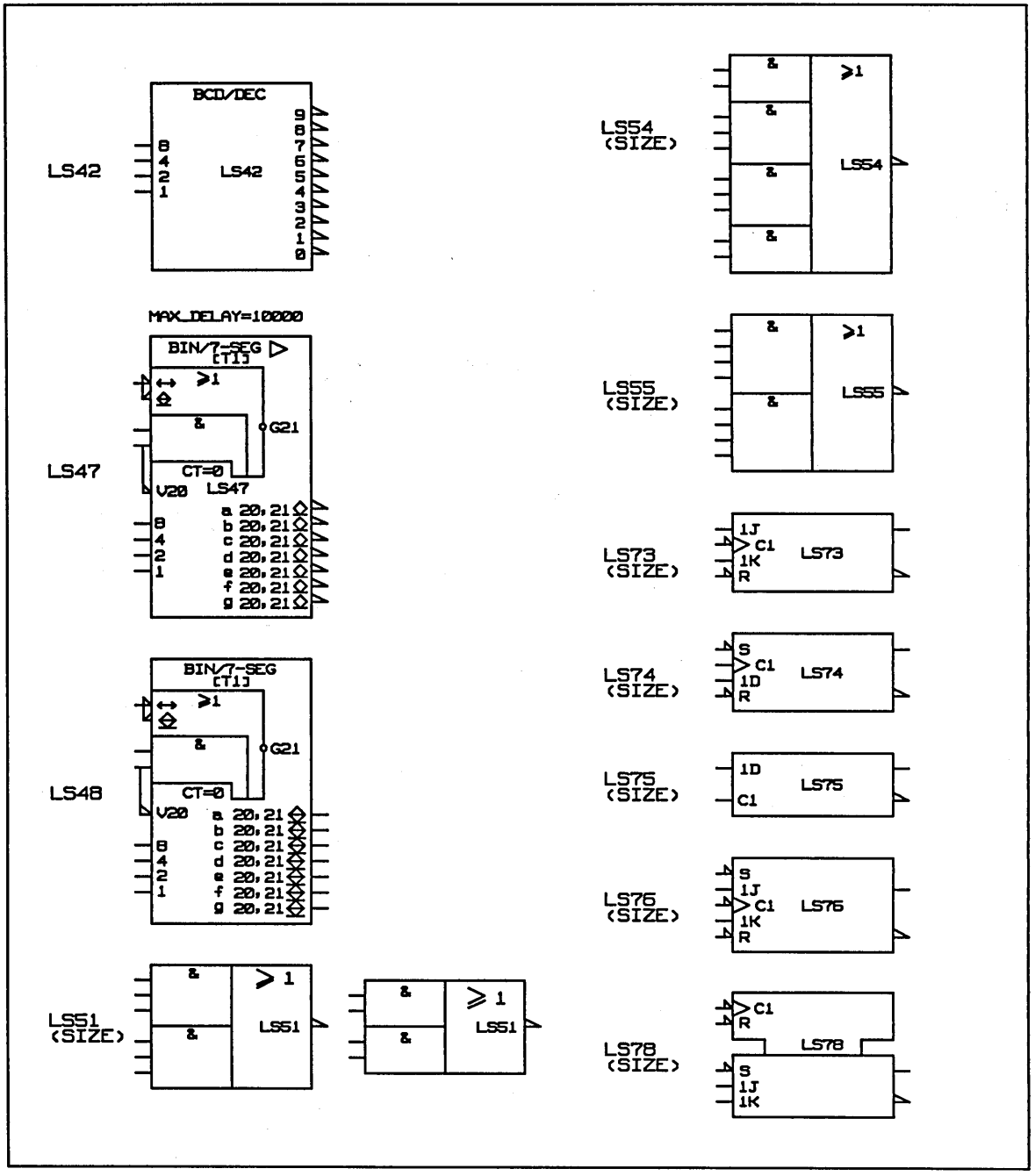

LS642
(SIZE)
MAX_DELAY=10000
LS642
OC
A
B
DIR E
MAX_DELAY=10000
LS642
OC
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
DIR E
LS645
(SIZE)
LS645
T3
A
B
DIR E
LS645
T3
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
DIR E
LS652
(SIZE)
LS652
T3
A
B
CAB
CBA
SBA SAB GAB GBA
LS652
T3(T3)
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
CAB
CBA
SBA SAB GAB GBA
LS668
LS668
DECADE CTR
UP/DN
T
P
RIPPLE CARRY
LD
LS668
DECADE CTR
UP/DN
T
P
RIPPLE CARRY
LD
LS669
LS669
BINARY CTR
UP/DN
T
P
RIPPLE CARRY
LD
LS669
BINARY CTR
UP/DN
T
P
RIPPLE CARRY
LD
LS670
LS670
4X4 REGISTER FILES
RE
WE
LS670
4X4 REGISTER FILES
RE
WE
LS671
LS671
SHIFT REGISTER
LSB IN
MSB IN
S1
S0
R/S
S
R
LS671
SHIFT REGISTER
LSB IN
MSB IN
S1
S0
R/S
S
R
LS672
LS672
SHIFT REGISTER
LSB IN
MSB IN
S1
S0
R/S
S
R
LS672
SHIFT REGISTER
LSB IN
MSB IN
S1
S0
R/S
S
R


LS674
LS684
LS693
LS699
LS793
(SIZE)
LS674
SHIFT REGISTER
SI/OHSB
D15-0
MODE
R/W CS
LS684
IDENTITY COMPARATOR
A7-0
B7-0
A=B
A>B
LS693
BINARY CTR
D3-0
Q3-0
CCK
RCK
RCO
R/C
T
P
G
LD RCL CCL
LS699
BINARY CTR
D3-0
Q3-0
CCK
RCK
RCO
R/C
T
P
G
LD U/D CCL
LS
793
D
Q
G
OE
LS793
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
G OE

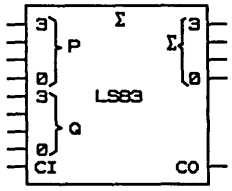

LS00
(SIZE)
&
LS00
&
LS00
MAX_DELAY=10000
LS01
(SIZE)
&
LS01
&
LS01
MAX_DELAY=10000
LS02
(SIZE)
≥1
LS02
≥1
LS02
MAX_DELAY=10000
LS03
(SIZE)
&
LS03
&
LS03
MAX_DELAY=10000
LS04
(SIZE)
1
LS04
1
LS04
LS05
(SIZE)
1
LS05
1
LS05
MAX_DELAY=10000
LS08
(SIZE)
&
LS08
&
LS08
LS09
(SIZE)
&
LS09
&
LS09
MAX_DELAY=10000
LS10
(SIZE)
&
LS10
&
LS10
LS11
(SIZE)
&
LS11
&
LS11
MAX_DELAY=10000


MAX_DELAY=10000
LS12
(SIZE)
LS12
LS13
LS19
LS14
LS15
LS18
LS19
LS20
LS21
LS22
LS24

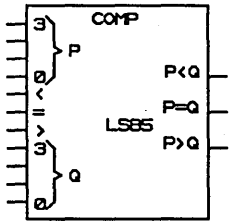

LS25
(SIZE)
MAX_DELAY=10000
LS26
LS27
(SIZE)
LS27
LS28
(SIZE)
LS28
LS30
(SIZE)
LS30
LS31
(SIZE)
23ns
32ns
LS31
45ns
48ns
LS31
5ns
5ns
LS31
LS32
(SIZE)
LS32
LS33
(SIZE)
MAX_DELAY=10000
LS33
LS37
(SIZE)
LS37
LS38
(SIZE)
MAX_DELAY=10000
LS38
LS40
(SIZE)
LS40


LS42
BCD/DEC
LS42
LS47
MAX_DELAY=10000
BIN/7-SEG
LS47
LS48
LS51
(SIZE)
LS54
LS55
LS73
LS74
LS75
LS76
LS78

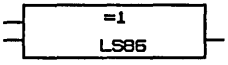
LS83

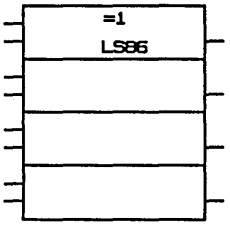


LS85

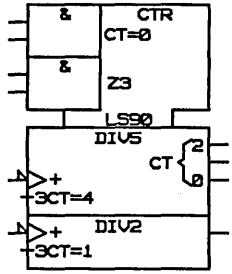


LS86 (SIZE)

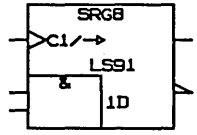




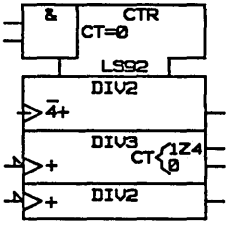
LS90



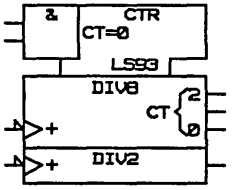
LS91



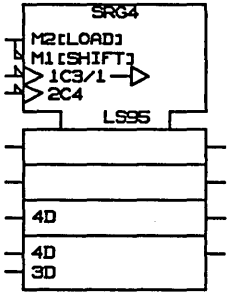
LS92



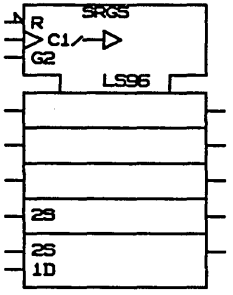
LS93



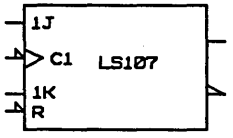
LS95

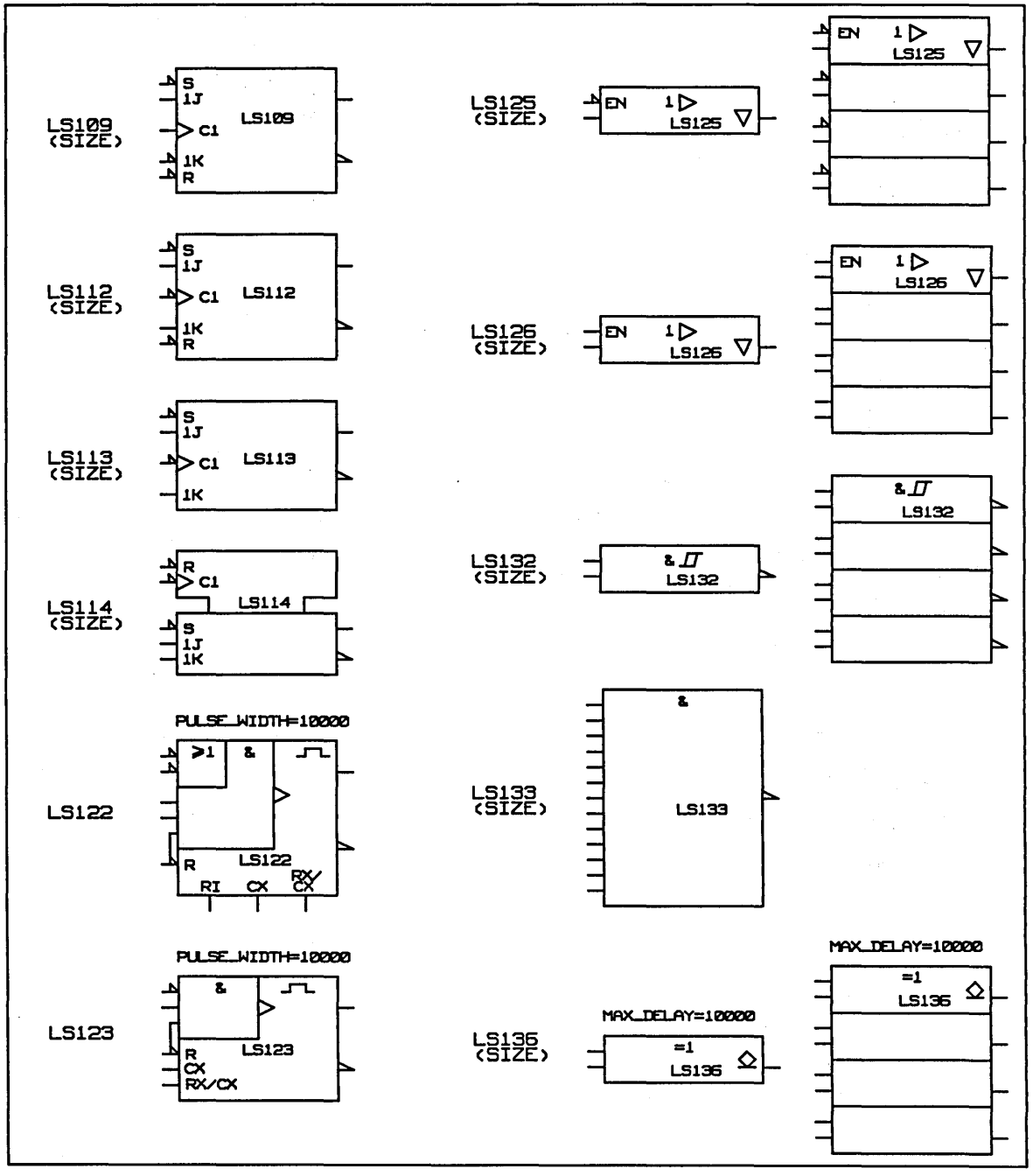


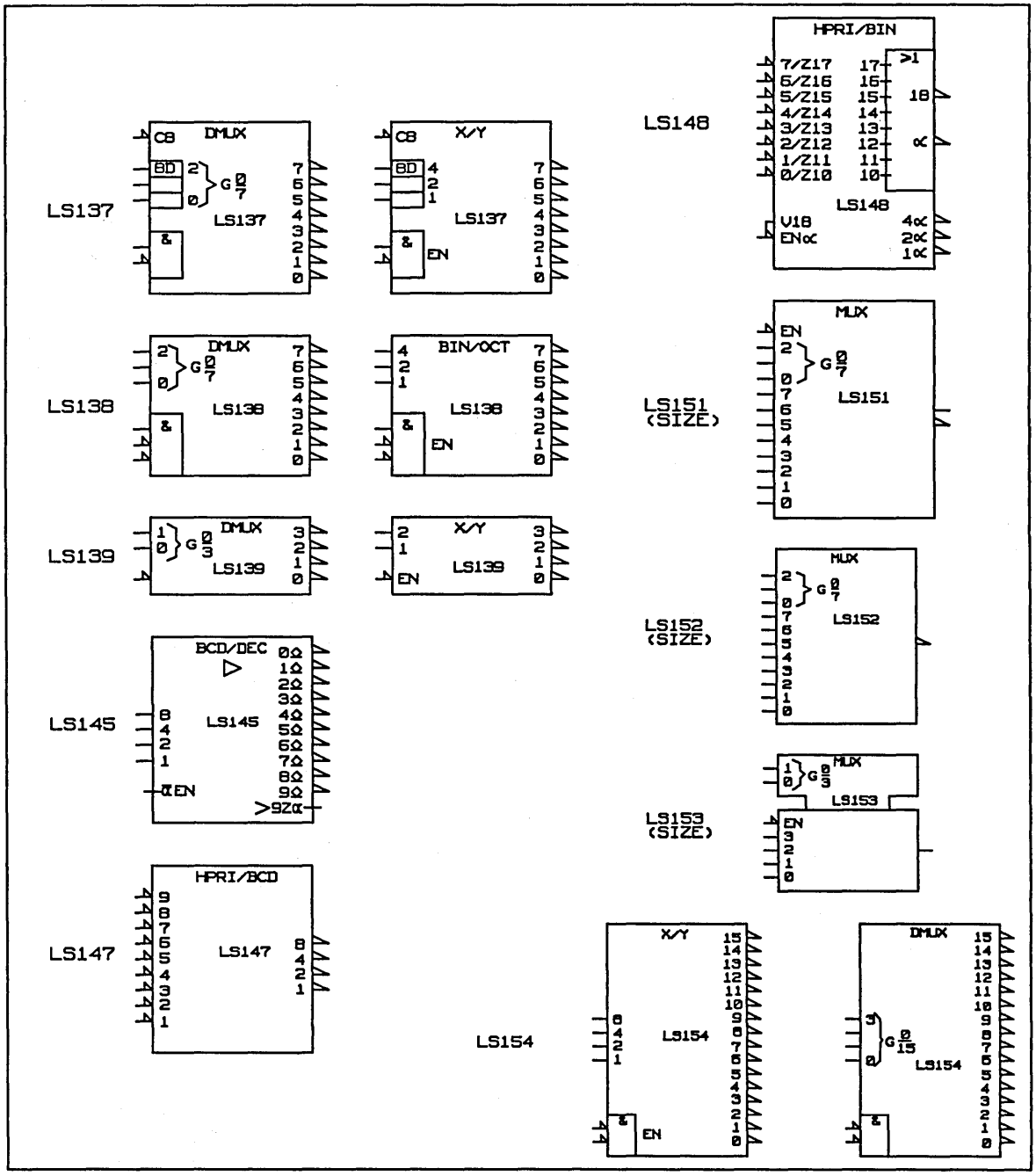
LS96

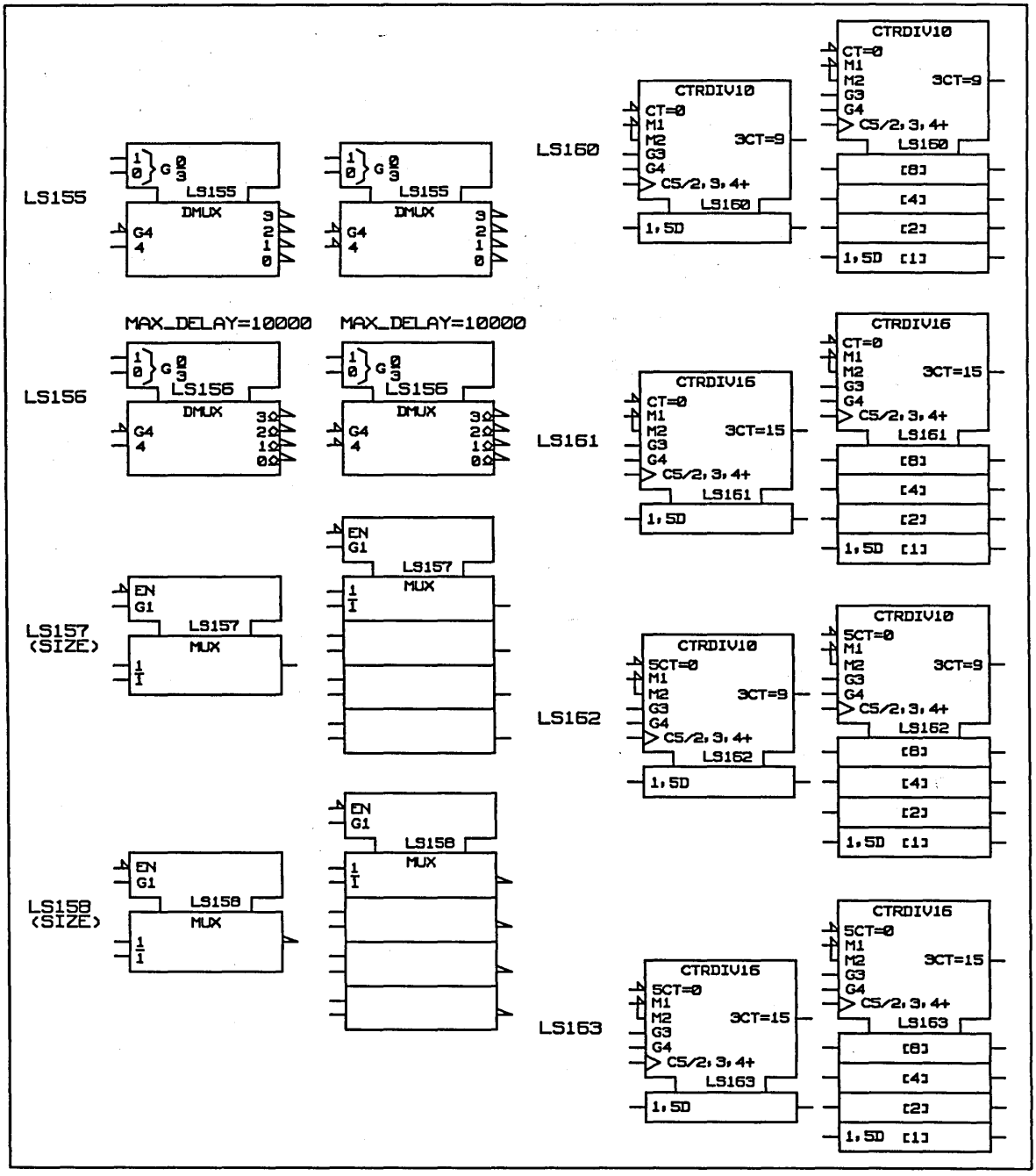


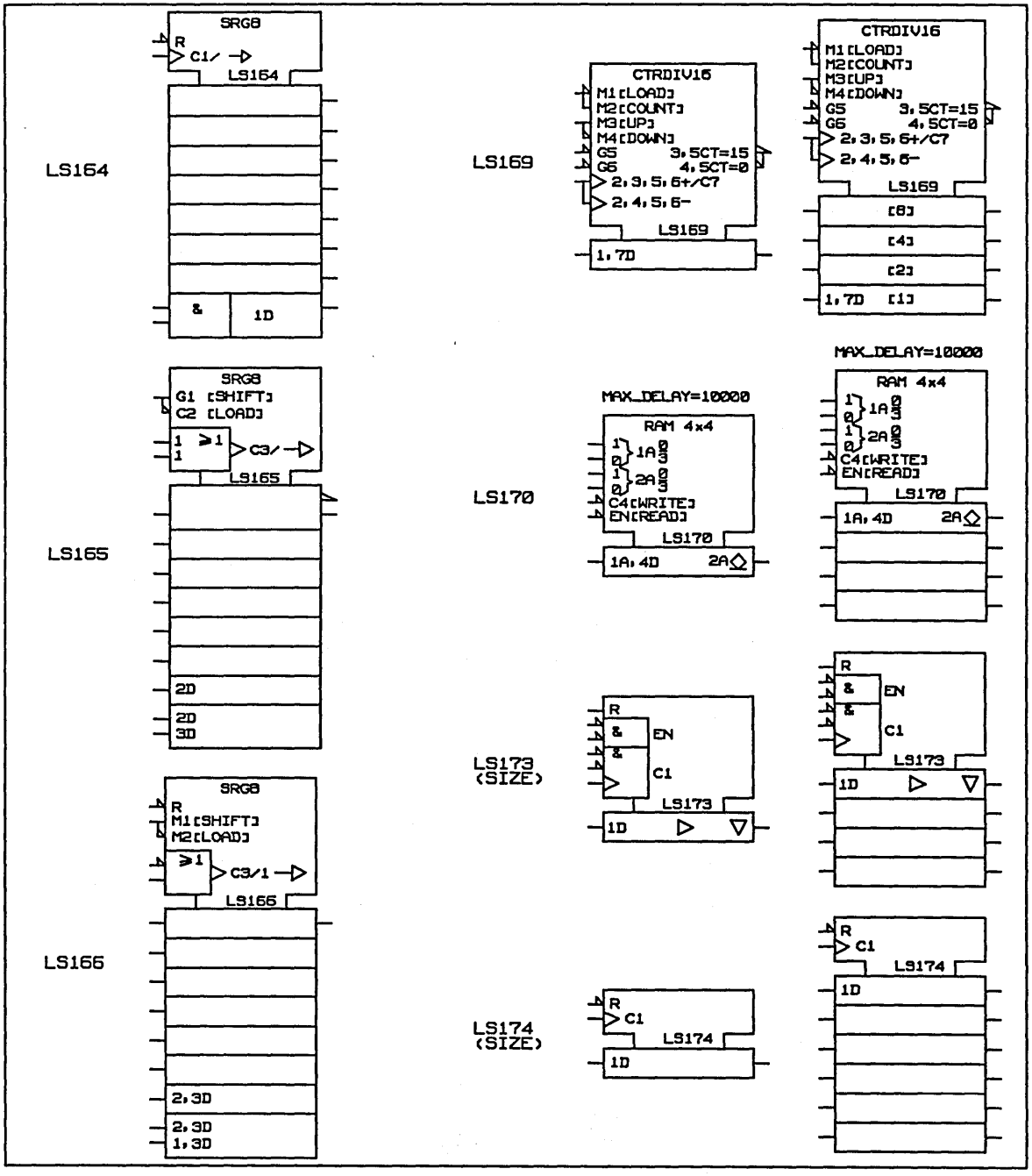
LS107 (SIZE)

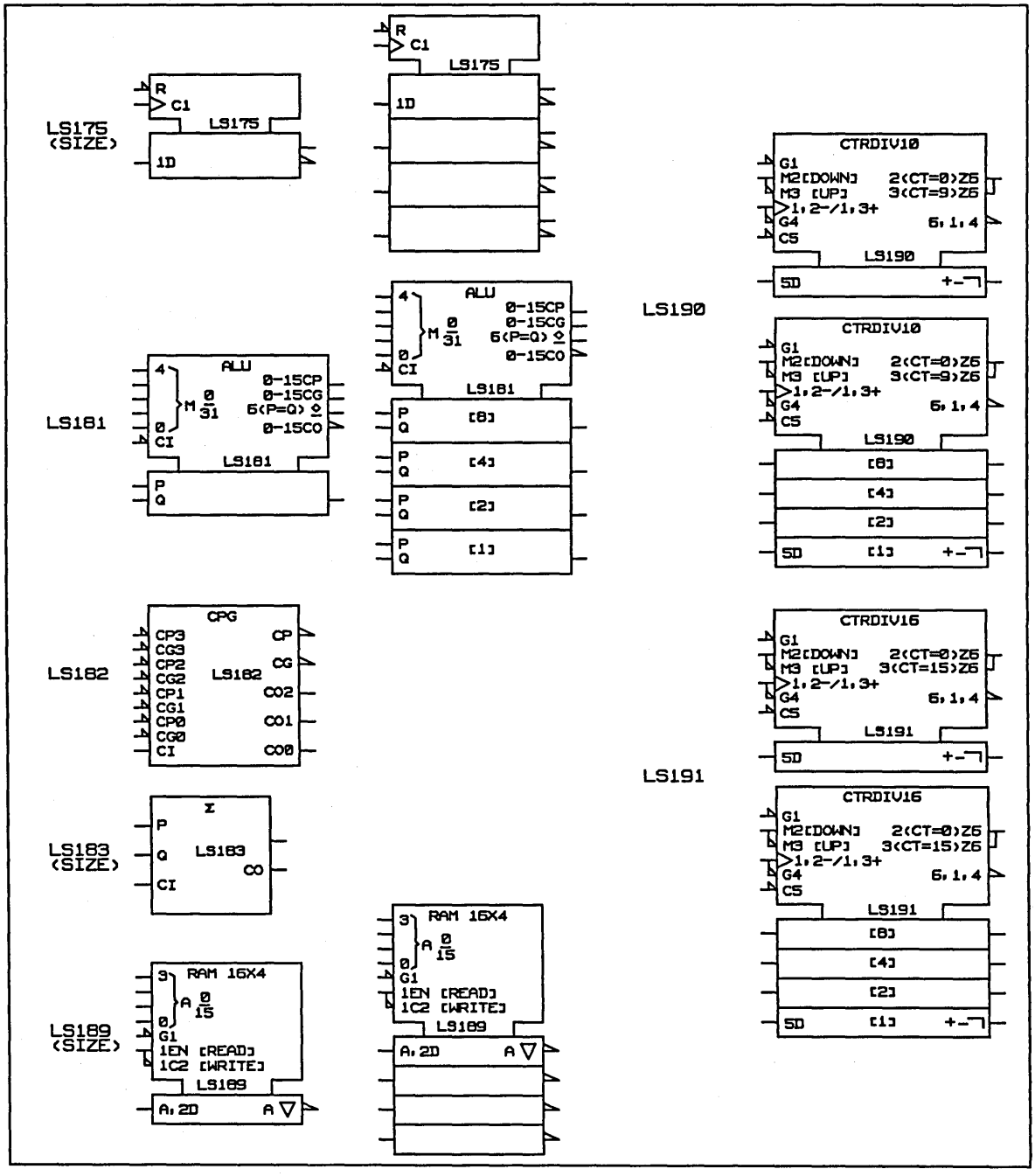


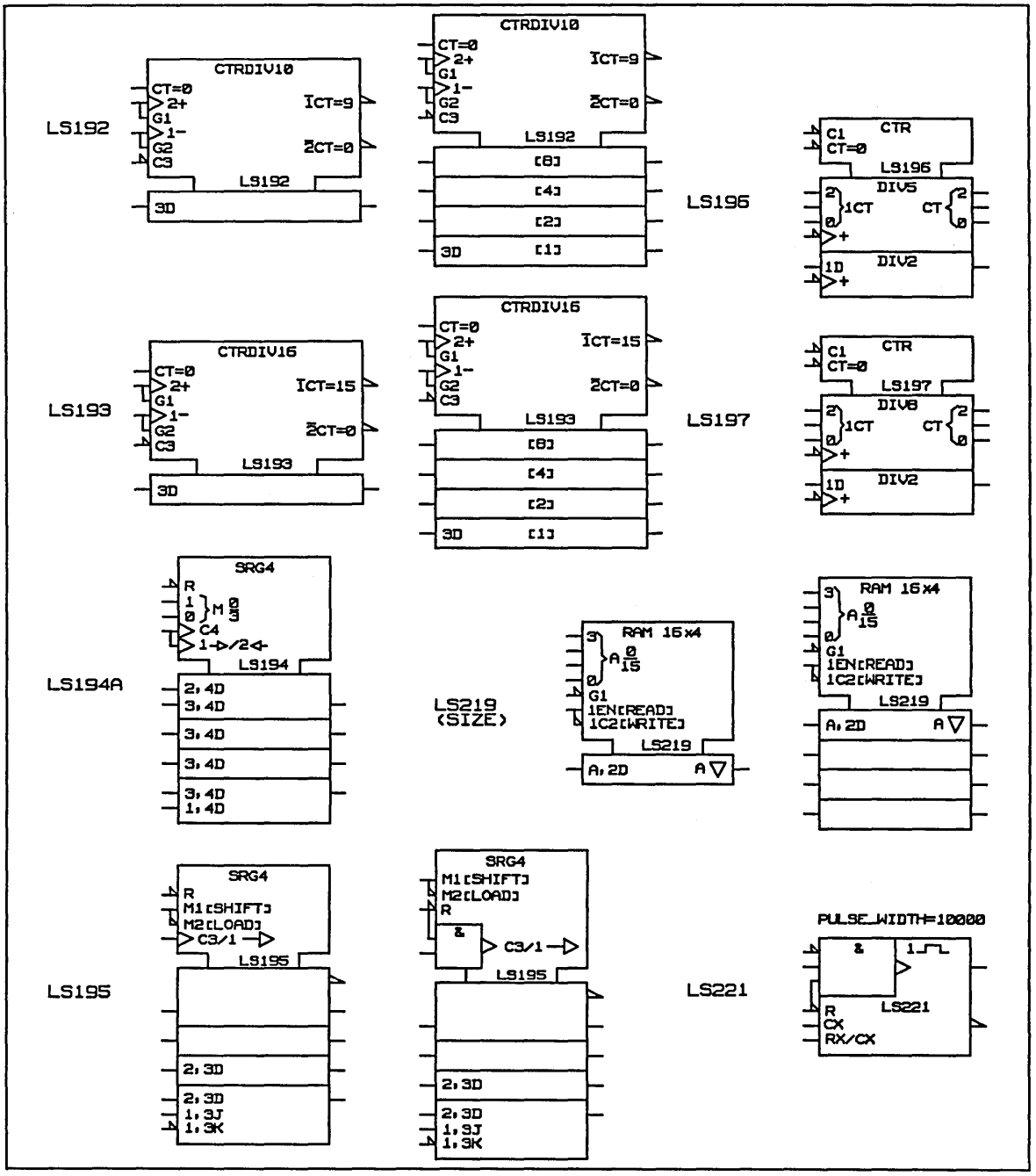

LS109
(SIZE)
S
1J
C1
LS109
1K
R
LS112
(SIZE)
S
1J
C1
LS112
1K
R
LS113
(SIZE)
S
1J
C1
LS113
1K
LS114
(SIZE)
R
C1
LS114
S
1J
1K
PULSE_WIDTH=10000
LS122
≥1
&
R
LS122
RI
CX
RX/CX
PULSE_WIDTH=10000
LS123
&
R
CX
RX/CX
LS123
LS125
(SIZE)
EN
1
LS125
EN
1
LS125
LS126
(SIZE)
EN
1
LS125
EN
1
LS125
LS132
(SIZE)
&
LS132
&
LS132
LS133
(SIZE)
&
LS133
MAX_DELAY=10000
LS136
(SIZE)
=1
LS136
MAX_DELAY=10000
=1
LS136


LS137
LS138
LS139
LS145
LS147
LS148
LS151
(SIZE)
LS152
(SIZE)
LS153
(SIZE)
LS154
DMUX
X/Y
BIN/OCT
BCD/DEC
HPRI/BCD
HPRI/BIN
MUX
EN

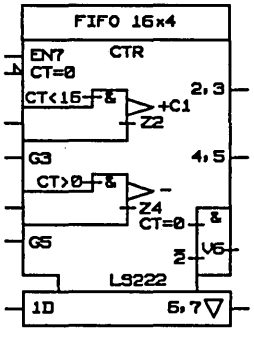

LS155
LS155
DMUX
G4
4
LS155
LS155
DMUX
G4
4
MAX_DELAY=10000
MAX_DELAY=10000
LS156
LS156
DMUX
G4
4
LS156
LS156
DMUX
G4
4
LS157
(SIZE)
EN
G1
LS157
MUX
LS157
MUX
LS158
(SIZE)
EN
G1
LS158
MUX
LS158
MUX
LS160
CTRDIV10
CT=0
M1
M2
G3
G4
C5/2,3,4+
3CT=9
LS160
1,5D
LS161
CTRDIV16
CT=0
3CT=15
LS161
LS162
CTRDIV10
5CT=0
3CT=9
LS162
LS163
CTRDIV16
5CT=0
3CT=15
LS163
[8]
[4]
[2]
[1]

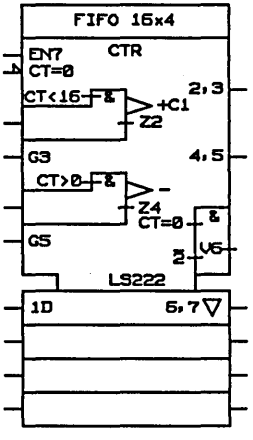

LS164
SRG8
R
C1/
LS164
&
1D
LS165
SRG8
G1 [SHIFT]
C2 [LOAD]
1
1
≥1
C3/
LS165
2D
2D
3D
LS166
SRG8
R
M1[SHIFT]
M2[LOAD]
≥1
C3/1
LS166
2,3D
2,3D
1,3D
LS169
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS169
1,7D
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS169
[8]
[4]
[2]
1,7D [1]
LS170
MAX_DELAY=10000
RAM 4x4
1A
2A
C4[WRITE]
EN[READ]
LS170
1A,4D 2A
MAX_DELAY=10000
RAM 4x4
1A
2A
C4[WRITE]
EN[READ]
LS170
1A,4D 2A
LS173
(SIZE)
R
&
EN
C1
LS173
1D
R
&
EN
C1
LS173
1D
LS174
(SIZE)
R
C1
LS174
1D
R
C1
LS174
1D


LS175
(SIZE)
R
C1
LS175
1D
LS181
ALU
M
0-15CP
0-15CG
0-15CO
P
Q
CI
LS182
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CO2
CO1
CO0
LS183
(SIZE)
LS189
(SIZE)
RAM 16X4
A
1EN [READ]
1C2 [WRITE]
A,2D
LS190
CTRDIV10
G1
M2[DOWN]
M3 [UP]
G4
C5
LS191
CTRDIV16
+-

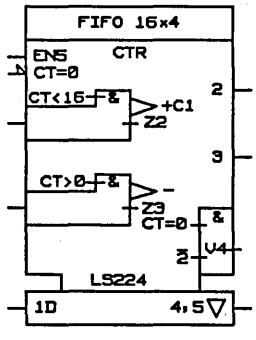

LS192
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
2CT=0
LS192
3D
LS193
CTRDIV16
CT=0
2+
G1
1-
G2
C3
ICT=15
2CT=0
LS193
3D
LS194A
SRG4
R
M
C4
1->/2<-
LS194
2,4D
3,4D
3,4D
3,4D
3,4D
1,4D
LS195
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
LS195
2,3D
2,3D
1,3J
1,3K
LS219
(SIZE)
RAM 16x4
A
G1
1EN[READ]
1C2[WRITE]
LS219
A,2D
A
LS196
CTR
C1
CT=0
LS196
DIV5
1CT
CT
DIV2
1D
LS197
CTR
C1
CT=0
LS197
DIV8
1CT
CT
DIV2
1D
LS221
PULSE_WIDTH=10000
&
1
LS221
R
CX
RX/CX

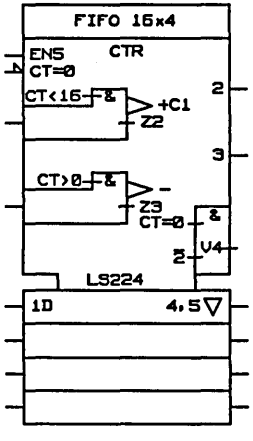
LS222



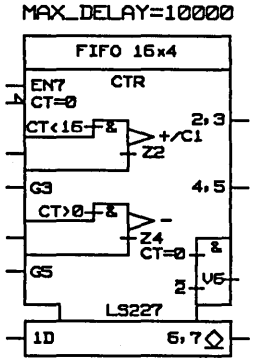


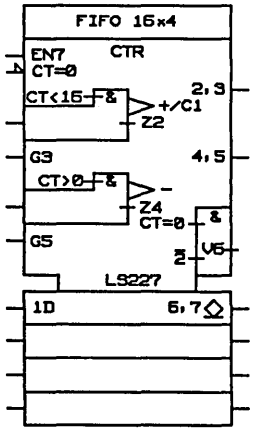
LS224

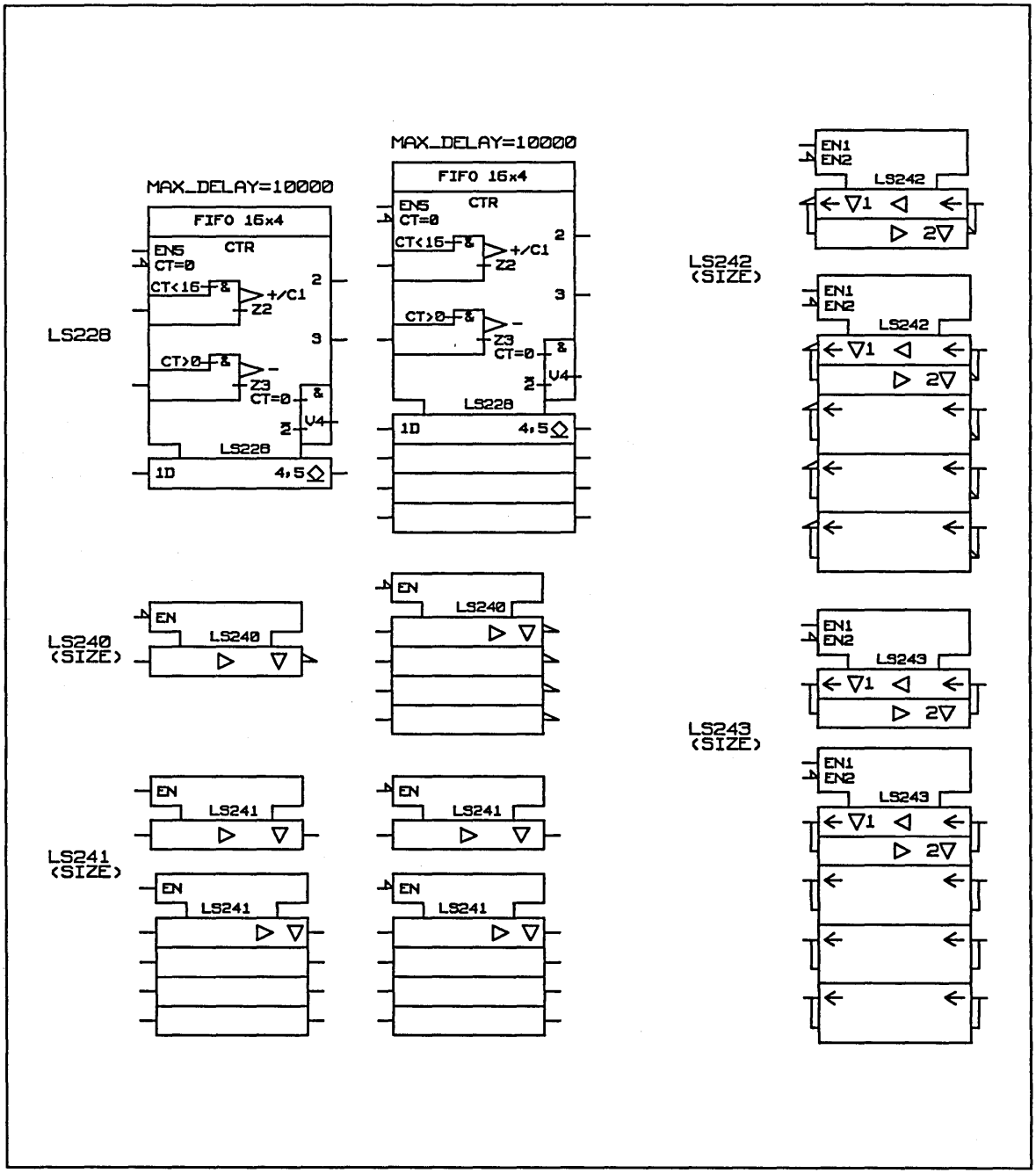


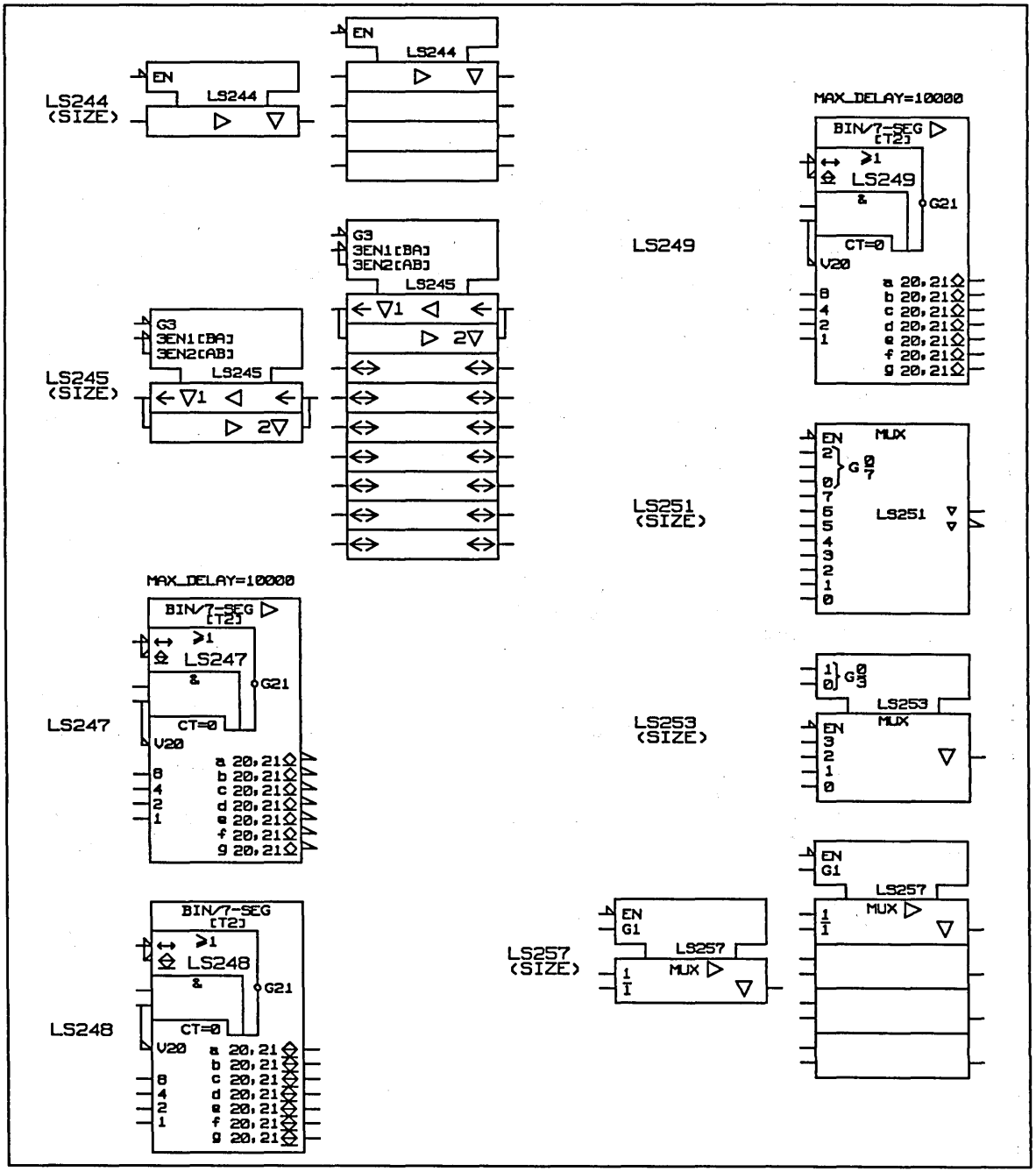


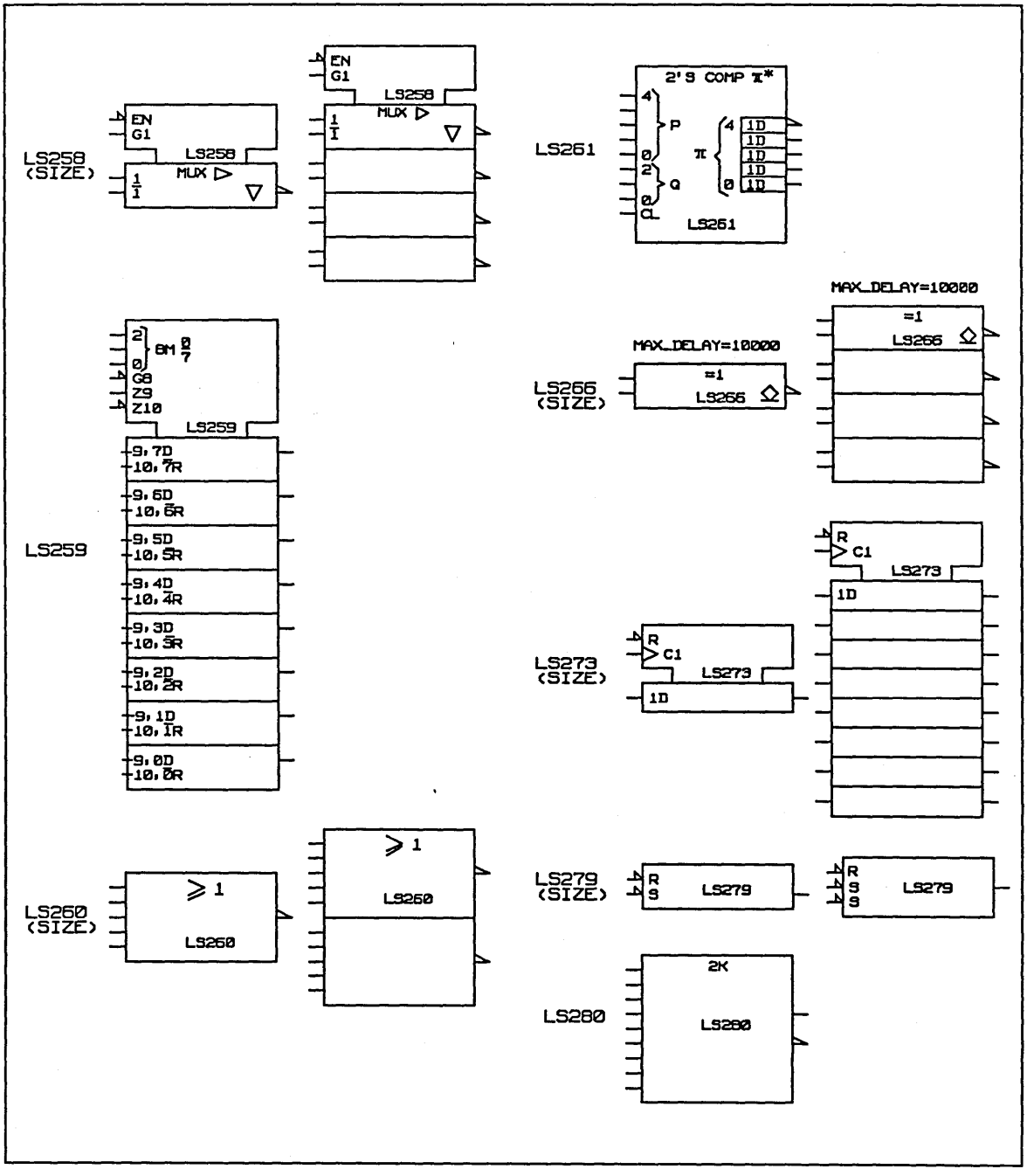
LS227

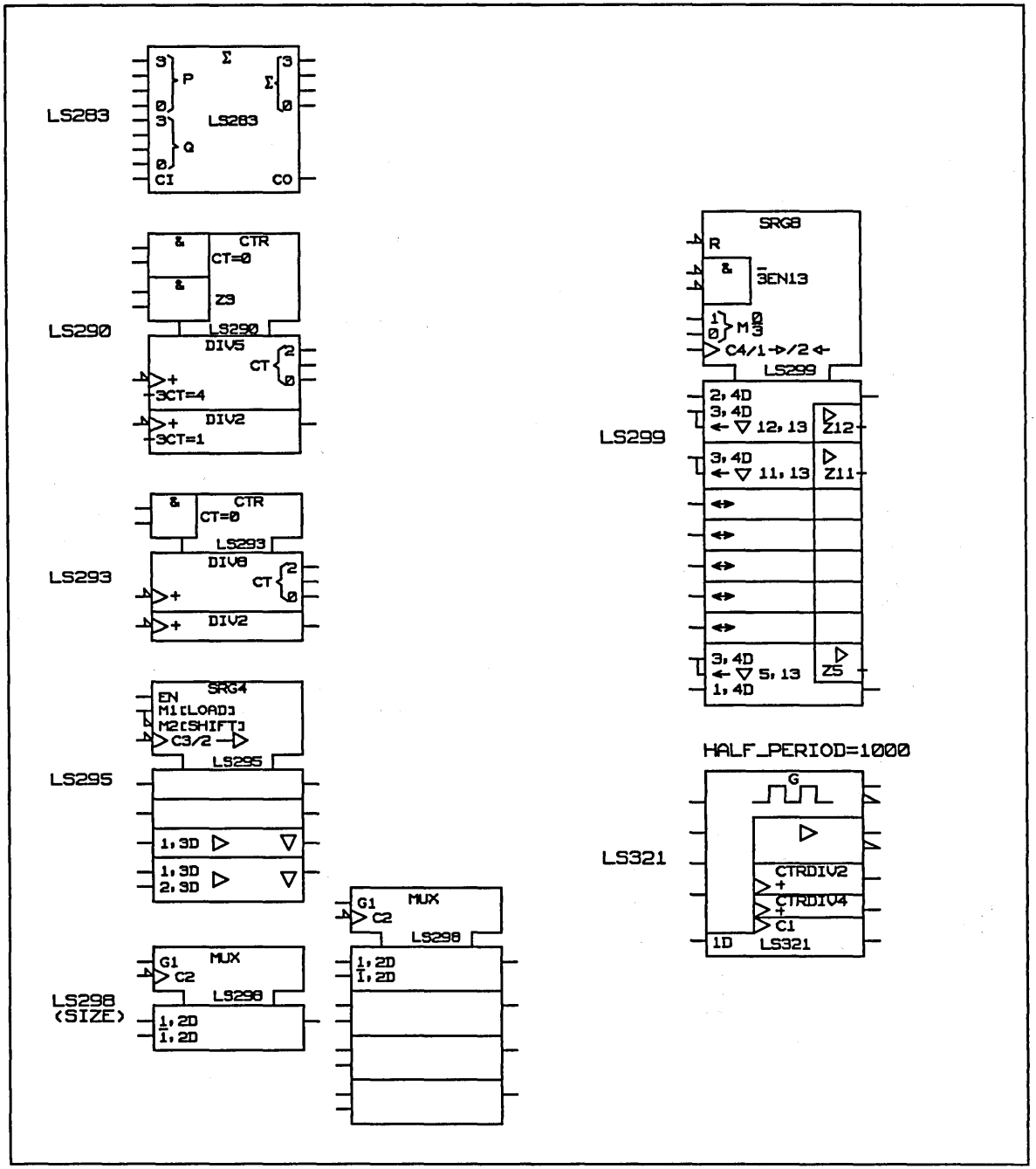




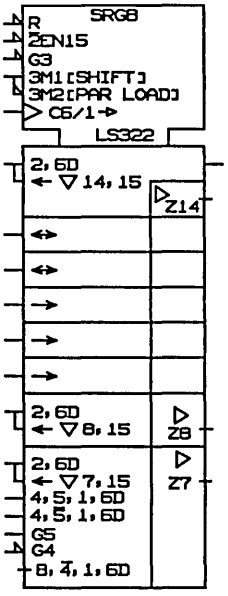

MAX_DELAY=10000
FIFO 16x4
EN5
CT=0
CTR
CT<16
+/C1
Z2
2
3
CT>0
Z3
CT=0
V4
LS228
1D
4,5
LS228
MAX_DELAY=10000
FIFO 16x4
LS240
(SIZE)
EN
LS240
LS241
(SIZE)
EN
LS241
LS242
(SIZE)
EN1
EN2
LS242
LS243
(SIZE)
LS243


LS244
(SIZE)
EN
LS244
LS245
(SIZE)
G3
3EN1[BA]
3EN2[AB]
LS245
LS247
MAX_DELAY=10000
BIN/7-SEG
[T2]
LS247
G21
CT=0
V20
LS248
LS249
LS251
(SIZE)
MUX
LS251
LS253
(SIZE)
LS253
LS257
(SIZE)
G1
LS257

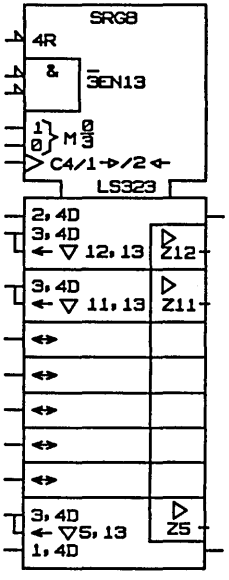

LS258
(SIZE)
EN
G1
LS258
MUX
LS261
2'S COMP π*
LS266
(SIZE)
MAX_DELAY=10000
=1
LS266
LS259
LS273
(SIZE)
LS273
R
C1
1D
LS260
(SIZE)
≥1
LS260
LS279
(SIZE)
R
S
LS279
LS280
2K
LS280


LS283
Σ
3
P
0
3
Q
0
CI
LS283
Σ
3
0
CO
LS290
&
CTR
CT=0
&
Z9
LS290
DIV5
CT
2
0
+
3CT=4
DIV2
+
3CT=1
LS293
&
CTR
CT=0
LS293
DIV8
CT
2
0
+
DIV2
LS295
EN
M1[LOAD]
M2[SHIFT]
C3/2
SRG4
LS295
1,3D
1,3D
2,3D
LS298
(SIZE)
G1
MUX
C2
LS298
1,2D
1,2D
G1
MUX
C2
LS298
1,2D
1,2D
LS299
SRG8
R
&
3EN13
1
0
M
0
3
C4/1→/2←
LS299
2,4D
3,4D
12,13
Z12
3,4D
11,13
Z11
3,4D
5,13
Z5
1,4D
HALF_PERIOD=1000
LS321
G
CTRDIV2
CTRDIV4
C1
1D
LS321

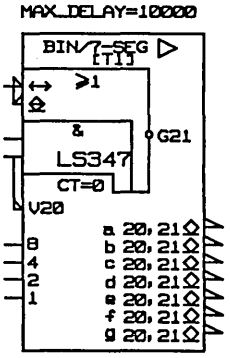
LS322



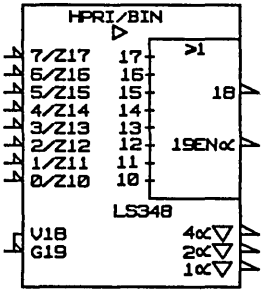
LS323



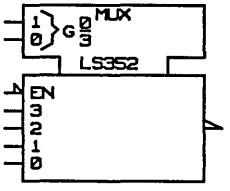
LS347



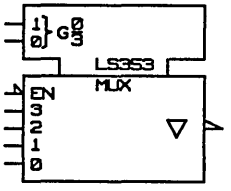
LS348



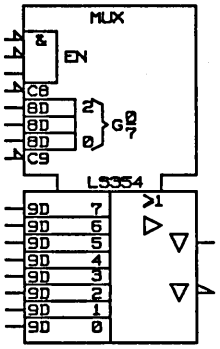
LS352
(SIZE)



LS353
(SIZE)

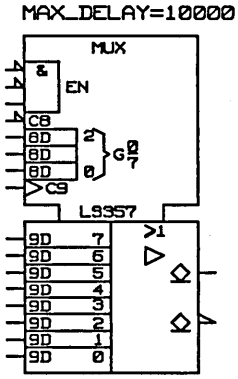


LS354
(SIZE)



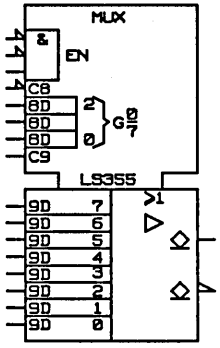
LS357
(SIZE)

MAX_DELAY=10000

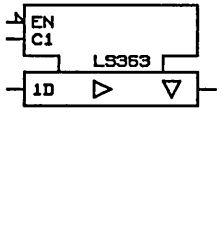


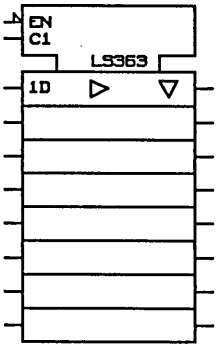
LS355
(SIZE)

MAX_DELAY=10000

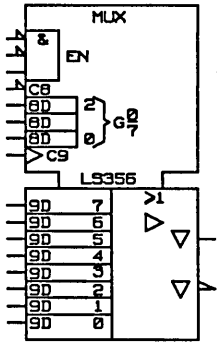


LS363
(SIZE)

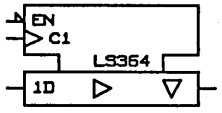


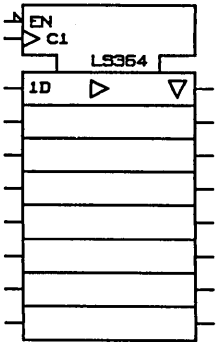


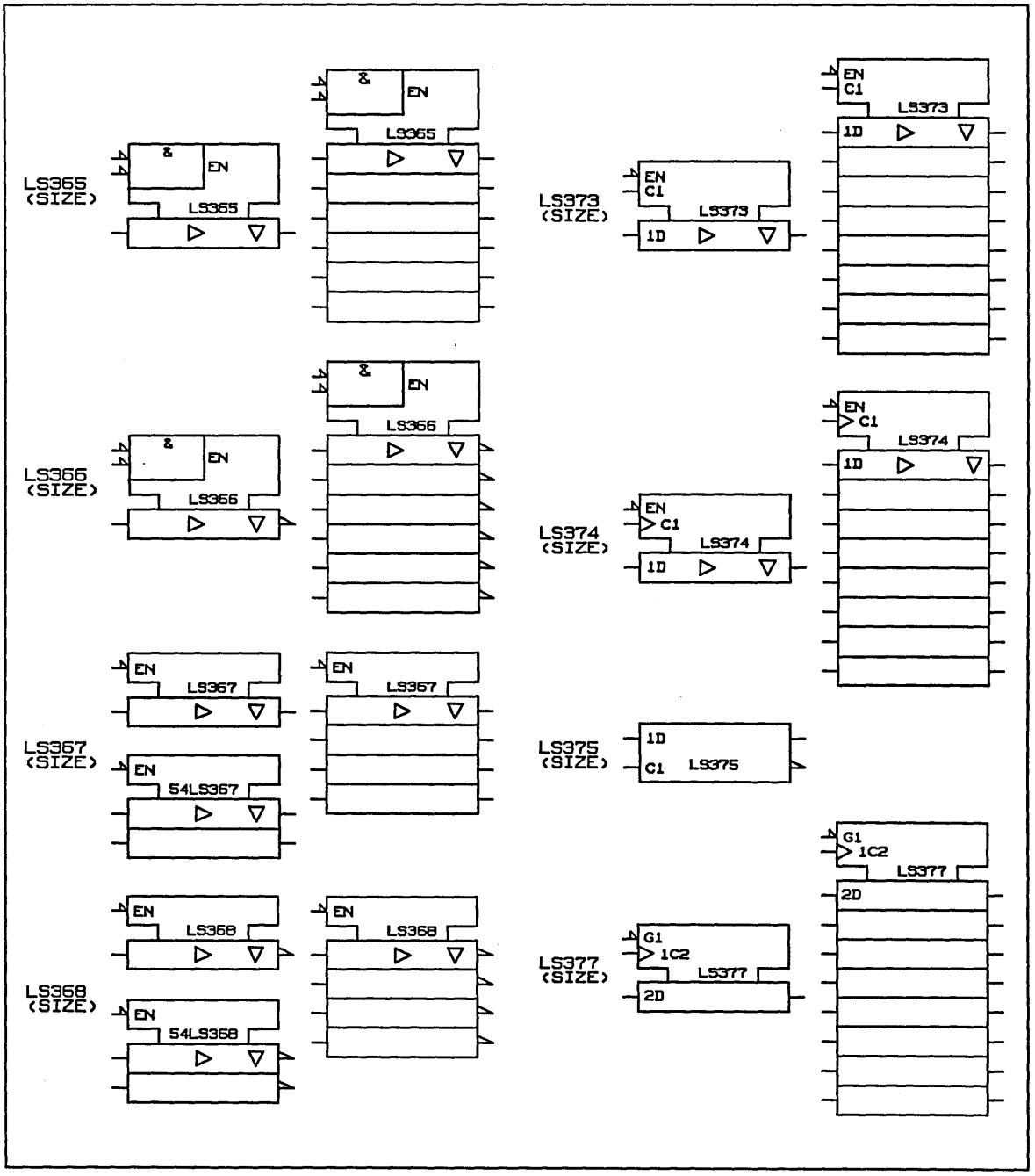
LS356
(SIZE)

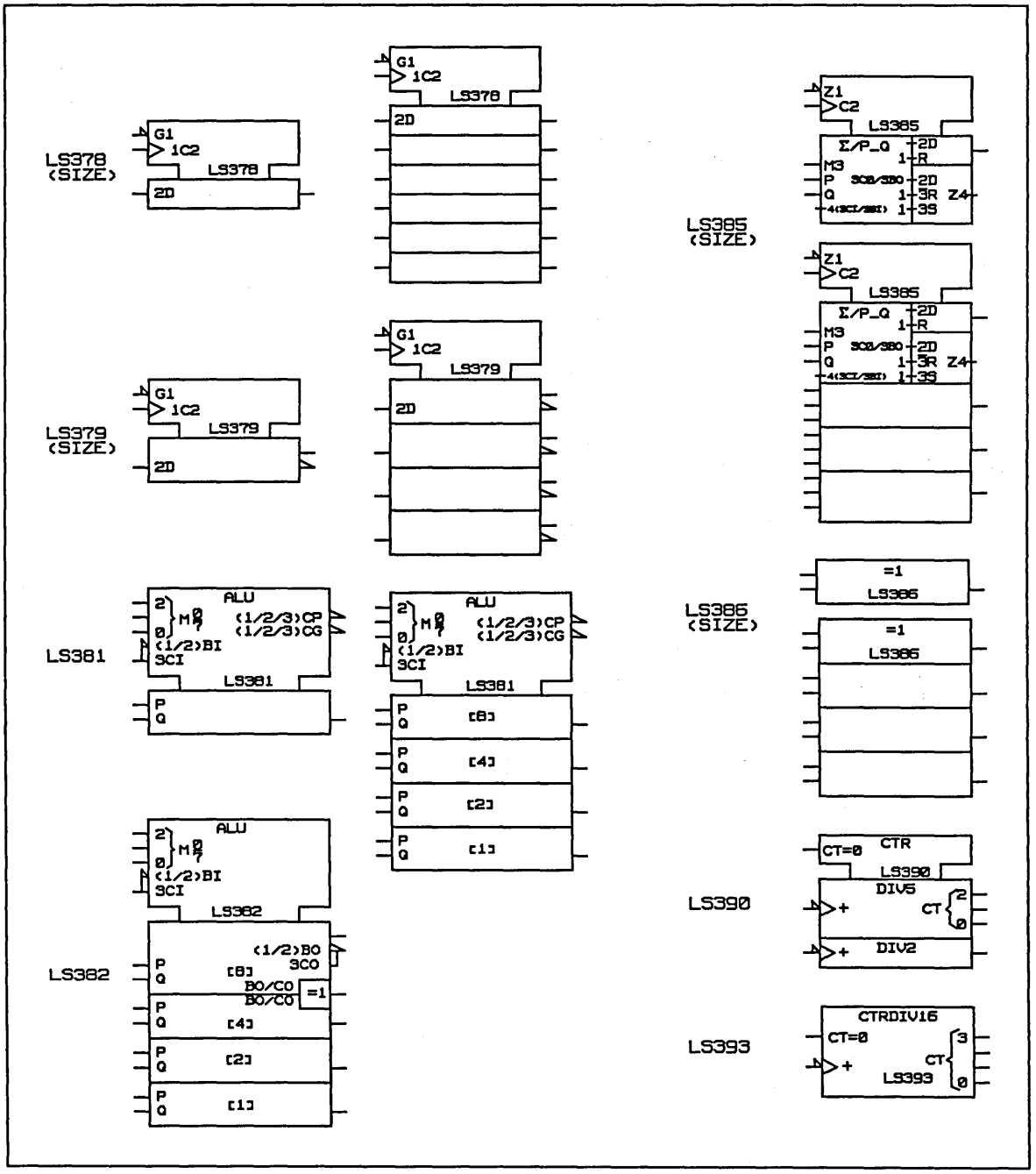


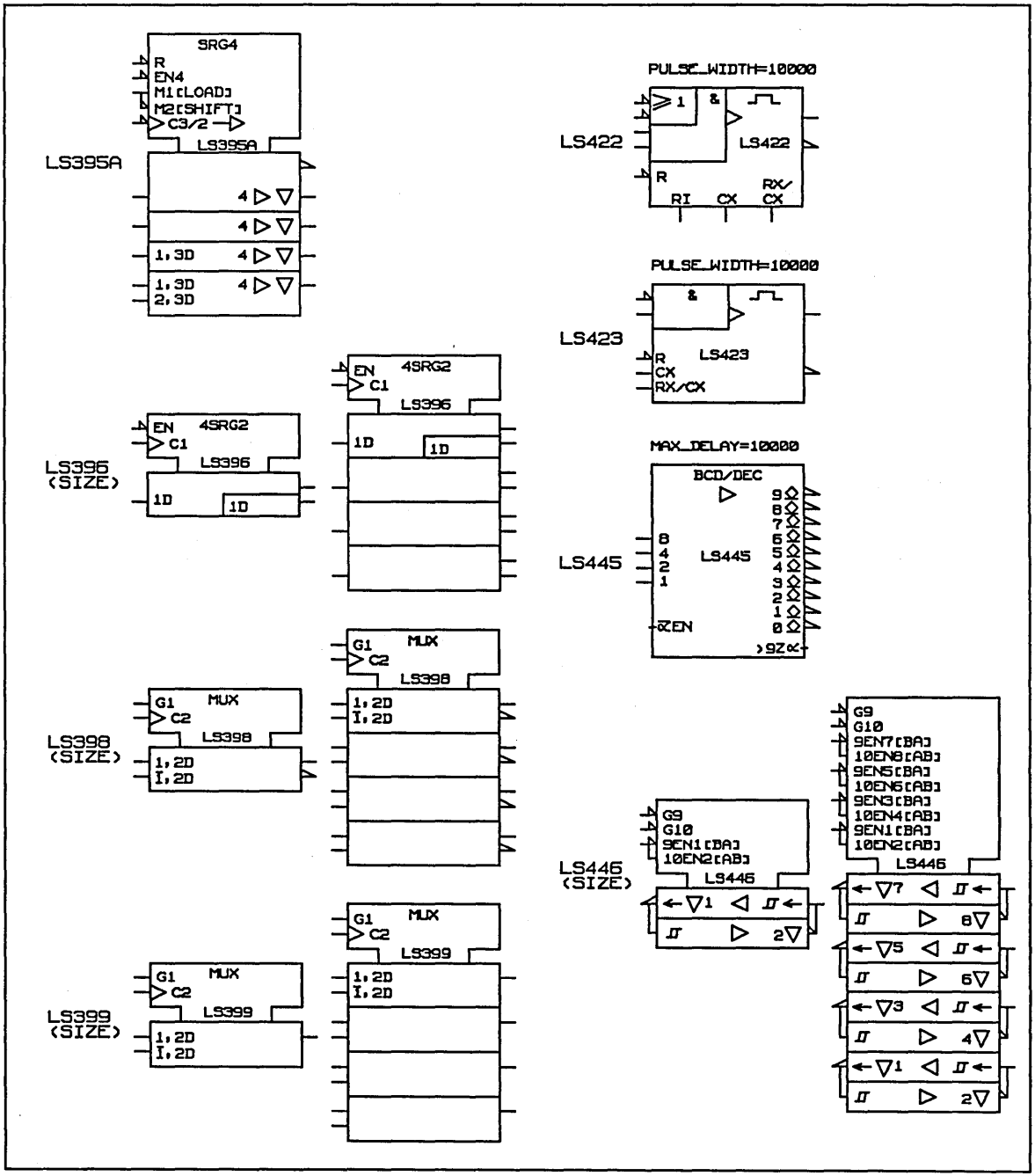
LS364
(SIZE)

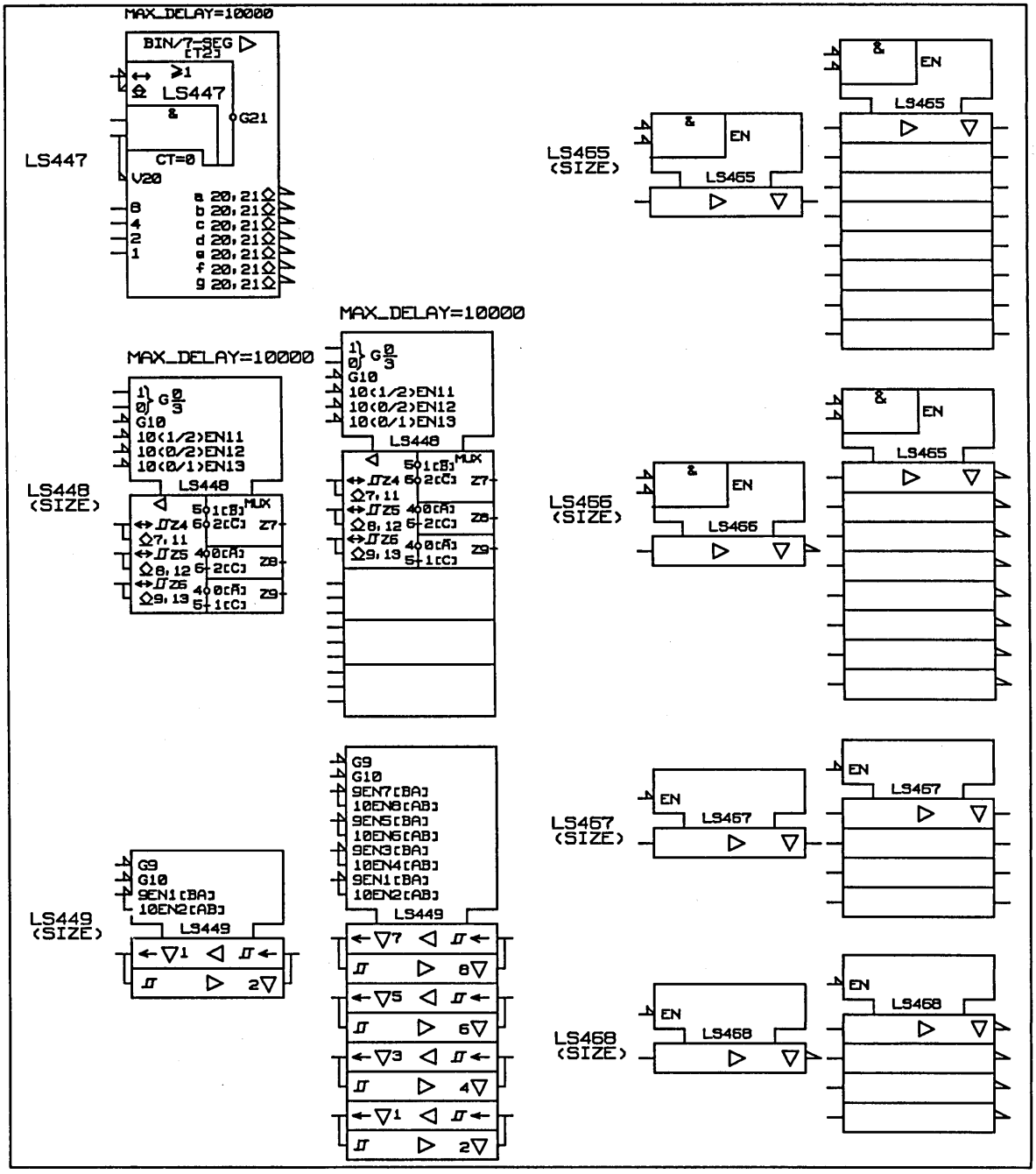


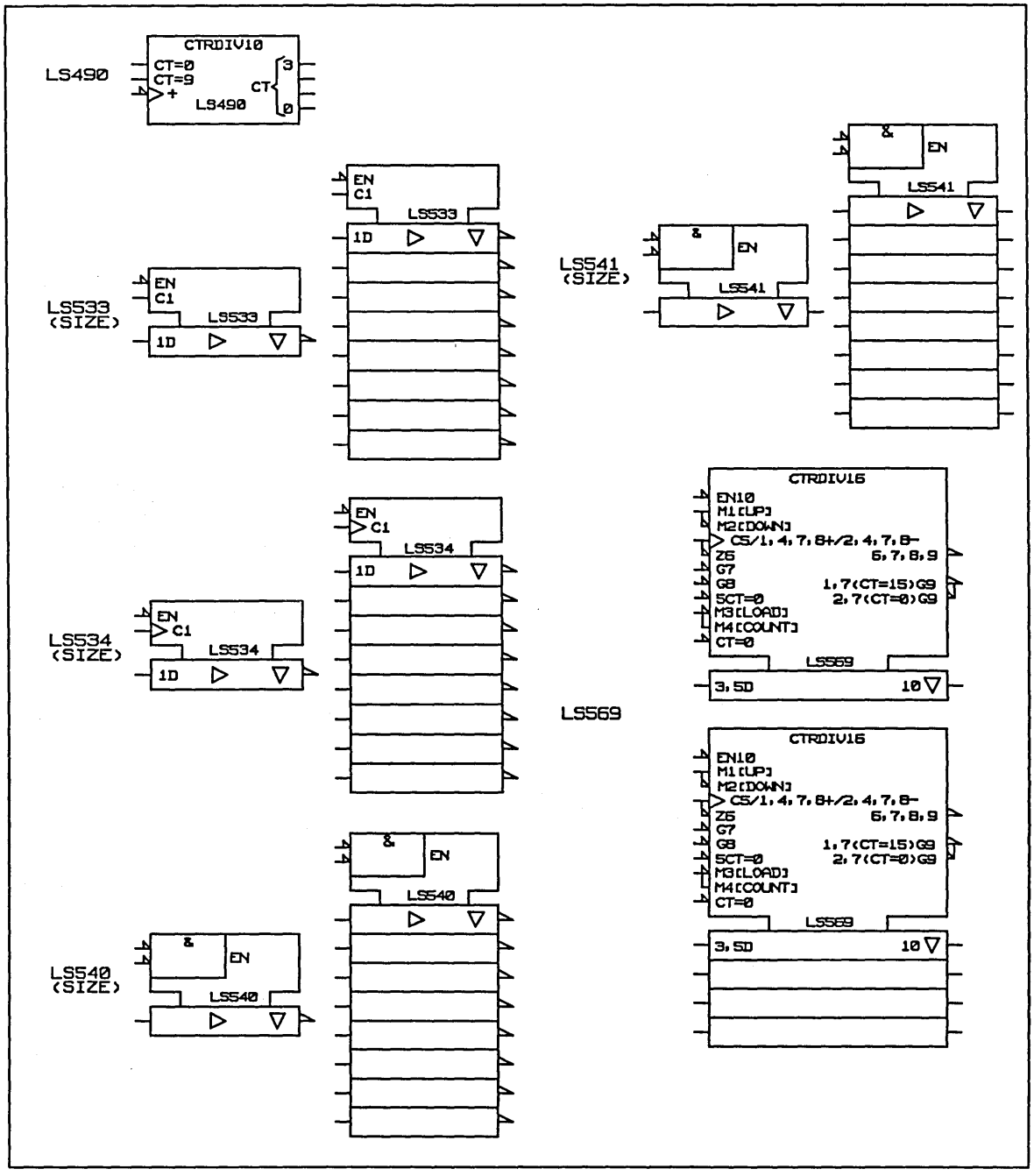


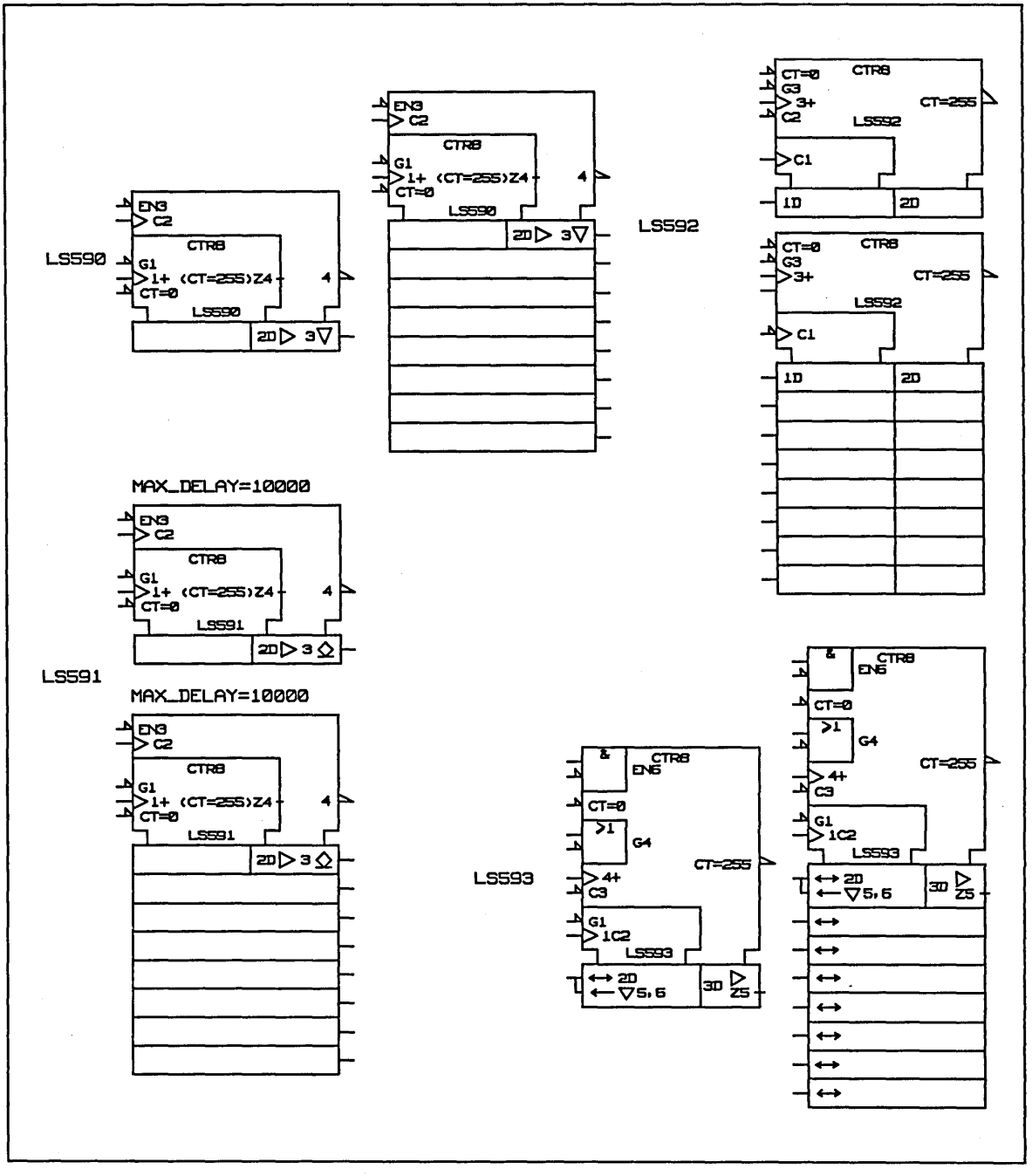

LS365
(SIZE)
&
EN
LS365
LS366
(SIZE)
&
EN
LS366
LS367
(SIZE)
EN
LS367
EN
54LS367
LS368
(SIZE)
EN
LS368
EN
54LS368
LS373
(SIZE)
EN
C1
LS373
1D
LS374
(SIZE)
EN
C1
LS374
1D
LS375
(SIZE)
1D
C1
LS375
LS377
(SIZE)
G1
1C2
LS377
2D

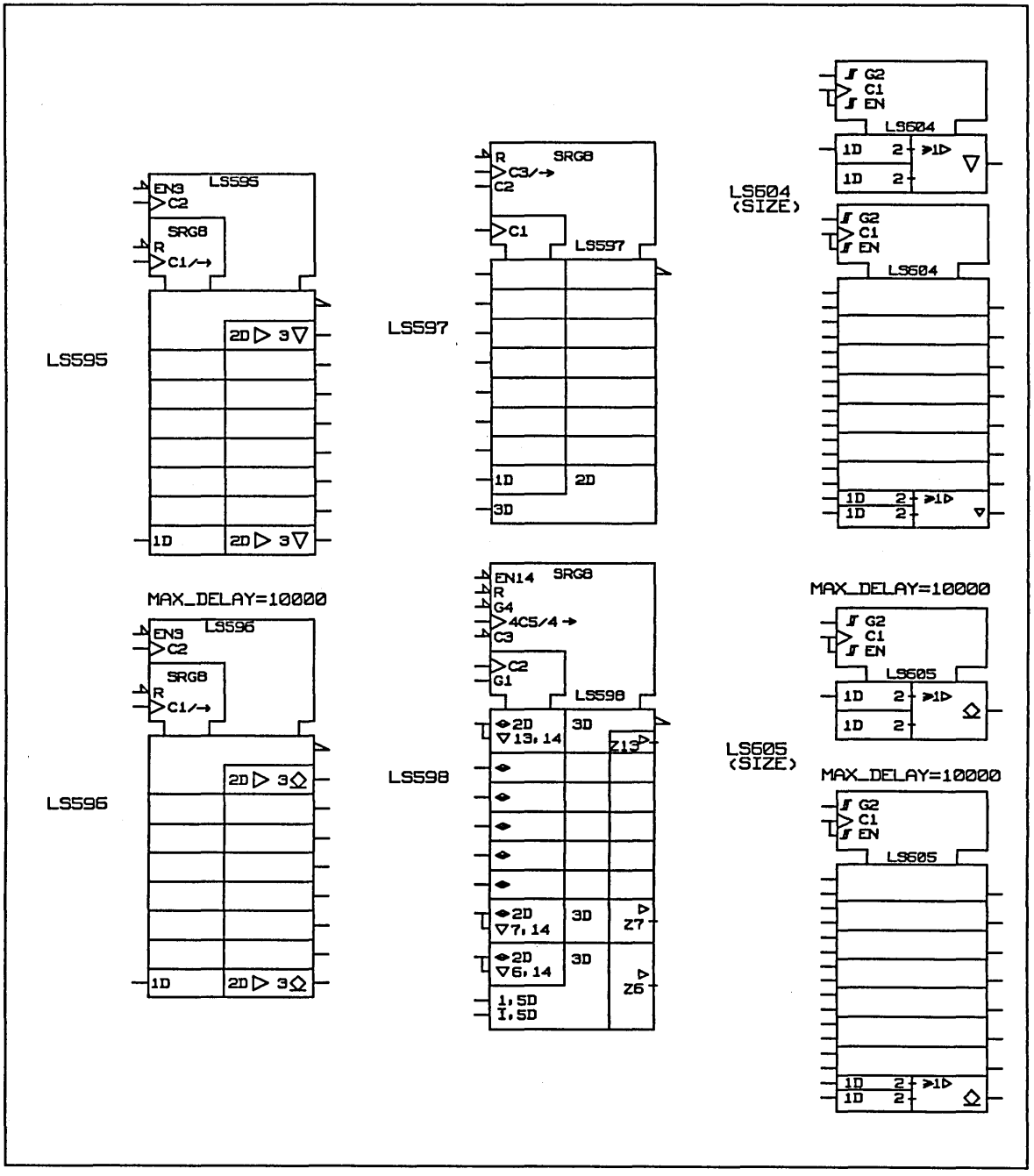

LS378
(SIZE)
G1
1C2
LS378
2D
LS379
(SIZE)
LS379
LS381
ALU
M
(1/2)BI
3CI
(1/2/3)CP
(1/2/3)CG
LS381
P
Q
LS382
(1/2)BO
3CO
BO/CO
=1
LS385
(SIZE)
Z1
C2
LS385
Σ/P_Q
M3
R
Z4
LS386
(SIZE)
=1
LS386
LS390
CT=0
CTR
LS390
DIV5
DIV2
CT
LS393
CTRDIV16
LS393

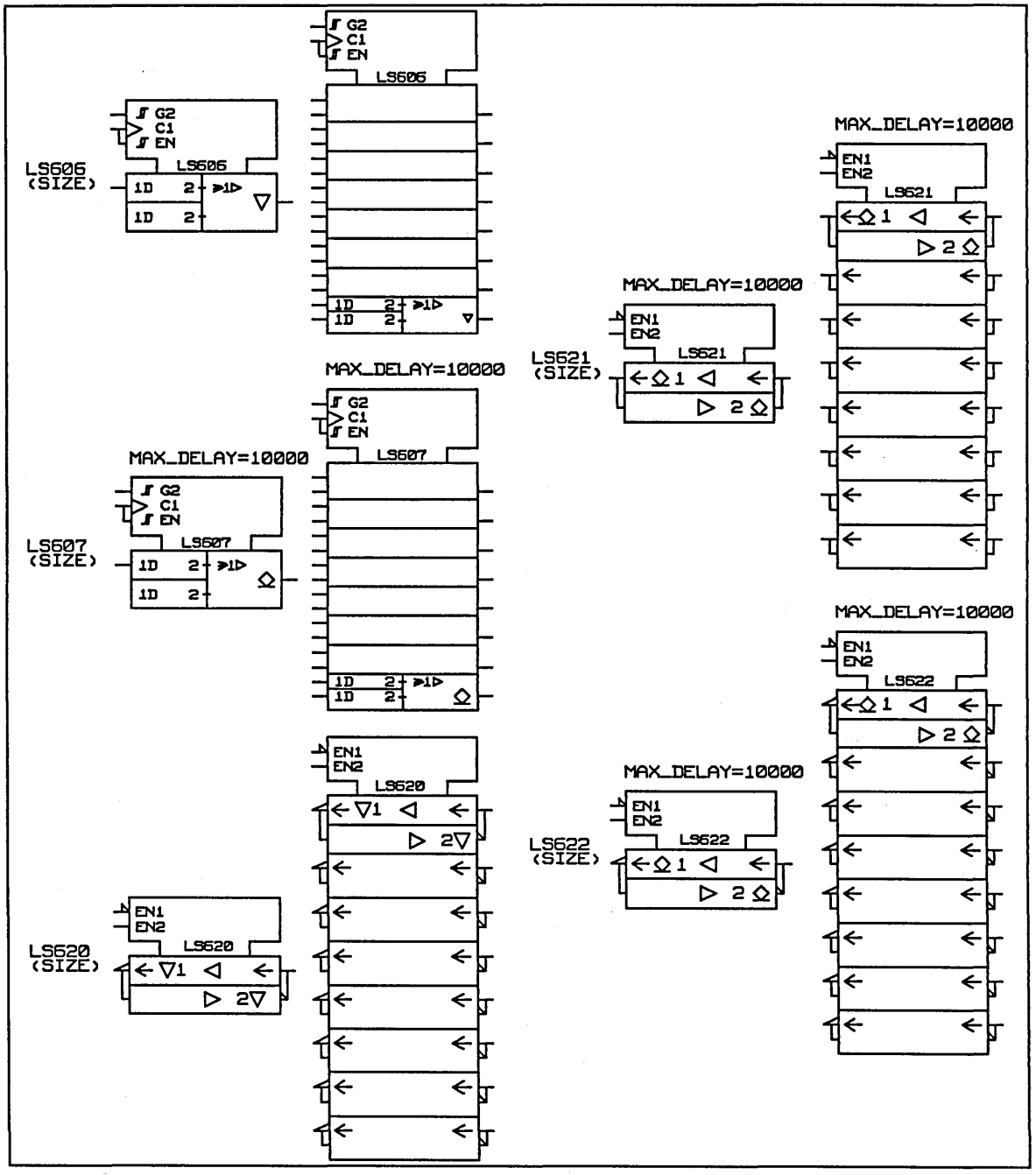

SRG4
R
EN4
M1[LOAD]
M2[SHIFT]
C3/2
LS395A
LS395A
4
4
1,3D
4
1,3D
2,3D
4
EN
4SRG2
C1
LS396
1D
1D
LS396
(SIZE)
G1
MUX
C2
LS398
1,2D
I,2D
LS398
(SIZE)
G1
MUX
C2
LS399
1,2D
I,2D
LS399
(SIZE)
PULSE_WIDTH=10000
LS422
1
&
LS422
R
RI
CX
RX/
CX
PULSE_WIDTH=10000
LS423
&
LS423
R
CX
RX/CX
MAX_DELAY=10000
LS445
BCD/DEC
8
4
2
1
LS445
9
8
7
6
5
4
3
2
1
0
EN
9Z
G9
G10
9EN1[BA]
10EN2[AB]
LS446
LS446
(SIZE)
G9
G10
9EN7[BA]
10EN8[AB]
9EN5[BA]
10EN6[AB]
9EN3[BA]
10EN4[AB]
9EN1[BA]
10EN2[AB]
LS446
7
8
5
6
3
4
1
2

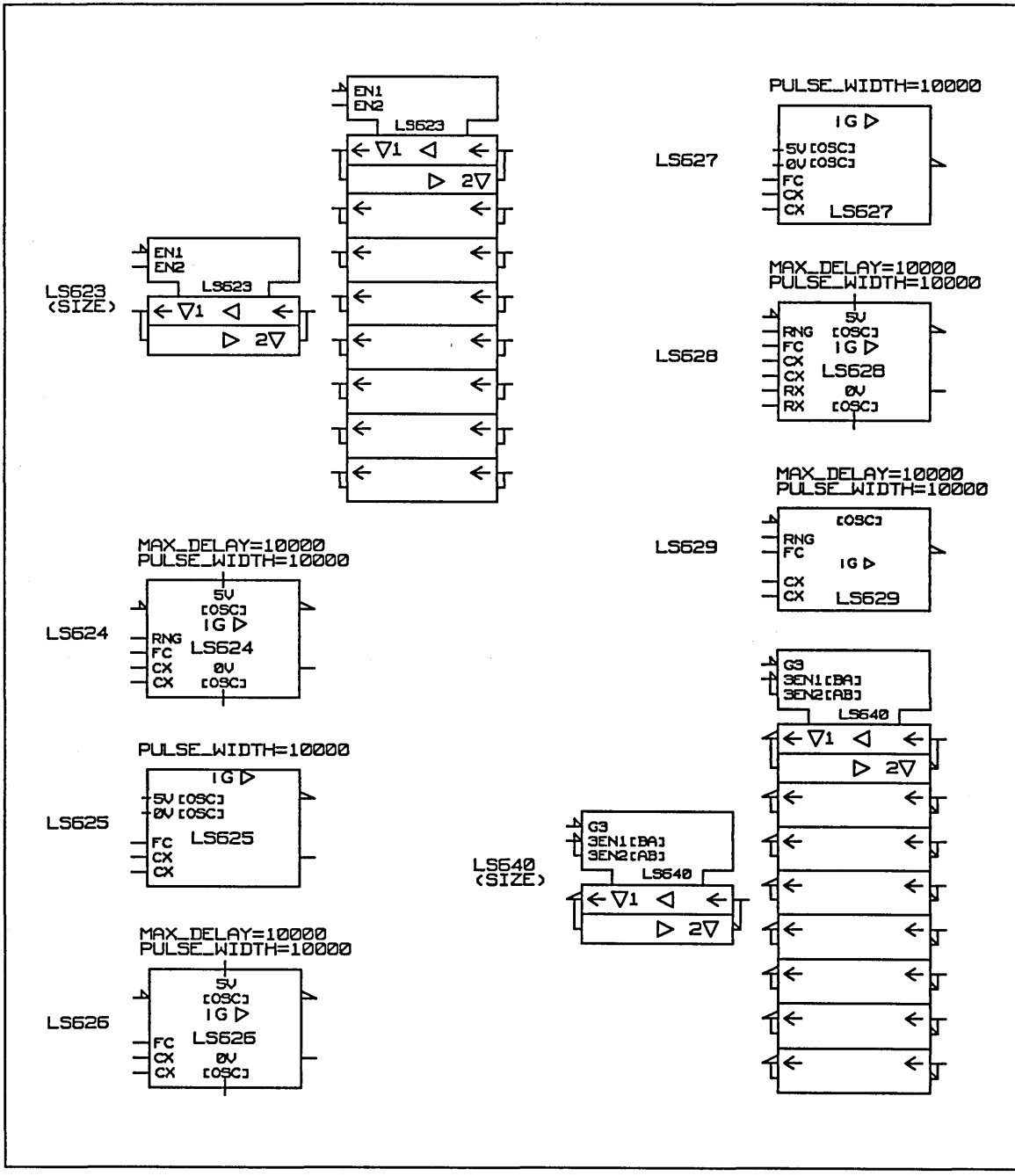

MAX_DELAY=10000
BIN/7-SEG
LS447
G21
CT=0
LS447
MAX_DELAY=10000
G10
LS448
LS448
(SIZE)
MAX_DELAY=10000
G10
LS448
LS449
(SIZE)
G9
G10
LS449
LS465
(SIZE)
LS465
LS466
(SIZE)
LS466
LS467
(SIZE)
LS467
LS468
(SIZE)
LS468
EN

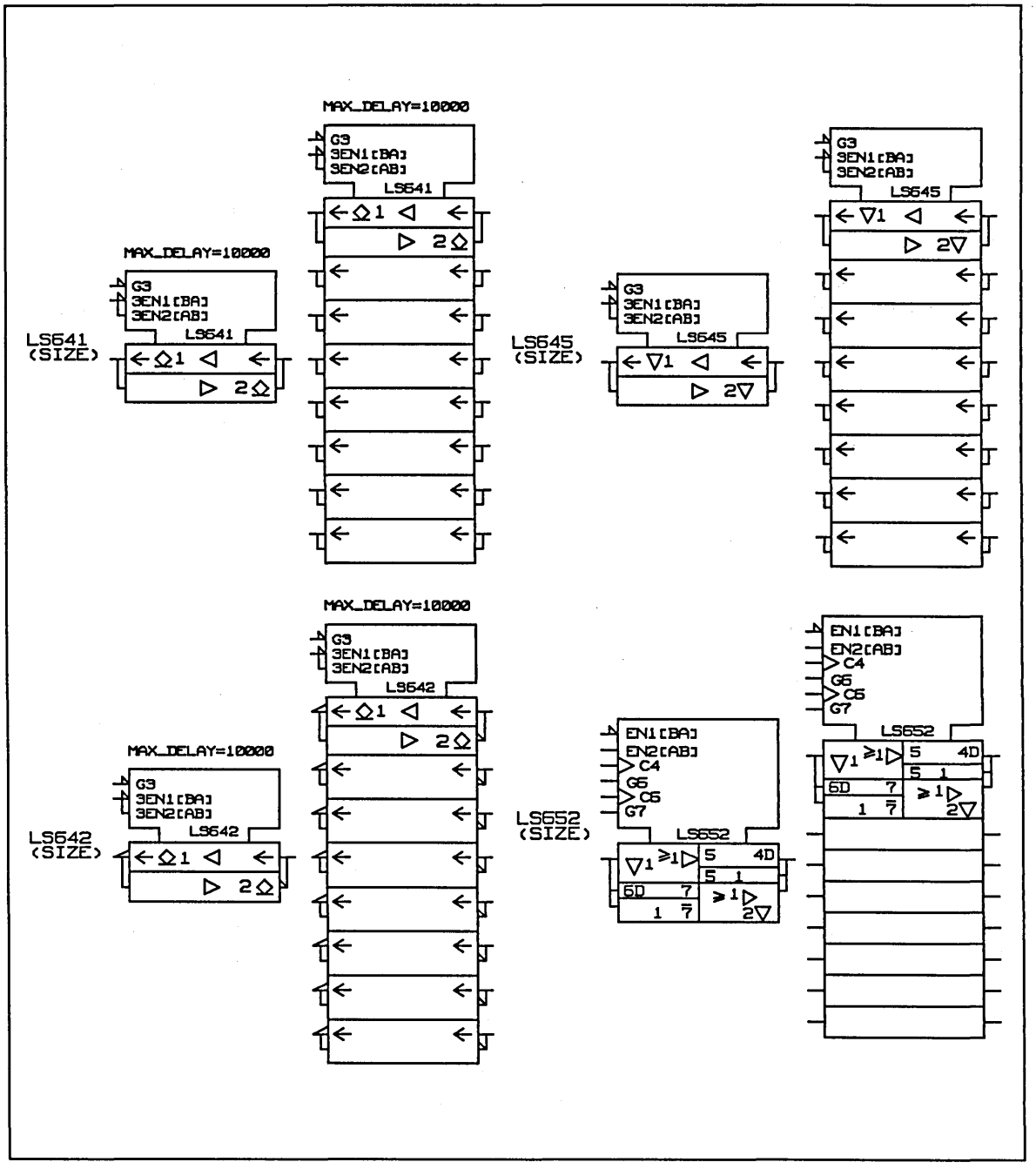

LS490
CTRDIV10
CT=0
CT=9
CT
3
0
LS490
LS533
(SIZE)
EN
C1
1D
LS533
LS534
(SIZE)
LS534
LS540
(SIZE)
&
EN
LS540
LS541
(SIZE)
LS541
CTRDIV16
EN10
M1[UP]
M2[DOWN]
CT=0
LS569
3,5D
10
G8
5CT=0

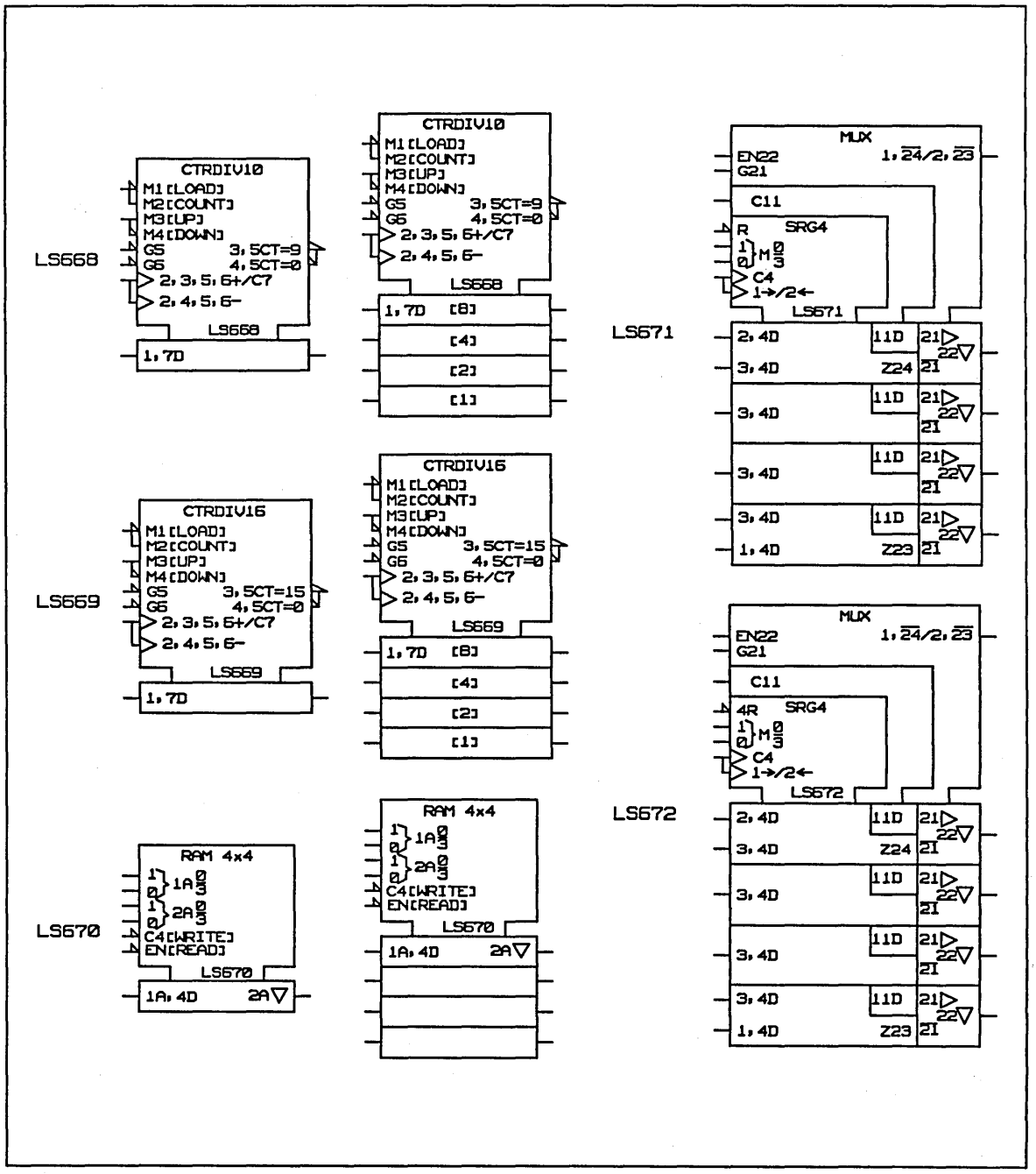

LS590
EN3
C2
CTR8
G1
1+ (CT=255)Z4
CT=0
4
LS590
2D
3
LS592
CT=0
CTR8
G3
3+
CT=255
C2
LS592
C1
1D
2D
MAX_DELAY=10000
LS591
LS593
&
EN5
>1
G4
4+
C3
1C2
5,6
3D
Z5

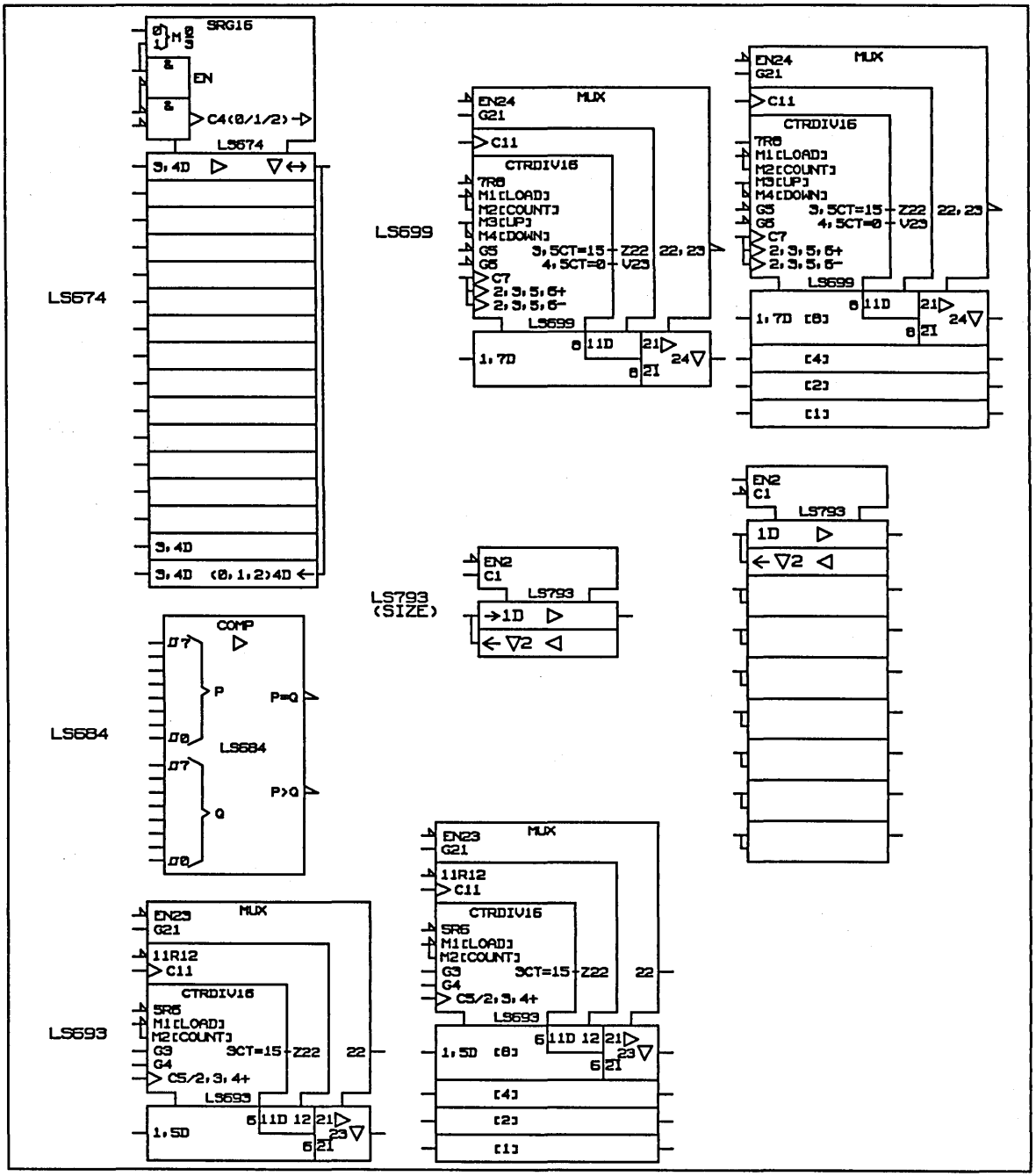

LS595
EN3
C2
SRG8
R
C1/→
LS595
2D ▷ 3▽
1D
2D ▷ 3▽
LS597
R
SRG8
C3/→
C2
C1
LS597
1D
2D
3D
LS604
(SIZE)
G2
C1
EN
LS604
1D
2
≥1▷
LS604
MAX_DELAY=10000
LS596
EN3
C2
SRG8
R
C1/→
LS596
2D ▷ 3◇
1D
2D ▷ 3◇
LS598
EN14
SRG8
R
G4
4C5/4→
C3
C2
G1
LS598
2D
▽13, 14
3D
Z13
2D
▽7, 14
3D
Z7
2D
▽6, 14
3D
Z6
1, 5D
I, 5D
LS605
(SIZE)
MAX_DELAY=10000
G2
C1
EN
LS605
1D
2
≥1▷
MAX_DELAY=10000
LS605

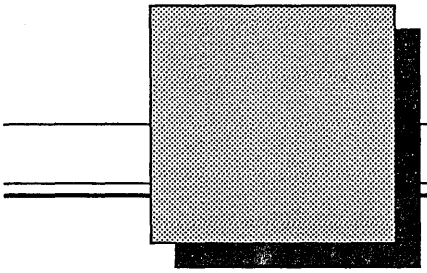

LS606
(SIZE)
LS606
LS607
(SIZE)
LS607
LS620
(SIZE)
LS620
LS621
(SIZE)
LS621
LS622
(SIZE)
LS622
MAX_DELAY=10000
G2
C1
EN
EN1
EN2
1D
2


LS623
(SIZE)
EN1
EN2
LS623
▽1
2▽
LS624
MAX_DELAY=10000
PULSE_WIDTH=10000
5V
[OSC]
IG
RNG
FC
CX
0V
LS625
PULSE_WIDTH=10000
LS626
LS627
PULSE_WIDTH=10000
LS628
MAX_DELAY=10000
PULSE_WIDTH=10000
LS629
MAX_DELAY=10000
PULSE_WIDTH=10000
LS640
(SIZE)
G3
3EN1[BA]
3EN2[AB]
LS640


MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
LS641
LS641
(SIZE)
LS645
(SIZE)
LS642
(SIZE)
LS652
(SIZE)
EN1[BA]
EN2[AB]
C4
G5
C5
G7


LS668
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=9
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS668
1,7D
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=9
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS668
1,7D [8]
[4]
[2]
[1]
LS669
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS669
1,7D
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
LS669
1,7D [8]
[4]
[2]
[1]
LS670
RAM 4x4
1A
2A
C4[WRITE]
EN[READ]
LS670
1A,4D 2A
RAM 4x4
1A
2A
C4[WRITE]
EN[READ]
LS670
1A,4D 2A
LS671
MUX
EN22
G21
1,2/4/2,3/4
C11
R SRG4
M
C4
1→/2←
LS671
2,4D 11D 21 22
3,4D Z24 21
3,4D 11D 21 22 21
3,4D 11D 21 22 21
3,4D 11D 21 22 21
1,4D Z23 21
LS672
MUX
EN22
G21
1,2/4/2,3/4
C11
4R SRG4
M
C4
1→/2←
LS672
2,4D 11D 21 22
3,4D Z24 21
3,4D 11D 21 22 21
3,4D 11D 21 22 21
3,4D 11D 21 22 21
1,4D Z23 21


LS674
LS699
LS793 (SIZE)
LS684
LS693
SRG16
EN
C4(0/1/2)
3,4D
3,4D (0,1,2)4D
EN24
G21
C11
MUX
CTRDIV16
7R8
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15 Z22 22,23
G6 4,5CT=0 V23
C7
2,3,5,6+
2,3,5,6-
LS699
1,7D
11D
21
24
21
[8]
[4]
[2]
[1]
EN2
C1
LS793
1D
2
COMP
P
P=Q
P>Q
Q
LS684
EN23
11R12
5R6
M1[LOAD]
M2[COUNT]
G3 3CT=15 Z22 22
G4
C5/2,3,4+
1,5D
11D 12
23
[8]
[4]
[2]
[1]



The STTL and ANSI STTL Libraries

The STTL Library requires approximately 2330 Kbytes of disk storage, and the ANSI STTL Library requires approximately 2293 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*sttl.lib* or *a74sttl.lib*).

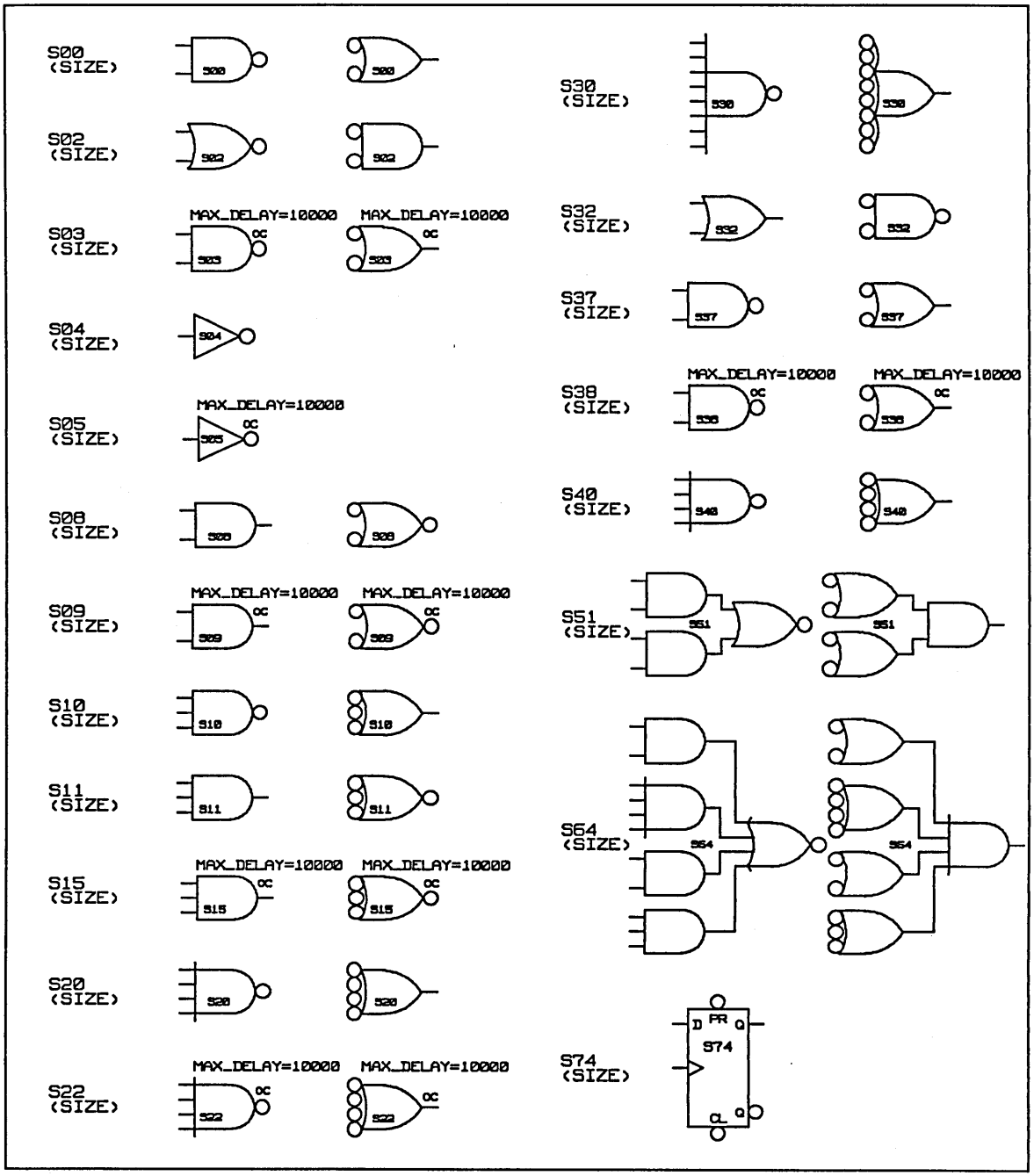
The release level of the STTL and ANSI STTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 72 components:

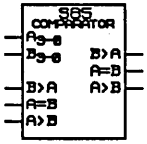
S00	Quad 2-input NAND
S02	Quad 2-input NOR
S03	Quad 2-input open-collector NAND
S04	Hex inverter
S05	Hex open-collector inverter
S08	Quad 2-input AND
S09	Quad 2-input open-collector AND
S10	Triple 3-input NAND
S11	Triple 3-input AND
S15	Triple 3-input open-collector AND
S20	Dual 4-input NAND
S22	Dual 4-input open-collector NAND
S30	8-input NAND
S32	Quad 2-input OR
S37	Quad 2-input NAND buffer
S38	Quad 2-input open-collector NAND buffer
S40	Dual 4-input positive NAND buffer
S51	2-wide 3-input, 2-wide 2-input AND-OR-invert
S64	4-2-3-2 input AND-OR-invert gates
S74	Dual positive-edge-triggered D flip-flop

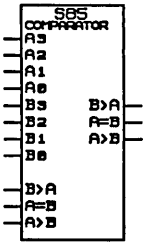
S85	4-bit magnitude comparator
S86	Quad 2-input exclusive-OR
S109	Dual JKbar positive-edge-triggered flip-flop
S112	Dual JK negative-edge-triggered flip-flop
S113	Dual JK negative-edge-triggered flip-flop with preset
S114	Dual JK negative-edge-triggered flip-flop with preset common clear and clock
S124	Dual voltage-controlled oscillators
S132	Quad 2-input positive NAND Schmitt triggers
S133	13-input positive NAND gates
S138	3-to-8 line decoders/multiplexers
S139	Dual 2-to-4 line decoders/multiplexers
S140	Dual 4-input positive NAND 50-ohm line drivers
S148	8-to-3 octal priority encoder
S151	1-of-8 data selectors/multiplexers
S153	Dual 4-line to 1-line data multiplexer
S157	Quad 2-to-1-line non-inverting multiplexer
S158	Quad 2-to-1-line inverting data multiplexer
S162	4-bit synchronous decade counters with synchronous clear
S163	4-bit synchronous binary counters with synchronous clear
S168	Synchronous decade up/down counters
S169	4-bit synchronous binary up/down counters
S174	Hex D-type flip-flops
S175	Quad D-type flip-flops
S181	Arithmetic logic units/function generators
S182	Look-ahead carry generators

S189	64-bit random access memories
S194	4-bit bidirectional shift register
S195	4-bit parallel-access shift register
S197	4-bit binary presetable counter/latch
S201	256-bit random memories
S225	Asynchronous first-in first-out memories
S226	4-bit parallel 3-state latched bus transceiver
S240	Octal inverting 3-state bus transceiver
S241	Octal non-inverting 3-state bus transceiver
S244	Octal non-inverting 3-state bus transceiver
S251	3-state data multiplexer
S253	Dual data selectors/multiplexers
S257	Quad 3-state non-inverting data multiplexer
S258	Quad 3-state inverting data multiplexer
S260	Dual 5-input positive NOR gates
S280	9-bit odd/even parity generators/checkers
S283	4-bit binary full adders
S288	Programmable read-only memory
S299	8-bit bidirectional 3-state shift/storage register
S340	Octal inverting 3-state bus transceiver
S344	Octal non-inverting 3-state bus transceiver
S373	Octal 3-state D-latch with common enable
S374	Octal 3-state positive-edge-triggered D register
S381	Arithmetic logic unit/function generator
S471	Programmable read-only memories
S533	8-bit inverting 3-state latch
S534	8-bit inverting 3-state register


S00 (SIZE)
S02 (SIZE)
S03 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
OC
S04 (SIZE)
S05 (SIZE)
MAX_DELAY=10000
OC
S08 (SIZE)
S09 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
OC
S10 (SIZE)
S11 (SIZE)
S15 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
OC
S20 (SIZE)
S22 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
OC
S30 (SIZE)
S32 (SIZE)
S37 (SIZE)
S38 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
OC
S40 (SIZE)
S51 (SIZE)
S64 (SIZE)
S74 (SIZE)
D
PR
Q
S74
CL
Q

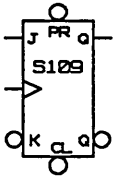
S85



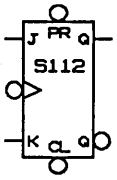


S86
(SIZE)

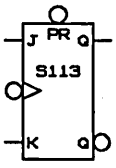
S109
(SIZE)



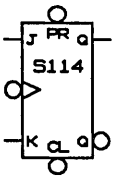
S112
(SIZE)



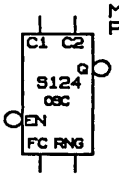
S113
(SIZE)



S114
(SIZE)



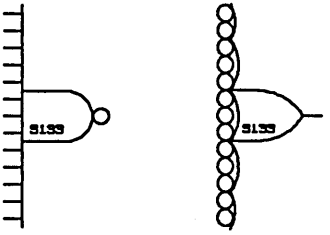
S124



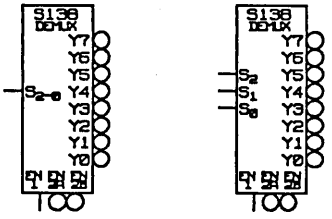
MAX_DELAY=10000
PULSE_WIDTH=10000

S132
(SIZE)

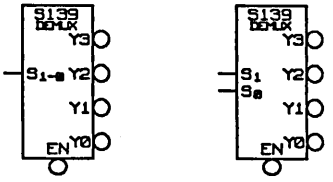
S133
(SIZE)



S138

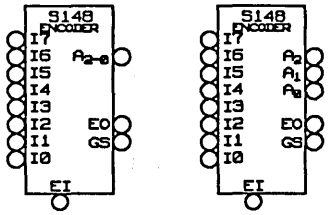


S139

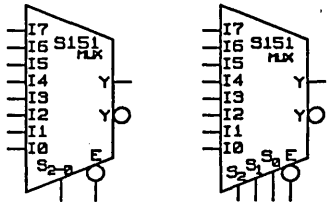


S140
(SIZE)

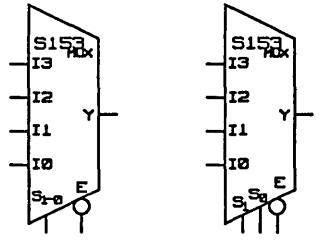
S148



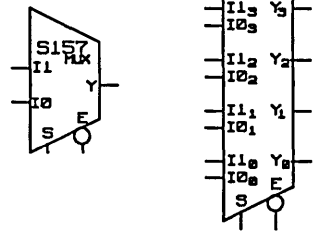
S151
(SIZE)



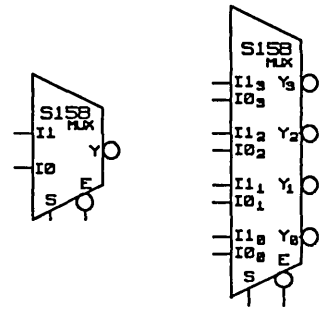
S153
(SIZE)



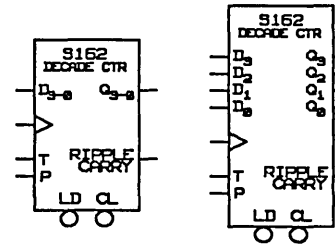
S157
(SIZE)



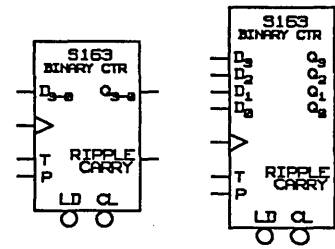
S158
(SIZE)



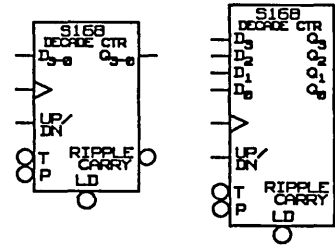
S162

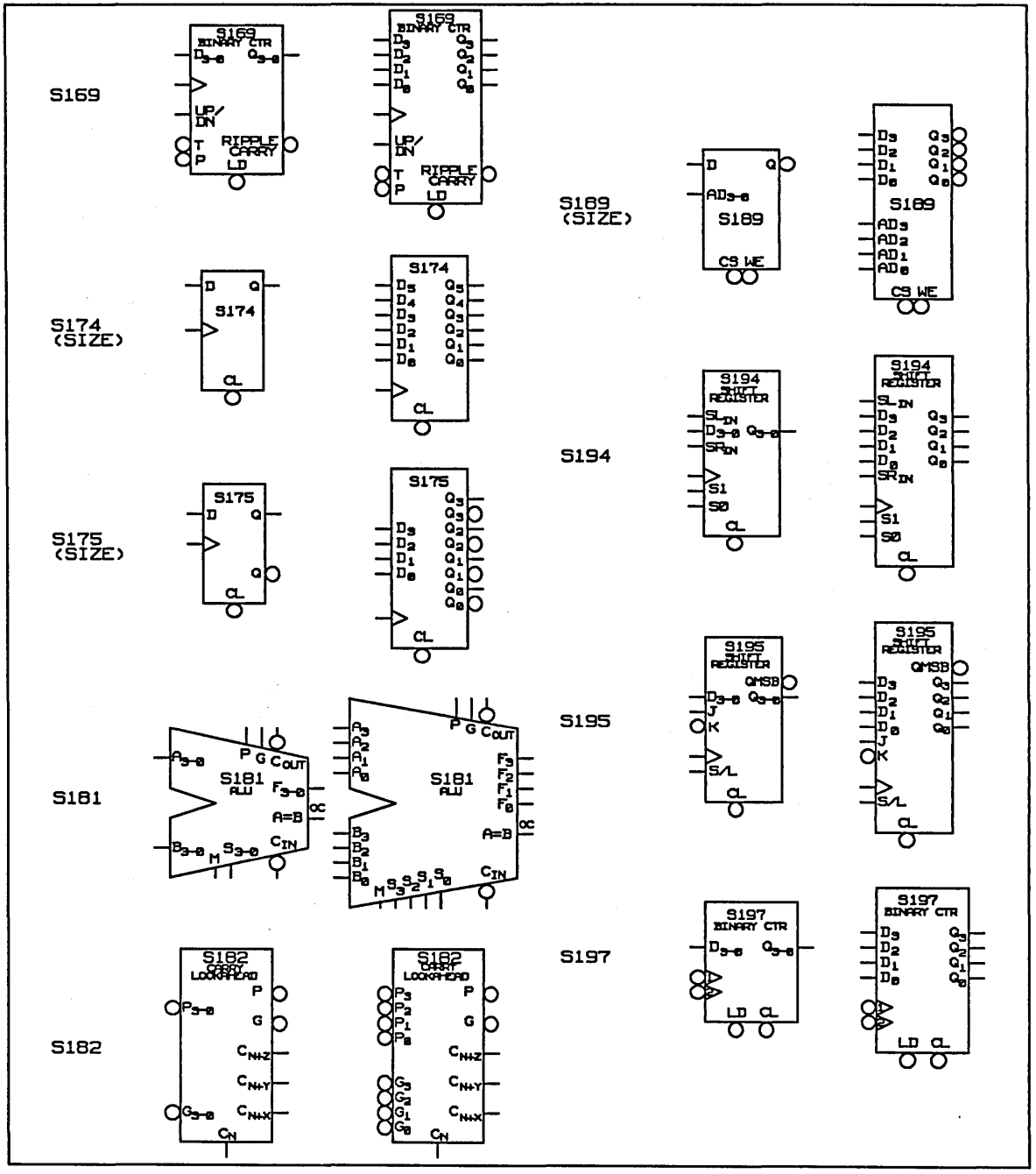


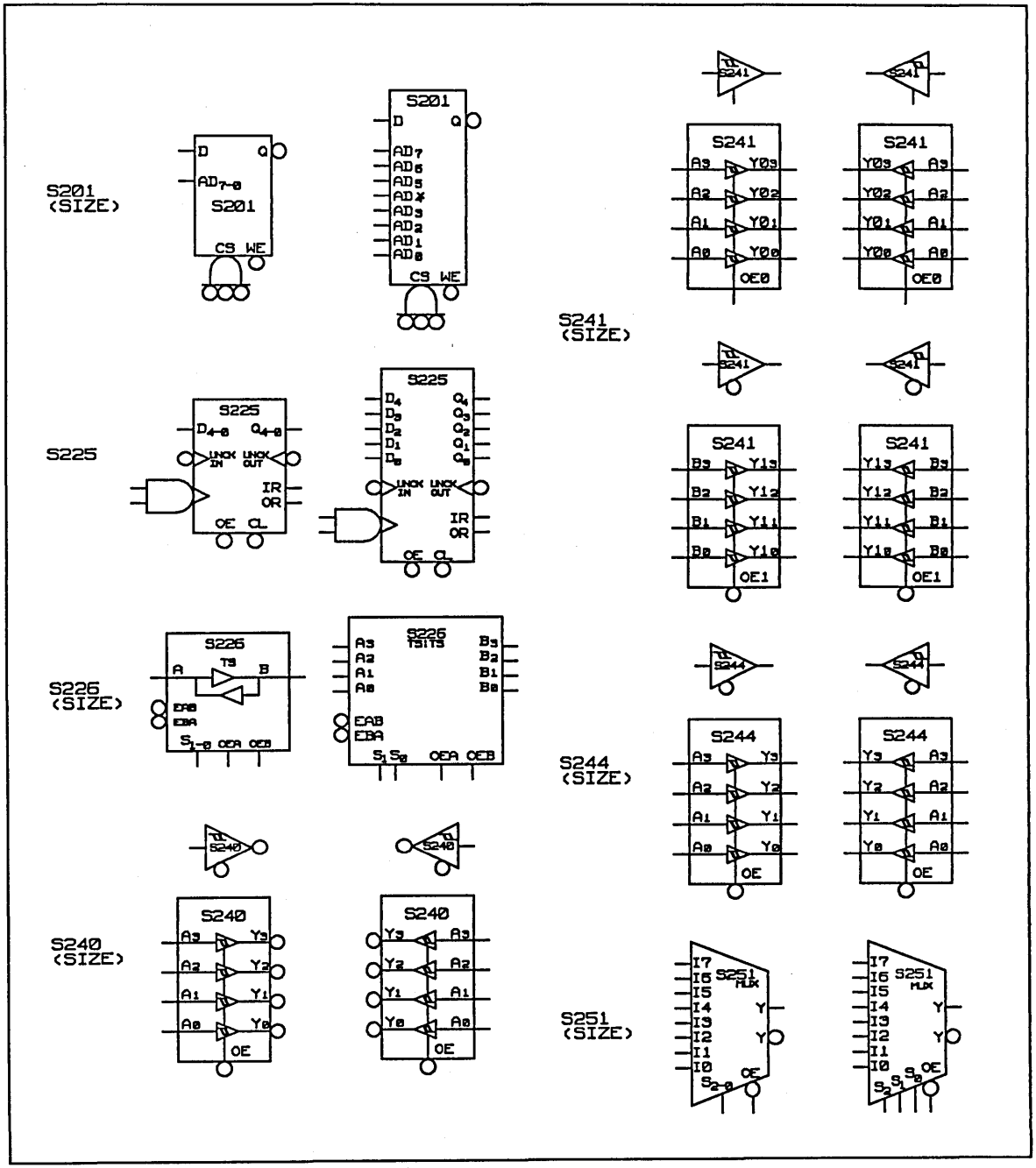
S163



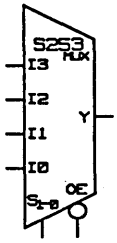
S168

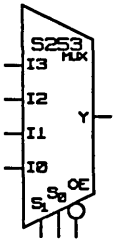



S169
S169
(SIZE)
S174
S174
(SIZE)
S175
S175
(SIZE)
S181
S182
S189
S189
(SIZE)
S194
S195
S197

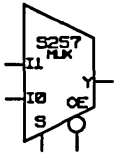

S201
(SIZE)
S225
S226
(SIZE)
S240
(SIZE)
S241
(SIZE)
S244
(SIZE)
S251
(SIZE)
S201
S225
S226
S240
S241
S244
S251
MUX

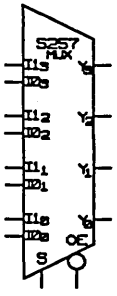
S253
(SIZE)



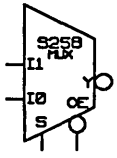


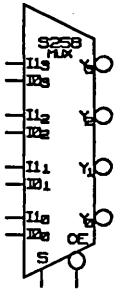
S257
(SIZE)



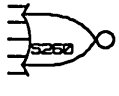


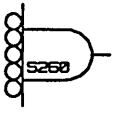
S258
(SIZE)



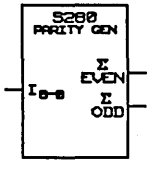


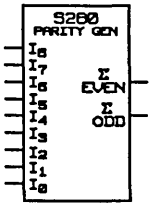
S260
(SIZE)



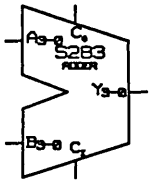


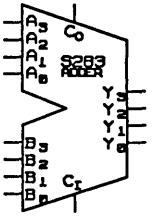
S280



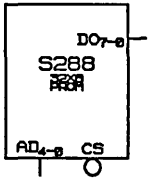


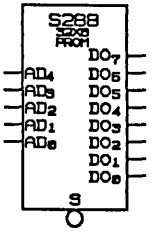
S283



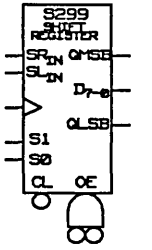


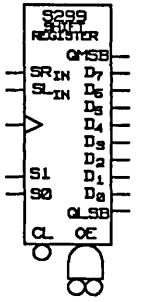
S288



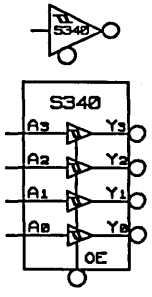


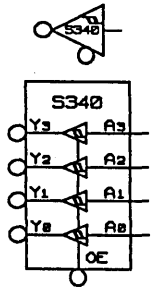
S299

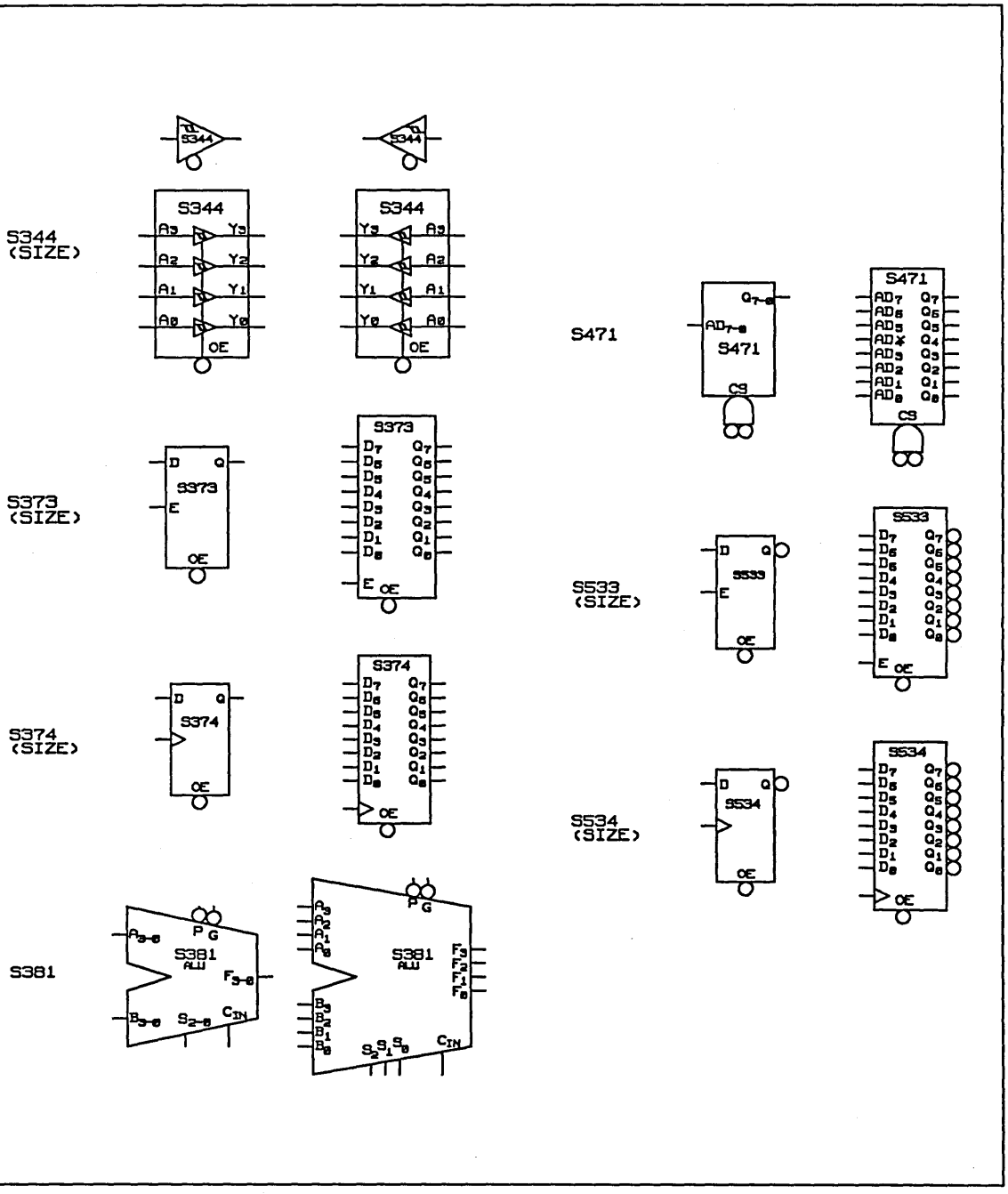


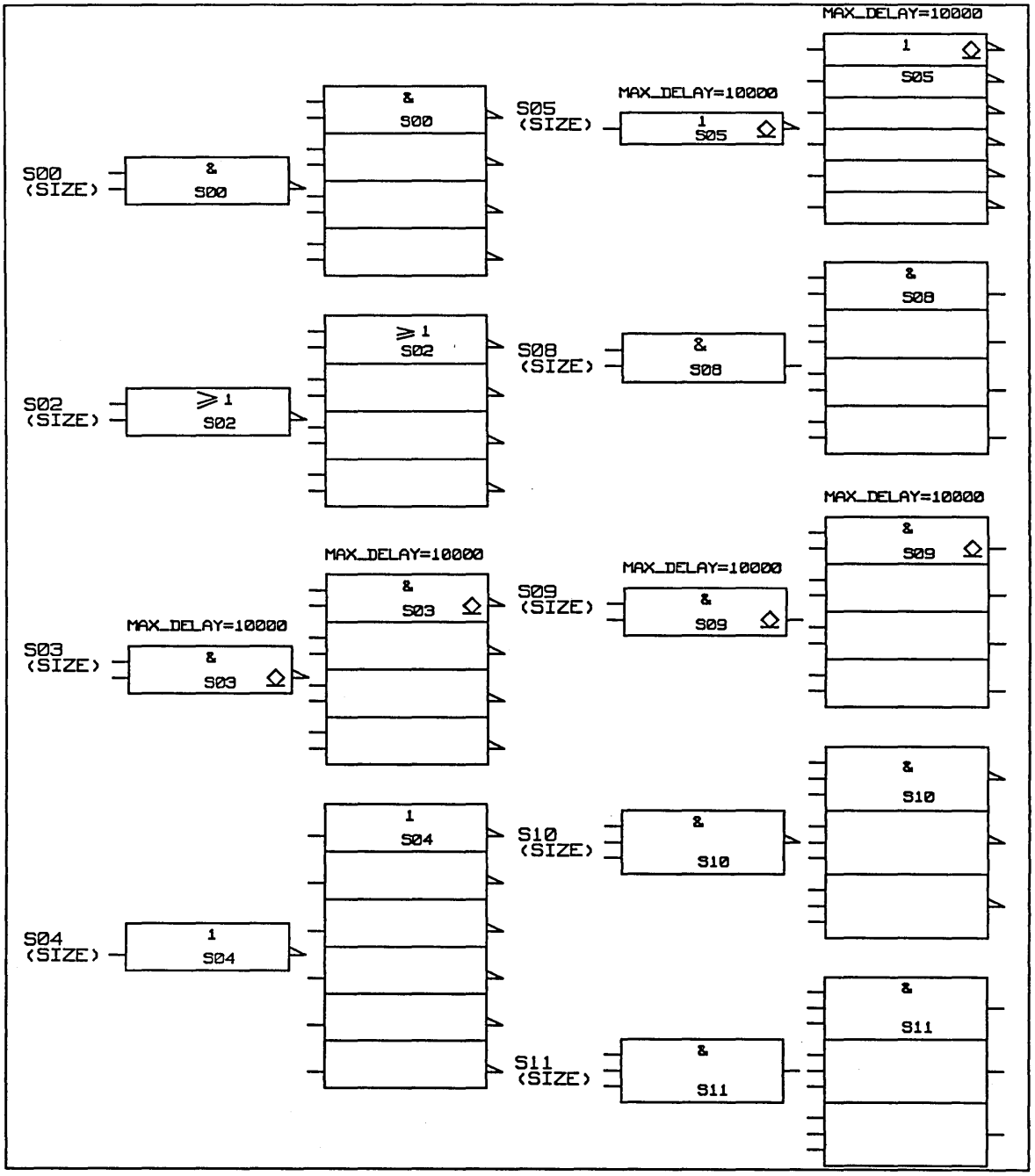


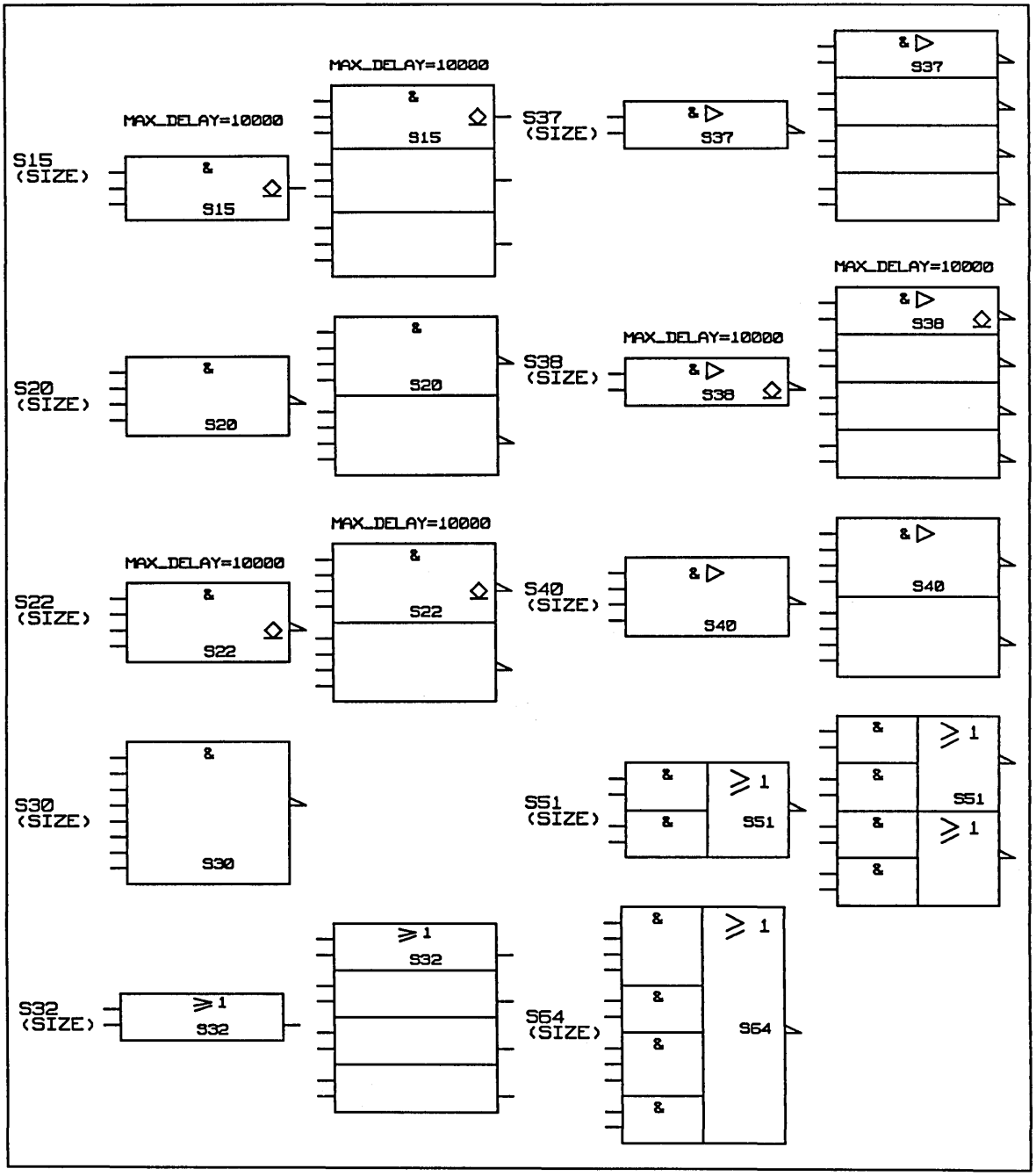
S340
(SIZE)

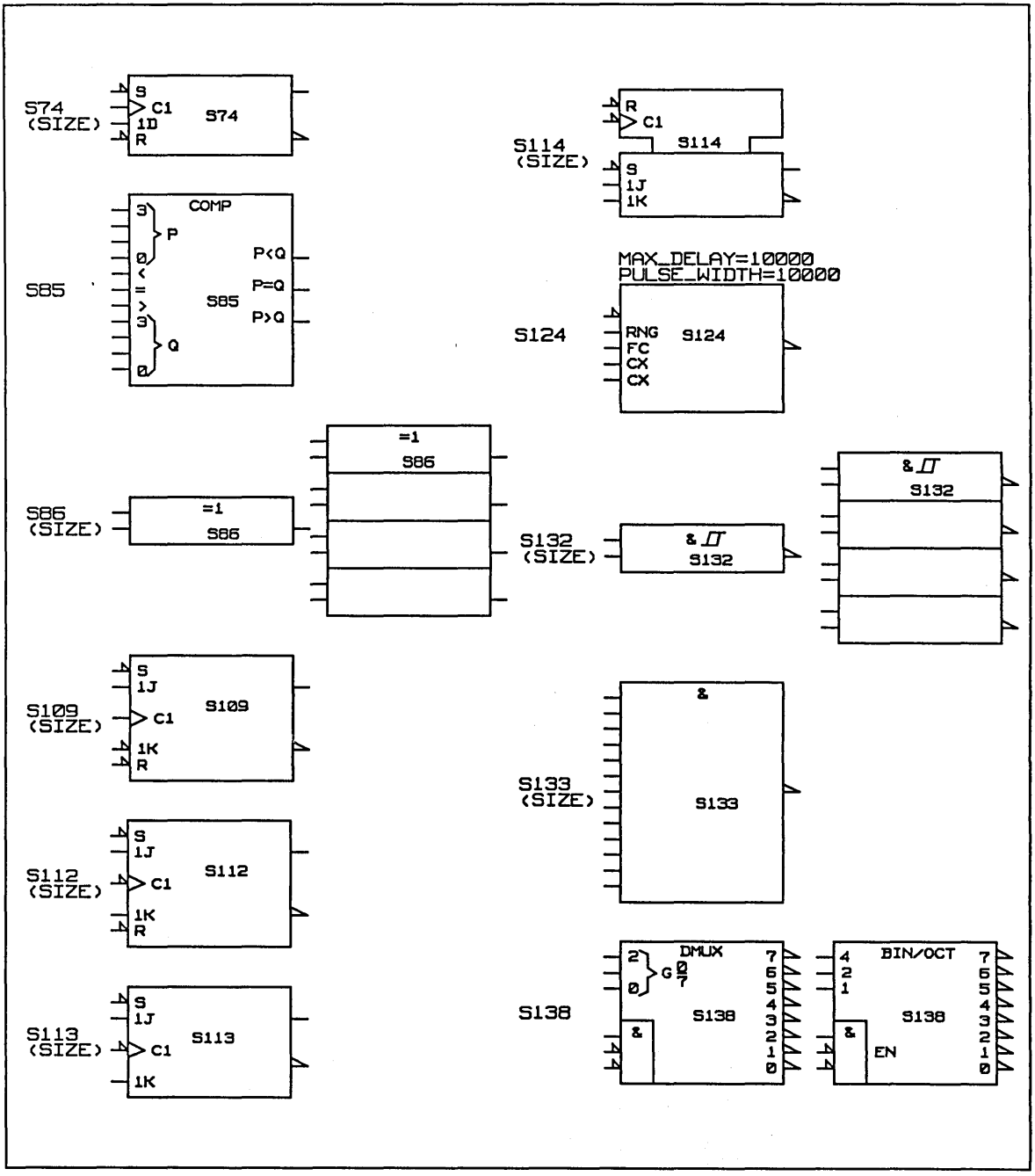


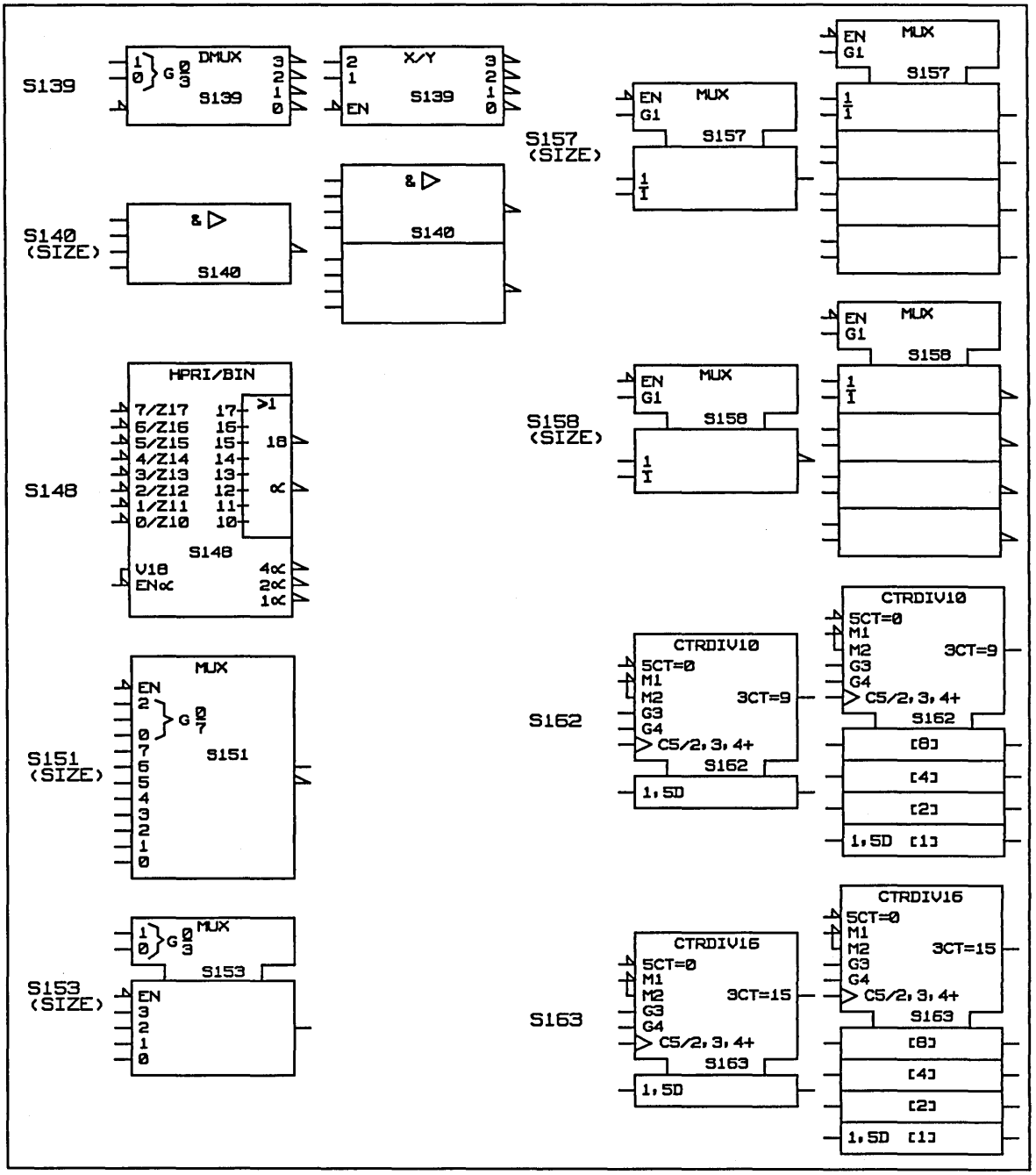


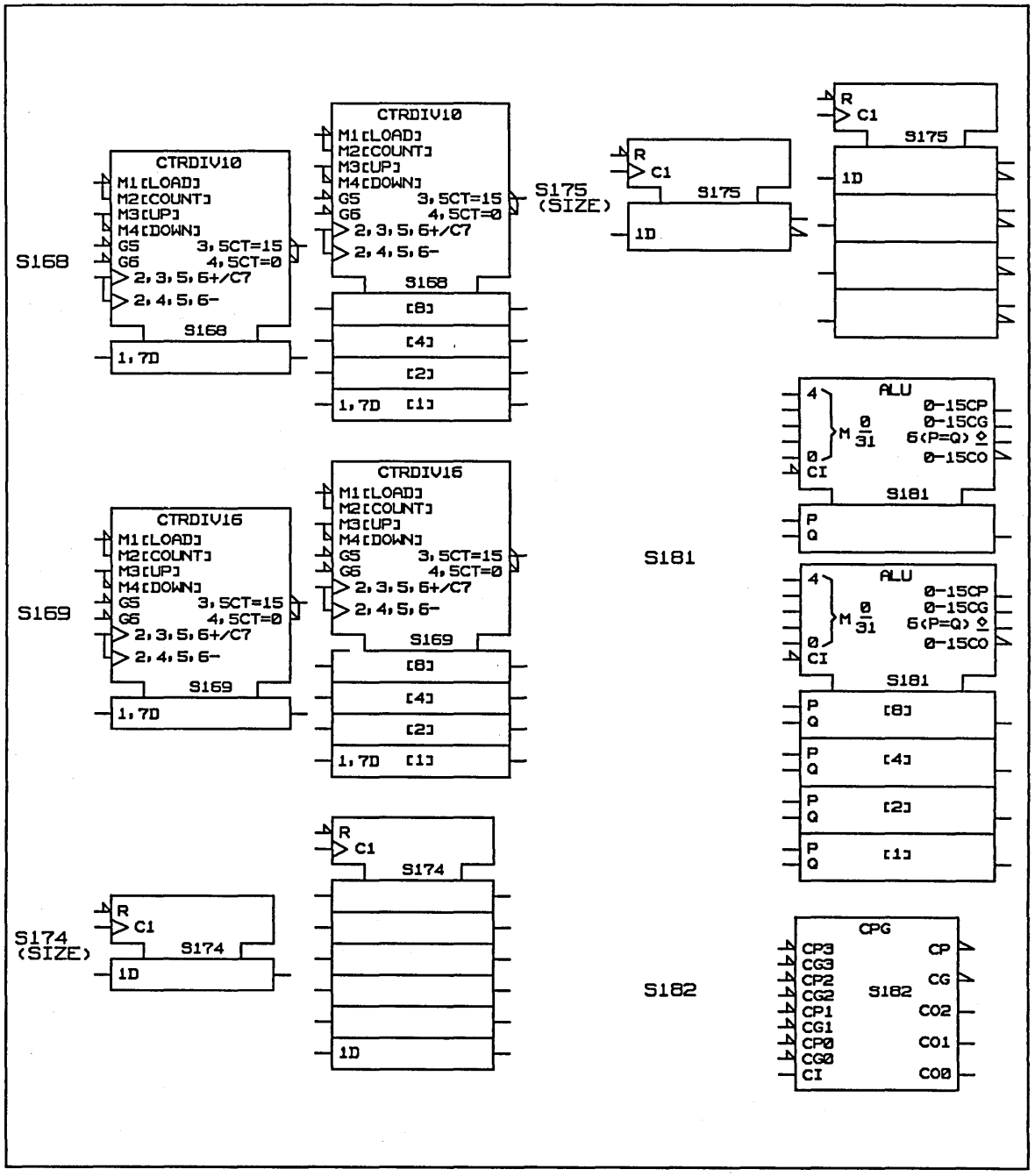

S344
(SIZE)
S373
(SIZE)
S374
(SIZE)
S381
S471
S533
(SIZE)
S534
(SIZE)
S344
S373
S374
S381
ALU
S471
S533
S534

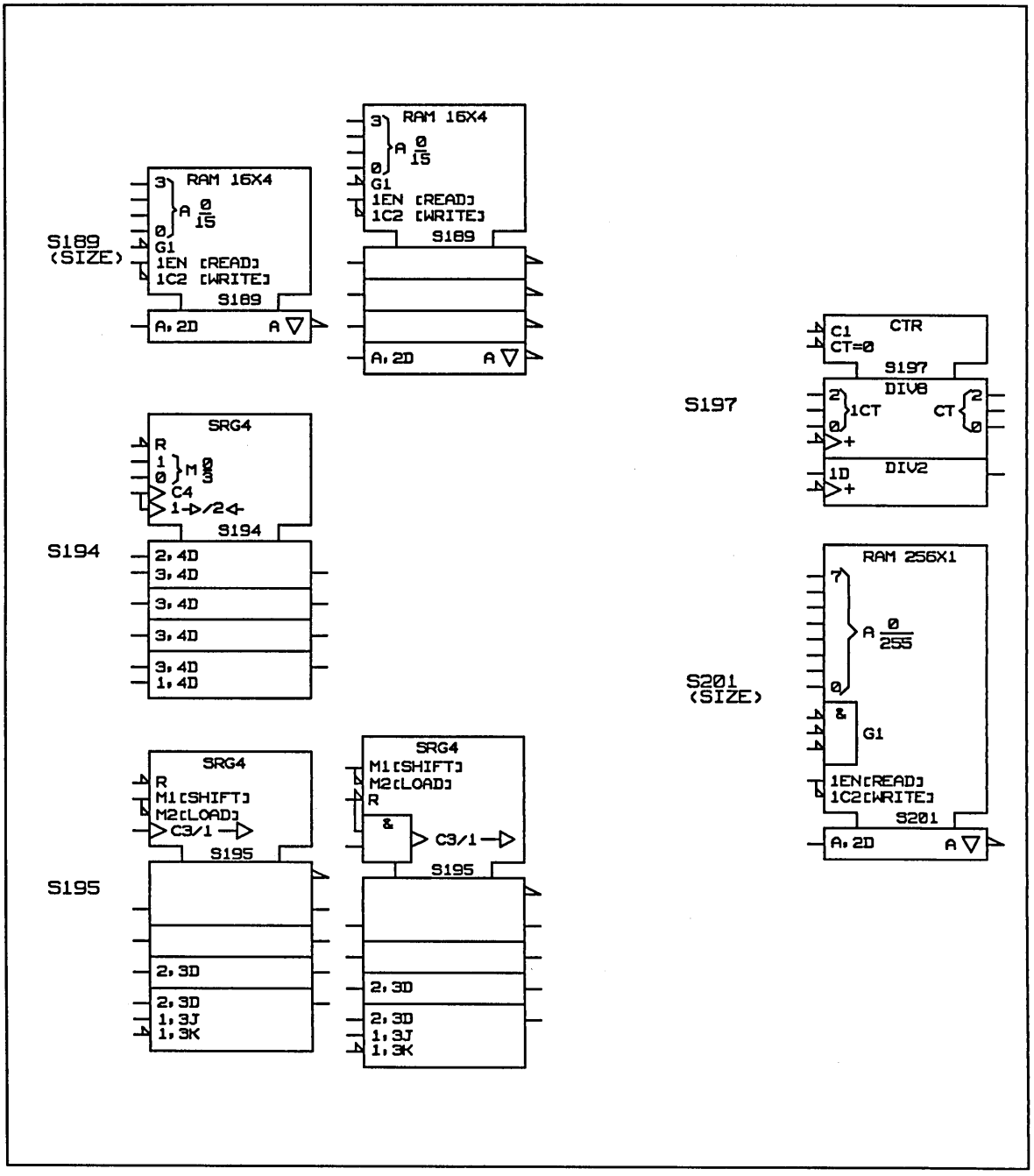

MAX_DELAY=10000
S00 (SIZE)
&
S00
S02 (SIZE)
≥1
S02
S03 (SIZE)
MAX_DELAY=10000
&
S03
S04 (SIZE)
1
S04
S05 (SIZE)
MAX_DELAY=10000
1
S05
S08 (SIZE)
&
S08
S09 (SIZE)
MAX_DELAY=10000
&
S09
S10 (SIZE)
&
S10
S11 (SIZE)
&
S11

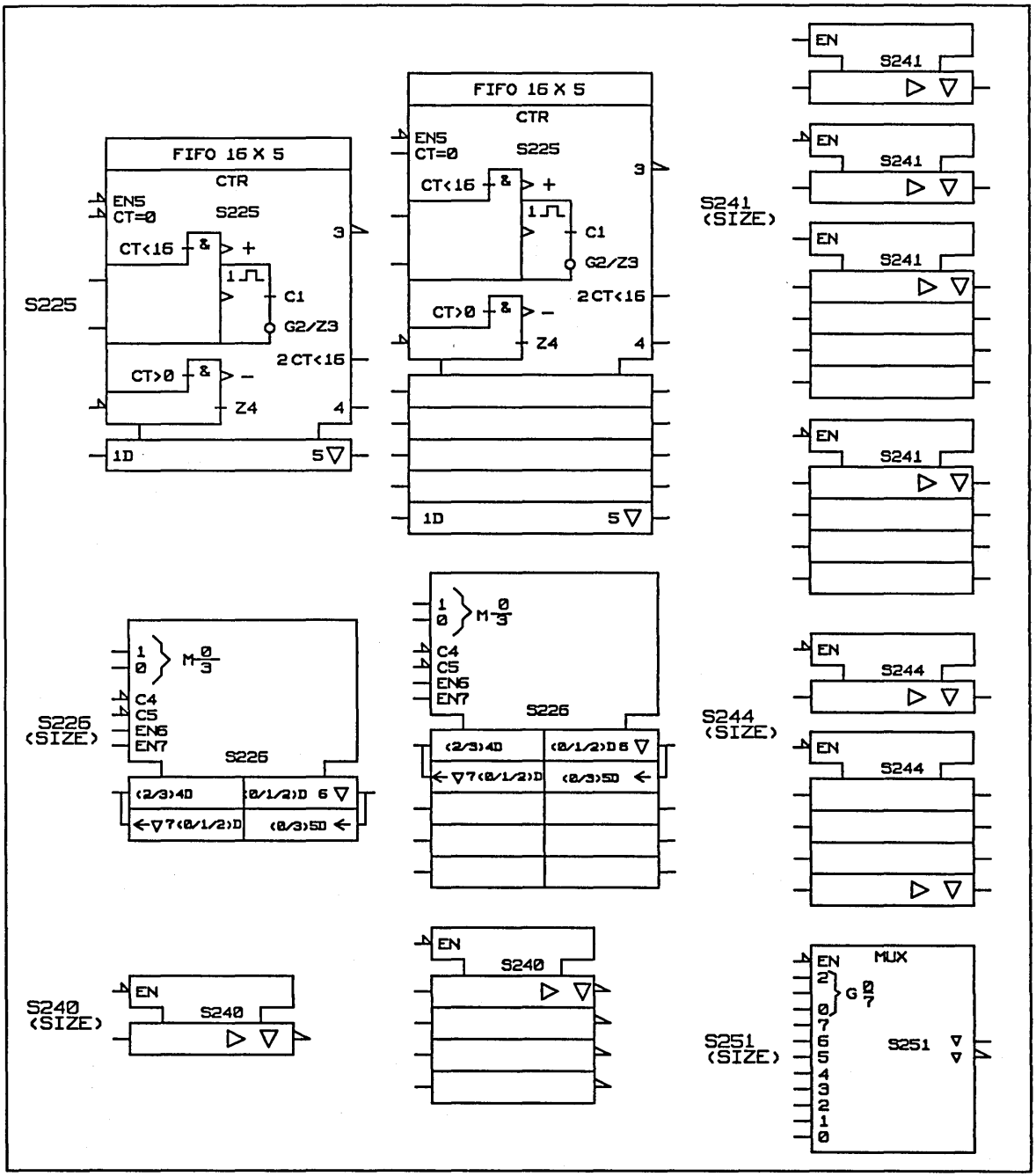

MAX_DELAY=10000
S15
(SIZE)
&
S15
MAX_DELAY=10000
&
S15
S37
(SIZE)
&
S37
&
S37
S20
(SIZE)
&
S20
&
S20
MAX_DELAY=10000
S38
(SIZE)
&
S38
MAX_DELAY=10000
&
S38
MAX_DELAY=10000
S22
(SIZE)
&
S22
MAX_DELAY=10000
&
S22
S40
(SIZE)
&
S40
&
S40
S30
(SIZE)
&
S30
S51
(SIZE)
&
&
≥1
S51
&
&
&
&
≥1
S51
≥1
S32
(SIZE)
≥1
S32
≥1
S32
S64
(SIZE)
&
&
&
&
≥1
S64

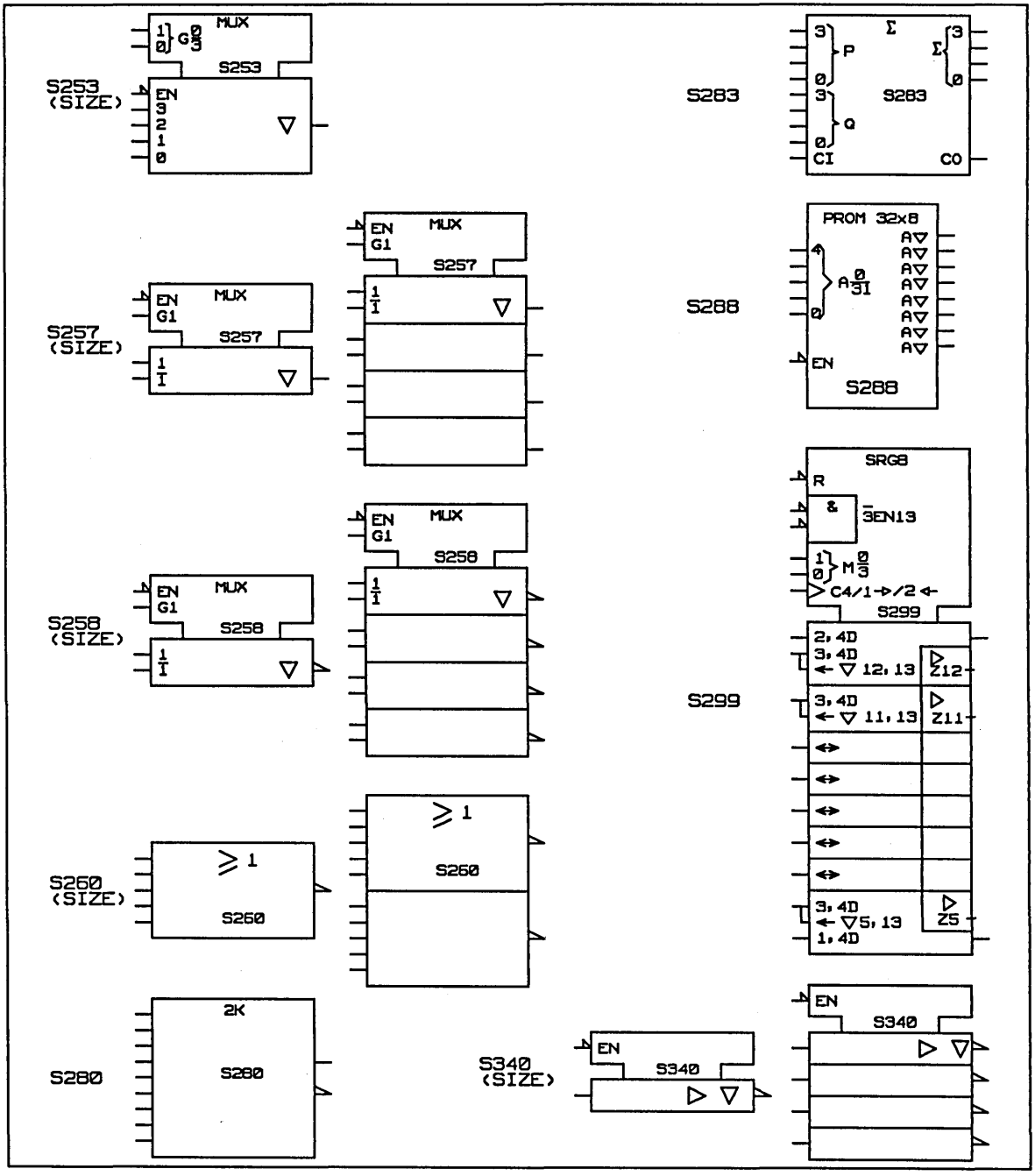

S74
(SIZE)
S
C1
1D
R
S74
S85
COMP
P
P<Q
P=Q
P>Q
Q
S86
(SIZE)
=1
S86
S109
(SIZE)
S
1J
C1
1K
R
S109
S112
(SIZE)
S112
S113
(SIZE)
S113
S114
(SIZE)
R
S114
1J
1K
MAX_DELAY=10000
PULSE_WIDTH=10000
S124
RNG
FC
CX
S124
S132
(SIZE)
&
S132
S133
(SIZE)
S133
S138
DMUX
G
S138
BIN/OCT
EN

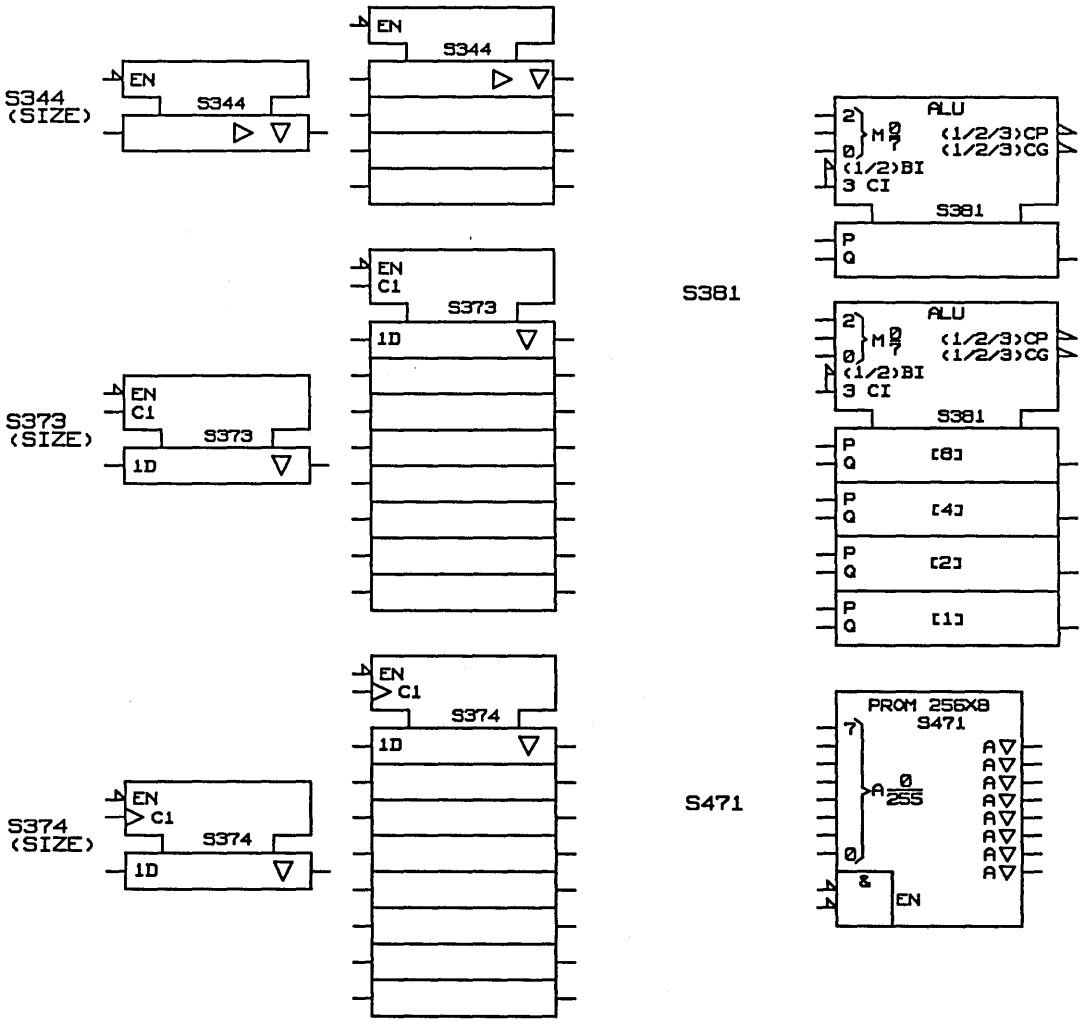

S139
DMUX
S139
X/Y
S139
S140
(SIZE)
&
S140
S148
HPRI/BIN
S148
S151
(SIZE)
MUX
S151
S153
(SIZE)
MUX
S153
S157
(SIZE)
MUX
S157
S158
(SIZE)
MUX
S158
S162
CTRDIV10
S162
S163
CTRDIV16
S163

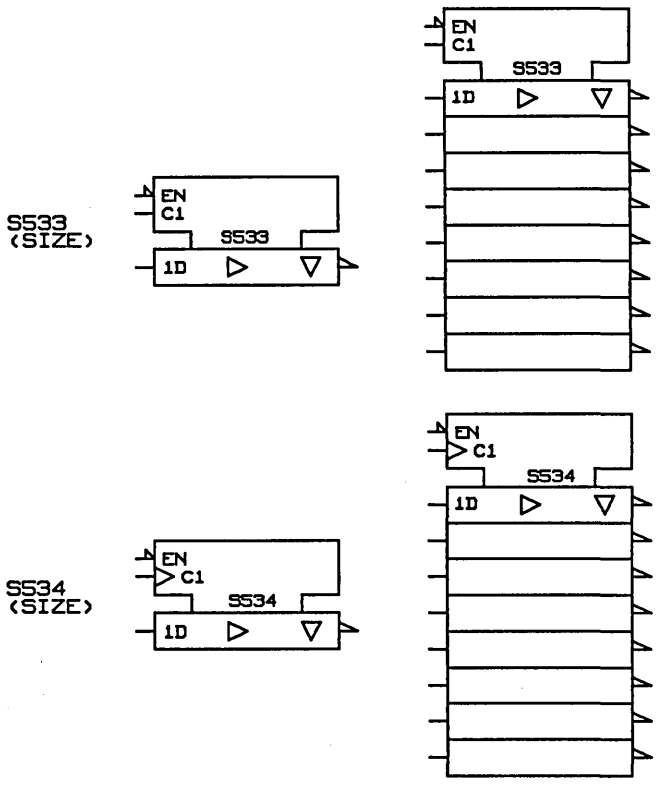

S168
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
S168
1,7D
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
S168
[8]
[4]
[2]
1,7D [1]
S175 (SIZE)
R
C1
S175
1D
R
C1
S175
1D
S169
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
S169
1,7D
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
S169
[8]
[4]
[2]
1,7D [1]
S174 (SIZE)
R
C1
S174
1D
R
C1
S174
1D
S181
ALU
4
M
0
31
0
CI
0-15CP
0-15CG
6(P=Q)
0-15CO
S181
P
Q
ALU
S181
[8]
[4]
[2]
[1]
S182
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
CP
CG
CO2
CO1
CO0
S182

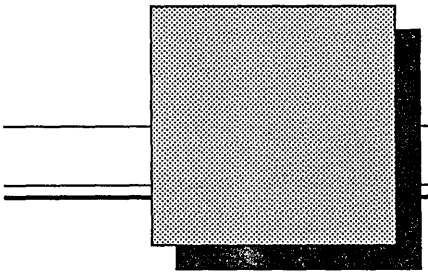

S189
(SIZE)
RAM 16X4
3
A 0
15
0
G1
1EN [READ]
1C2 [WRITE]
S189
A, 2D
A
RAM 16X4
3
A 0
15
0
G1
1EN [READ]
1C2 [WRITE]
S189
A, 2D
A
S197
CTR
C1
CT=0
S197
DIV8
2
1CT
0
+
CT
2
0
1D
DIV2
+
S194
SRG4
R
1
0
M 0
3
C4
1-▷/2◁-
S194
2, 4D
3, 4D
3, 4D
3, 4D
3, 4D
1, 4D
S201
(SIZE)
RAM 256X1
A 0
255
0
&
G1
1EN [READ]
1C2 [WRITE]
S201
A, 2D
A
S195
SRG4
R
M1 [SHIFT]
M2 [LOAD]
C3/1
S195
2, 3D
2, 3D
1, 3J
1, 3K
SRG4
M1 [SHIFT]
M2 [LOAD]
R
&
C3/1
S195
2, 3D
2, 3D
1, 3J
1, 3K


FIFO 16 X 5
CTR
EN5
CT=0
S225
CT<16
&
+
1
C1
G2/Z3
CT>0
2CT<16
Z4
4
3
1D
5
S225
FIFO 16 X 5
CTR
EN5
CT=0
S225
CT<16
&
+
1
C1
G2/Z3
CT>0
2CT<16
Z4
4
3
1D
5
EN
S241
S241
(SIZE)
EN
S241
EN
S241
EN
S241
EN
S241
1
0
M
0
3
C4
C5
EN6
EN7
S225
S225
(SIZE)
S225
(2/3)4D
(0/1/2)D 6
7(0/1/2)D
(0/3)5D
1
0
M
0
3
C4
C5
EN6
EN7
S226
(2/3)4D
(0/1/2)D 6
7(0/1/2)D
(0/3)5D
EN
S244
S244
(SIZE)
EN
S244
EN
S240
S240
(SIZE)
EN
S240
EN
MUX
2
0
7
G
0
7
6
5
4
3
2
1
0
S251
S251
(SIZE)


S253
(SIZE)
MUX
S253
EN
S283
S283
P
Q
CI
CO
S257
(SIZE)
EN
G1
MUX
S257
S288
PROM 32x8
S288
S258
(SIZE)
S258
SRG8
R
3EN13
C4/1→/2←
S299
S299
12, 13
11, 13
5, 13
1, 4D
Z12
Z11
Z5
S260
(SIZE)
S260
S280
2K
S280
S340
(SIZE)
S340


S344
(SIZE)
EN
S344
S373
(SIZE)
EN
C1
S373
1D
S374
(SIZE)
EN
C1
S374
1D
S381
ALU
2
0
M
(1/2/3)CP
(1/2/3)CG
(1/2)BI
3 CI
S381
P
Q
[8]
[4]
[2]
[1]
S471
PROM 256X8
S471
7
0
A
255
&
EN


S533
(SIZE)
EN
C1
S533
1D
EN
C1
S533
1D
S534
(SIZE)
EN
C1
S534
1D
EN
C1
S534
1D



The ASTTL and ANSI ASTTL Libraries

The ASTTL Library requires approximately 2810 Kbytes of disk storage, and the ANSI ASTTL Library requires approximately 2859 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*asttl.lib* or *a74asttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books.

The release level of the ASTTL and ANSI ASTTL Libraries is 9.0.

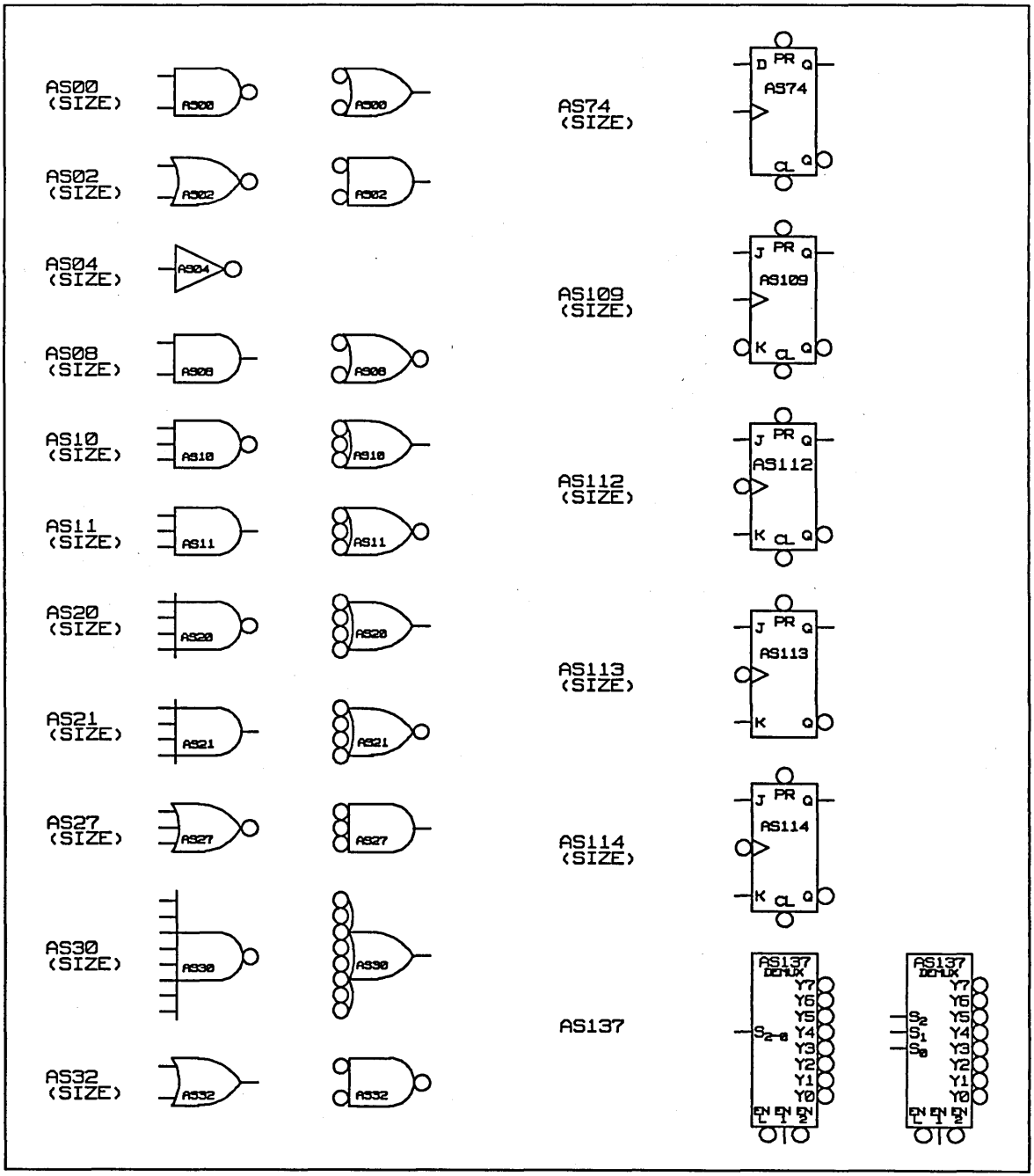
Each library contains body drawings and physical, timing, and simulation models for the following 80 components:

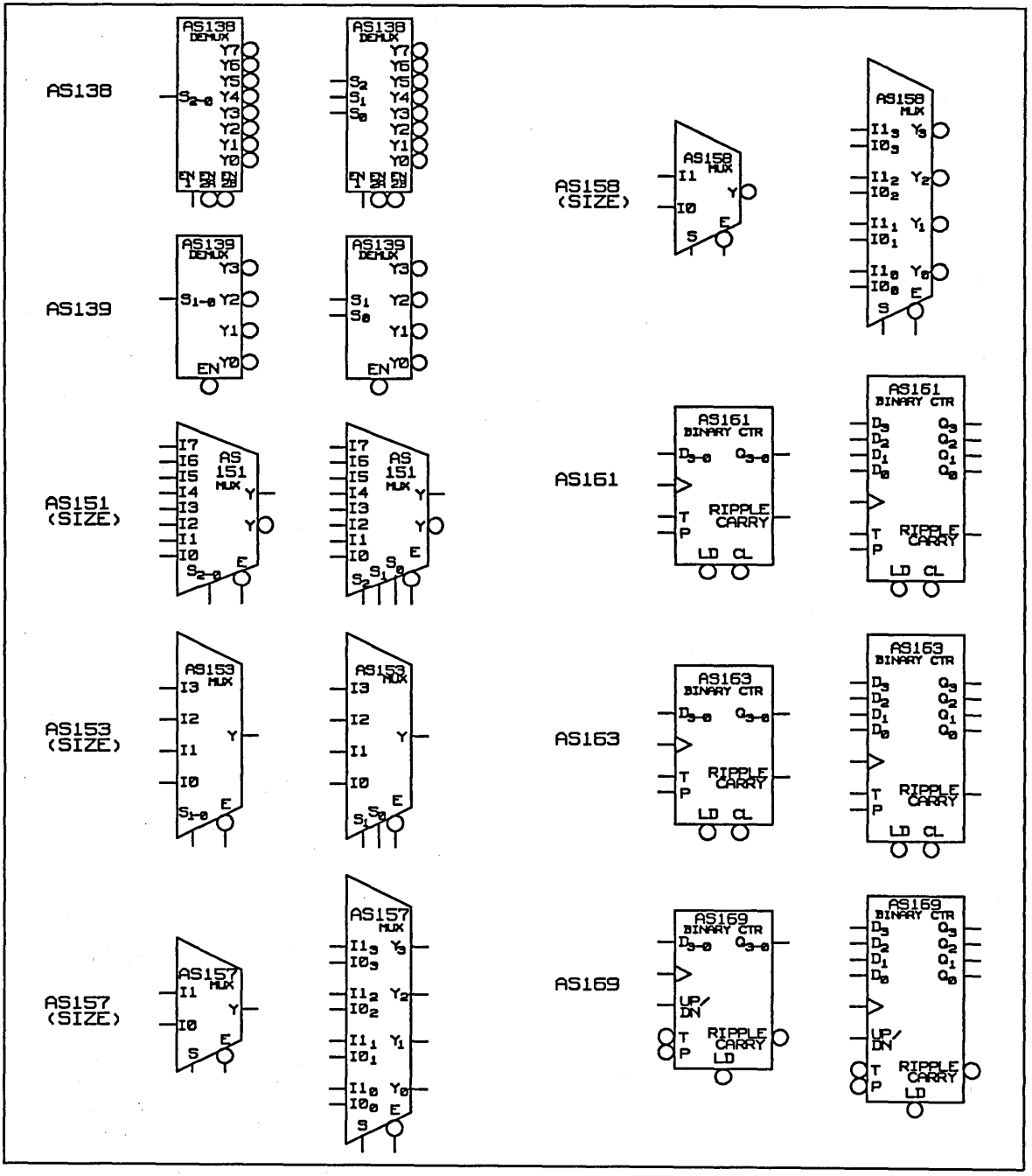
AS00	Quad 2-input NAND
AS02	Quad 2-input NOR
AS04	Hex inverter
AS08	Quad 2-input AND
AS10	Triple 3-input NAND
AS11	Triple 3-input AND
AS20	Dual 4-input NAND
AS21	Dual 4-input AND
AS27	Triple 3-input NOR
AS30	8-input NAND
AS32	Quad 2-input OR
AS74	Dual positive-edge-triggered D flip-flop
AS109	Dual JKbar positive-edge-triggered flip-flop with clear and preset
AS112	Dual JK negative-edge-triggered flip-flop with clear and preset
AS113	Dual JK negative-edge-triggered flip-flop with preset
AS114	Dual JK negative-edge-triggered flip-flop with preset common clear and clock
AS137	3-to-8 line decoders/multiplexer with address latch
AS138	3-to-8 line decoders/multiplexer
AS139	Dual 2-to-4 line decoders/multiplexer
AS151	1 of 8 data selectors/multiplexer

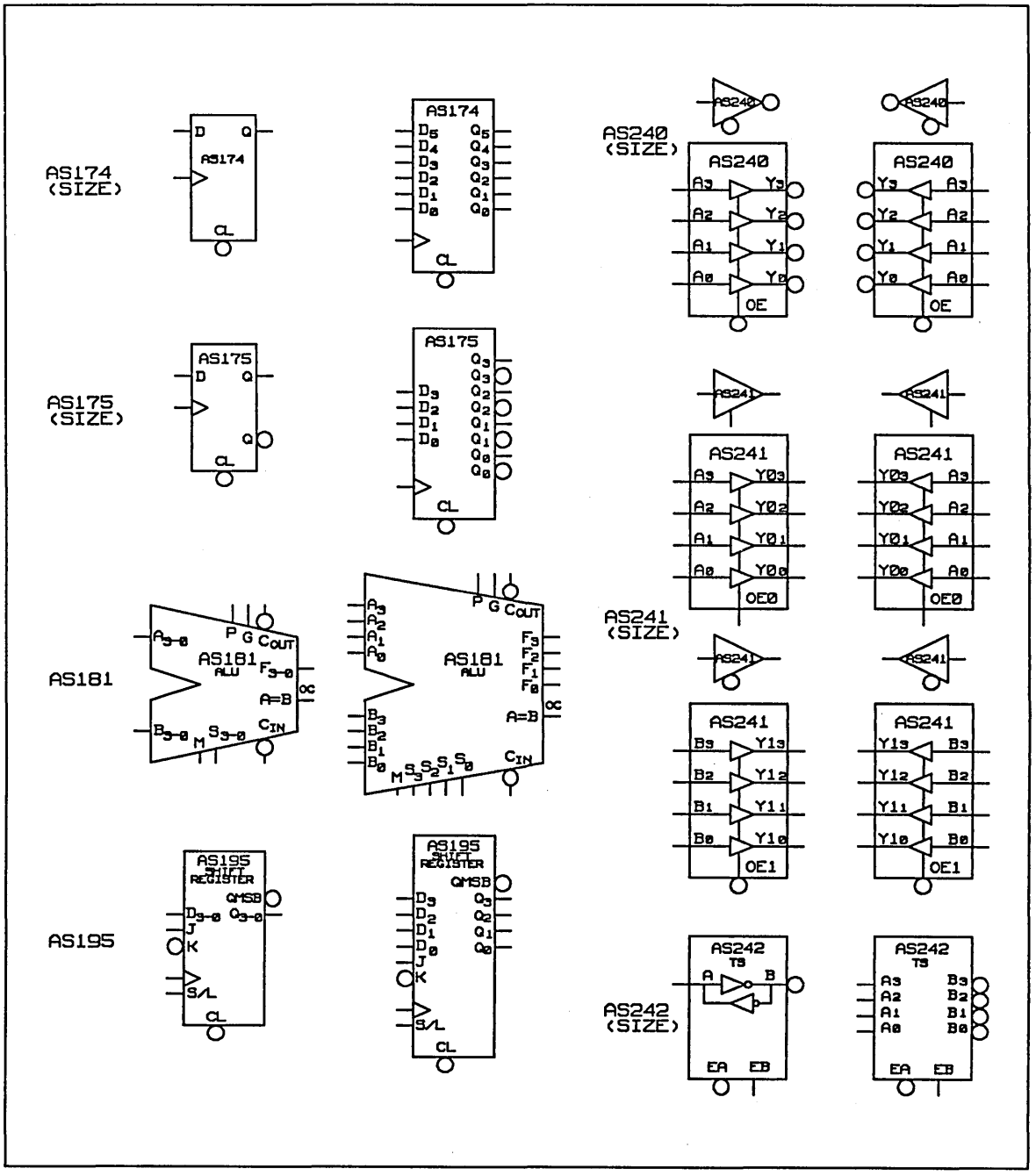
AS153	Dual 1 of 4 data selectors/multiplexer
AS157	Quad 1 of 2 data selector/multiplexer
AS158	Quad 1 of 2 data selector/multiplexer
AS161	4-bit synchronous binary counters with direct clear
AS163	Synchronous 4-bit binary counter
AS169	4-bit synchronous binary up/down counter
AS174	Hex D-type flip-flops with clear
AS175	Quad D-type flip-flops with clear
AS181	Arithmetic logic unit/function generator
AS195	4-bit bidirectional shift registers
AS240	Octal buffer and line driver with 3-state output
AS241	Octal buffer and line driver with 3-state output
AS242	Quad inverted 3-state bus transceiver
AS243	Quad noninverted 3-state bus transceiver
AS244	Octal buffer and line driver with 3-state output
AS245	Octal noninverted 3-state bus transceiver
AS251	1 of 8 3-state data selectors/multiplexer
AS253	Dual 1 of 4 data selector/multiplexer with 3-state output
AS257	Quad 1 of 2 data selector/multiplexer with 3-state output
AS258	Quad 1 of 2 data selector/multiplexer with 3-state output
AS280	9-bit parity generator/checker
AS286	9-bit parity generator/checker with bus driver parity I/O port
AS298	Quad 2-input multiplexer with storage
AS299	8-input 3-state universal shift/storage register
AS323	8-input 3-state universal shift/storage register

AS353	Dual 1 of 4 data selector/multiplexer with 3-state output
AS373	Octal D-type 3-state transparent latch
AS374	Octal D-type edge-triggered flip-flop
AS533	Octal D-type 3-state transparent latch
AS534	Octal D-type edge-triggered flip-flop with 3-state output
AS573	Octal D-type 3-state transparent latch
AS574	Octal D-type edge-triggered flip-flop with 3-state output
AS575	Octal D-type flip-flops with 3-state outputs
AS576	Octal D-type flip-flops with 3-state outputs
AS580	Octal D-type 3-state transparent latch
AS638	Octal bus transceivers
AS640	Octal bus transceivers
AS645	Octal bus transceivers
AS648	Octal bus transceivers and registers
AS652	Octal bus transceivers and registers
AS804A	Hex 2-input NAND drivers
AS805A	Hex 2-input NOR drivers
AS808A	Hex 2-input AND drivers
AS821	10-bit bus interface flip-flops with 3-state outputs
AS823	9-bit bus interface flip-flops with 3-state outputs
AS832A	Hex 2-input OR drivers
AS843	9-bit bus interface D-type latches with 3-state outputs
AS857	Hex 2-to-1 universal multiplexer
AS866	8-bit magnitude comparator
AS867	Synchronous 8-bit up/down counter

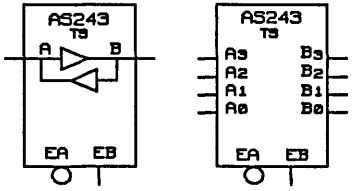
AS869	Synchronous 8-bit up/down counter
AS873	Dual 4-bit D-type latches with 3-state outputs
AS874	Dual 4-bit D-type edge-triggered flip-flops
AS877	8-bit universal transceiver port controllers
AS878	Dual 4-bit D-type edge-triggered flip-flops with 3-state outputs
AS882	32-bit look-ahead carry generator
AS1000	Quad 2-input NAND buffer
AS1004	Hex inverting drivers
AS1008	Quad 2-input positive-AND buffers/drivers
AS1034	Hex drivers


AS00 (SIZE)
AS02 (SIZE)
AS04 (SIZE)
AS08 (SIZE)
AS10 (SIZE)
AS11 (SIZE)
AS20 (SIZE)
AS21 (SIZE)
AS27 (SIZE)
AS30 (SIZE)
AS32 (SIZE)
AS74 (SIZE)
AS109 (SIZE)
AS112 (SIZE)
AS113 (SIZE)
AS114 (SIZE)
AS137
D PR Q
AS74
CL Q
J PR Q
AS109
K CL Q
AS112
AS113
AS114
AS137 DEMUX
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
S2-0
EN EN EN
1 2

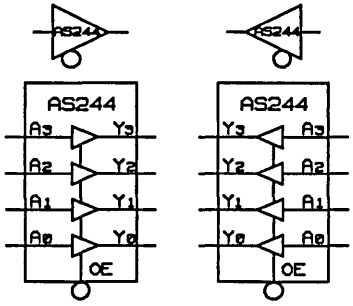

AS138
AS139
AS151 (SIZE)
AS153 (SIZE)
AS157 (SIZE)
AS158 (SIZE)
AS161
AS163
AS169
DEMUX
MUX
BINARY CTR
RIPPLE CARRY
LD
CL
UP/DN


AS174
(SIZE)
AS175
(SIZE)
AS181
AS195
AS240
(SIZE)
AS241
(SIZE)
AS242
(SIZE)
AS174
AS175
AS181
ALU
AS195
SHIFT REGISTER
AS240
AS241
AS242
TS
OE
OE0
OE1
EA
EB

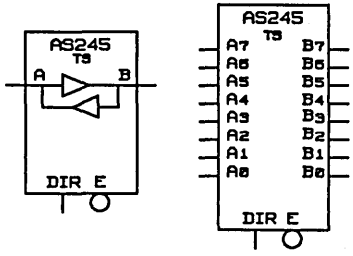
AS243 (SIZE)



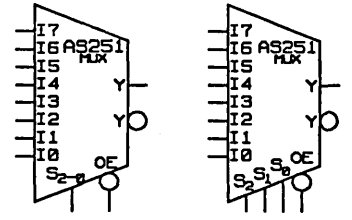
AS244 (SIZE)



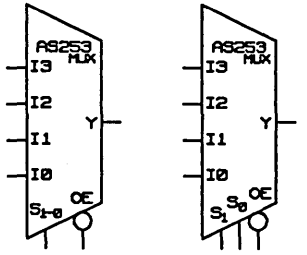
AS245 (SIZE)



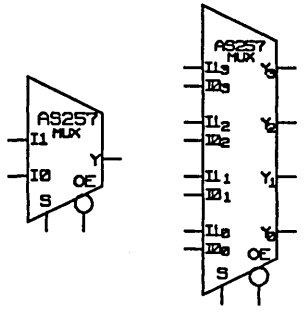
AS251 (SIZE)



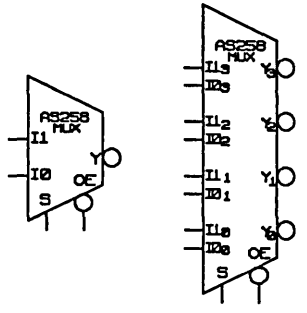
AS253 (SIZE)



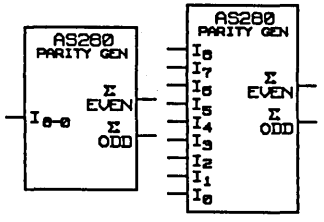
AS257 (SIZE)



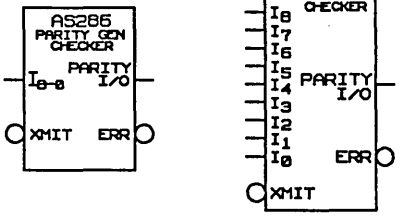
AS258 (SIZE)



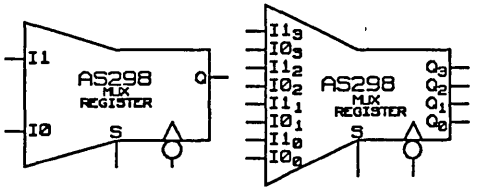
AS280



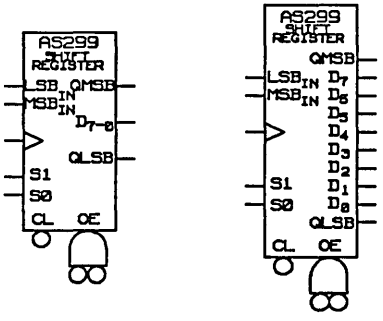
AS286



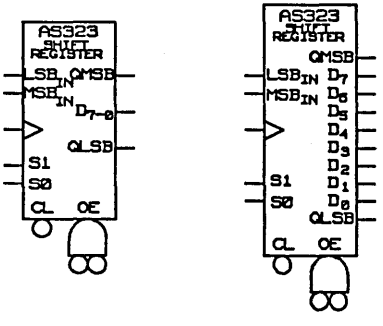
AS298 (SIZE)



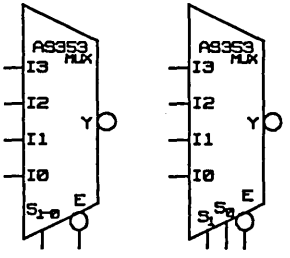
AS299



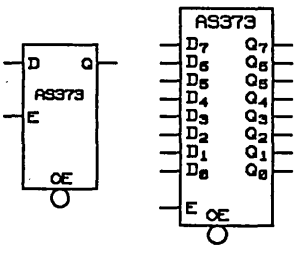
AS323



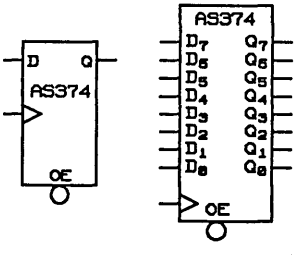
AS353 (SIZE)



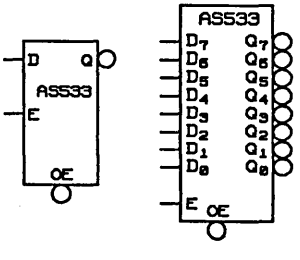
AS373 (SIZE)

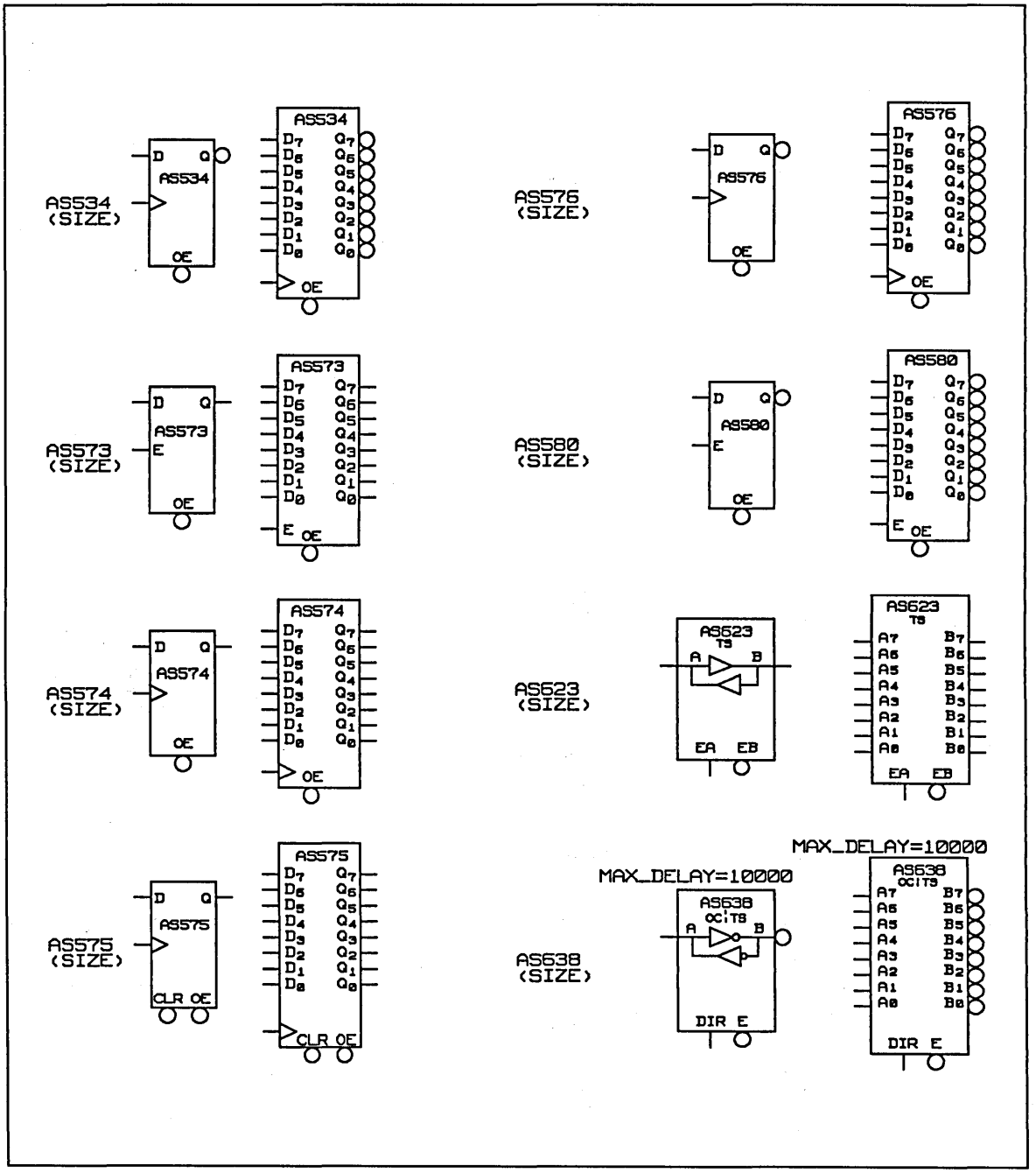


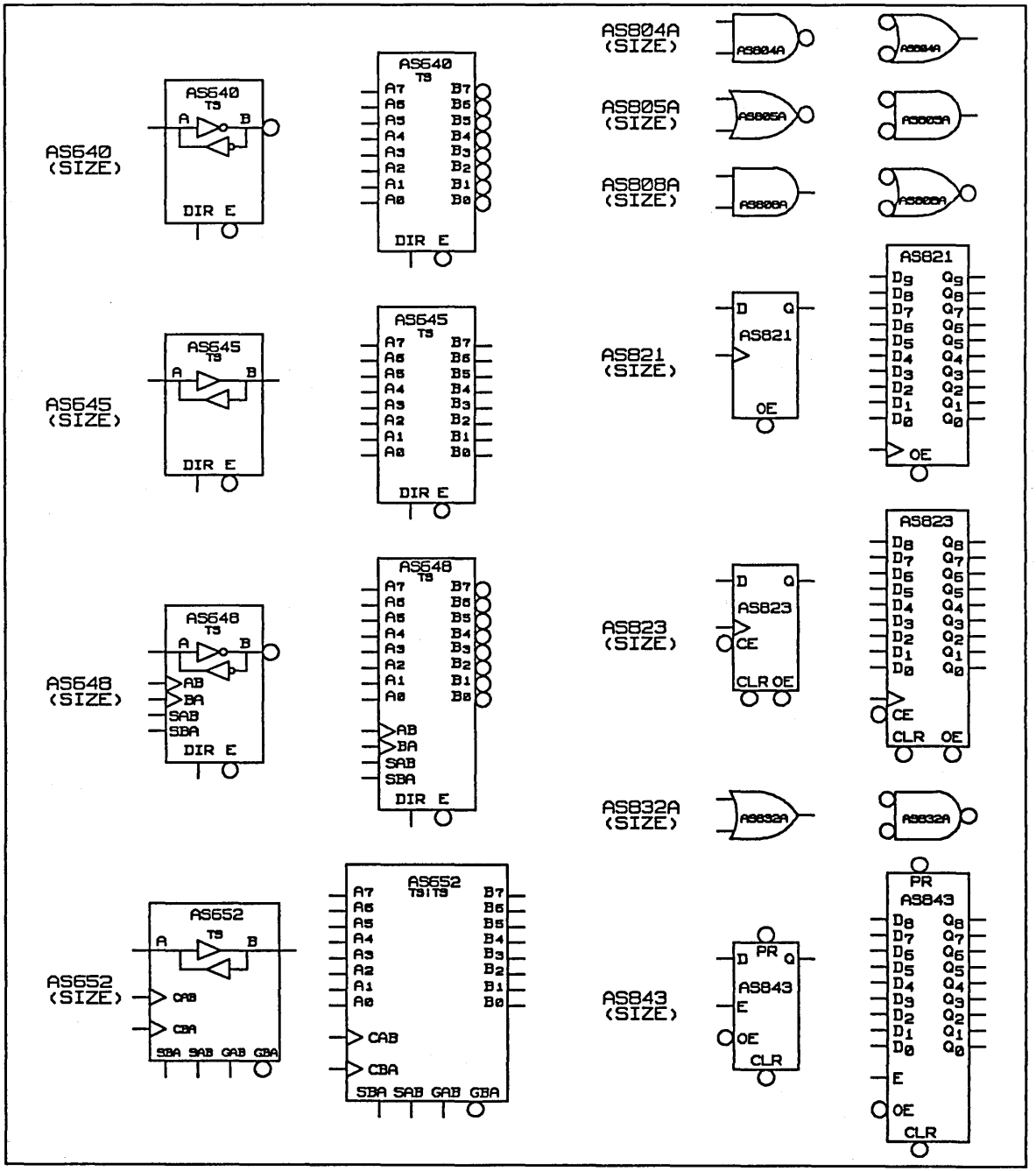
AS374 (SIZE)

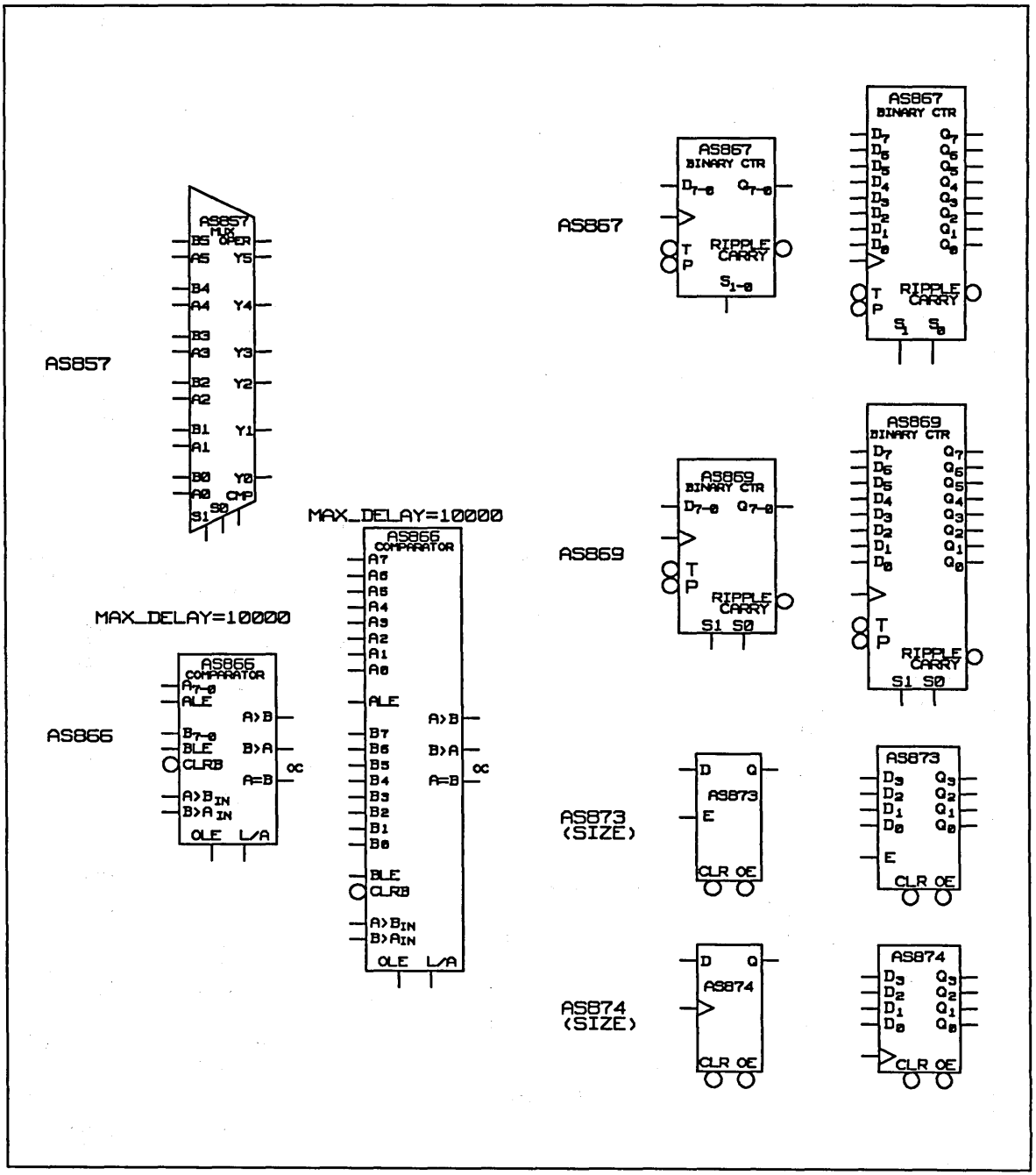


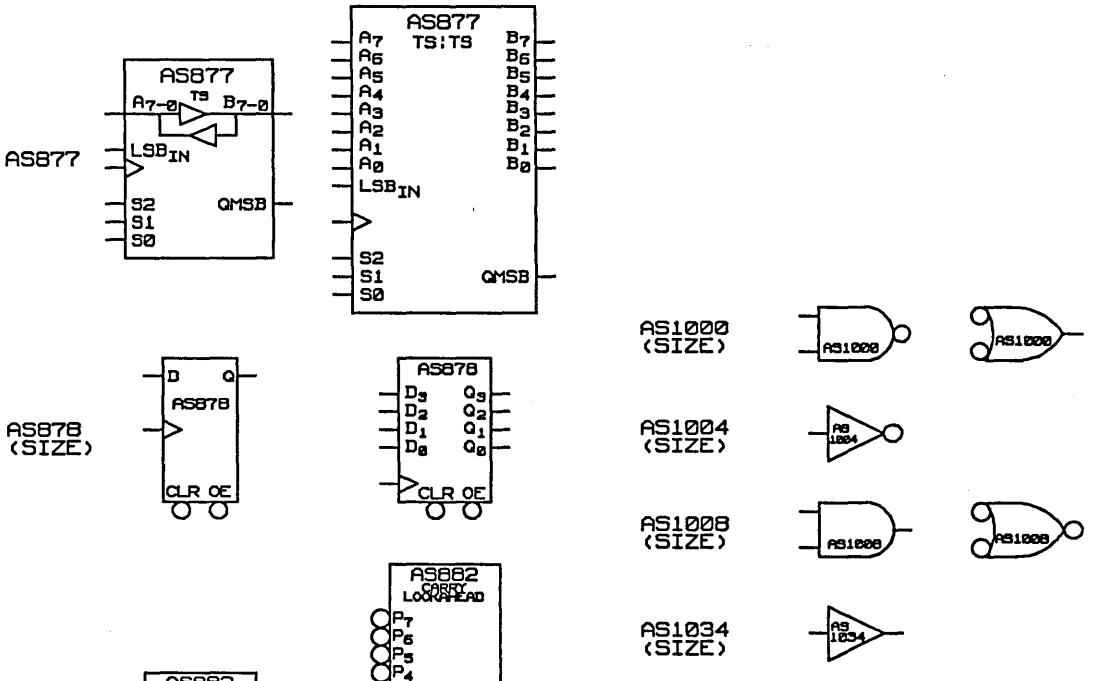
AS533 (SIZE)

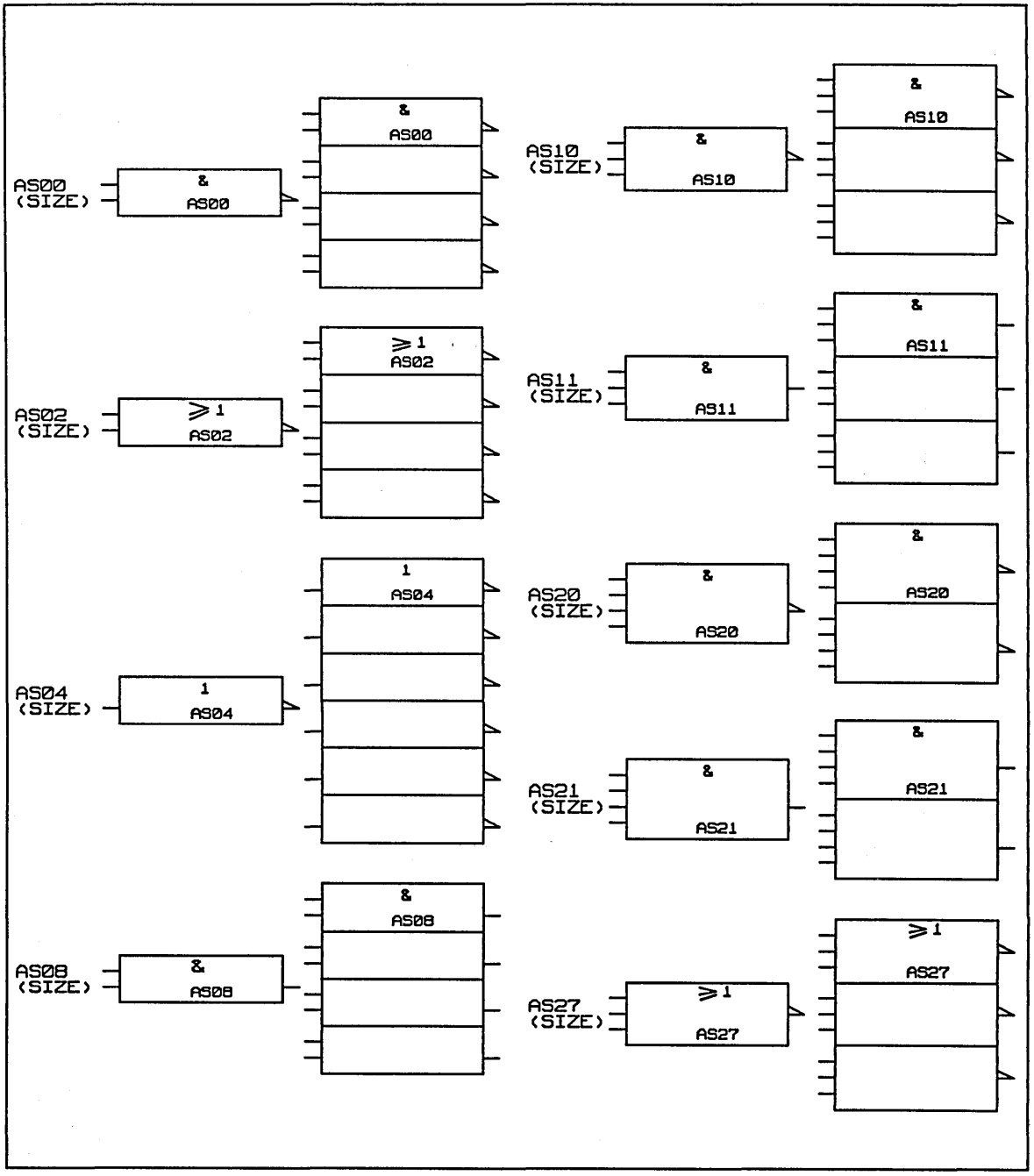


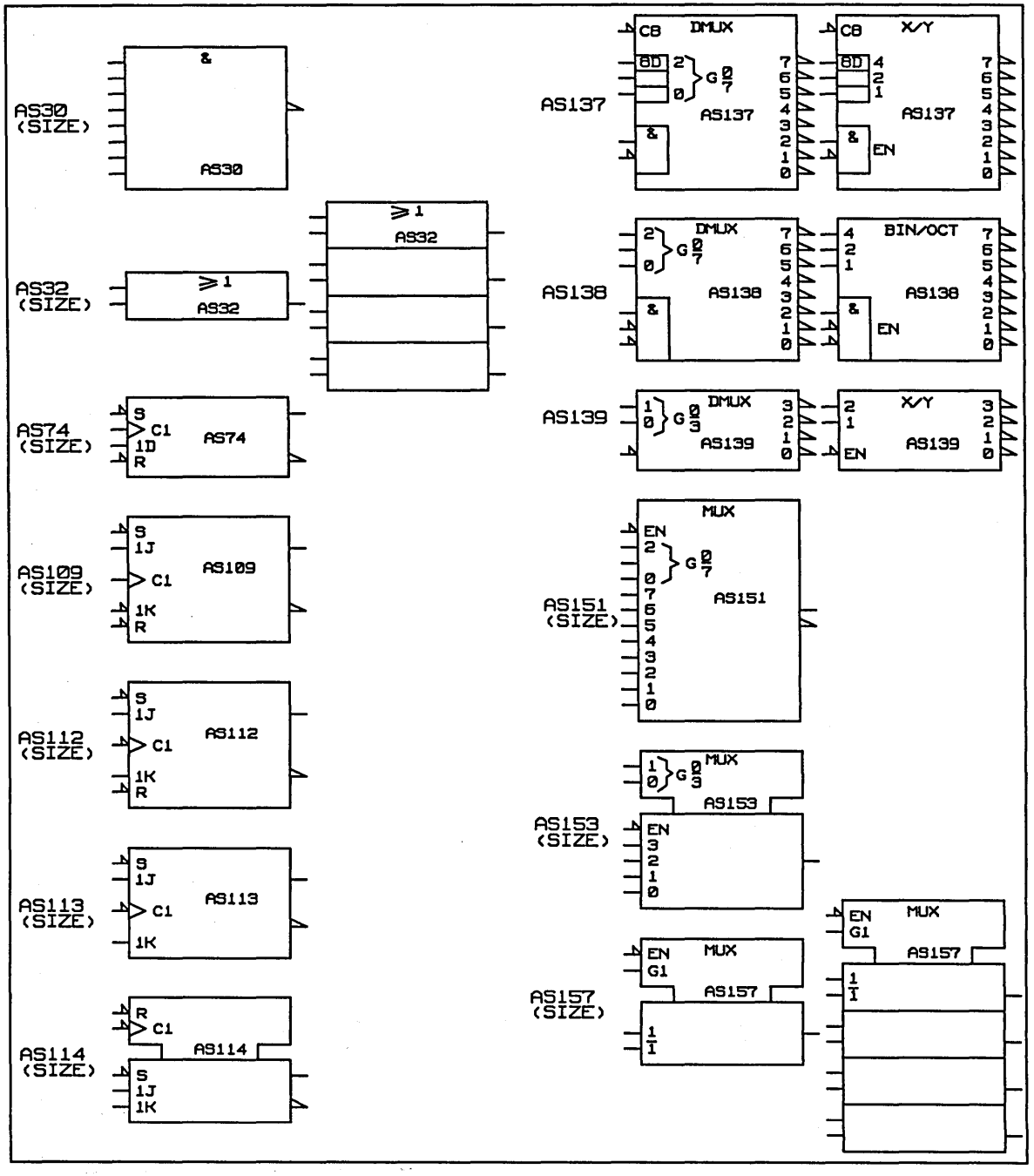

AS534
(SIZE)
D
Q
AS534
OE
AS534
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
OE
AS576
(SIZE)
D
Q
AS576
OE
AS576
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
OE
AS573
(SIZE)
D
Q
AS573
E
OE
AS573
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OE
AS580
(SIZE)
D
Q
AS580
E
OE
AS580
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OE
AS574
(SIZE)
D
Q
AS574
OE
AS574
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
OE
AS623
(SIZE)
AS623
T3
A
B
EA
EB
AS623
T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
EA
EB
AS575
(SIZE)
D
Q
AS575
CLR
OE
AS575
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CLR
OE
AS638
(SIZE)
MAX_DELAY=10000
AS638
OC:T8
A
B
DIR
E
MAX_DELAY=10000
AS638
OC:T8
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
DIR
E

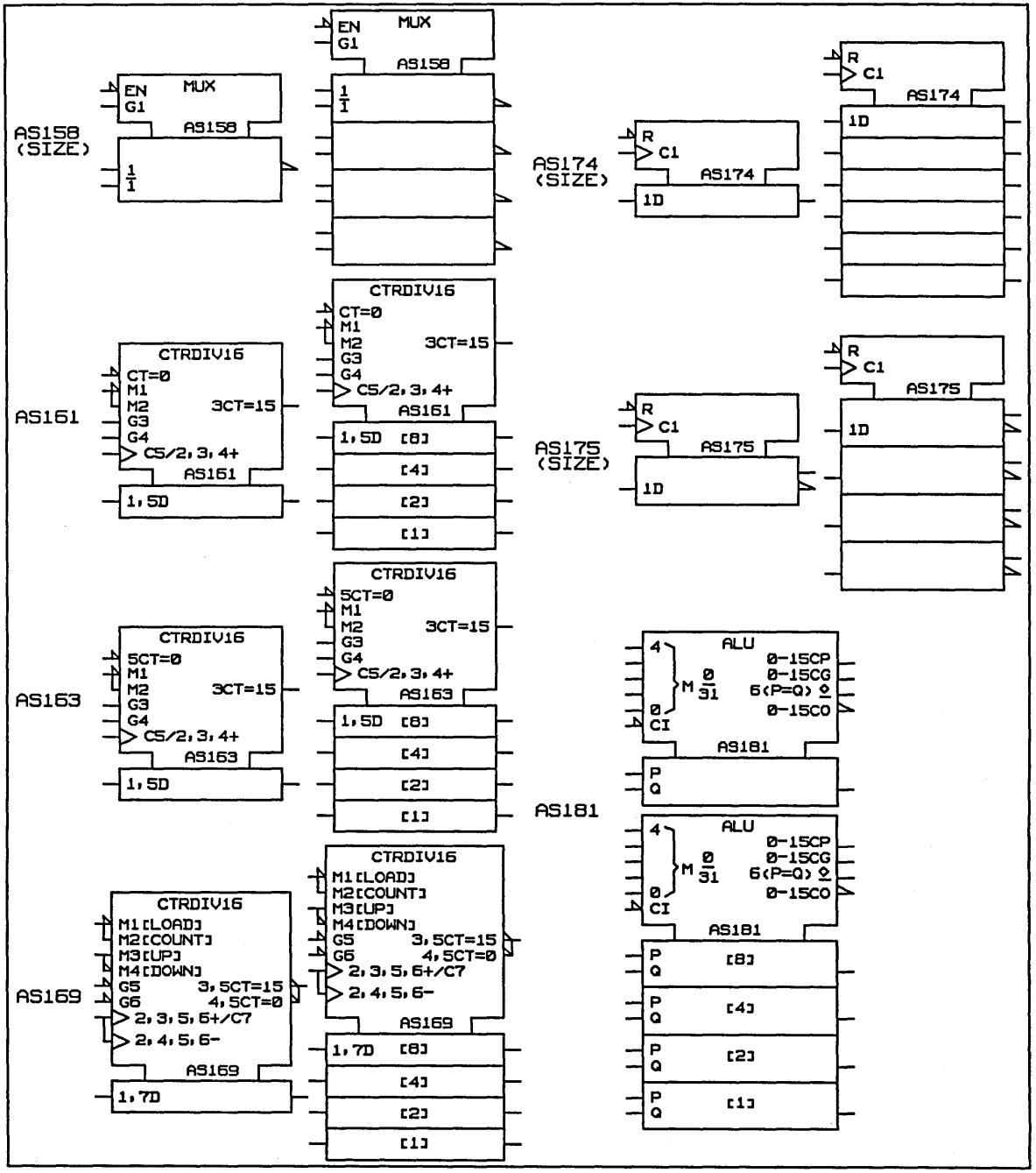

AS640 (SIZE)
AS640
TS
A
B
DIR E
AS640
TS
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
DIR E
AS645 (SIZE)
AS645
TS
A
B
DIR E
AS645
TS
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
DIR E
AS648 (SIZE)
AS648
TS
A
B
AB
BA
SAB
SBA
DIR E
AS648
TS
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
AB
BA
SAB
SBA
DIR E
AS652 (SIZE)
AS652
TS
A
B
CAB
CBA
SBA SAB GAB GBA
AS652
TS1TS
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
CAB
CBA
SBA SAB GAB GBA
AS804A (SIZE)
AS804A
AS804A
AS805A (SIZE)
AS805A
AS805A
AS808A (SIZE)
AS808A
AS808A
AS821 (SIZE)
D Q
AS821
OE
AS821
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
OE
AS823 (SIZE)
D Q
AS823
CE
CLR OE
AS823
D8 D7 D6 D5 D4 D3 D2 D1 D0
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CE
CLR OE
AS832A (SIZE)
AS832A
AS832A
AS843 (SIZE)
PR
D Q
AS843
E
OE
CLR
PR
AS843
D8 D7 D6 D5 D4 D3 D2 D1 D0
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E
OE
CLR

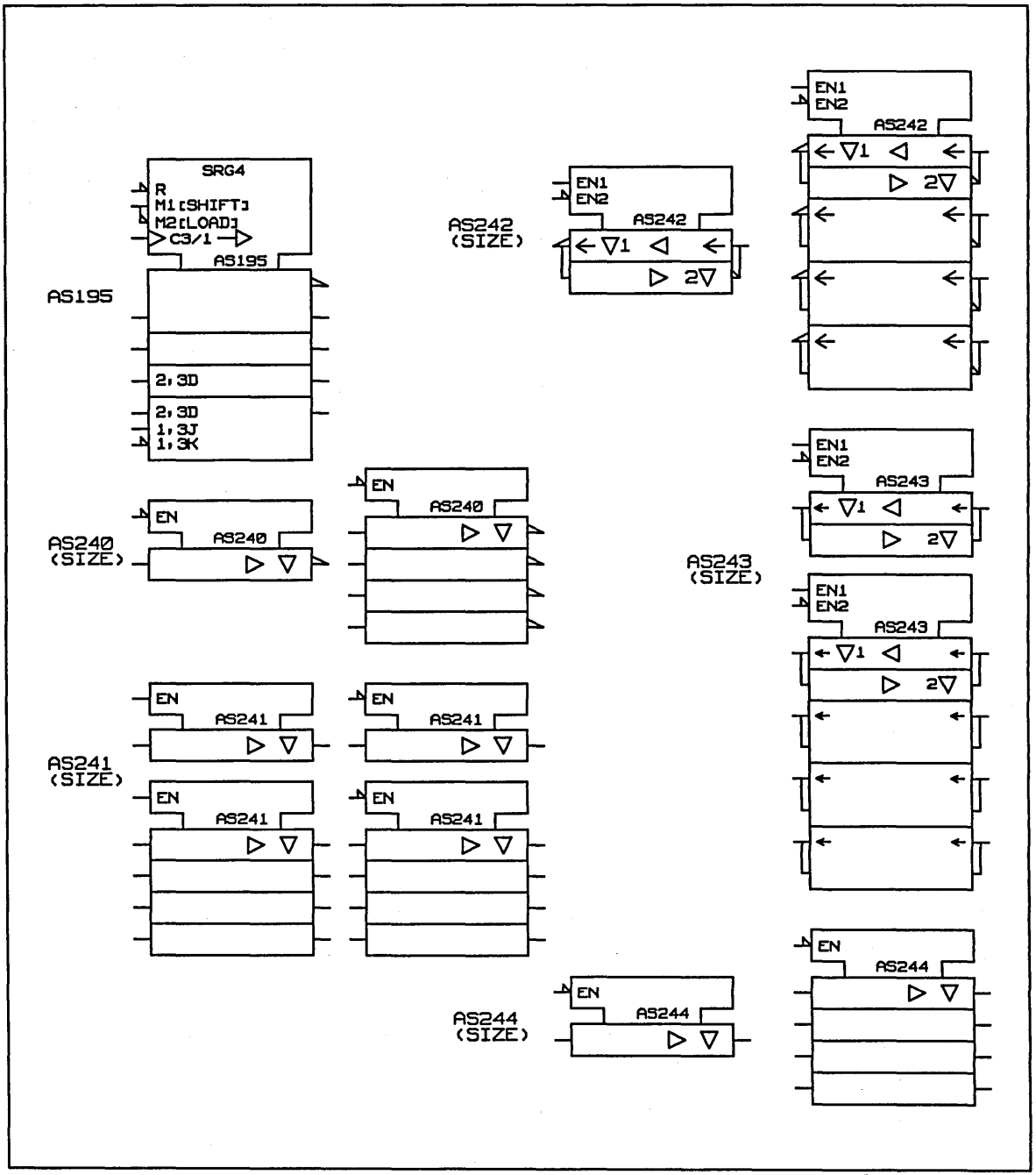

AS857
AS857
MUX OPER
B5
A5
Y5
B4
A4
Y4
B3
A3
Y3
B2
A2
Y2
B1
A1
Y1
B0
A0
Y0
CMP
S1
S0
MAX_DELAY=10000
AS866
COMPARATOR
A7-0
ALE
A>B
B7-0
BLE
B>A
CLRB
A=B
OC
A>BIN
B>AIN
OLE
L/A
MAX_DELAY=10000
AS866
COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
ALE
A>B
B7
B6
B5
B4
B3
B2
B1
B0
B>A
A=B
OC
BLE
CLRB
A>BIN
B>AIN
OLE
L/A
AS867
AS867
BINARY CTR
D7-0
Q7-0
T
P
RIPPLE CARRY
S1-0
AS867
BINARY CTR
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
T
P
RIPPLE CARRY
S1
S0
AS869
AS869
BINARY CTR
D7-0
Q7-0
T
P
RIPPLE CARRY
S1 S0
AS869
BINARY CTR
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
T
P
RIPPLE CARRY
S1 S0
AS873
(SIZE)
D
Q
AS873
E
CLR OE
AS873
D3
D2
D1
D0
Q3
Q2
Q1
Q0
E
CLR OE
AS874
(SIZE)
D
Q
AS874
CLR OE
AS874
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CLR OE

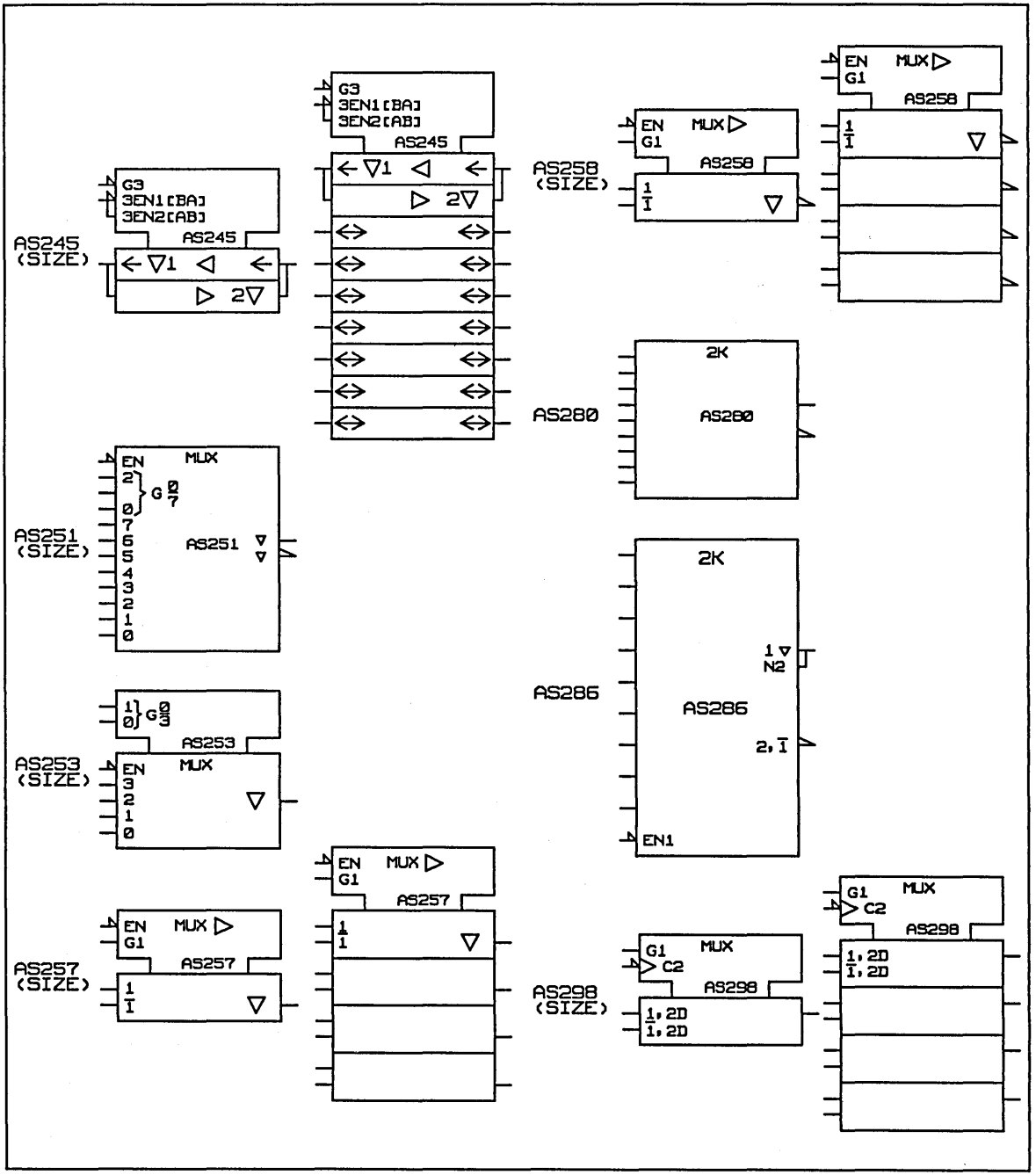

AS877
AS877
A7-0
TS
B7-0
LSBIN
S2
S1
S0
QMSB
AS877
TS:TS
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
LSBIN
S2
S1
S0
QMSB
AS878
(SIZE)
D
Q
AS878
CLR OE
AS878
D3
D2
D1
D0
Q3
Q2
Q1
Q0
CLR OE
AS882
CARRY LOOKAHEAD
P7-0
CN+Z
CN+Y
CN+X
G7-0
CN+W
CN
AS882
CARRY LOOKAHEAD
P7
P6
P5
P4
P3
P2
P1
P0
G7
G6
G5
G4
G3
G2
G1
G0
CN+Z
CN+Y
CN+X
CN+W
CN
AS1000
(SIZE)
AS1004
(SIZE)
AS1008
(SIZE)
AS1034
(SIZE)

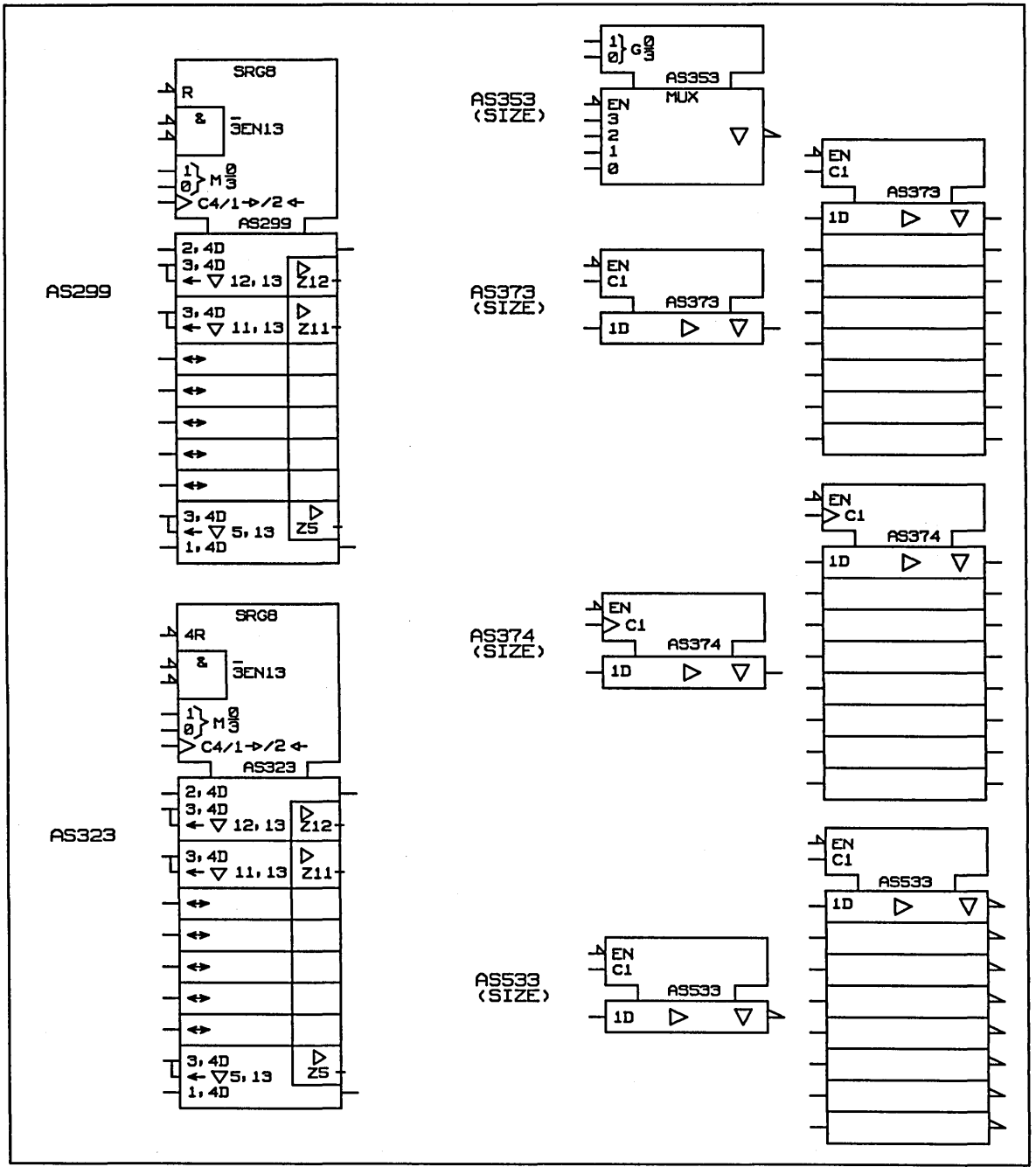

AS00
(SIZE)
&
AS00
&
AS00
AS02
(SIZE)
≥1
AS02
≥1
AS02
AS04
(SIZE)
1
AS04
1
AS04
AS08
(SIZE)
&
AS08
&
AS08
AS10
(SIZE)
&
AS10
&
AS10
AS11
(SIZE)
&
AS11
&
AS11
AS20
(SIZE)
&
AS20
&
AS20
AS21
(SIZE)
&
AS21
&
AS21
AS27
(SIZE)
≥1
AS27
≥1
AS27

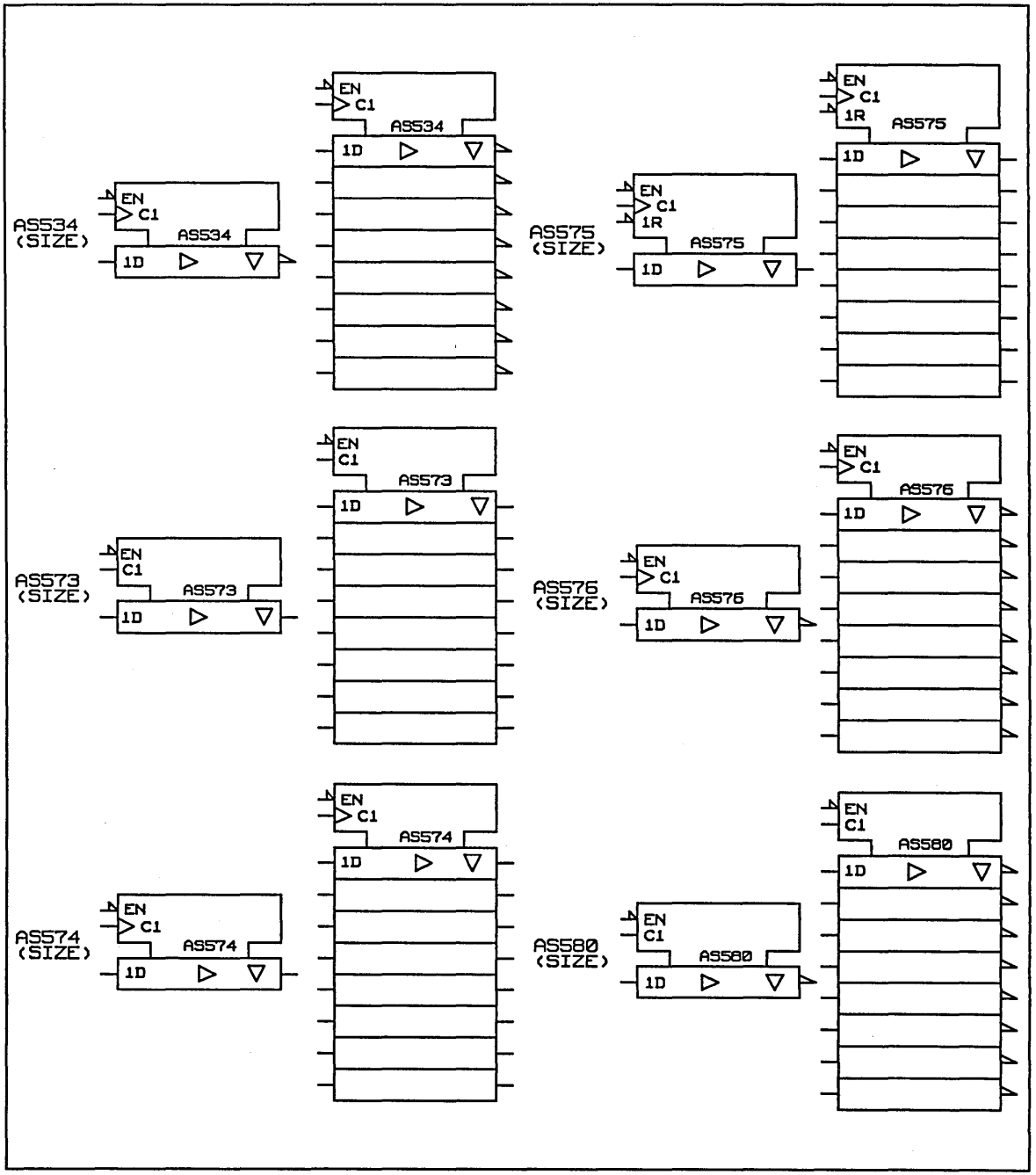

AS30
(SIZE)
&
AS30
AS32
(SIZE)
≥1
AS32
AS74
(SIZE)
S
C1
1D
R
AS74
AS109
(SIZE)
S
1J
C1
1K
R
AS109
AS112
(SIZE)
S
1J
C1
1K
R
AS112
AS113
(SIZE)
S
1J
C1
1K
AS113
AS114
(SIZE)
R
C1
AS114
S
1J
1K
AS137
CB
DMUX
BD
G
AS137
&
X/Y
EN
AS138
DMUX
BIN/OCT
AS138
AS139
DMUX
X/Y
AS139
AS151
(SIZE)
MUX
EN
G
AS151
AS153
(SIZE)
MUX
AS153
AS157
(SIZE)
MUX
EN
G1
AS157

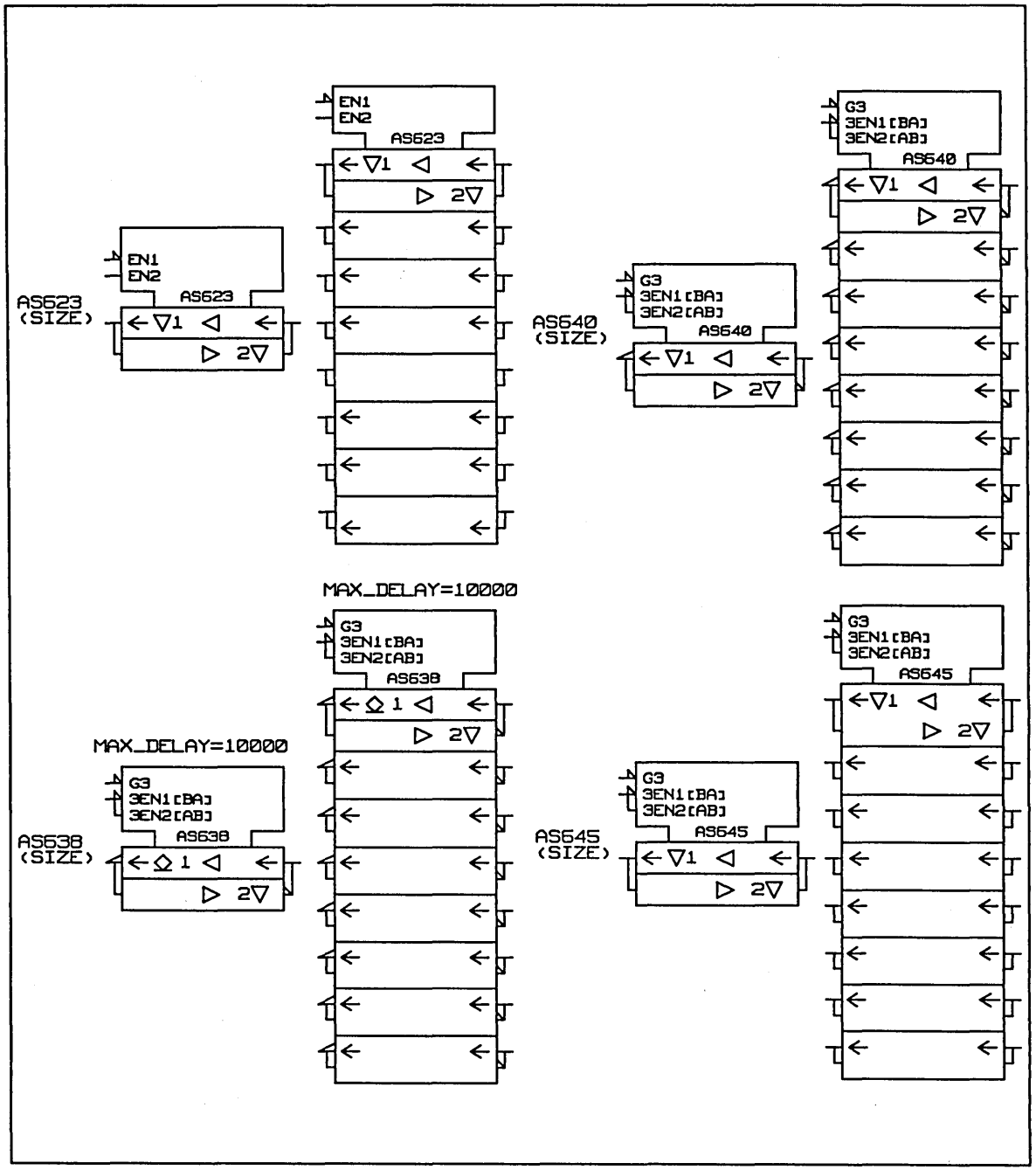

AS158 (SIZE)
EN
G1
MUX
AS158
1
1
AS174 (SIZE)
R
C1
AS174
1D
AS161
CT=0
M1
M2
G3
G4
CS/2, 3, 4+
3CT=15
AS161
1, 5D
[8]
[4]
[2]
[1]
AS175 (SIZE)
AS175
AS163
5CT=0
AS163
AS169
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5
3, 5CT=15
G6
4, 5CT=0
2, 3, 5, 6+/C7
2, 4, 5, 6-
AS169
1, 7D
AS181
ALU
M
0
31
CI
0-15CP
0-15CG
6(P=Q)
0-15C0
P
Q

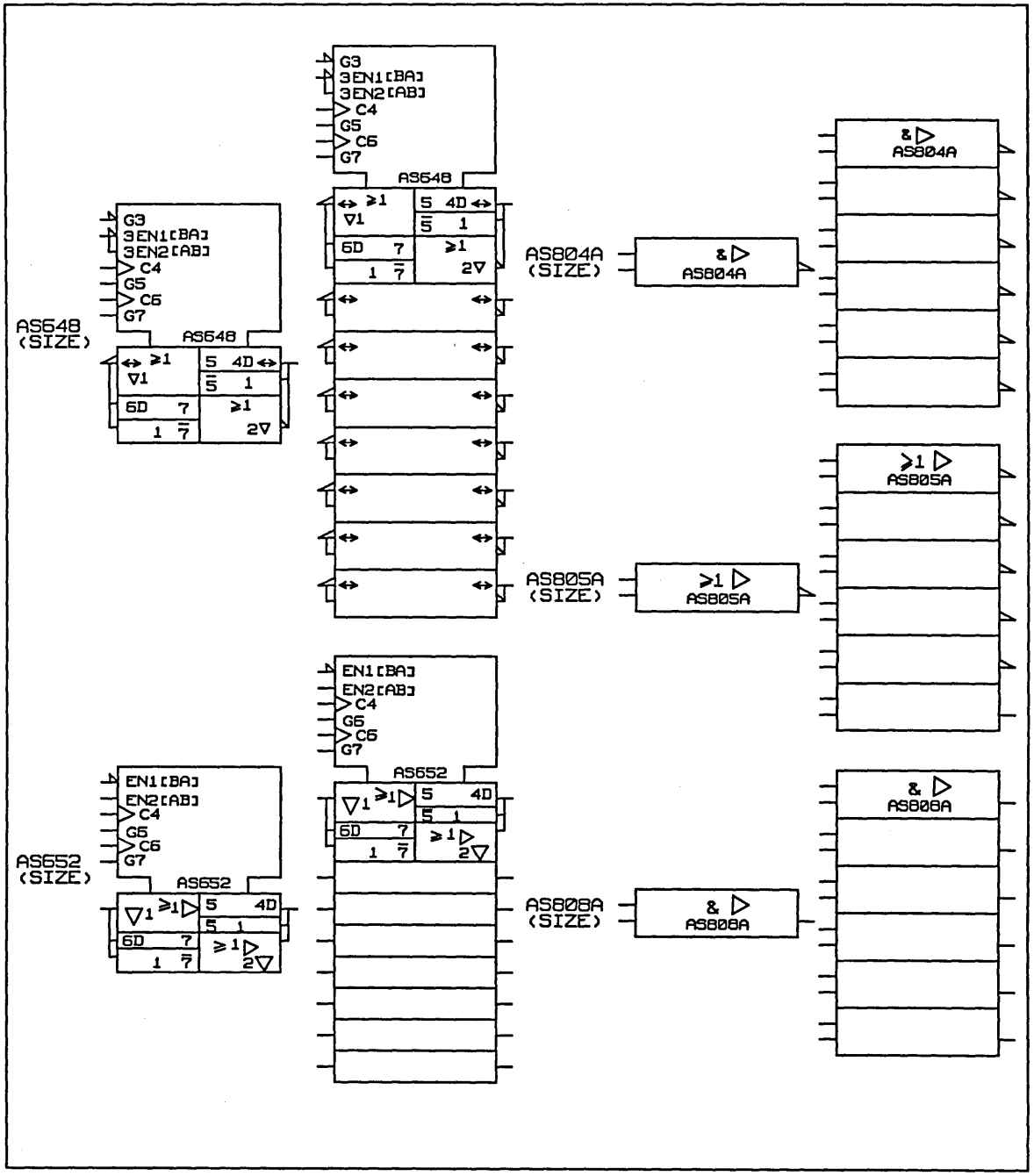

SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
AS195
AS195
2,3D
2,3D
1,3J
1,3K
EN
AS240
AS240
(SIZE)
EN
AS240
AS241
(SIZE)
EN
AS241
EN1
EN2
AS242
AS242
(SIZE)
EN1
EN2
AS242
1
2
EN1
EN2
AS243
AS243
(SIZE)
EN1
EN2
AS243
EN
AS244
AS244
(SIZE)
EN
AS244

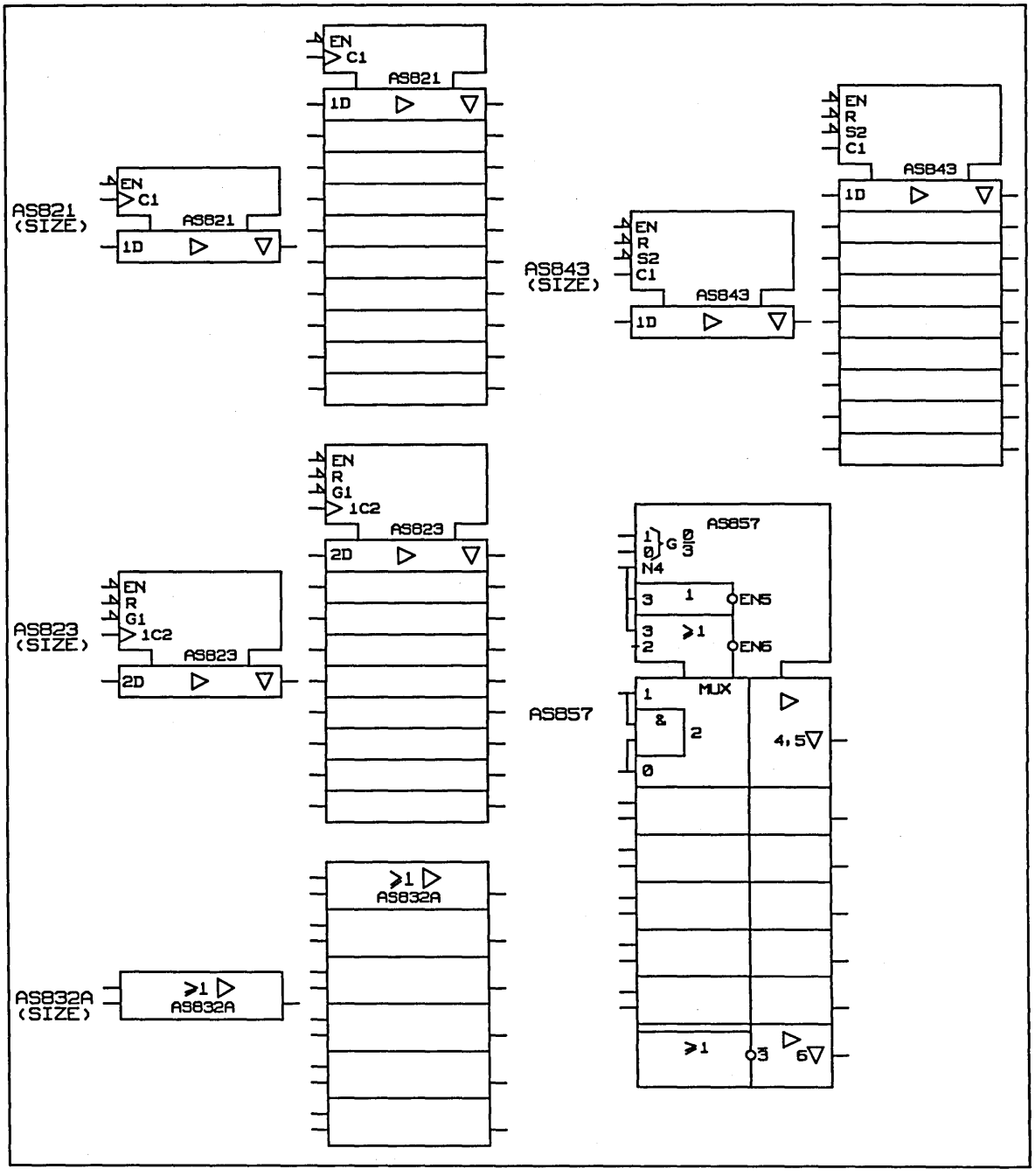

AS245
(SIZE)
G3
3EN1[BA]
3EN2[AB]
AS245
AS251
(SIZE)
EN
MUX
AS251
AS253
(SIZE)
AS253
AS257
(SIZE)
G1
AS257
AS258
(SIZE)
AS258
AS280
2K
AS280
AS286
AS286
EN1
AS298
(SIZE)
C2
AS298

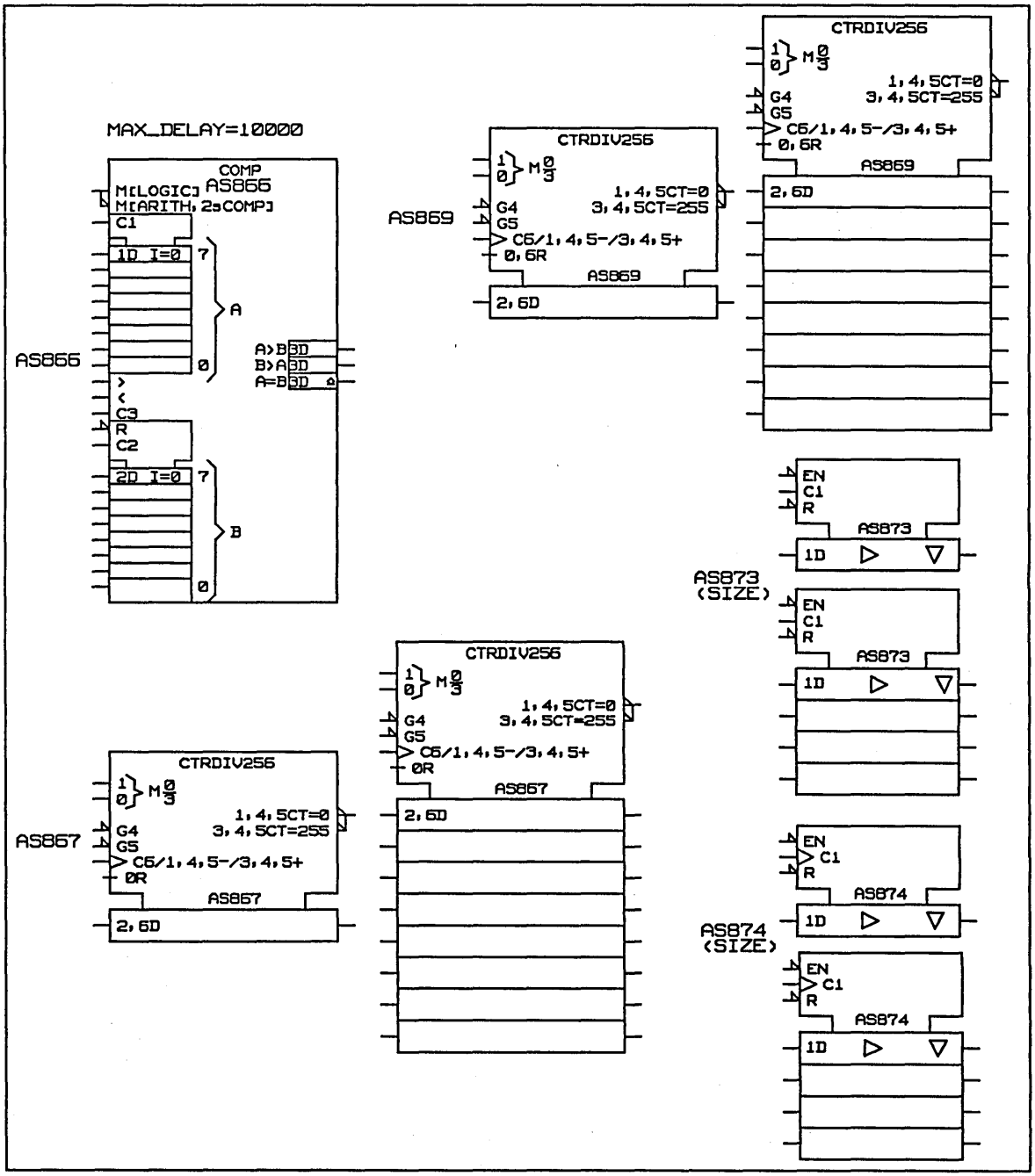

AS299
SRG8
R
&
3EN13
M
C4/1
/2
AS299
2,4D
3,4D
12,13
Z12
3,4D
11,13
Z11
3,4D
5,13
Z5
1,4D
AS323
SRG8
4R
&
3EN13
M
C4/1
/2
AS323
2,4D
3,4D
12,13
Z12
3,4D
11,13
Z11
3,4D
5,13
Z5
1,4D
AS353
(SIZE)
G
AS353
MUX
EN
3
2
1
0
AS373
(SIZE)
EN
C1
AS373
1D
AS374
(SIZE)
EN
C1
AS374
1D
AS533
(SIZE)
EN
C1
AS533
1D
EN
C1
AS373
1D
EN
C1
AS374
1D
EN
C1
AS533
1D

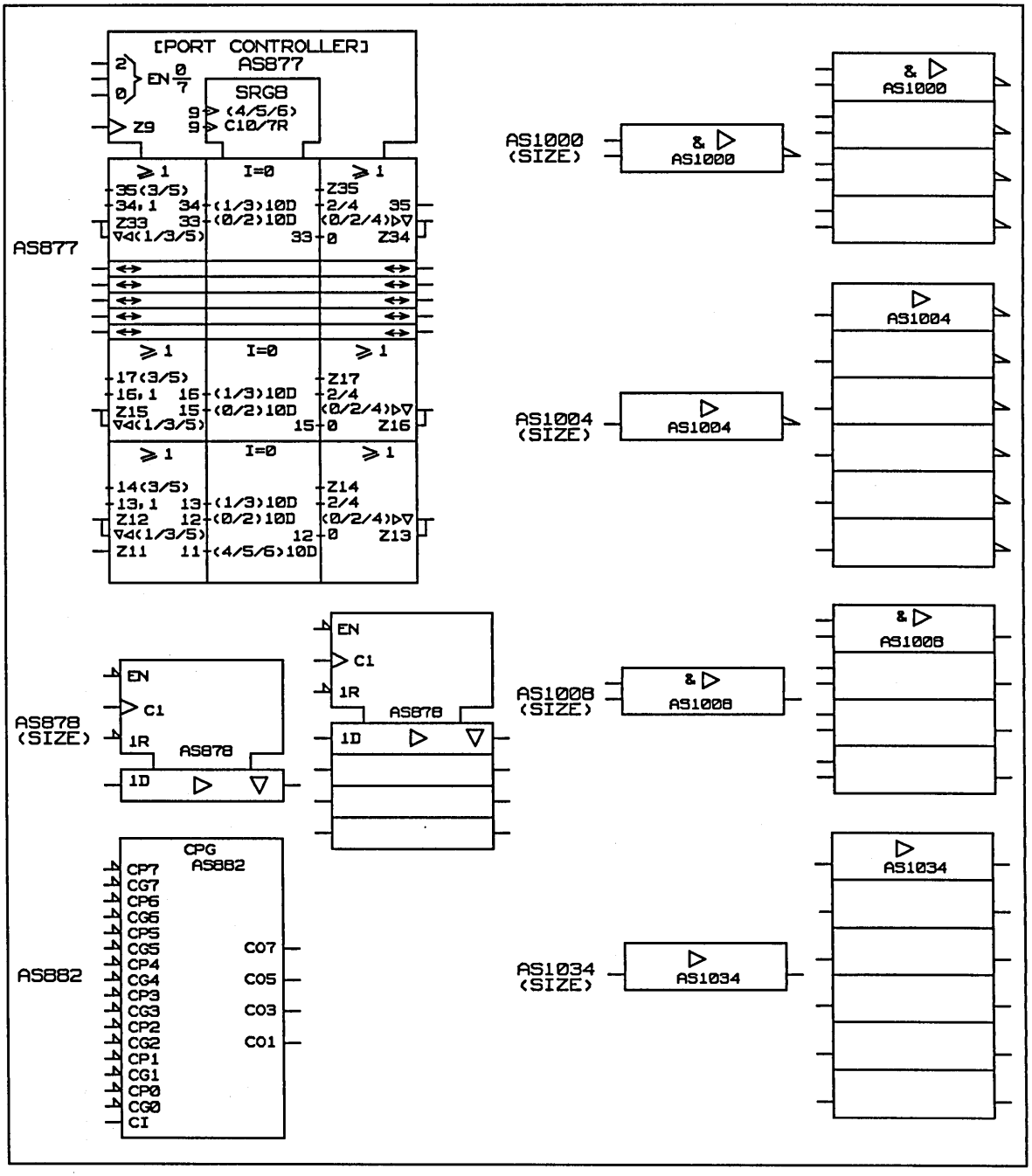

AS534
(SIZE)
EN
C1
1D
AS534
AS575
(SIZE)
EN
C1
1R
1D
AS575
AS573
(SIZE)
AS573
AS576
(SIZE)
AS576
AS574
(SIZE)
AS574
AS580
(SIZE)
AS580

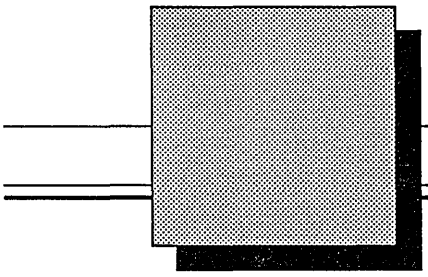

EN1
EN2
AS623
AS623
(SIZE)
AS640
(SIZE)
G3
3EN1[BA]
3EN2[AB]
AS640
MAX_DELAY=10000
AS638
(SIZE)
AS645
(SIZE)
AS638
AS645


G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
AS648
AS648
(SIZE)
AS804A
(SIZE)
AS804A
AS805A
(SIZE)
AS805A
EN1[BA]
EN2[AB]
C4
G5
C6
G7
AS652
AS652
(SIZE)
AS808A
(SIZE)
AS808A


AS821
(SIZE)
EN
C1
1D
AS821
AS843
(SIZE)
EN
R
S2
C1
1D
AS843
AS823
(SIZE)
EN
R
G1
1C2
2D
AS823
AS857
N4
G
MUX
EN5
EN6
4,5
AS832A
(SIZE)
≥1
AS832A


MAX_DELAY=10000
COMP
AS866
M[LOGIC]
M[ARITH,2,COMP]
C1
1D I=0
7
A
0
A>B 3D
B>A 3D
A=B 3D
>
<
C3
R
C2
2D I=0
7
B
0
AS866
CTRDIV256
1
0
M 0 3
1,4,5CT=0
3,4,5CT=255
G4
G5
C6/1,4,5-/3,4,5+
0,6R
AS869
2,6D
AS869
CTRDIV256
1
0
M 0 3
1,4,5CT=0
3,4,5CT=255
G4
G5
C6/1,4,5-/3,4,5+
0,6R
AS869
2,6D
CTRDIV256
1
0
M 0 3
1,4,5CT=0
3,4,5CT=255
G4
G5
C6/1,4,5-/3,4,5+
0R
AS867
2,6D
CTRDIV256
1
0
M 0 3
1,4,5CT=0
3,4,5CT=255
G4
G5
C6/1,4,5-/3,4,5+
0R
AS867
2,6D
AS867
EN
C1
R
AS873
1D
AS873
(SIZE)
EN
C1
R
AS873
1D
EN
C1
R
AS874
1D
AS874
(SIZE)
EN
C1
R
AS874
1D


[PORT CONTROLLER]
AS877
SRG8
AS877
AS878
(SIZE)
AS878
AS882
CPG
AS882
AS1000
(SIZE)
AS1000
AS1004
(SIZE)
AS1004
AS1008
(SIZE)
AS1008
AS1034
(SIZE)
AS1034



The ALSTTL and ANSI ALSTTL Libraries

The ALSTTL Library requires approximately 3431 Kbytes of disk storage, and the ANSI ALSTTL Library requires approximately 3488 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*alsttl.lib* or *a74alsttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books.

The release level of the ALSTTL and ANSI ALSTTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 110 components:

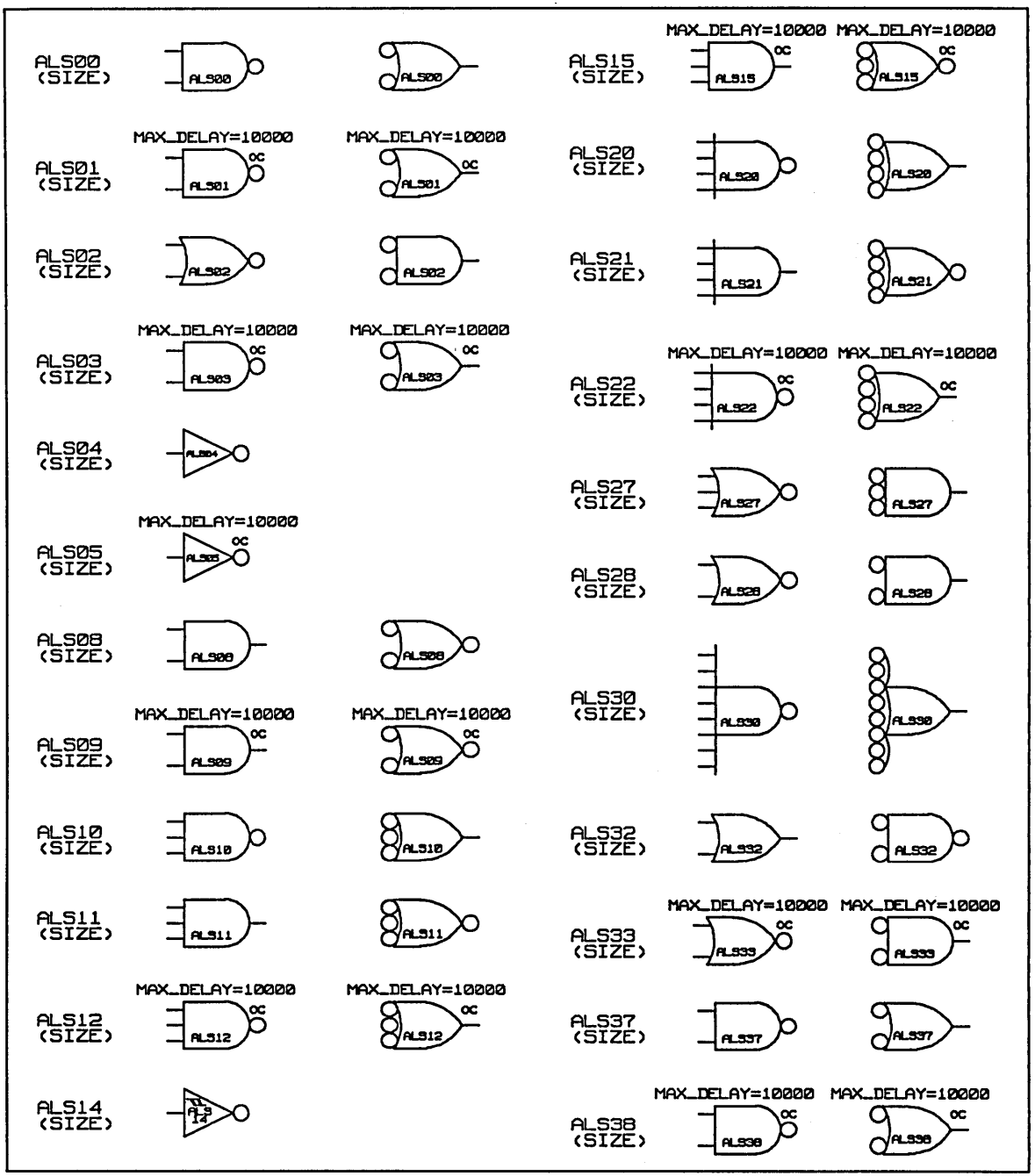
ALS00	Quad 2-input NAND
ALS01	Quad 2-input open-collector NAND
ALS02	Quad 2-input NOR
ALS03	Quad 2-input open-collector NAND
ALS04	Hex inverter
ALS05	Hex open-collector inverter
ALS08	Quad 2-input AND
ALS09	Quad 2-input open-collector AND
ALS10	Triple 3-input NAND
ALS11	Triple 3-input AND
ALS12	Triple 3-input open-collector NAND
ALS14	Hex Schmitt-trigger inverter
ALS15	Triple 3-input open-collector AND
ALS20	Dual 4-input NAND
ALS21	Dual 4-input AND
ALS22	Dual 4-input open-collector NAND
ALS27	Triple 3-input NOR
ALS28	Quad 2-input NOR buffer
ALS30	8-input NAND
ALS32	Quad 2-input OR
ALS33	Quad 2-input open-collector NOR buffer
ALS37	Quad 2-input NAND buffer
ALS38	Quad 2-input open-collector NAND buffer
ALS40	Dual 4-input NAND buffer
ALS74	Dual positive-edge-triggered D flip-flop

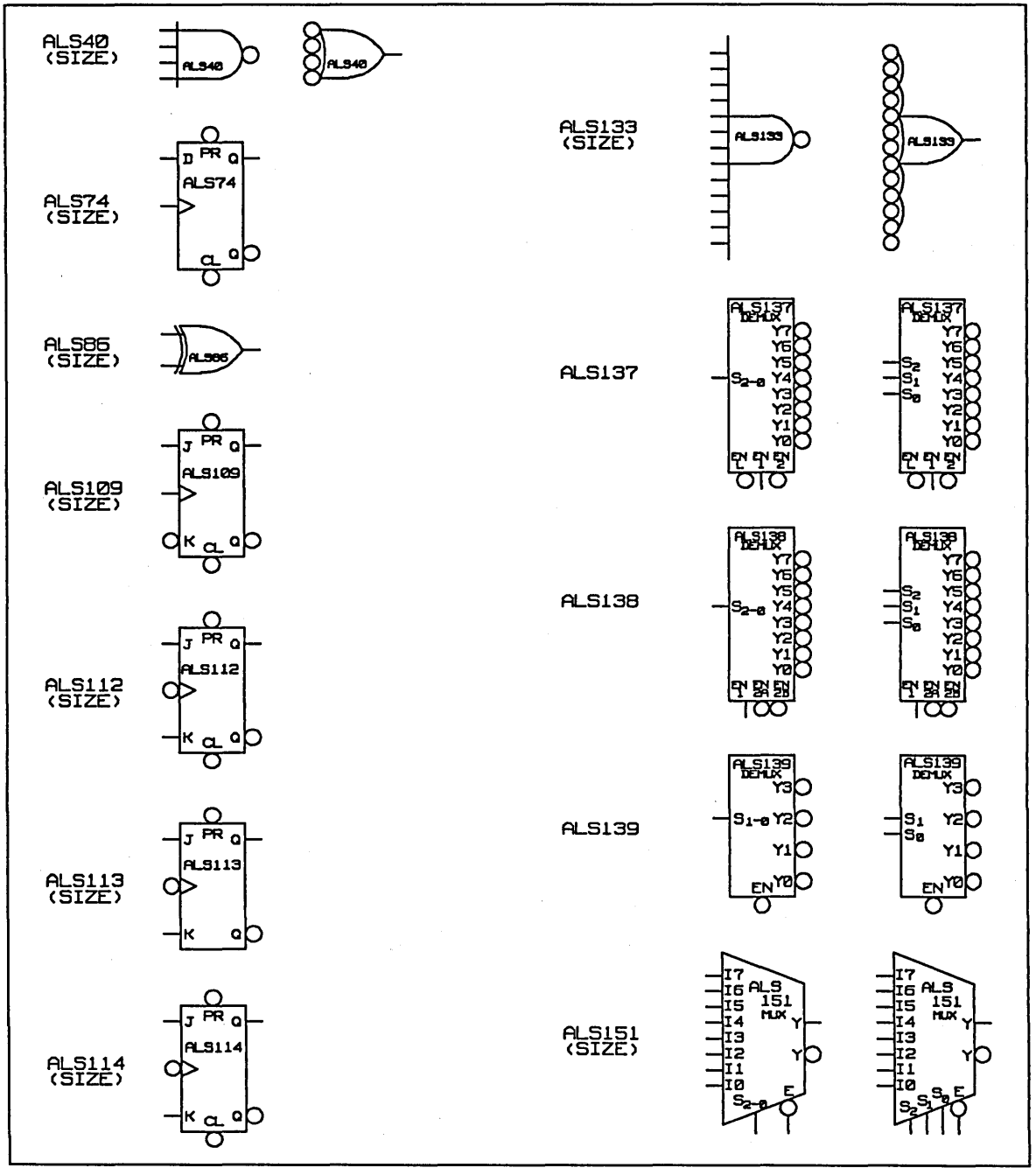
ALS86	Quad 2-input exclusive-OR
ALS109	Dual JKbar positive-edge-triggered flip-flop
ALS112	Dual JK negative-edge-triggered flip-flop with clear and preset
ALS113	Dual JK negative-edge-triggered flip-flop with preset
ALS114	Dual JK negative-edge-triggered flip-flop with preset, common clear, and clock
ALS133	13-input NAND
ALS137	3-to-8 line decoders/multiplexers with address latches
ALS138	3-to-8 line decoders/multiplexers
ALS139	Dual 2-to-4 line decoders/multiplexers
ALS151	1-of-8 data selectors/multiplexers
ALS153	Dual 1-of-4 data selector/multiplexer
ALS157	Quad 1-of-2 data selector/multiplexer
ALS158	Quad 1-of-2 inverted data selector/multiplexer
ALS160	4-bit synchronous decade counters with direct clear
ALS161	4-bit synchronous binary counters with direct clear
ALS162	4-bit synchronous decade counters with synch clear
ALS163	4-bit synchronous binary counters with synch clear
ALS164	8-bit parallel output serial shift register
ALS165	Parallel-load 8-bit shift register
ALS166	8-bit shift registers

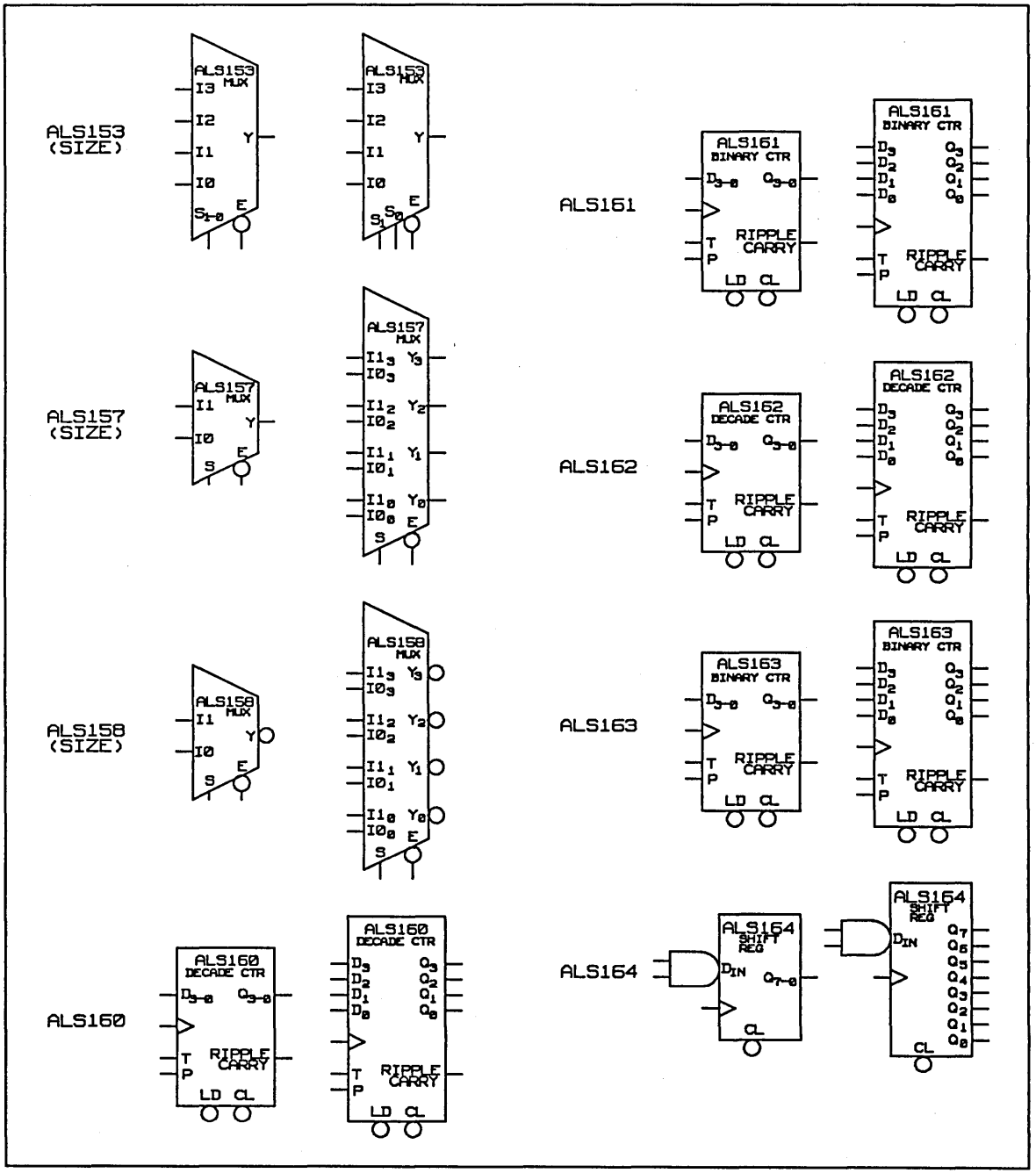
ALS168	4-bit synchronous decade up/down counters
ALS169	4-bit synchronous binary up/down counters
ALS174	Hex D-type flip-flops
ALS175	Quad D-type flip-flops
ALS190	Synchronous BCD up/down counter
ALS191	Synchronous binary up/down counter
ALS192	Synchronous BCD up/down dual clock counters
ALS193	Synchronous binary up/down dual clock counters
ALS240	Octal buffer and line driver with 3-state output
ALS241	Octal buffer and line driver with 3-state output
ALS242	Quad inverting 3-state bus transceiver
ALS243	Quad non-inverting 3-state bus transceiver
ALS244	Octal buffer and line driver with 3-state output
ALS245	Octal non-inverting 3-state bus transceiver
ALS251	3-state data multiplexer
ALS253	Dual data selectors/multiplexers
ALS257	Quad 3-state non-inverting data multiplexer
ALS258	Quad 3-state inverting data multiplexer
ALS273	Octal D-type flip-flop with clear
ALS299	8-bit universal shift/storage register with 3-state output
ALS323	8-bit universal shift/storage register with 3-state output
ALS353	Dual 1-of-4 data selectors/multiplexers
ALS365	Hex non-inverting 3-state bus transceiver with gated enables
ALS366	Hex inverting 3-state bus transceiver with gated enables
ALS367	Hex non-inverting 3-state bus driver

ALS368	Hex inverting 3-state bus driver
ALS373	Octal 3-state D-latch with common enable
ALS374	Octal D-type edge-triggered flip-flop
ALS520	8-bit identity comparator
ALS521	8-bit identity comparator
ALS533	Octal D-type transparent latches with 3-state output
ALS534	Octal D-type edge-triggered flip-flop with 3-state output
ALS538	3-line to 8-line decoder/demultiplexer with 3-state output
ALS540	Octal buffer and line driver with 3-state output
ALS541	Octal buffer and line driver with 3-state output
ALS563	Octal D-type transparent latch with 3-state output
ALS564	Octal D-type edge-triggered flip-flop with 3-state output
ALS569	Synchronous 4-bit up/down binary counter with 3-state output
ALS573	Octal D-type transparent latch with 3-state output
ALS574	Octal D-type edge-triggered flip-flop with 3-state output
ALS575	Octal D-type edge-triggered flip-flop with 3-state output
ALS576	Octal D-type edge-triggered flip-flop with 3-state output
ALS580	Octal D-type transparent latch with 3-state output
ALS623	Octal 3-state non-inverting bus transceiver
ALS640	Octal 3-state inverting bus transceiver

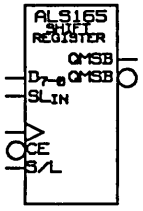
ALS645	Octal 3-state non-inverting bus transceiver
ALS648	Octal bus transceivers and registers
ALS651	Octal 3-state bus transceiver and register
ALS652	Octal 3-state non-inverting bus transceiver and register
ALS677	Address comparator
ALS688	8-bit identity comparator
ALS804	Hex 2-input NAND driver
ALS805	Hex 2-input NOR driver
ALS808	Hex 2-input AND driver
ALS857	Hex 2-to-1 universal multiplexer
ALS873	Dual 4-bit D-type 3-state latch
ALS874	Dual 4-bit D-type edge-triggered flip-flop
ALS878	Dual 4-bit D-type edge-triggered flip-flop with 3-state outputs
ALS990	8-bit D-type transparent read-back latches
ALS1000	Quad 2-input NAND buffer
ALS1002	Quad 2-input NOR buffer
ALS1004	Hex inverter
ALS1005	Hex 3-state inverter buffer
ALS1008	Quad 2-input positive-AND buffer/driver
ALS1034	Hex driver

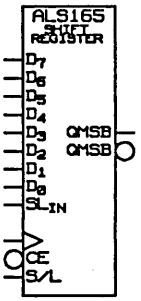

ALS00 (SIZE)
ALS01 (SIZE)
ALS02 (SIZE)
ALS03 (SIZE)
ALS04 (SIZE)
ALS05 (SIZE)
ALS08 (SIZE)
ALS09 (SIZE)
ALS10 (SIZE)
ALS11 (SIZE)
ALS12 (SIZE)
ALS14 (SIZE)
ALS15 (SIZE)
ALS20 (SIZE)
ALS21 (SIZE)
ALS22 (SIZE)
ALS27 (SIZE)
ALS28 (SIZE)
ALS30 (SIZE)
ALS32 (SIZE)
ALS33 (SIZE)
ALS37 (SIZE)
ALS38 (SIZE)
MAX_DELAY=10000
OC


ALS40
(SIZE)
ALS40
ALS40
ALS74
(SIZE)
D
PR
Q
ALS74
CL
Q
ALS86
(SIZE)
ALS86
ALS109
(SIZE)
J
PR
Q
ALS109
K
CL
Q
ALS112
(SIZE)
J
PR
Q
ALS112
K
CL
Q
ALS113
(SIZE)
J
PR
Q
ALS113
K
Q
ALS114
(SIZE)
J
PR
Q
ALS114
K
CL
Q
ALS133
(SIZE)
ALS133
ALS133
ALS137
ALS137
DEMUX
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
S2-0
S2
S1
S0
EN
C
EN
1
EN
2
ALS138
ALS138
DEMUX
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
S2-0
S2
S1
S0
EN
1
EN
2A
EN
2B
ALS139
ALS139
DEMUX
Y3
Y2
Y1
Y0
S1-0
S1
S0
EN
ALS151
(SIZE)
I7
I6
I5
I4
I3
I2
I1
I0
ALS
151
MUX
Y
E
S2-0
S2
S1
S0

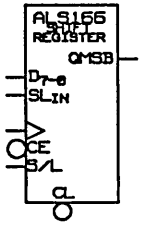

ALS153 (SIZE)
ALS153 MUX
I3
I2
I1
I0
Y
S1-0
S1
S0
E
ALS157 (SIZE)
ALS157 MUX
I1
I0
Y
S
E
I13
I03
I12
I02
I11
I01
I10
I00
Y3
Y2
Y1
Y0
ALS158 (SIZE)
ALS158 MUX
ALS160
ALS160 DECADE CTR
D3-0
Q3-0
T
P
RIPPLE CARRY
LD
CL
D3
D2
D1
D0
Q3
Q2
Q1
Q0
ALS161
ALS161 BINARY CTR
ALS162
ALS162 DECADE CTR
ALS163
ALS163 BINARY CTR
ALS164
ALS164 SHIFT REG
DIN
Q7-0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CL

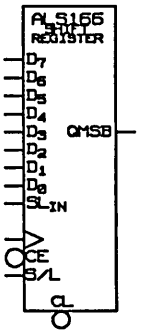
ALS165



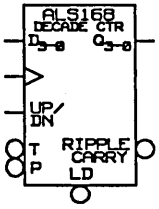


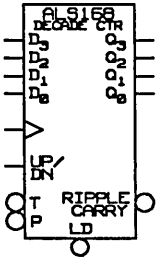
ALS166



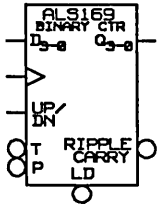


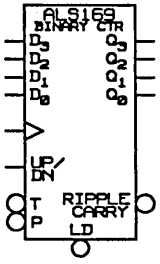
ALS168



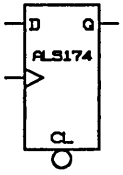


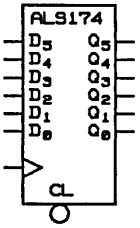
ALS169



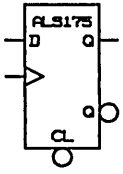


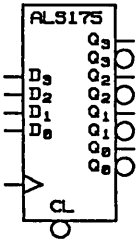
ALS174
(SIZE)



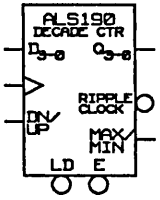


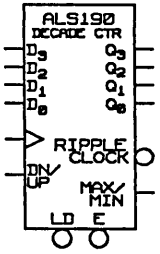
ALS175
(SIZE)



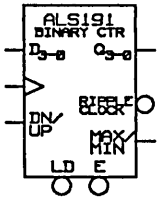


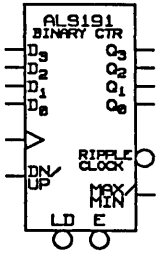
ALS190



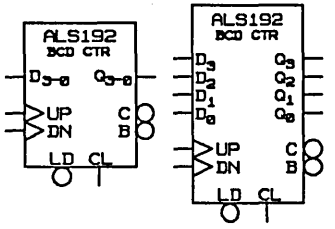


ALS191

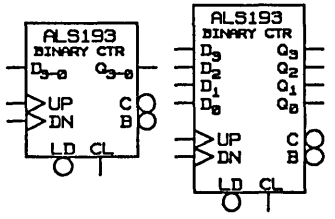




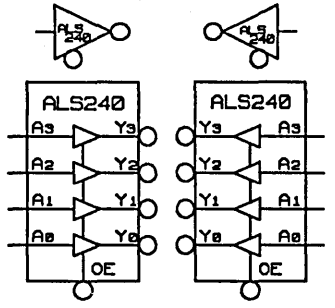
ALS192



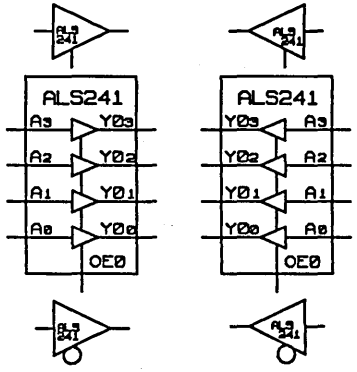
ALS193

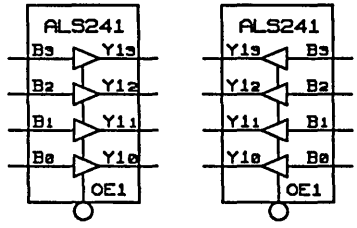


ALS240
(SIZE)

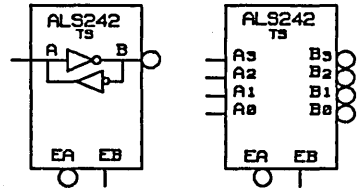


ALS241
(SIZE)

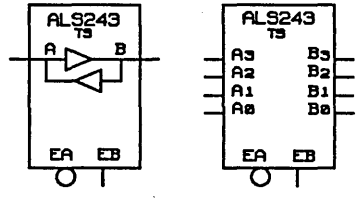




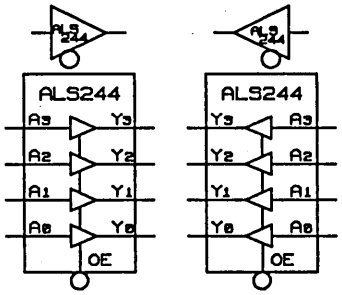
ALS242
(SIZE)



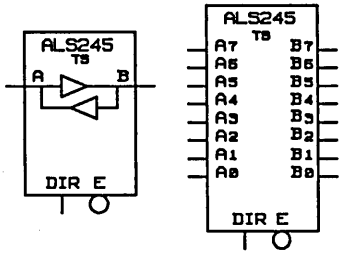
ALS243
(SIZE)



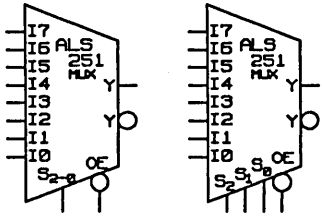
ALS244 (SIZE)



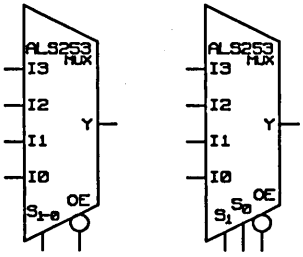
ALS245 (SIZE)



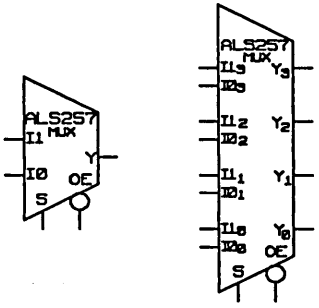
ALS251 (SIZE)



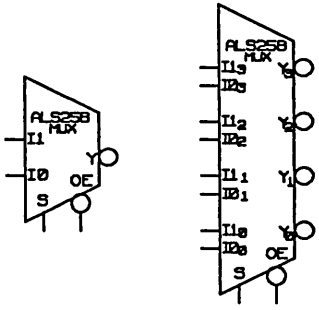
ALS253 (SIZE)



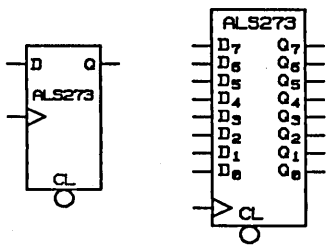
ALS257 (SIZE)



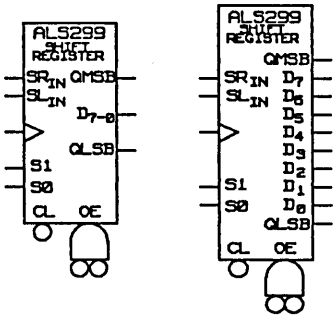
ALS258 (SIZE)



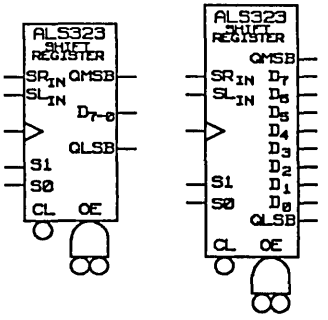
ALS273 (SIZE)



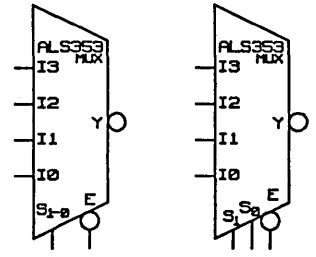
ALS299



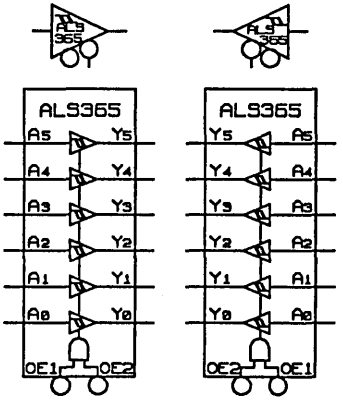
ALS323



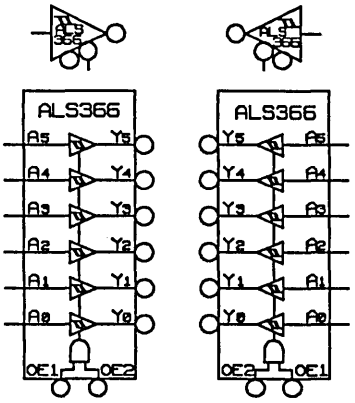
ALS353 (SIZE)



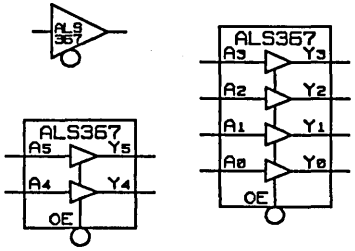
ALS365 (SIZE)



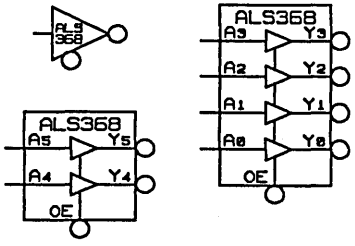
ALS366 (SIZE)



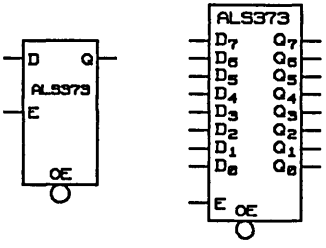
ALS367 (SIZE)

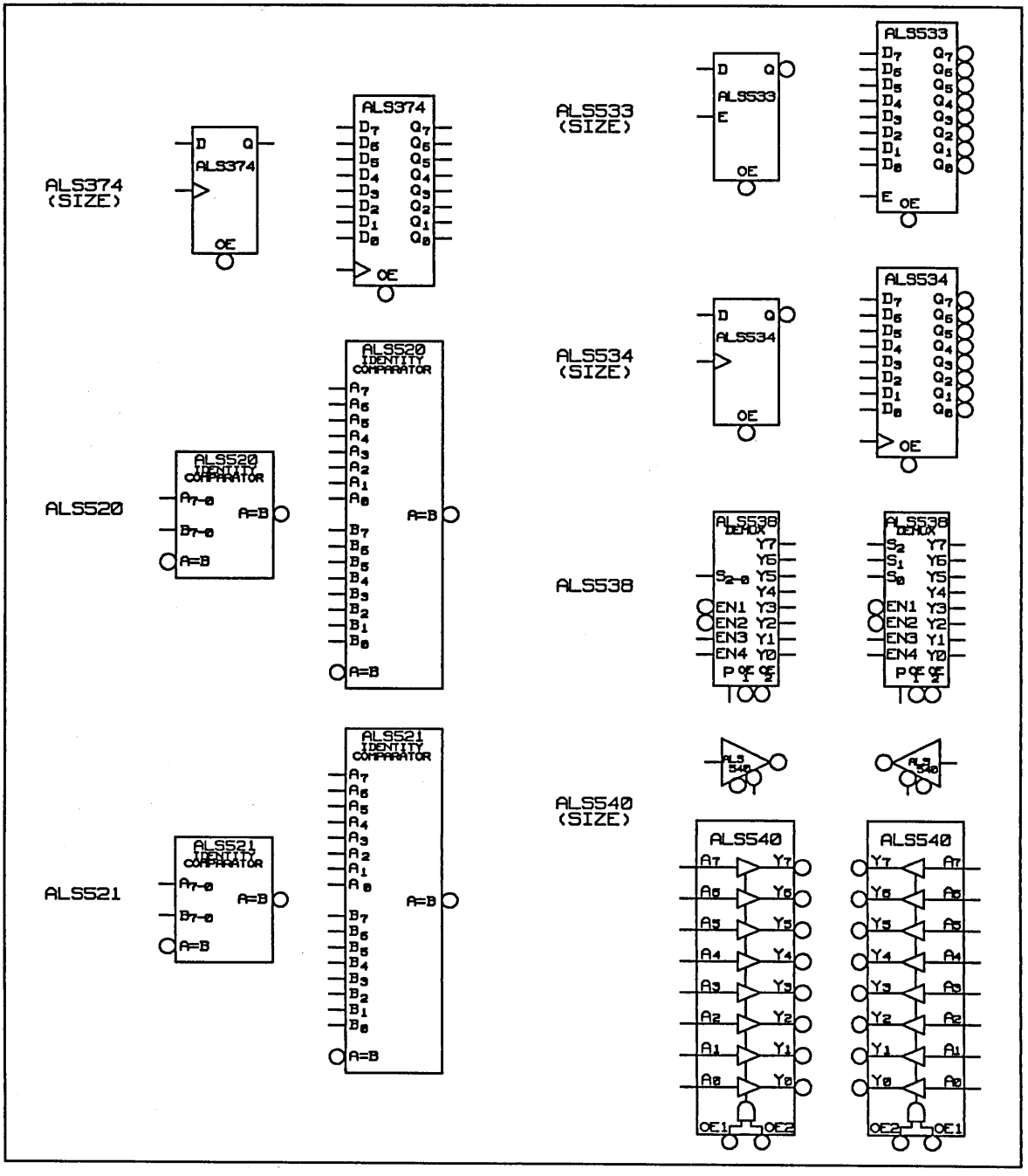


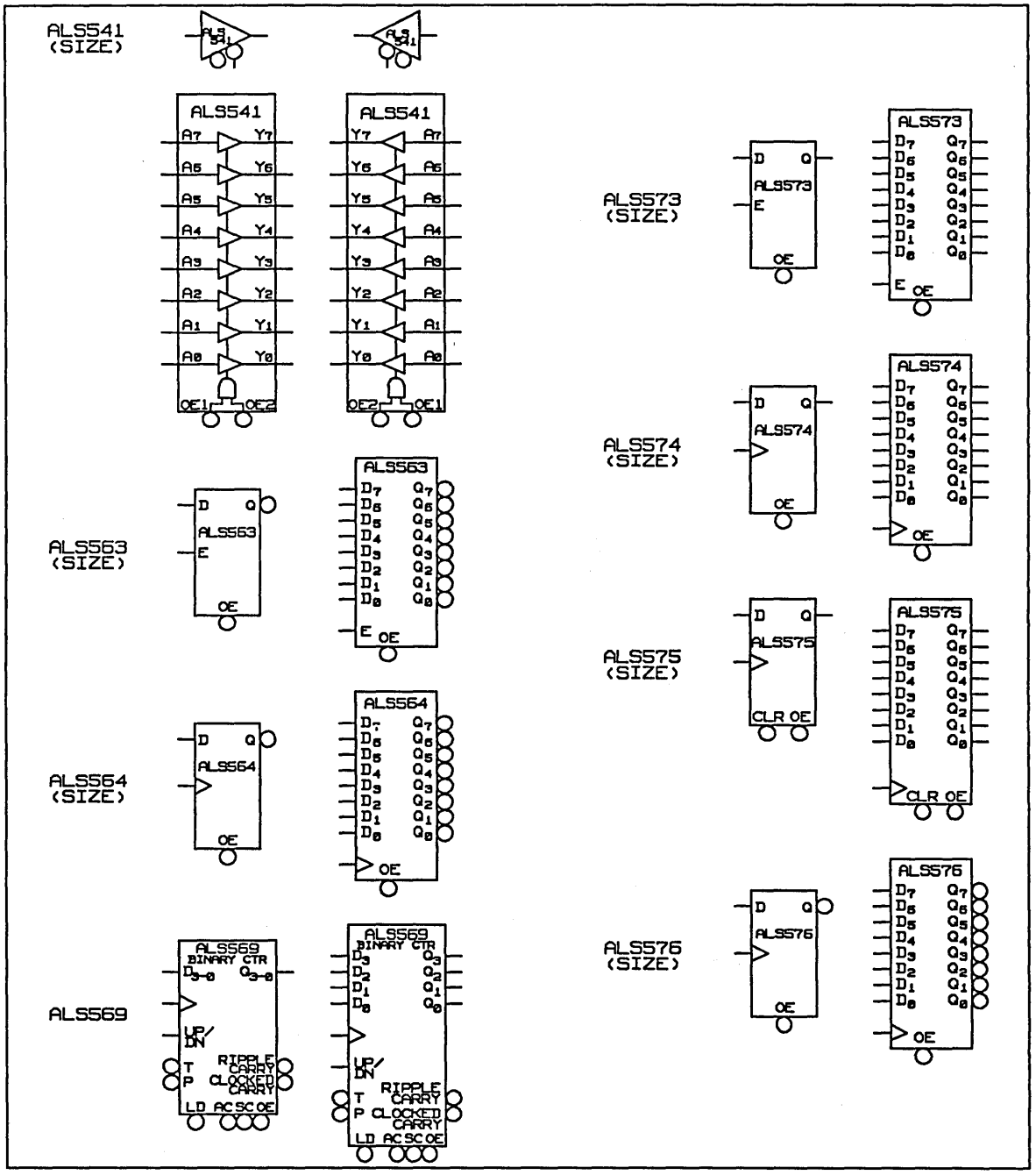
ALS368 (SIZE)

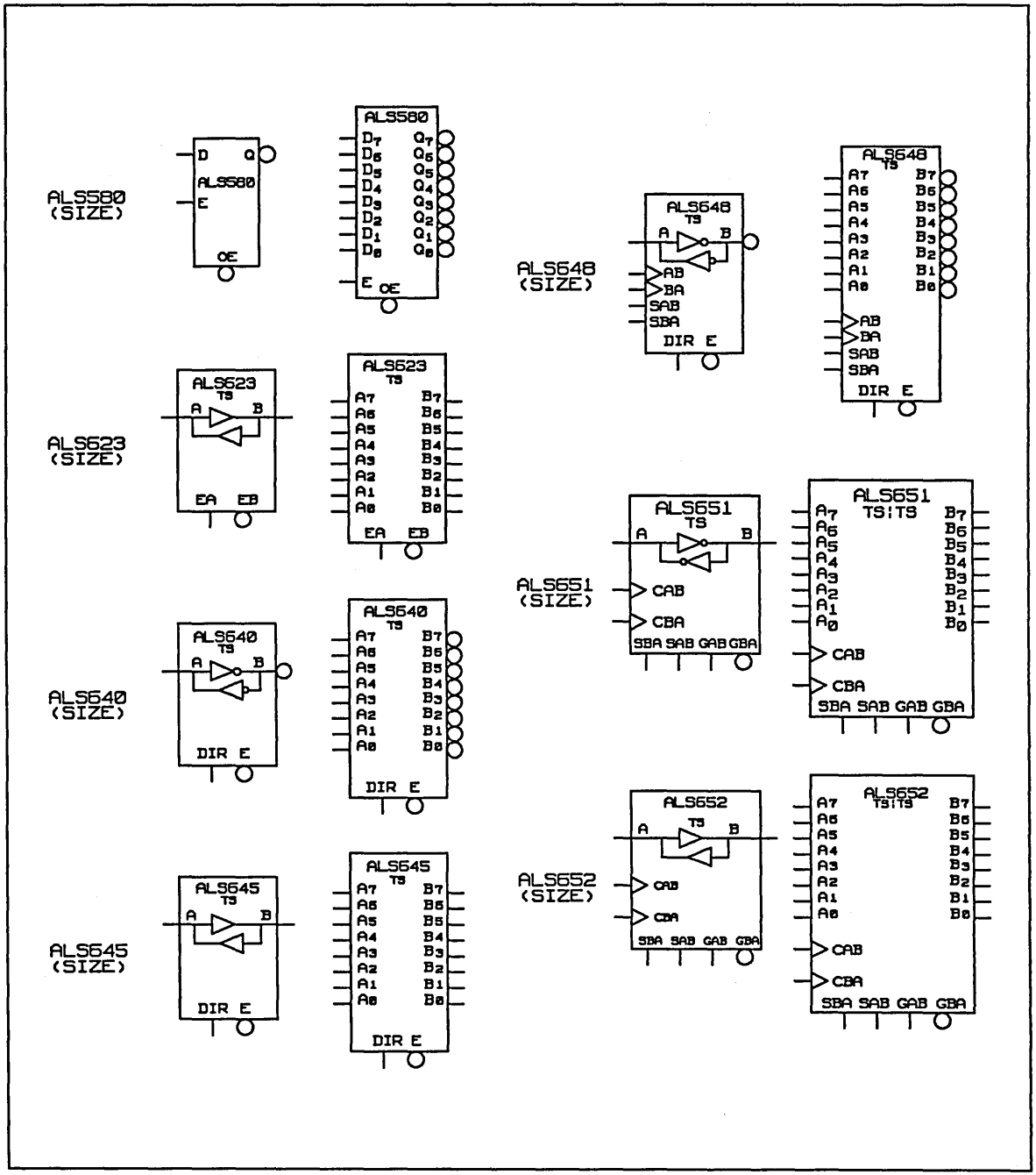


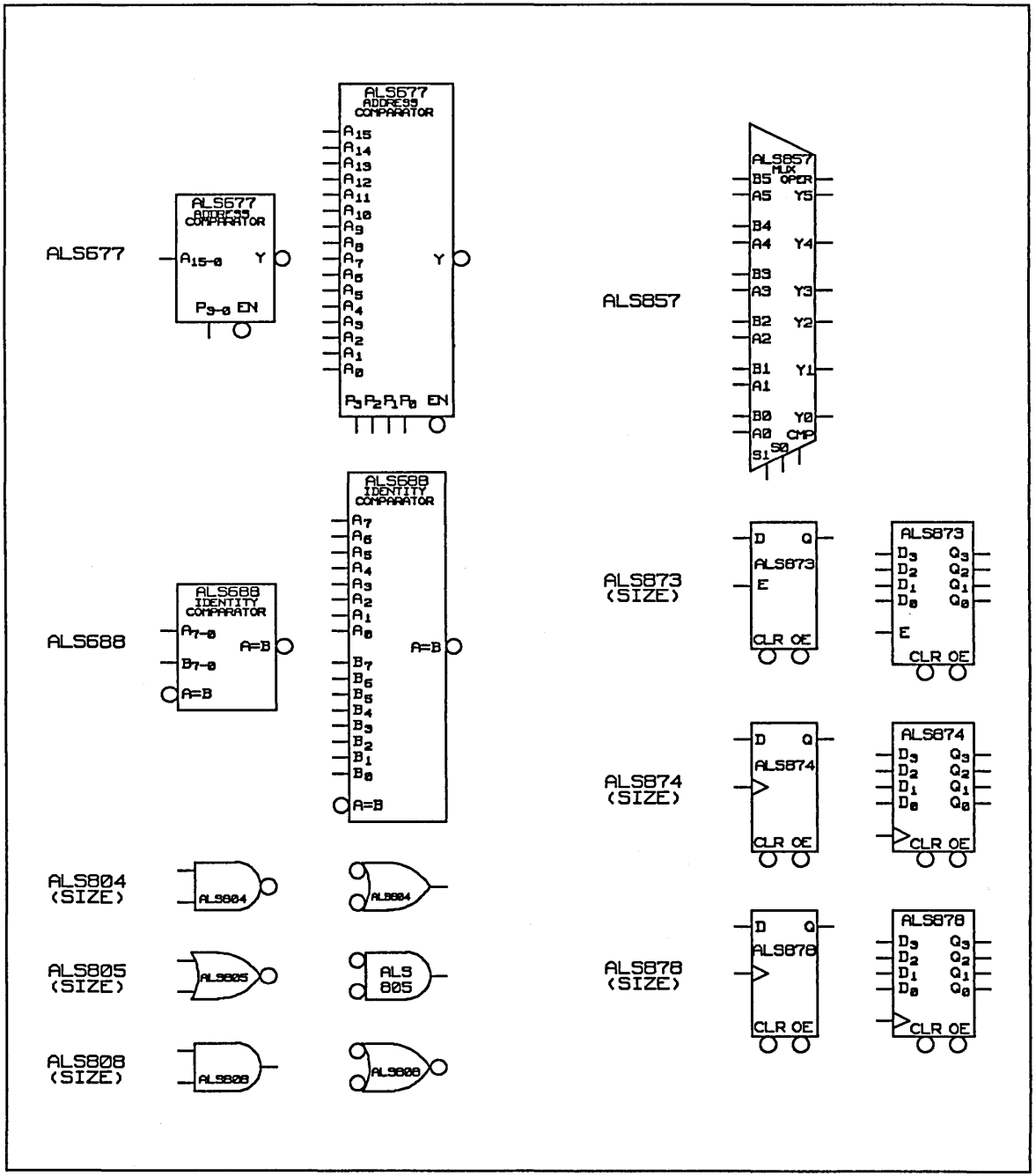
ALS373 (SIZE)

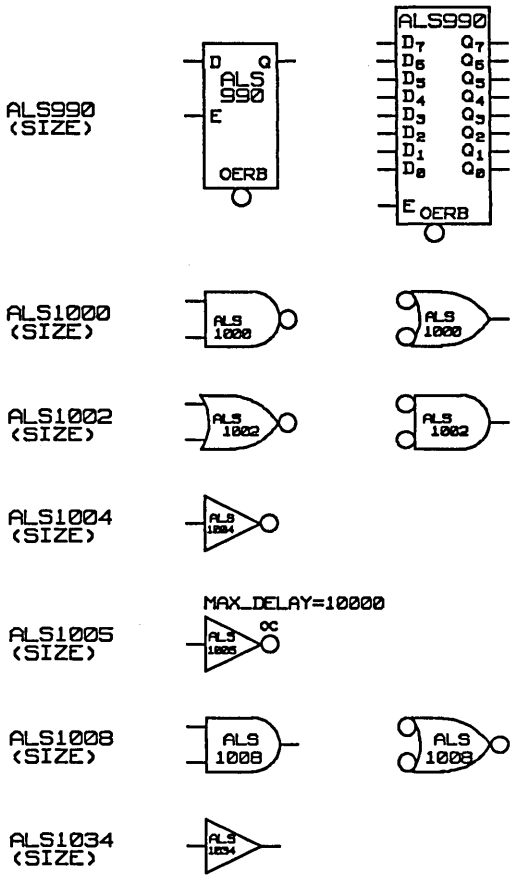


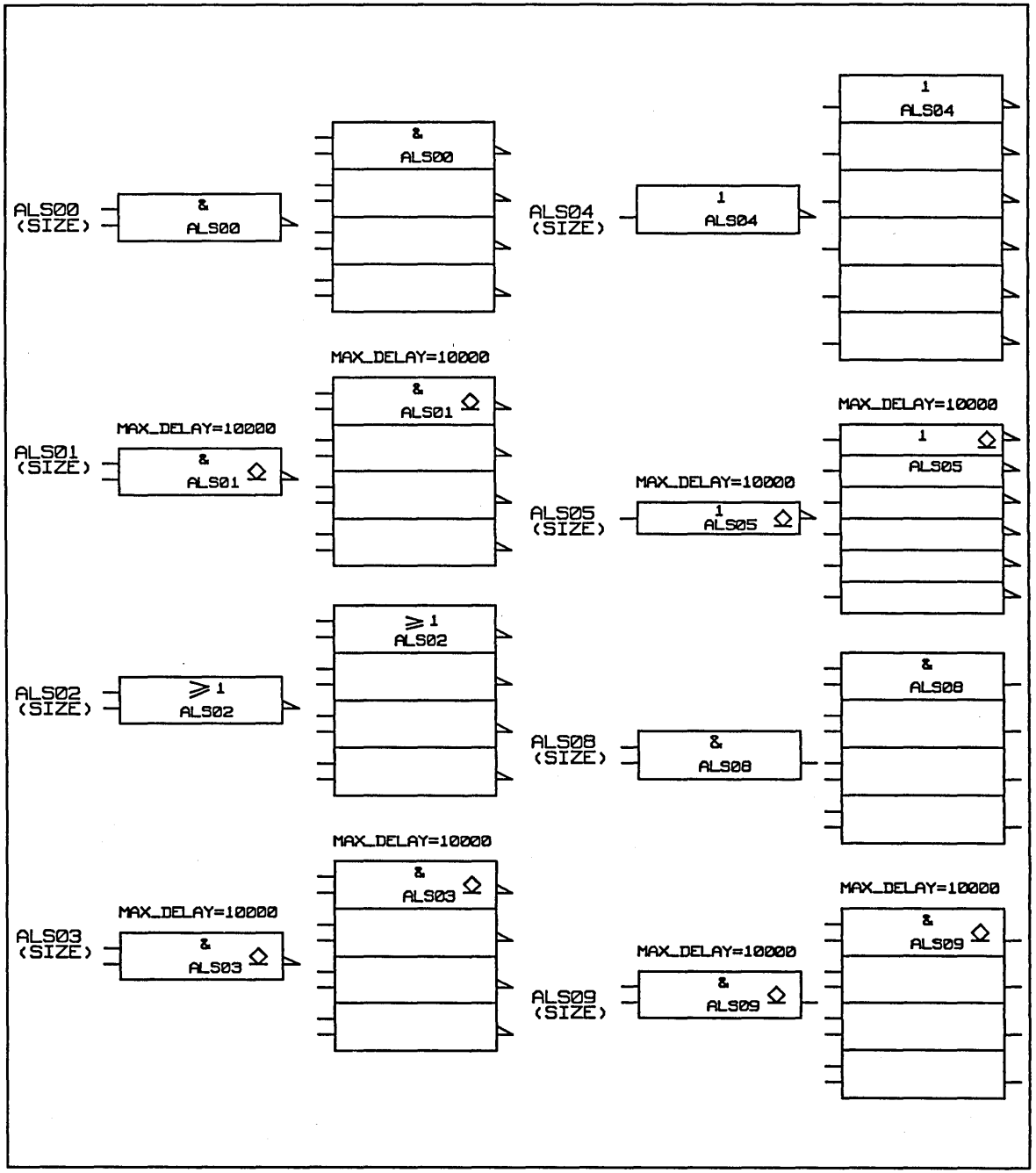

ALS374
(SIZE)
ALS374
ALS520
ALS520
IDENTITY
COMPARATOR
ALS521
ALS521
IDENTITY
COMPARATOR
ALS533
(SIZE)
ALS533
ALS534
(SIZE)
ALS534
ALS538
ALS538
DEMUX
ALS540
(SIZE)
ALS540

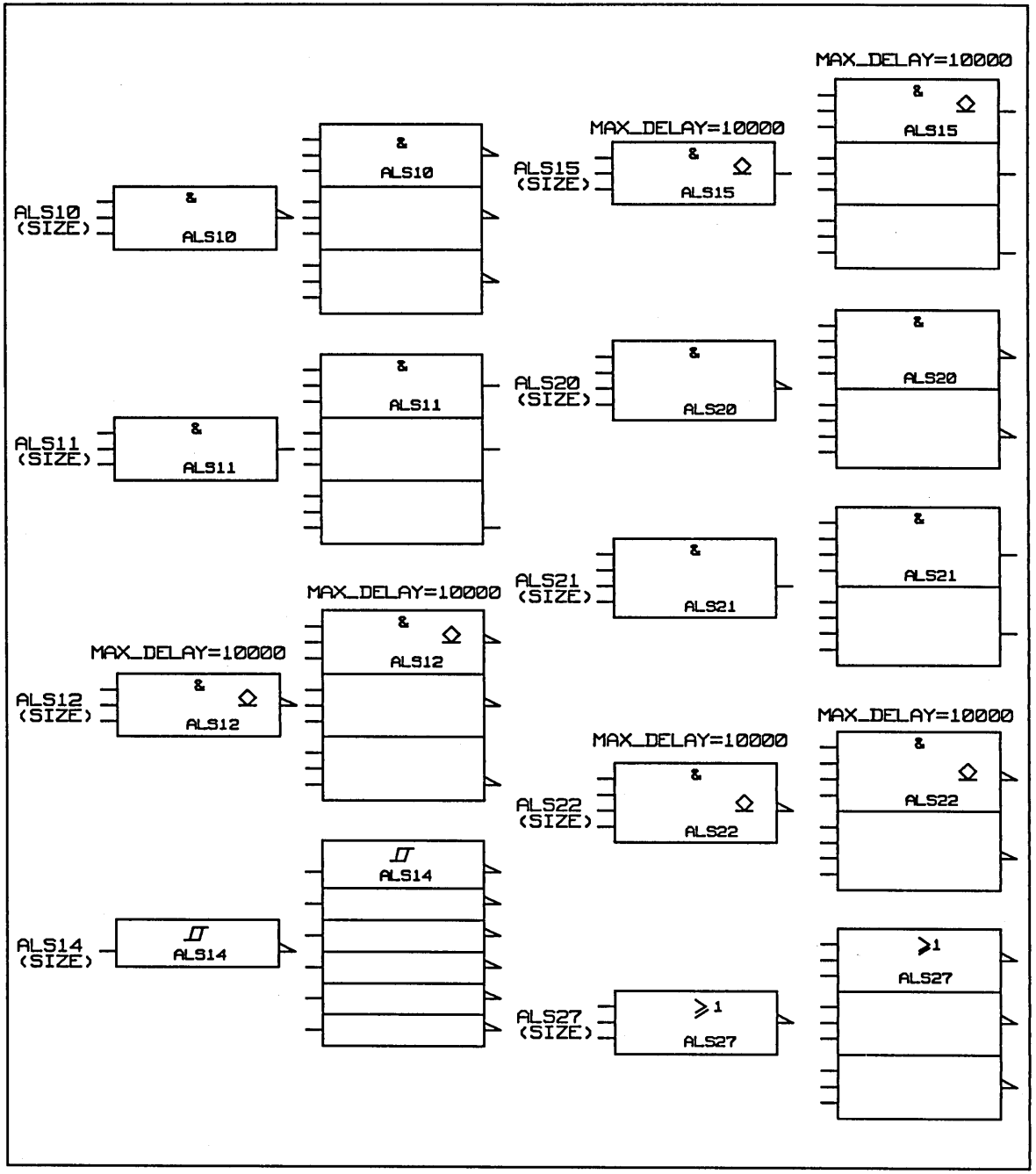

ALS541
(SIZE)
ALS541
A7 Y7
A6 Y6
A5 Y5
A4 Y4
A3 Y3
A2 Y2
A1 Y1
A0 Y0
OE1 OE2
ALS563
(SIZE)
ALS563
D Q
E
OE
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
ALS564
(SIZE)
ALS564
ALS569
ALS569
BINARY CTR
UP/
DN
RIPPLE
CARRY
CLOCKED
CARRY
LD AC SC OE
ALS573
(SIZE)
ALS573
ALS574
(SIZE)
ALS574
ALS575
(SIZE)
ALS575
CLR OE
ALS576
(SIZE)
ALS576

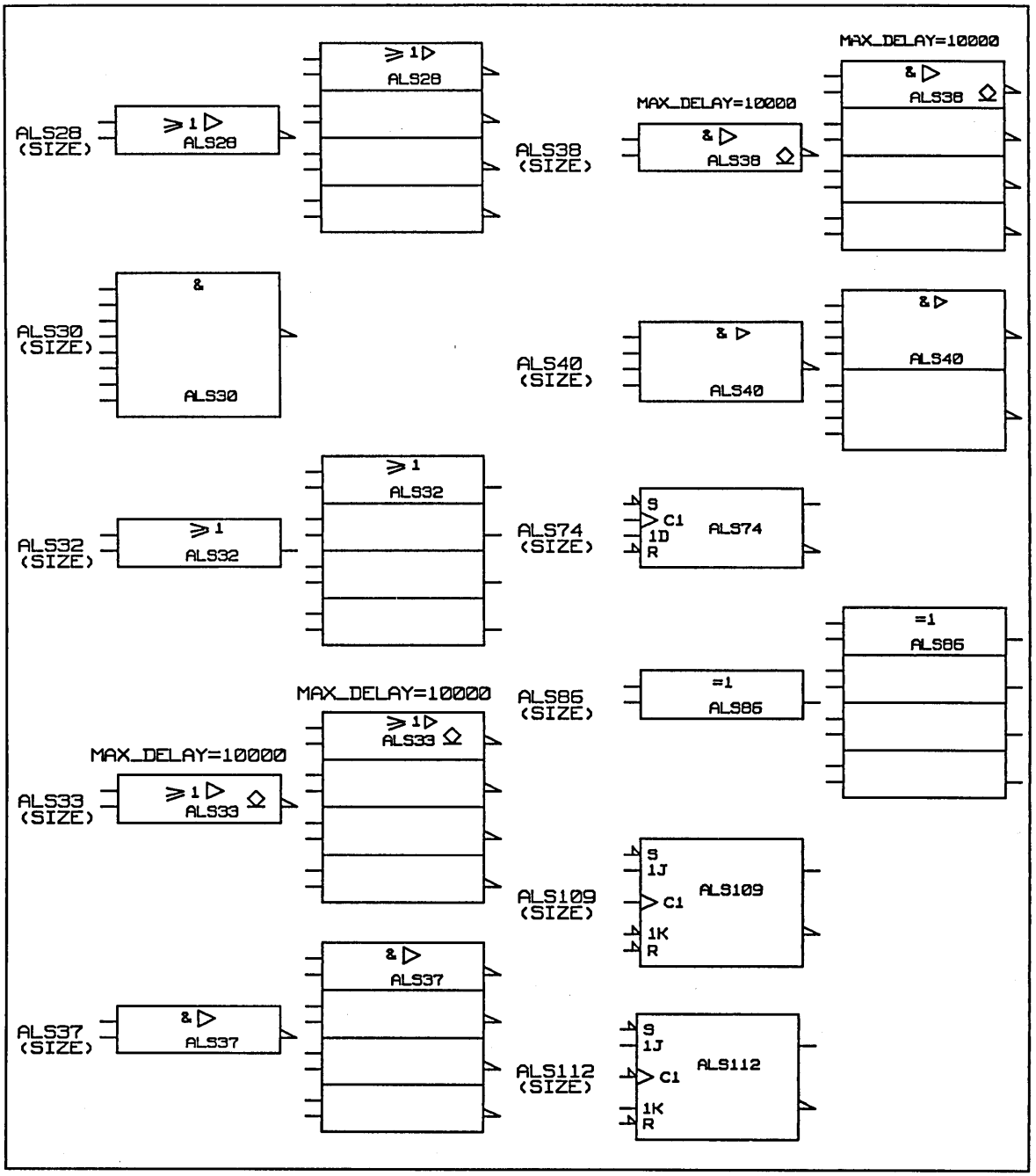

ALS580
(SIZE)
D
Q
ALS580
E
OE
ALS580
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OE
ALS623
(SIZE)
ALS623
T3
A
B
EA
EB
ALS623
T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
EA
EB
ALS640
(SIZE)
ALS640
T3
A
B
DIR
E
ALS640
T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
DIR
E
ALS645
(SIZE)
ALS645
T3
A
B
DIR
E
ALS645
T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
DIR
E
ALS648
(SIZE)
ALS648
T3
A
B
AB
BA
SAB
SBA
DIR
E
ALS648
T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
AB
BA
SAB
SBA
DIR
E
ALS651
(SIZE)
ALS651
TS
A
B
CAB
CBA
SBA
SAB
GAB
GBA
ALS651
TS!TS
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
CAB
CBA
SBA
SAB
GAB
GBA
ALS652
(SIZE)
ALS652
T3
A
B
CAB
CBA
SBA
SAB
GAB
GBA
ALS652
T3!T3
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
CAB
CBA
SBA
SAB
GAB
GBA

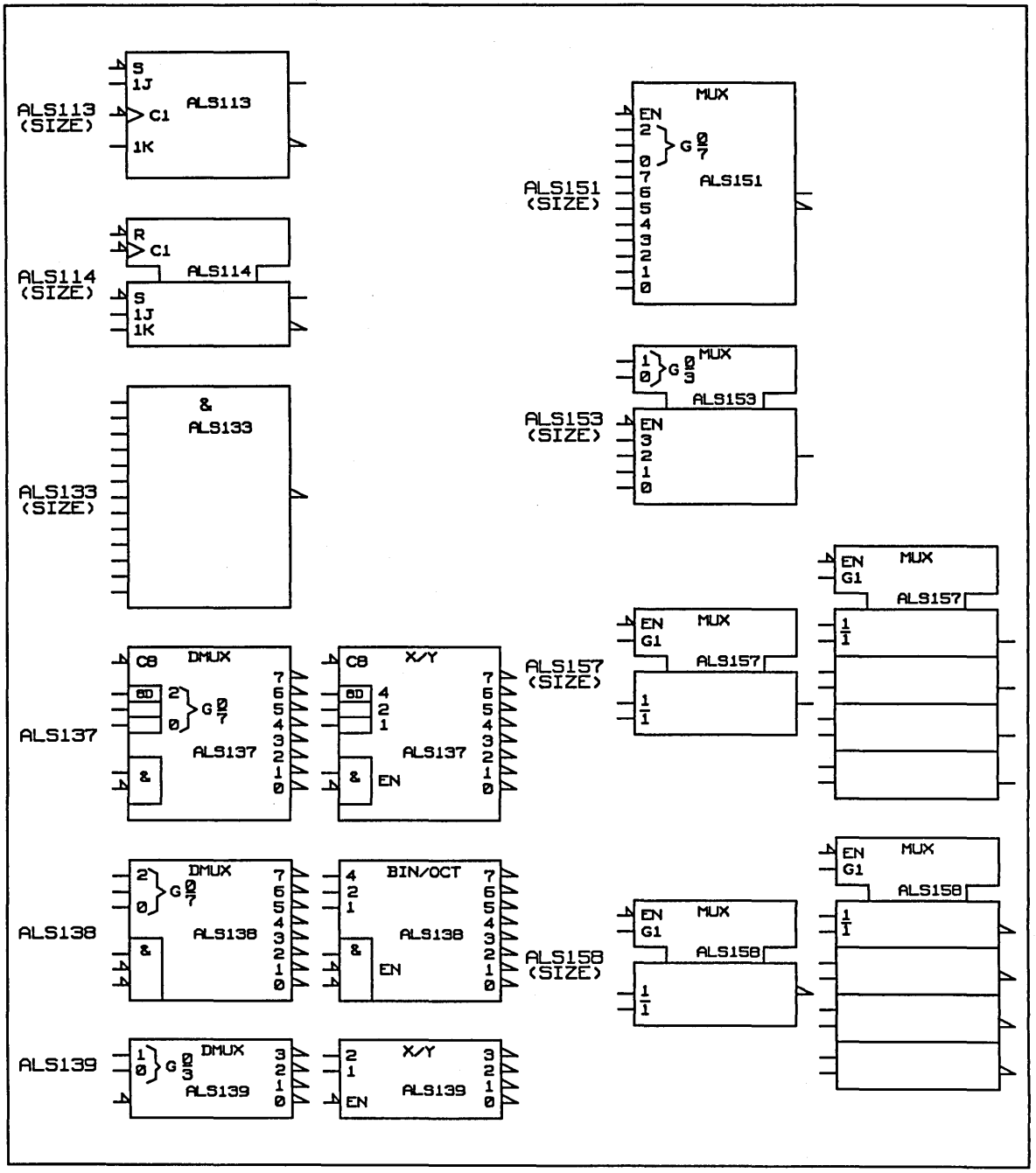

ALS677
ALS677
ADDRESS COMPARATOR
A15-0
Y
P3-0 EN
ALS677
ADDRESS COMPARATOR
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
Y
P3 P2 P1 P0 EN
ALS857
ALS857
MUX
B5 OPER
A5 Y5
B4
A4 Y4
B3
A3 Y3
B2 Y2
A2
B1 Y1
A1
B0 Y0
A0 CMP
S1 S0
ALS688
ALS688
IDENTITY COMPARATOR
A7-0
A=B
B7-0
A=B
ALS688
IDENTITY COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
A=B
B7
B6
B5
B4
B3
B2
B1
B0
A=B
ALS873
(SIZE)
D Q
ALS873
E
CLR OE
ALS873
D3 Q3
D2 Q2
D1 Q1
D0 Q0
E
CLR OE
ALS874
(SIZE)
D Q
ALS874
CLR OE
ALS874
D3 Q3
D2 Q2
D1 Q1
D0 Q0
CLR OE
ALS804
(SIZE)
ALS804
ALS804
ALS805
(SIZE)
ALS805
ALS
805
ALS808
(SIZE)
ALS808
ALS808
ALS878
(SIZE)
D Q
ALS878
CLR OE
ALS878
D3 Q3
D2 Q2
D1 Q1
D0 Q0
CLR OE

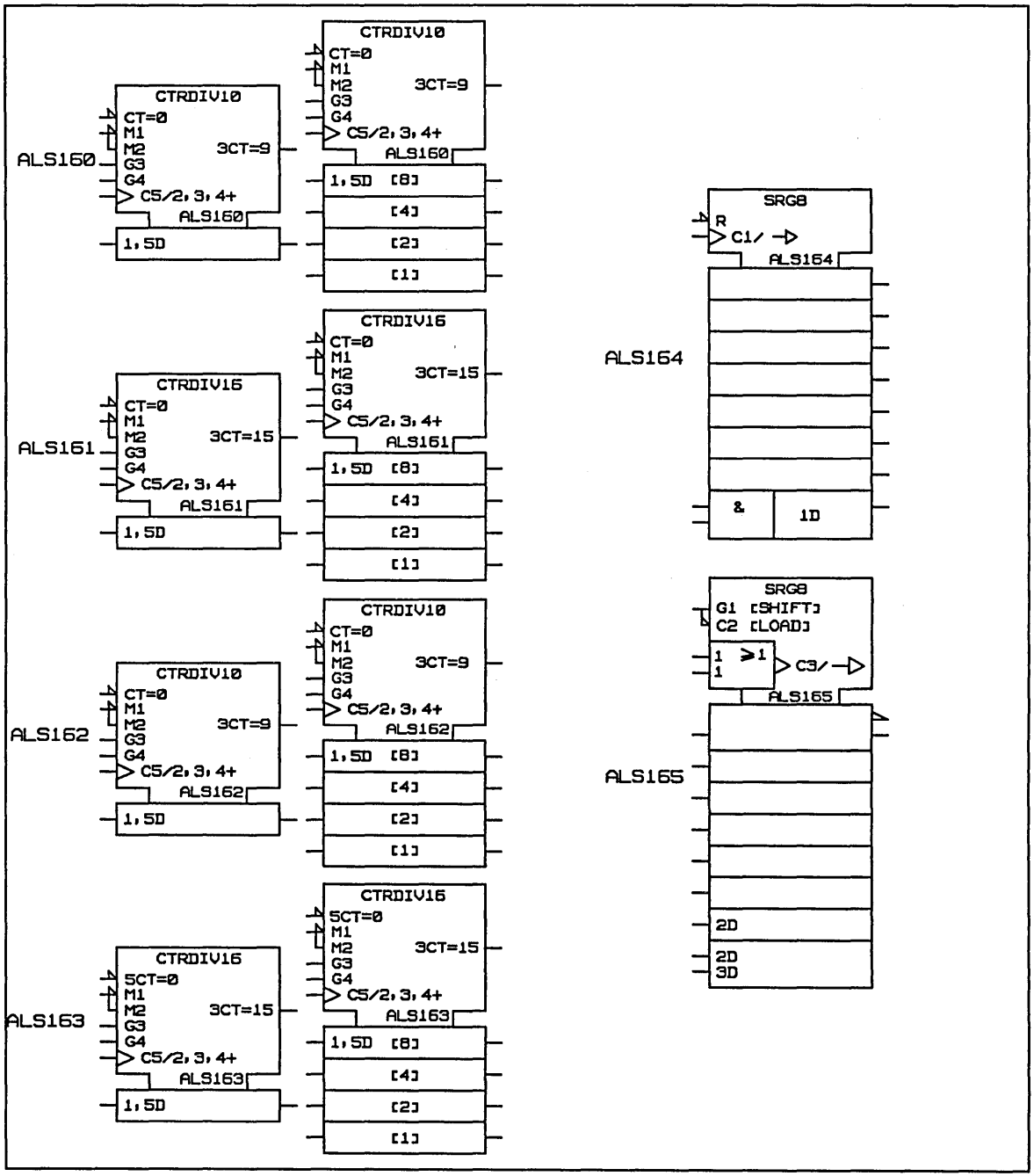

ALS990
(SIZE)
D
Q
ALS
990
E
OERB
ALS990
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OERB
ALS1000
(SIZE)
ALS
1000
ALS1002
(SIZE)
ALS
1002
ALS1004
(SIZE)
ALS1005
(SIZE)
MAX_DELAY=10000
OC
ALS1008
(SIZE)
ALS
1008
ALS1034
(SIZE)

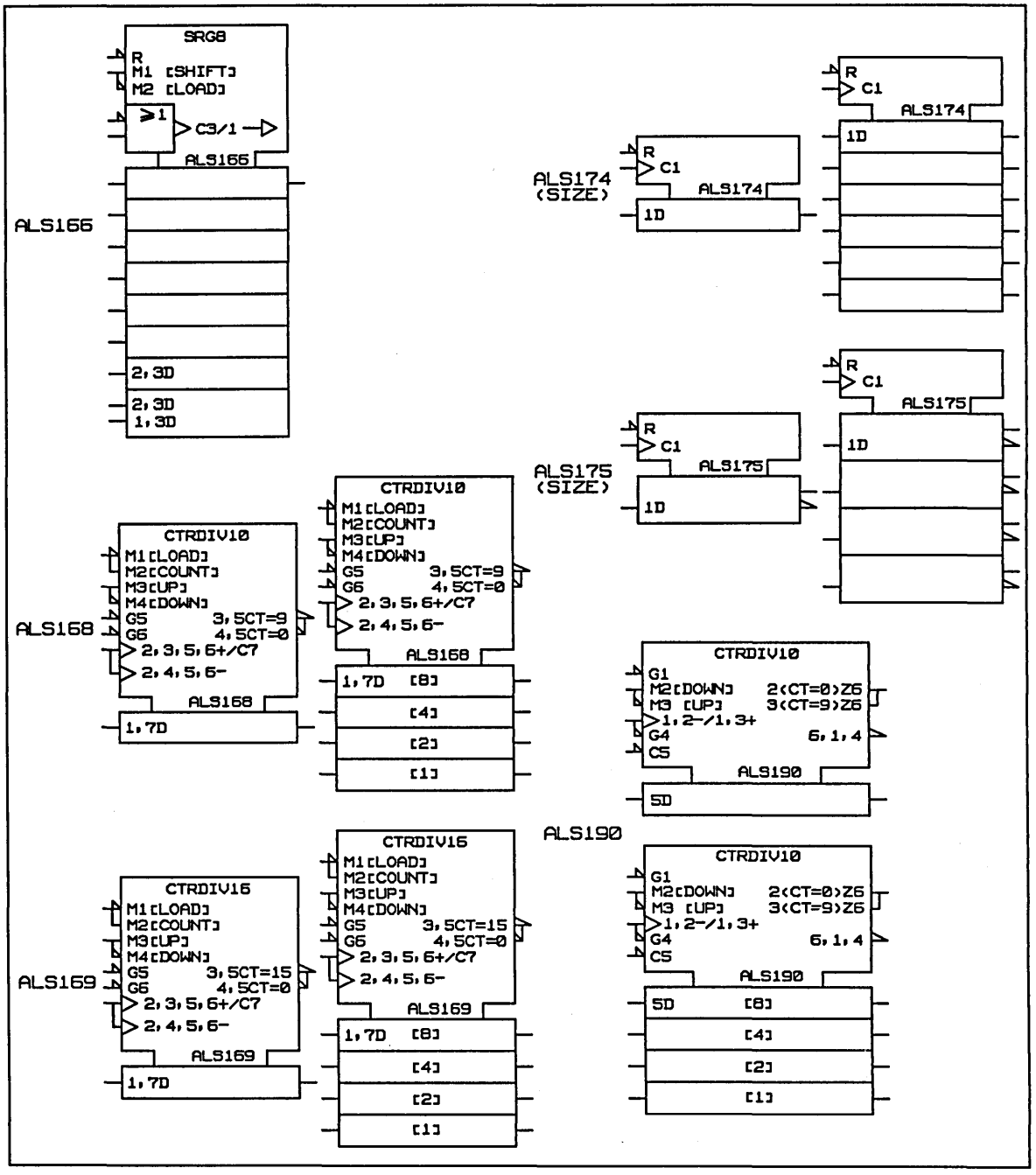

ALS00
(SIZE)
&
ALS00
&
ALS00
ALS04
(SIZE)
1
ALS04
1
ALS04
MAX_DELAY=10000
ALS01
(SIZE)
MAX_DELAY=10000
&
ALS01
&
ALS01
MAX_DELAY=10000
ALS05
(SIZE)
MAX_DELAY=10000
1
ALS05
1
ALS05
ALS02
(SIZE)
≥1
ALS02
≥1
ALS02
ALS08
(SIZE)
&
ALS08
&
ALS08
MAX_DELAY=10000
ALS03
(SIZE)
MAX_DELAY=10000
&
ALS03
&
ALS03
MAX_DELAY=10000
ALS09
(SIZE)
MAX_DELAY=10000
&
ALS09
&
ALS09

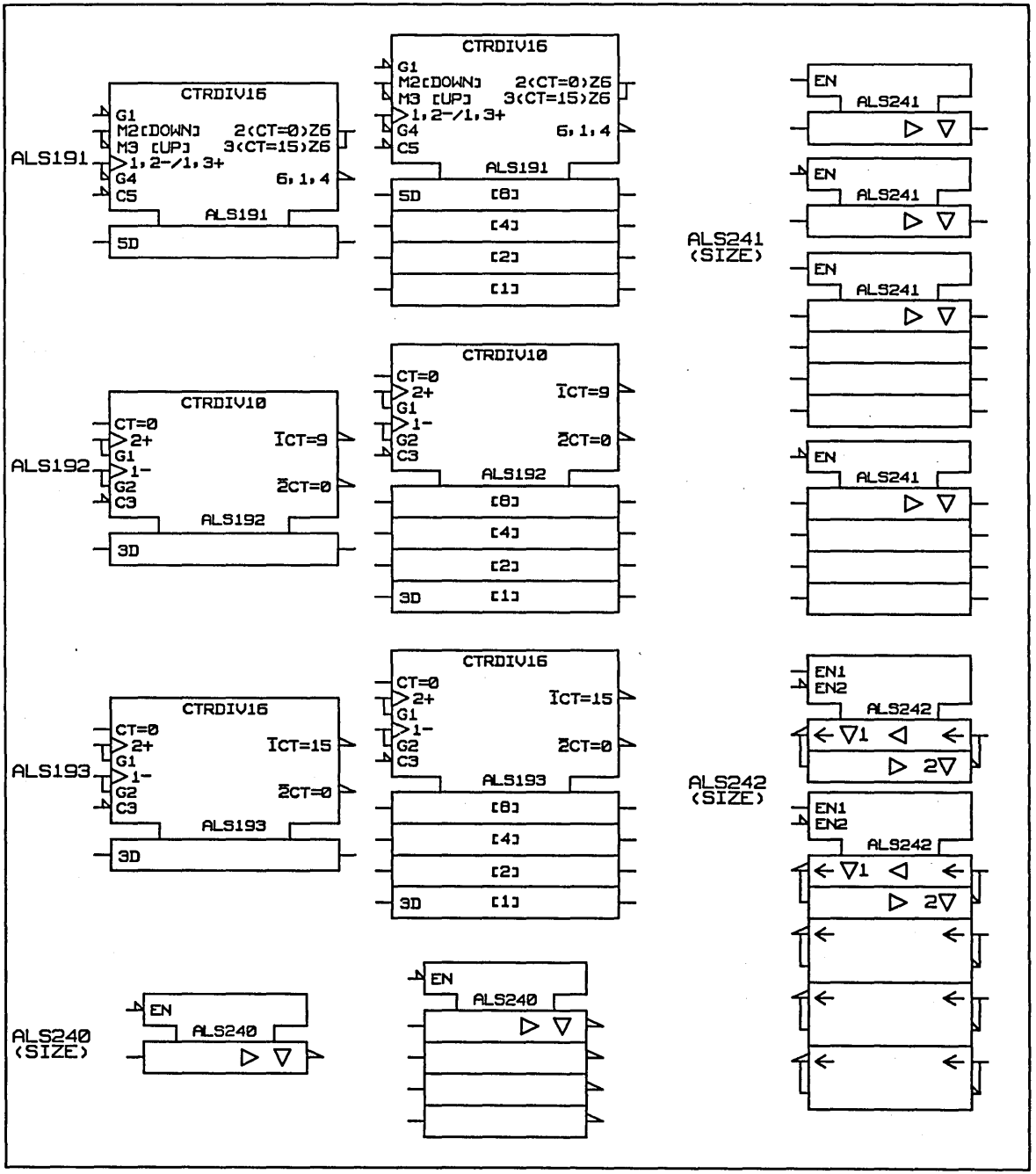

ALS10
(SIZE)
&
ALS10
&
ALS10
ALS11
(SIZE)
&
ALS11
&
ALS11
MAX_DELAY=10000
ALS12
(SIZE)
&
ALS12
MAX_DELAY=10000
&
ALS12
ALS14
(SIZE)
ALS14
ALS14
ALS15
(SIZE)
MAX_DELAY=10000
&
ALS15
MAX_DELAY=10000
&
ALS15
ALS20
(SIZE)
&
ALS20
&
ALS20
ALS21
(SIZE)
&
ALS21
&
ALS21
ALS22
(SIZE)
MAX_DELAY=10000
&
ALS22
MAX_DELAY=10000
&
ALS22
ALS27
(SIZE)
≥1
ALS27
≥1
ALS27

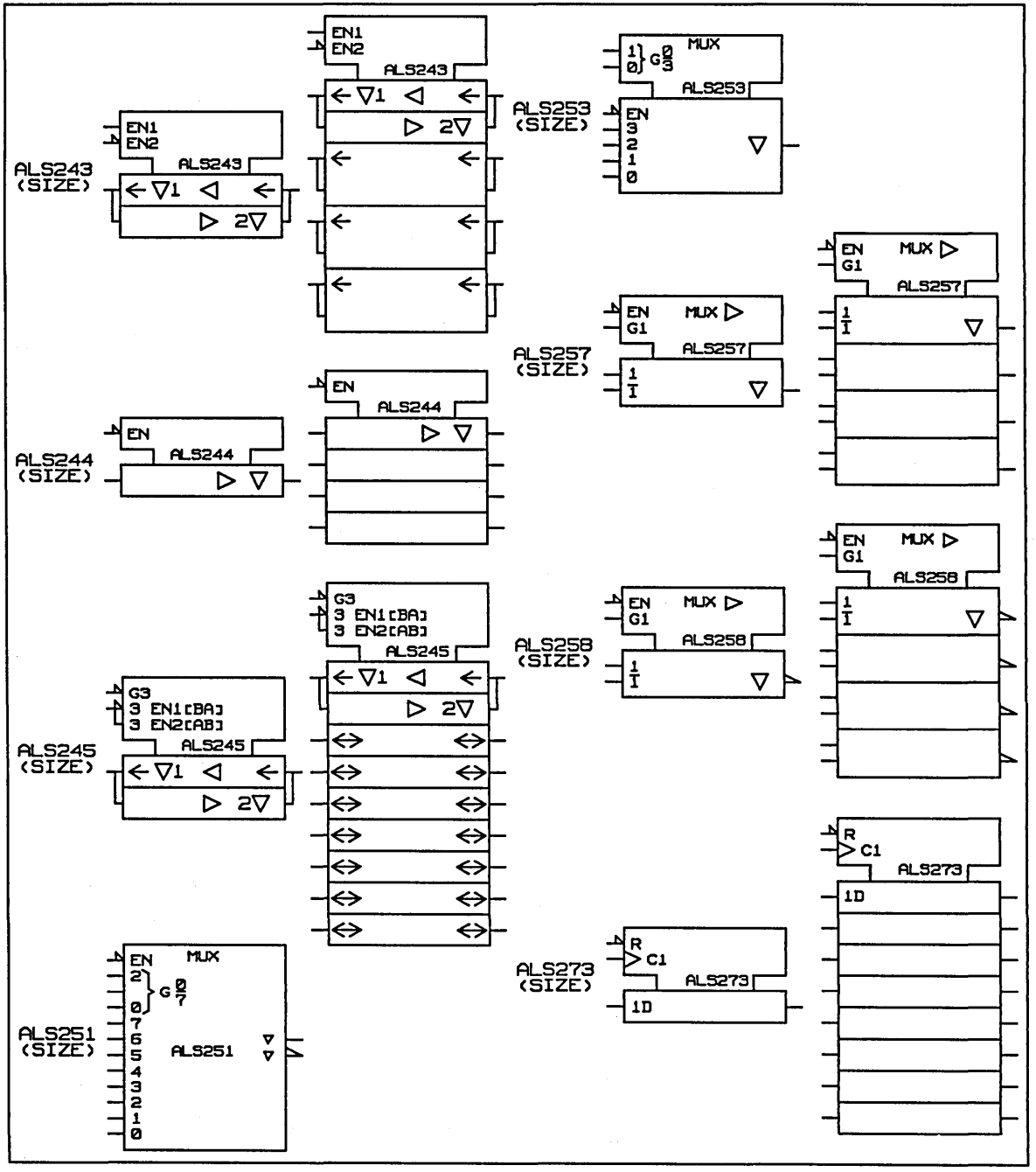

ALS28 (SIZE)
≥1
ALS28
ALS38 (SIZE)
MAX_DELAY=10000
&
ALS38
ALS30 (SIZE)
ALS30
ALS40 (SIZE)
ALS40
ALS32 (SIZE)
ALS32
ALS74 (SIZE)
S
C1
1D
R
ALS74
ALS86 (SIZE)
=1
ALS86
MAX_DELAY=10000
ALS33 (SIZE)
ALS33
ALS109 (SIZE)
S
1J
C1
1K
R
ALS109
ALS37 (SIZE)
ALS37
ALS112 (SIZE)
ALS112

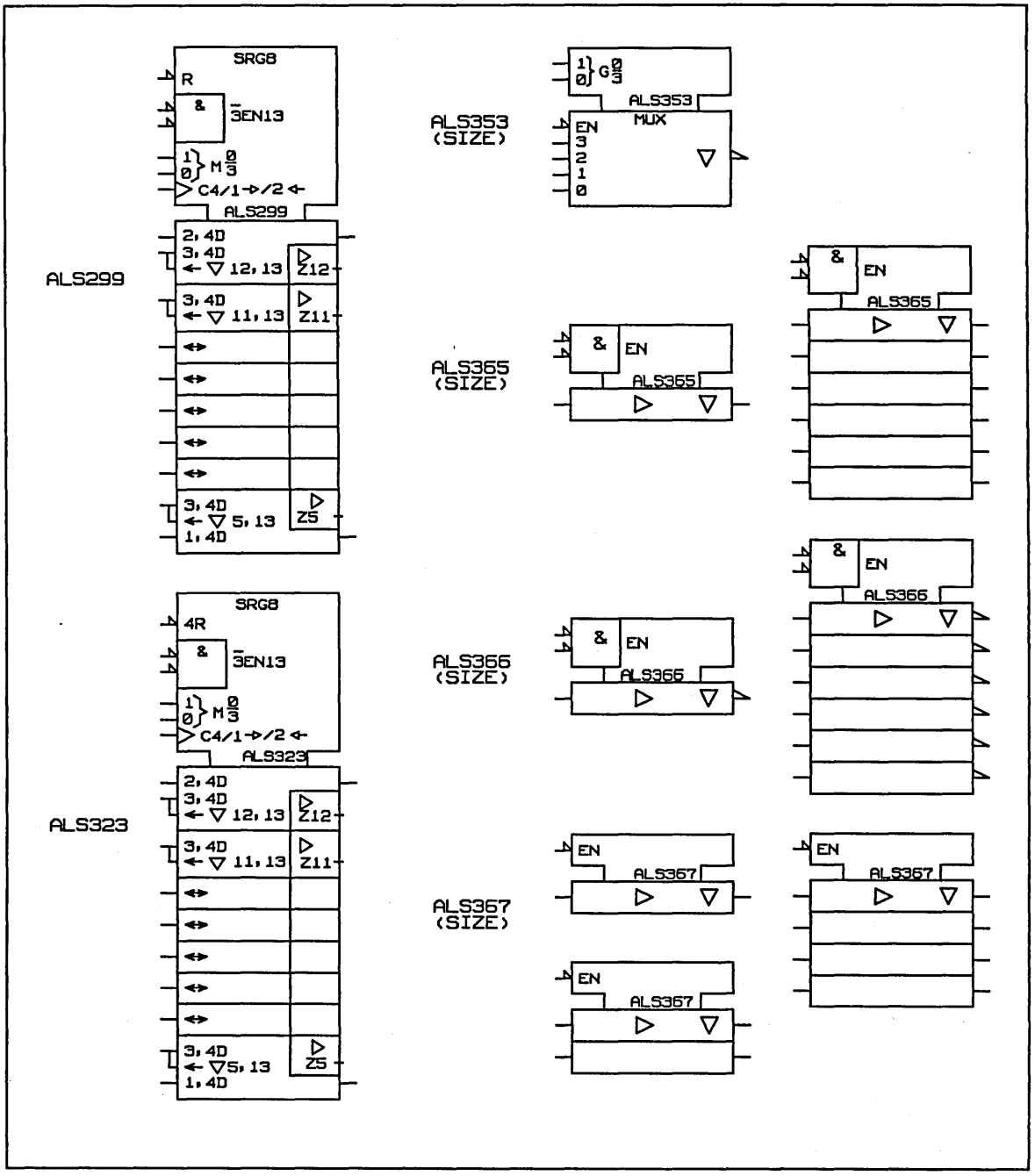

ALS113
(SIZE)
S
1J
C1
1K
ALS113
ALS114
(SIZE)
R
C1
ALS114
S
1J
1K
ALS133
(SIZE)
&
ALS133
ALS137
C8
DMUX
G
ALS137
X/Y
EN
ALS138
DMUX
BIN/OCT
ALS138
EN
ALS139
DMUX
X/Y
ALS139
EN
ALS151
(SIZE)
MUX
EN
G
ALS151
ALS153
(SIZE)
MUX
ALS153
EN
ALS157
(SIZE)
MUX
EN
G1
ALS157
ALS158
(SIZE)
MUX
EN
G1
ALS158

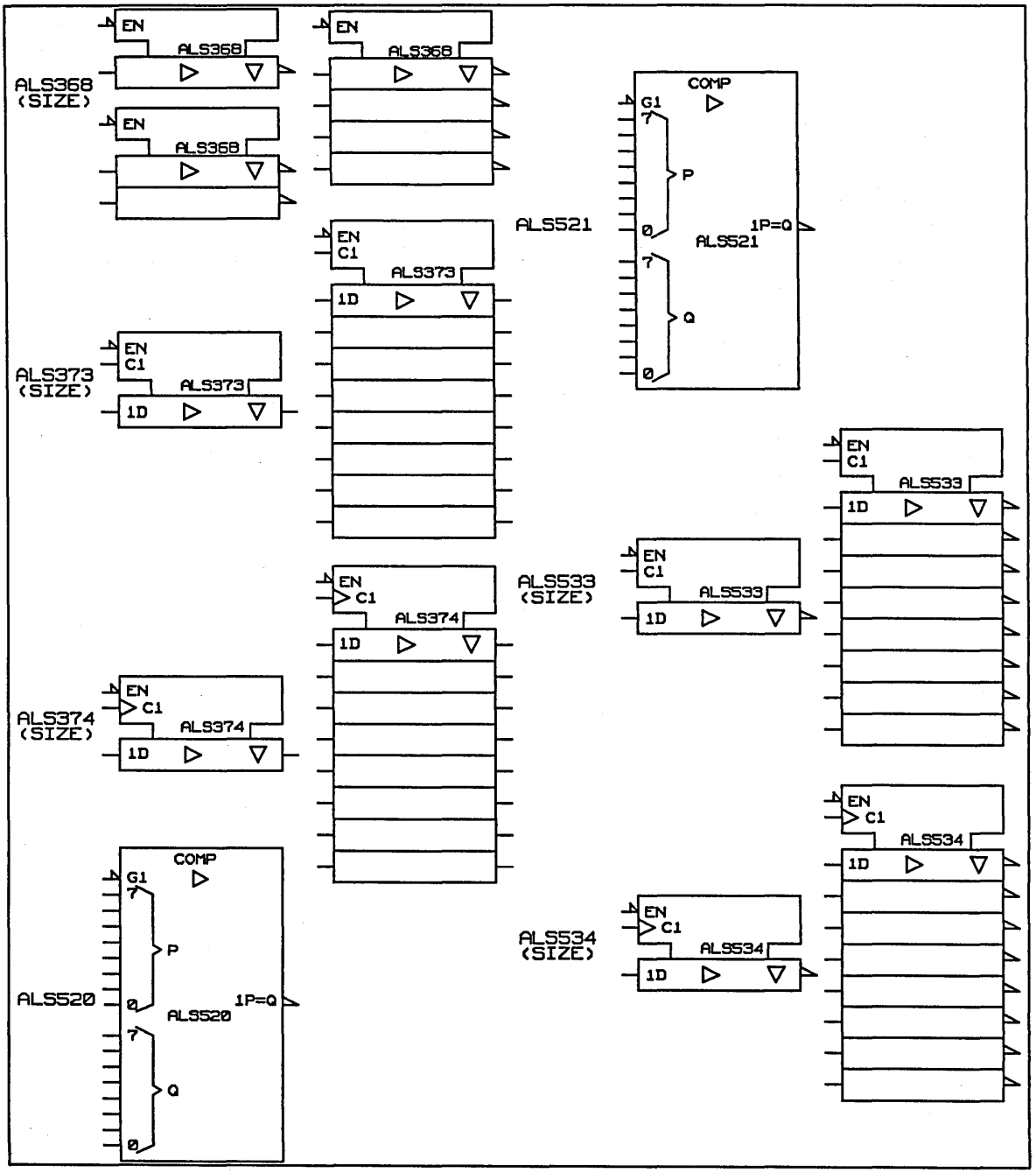

ALS160
CTRDIV10
CT=0
M1
M2
G3
G4
C5/2,3,4+
3CT=9
ALS160
1,5D
[8]
[4]
[2]
[1]
ALS161
CTRDIV16
3CT=15
ALS161
ALS162
ALS163
5CT=0
ALS164
SRG8
R
C1/
&
1D
ALS165
G1 [SHIFT]
C2 [LOAD]
1
≥1
C3/
2D
3D

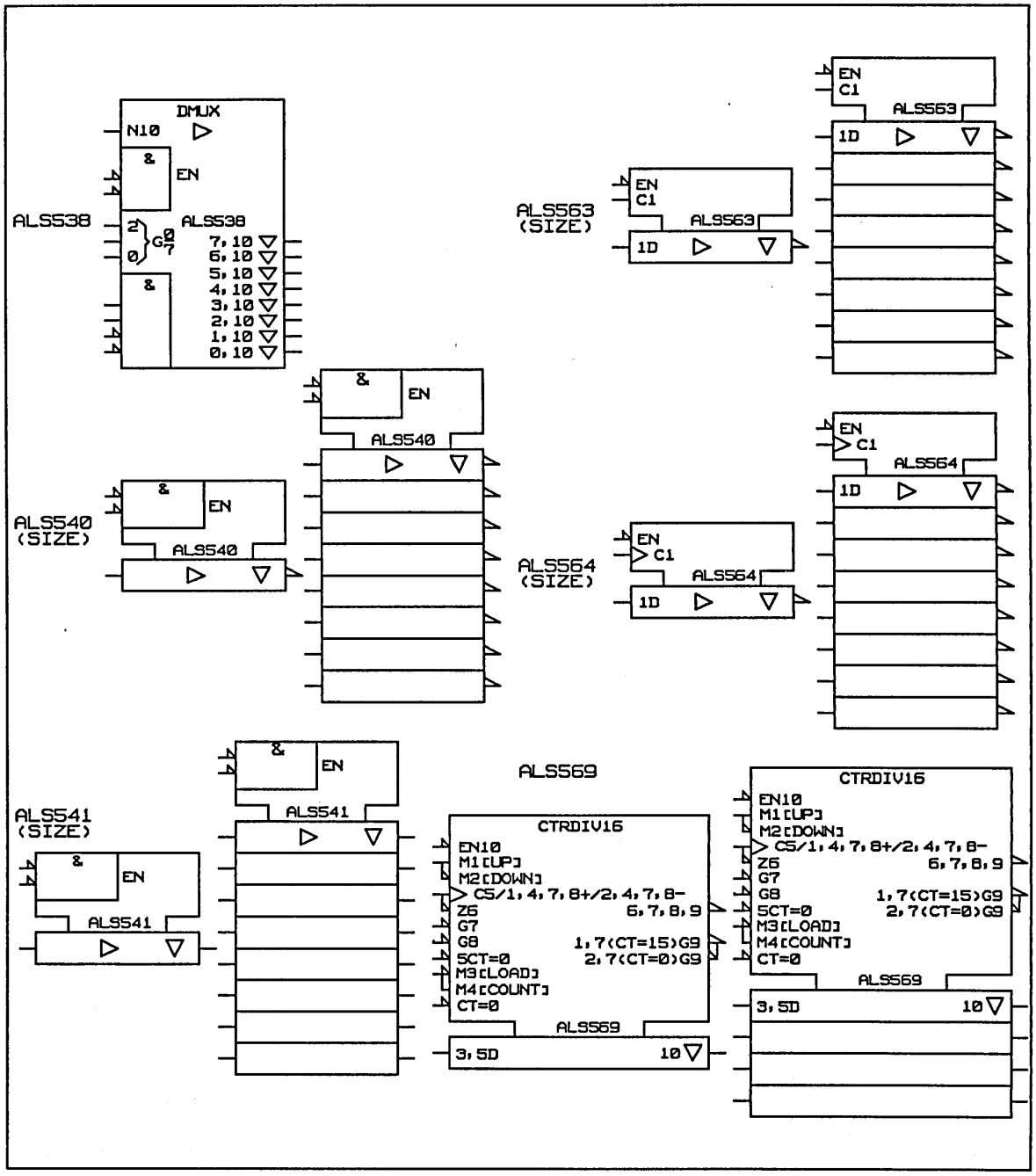

SRG8
R
M1 [SHIFT]
M2 [LOAD]
≥1
C3/1
ALS166
ALS166
2,3D
2,3D
1,3D
R
C1
ALS174
1D
ALS174
(SIZE)
R
C1
ALS174
1D
R
C1
ALS175
1D
ALS175
(SIZE)
R
C1
ALS175
1D
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=9
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
ALS168
1,7D [8]
[4]
[2]
[1]
ALS168
1,7D
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=9
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
ALS168
CTRDIV10
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=9>Z6
1,2-/1,3+
G4 6,1,4
C5
ALS190
5D
ALS190
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
ALS169
1,7D [8]
[4]
[2]
[1]
ALS169
1,7D
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
ALS169
CTRDIV10
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=9>Z6
1,2-/1,3+
G4 6,1,4
C5
ALS190
5D [8]
[4]
[2]
[1]

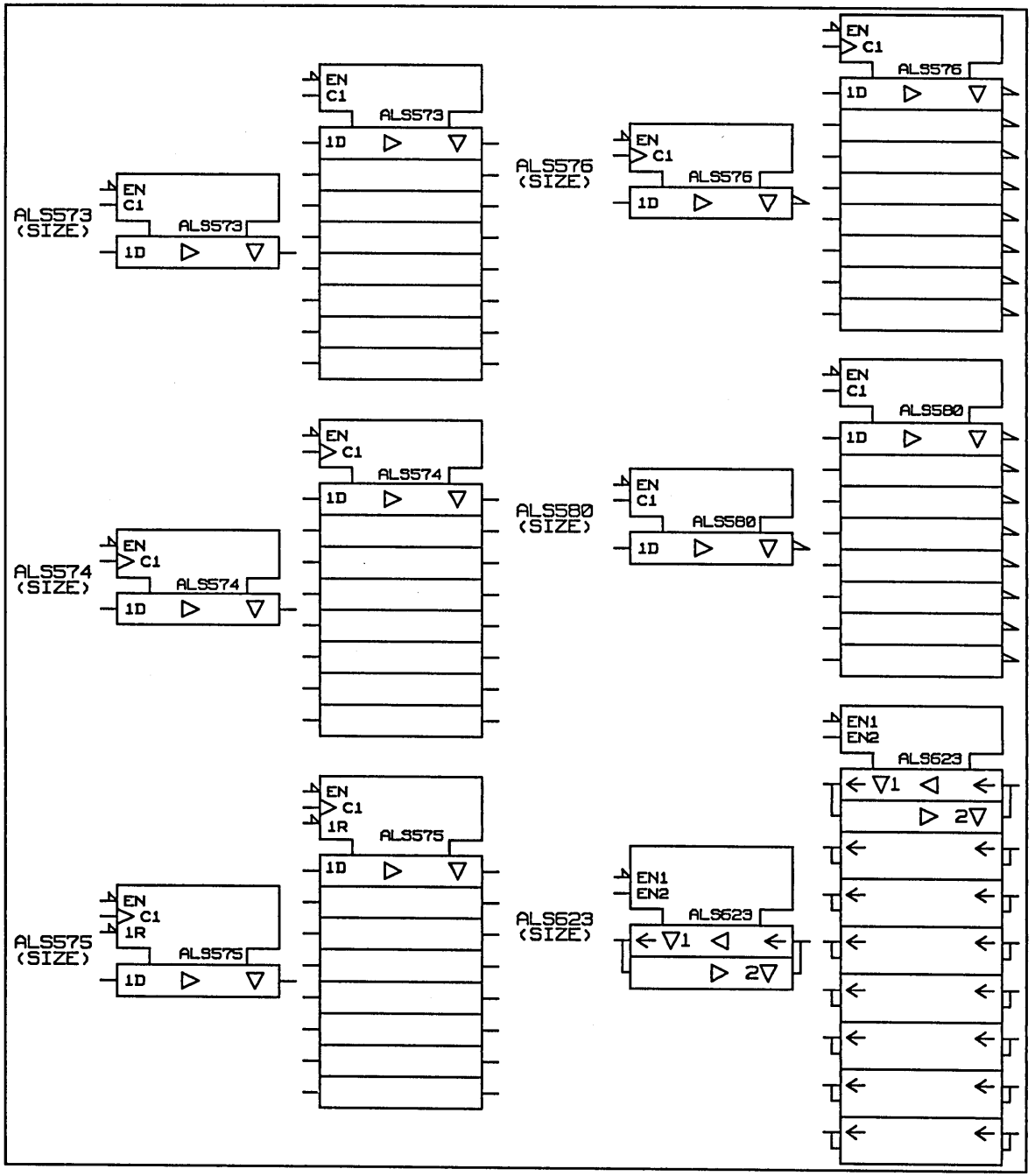

ALS191
CTRDIV16
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=15>Z6
1,2-/1,3+
G4 6,1,4
C5
ALS191
5D
CTRDIV16
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=15>Z6
1,2-/1,3+
G4 6,1,4
C5
ALS191
5D [8]
[4]
[2]
[1]
ALS241
(SIZE)
EN
ALS241
ALS192
CTRDIV10
CT=0
2+
G1
1-
G2 ICT=9
C3 ZCT=0
ALS192
3D
CTRDIV10
CT=0
2+
G1
1-
G2 ICT=9
C3 ZCT=0
ALS192
3D [8]
[4]
[2]
[1]
ALS193
CTRDIV16
CT=0
2+
G1
1-
G2 ICT=15
C3 ZCT=0
ALS193
3D
CTRDIV16
CT=0
2+
G1
1-
G2 ICT=15
C3 ZCT=0
ALS193
3D [8]
[4]
[2]
[1]
ALS242
(SIZE)
EN1
EN2
ALS242
1
2
ALS240
(SIZE)
EN
ALS240

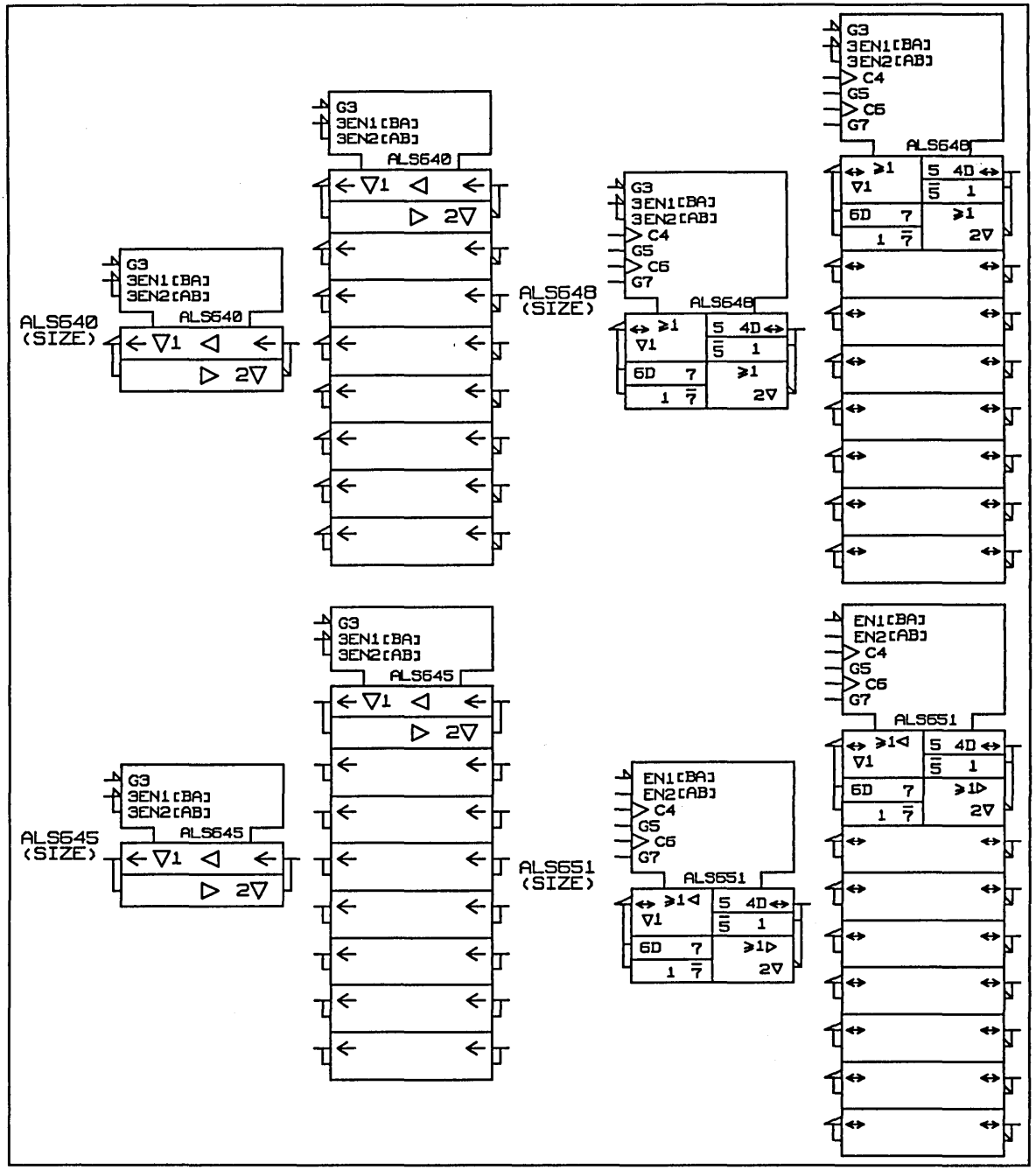

EN1
EN2
ALS243
ALS243
(SIZE)
EN
ALS244
ALS244
(SIZE)
G3
3 EN1[BA]
3 EN2[AB]
ALS245
ALS245
(SIZE)
EN
MUX
ALS251
ALS251
(SIZE)
MUX
ALS253
ALS253
(SIZE)
EN
G1
MUX
ALS257
ALS257
(SIZE)
EN
G1
MUX
ALS258
ALS258
(SIZE)
R
C1
ALS273
1D
ALS273
(SIZE)

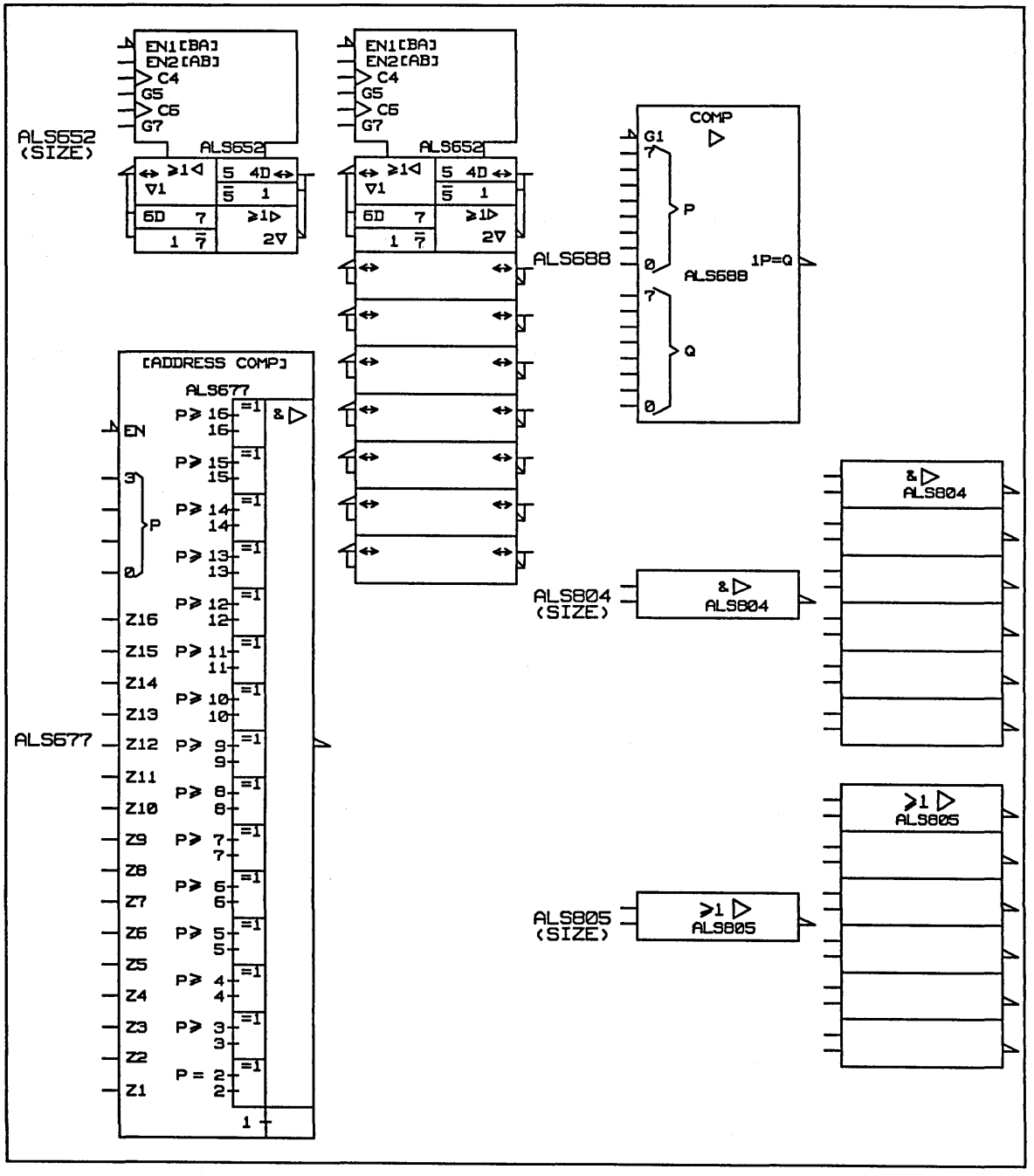

ALS299
SRG8
R
&
3EN13
M
C4/1→/2←
ALS299
2, 4D
3, 4D
12, 13
Z12
3, 4D
11, 13
Z11
3, 4D
5, 13
Z5
1, 4D
ALS323
SRG8
4R
&
3EN13
M
C4/1→/2←
ALS323
2, 4D
3, 4D
12, 13
Z12
3, 4D
11, 13
Z11
3, 4D
5, 13
Z5
1, 4D
ALS353
(SIZE)
G
ALS353
MUX
EN
3
2
1
0
ALS365
(SIZE)
&
EN
ALS365
ALS366
(SIZE)
&
EN
ALS366
ALS367
(SIZE)
EN
ALS367
EN
ALS367
&
EN
ALS365
&
EN
ALS366
EN
ALS367

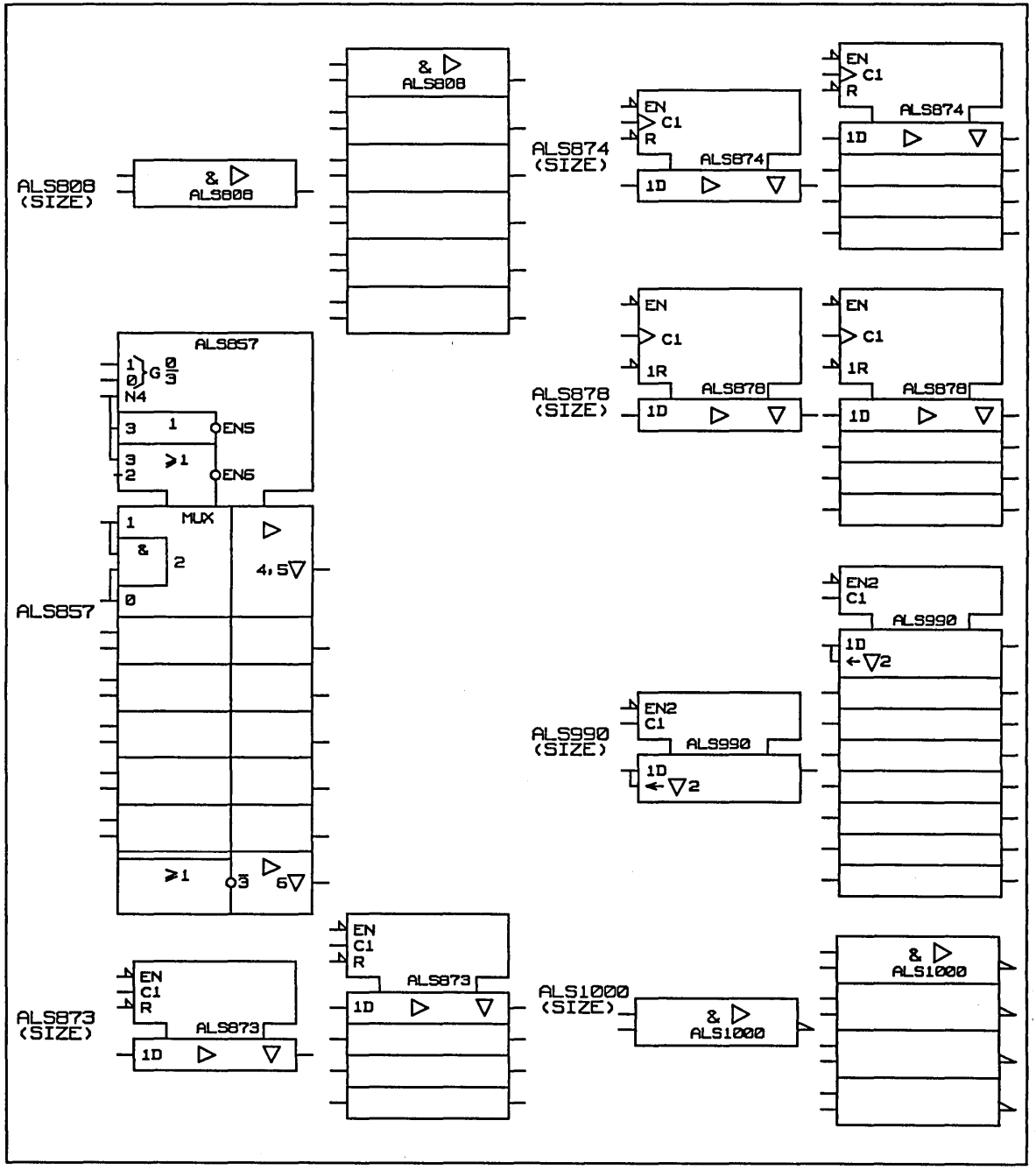

EN
ALS368
ALS368
(SIZE)
EN
ALS368
EN
ALS368
EN
C1
ALS373
1D
ALS521
COMP
G1
P
0
1P=Q
ALS521
Q
EN
C1
ALS373
ALS373
(SIZE)
1D
EN
C1
ALS533
1D
EN
C1
ALS374
1D
ALS533
(SIZE)
EN
C1
ALS533
1D
EN
C1
ALS374
ALS374
(SIZE)
1D
EN
C1
ALS534
1D
COMP
G1
P
ALS520
0
1P=Q
ALS520
Q
EN
C1
ALS534
ALS534
(SIZE)
1D

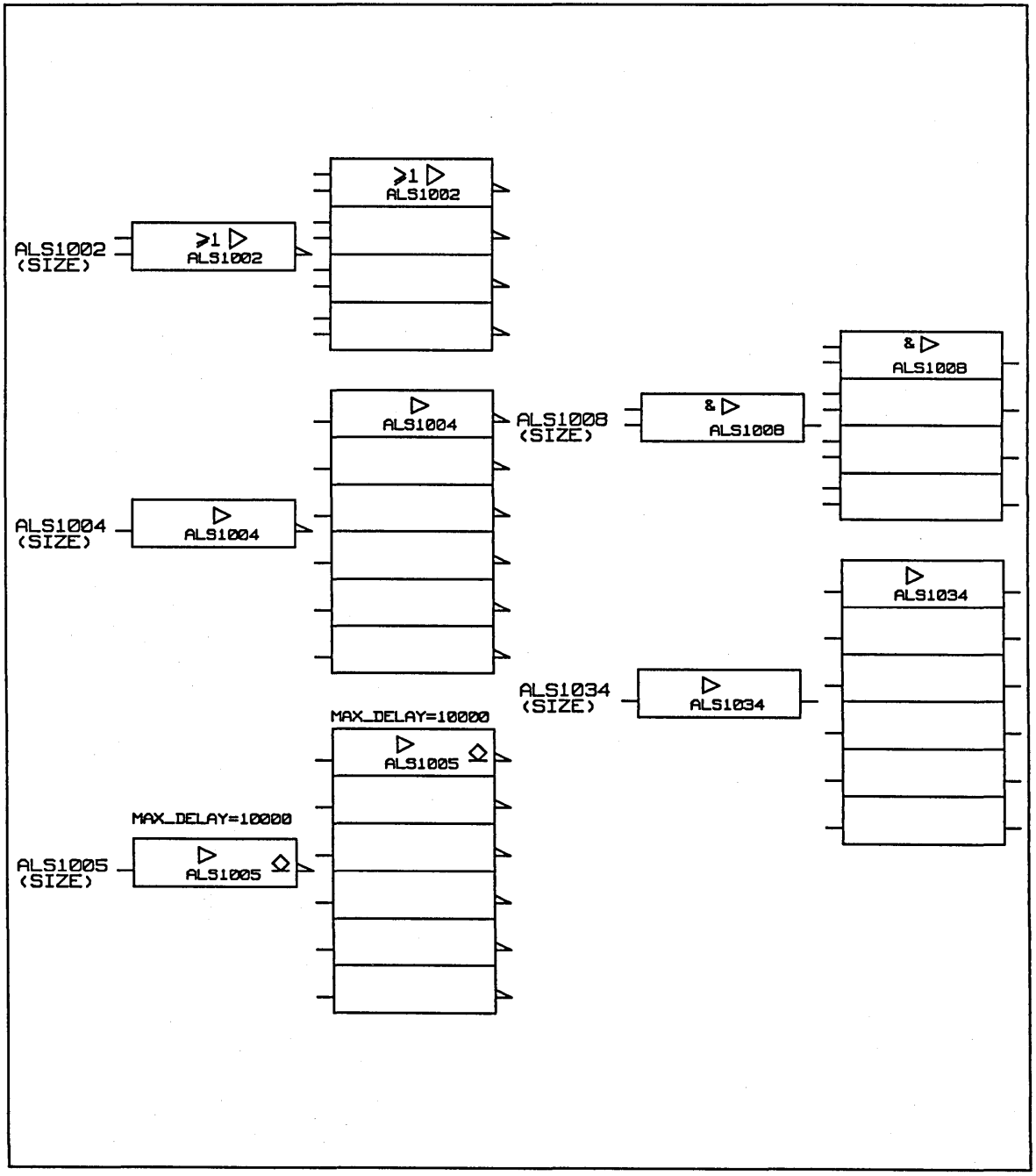

DMUX
N10
&
EN
ALS538
2
0
G0
G7
ALS538
7,10
6,10
5,10
4,10
3,10
2,10
1,10
0,10
EN
C1
ALS563
1D
ALS563
(SIZE)
ALS540
ALS540
(SIZE)
ALS564
ALS564
(SIZE)
ALS541
ALS541
(SIZE)
ALS569
CTRDIV16
EN10
M1[UP]
M2[DOWN]
CS/1,4,7,8+/2,4,7,8-
Z6
6,7,8,9
G7
G8
1,7(CT=15)G9
5CT=0
2,7(CT=0)G9
M3[LOAD]
M4[COUNT]
CT=0
3,5D
10

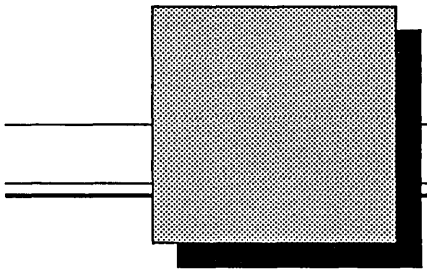

EN
C1
ALS573
1D
ALS573
(SIZE)
ALS576
(SIZE)
ALS576
ALS574
(SIZE)
ALS580
(SIZE)
ALS580
ALS575
(SIZE)
1R
ALS575
ALS623
(SIZE)
EN1
EN2
ALS623
1
2


G3
3EN1[BA]
3EN2[AB]
ALS640
ALS640
(SIZE)
ALS648
(SIZE)
ALS648
G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
ALS648
ALS645
ALS645
(SIZE)
ALS651
(SIZE)
EN1[BA]
EN2[AB]
ALS651


ALS652
(SIZE)
EN1[BA]
EN2[AB]
C4
G5
C6
G7
ALS652
ALS688
COMP
G1
P
Q
1P=Q
ALS688
[ADDRESS COMP]
ALS677
EN
Z16
Z15
Z14
Z13
Z12
Z11
Z10
Z9
Z8
Z7
Z6
Z5
Z4
Z3
Z2
Z1
ALS804
(SIZE)
ALS804
ALS805
(SIZE)
ALS805


ALS808
(SIZE)
&
ALS808
ALS808
ALS874
(SIZE)
EN
C1
R
ALS874
1D
ALS874
ALS878
(SIZE)
EN
C1
1R
ALS878
1D
ALS878
ALS857
MUX
ALS857
ALS990
(SIZE)
EN2
C1
ALS990
1D
2
ALS873
(SIZE)
EN
C1
R
ALS873
1D
ALS873
ALS1000
(SIZE)
&
ALS1000
ALS1000


≥1
ALS1002
ALS1002
(SIZE)
≥1
ALS1002
ALS1004
ALS1004
(SIZE)
ALS1004
&
ALS1008
ALS1008
(SIZE)
&
ALS1008
ALS1034
ALS1034
(SIZE)
ALS1034
MAX_DELAY=10000
ALS1005
MAX_DELAY=10000
ALS1005
(SIZE)
ALS1005



The HCMOS and ANSI HCMOS Libraries

The HCMOS Library requires approximately 5436 Kbytes of disk storage, and the ANSI HCMOS Library requires approximately 5287 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*hcmos.lib* or *a74hcmos.lib*).

The specifications used to construct the models in these libraries were taken from the Motorola data books.

The release level of the HCMOS and ANSI HCMOS Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 141 components:

HC00	Quad 2-input NAND
HC02	Quad 2-input NOR
HC03	Quad 2-input open-collector NAND
HC04	Hex inverter
HC08	Quad 2-input AND
HC10	Triple 3-input NAND
HC11	Triple 3-input AND
HC14	Hex Schmitt-trigger inverter
HC20	Dual 4-input NAND
HC27	Triple 3-input NOR
HC30	8-input NAND
HC32	Quad 2-input OR
HC42	4-to-10-line decoder
HC51	2-wide 3-input, 2-wide 2-input AND-OR-invert
HC58	2-wide 3-input, 2-wide 2-input AND-OR
HC73	Dual JK flip-flop with clear
HC74	Dual positive-edge-triggered D flip-flop
HC75	4-bit bistable latch
HC76	Dual JK flip-flop with preset and clear
HC85	4-bit magnitude comparator
HC86	Quad 2-input exclusive-OR
HC107	Dual JK negative-edge-triggered flip-flop
HC109	Dual JKbar positive-edge-triggered flip-flop
HC112	Dual JK negative-edge-triggered flip-flop
HC113	Dual JK negative-edge-triggered flip-flop

HC123	Dual retriggerable monostable multivibrators with clear
HC125	Quad bus buffer with three-state output
HC126	Quad bus buffer with three-state output
HC132	Quad 2-input positive-NAND Schmitt triggers
HC133	13-input NAND
HC137	3-to-8 line decoder/demultiplexer with address latch
HC138	3-to-8 line decoder/demultiplexer
HC139	Dual 2-to-4 line decoder/multiplexer
HC147	10-line decimal to 4-line BCD priority encoder
HC151	1-of-8 data selector/multiplexer
HC153	Dual 4-line to 1-line data multiplexer
HC154	4-to-16 line decoder/demultiplexer
HC157	Quad 2-to-1-line non-inverting multiplexer
HC158	Quad 2-to-1-line inverting data multiplexer
HC160	4-bit synchronous decade counters with direct clear
HC161	4-bit synchronous binary counters with direct clear
HC162	4-bit synchronous decade counters with synchronous clear
HC163	4-bit synchronous binary counters with synchronous clear
HC164	8-bit parallel output serial shift register
HC165	8-bit serial output shift register

HC166	8-bit shift register
HC173	Quad D-type flip-flop
HC174	Hex D-type flip-flop
HC175	Quad D-type flip-flop
HC180	9-bit parity generator/checker
HC182	Look-ahead carry generators
HC190	Synchronous BCD up/down counter
HC191	Synchronous binary up/down counter
HC192	Synchronous BCD up/down counter
HC193	Synchronous binary up/down dual clock counters
HC194	4-bit bidirectional shift register
HC195	4-bit universal shift register
HC221	Dual non-retriggerable monostable multivibrator
HC237	3-to-8 line decoder/demultiplexer with address latch
HC240	Octal inverting 3-state bus transceiver
HC241	Octal non-inverting 3-state bus transceiver
HC242	Quad inverting 3-state bus transceiver
HC243	Quad non-inverting 3-state bus transceiver
HC244	Octal non-inverting 3-state bus transceiver
HC245	Octal non-inverting 3-state bus transceiver
HC251	3-state data multiplexer
HC253	Dual data selector/multiplexer
HC259	8-bit addressable latches
HC266	Quad 2-input exclusive-NOR gate
HC257	Quad 3-state non-inverting data multiplexer

HC273	Octal D-type flip-flop
HC280	9-bit odd/even parity generators/checker
HC283	4-bit binary full adders
HC292	Programmable frequency divider/digital timer
HC294	Programmable frequency divider/digital timer
HC298	Quad 2-input multiplexers with storage
HC299	8-bit bidirectional 3-state shift/storage register
HC354	1-of-8 data selector/multiplexer with data and address latches and 3-state output
HC356	1-of-8 data selector/multiplexer with data and address latches and 3-state output
HC365	Hex non-inverted 3-state bus drivers
HC366	Hex inverted 3-state bus drivers
HC367	Hex bus driver
HC368	Hex bus driver
HC373	Octal 3-state D-latch with common enable
HC374	Octal 3-state positive-edge-triggered D register
HC390	Dual 4-stage binary ripple counter
HC393	Dual 4-stage binary ripple counter
HC423	Dual retriggerable monostable multivibrators
HC533	8-bit latch with inverting outputs
HC534	8-bit register with inverting outputs
HC540	Octal buffers and line drivers with 3-state outputs
HC541	Octal buffers and line drivers with 3-state outputs
HC563	8-bit latch with inverting 3-state outputs
HC564	8-bit register with inverting 3-state outputs
HC573	Octal latch with three-state output

HC574	Octal D-type flip-flop with three-state output
HC590	8-bit binary counter/three state latch
HC595	8-bit serial-input/serial- or parallel-output shift register with latched 3-state output
HC597	8-bit serial- or parallel-input/serial-output shift register with input latch
HC640	Octal 3-state inverting bus transceiver
HC643	Octal 3-state inverting and non-inverting bus transceiver
HC646	Octal 3-state non-inverting bus transceiver and D-type flip-flop
HC648	Octal 3-state inverting bus transceiver and D-type flip-flop
HC688	8-bit equality comparator
HC4002	Dual 4-input NOR
HC4016	Quad analog switch/multiplexer/demultiplexer
HC4017	Decade counter/divider
HC4020	14-bit binary counter
HC4024	7-bit binary counter
HC4040	12-bit binary counter
HC4049	Hex inverting buffer/logic-level down converter
HC4050	Hex non-inverting buffer/logic-level down converter
HC4051	8-channel analog multiplexer/demultiplexer
HC4052	Dual 4-channel analog multiplexer/demultiplexer
HC4053	Triple 2-channel analog multiplexer/demultiplexer

HC4066	Quad analog switch/multiplexer/demultiplexer with enhanced on-resistance linearity
HC4075	Triple 3-input OR
HC4078	8-input NOR/OR
HC4316	Quad analog switch/multiplexer/demultiplexer with separate analog and digital power supplies
HC4351	8-channel analog multiplexer/demultiplexer with address latch
HC4352	Dual 4-channel analog multiplexer/demultiplexer with address latch
HC4353	Triple 2-channel analog multiplexer/demultiplexer with address latch
HC4514	4-to-16 line decoder/demultiplexer with address latch
HC4538	Dual monostable multivibrator
HCT00	Quad 2-input NAND gate
HCT02	Quad 2-input NOR gate
HCT04	Hex inverter
HCT32	Quad 2-input OR gate
HCT138	3-to-8 line decoder/demultiplexer
HCT240	Octal inverting 3-state bus transceiver
HCT241	Octal non-inverting 3-state bus transceiver
HCT244	Octal non-inverting 3-state bus transceiver
HCT245	Octal three state bus transceiver
HCT280	9-bit odd/even parity generators/checker
HCT373	Octal 3-state D-latch with common enable

HCT374	Octal 3-state positive-edge-triggered D register
HCT640	Octal 3-state inverting bus transceiver
HCT643	Octal 3-state inverting and non-inverting
HCT688	8-bit equality comparator
HCT670	4x4 register file/3-state output
HCU04	Hex inverter

Application Notes

Monostable Multivibrators

The 74HC123, 74HC423, 74HC221, and 74HC4538 models fully support the simulation and timing behavior of retrigerrable and non-retriggerable multivibrators which are resettable at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

  ```
  LATCH_ERR_MODEL CLOSED;
  ```

- The first trigger edge must occur after 'PULSE_WIDTH' ns.

- The maximum trigger frequency is

  ```
  2 * RETRIG_DIV2 -1
  ```

  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6-1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.

Capacitive Loading Effects

The delay calculations for the timing and simulation models are based on values from the *Motorola High-Speed CMOS Logic Data* book (1983). The delay times are calculated using the short circuit current method with a Vcc of 4.5 volts and a temperature of 25°C (see page 4-12 of the data book). The typical drive is therefore:

0.5 * 4.5 / 17.3 (mA) = 0.13

The typical and maximum delays for the individual components in the data book are given with a capacitive load of 50pF. Using these values, the typical no-load delay is calculated from the equation:

typ_delay (no load) = *typ_delay* (50pF) - 0.13 * 50

Assuming that the ratio of maximum no-load delay to maximum delay (50pF) is the same as typical no-load delay to typical delay (50pF), the maximum no-load delay is:

typ_delay (no load) * *max_delay* (50pF) / *typ_delay* (5(

The minimum delay for timing and simulation models is one-half of typical or one-third of maximum; the minimum drive is calculated from:

min_delay (50pF) - *min_delay* (no load) / 50

The following examples show the delay and drive calculations for a HC00 and an HC74.

HC00 Data Book:

typical delay (50pF) = 9
maximum delay (50pF) = 18
typical drive = 0.13

HC00 Calculation:

typical delay (no load) = 9 – 0.13 * 50 = 2.5
maximum delay (no load) = 2.5 * 18 / 9 = 5.0
minimum delay (50pF) = 9 / 2 = 4.5
minimum delay (no load) = 2.5 / 2 = 1.25
maximum drive = (18 – 5) / 50pF = 0.26
minimum drive = (4.5 – 1.25) / 50pF = 0.065

From these calculations, the min/max delay for the HC00 timing model is 1.25/5.0, and the min/max drive for the timing model is 0.065/0.26. The min/typ/max delay for the HC00 simulation model is 1.25/2.5/5.0, and the min/typ/max drive for the simulation model is 0.065/0.13/0.26.

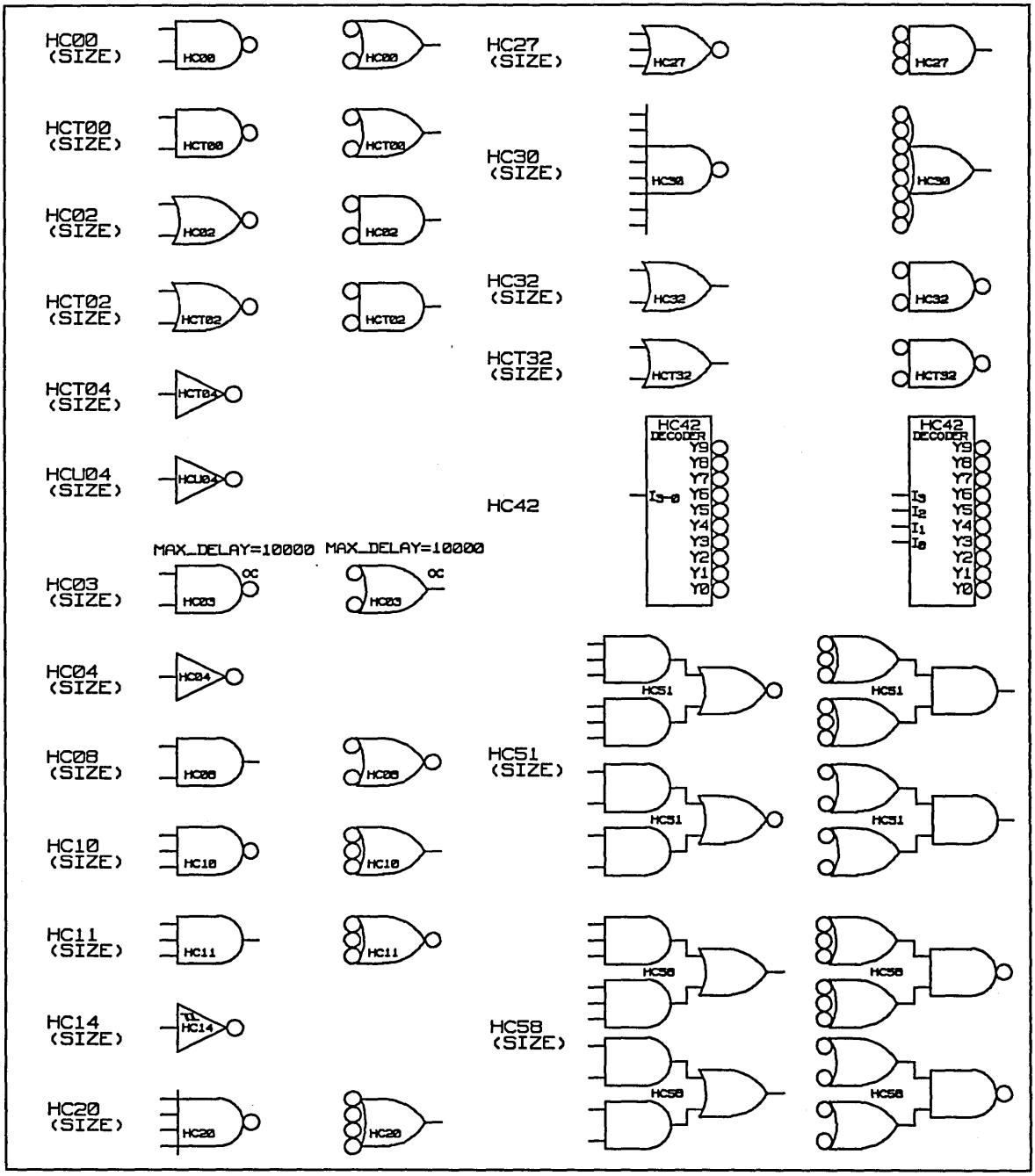
HC74 Data Book (from CLK to Q or Q*):

typical delay (50pF) = 18
maximum delay (50pF) = 35
typical drive = 0.13

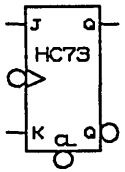
HC74 Calculation:

typical delay (no load) = 18 – 0.13 * 50 = 11.5
maximum delay (no load) = 11.5 * 35 / 18 = 22.36
minimum delay (50pF) = 18 / 2 = 9.0
minimum delay (no load) = 11.5 / 2 = 5.75
maximum drive = (35 – 22.36) / 50pF = 0.253
minimum drive = (9.0 – 5.75) / 50pF = 0.065

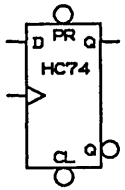
From these calculations, the min/max delay for the HC74 timing model is 5.75/22.36, and the min/max drive for the timing model is 0.065/0.253. The min/typ/max delay for the HC74 simulation model is 5.75/11.5/22.36, and the min/typ/max drive for the simulation model is 0.065/0.13/0.253.


HC00 (SIZE)
HCT00 (SIZE)
HC02 (SIZE)
HCT02 (SIZE)
HCT04 (SIZE)
HCU04 (SIZE)
MAX_DELAY=10000
MAX_DELAY=10000
HC03 (SIZE)
HC04 (SIZE)
HC08 (SIZE)
HC10 (SIZE)
HC11 (SIZE)
HC14 (SIZE)
HC20 (SIZE)
HC27 (SIZE)
HC30 (SIZE)
HC32 (SIZE)
HCT32 (SIZE)
HC42
HC42 DECODER
I3-0
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
I3
I2
I1
I0
HC51 (SIZE)
HC58 (SIZE)

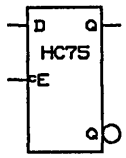
HC73
(SIZE)



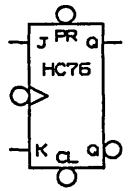
HC74
(SIZE)



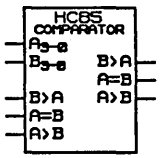
HC75
(SIZE)

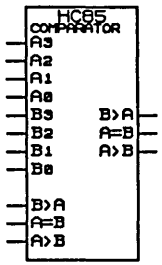


HC76
(SIZE)



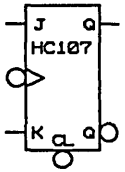
HC85



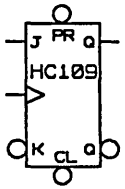


HC86
(SIZE)

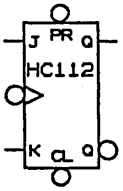
HC107
(SIZE)



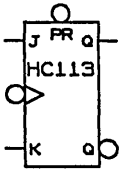
HC109
(SIZE)



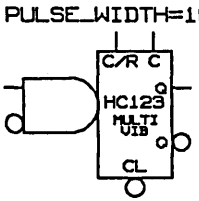
HC112
(SIZE)



HC113
(SIZE)

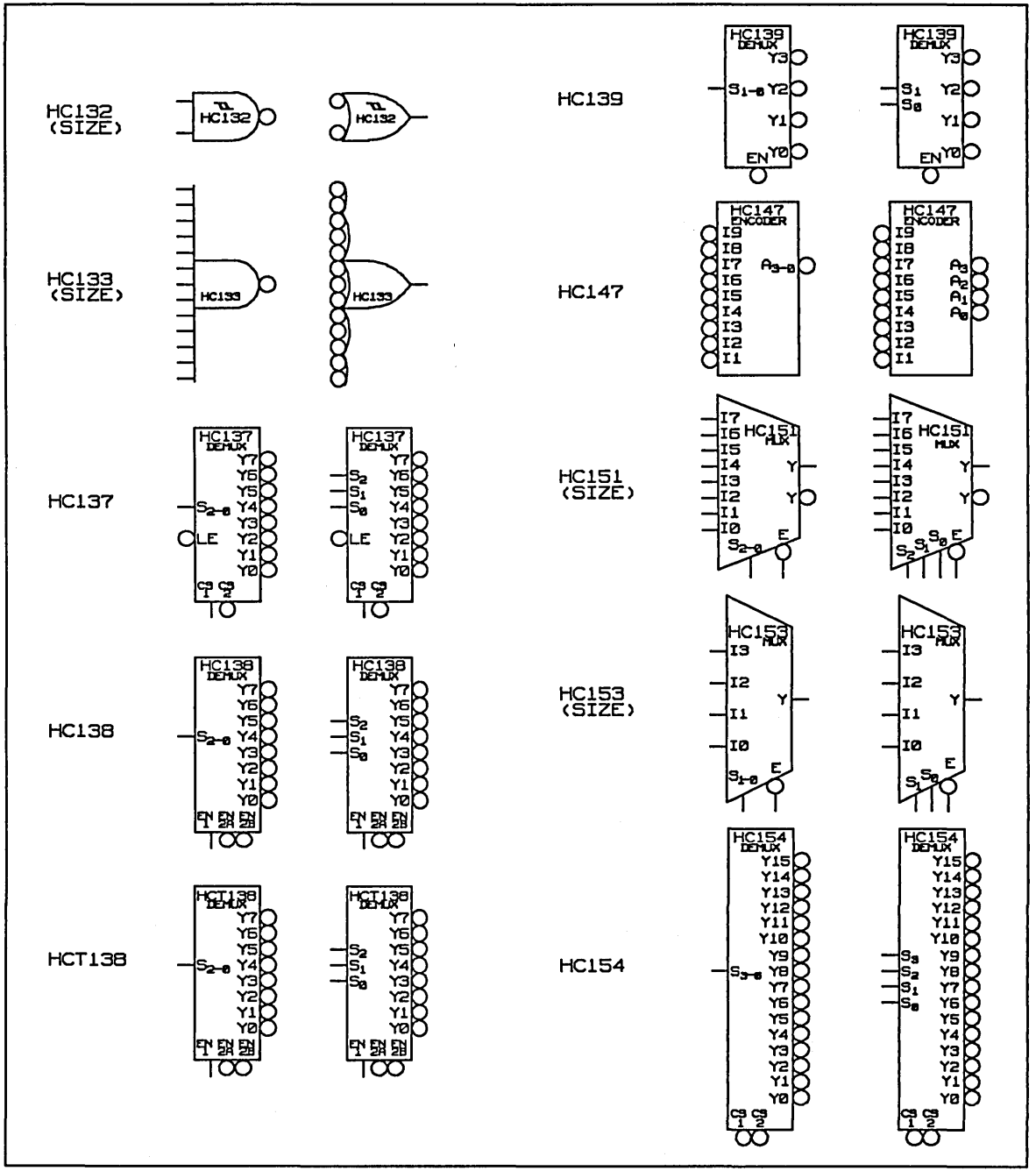


HC123

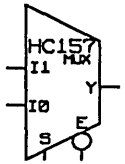


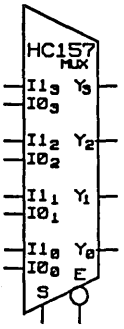
HC125
(SIZE)

HC126
(SIZE)

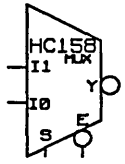

HC132
(SIZE)
HC132
HC132
HC133
(SIZE)
HC133
HC133
HC137
HC137
DEMUX
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
S2-0
LE
G1
G2
HC138
HC138
DEMUX
S2
S1
S0
EN1
EN2A
EN2B
HCT138
HCT138
HC139
HC139
DEMUX
Y3
Y2
Y1
Y0
S1-0
EN
S1
S0
HC147
HC147
ENCODER
I9
I8
I7
I6
I5
I4
I3
I2
I1
A3-0
A3
A2
A1
A0
HC151
(SIZE)
HC151
MUX
I7
I6
I5
I4
I3
I2
I1
I0
Y
E
S2-0
S2
S1
S0
HC153
(SIZE)
HC153
MUX
I3
I2
I1
I0
Y
E
S1-0
S1
S0
HC154
HC154
DEMUX
Y15
Y14
Y13
Y12
Y11
Y10
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
S3-0
S3
S2
S1
S0
G1
G2

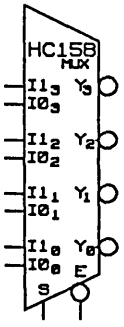
HC157 (SIZE)



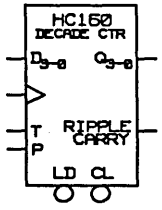


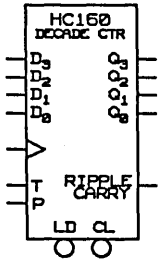
HC158 (SIZE)



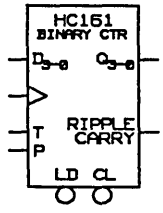


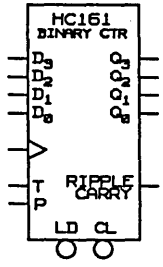
HC160



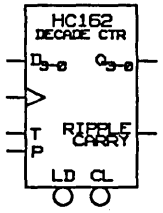


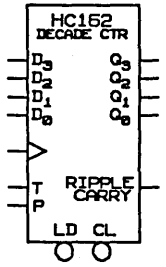
HC161



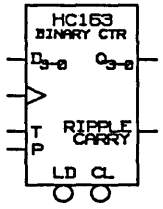


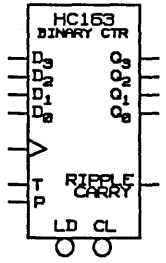
HC162



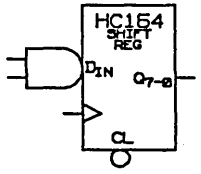


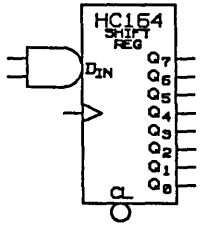
HC163



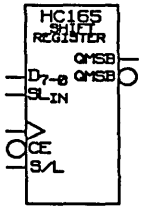


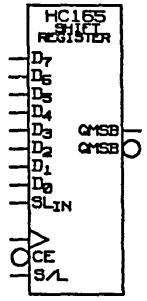
HC164

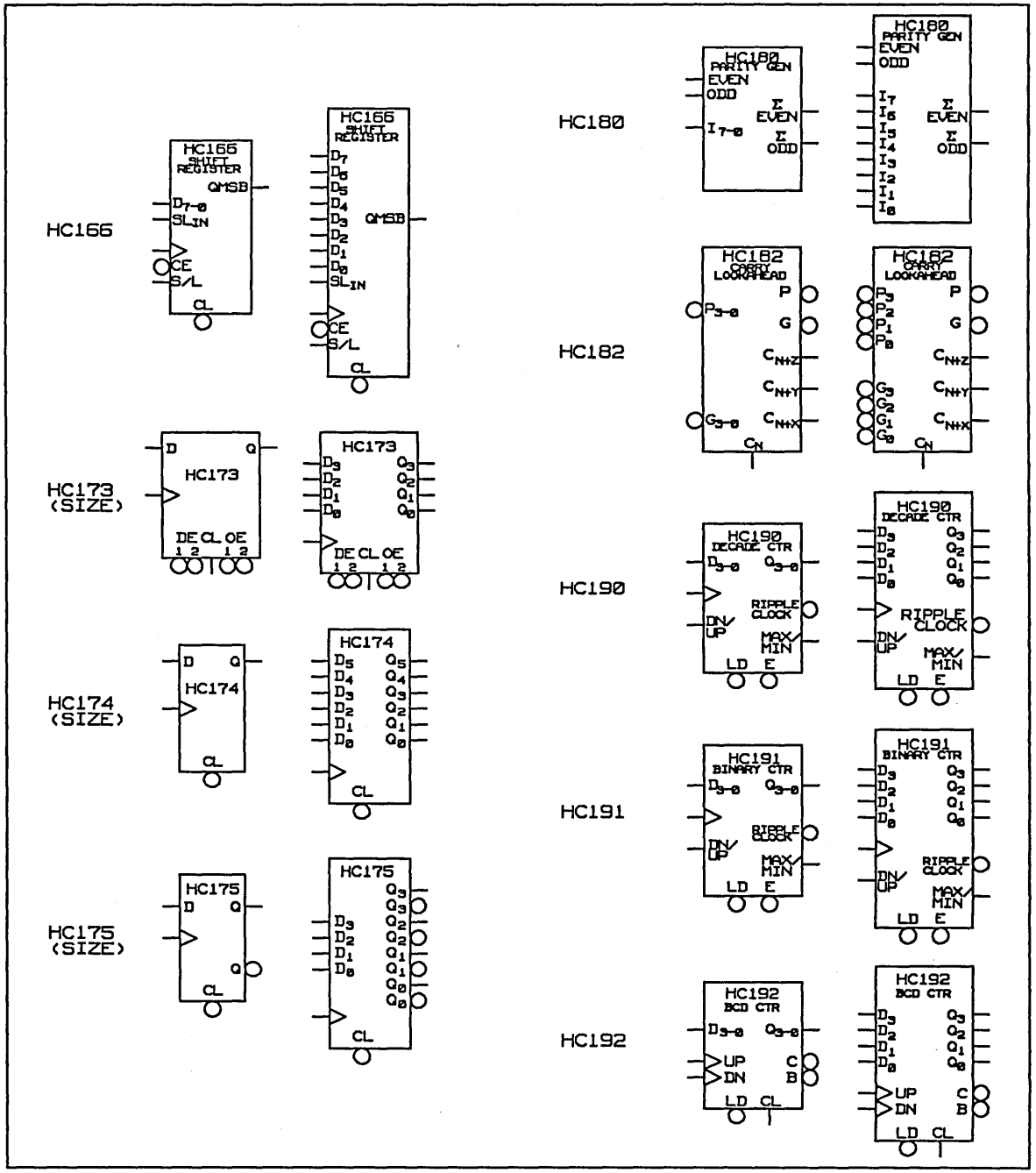


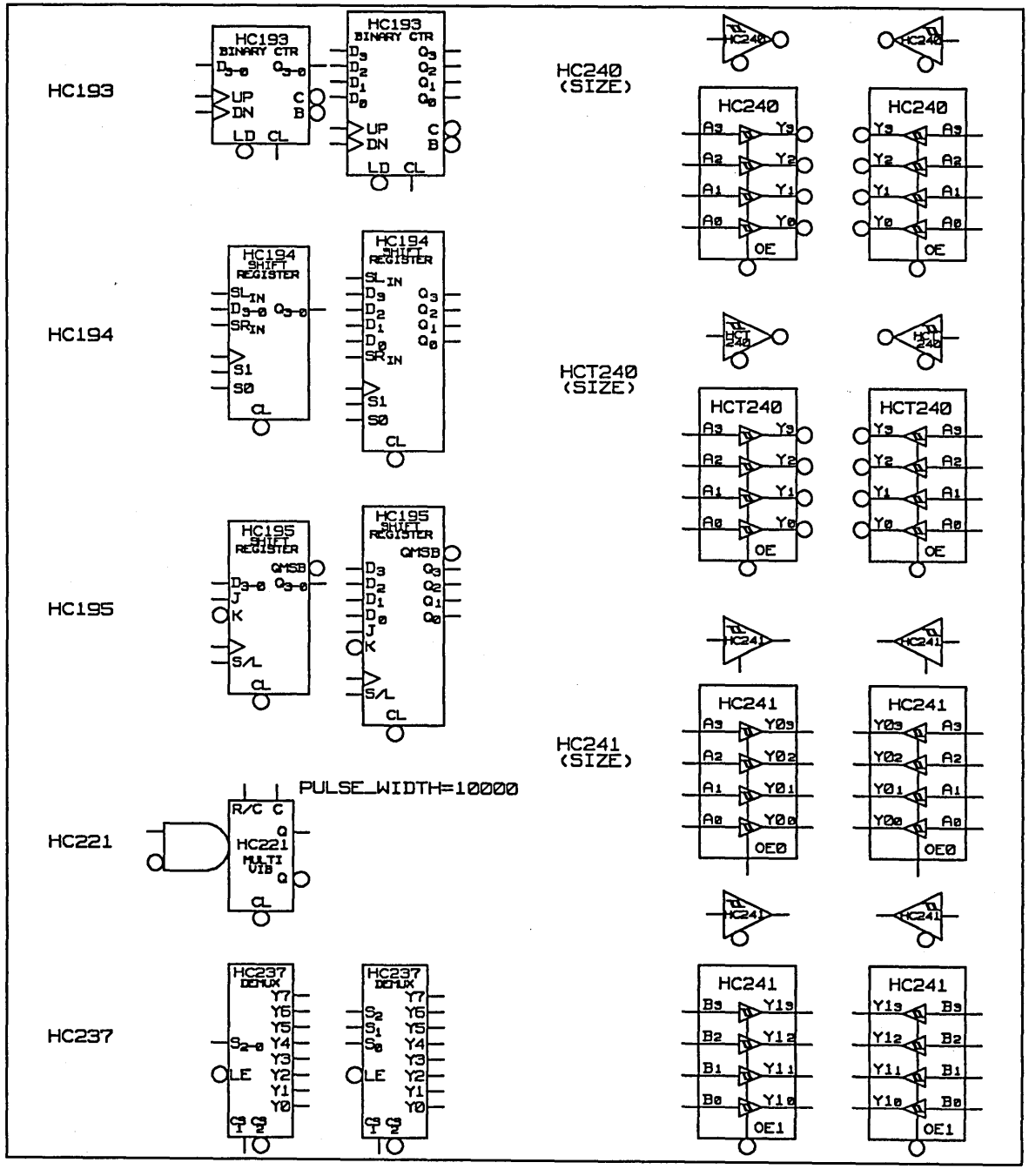


HC165

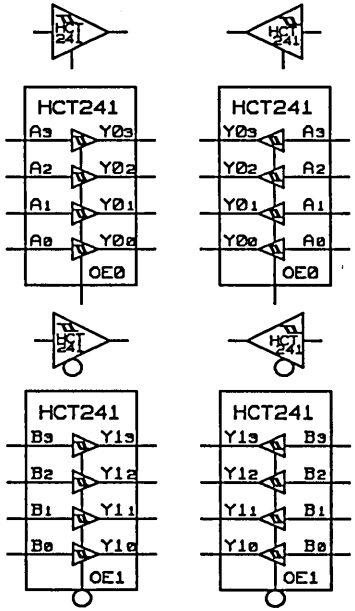




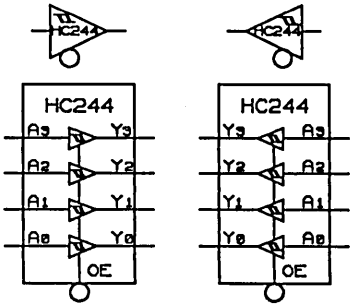

HC166
HC166
SHIFT REGISTER
QMSB
D7-0
SLIN
CE
S/L
CL
HC166
SHIFT REGISTER
D7
D6
D5
D4
D3
D2
D1
D0
QMSB
SLIN
CE
S/L
CL
HC173
(SIZE)
D
Q
HC173
DE CL OE
1 2 1 2
HC173
D3
D2
D1
D0
Q3
Q2
Q1
Q0
DE CL OE
1 2 1 2
HC174
(SIZE)
D
Q
HC174
CL
HC174
D5
D4
D3
D2
D1
D0
Q5
Q4
Q3
Q2
Q1
Q0
CL
HC175
(SIZE)
HC175
D
Q
Q
CL
HC175
D3
D2
D1
D0
Q3
Q3
Q2
Q2
Q1
Q1
Q0
Q0
CL
HC180
HC180
PARITY GEN
EVEN
ODD
I7-0
Σ EVEN
Σ ODD
HC180
PARITY GEN
EVEN
ODD
I7
I6
I5
I4
I3
I2
I1
I0
Σ EVEN
Σ ODD
HC182
HC182
CARRY LOOKAHEAD
P3-0
G3-0
P
G
CN+Z
CN+Y
CN+X
CN
HC182
CARRY LOOKAHEAD
P3
P2
P1
P0
G3
G2
G1
G0
P
G
CN+Z
CN+Y
CN+X
CN
HC190
HC190
DECADE CTR
D3-0
Q3-0
RIPPLE CLOCK
DN
UP
MAX MIN
LD
E
HC190
DECADE CTR
D3
D2
D1
D0
Q3
Q2
Q1
Q0
RIPPLE CLOCK
DN
UP
MAX MIN
LD
E
HC191
HC191
BINARY CTR
D3-0
Q3-0
RIPPLE CLOCK
DN
UP
MAX MIN
LD
E
HC191
BINARY CTR
D3
D2
D1
D0
Q3
Q2
Q1
Q0
RIPPLE CLOCK
DN
UP
MAX MIN
LD
E
HC192
HC192
BCD CTR
D3-0
Q3-0
UP
DN
C
B
LD
CL
HC192
BCD CTR
D3
D2
D1
D0
Q3
Q2
Q1
Q0
UP
DN
C
B
LD
CL


HC193
HC193
BINARY CTR
UP
DN
LD
CL
HC194
HC194
SHIFT REGISTER
SL_IN
SR_IN
S1
S0
CL
HC195
HC195
SHIFT REGISTER
QMSB
J
K
S/L
CL
HC221
HC221
MULTI VIB
R/C
C
Q
CL
PULSE_WIDTH=10000
HC237
HC237
DEMUX
LE
HC240
(SIZE)
HC240
OE
HCT240
(SIZE)
HCT240
OE
HC241
(SIZE)
HC241
OE0
OE1

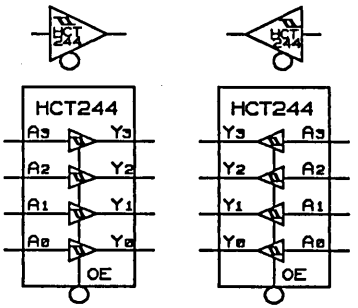
HCT241 (SIZE)



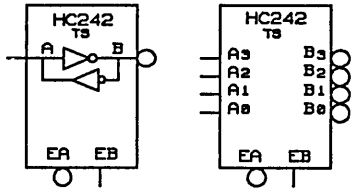
HC244 (SIZE)



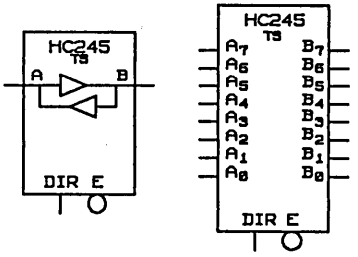
HCT244 (SIZE)



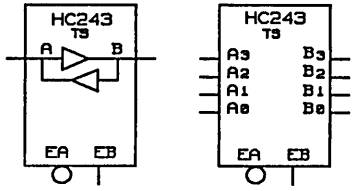
HC242 (SIZE)



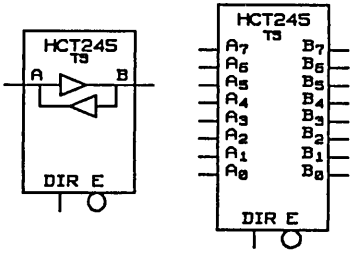
HC245 (SIZE)



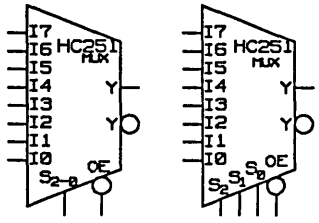
HC243 (SIZE)



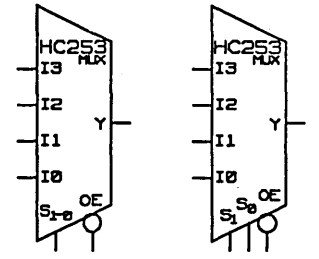
HCT245 (SIZE)



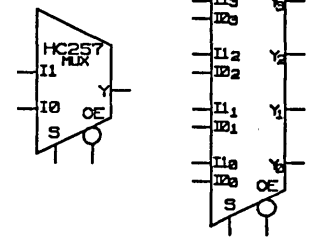
HC251 (SIZE)



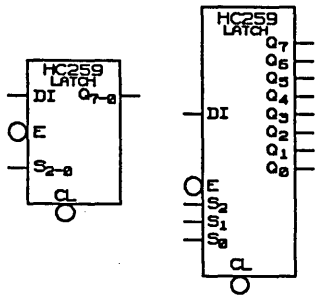
HC253 (SIZE)



HC257 (SIZE)

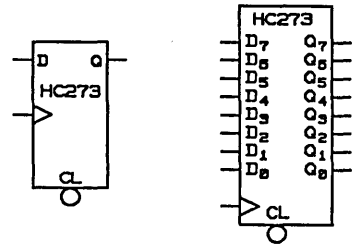


HC259

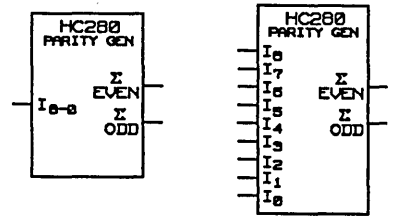


HC266 (SIZE)

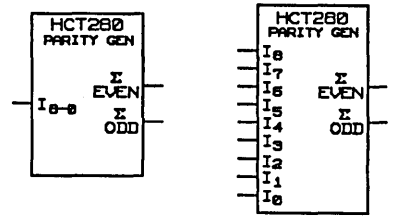
HC273 (SIZE)



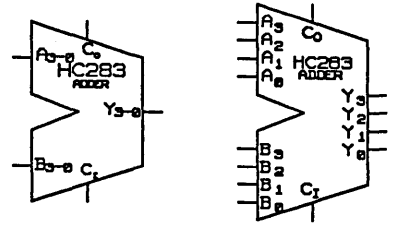
HC280



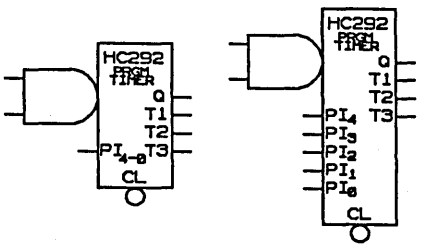
HCT280

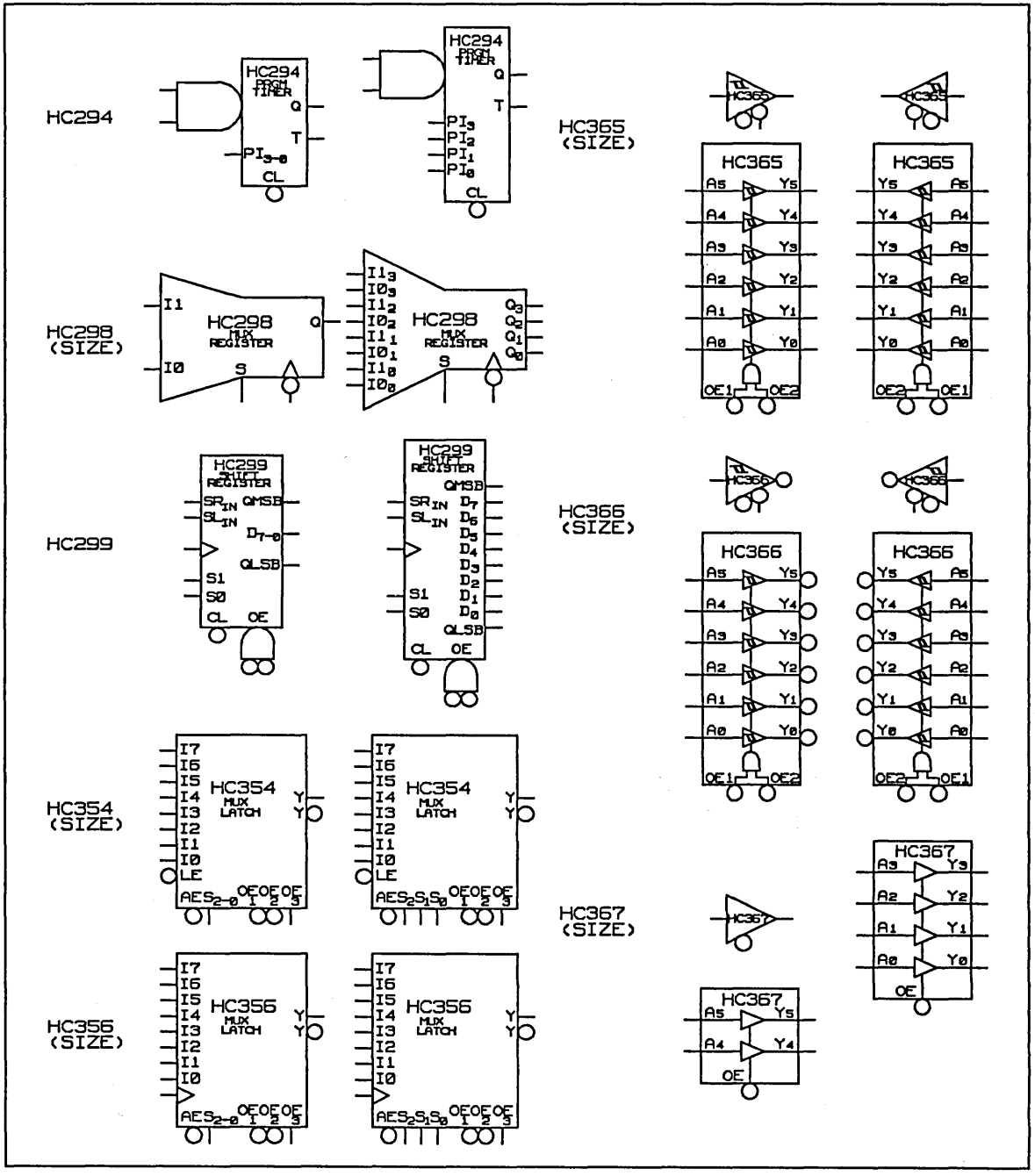


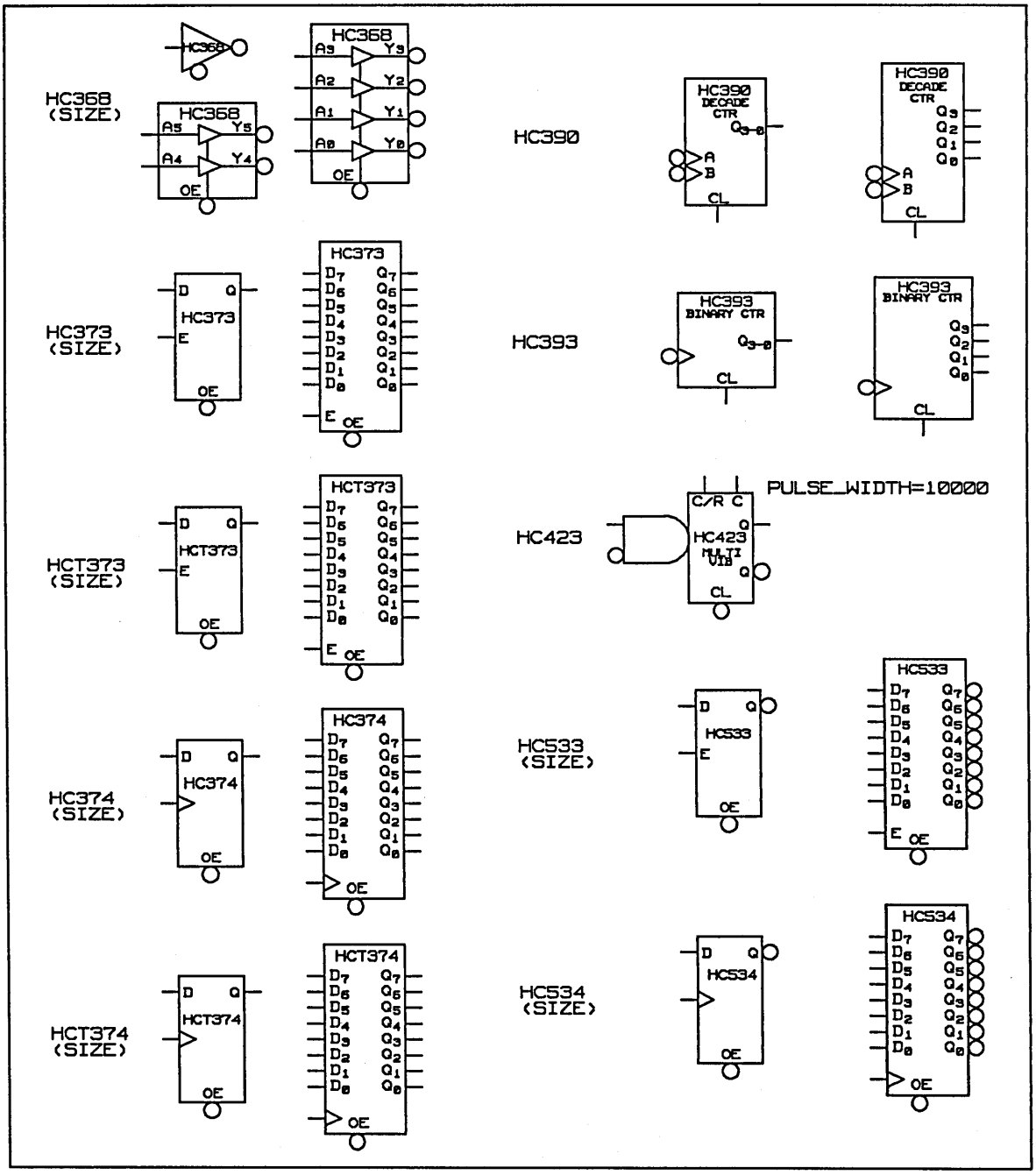
HC283

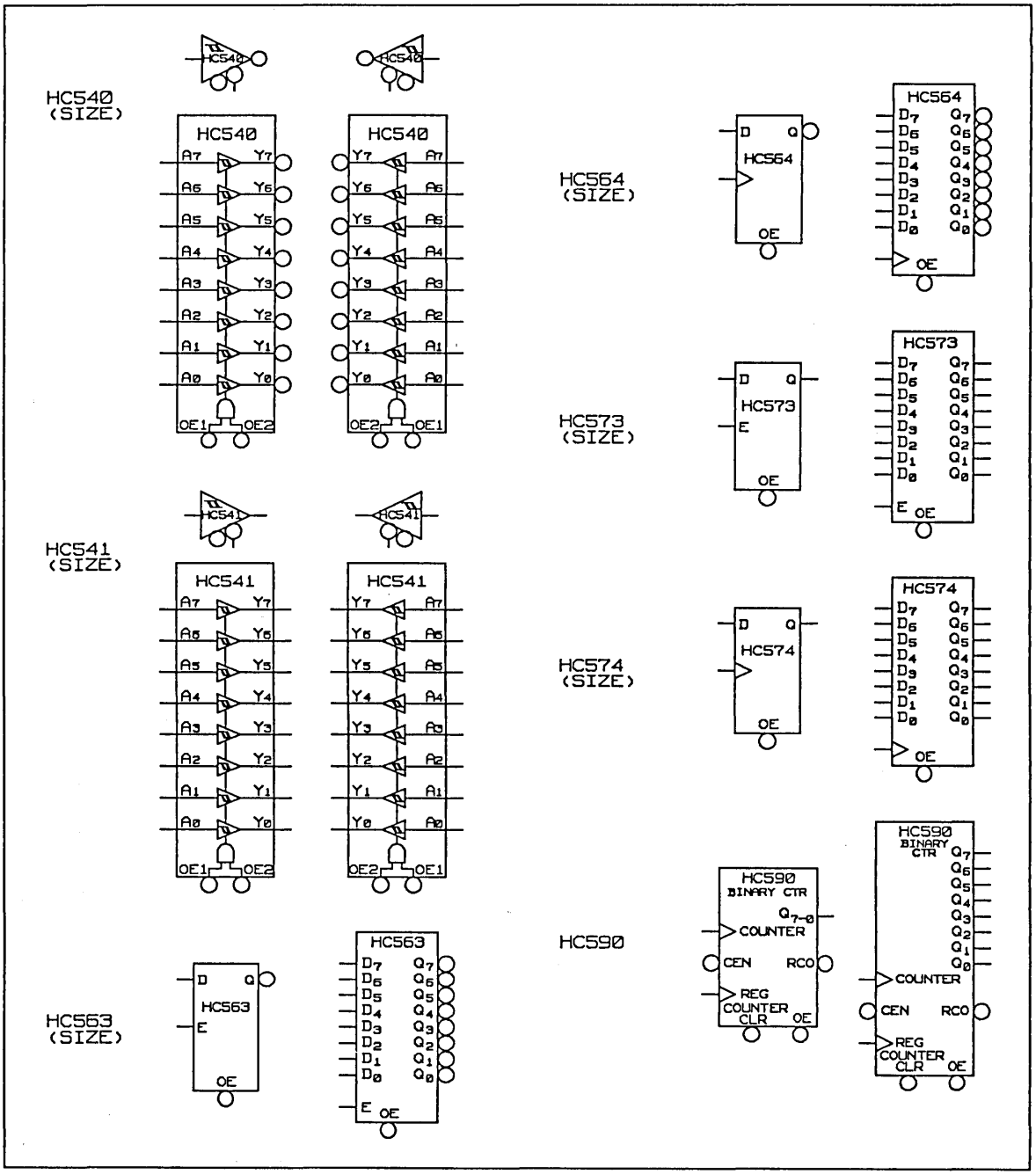


HC292

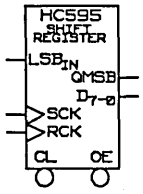


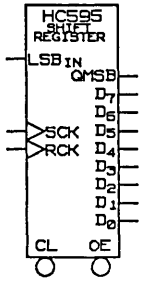

HC294
HC294
PRGM TIMER
Q
T
PI3-0
CL
HC294
PRGM TIMER
Q
T
PI3
PI2
PI1
PI0
CL
HC298 (SIZE)
HC298
MUX REGISTER
I1
I0
Q
S
HC298
MUX REGISTER
I13
I03
I12
I02
I11
I01
I10
I00
Q3
Q2
Q1
Q0
S
HC299
HC299
SHIFT REGISTER
SRIN
SLIN
QMSB
D7-0
QLSB
S1
S0
CL
OE
HC299
SHIFT REGISTER
SRIN
SLIN
QMSB
D7
D6
D5
D4
D3
D2
D1
D0
QLSB
S1
S0
CL
OE
HC354 (SIZE)
HC354
MUX LATCH
I7
I6
I5
I4
I3
I2
I1
I0
LE
Y
AES2-0
OE1
OE2
OE3
HC354
MUX LATCH
I7
I6
I5
I4
I3
I2
I1
I0
LE
Y
AES2S1S0
OE1
OE2
OE3
HC356 (SIZE)
HC356
MUX LATCH
I7
I6
I5
I4
I3
I2
I1
I0
Y
AES2-0
OE1
OE2
OE3
HC356
MUX LATCH
I7
I6
I5
I4
I3
I2
I1
I0
Y
AES2S1S0
OE1
OE2
OE3
HC365 (SIZE)
HC365
HC365
HC365
HC365
A5
A4
A3
A2
A1
A0
Y5
Y4
Y3
Y2
Y1
Y0
OE1
OE2
HC366 (SIZE)
HC366
HC366
HC366
HC366
A5
A4
A3
A2
A1
A0
Y5
Y4
Y3
Y2
Y1
Y0
OE1
OE2
HC367 (SIZE)
HC367
HC367
A3
A2
A1
A0
Y3
Y2
Y1
Y0
OE
HC367
A5
A4
Y5
Y4
OE


HC368
(SIZE)
HC368
A5
Y5
A4
Y4
OE
HC368
A3
Y3
A2
Y2
A1
Y1
A0
Y0
OE
HC373
(SIZE)
D
Q
HC373
E
OE
HC373
D7
D6
D5
D4
D3
D2
D1
D0
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
E
OE
HCT373
(SIZE)
HCT373
HCT373
HC374
(SIZE)
HC374
HC374
HCT374
(SIZE)
HCT374
HCT374
HC390
HC390
DECADE
CTR
Q3-0
A
B
CL
HC393
HC393
BINARY CTR
HC423
C/R
C
HC423
MULTI
VIB
PULSE_WIDTH=10000
HC533
(SIZE)
HC533
HC533
HC534
(SIZE)
HC534
HC534

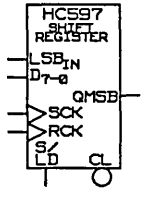

HC540
(SIZE)
HC540
A7 Y7
A6 Y6
A5 Y5
A4 Y4
A3 Y3
A2 Y2
A1 Y1
A0 Y0
OE1 OE2
HC540
Y7 A7
Y6 A6
Y5 A5
Y4 A4
Y3 A3
Y2 A2
Y1 A1
Y0 A0
OE2 OE1
HC541
(SIZE)
HC541
A7 Y7
A6 Y6
A5 Y5
A4 Y4
A3 Y3
A2 Y2
A1 Y1
A0 Y0
OE1 OE2
HC541
Y7 A7
Y6 A6
Y5 A5
Y4 A4
Y3 A3
Y2 A2
Y1 A1
Y0 A0
OE2 OE1
HC563
(SIZE)
D Q
HC563
E
OE
HC563
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
E OE
HC564
(SIZE)
D Q
HC564
OE
HC564
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
OE
HC573
(SIZE)
D Q
HC573
E
OE
HC573
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
E OE
HC574
(SIZE)
D Q
HC574
OE
HC574
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
OE
HC590
HC590
BINARY CTR
Q7-0
COUNTER
CEN RCO
REG
COUNTER
CLR OE
HC590
BINARY CTR
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
COUNTER
CEN RCO
REG
COUNTER
CLR OE

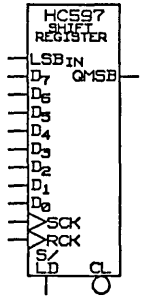
HC595



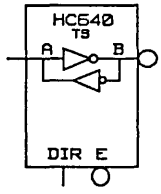


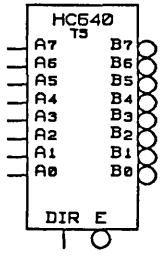
HC597



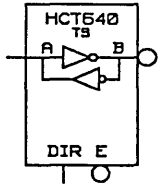


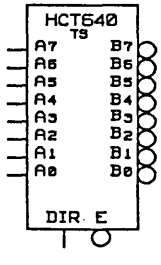
HC640 (SIZE)



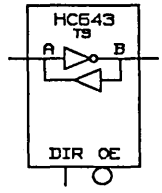


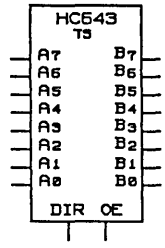
HCT640 (SIZE)



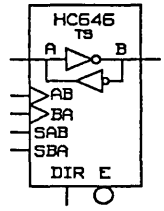


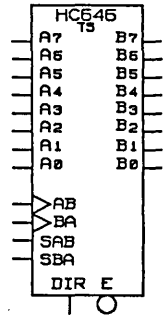
HC643 (SIZE)



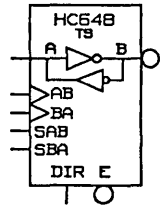


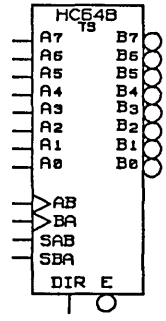
HC646 (SIZE)



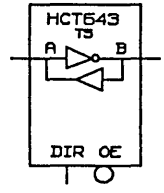


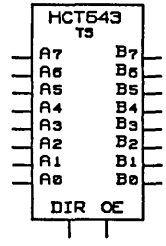
HC648 (SIZE)

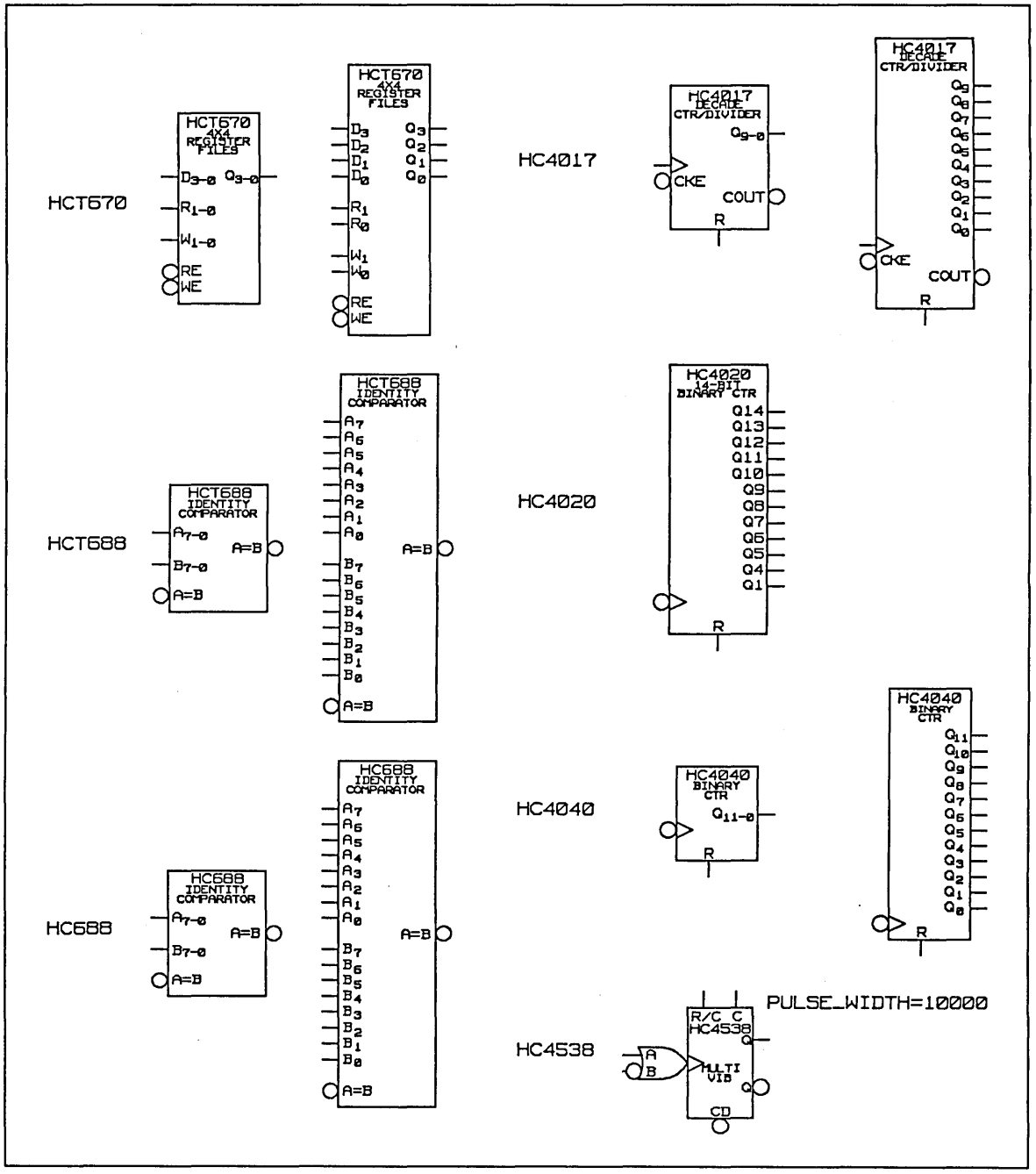


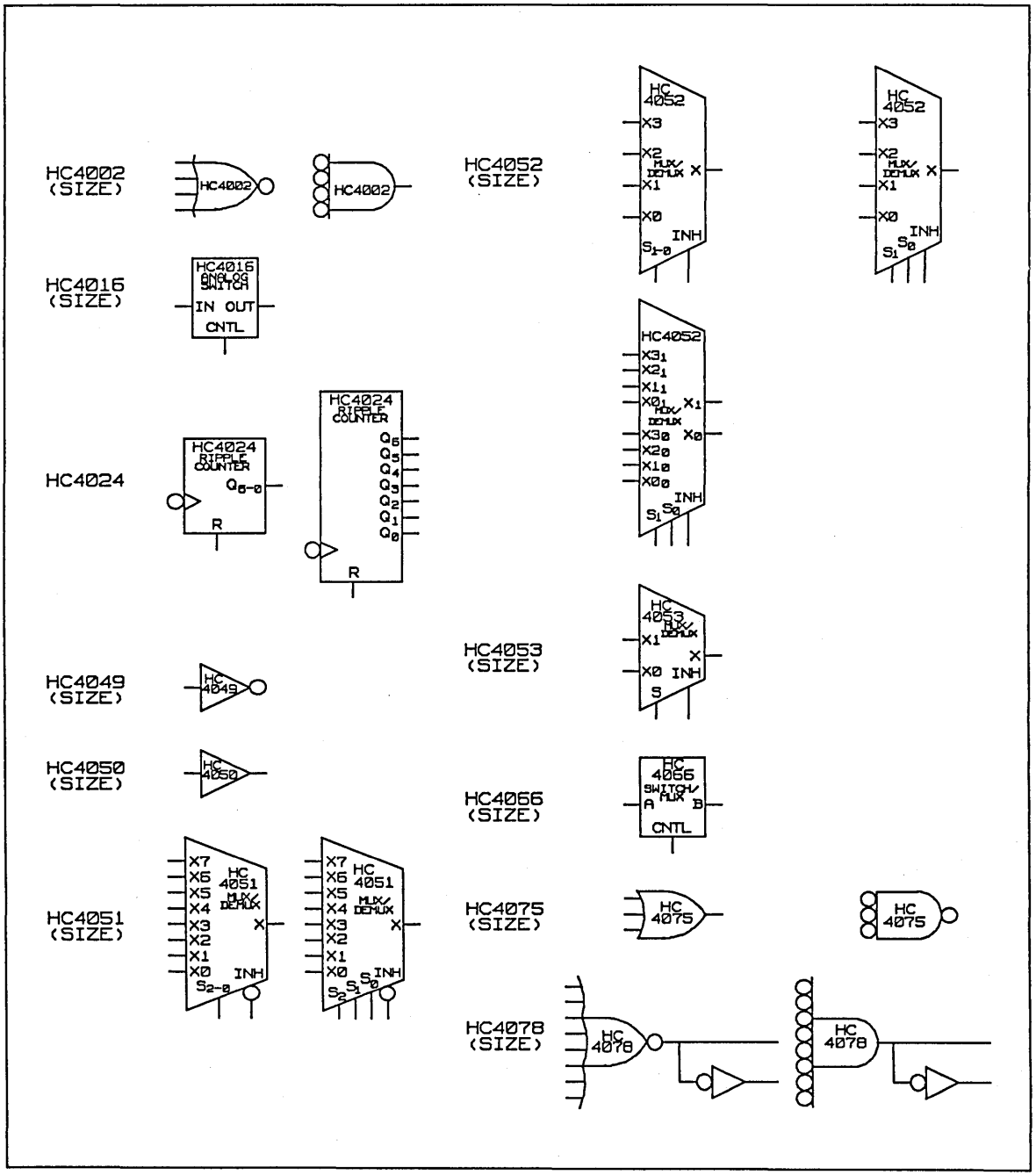


HCT643 (SIZE)



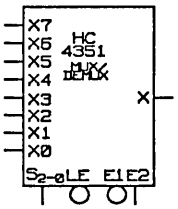


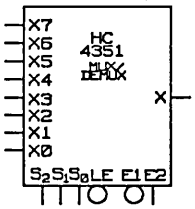

HCT670
HCT670
4X4
REGISTER
FILES
D3-0
Q3-0
R1-0
W1-0
RE
WE
HCT670
4X4
REGISTER
FILES
D3
D2
D1
D0
Q3
Q2
Q1
Q0
R1
R0
W1
W0
RE
WE
HC4017
HC4017
DECADE
CTR/DIVIDER
Q9-0
CKE
COUT
R
HC4017
DECADE
CTR/DIVIDER
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CKE
COUT
R
HCT688
HCT688
IDENTITY
COMPARATOR
A7-0
B7-0
A=B
A=B
HCT688
IDENTITY
COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
A=B
A=B
HC4020
HC4020
14-BIT
BINARY CTR
Q14
Q13
Q12
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q1
R
HC688
HC688
IDENTITY
COMPARATOR
A7-0
B7-0
A=B
A=B
HC688
IDENTITY
COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
A=B
A=B
HC4040
HC4040
BINARY
CTR
Q11-0
R
HC4040
BINARY
CTR
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
R
HC4538
R/C C
HC4538
A
B
MULTI
VIB
Q
Q
CD
PULSE_WIDTH=10000


HC4002
(SIZE)
HC4002
HC4002
HC4016
(SIZE)
HC4016
ANALOG
SWITCH
IN OUT
CNTL
HC4024
HC4024
RIPPLE
COUNTER
Q6-0
R
HC4024
RIPPLE
COUNTER
Q6
Q5
Q4
Q3
Q2
Q1
Q0
R
HC4049
(SIZE)
HC
4049
HC4050
(SIZE)
HC
4050
HC4051
(SIZE)
X7
X6
X5
X4
X3
X2
X1
X0
HC
4051
MUX/
DEMUX
X
INH
S2-0
X7
X6
X5
X4
X3
X2
X1
X0
HC
4051
MUX/
DEMUX
X
INH
S2
S1
S0
HC4052
(SIZE)
HC
4052
X3
X2
X1
X0
MUX/
DEMUX
X
INH
S1-0
HC
4052
X3
X2
X1
X0
MUX/
DEMUX
X
INH
S0
S1
HC4052
X31
X21
X11
X01
X1
MUX/
DEMUX
X30
X20
X10
X00
X0
INH
S1
S0
HC4053
(SIZE)
HC
4053
MUX/
DEMUX
X1
X
X0
INH
S
HC4066
(SIZE)
HC
4066
SWITCH/
MUX
A
B
CNTL
HC4075
(SIZE)
HC
4075
HC
4075
HC4078
(SIZE)
HC
4078
HC
4078

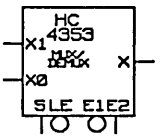
HC4316
(SIZE)

HC4351
(SIZE)

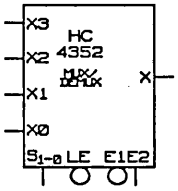


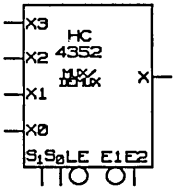


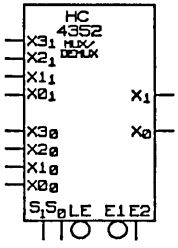
HC4353
(SIZE)



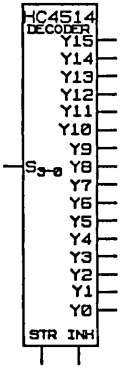
HC4352
(SIZE)

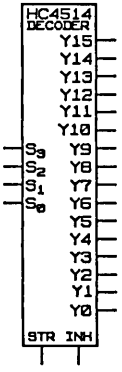


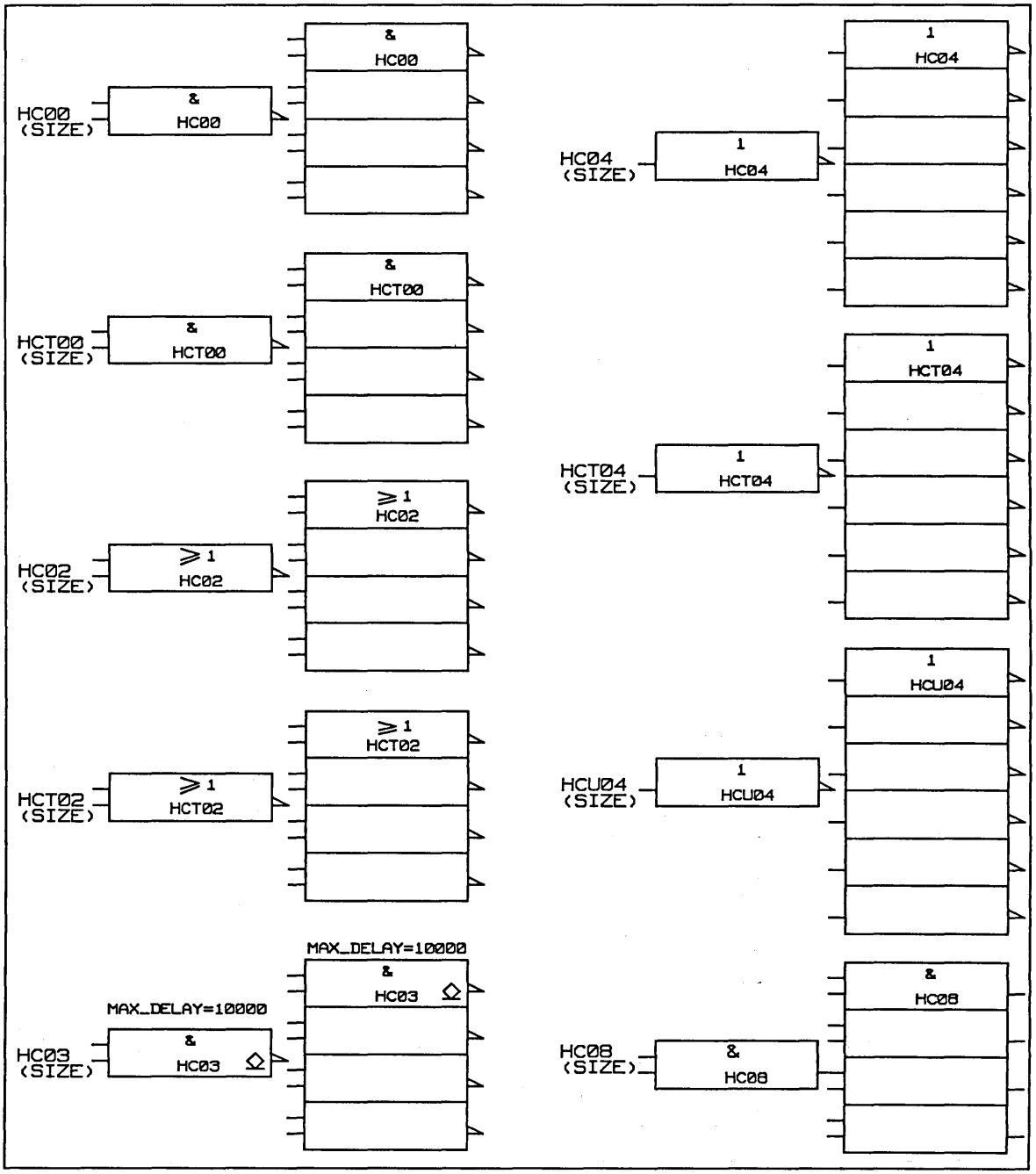


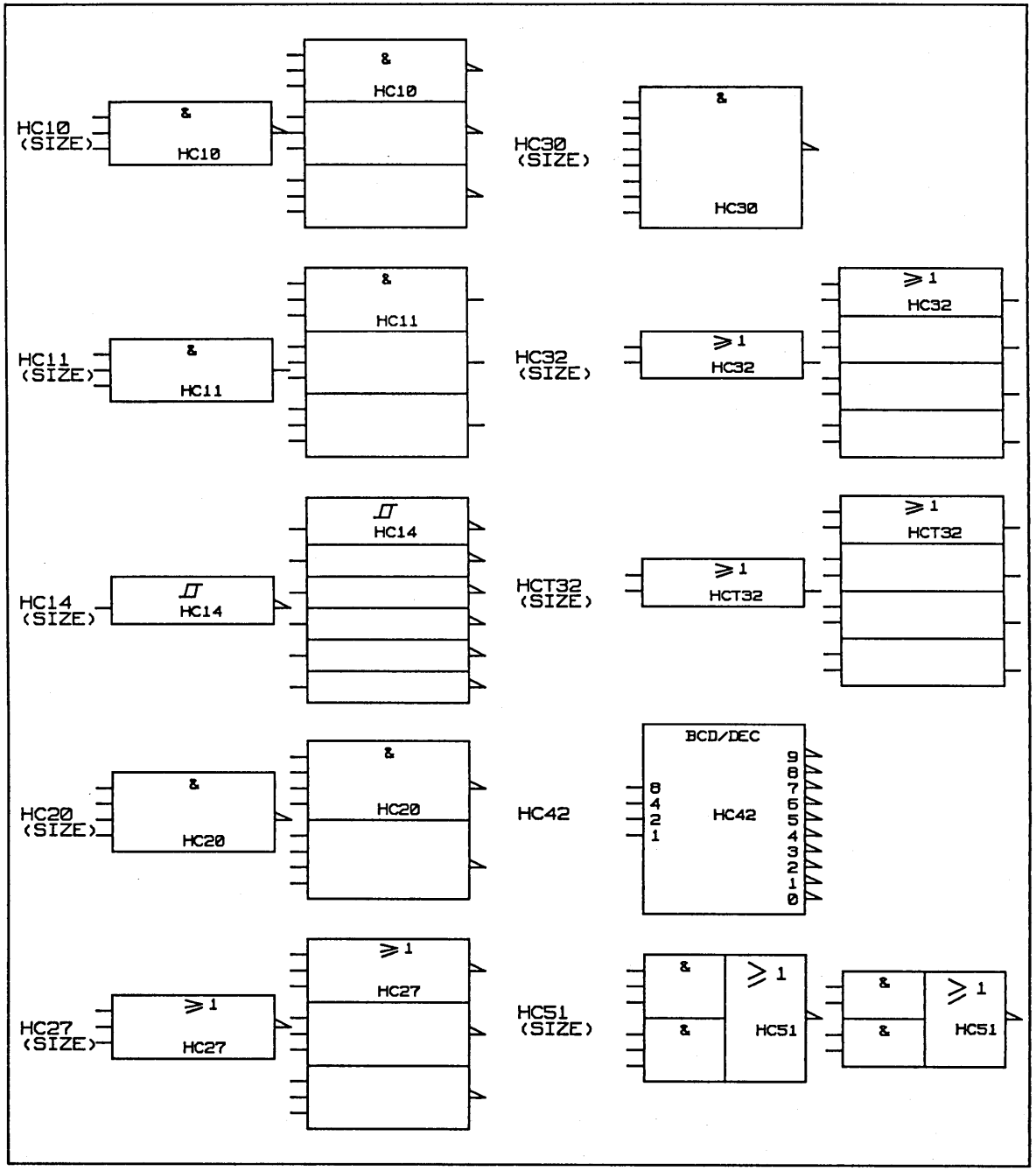


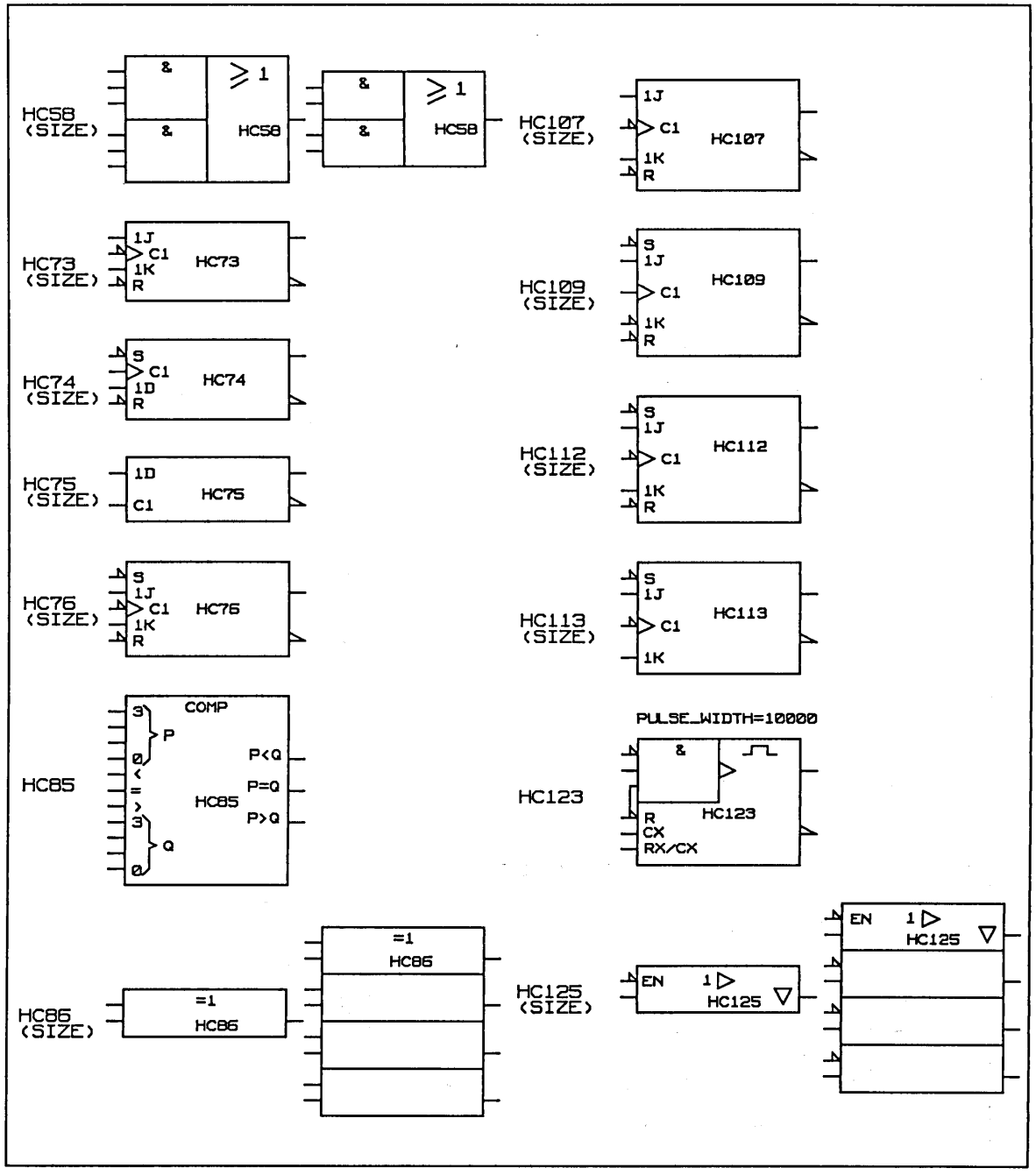
HC4514

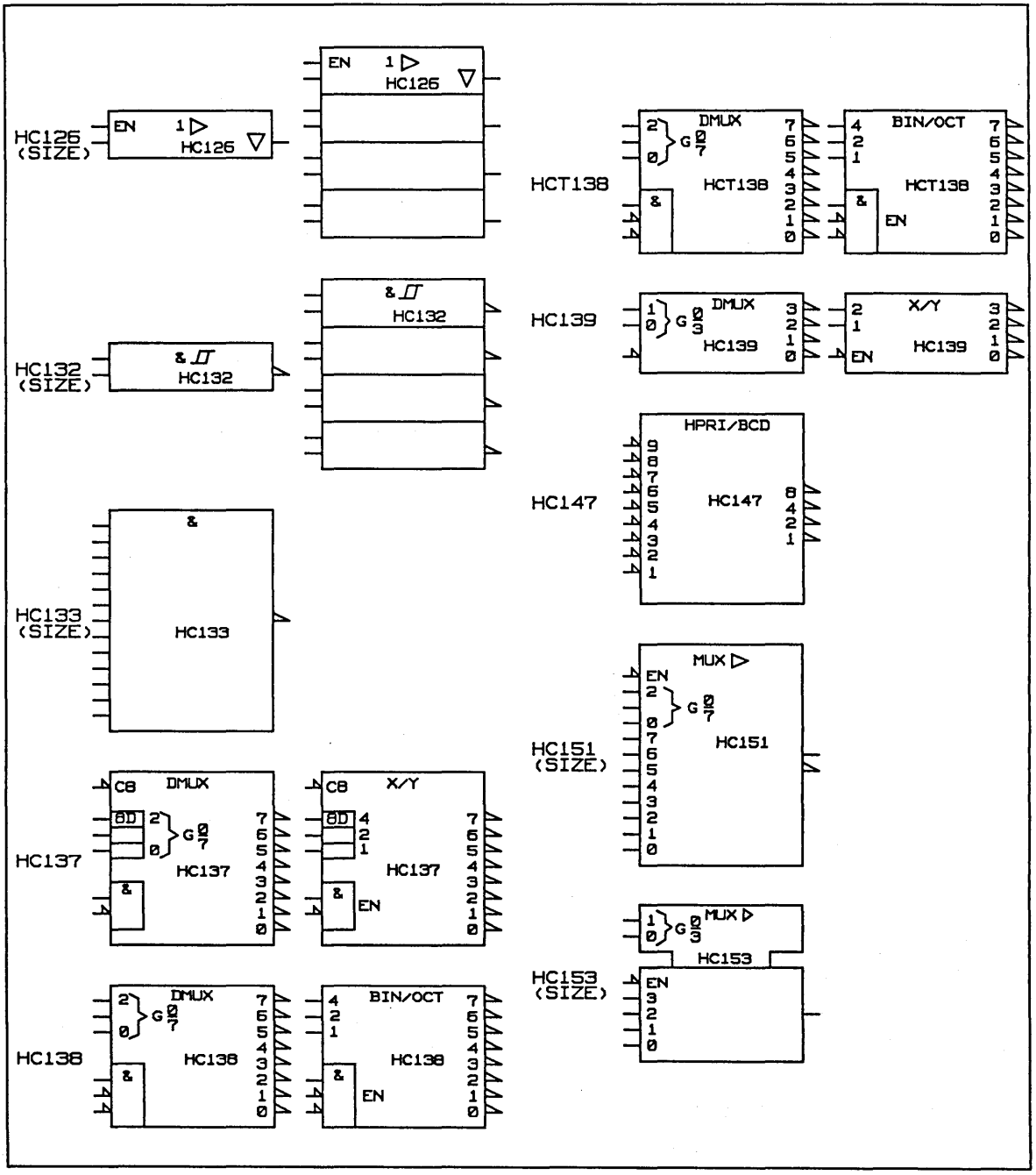


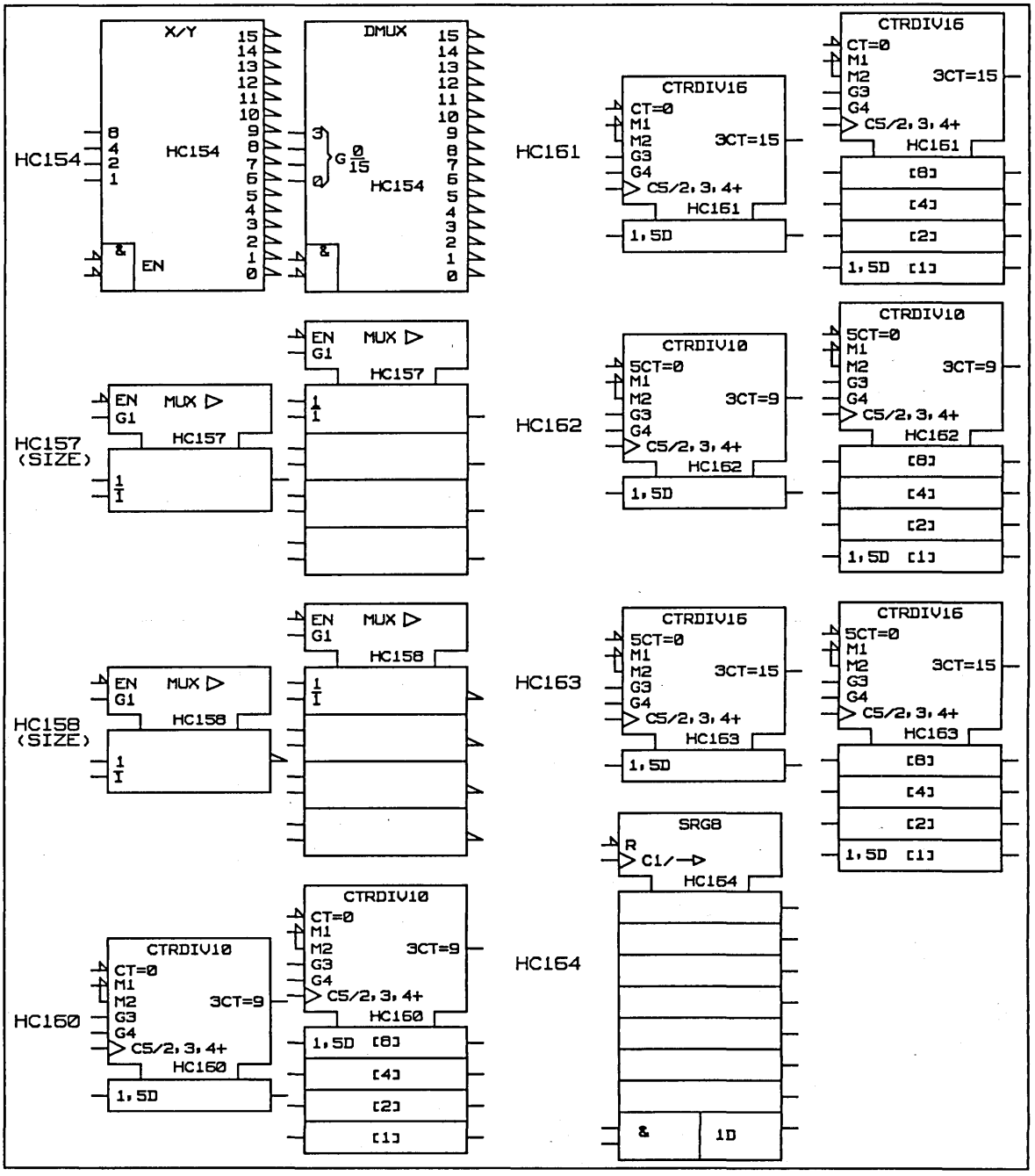


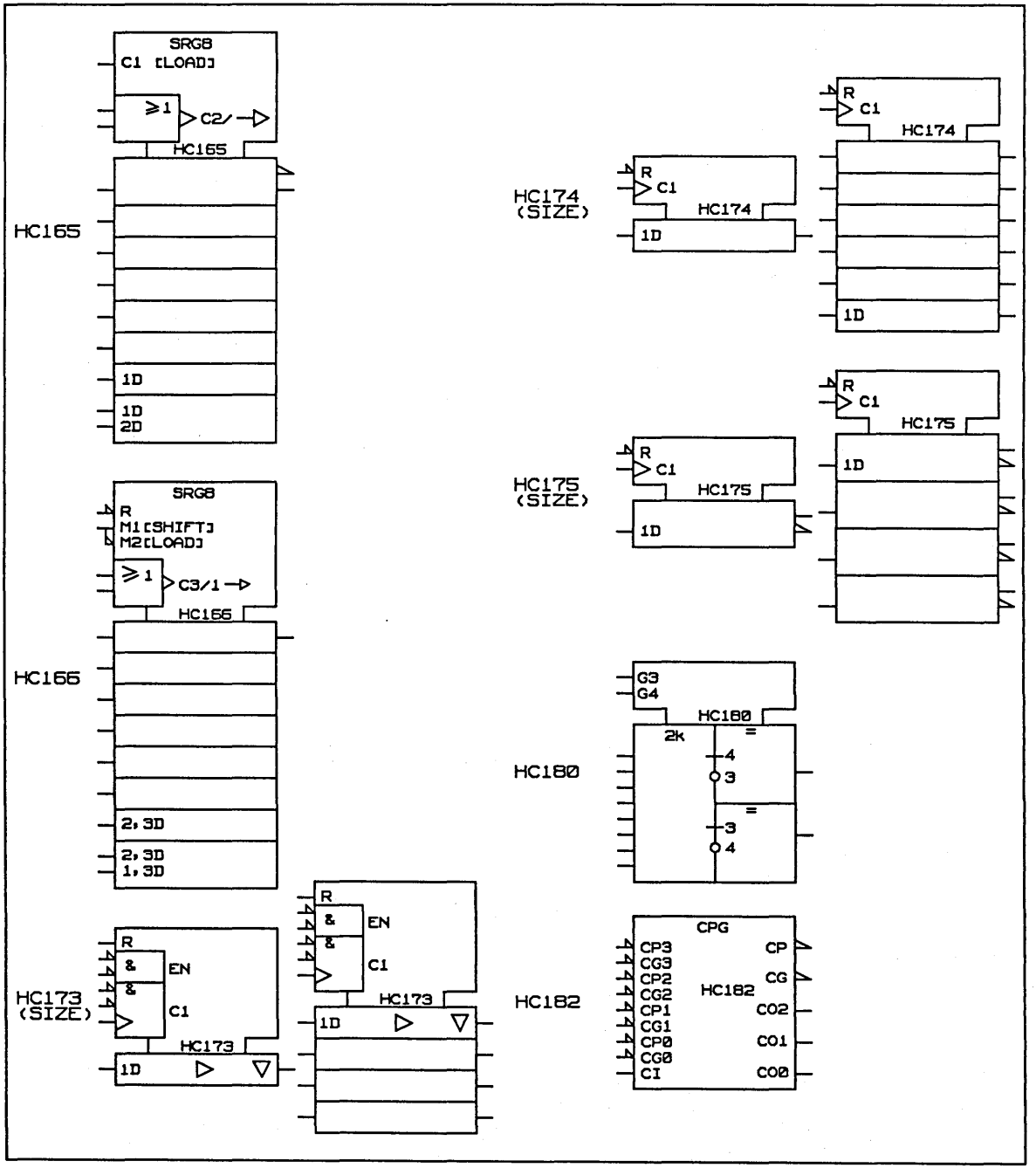

HC00
(SIZE)
&
HC00
HCT00
(SIZE)
&
HCT00
HC02
(SIZE)
≥1
HC02
HCT02
(SIZE)
≥1
HCT02
MAX_DELAY=10000
HC03
(SIZE)
&
HC03
HC04
(SIZE)
1
HC04
HCT04
(SIZE)
1
HCT04
HCU04
(SIZE)
1
HCU04
HC08
(SIZE)
&
HC08

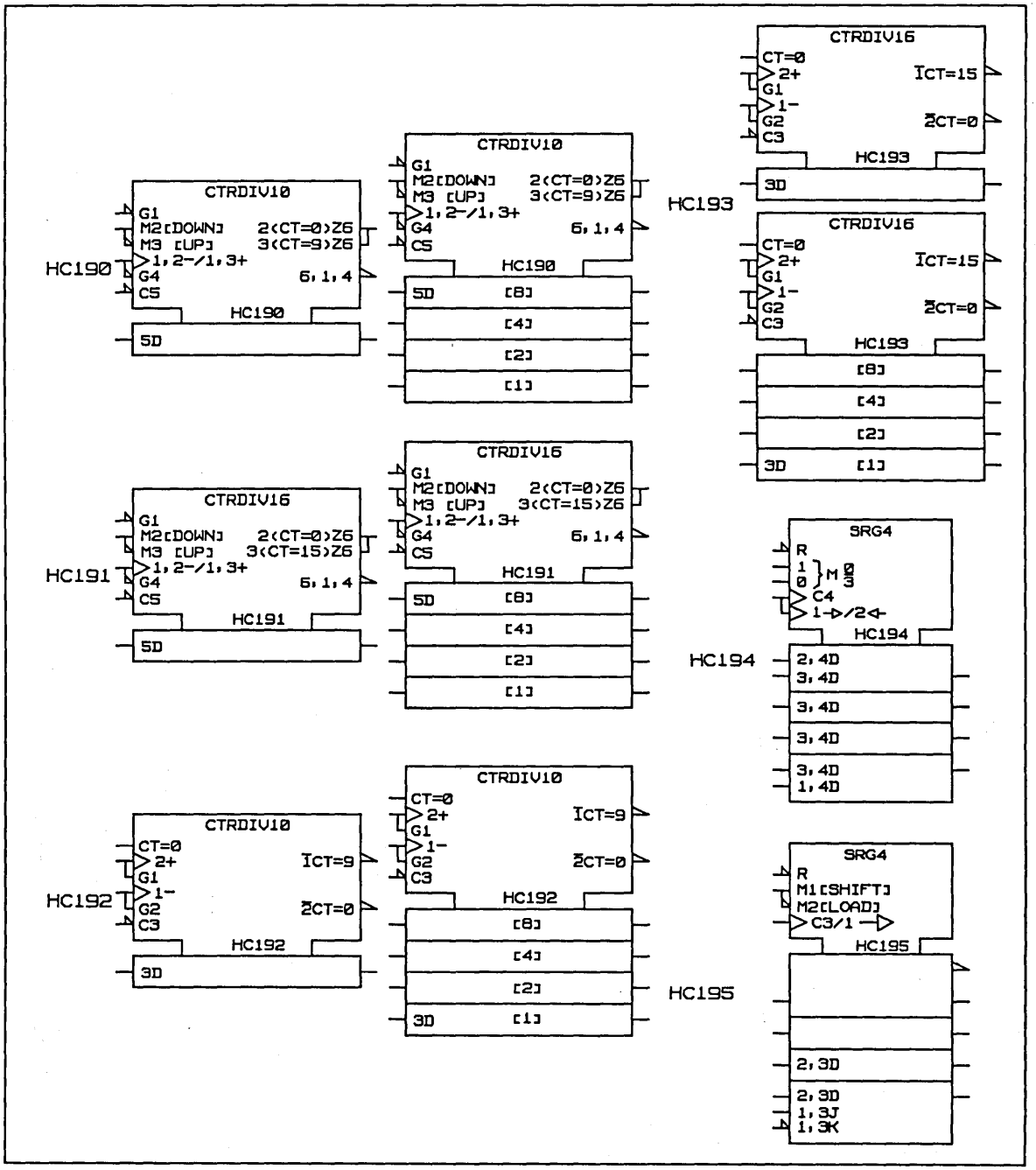

HC10
(SIZE)
&
HC10
HC30
(SIZE)
HC30
HC11
(SIZE)
HC11
HC32
(SIZE)
≥1
HC32
HC14
(SIZE)
HC14
HCT32
(SIZE)
HCT32
HC20
(SIZE)
HC20
HC42
BCD/DEC
8
4
2
1
9
8
7
6
5
4
3
2
1
0
HC42
HC27
(SIZE)
HC27
HC51
(SIZE)
HC51

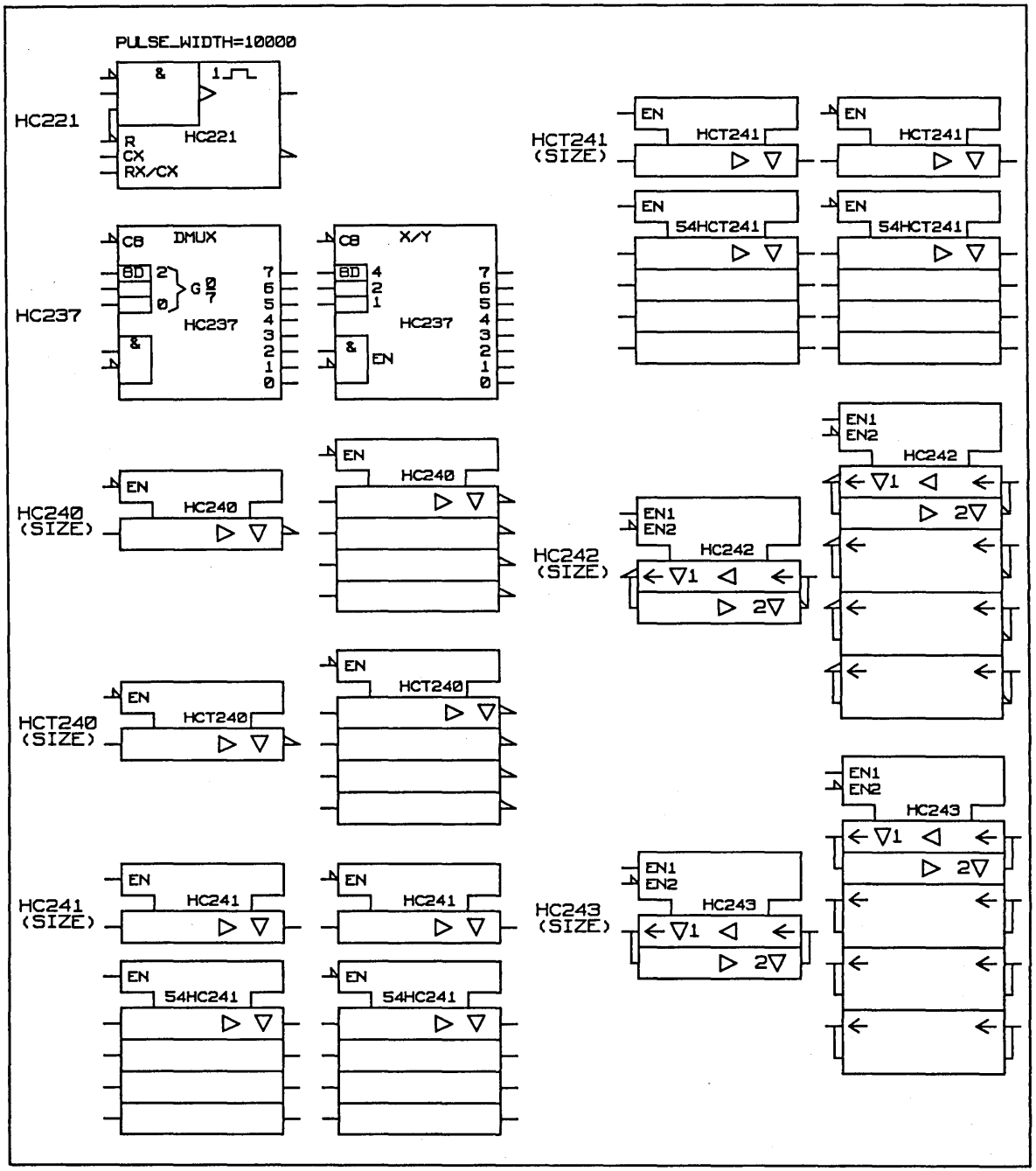

HC58
(SIZE)
&
&
≥1
HC58
HC73
(SIZE)
1J
C1
1K
R
HC73
HC74
(SIZE)
S
C1
1D
R
HC74
HC75
(SIZE)
1D
C1
HC75
HC76
(SIZE)
S
1J
C1
1K
R
HC76
HC85
COMP
P
Q
P<Q
P=Q
P>Q
HC85
HC86
(SIZE)
=1
HC86
HC107
(SIZE)
1J
C1
1K
R
HC107
HC109
(SIZE)
S
1J
C1
1K
R
HC109
HC112
(SIZE)
S
1J
C1
1K
R
HC112
HC113
(SIZE)
S
1J
C1
1K
HC113
HC123
PULSE_WIDTH=10000
&
R
CX
RX/CX
HC123
HC125
(SIZE)
EN
1
HC125

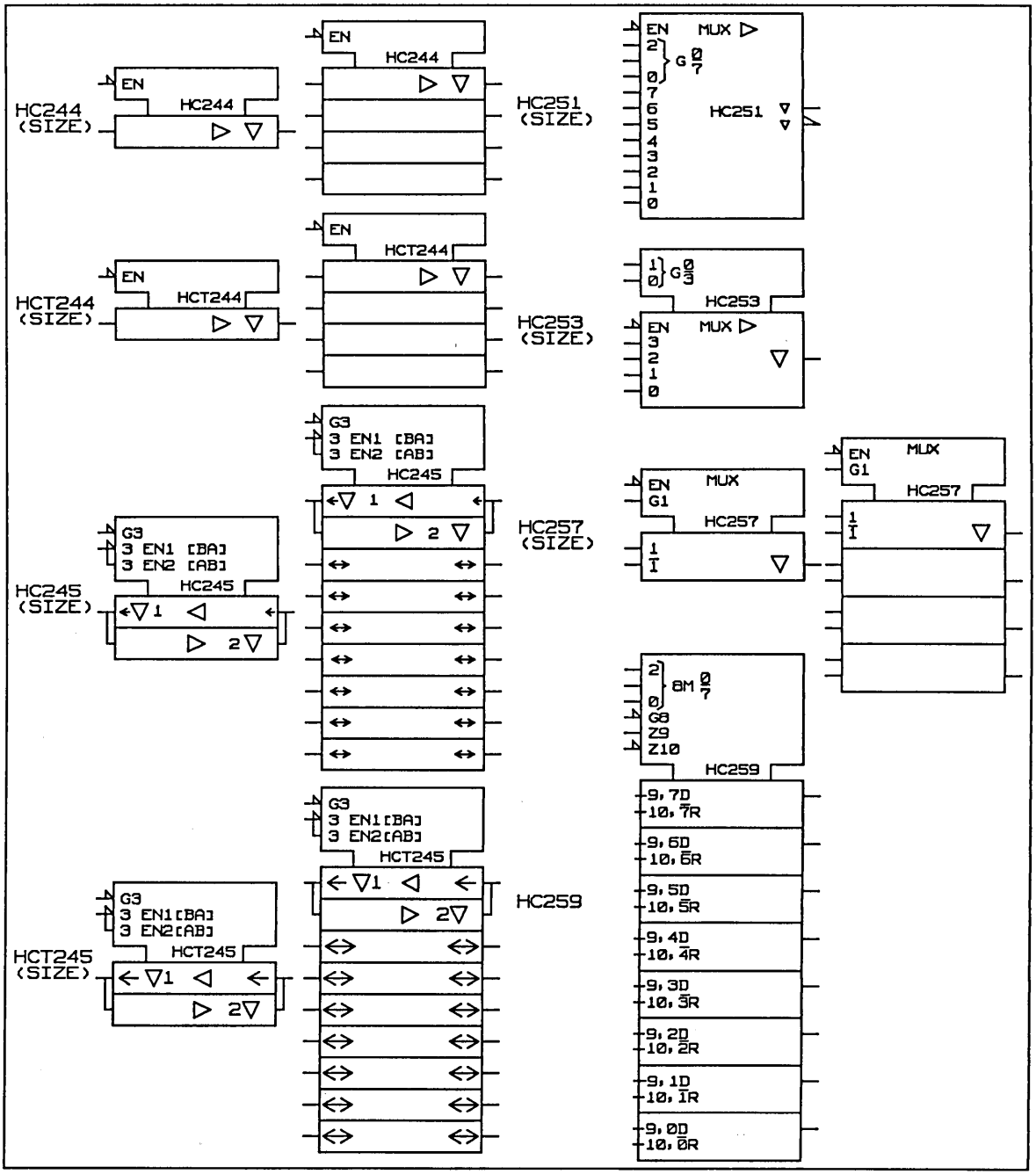

HC126
(SIZE)
EN
1
HC126
HC132
(SIZE)
&
HC132
HC133
(SIZE)
&
HC133
HC137
C8
DMUX
8D
2
0
G
0
7
HC137
&
7 6 5 4 3 2 1 0
C8
X/Y
8D
4
2
1
HC137
&
EN
7 6 5 4 3 2 1 0
HC138
DMUX
2
0
G
0
7
HC138
&
7 6 5 4 3 2 1 0
4
2
1
BIN/OCT
HC138
&
EN
7 6 5 4 3 2 1 0
HC126
HC132
HCT138
DMUX
2
0
G
0
7
HCT138
&
7 6 5 4 3 2 1 0
4
2
1
BIN/OCT
HCT138
&
EN
7 6 5 4 3 2 1 0
HC139
1
0
G
0
3
DMUX
HC139
3 2 1 0
2
1
X/Y
HC139
EN
3 2 1 0
HC147
HPRI/BCD
9 8 7 6 5 4 3 2 1
HC147
8 4 2 1
HC151
(SIZE)
MUX
EN
2
0
G
0
7
7 6 5 4 3 2 1 0
HC151
HC153
(SIZE)
1
0
G
0
3
MUX
HC153
EN
3 2 1 0

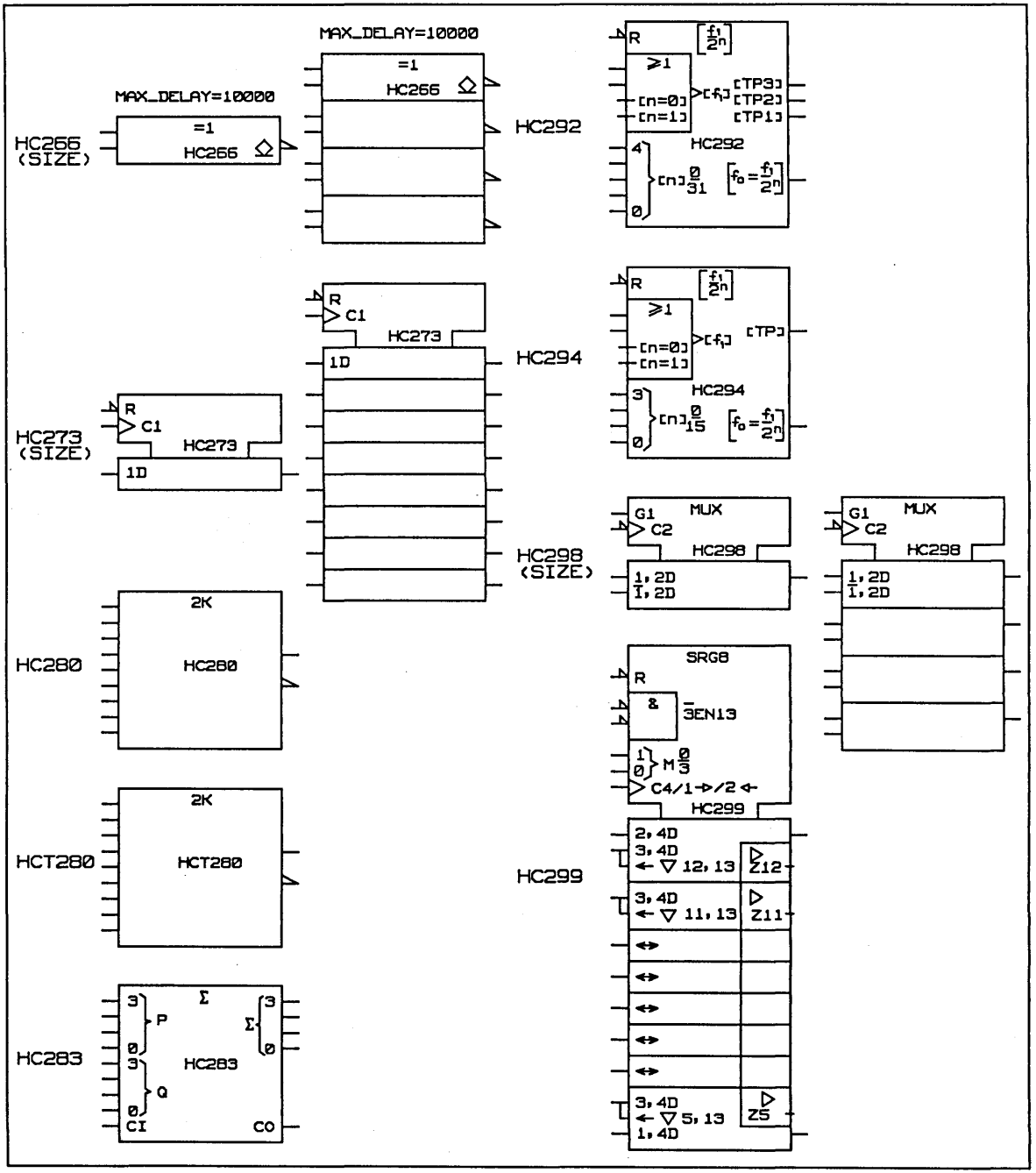

HC154
X/Y
HC154
EN
DMUX
HC154
HC161
CTRDIV16
CT=0
M1
M2
G3
G4
3CT=15
C5/2, 3, 4+
HC161
1, 5D
HC157
(SIZE)
EN
G1
MUX
HC157
HC162
CTRDIV10
5CT=0
3CT=9
HC162
HC158
(SIZE)
HC158
HC163
HC164
SRG8
R
C1/
HC164
&
1D
HC160
CTRDIV10
HC160

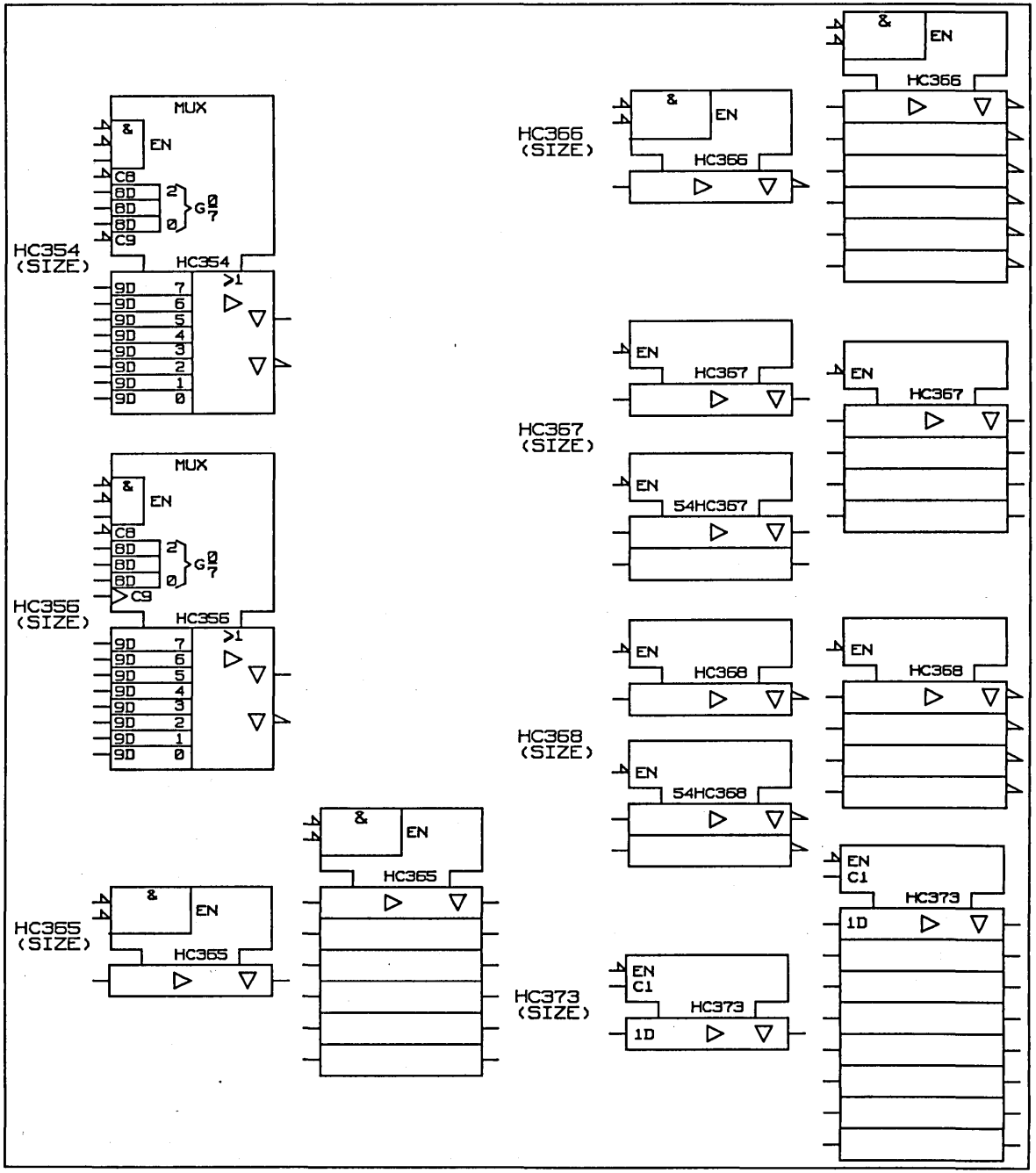

SRG8
C1 [LOAD]
≥1
C2/
HC165
HC165
1D
1D
2D
SRG8
R
M1 [SHIFT]
M2 [LOAD]
≥1
C3/1
HC166
HC166
2,3D
2,3D
1,3D
R
&
EN
C1
HC173
HC173
1D
HC173 (SIZE)
R
&
EN
C1
HC173
1D
HC174 (SIZE)
R
C1
HC174
1D
R
C1
HC174
1D
HC175 (SIZE)
R
C1
HC175
1D
R
C1
HC175
1D
G3
G4
HC180
2k
=
4
3
=
3
4
HC180
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
HC182
CP
CG
CO2
CO1
CO0
HC182

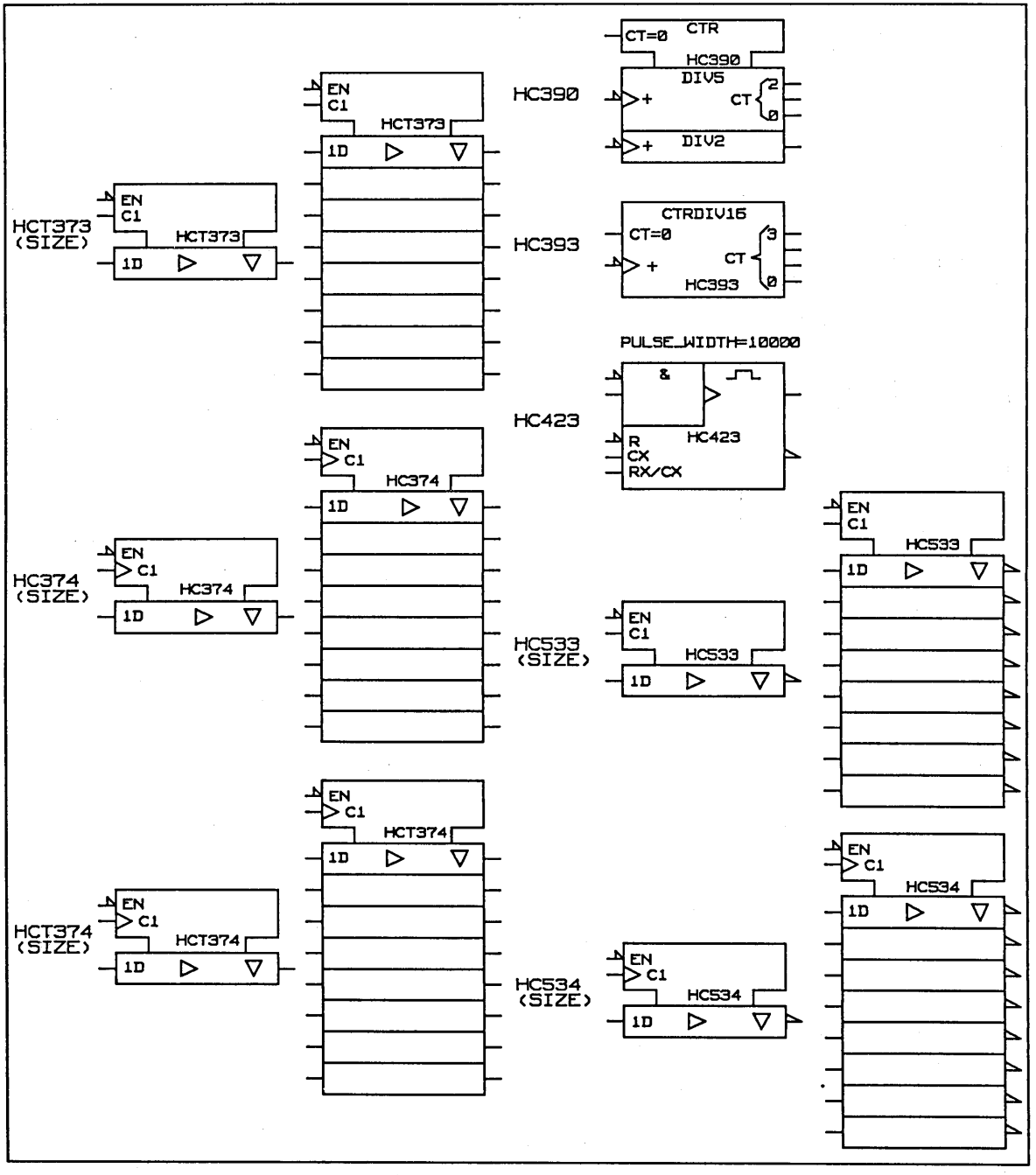

CTRDIV16
CT=0
2+
G1
1-
G2
C3
ICT=15
2CT=0
HC193
3D
HC193
CTRDIV10
G1
M2[DOWN]
M3 [UP]
1,2-/1,3+
G4
CS
2<CT=0>Z6
3<CT=9>Z6
6,1,4
HC190
5D
[8]
[4]
[2]
[1]
HC190
CTRDIV16
G1
M2[DOWN]
M3 [UP]
1,2-/1,3+
G4
CS
2<CT=0>Z6
3<CT=15>Z6
6,1,4
HC191
5D
[8]
[4]
[2]
[1]
HC191
SRG4
R
1
0
M
C4
1-▷/2◁-
HC194
2,4D
3,4D
3,4D
3,4D
3,4D
1,4D
HC194
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
2CT=0
HC192
3D
[8]
[4]
[2]
[1]
HC192
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
HC195
2,3D
2,3D
1,3J
1,3K
HC195

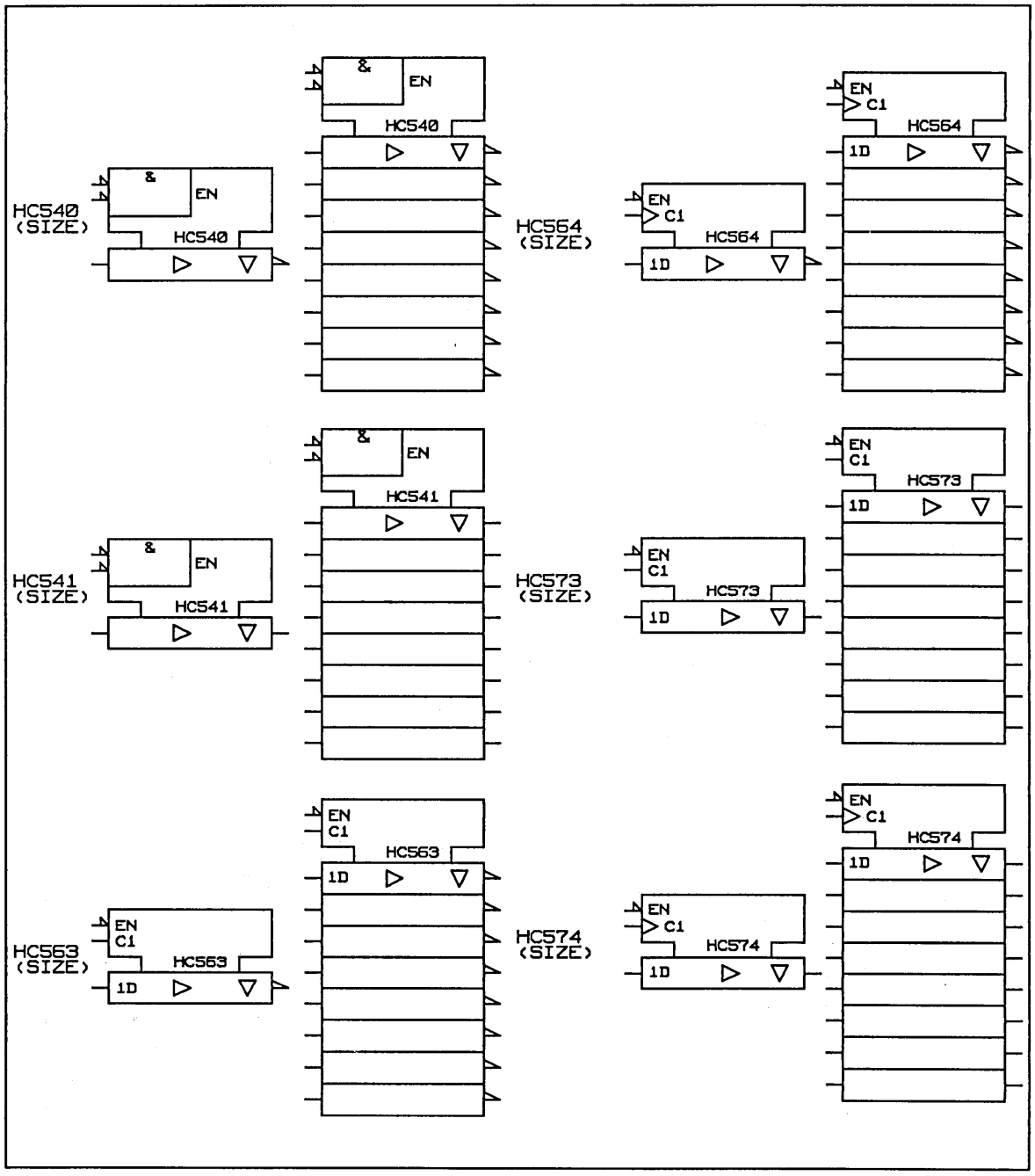

PULSE_WIDTH=10000
HC221
HC221
R
CX
RX/CX
HC237
CB
DMUX
BD
G
HC237
X/Y
EN
HC240
(SIZE)
HCT240
HC241
54HC241
HCT241
54HCT241
HC242
HC243
EN1
EN2
1
2

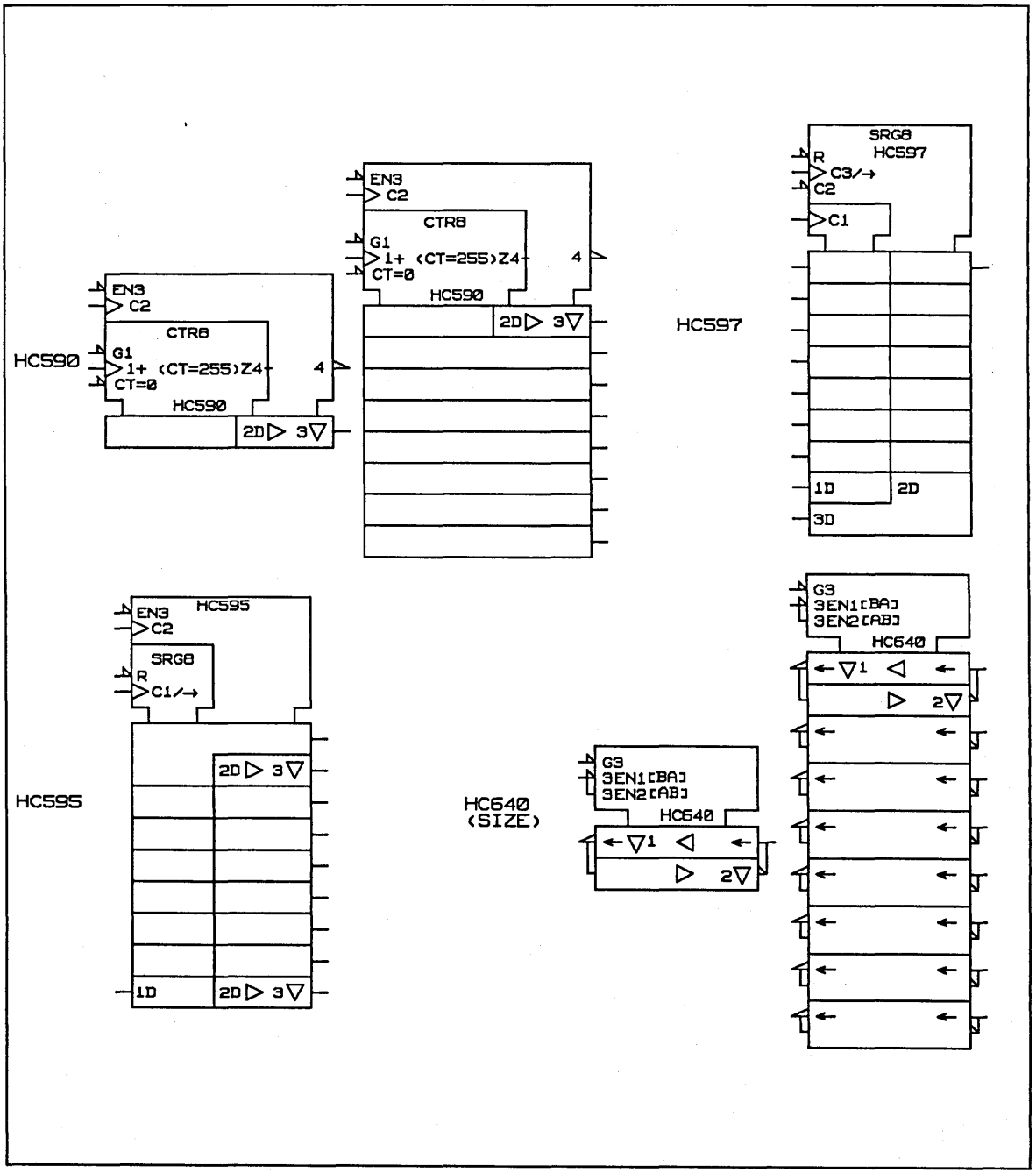

HC244
(SIZE)
EN
HC244
HCT244
(SIZE)
HCT244
G3
3 EN1 [BA]
3 EN2 [AB]
HC245
HCT245
HC251
(SIZE)
HC253
(SIZE)
HC257
(SIZE)
HC259
MUX
HC251
HC253
HC257
HC259
8M
9,7D
10,7R
9,6D
10,6R
9,5D
10,5R
9,4D
10,4R
9,3D
10,3R
9,2D
10,2R
9,1D
10,1R
9,0D
10,0R

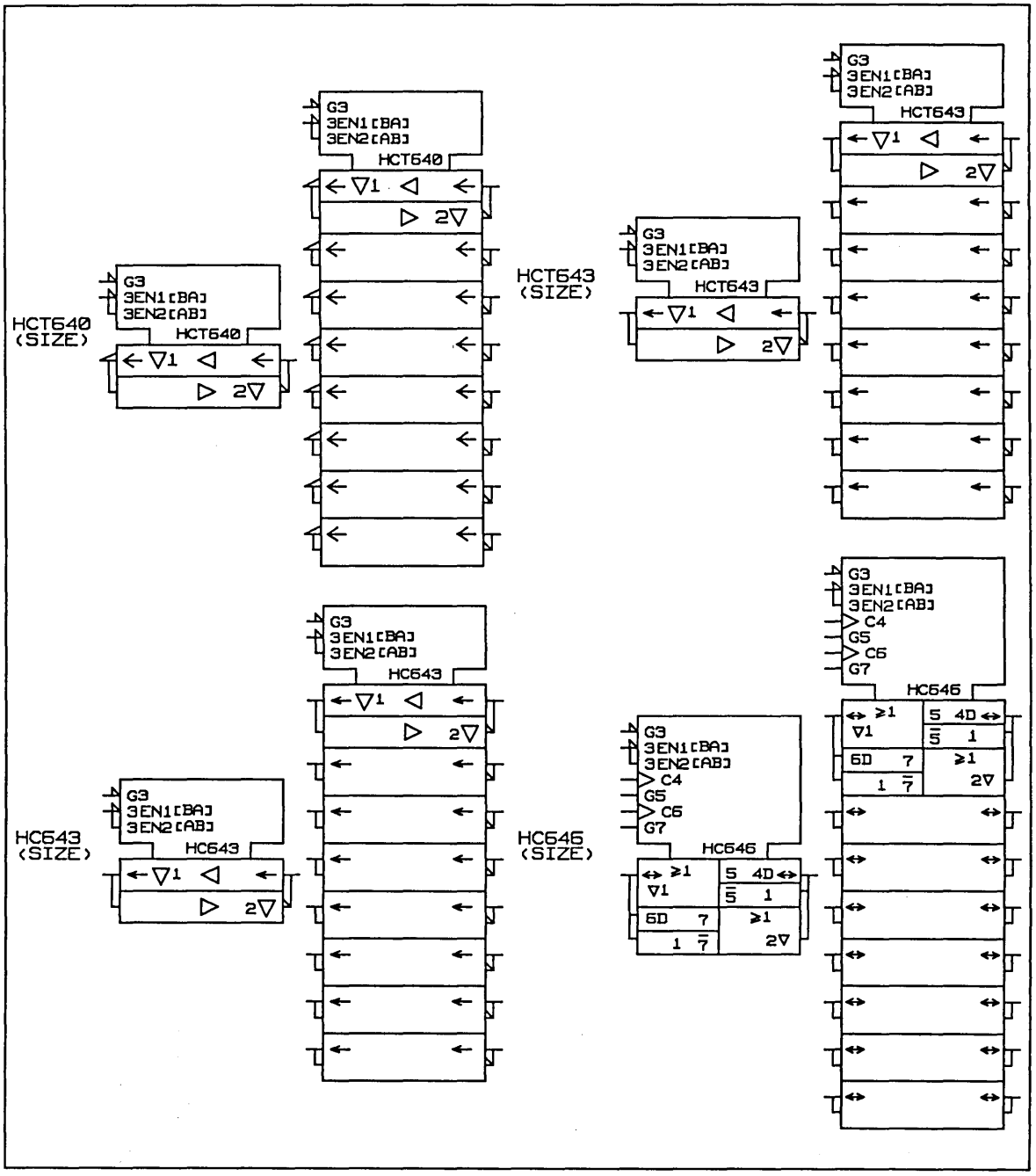

MAX_DELAY=10000
=1
HC266
HC266
(SIZE)
HC292
HC273
(SIZE)
HC294
HC298
(SIZE)
HC280
HCT280
HC283
HC299
HC273
1D
2K
HC280
HCT280
P
Q
Σ
CI
CO
R
C1
≥1
[n=0]
[n=1]
[TP3]
[TP2]
[TP1]
[TP]
G1
C2
MUX
SRG8
&
3EN13
C4/1→/2←
2,4D
3,4D
12,13
11,13
5,13
1,4D
Z12
Z11
Z5

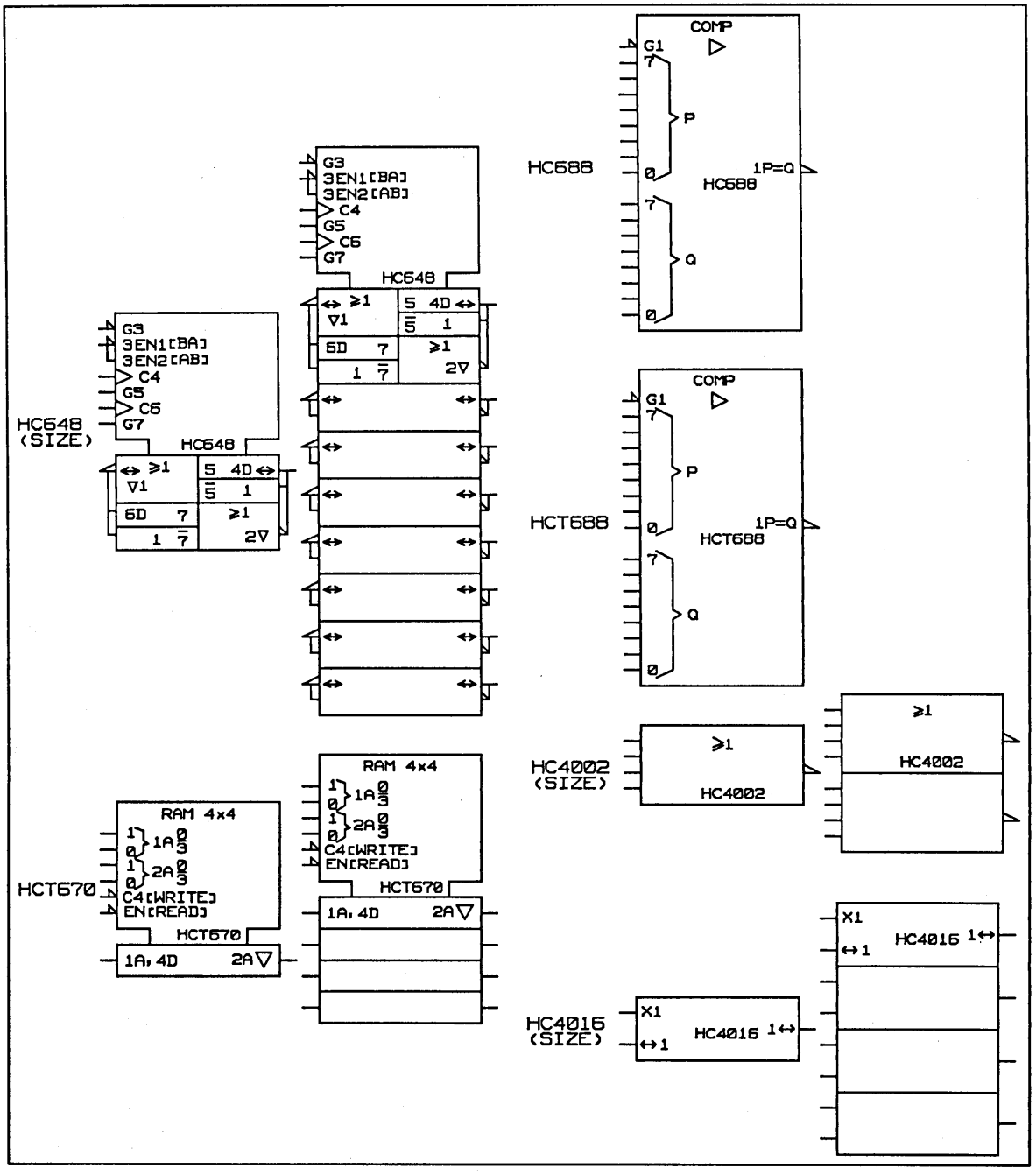

MUX
&
EN
C8
8D
8D
8D
C9
2
0
G0
7
HC354
(SIZE)
HC354
9D 7
9D 6
9D 5
9D 4
9D 3
9D 2
9D 1
9D 0
>1
MUX
&
EN
C8
8D
8D
8D
C9
2
0
G0
7
HC356
(SIZE)
HC356
9D 7
9D 6
9D 5
9D 4
9D 3
9D 2
9D 1
9D 0
>1
&
EN
HC365
&
EN
HC365
HC365
(SIZE)
&
EN
HC366
HC366
(SIZE)
&
EN
HC366
EN
HC367
EN
HC367
HC367
(SIZE)
EN
54HC367
EN
HC368
EN
HC368
HC368
(SIZE)
EN
54HC368
EN
C1
HC373
1D
EN
C1
HC373
HC373
(SIZE)
1D

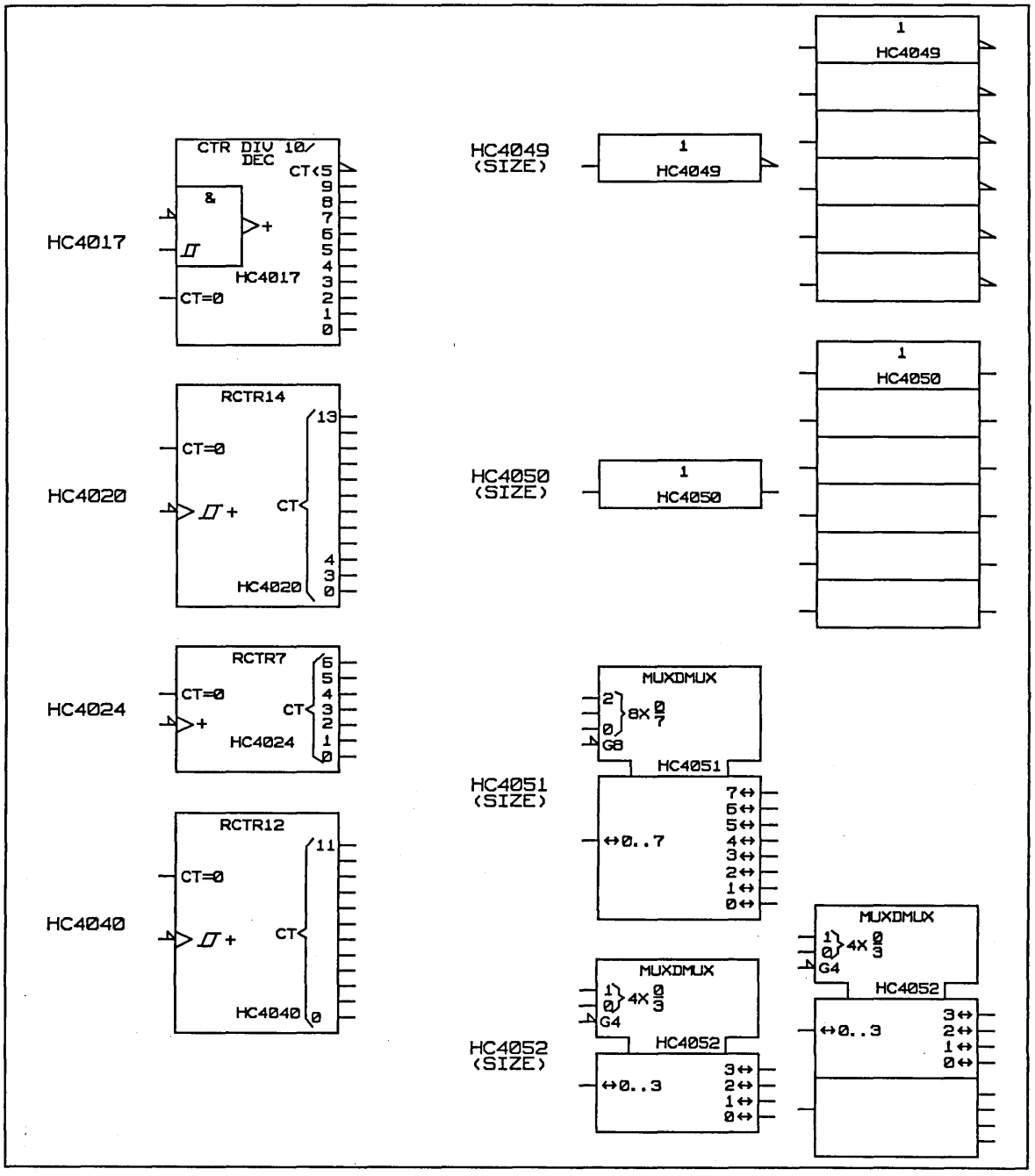

HCT373
(SIZE)
EN
C1
1D
HCT373
HC390
CT=0
CTR
HC390
DIV5
CT
2
0
DIV2
HC393
CTRDIV16
CT=0
CT
3
0
HC393
PULSE_WIDTH=10000
HC423
&
R
CX
RX/CX
HC374
(SIZE)
HC374
HC533
(SIZE)
HC533
HCT374
(SIZE)
HCT374
HC534
(SIZE)
HC534

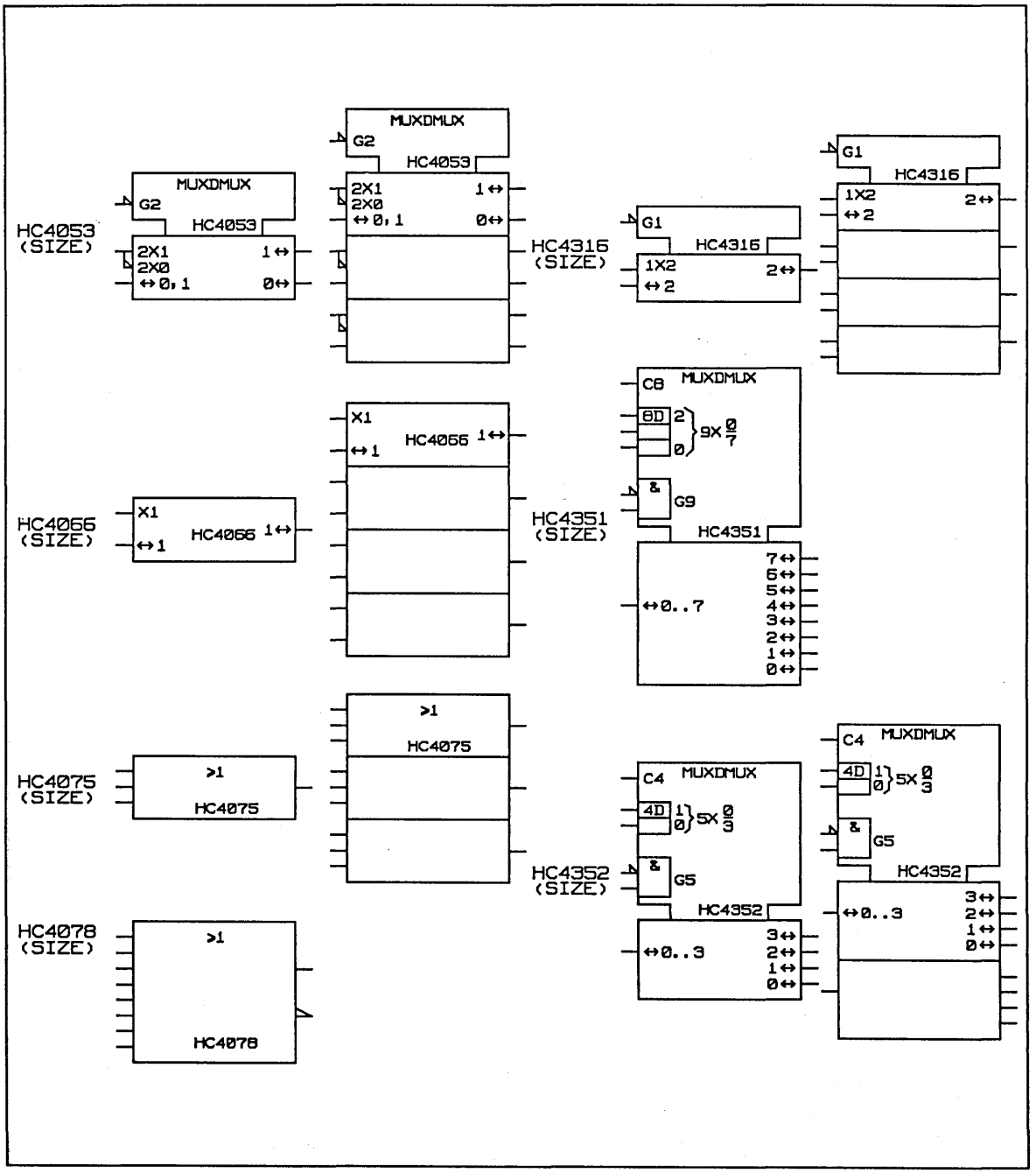

HC540
(SIZE)
&
EN
HC540
HC564
(SIZE)
EN
C1
1D
HC564
HC541
(SIZE)
HC541
HC573
(SIZE)
HC573
HC563
(SIZE)
HC563
HC574
(SIZE)
HC574


HC590
EN3
C2
CTR8
G1
1+ (CT=255)Z4
CT=0
4
HC590
2D
3
HC597
SRG8
HC597
R
C3/→
C2
C1
1D
2D
3D
HC595
EN3
C2
HC595
SRG8
R
C1/→
2D
3
1D
HC640
(SIZE)
G3
3EN1[BA]
3EN2[AB]
HC640
1
2

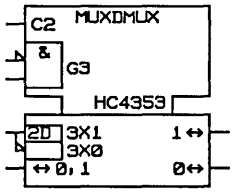

HCT640
(SIZE)
HCT643
(SIZE)
HC643
(SIZE)
HC646
(SIZE)
G3
3EN1[BA]
3EN2[AB]
HCT640
HCT643
HC643
HC646
C4
G5
C6
G7
∇1
2∇
≥1
6D
7
5
4D
1

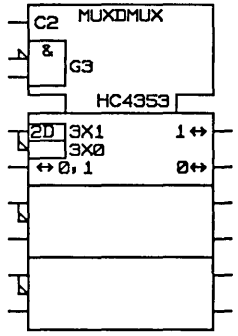

COMP
G1
P
Q
1P=Q
HC688
HC688
HCT688
HCT688
G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
HC648
HC648
(SIZE)
RAM 4x4
1A
2A
C4[WRITE]
EN[READ]
HCT670
1A, 4D
2A
HC4002
HC4002
(SIZE)
X1
HC4016 1↔
HC4016
(SIZE)


HC4017
CTR DIV 10/ DEC
CT<5
9
8
7
6
5
4
3
2
1
0
&
+
HC4017
CT=0
HC4020
RCTR14
CT=0
CT
13
4
3
0
HC4020
HC4024
RCTR7
CT=0
CT
5
5
4
3
2
1
0
HC4024
HC4040
RCTR12
CT=0
CT
11
HC4040
0
HC4049
(SIZE)
1
HC4049
1
HC4049
HC4050
(SIZE)
1
HC4050
1
HC4050
HC4051
(SIZE)
MUXDMUX
2
0
8X 0 7
G8
HC4051
↔0..7
7↔
6↔
5↔
4↔
3↔
2↔
1↔
0↔
HC4052
(SIZE)
MUXDMUX
1
0
4X 0 3
G4
HC4052
↔0..3
3↔
2↔
1↔
0↔
MUXDMUX
1
0
4X 0 3
G4
HC4052
↔0..3
3↔
2↔
1↔
0↔

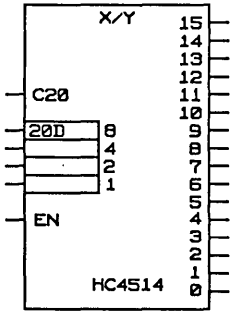

HC4053
(SIZE)
MUXDMUX
G2
HC4053
2X1
2X0
↔0,1
1↔
0↔
HC4316
(SIZE)
G1
HC4316
1X2
↔2
2↔
HC4066
(SIZE)
X1
↔1
HC4066
1↔
HC4351
(SIZE)
C8
MUXDMUX
8D
2
0
9X 0 7
&
G9
HC4351
↔0..7
7↔
6↔
5↔
4↔
3↔
2↔
1↔
0↔
HC4075
(SIZE)
>1
HC4075
HC4352
(SIZE)
C4
MUXDMUX
4D
1
0
5X 0 3
&
G5
HC4352
↔0..3
3↔
2↔
1↔
0↔
HC4078
(SIZE)
>1
HC4078

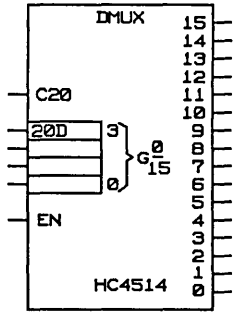
HC4353
(SIZE)



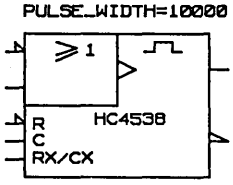


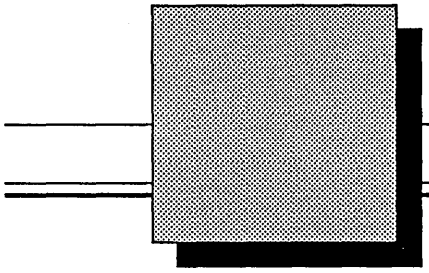
HC4514





HC4538





The FAST and ANSI FAST Libraries

The FAST Library requires approximately 7778 Kbytes of disk storage, and the ANSI FAST Library requires approximately 7679 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*fast.lib* or *a74fast.lib*).

The specifications used to construct the models in these libraries were taken from either the Fairchild data books or the Signetics data books. Those marked with an asterisk (*) are from the Signetics data books..

The release level of the FAST and ANSI FAST Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 195 components:

F00	Quad 2-input NAND
F02	Quad 2-input NOR
F04	Hex inverter
F08	Quad 2-input AND
F10	Triple 3-input NAND
F11	Triple 3-input AND
* **F13**	Dual 4-input NAND Schmitt trigger
* **F14**	Hex inverter Schmitt trigger
F20	Dual 4-input NAND
* **F30**	8-input NAND gate
F32	Quad 2-input OR
* **F37**	Quad 2-input NAND buffer
F38	Quad 2-input NAND buffer (open-collector)
* **F40**	Dual 4-input NAND buffer
* **F51**	Dual 2-wide 3-input, 2-wide 2-input AND-OR-invert
F64	4-2-3-2-input AND-OR-invert gate
F74	Dual positive-edge-triggered D flip-flop
* **F83**	4-bit binary adder with fast carry (center power pin version of F283)
F85	4-bit magnitude comparator
F86	Quad 2-input exclusive-OR

F109	Dual JKbar positive-edge-triggered flip-flop
F112	Dual JK negative-edge-triggered flip-flop
F113	Dual JK edge-triggered flip-flop
F114	Dual JK negative-edge-triggered flip-flop
* **F125**	Quad buffer (3-state)
* **F126**	Quad buffer (3-state)
* **F132**	Quad 2-input NAND Schmitt trigger
* **F133**	13-input NAND
F138	3-to-8-line decoders/multiplexers
F139	Dual 2-to-4-line decoders/multiplexers
F148	8-line to 3-line Octal priority encoder
F151	1-of-8 data selectors/multiplexers
* **F151A**	8-input multiplexers
F153	Dual 4-line to 1-line data multiplexer
* **F154**	1-of-16 decoder/demultiplexer
F157	Quad 2-to-1-line non-inverting multiplexer
* **F157A**	Quad 2-input data selector/multiplexer (non-inverted)
F158	Quad 2-to-1-line inverting data multiplexer
* **F158A**	Quad 2-input data selector/multiplexer (inverted)
F160	4-bit synchronous decade counters with direct clear
* **F160A**	BCD decade counter
F161	4-bit synchronous binary counters with direct clear
* **F161A**	4-bit binary counter
F162	4-bit synchronous decade counters with synch clear
* **F162A**	BCD decade counter

F163	4-bit synchronous binary counters with synch clear
* **F163A**	4-bit binary counter
F164	8-bit parallel output serial shift register
* **F166**	8-bit serial/parallel-in, serial out shift register
F168	4-bit synchronous decade up/down counters
F169	4-bit synchronous binary up/down counters
* **F173**	Quad D-type flip-flops with 3-state output
F174	Hex D-type flip-flops
F175	Quad D-type flip-flops
F181	Arithmetic logic units/function generators
F182	Look-ahead carry generators
F189	64-bit random access memory
* **F189A**	64-bit TTL bipolar RAM
F190	Synchronous BCD up/down counter
F191	Synchronous binary up/down counter
F192	Synchronous decade up/down counter
F193	Synchronous binary up/down dual clock counters
F194	4-bit bidirectional shift register
* **F195**	4-bit parallel access shift register
* **F198**	8-bit bidirectional universal shift register
* **F199**	8-bit parallel-access shift register
F219	64-bit random access memory
* **F219A**	64-bit random access memory
F240	Octal inverting 3-state bus transceiver
F241	Octal non-inverting 3-state bus transceiver

F242	Quad inverting 3-state bus transceiver
F243	Quad non-inverting 3-state bus transceiver
F244	Octal non-inverting 3-state bus transceiver
F245	Octal non-inverting 3-state bus transceiver
F251	3-state data multiplexer
* **F251A**	8-input multiplexer (3-state)
F253	Dual data selectors/multiplexers
* **F256**	Dual 4-bit addressable latch
F257	Quad 3-state non-inverting data multiplexer
* **F257A**	Quad 2-to-1 line data selector/multiplexer (3-state)
F258	Quad 3-state inverting data multiplexer
* **F258A**	Quad 2-to-1 line data selector/multiplexer (3-state)
* **F259**	8-bit addressable latch
F269	8-bit bidirectional binary counter
F273	Octal D flip-flop
F280	9-bit odd/even parity generators/checkers
F283	4-bit binary full adders
* **F298**	Quad 2-input multiplexer with storage
F299	8-bit bidirectional 3-state shift/storage register
F322	8-bit serial/parallel register with sign extend
F323	8-bit universal shift/storage register with synch reset and common I/O pins
* **F350**	4-bit shifter (3-state)
* **F352**	Dual 4-to-1 line multiplexer
F353	Dual 4-input multiplexer with 3-state output
* **F365**	Hex buffer with common enable (3-state)

* **F366**	Hex inverter with common enable (3-state)
F367	Hex buffer/driver with 3-state output
* **F368**	Hex inverter, 4-bit and 2-bit (3-state)
F373	Octal 3-state D-latch with common enable
F374	Octal 3-state positive-edge-triggered D register
F377	Octal D-type flip-flops with clock enable
F378	Hex parallel D register with enable
F379	Quad D-type flip-flops with enable
F381	Arithmetic logic unit/function generator
* **F382**	4-bit arithmetic logic unit
* **F385**	Quad serial adder/subtractor
* **F393**	Dual 4-bit binary ripple counter
* **F395**	4-bit cascadable shift register (3-state)
* **F398**	Quad 2-port register with true and complementary outputs
F399	Quad 2-port register
* **F412**	Multi-mode buffered latch (non-inverted 3-state)
* **F432**	Multi-mode buffered latch (inverted 3-state)
* **F455**	Octal buffer w/parity generator checker
* **F456**	Octal buffer w/parity generator checker
F521	8-bit identity comparator
F524	8-bit registered comparator
F533	Octal transparent latch
* **F534**	Octal D flip-flop (3-state)
* **F537**	1-of-10 decoder (3-state)
F538	1-of-8 decoder

* F539	Dual 1-of-4 decoder (3-state)
* F540	Octal inverting buffer (3-state) broadside pinout 'F240'
* F541	Octal inverting buffer (3-state) broadside pinout 'F244'
* F544	Octal transparent bidirectional latch
* F545	Octal bidirectional transceiver (3-state I/O)
F547	Octal decoder/demultiplexer
* F548	Octal decoder/demultiplexer with acknowledge
* F550	Octal registered transceiver with status flags (non-inverted 3-state)
* F551	Octal registered transceiver with status flags (inverted 3-state)
F552	Octal registered transceiver with parity and flags
* F563	Octal transparent latch (3-state)
* F564	Octal D flip-flop (3-state)
* F573	Octal transparent latch (3-state)
F574	Octal D-type flip-flop with 3-state output
F579	8-bit bidirectional binary counter with 3-state output
* F582	4-bit BCD arithmetic logic unit
* F583	4-bit BCD adder
* F588	Octal bidirectional transceiver with IEEE-488 termination resisters (3-state I/O)
* F595	8-bit shift registers with output latches (3-state)
* F597	8-bit shift registers with input latches (3-state)

* F598	8-bit shift registers with input latches (3-state)
* F604	Dual 8-bit latch (3-state)
* F605	Dual 8-bit latch (O.C.)
* F620	Octal bus transceiver inverting (3-state)
* F621	Octal bus transceiver inverting (O.C.)
F622	Octal bus transceiver with open collector output
* F623	Octal bus transceiver non-inverting (3-state)
* F640	Octal bus transceiver inverting (3-state)
* F641	Octal bus transceiver (O.C.)
* F642	Octal bus transceiver, inverting (O.C.)
F646	Octal transceiver/register with 3-state output
* F647	Octal transceiver and register, NINV (O.C.)
F648	Octal transceiver/register with 3-state output
* F651	Octal bus transceiver and register, INV (3-state)
* F652	Octal bus transceiver and register, NINV (3-state)
* F653	Octal bus transceiver and register, INV (O.C.)
* F654	Octal bus transceiver and register, NINV (O.C.)
* F655a	Octal inverting buffer with parity generator-checker (3-state)
* F656a	Octal buffer with parity generator-checker (3-state)
F657	Octal bidirectional transceiver with 8-bit parity generator/checker and 3-state output
* F670	4 x 4 register file (3-state)
* F674	16-bit shift register parallel-in/serial-in/serial-out (3-state)
* F676	16-bit serial/parallel-in serial-out (3-state)
* F732	Quad data multiplexer (inverting, 3-state)
* F733	Quad data multiplexer (non-inverting, 3-state)

* F755	Octal mailbox register with ready flag (3-state)
* F779	8-bit up/down counter, common I/O (3-state)
* F786	4-input asynchronous bus arbitor
* F804	Hex 2-input NAND driver
* F805	Hex 2-input NOR driver
* F827	10-bit buffer, NINV (3-state)
* F828	10-bit buffer, INV (3-state)
* F841	10-bit latch, NINV (3-state)
* F842	10-bit latch, INV (3-state)
* F844	9-bit latch, INV (3-state)
* F846	8-bit latch, INV (3-state)
* F861	10-bit transceiver, NINV (3-state)
* F862	10-bit transceiver, INV (3-state)
* F863	9-bit transceiver, NINV (3-state)
* F864	9-bit transceiver, INV (3-state)
* F881	Arithmetic logic UNIX/function generator
* F882	32-bit look-ahead carry generator
* F1240	Octal buffer (3-state) light load 'F240'
* F1241	Octal buffer (3-state) light load 'F241'
* F1242	Quad transceiver, INV (3-state) light load 'F242'
* F1243	Quad transceiver, INV (3-state) light load 'F243'
* F1244	Octal buffer (3-state) light load 'F244'
* F1245	Octal bus transceiver (3-state) light load 'F245'
* F3037	Quad 2-input 30 ohm Xmission line driver, NINV
* F3038	Quad 2-input 30 ohm Xmission line driver, NINV (O.C.)

* **F3040**	Dual 4-input 30 ohm transmission line driver
* **F30240**	Octal 30 ohm transmission line/backplane driver INV (O.C.)
* **F30244**	Octal 30 ohm transmission line/backplane driver NINV (O.C.)
* **F30245**	Octal 30 ohm transmission line/backplane transceiver NINV
* **F30640**	Octal 30 ohm transmission line/backplane transceiver INV

Application Notes

DELAY_EQ Property

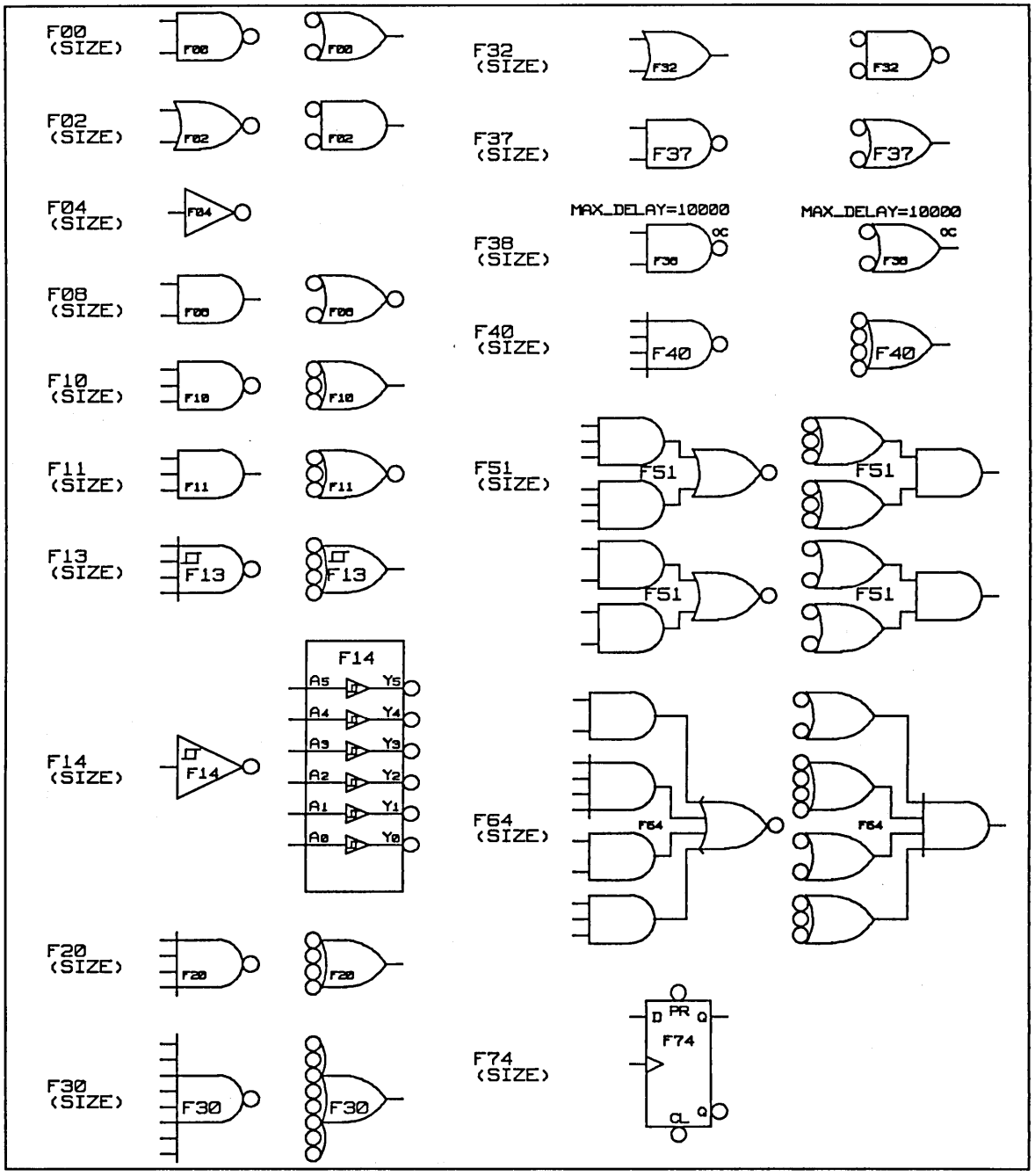
The FAST library supports specification of a DELAY_EQ property on the simulation model primitives.

Use the DELAY_EQ property on the model along with the USER_EXPRESSION directive in the *simulate.cmd* file to adjust primitive delay times for various test conditions. By combining the property and the directive, you avoid changing the delay values directly on the sim models in the library and eliminate the need to recompile the design each time the delay is changed.

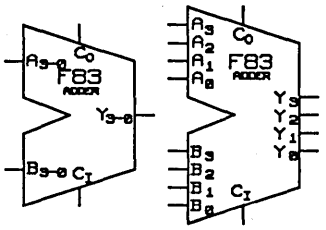
For example, to increase the delay on the simulation models for the library by a factor of two, include the following USER_EXPRESSION in the *simulator.cmd* file:

```
user_expression fast, rep=`delay*2.0´;
```

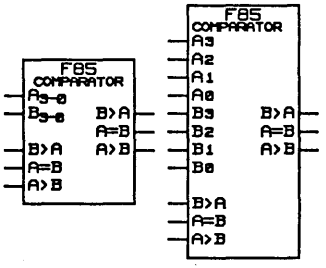
Additional information on the USER_EXPRESSION directive can be found in the "Expression Evaluator" section of the *ValidSIM Reference Manual*.


F00 (SIZE)
F02 (SIZE)
F04 (SIZE)
F08 (SIZE)
F10 (SIZE)
F11 (SIZE)
F13 (SIZE)
F14 (SIZE)
F20 (SIZE)
F30 (SIZE)
F14
A5 A4 A3 A2 A1 A0
Y5 Y4 Y3 Y2 Y1 Y0
F32 (SIZE)
F37 (SIZE)
F38 (SIZE)
F40 (SIZE)
MAX_DELAY=10000
F51 (SIZE)
F64 (SIZE)
F74 (SIZE)
D PR Q
F74
CL Q

F83

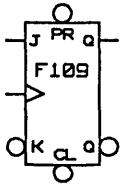


F85

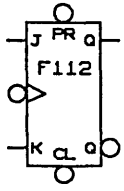


F86 (SIZE)

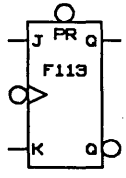
F109 (SIZE)



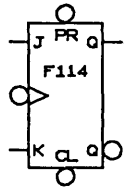
F112 (SIZE)



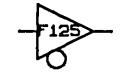
F113 (SIZE)



F114 (SIZE)



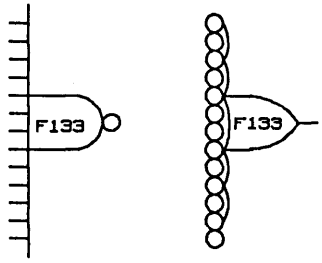
F125 (SIZE)



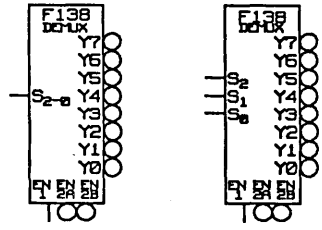
F126 (SIZE)

F132 (SIZE)

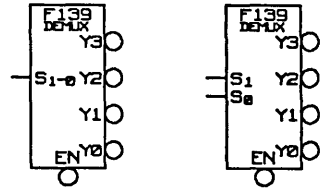
F133 (SIZE)



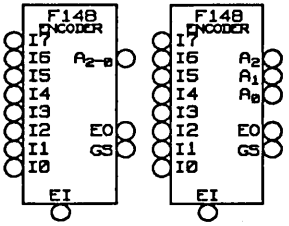
F138



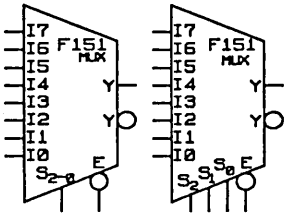
F139



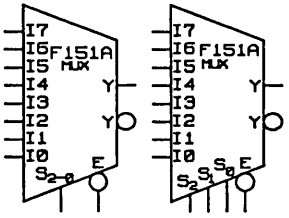
F148



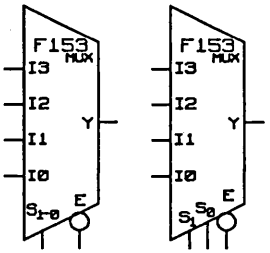
F151
(SIZE)



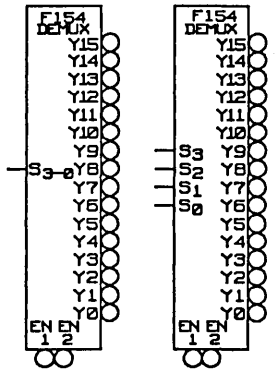
F151A
(SIZE)



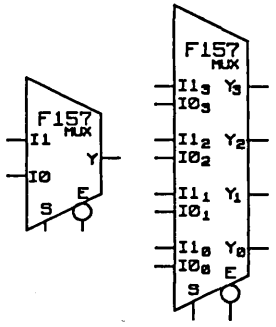
F153
(SIZE)



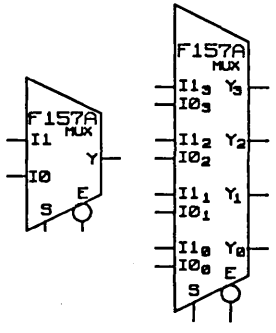
F154



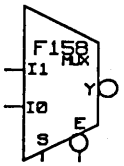
F157
(SIZE)

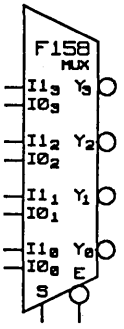


F157A
(SIZE)

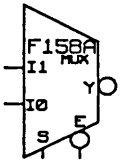


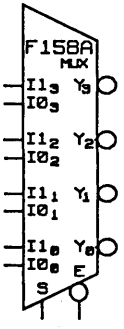
F158 (SIZE)



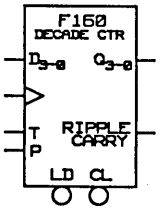


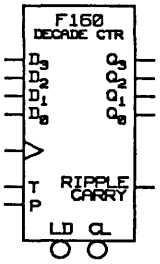
F158A (SIZE)



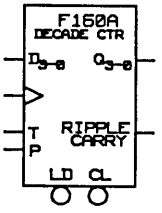


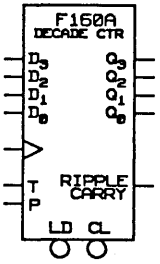
F160



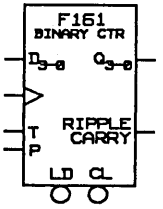


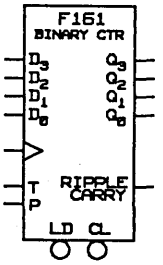
F160A



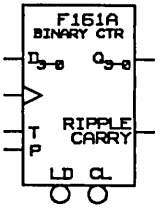


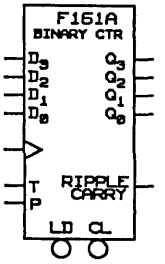
F161



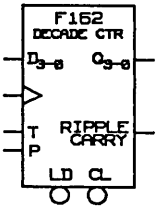


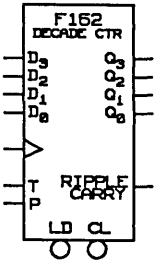
F161A



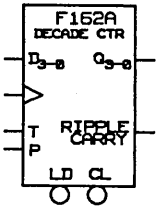


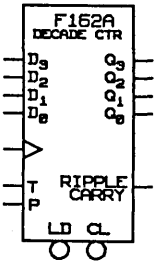
F162



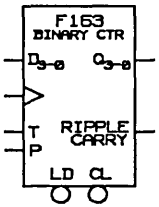


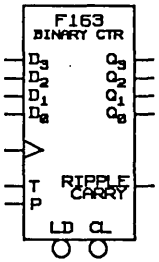
F162A



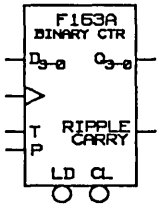


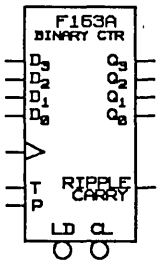
F163



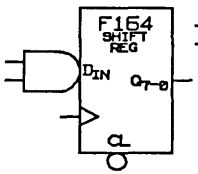


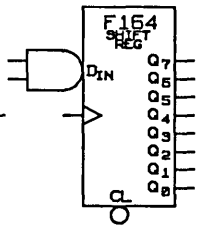
F163A



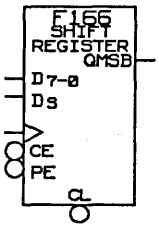


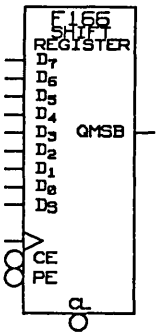
F164



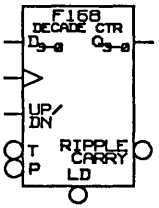


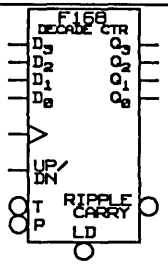
F166



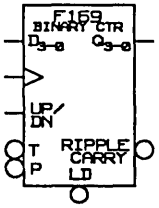


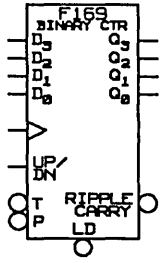
F168



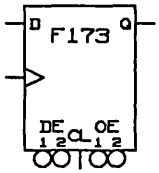


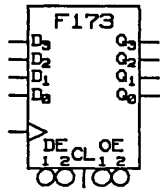
F169



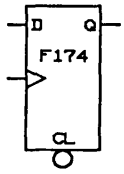


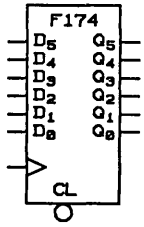
F173 (SIZE)



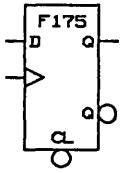


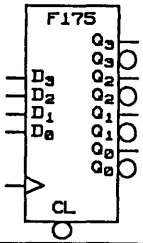
F174 (SIZE)



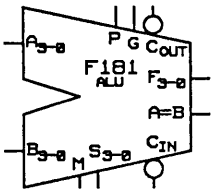


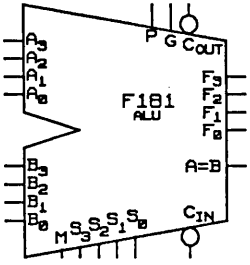
F175 (SIZE)



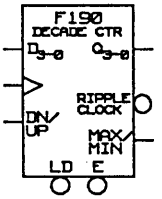


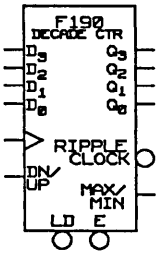
F181



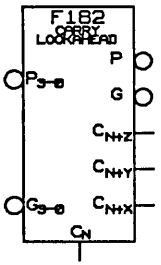


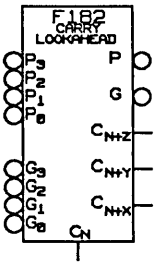
F190



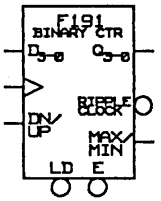


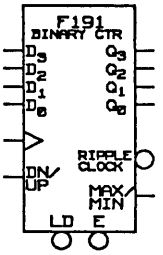
F182



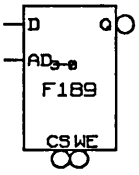


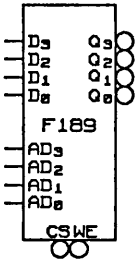
F191



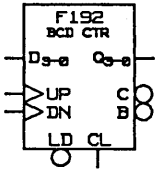


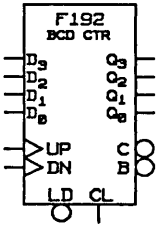
F189
(SIZE)



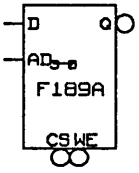


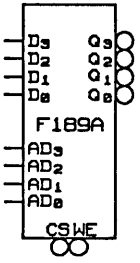
F192



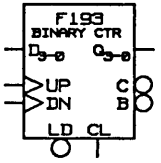


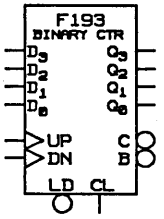
F189A
(SIZE)

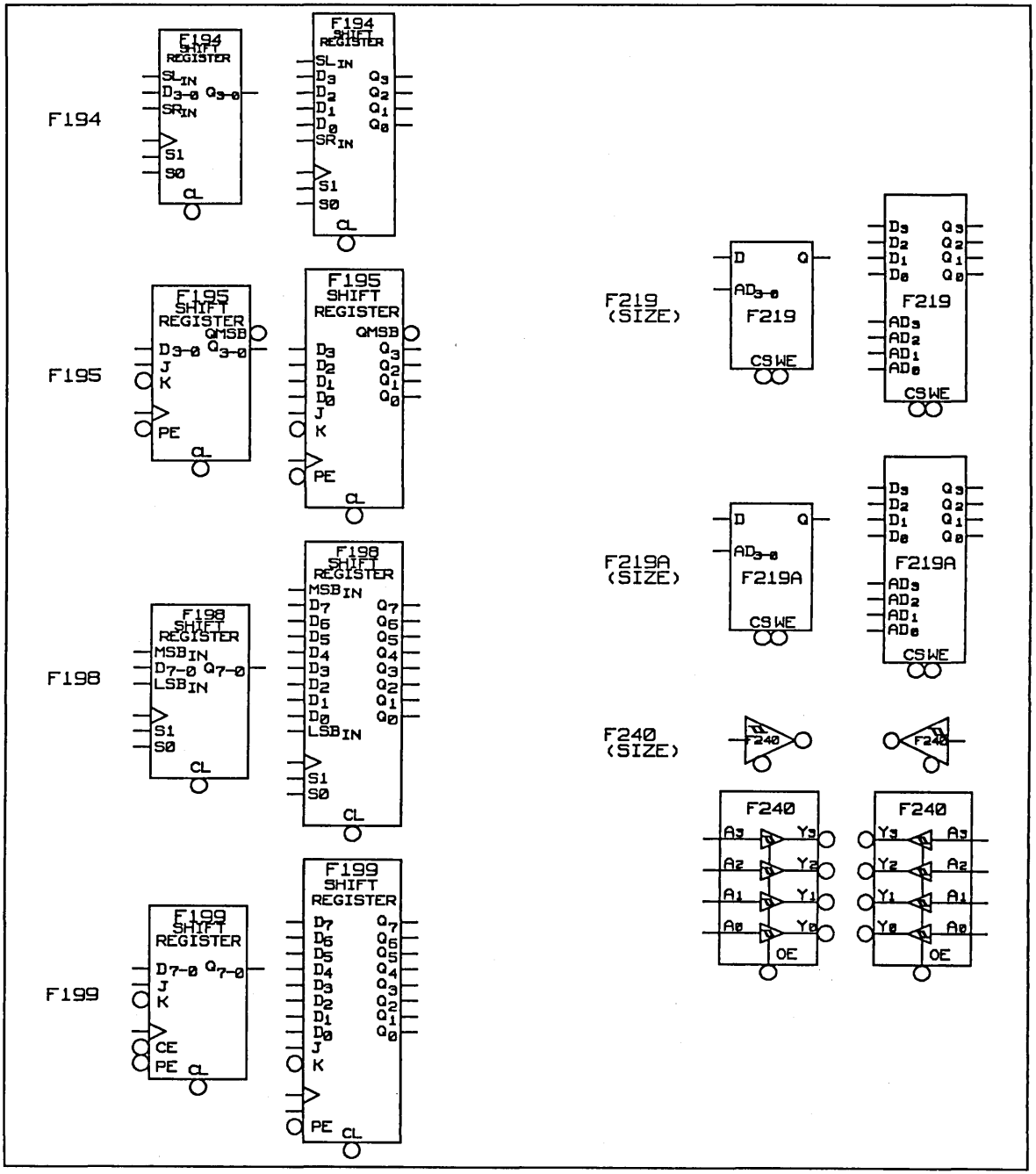


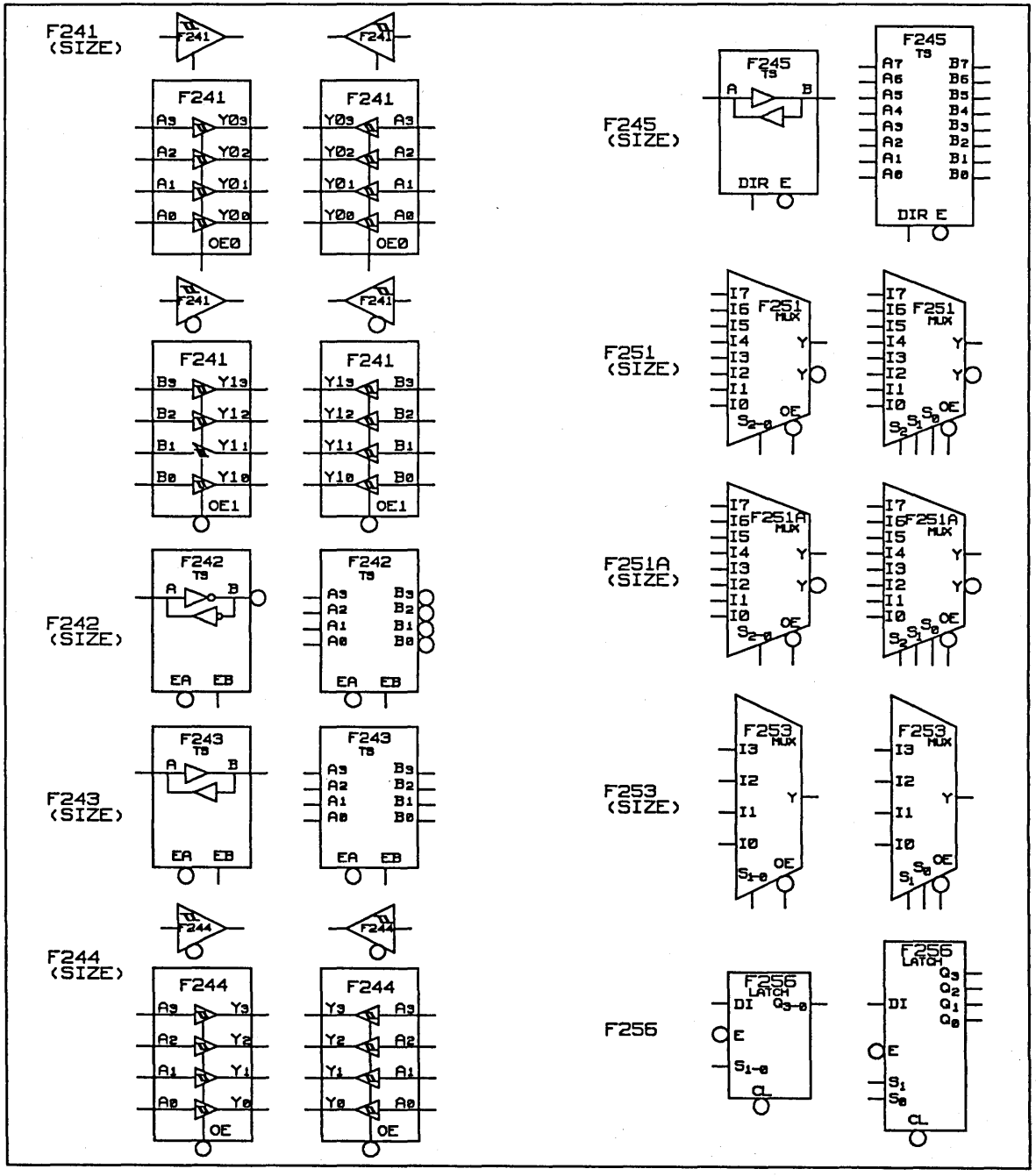


F193

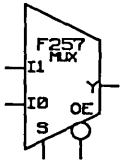


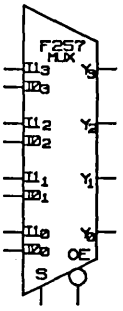



F194
F194 SHIFT REGISTER
SLIN
D3-0
Q3-0
SRIN
S1
S0
CL
F194 SHIFT REGISTER
SLIN
D3
D2
D1
D0
SRIN
Q3
Q2
Q1
Q0
F195
F195 SHIFT REGISTER
QMSB
D3-0
Q3-0
J
K
PE
CL
F195 SHIFT REGISTER
QMSB
F198
F198 SHIFT REGISTER
MSBIN
D7-0
Q7-0
LSBIN
F198 SHIFT REGISTER
F199
F199 SHIFT REGISTER
CE
F219
(SIZE)
D
Q
AD3-0
F219
CS WE
F219A
(SIZE)
F219A
F240
(SIZE)
F240
A3
A2
A1
A0
Y3
Y2
Y1
Y0
OE

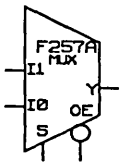

F241
(SIZE)
F241
A3 Y03
A2 Y02
A1 Y01
A0 Y00
OE0
F241
Y03 A3
Y02 A2
Y01 A1
Y00 A0
OE0
F241
B3 Y13
B2 Y12
B1 Y11
B0 Y10
OE1
F241
Y13 B3
Y12 B2
Y11 B1
Y10 B0
OE1
F242
(SIZE)
F242
TS
A B
EA EB
F242
TS
A3 B3
A2 B2
A1 B1
A0 B0
EA EB
F243
(SIZE)
F243
TS
A B
EA EB
F243
TS
A3 B3
A2 B2
A1 B1
A0 B0
EA EB
F244
(SIZE)
F244
A3 Y3
A2 Y2
A1 Y1
A0 Y0
OE
F244
Y3 A3
Y2 A2
Y1 A1
Y0 A0
OE
F245
(SIZE)
F245
TS
A B
DIR E
F245
TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR E
F251
(SIZE)
F251
MUX
I7
I6
I5
I4
I3
I2
I1
I0
Y
Y
OE
S2-0
F251
MUX
I7
I6
I5
I4
I3
I2
I1
I0
Y
Y
OE
S2 S1 S0
F251A
(SIZE)
F251A
MUX
I7
I6
I5
I4
I3
I2
I1
I0
Y
Y
OE
S2-0
F251A
MUX
I7
I6
I5
I4
I3
I2
I1
I0
Y
Y
OE
S2 S1 S0
F253
(SIZE)
F253
MUX
I3
I2
I1
I0
Y
OE
S1-0
F253
MUX
I3
I2
I1
I0
Y
OE
S0
S1
F256
F256
LATCH
DI Q3-0
E
S1-0
CL
F256
LATCH
DI
Q3
Q2
Q1
Q0
E
S1
S0
CL

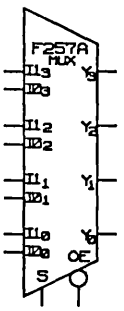
F257
(SIZE)



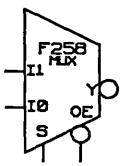


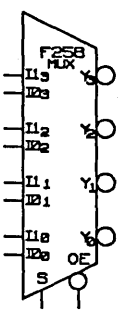
F257A
(SIZE)



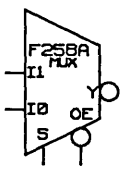


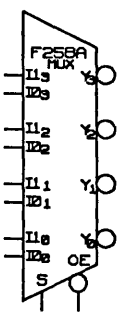
F258
(SIZE)



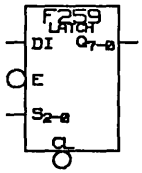


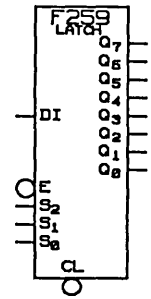
F258A
(SIZE)



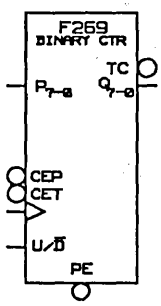


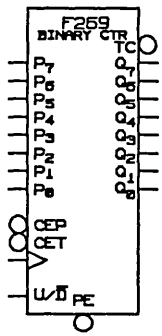
F259



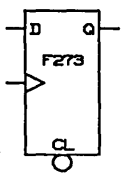


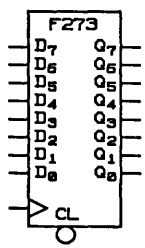
F269



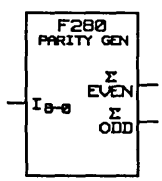


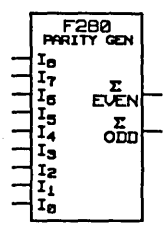
F273
(SIZE)



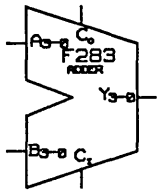


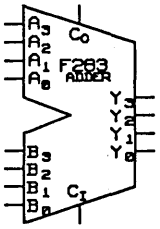
F280



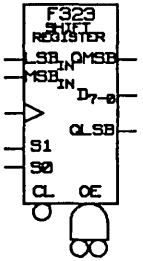


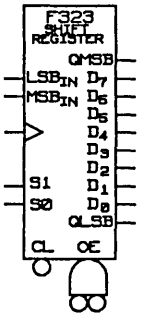
F283



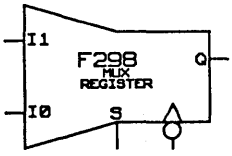


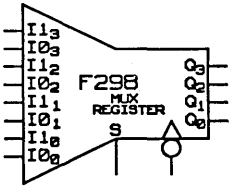
F323



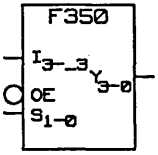


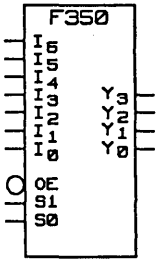
F298
(SIZE)



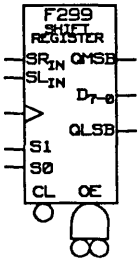


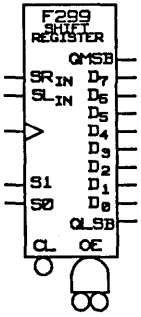
F350



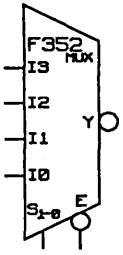


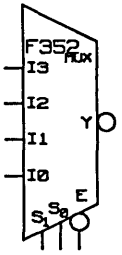
F299



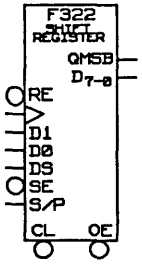


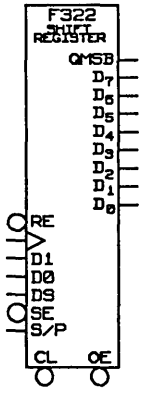
F352
(SIZE)



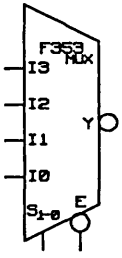


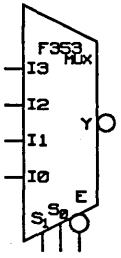
F322

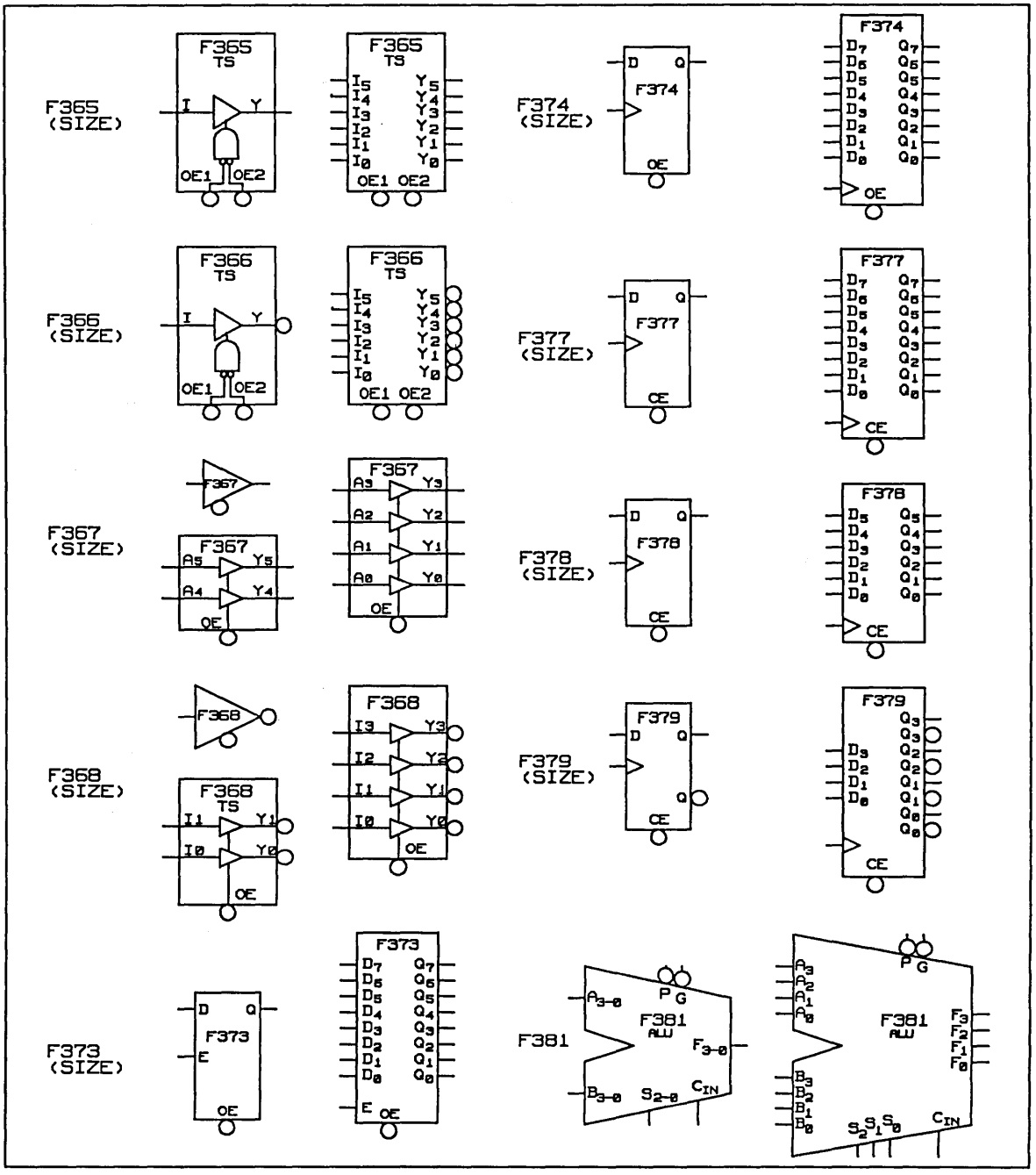


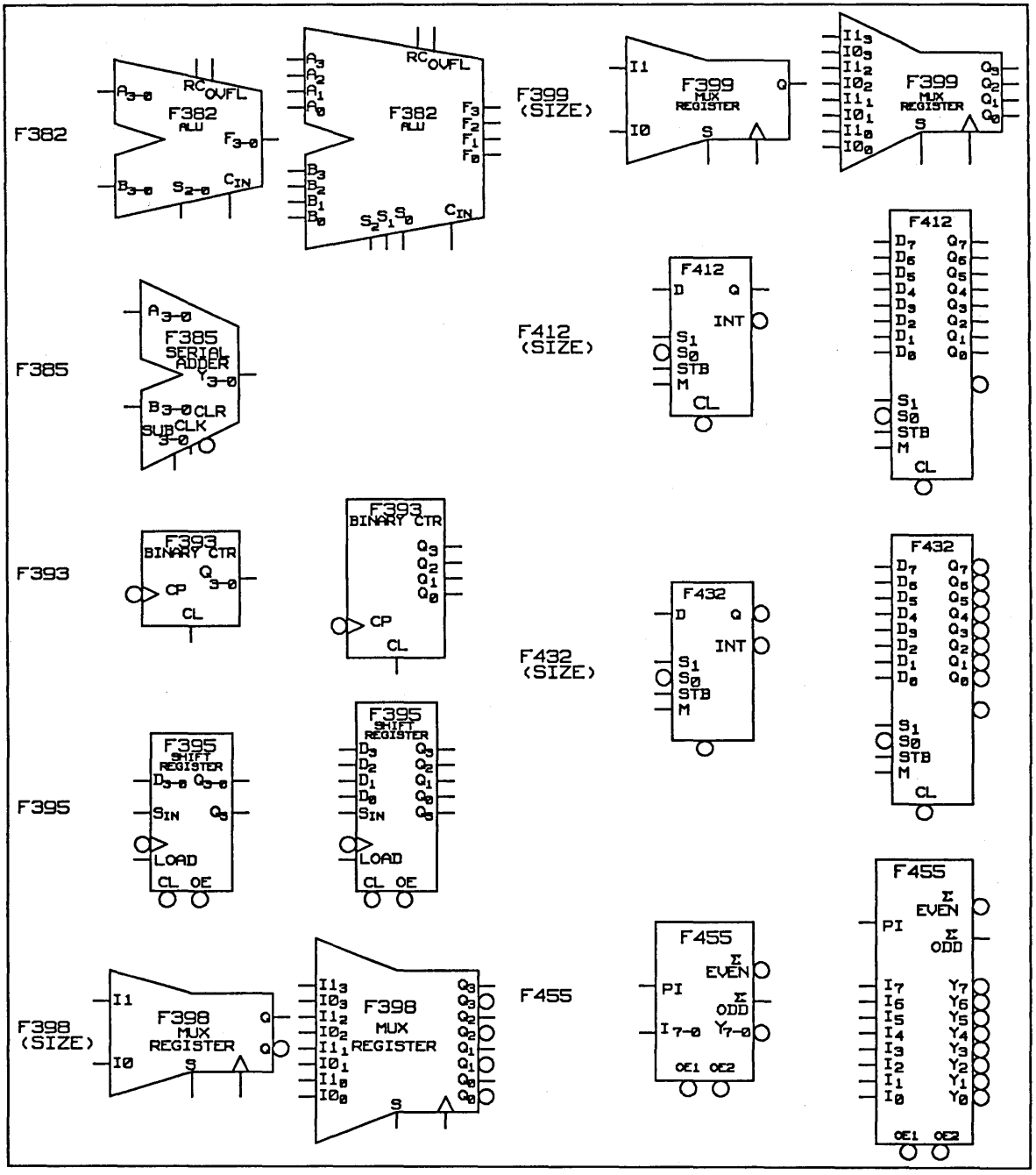


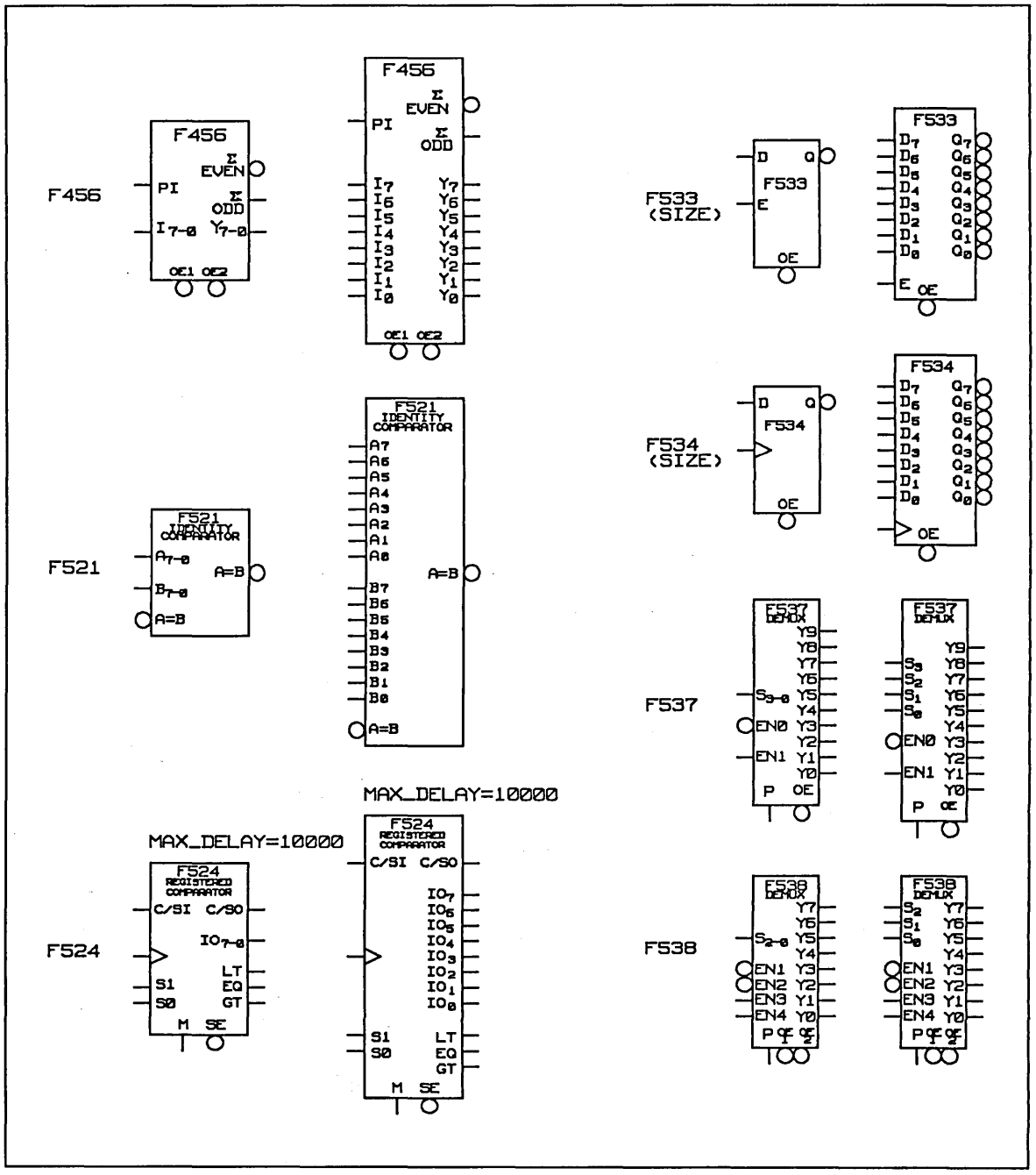
F353
(SIZE)

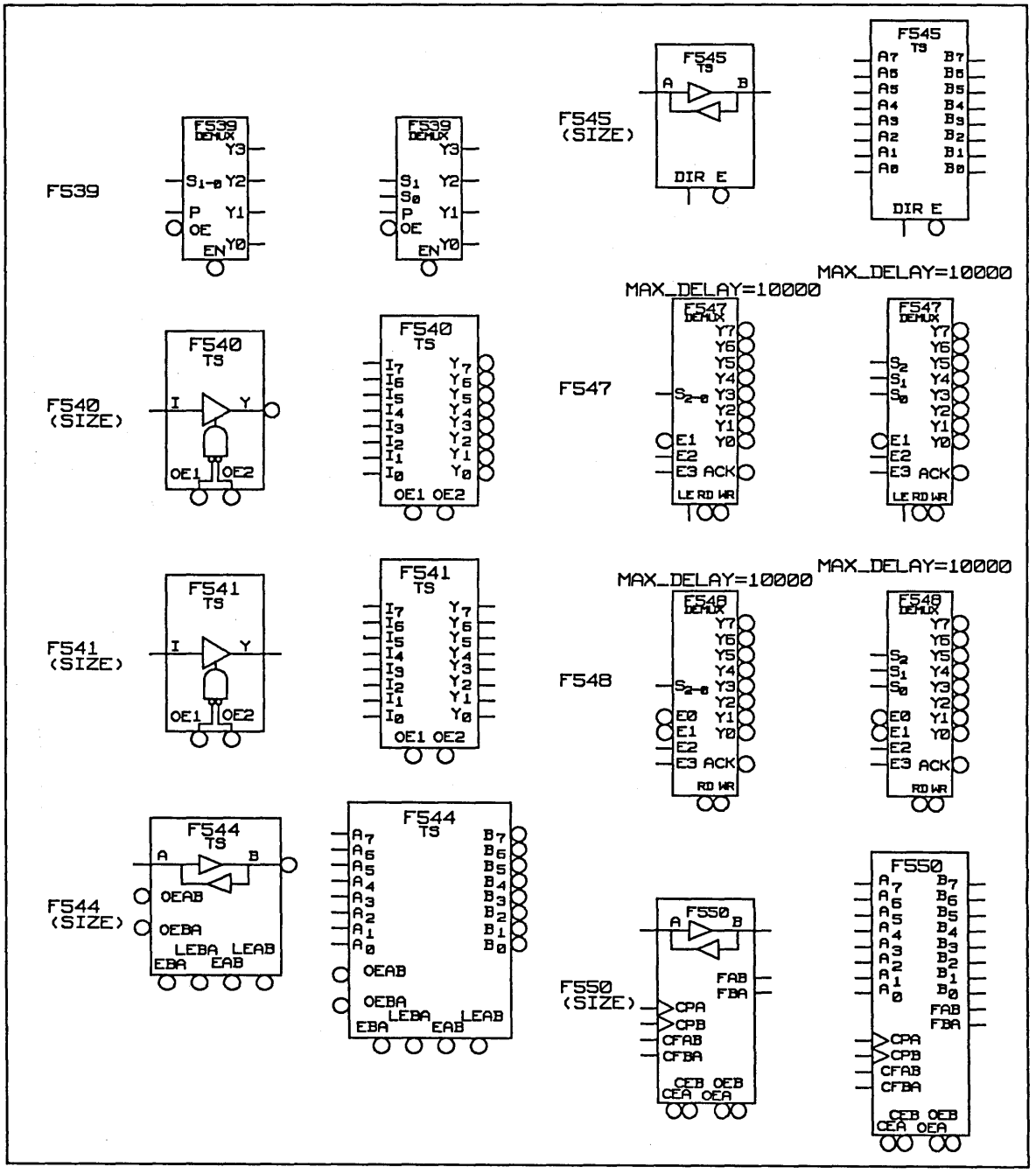


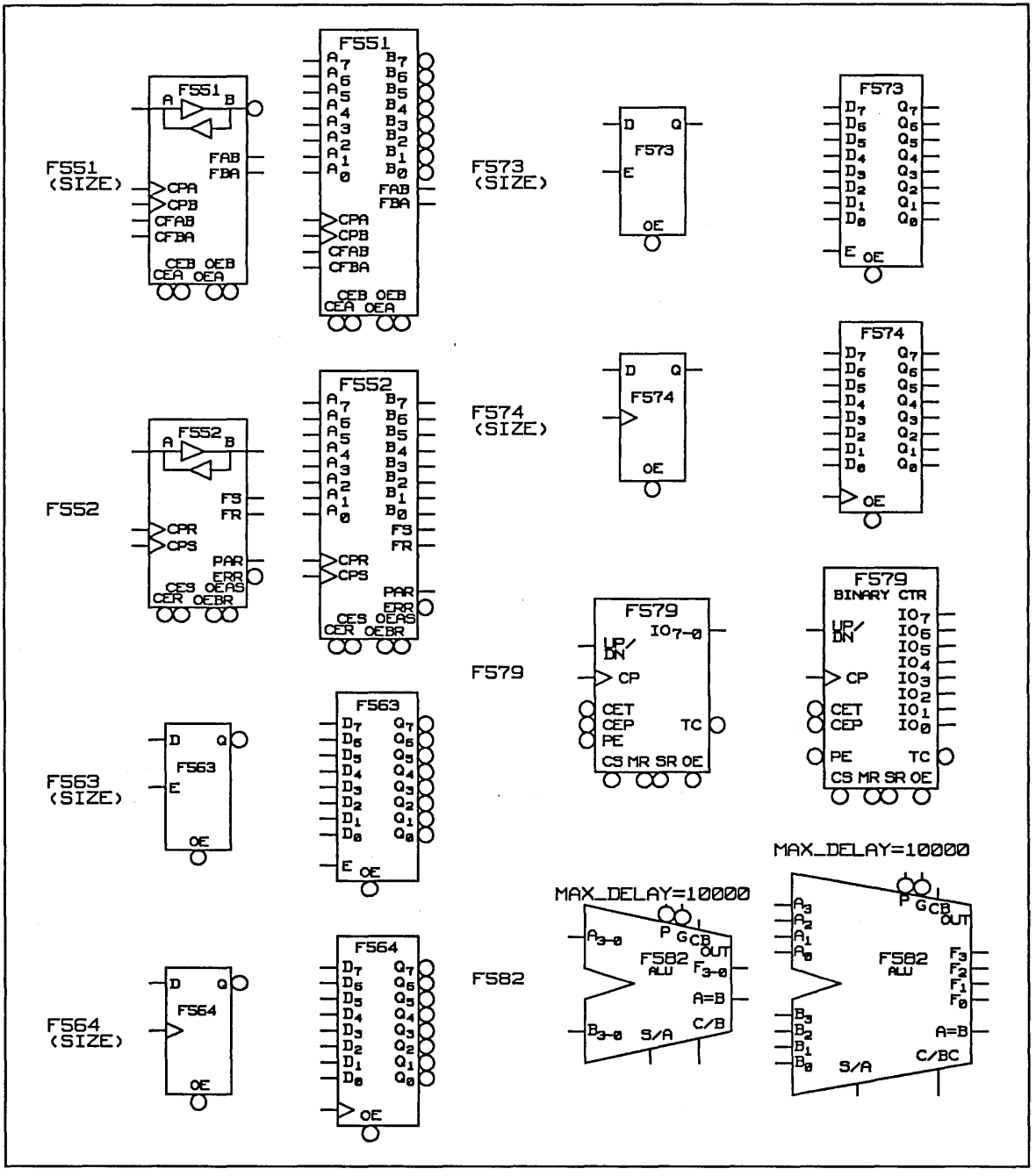


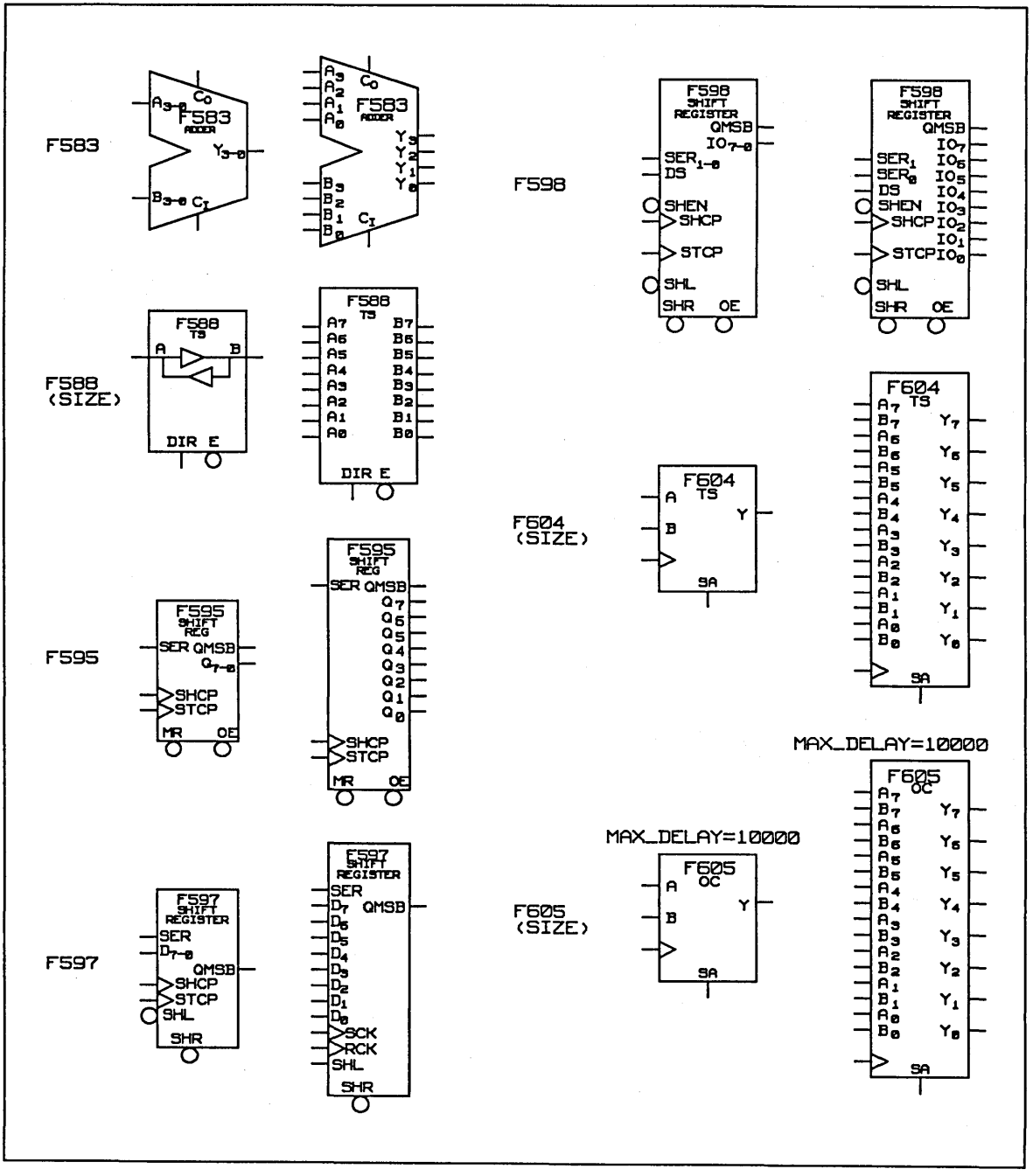

F365 (SIZE)
F365 TS
I
Y
OE1
OE2
F365 TS
I5 I4 I3 I2 I1 I0
Y5 Y4 Y3 Y2 Y1 Y0
OE1 OE2
F366 (SIZE)
F366 TS
F367 (SIZE)
F367
A5 A4
Y5 Y4
OE
A3 A2 A1 A0
Y3 Y2 Y1 Y0
F368 (SIZE)
F368
F368 TS
I1 I0
Y1 Y0
F373 (SIZE)
F373
D Q
E
F374 (SIZE)
F374
F377 (SIZE)
F377
CE
F378 (SIZE)
F378
F379 (SIZE)
F379
F381
A3-0
B3-0
S2-0
CIN
F3-0
P G
ALU

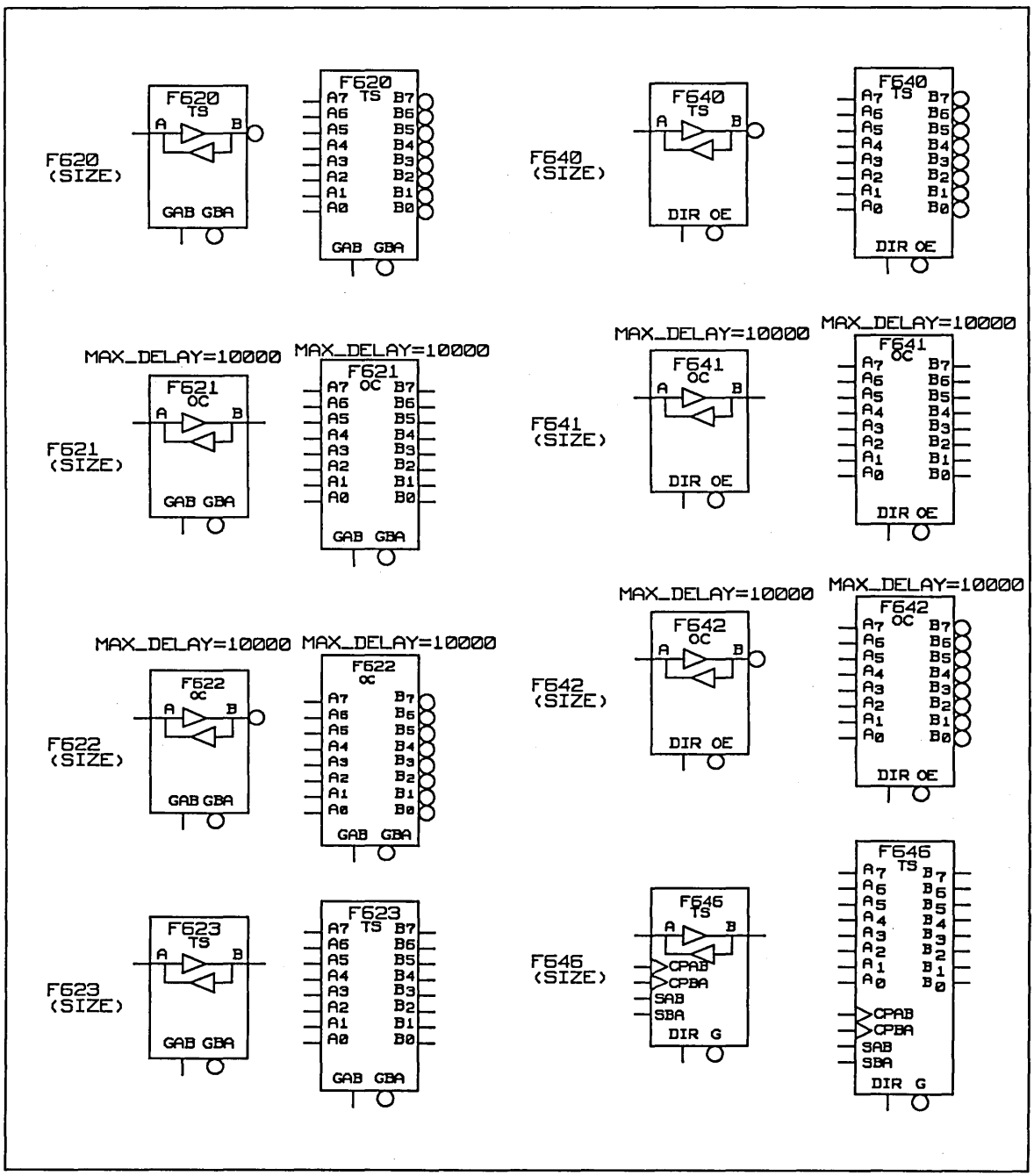

F382
F382 ALU
F399 (SIZE)
F399 MUX REGISTER
F385
F385 SERIAL ADDER
F412 (SIZE)
F412
F393
F393 BINARY CTR
F432 (SIZE)
F432
F395
F395 SHIFT REGISTER
F455
F455
F398 (SIZE)
F398 MUX REGISTER

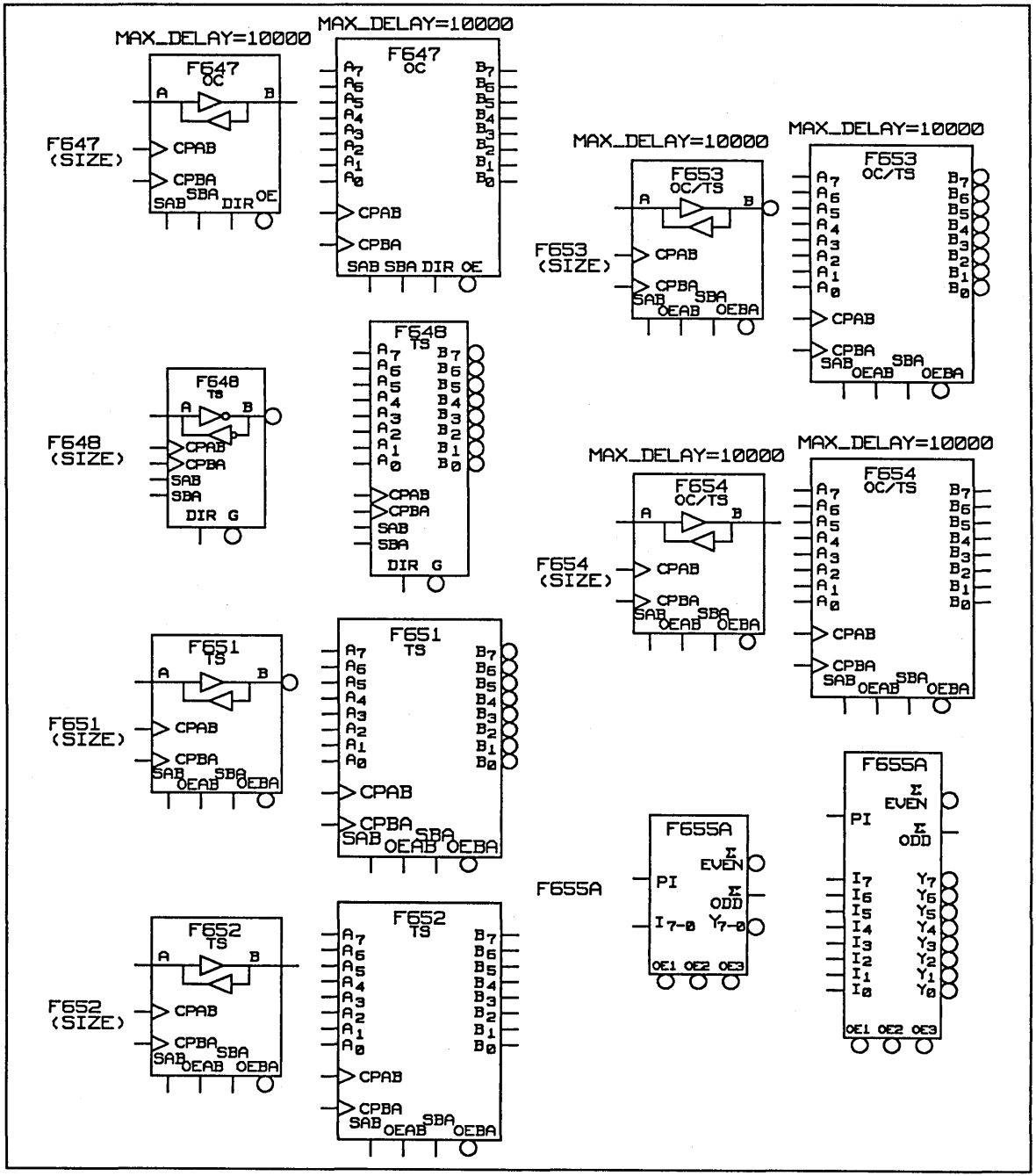

F456
F456
PI
EVEN
ODD
I7-0
Y7-0
OE1 OE2
F456
PI
EVEN
ODD
I7
I6
I5
I4
I3
I2
I1
I0
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
OE1 OE2
F533
(SIZE)
D
Q
F533
E
OE
F533
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
E OE
F534
(SIZE)
D
Q
F534
OE
F534
D7 Q7
D6 Q6
D5 Q5
D4 Q4
D3 Q3
D2 Q2
D1 Q1
D0 Q0
OE
F521
F521
IDENTITY COMPARATOR
A7-0
B7-0
A=B
A=B
F521
IDENTITY COMPARATOR
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
A=B
A=B
F537
F537
DEMUX
S3-0
EN0
EN1
P
OE
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
F537
DEMUX
S3
S2
S1
S0
EN0
EN1
P
OE
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
MAX_DELAY=10000
F524
F524
REGISTERED COMPARATOR
C/SI
C/SO
IO7-0
LT
EQ
GT
S1
S0
M
SE
MAX_DELAY=10000
F524
REGISTERED COMPARATOR
C/SI
C/SO
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
S1
S0
LT
EQ
GT
M
SE
F538
F538
DEMUX
S2-0
EN1
EN2
EN3
EN4
P
OE
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
F538
DEMUX
S2
S1
S0
EN1
EN2
EN3
EN4
P
OE
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0

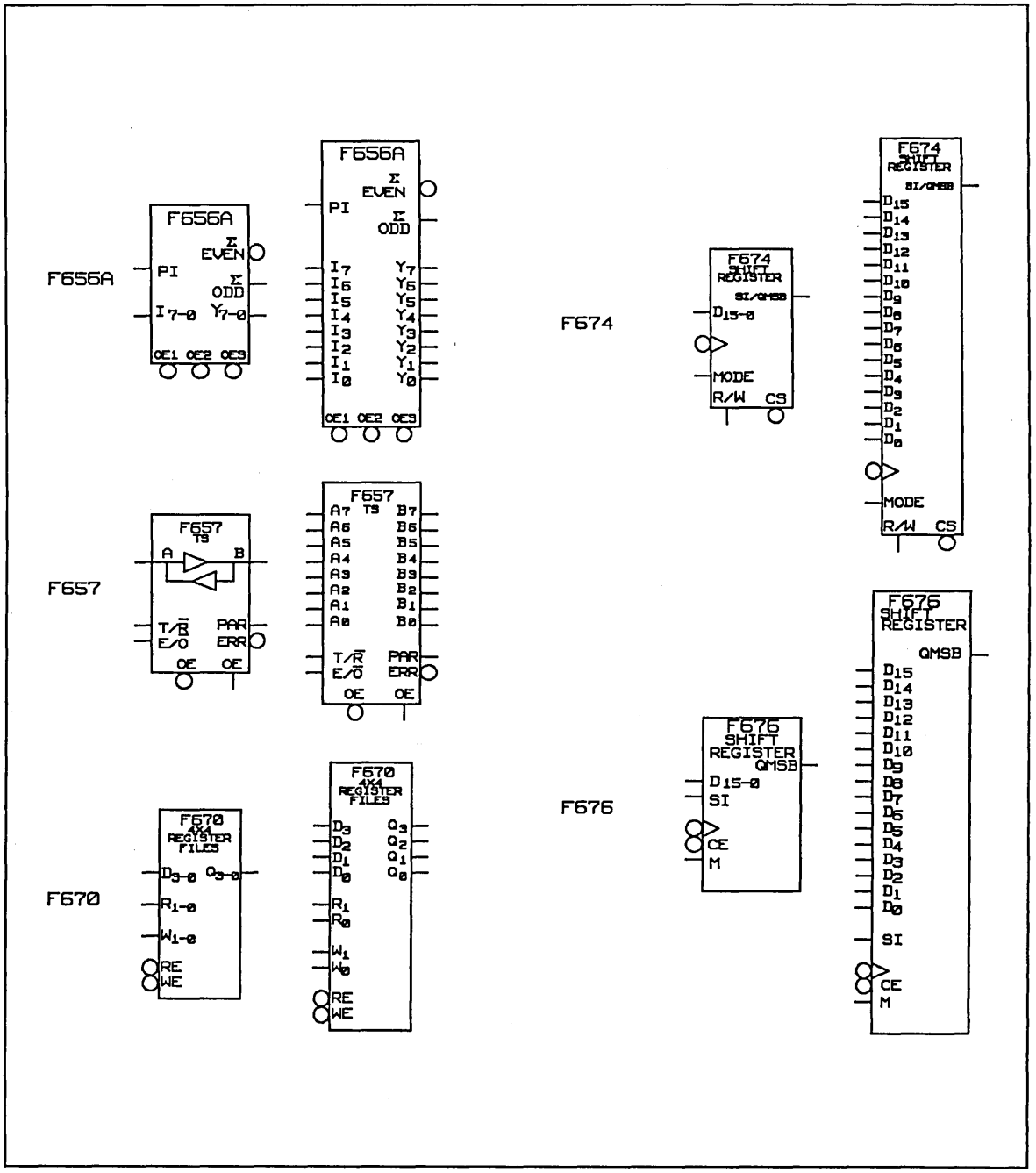

F539
F539 DEMUX
Y3
S1-0 Y2
P Y1
OE
EN Y0
F539 DEMUX
Y3
S1 Y2
S0
P Y1
OE
EN Y0
F545 (SIZE)
F545 TS
A B
DIR E
F545 TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR E
MAX_DELAY=10000
MAX_DELAY=10000
F540 (SIZE)
F540 TS
I Y
OE1 OE2
F540 TS
I7 Y7
I6 Y6
I5 Y5
I4 Y4
I3 Y3
I2 Y2
I1 Y1
I0 Y0
OE1 OE2
F547
F547 DEMUX
Y7
Y6
Y5
Y4
S2-0 Y3
Y2
Y1
E1 Y0
E2
E3 ACK
LE RD WR
F547 DEMUX
Y7
Y6
S2 Y5
S1 Y4
S0 Y3
Y2
Y1
E1 Y0
E2
E3 ACK
LE RD WR
MAX_DELAY=10000
MAX_DELAY=10000
F541 (SIZE)
F541 TS
I Y
OE1 OE2
F541 TS
I7 Y7
I6 Y6
I5 Y5
I4 Y4
I3 Y3
I2 Y2
I1 Y1
I0 Y0
OE1 OE2
F548
F548 DEMUX
Y7
Y6
Y5
Y4
S2-0 Y3
Y2
E0 Y1
E1 Y0
E2
E3 ACK
RD WR
F548 DEMUX
Y7
Y6
S2 Y5
S1 Y4
S0 Y3
Y2
E0 Y1
E1 Y0
E2
E3 ACK
RD WR
F544 (SIZE)
F544 TS
A B
OEAB
OEBA
LEBA LEAB
EBA EAB
F544 TS
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
OEAB
OEBA
LEBA LEAB
EBA EAB
F550 (SIZE)
F550
A B
FAB
FBA
CPA
CPB
CFAB
CFBA
CEB OEB
CEA OEA
F550
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
FAB
FBA
CPA
CPB
CFAB
CFBA
CEB OEB
CEA OEA

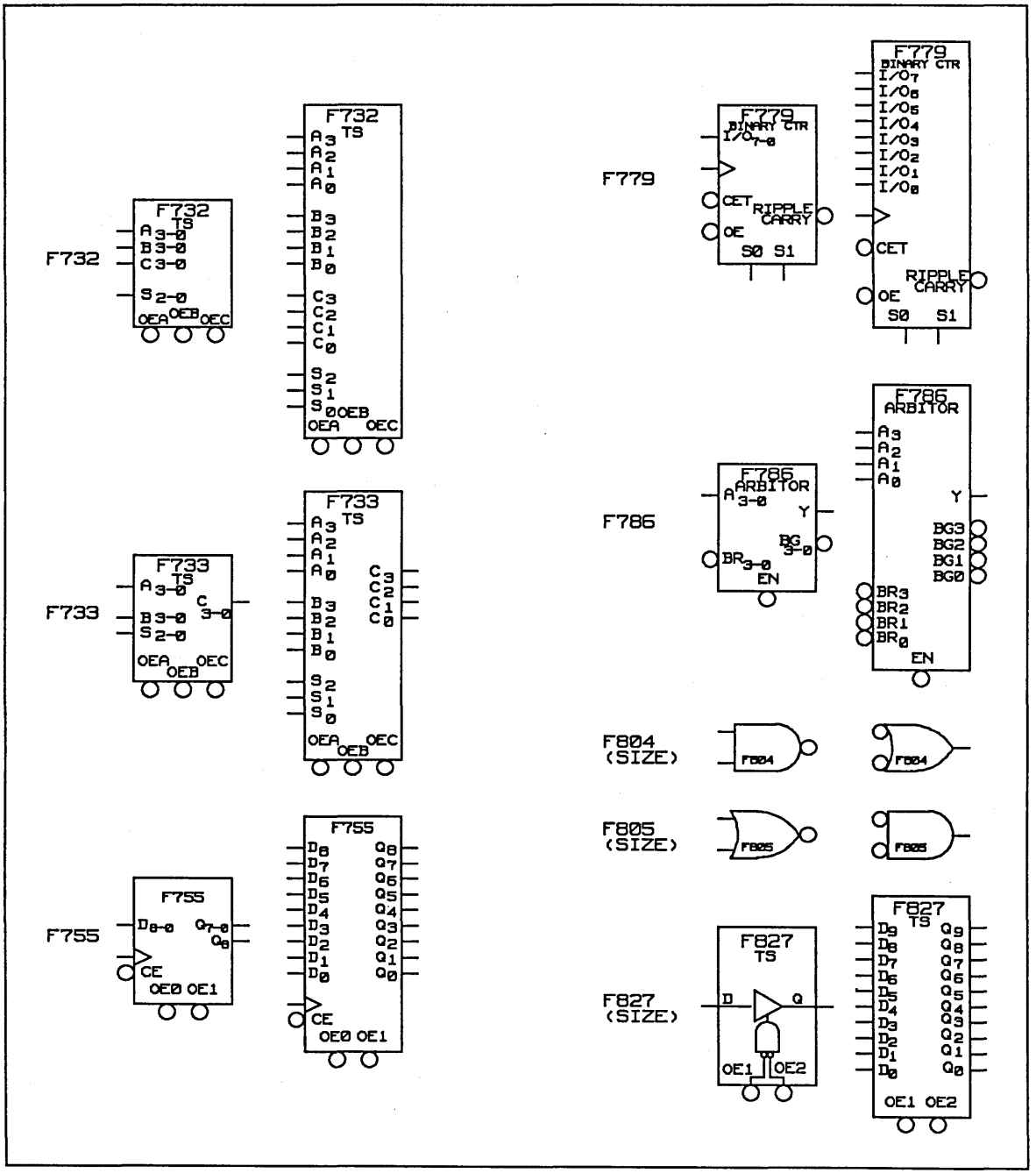

F551
(SIZE)
F551
A
B
FAB
FBA
CPA
CPB
CFAB
CFBA
CEB OEB
CEA OEA
F551
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
FAB
FBA
CPA
CPB
CFAB
CFBA
CEB OEB
CEA OEA
F573
(SIZE)
D Q
F573
E
OE
F573
D7 D6 D5 D4 D3 D2 D1 D0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E OE
F552
F552
A
B
FS
FR
CPR
CPS
PAR
ERR
CES OEAS
CER OEBR
F552
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
FS
FR
CPR
CPS
PAR
ERR
CES OEAS
CER OEBR
F574
(SIZE)
D Q
F574
OE
F574
D7 D6 D5 D4 D3 D2 D1 D0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
OE
F563
(SIZE)
D Q
F563
E
OE
F563
D7 D6 D5 D4 D3 D2 D1 D0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E OE
F579
F579
IO7-0
UP/DN
CP
CET
CEP
PE
TC
CS MR SR OE
F579
BINARY CTR
IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0
UP/DN
CP
CET
CEP
PE
TC
CS MR SR OE
F564
(SIZE)
D Q
F564
OE
F564
D7 D6 D5 D4 D3 D2 D1 D0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
OE
F582
MAX_DELAY=10000
A3-0
B3-0
P G CB
OUT
F582
ALU
F3-0
A=B
S/A
C/B
MAX_DELAY=10000
A3 A2 A1 A0
B3 B2 B1 B0
P G CB
OUT
F582
ALU
F3 F2 F1 F0
A=B
S/A
C/BC

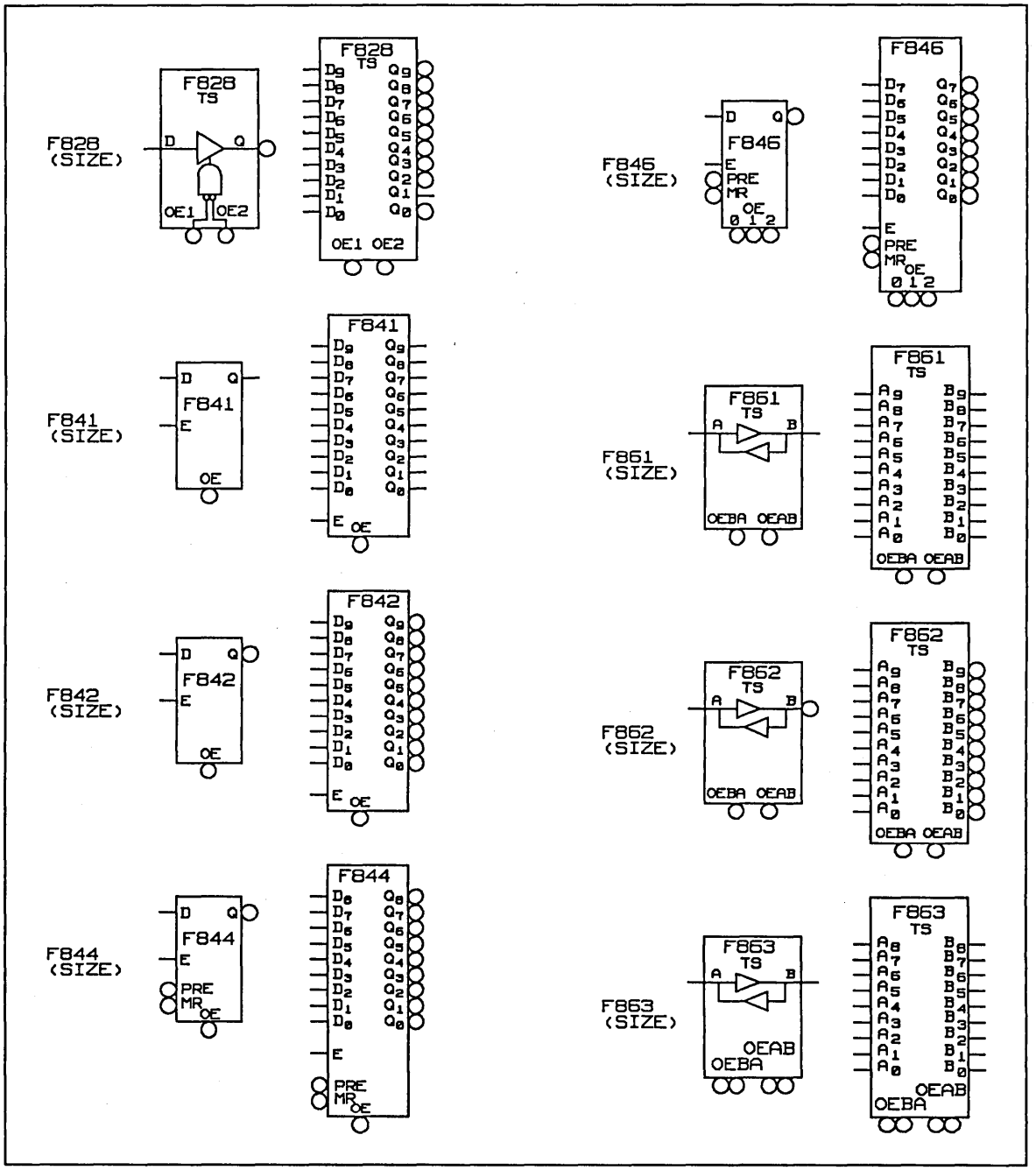

F583
F588
(SIZE)
F595
F597
F598
F604
(SIZE)
F605
(SIZE)
MAX_DELAY=10000
MAX_DELAY=10000

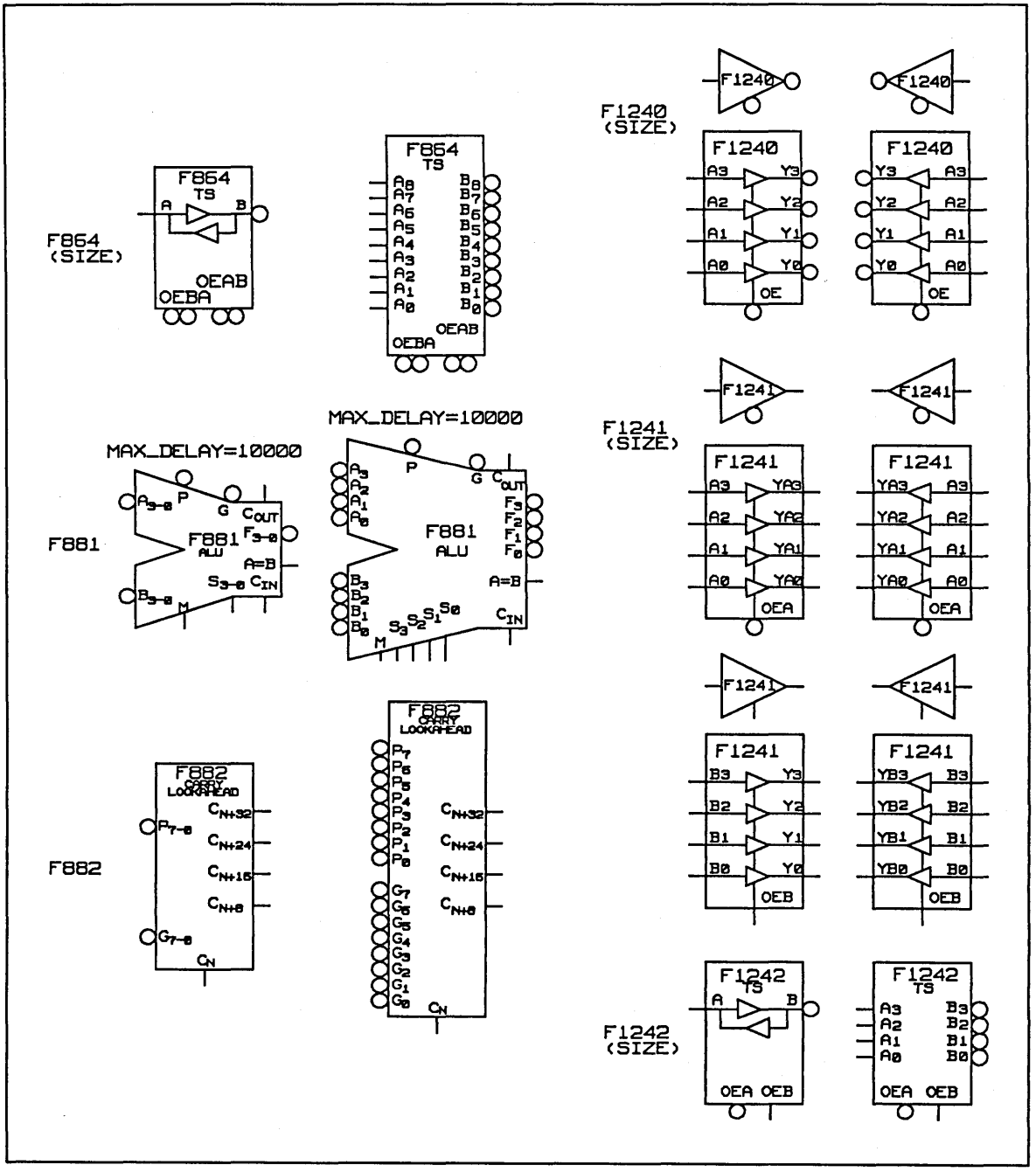

F620
(SIZE)
F620
TS
A
B
GAB GBA
F620
A7 TS B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
GAB GBA
F640
(SIZE)
F640
TS
A
B
DIR OE
F640
A7 TS B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR OE
MAX_DELAY=10000
F621
(SIZE)
F621
OC
A
B
GAB GBA
MAX_DELAY=10000
F621
A7 OC B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
GAB GBA
MAX_DELAY=10000
F641
(SIZE)
F641
OC
A
B
DIR OE
MAX_DELAY=10000
F641
A7 OC B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR OE
MAX_DELAY=10000
F622
(SIZE)
F622
OC
A
B
GAB GBA
MAX_DELAY=10000
F622
OC
A7 B7
A6 B5
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
GAB GBA
MAX_DELAY=10000
F642
(SIZE)
F642
OC
A
B
DIR OE
MAX_DELAY=10000
F642
OC
A7 B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
DIR OE
F623
(SIZE)
F623
TS
A
B
GAB GBA
F623
A7 TS B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
GAB GBA
F645
(SIZE)
F645
TS
A
B
CPAB
CPBA
SAB
SBA
DIR G
F645
A7 TS B7
A6 B6
A5 B5
A4 B4
A3 B3
A2 B2
A1 B1
A0 B0
CPAB
CPBA
SAB
SBA
DIR G

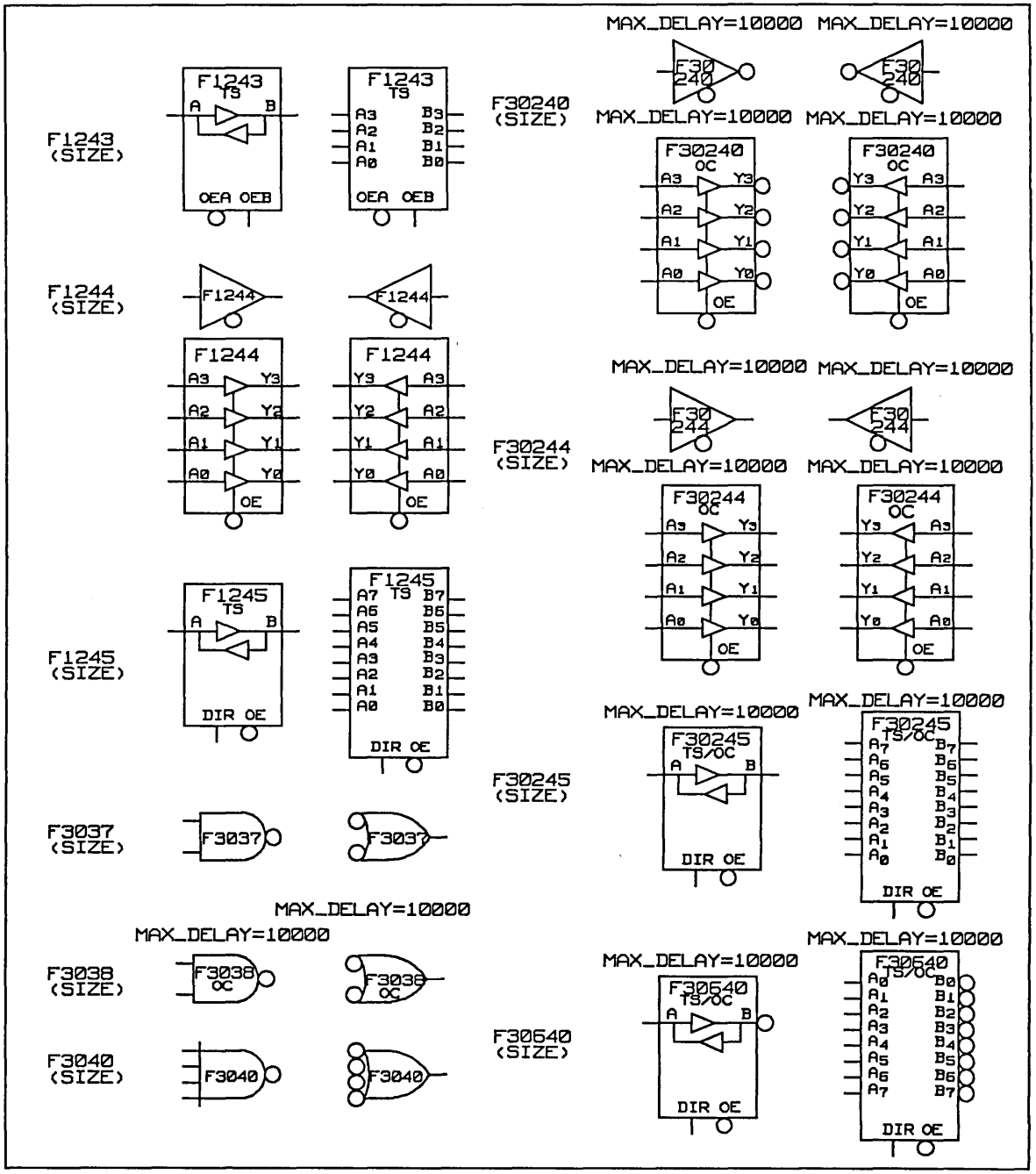

MAX_DELAY=10000
F647
OC
F647
(SIZE)
CPAB
CPBA
SAB
SBA
DIR
OE
MAX_DELAY=10000
F647
OC
CPAB
CPBA
SAB SBA DIR OE
MAX_DELAY=10000
F653
OC/TS
F653
(SIZE)
CPAB
CPBA
SAB
SBA
OEAB
OEBA
MAX_DELAY=10000
F653
OC/TS
CPAB
CPBA
SAB SBA
OEAB OEBA
F648
TS
F648
(SIZE)
CPAB
CPBA
SAB
SBA
DIR G
F648
TS
CPAB
CPBA
SAB
SBA
DIR G
MAX_DELAY=10000
F654
OC/TS
F654
(SIZE)
CPAB
CPBA
SAB
SBA
OEAB
OEBA
MAX_DELAY=10000
F654
OC/TS
CPAB
CPBA
SAB SBA
OEAB OEBA
F651
TS
F651
(SIZE)
CPAB
CPBA
SAB
SBA
OEAB
OEBA
F651
TS
CPAB
CPBA
SAB SBA
OEAB OEBA
F655A
PI
EVEN
ODD
I7-0
Y7-0
OE1 OE2 OE3
F655A
PI
EVEN
ODD
I7-0
Y7-0
OE1 OE2 OE3
F652
TS
F652
(SIZE)
CPAB
CPBA
SAB
SBA
OEAB
OEBA
F652
TS
CPAB
CPBA
SAB SBA
OEAB OEBA

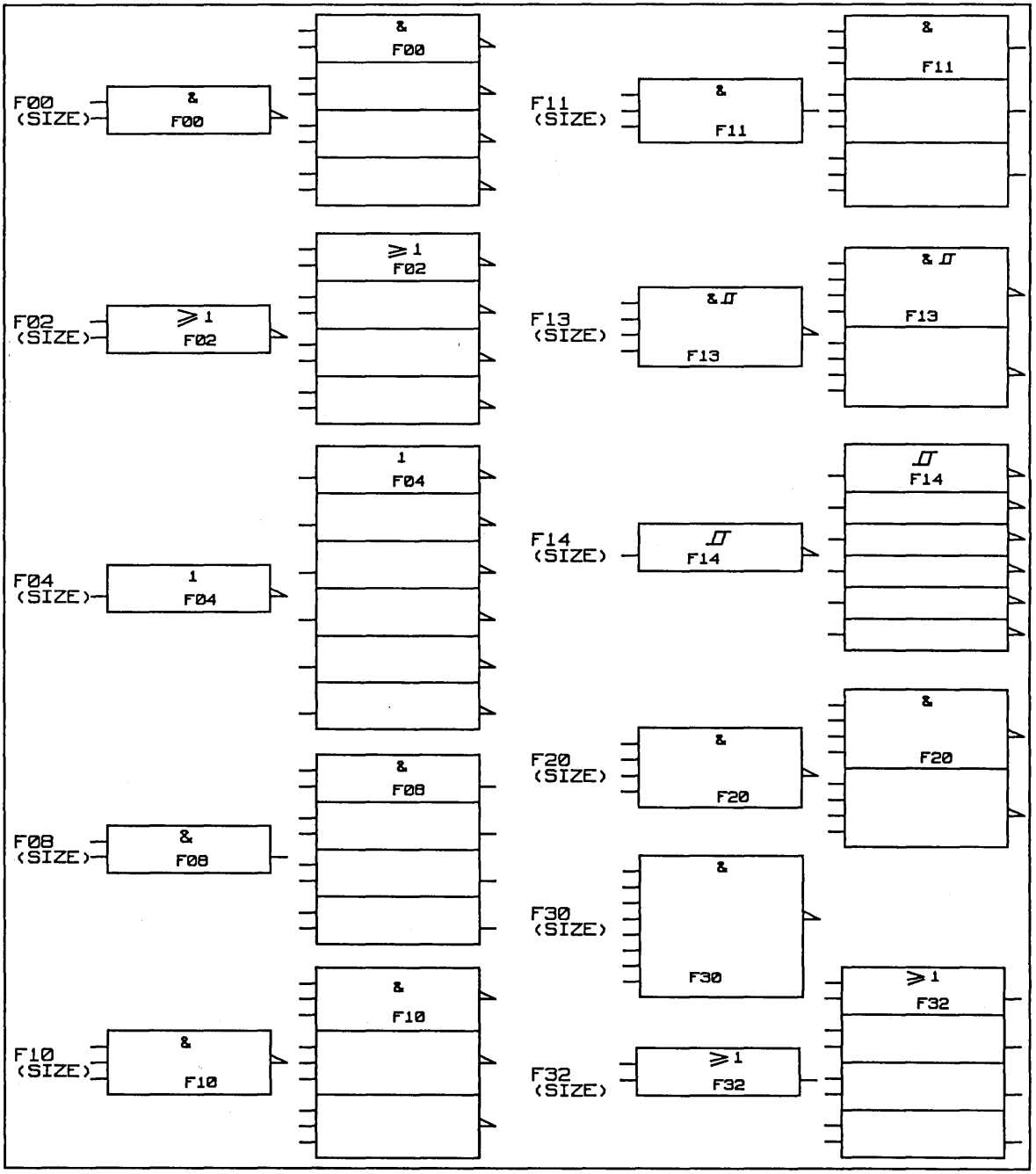

F656A
F656A
F656A
F657
F657
F657
F670
F670
F670
F674
F674
F674
F676
F676
F676

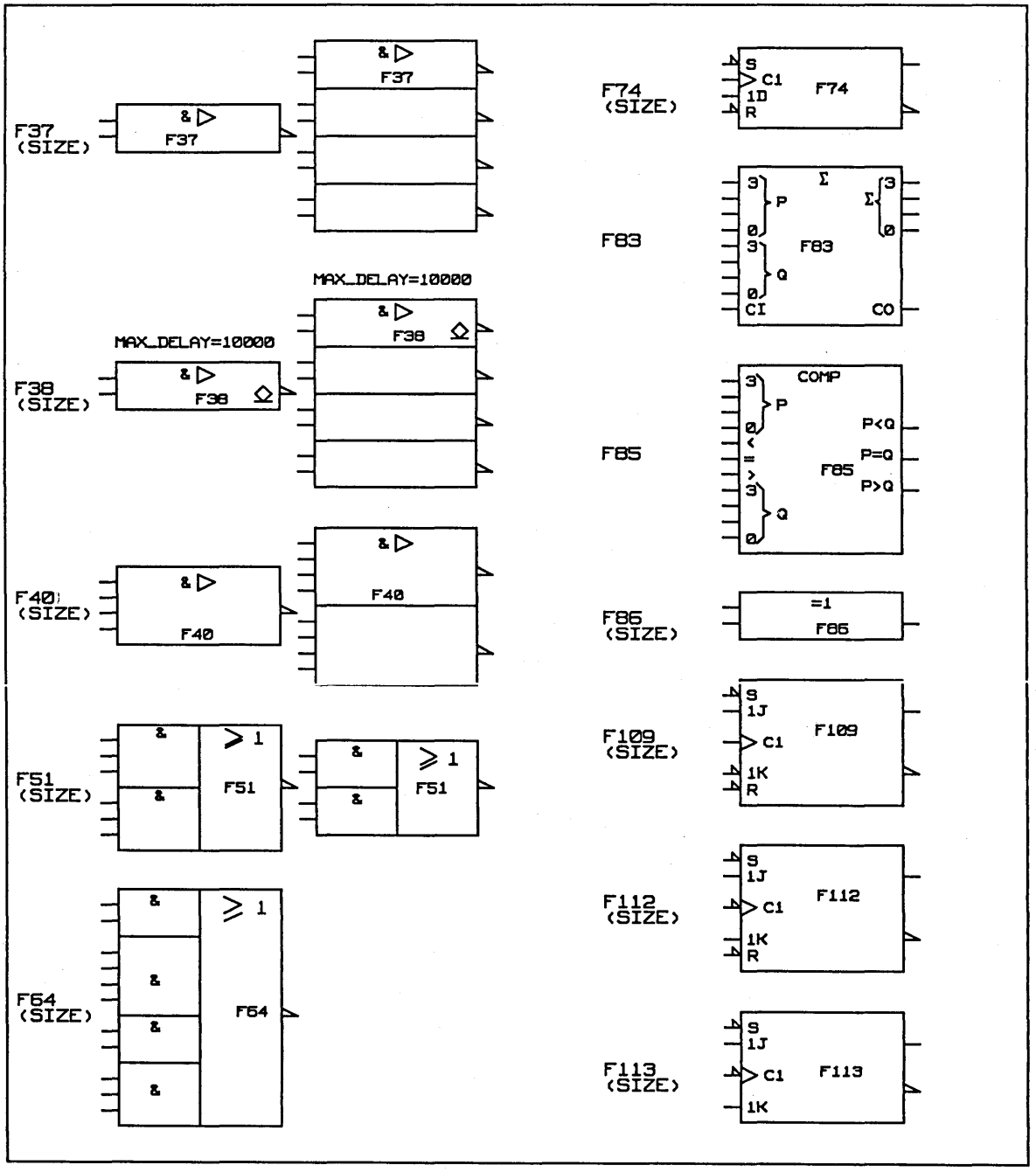

F732
F732
F733
F733
F755
F755
F779
F779
F786
F786
F804
(SIZE)
F805
(SIZE)
F827
(SIZE)
F827
TS
BINARY CTR
ARBITOR
RIPPLE CARRY

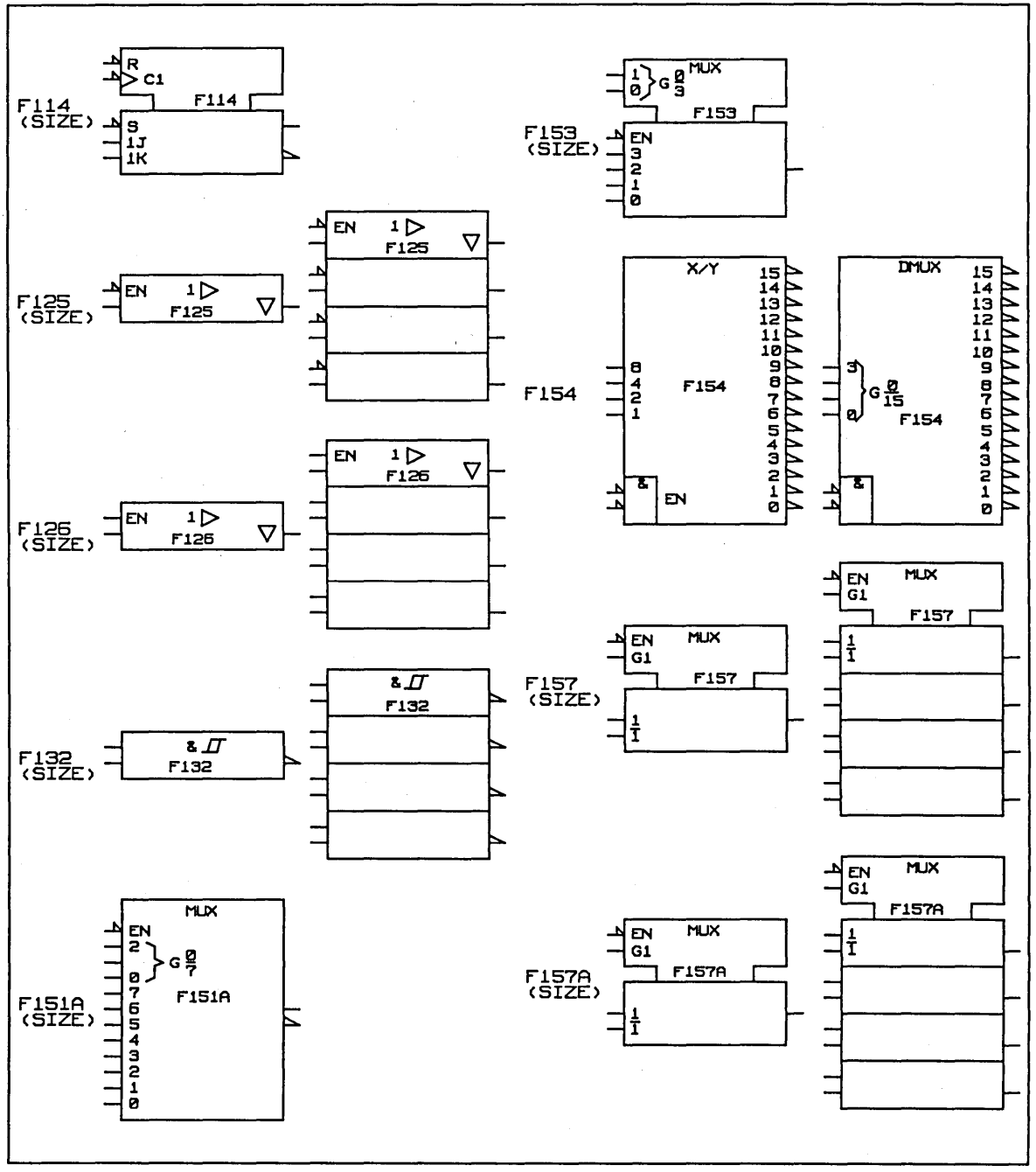

F828 (SIZE)
F828
TS
D
Q
OE1
OE2
F828
TS
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
OE1 OE2
F841 (SIZE)
D
Q
F841
E
OE
F841
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E OE
F842 (SIZE)
D
Q
F842
E
OE
F842
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E OE
F844 (SIZE)
D
Q
F844
E
PRE
MR
OE
F844
D8 D7 D6 D5 D4 D3 D2 D1 D0
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E
PRE
MR
OE
F846 (SIZE)
D
Q
F846
E
PRE
MR
OE
0 1 2
F846
D7 D6 D5 D4 D3 D2 D1 D0
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
E
PRE
MR
OE
0 1 2
F861 (SIZE)
F861
TS
A
B
OEBA OEAB
F861
TS
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
OEBA OEAB
F862 (SIZE)
F862
TS
A
B
OEBA OEAB
F862
TS
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
OEBA OEAB
F863 (SIZE)
F863
TS
A
B
OEAB
OEBA
F863
TS
A8 A7 A6 A5 A4 A3 A2 A1 A0
B8 B7 B6 B5 B4 B3 B2 B1 B0
OEAB
OEBA

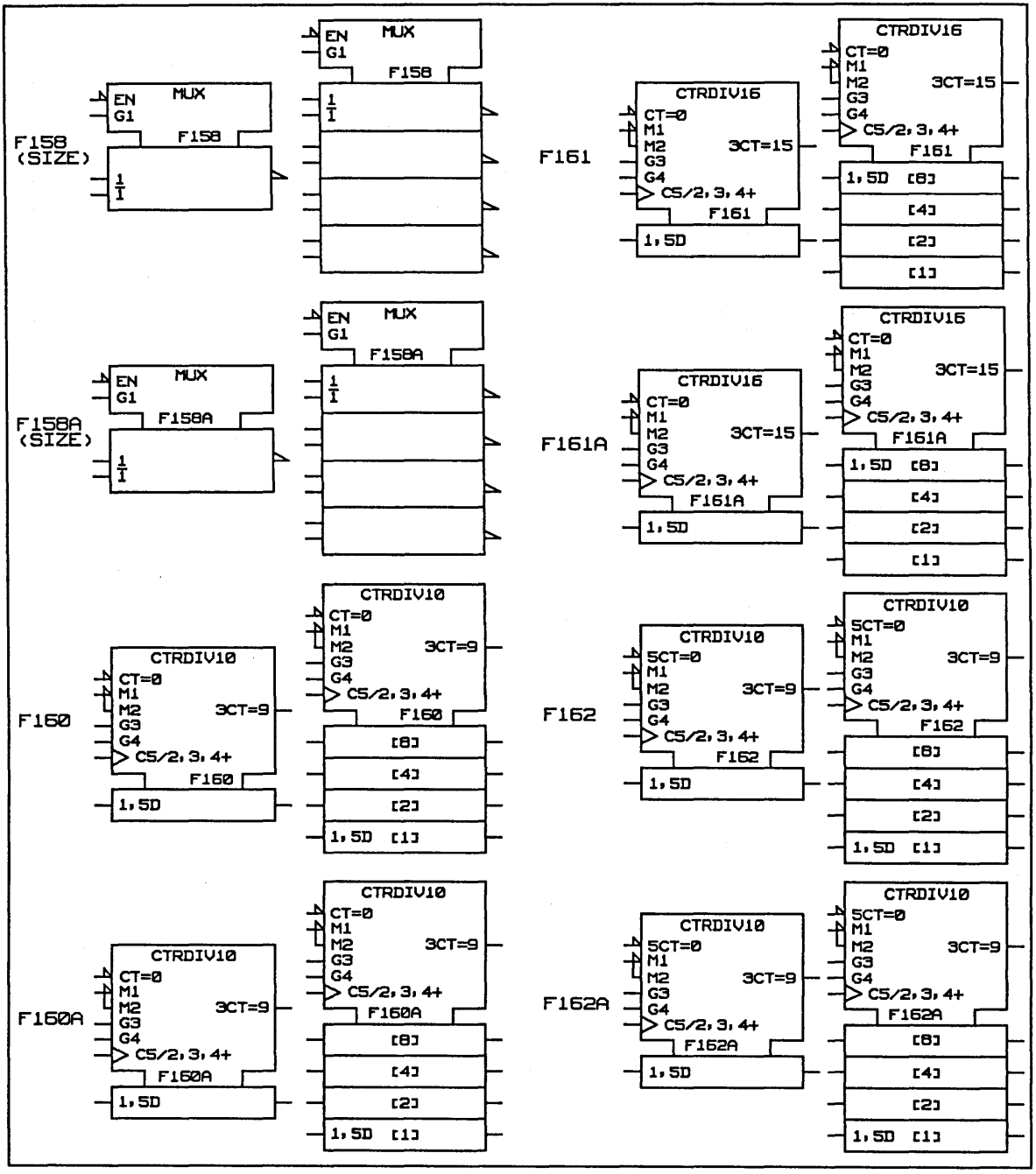

F864
(SIZE)
F864
TS
A
B
OEAB
OEBA
F864
TS
A8
A7
A6
A5
A4
A3
A2
A1
A0
B8
B7
B6
B5
B4
B3
B2
B1
B0
OEAB
OEBA
MAX_DELAY=10000
F881
F881
ALU
P
G
COUT
A=B
CIN
M
MAX_DELAY=10000
F881
ALU
F882
CARRY LOOKAHEAD
CN+32
CN+24
CN+16
CN+8
CN
F882
CARRY LOOKAHEAD
F1240
(SIZE)
F1240
F1240
A3
A2
A1
A0
Y3
Y2
Y1
Y0
OE
F1241
(SIZE)
F1241
F1241
YA3
YA2
YA1
YA0
OEA
F1241
F1241
B3
B2
B1
B0
OEB
F1242
(SIZE)
F1242
TS
A
B
OEA OEB
F1242
TS
OEA OEB

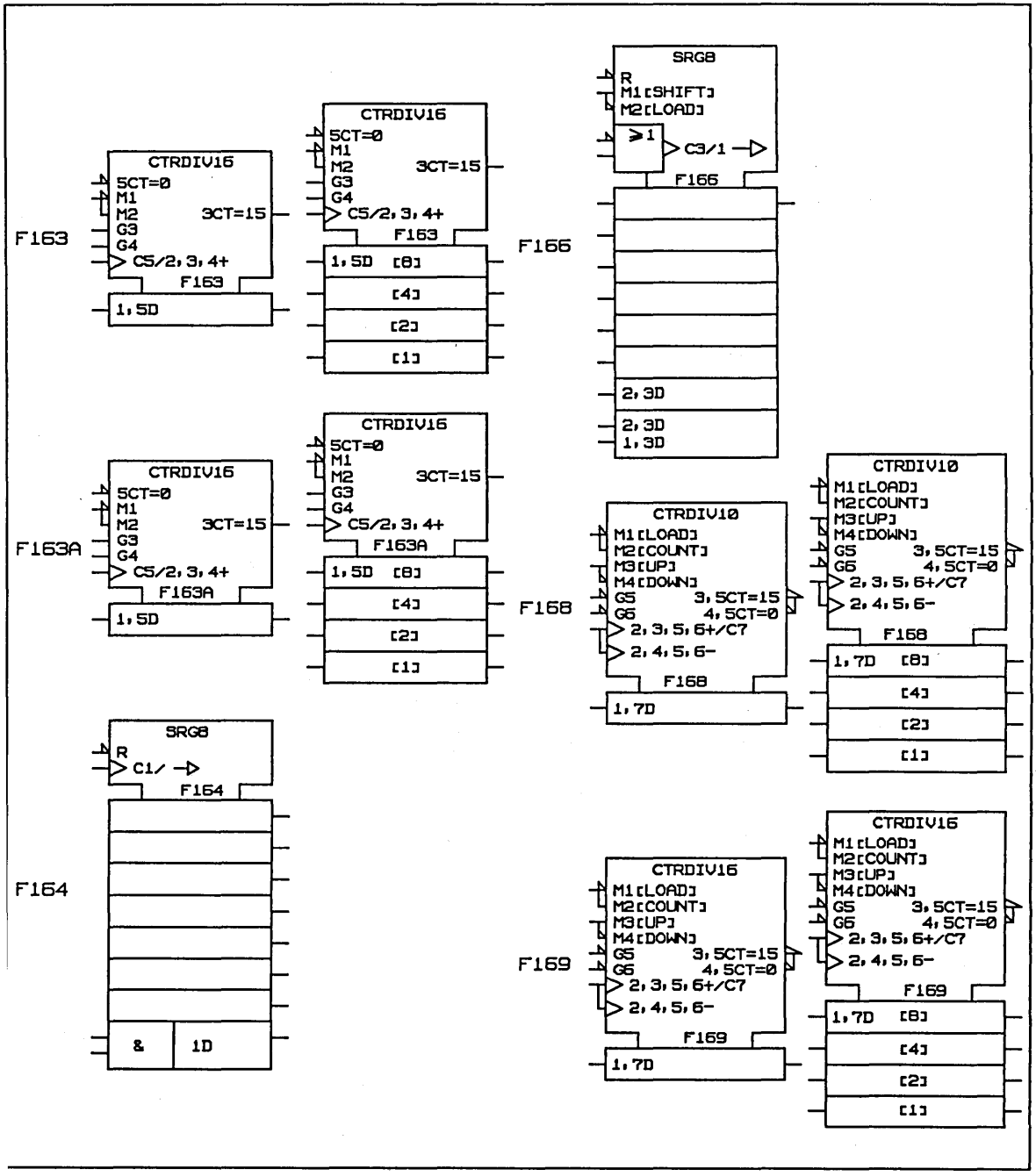

F1243 (SIZE)
F1244 (SIZE)
F1245 (SIZE)
F3037 (SIZE)
F3038 (SIZE)
F3040 (SIZE)
F30240 (SIZE)
F30244 (SIZE)
F30245 (SIZE)
F30640 (SIZE)
MAX_DELAY=10000
F1243
TS
A
B
OEA OEB
A3 A2 A1 A0
B3 B2 B1 B0
F1244
A3 A2 A1 A0
Y3 Y2 Y1 Y0
OE
F1245
TS
A
B
DIR OE
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
F3037
F3038
OC
F3040
F30240
OC
F30244
OC
F30245
TS/OC
F30640
TS/OC

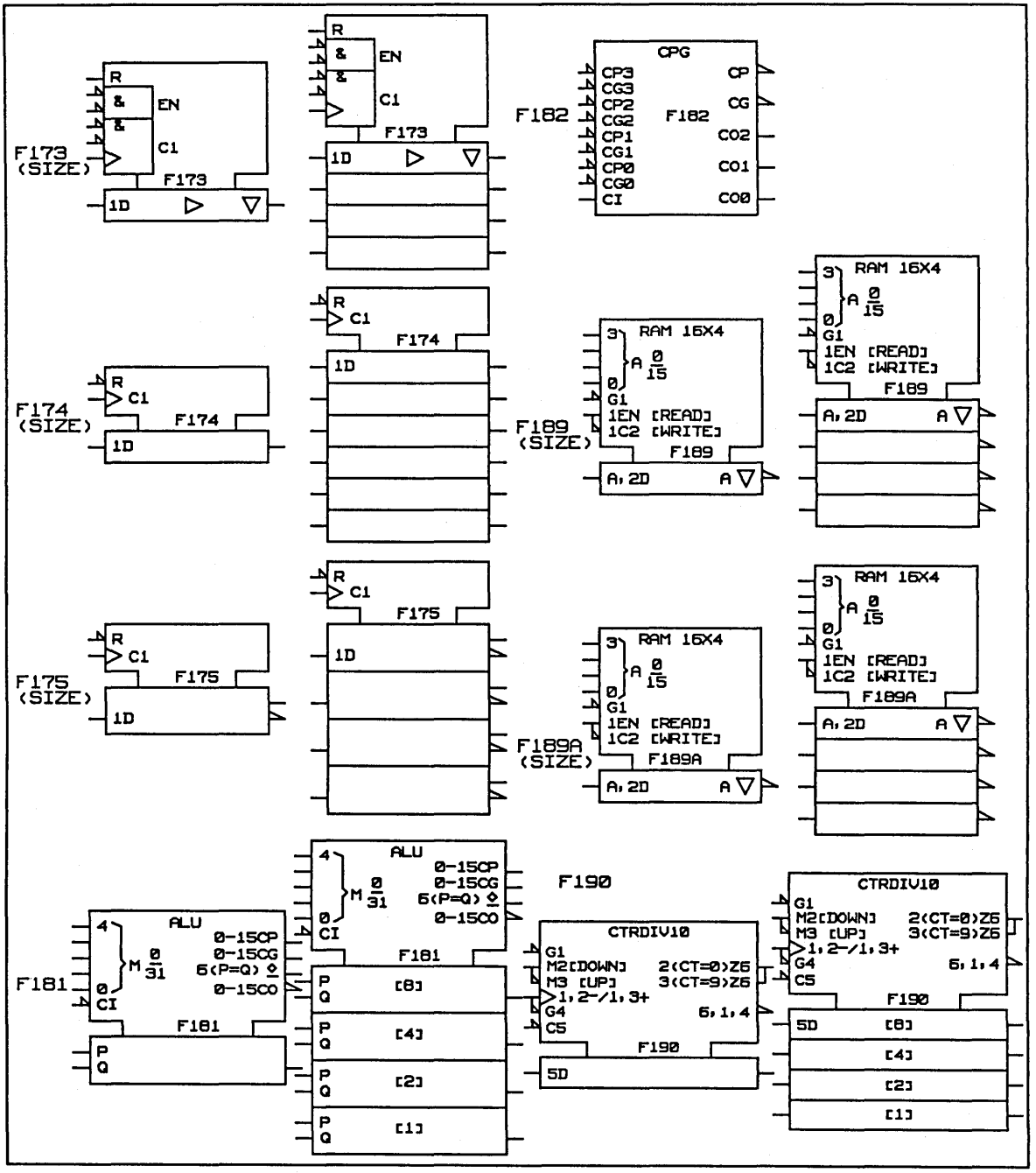

F00
(SIZE)
&
F00
&
F00
F02
(SIZE)
≥1
F02
≥1
F02
F04
(SIZE)
1
F04
1
F04
F08
(SIZE)
&
F08
&
F08
F10
(SIZE)
&
F10
&
F10
F11
(SIZE)
&
F11
&
F11
F13
(SIZE)
&⊓
F13
&⊓
F13
F14
(SIZE)
⊓
F14
⊓
F14
F20
(SIZE)
&
F20
&
F20
F30
(SIZE)
&
F30
F32
(SIZE)
≥1
F32
≥1
F32

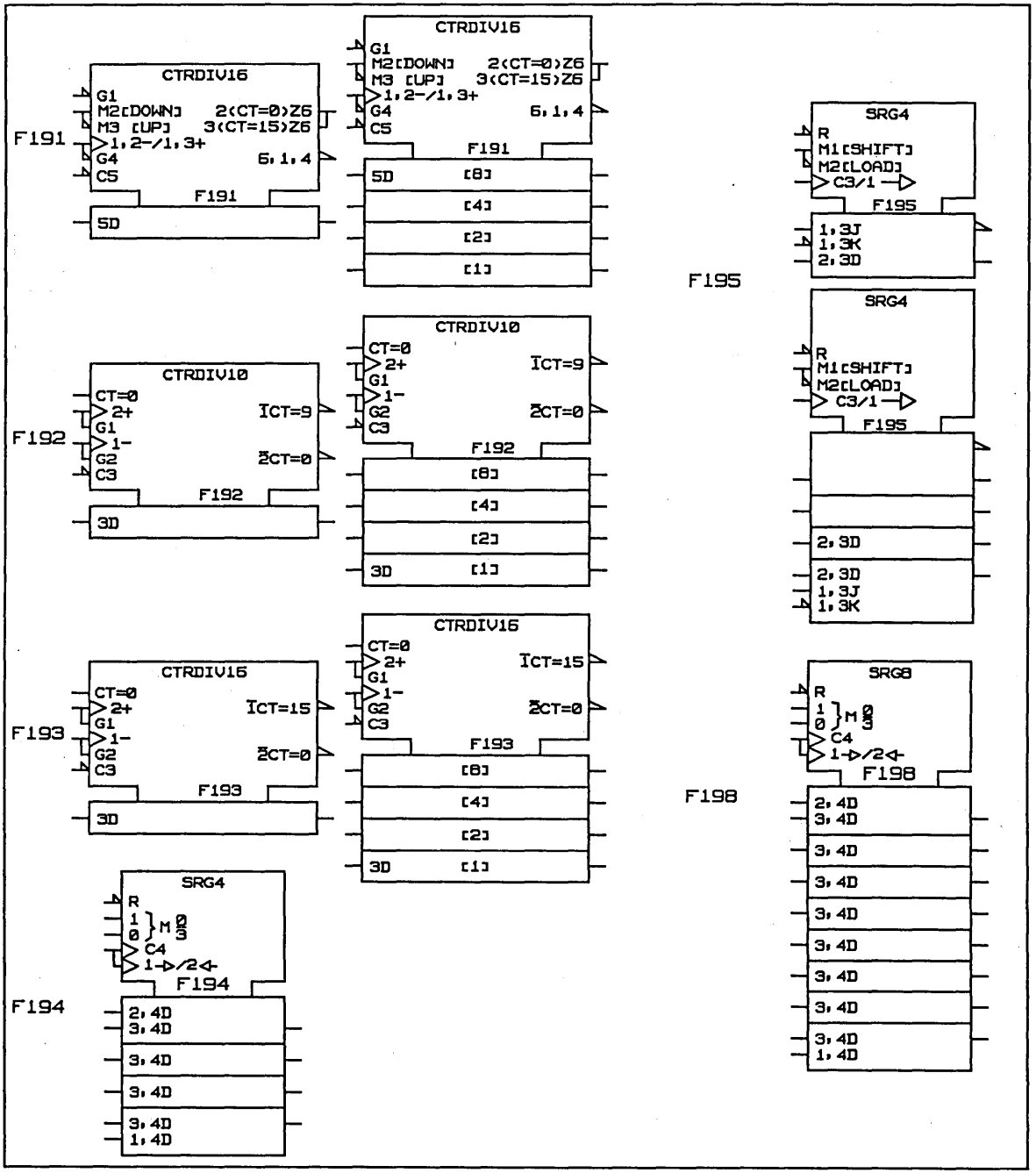

F37
(SIZE)
&
F37
&
F37
MAX_DELAY=10000
F38
(SIZE)
&
F38
MAX_DELAY=10000
&
F38
F40
(SIZE)
&
F40
&
F40
F51
(SIZE)
&
&
≥1
F51
&
&
≥1
F51
F64
(SIZE)
&
&
&
&
≥1
F64
F74
(SIZE)
S
C1
1D
R
F74
F83
3
P
0
3
Q
0
CI
Σ
3
0
F83
CO
F85
3
P
0
<
=
>
3
Q
0
COMP
P<Q
P=Q
P>Q
F85
F86
(SIZE)
=1
F86
F109
(SIZE)
S
1J
C1
1K
R
F109
F112
(SIZE)
S
1J
C1
1K
R
F112
F113
(SIZE)
S
1J
C1
1K
F113

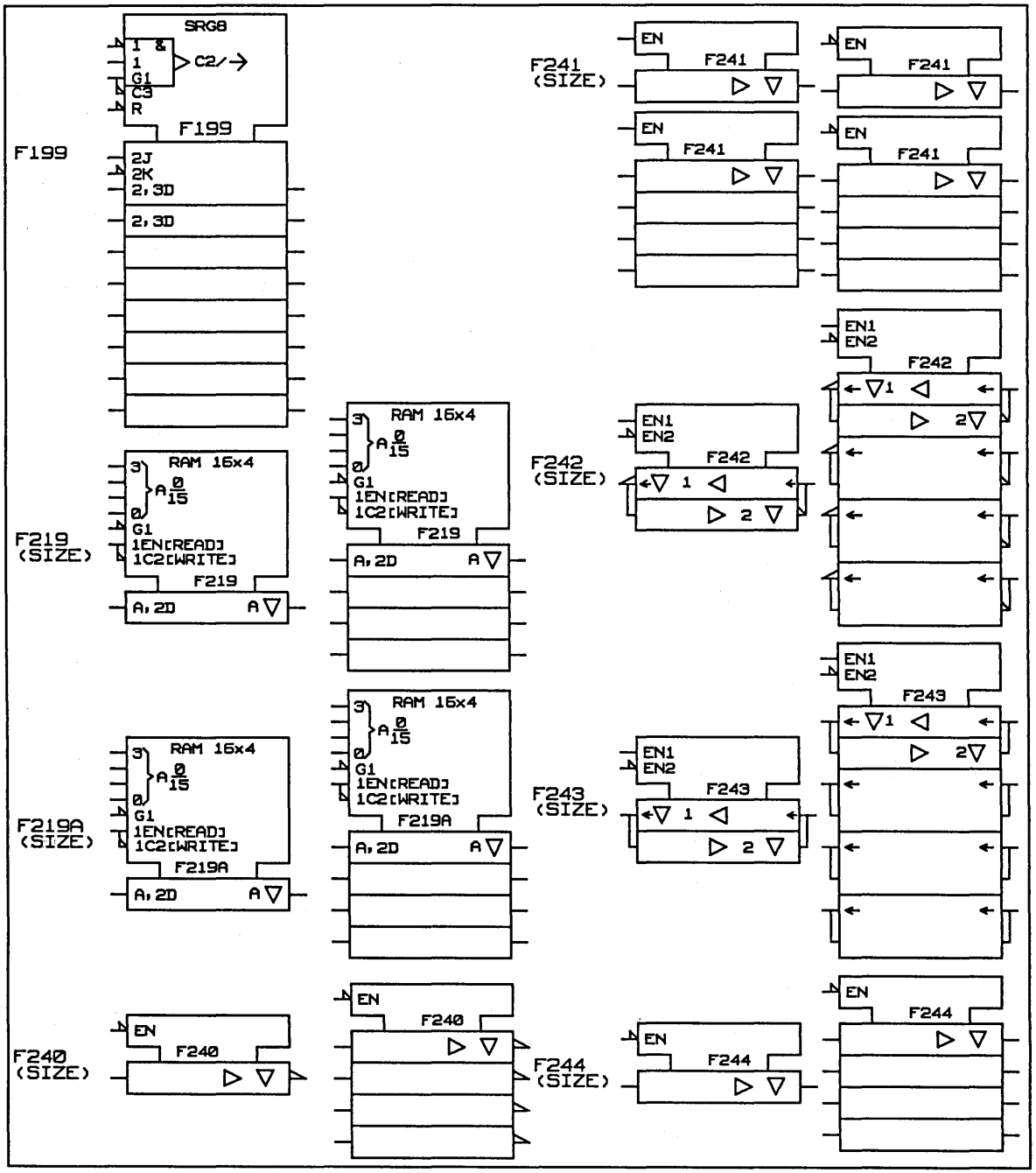

F114
(SIZE)
R
C1
S
1J
1K
F114
F125
(SIZE)
EN
1
F125
F126
(SIZE)
F126
F132
(SIZE)
&
F132
F151A
(SIZE)
MUX
EN
G
F151A
F153
(SIZE)
F153
F154
X/Y
F154
DMUX
F157
(SIZE)
G1
F157
F157A
(SIZE)
F157A

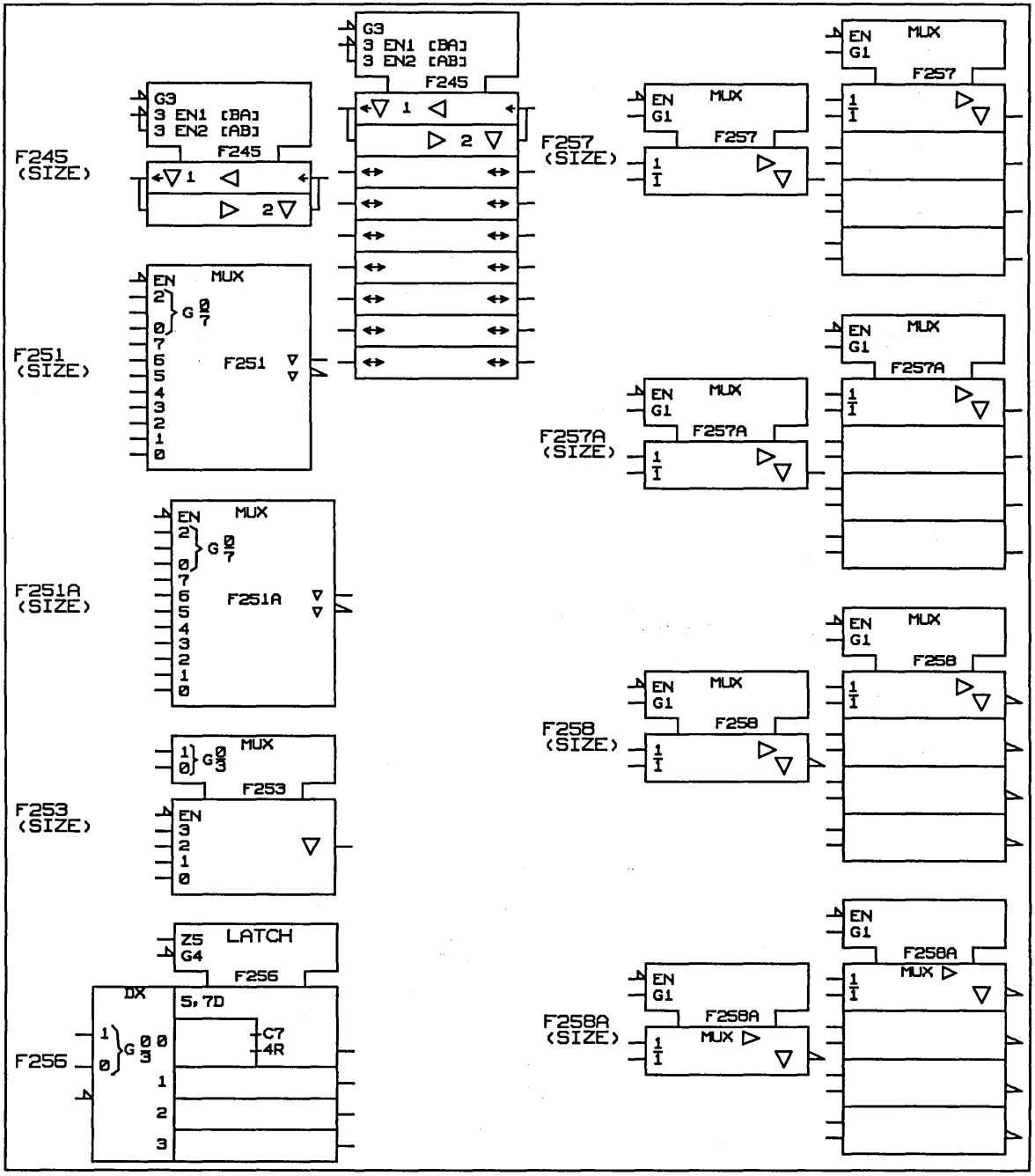

F158
(SIZE)
MUX
EN
G1
F158
1
I
F158A
(SIZE)
F158A
F160
CTRDIV10
CT=0
M1
M2
G3
G4
3CT=9
C5/2,3,4+
F160
1,5D
[8]
[4]
[2]
[1]
F160A
F160A
F161
CTRDIV16
3CT=15
F161
F161A
F161A
F162
5CT=0
F162
F162A
F162A

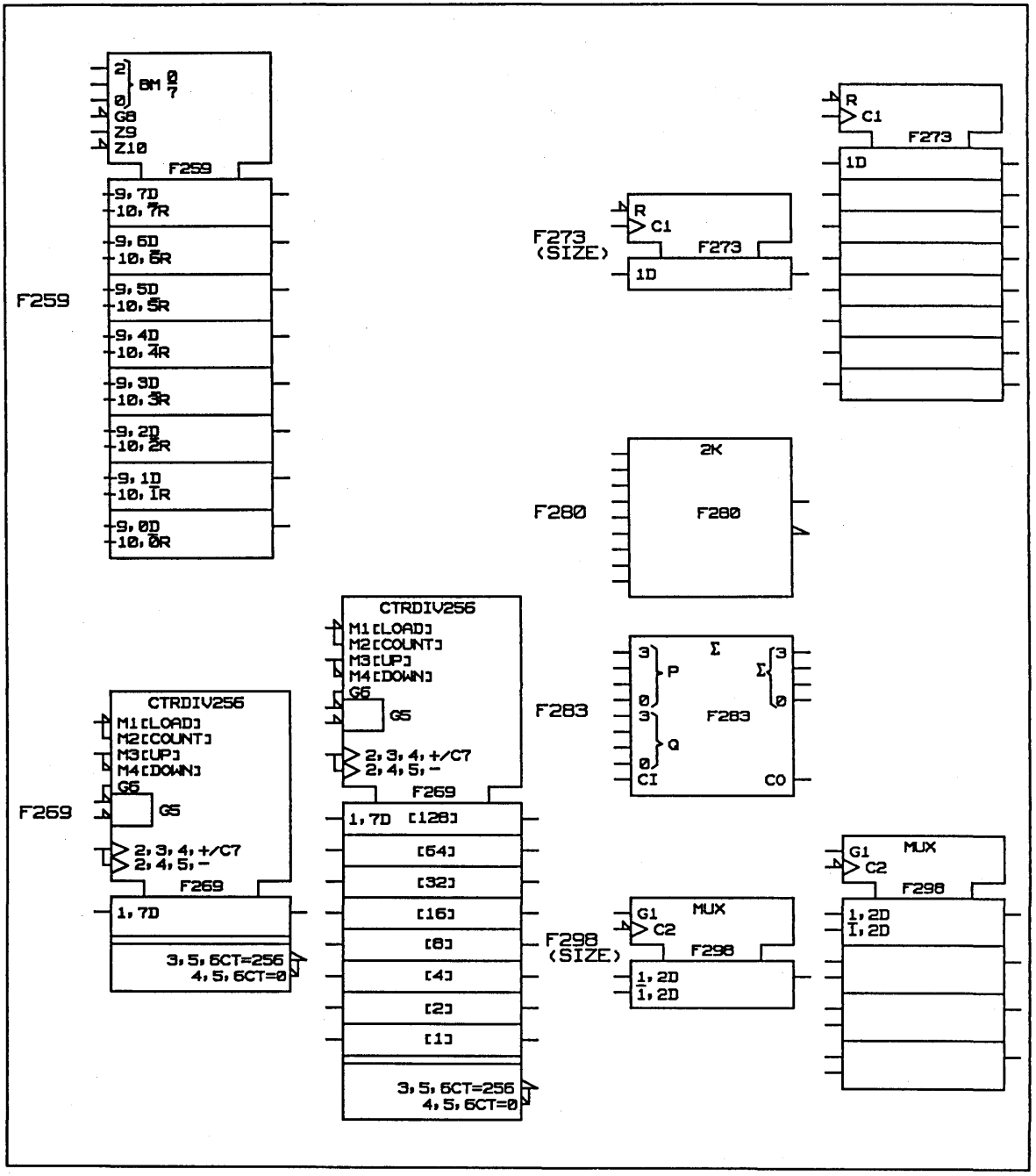

F163
CTRDIV16
5CT=0
M1
M2
3CT=15
G3
G4
C5/2,3,4+
F163
1,5D
CTRDIV16
5CT=0
M1
M2
3CT=15
G3
G4
C5/2,3,4+
F163
1,5D [8]
[4]
[2]
[1]
F166
SRG8
R
M1[SHIFT]
M2[LOAD]
≥1
C3/1
F166
2,3D
2,3D
1,3D
F163A
CTRDIV16
5CT=0
M1
M2
3CT=15
G3
G4
C5/2,3,4+
F163A
1,5D
CTRDIV16
5CT=0
M1
M2
3CT=15
G3
G4
C5/2,3,4+
F163A
1,5D [8]
[4]
[2]
[1]
F168
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
F168
1,7D
CTRDIV10
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
F168
1,7D [8]
[4]
[2]
[1]
F164
SRG8
R
C1/
F164
&
1D
F169
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
F169
1,7D
CTRDIV16
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
G5 3,5CT=15
G6 4,5CT=0
2,3,5,6+/C7
2,4,5,6-
F169
1,7D [8]
[4]
[2]
[1]


F173
(SIZE)
R
&
EN
C1
1D
F173
F182
CPG
CP3
CG3
CP2
CG2
CP1
CG1
CP0
CG0
CI
CP
CG
CO2
CO1
CO0
F174
(SIZE)
F174
F189
(SIZE)
RAM 16X4
A 0 15
G1
1EN [READ]
1C2 [WRITE]
F189
A,2D
F175
(SIZE)
F175
F189A
(SIZE)
F189A
F181
ALU
M 0 31
CI
0-15CP
0-15CG
6(P=Q)
0-15C0
P
Q
[8]
[4]
[2]
[1]
F190
CTRDIV10
G1
M2[DOWN]
M3 [UP]
1,2-/1,3+
G4
C5
2(CT=0)Z6
3(CT=9)Z6
6,1,4
5D

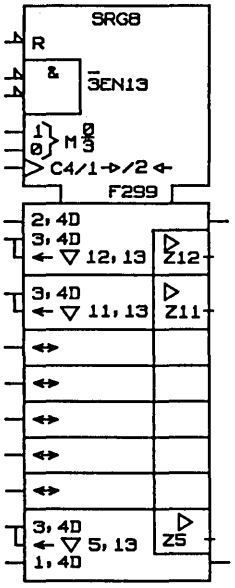

CTRDIV16
G1
M2[DOWN] 2<CT=0>Z6
M3 [UP] 3<CT=15>Z6
1,2-/1,3+
G4 6,1,4
C5
F191
5D
[8]
[4]
[2]
[1]
CTRDIV10
CT=0
2+
G1
1-
G2
C3
ICT=9
ZCT=0
F192
3D
CTRDIV16
CT=0
2+
G1
1-
G2
C3
ICT=15
ZCT=0
F193
SRG4
R
M1[SHIFT]
M2[LOAD]
C3/1
F195
1,3J
1,3K
2,3D
SRG8
R
1
0
M
C4
1-▷/2◁
F198
2,4D
3,4D
1,4D
F191
F192
F193
F194
F195
F198


SRG8
1 &
1
G1
C3
R
C2/→
F199
F199
2J
2K
2,3D
2,3D
RAM 16x4
A 0 15
G1
1EN(READ)
1C2(WRITE)
F219
A,2D
A
F219
(SIZE)
F219A
(SIZE)
F240
(SIZE)
EN
F240
F241
(SIZE)
EN1
EN2
F242
1
2
F242
(SIZE)
F243
F243
(SIZE)
F244
F244
(SIZE)

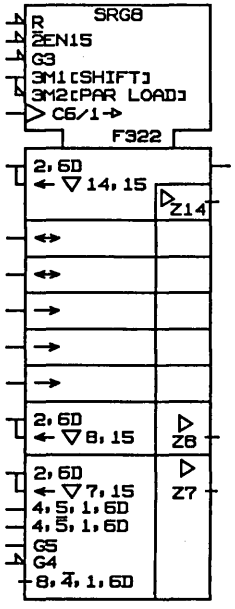

F245
(SIZE)
G3
3 EN1 [BA]
3 EN2 [AB]
F245
1
2
F251
(SIZE)
EN
MUX
G
F251
F251A
(SIZE)
F251A
F253
(SIZE)
F253
LATCH
Z5
G4
F256
DX
5,7D
C7
4R
F257
(SIZE)
F257
G1
1
I
F257A
(SIZE)
F257A
F258
(SIZE)
F258
F258A
(SIZE)
F258A


F259
F273
(SIZE)
F280
F283
F269
F298
(SIZE)
CTRDIV256
MUX
2K
F280
F283
F269
F273
F298
BM
G8
Z9
Z10
1D
R
C1
P
Q
CI
CO
G5
G6
M1[LOAD]
M2[COUNT]
M3[UP]
M4[DOWN]
2,3,4,+/C7
2,4,5,−
1,7D
[128]
[64]
[32]
[16]
[8]
[4]
[2]
[1]
3,5,6CT=256
4,5,6CT=0
G1
C2
1,2D
Ī,2D

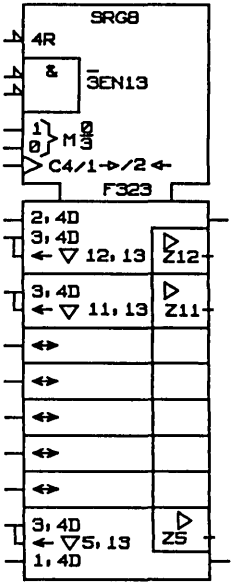
F299



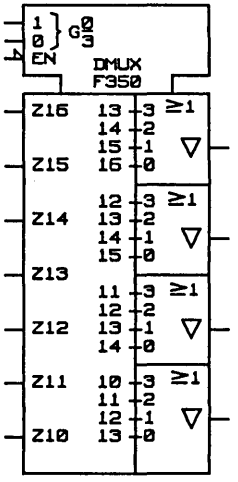
F322

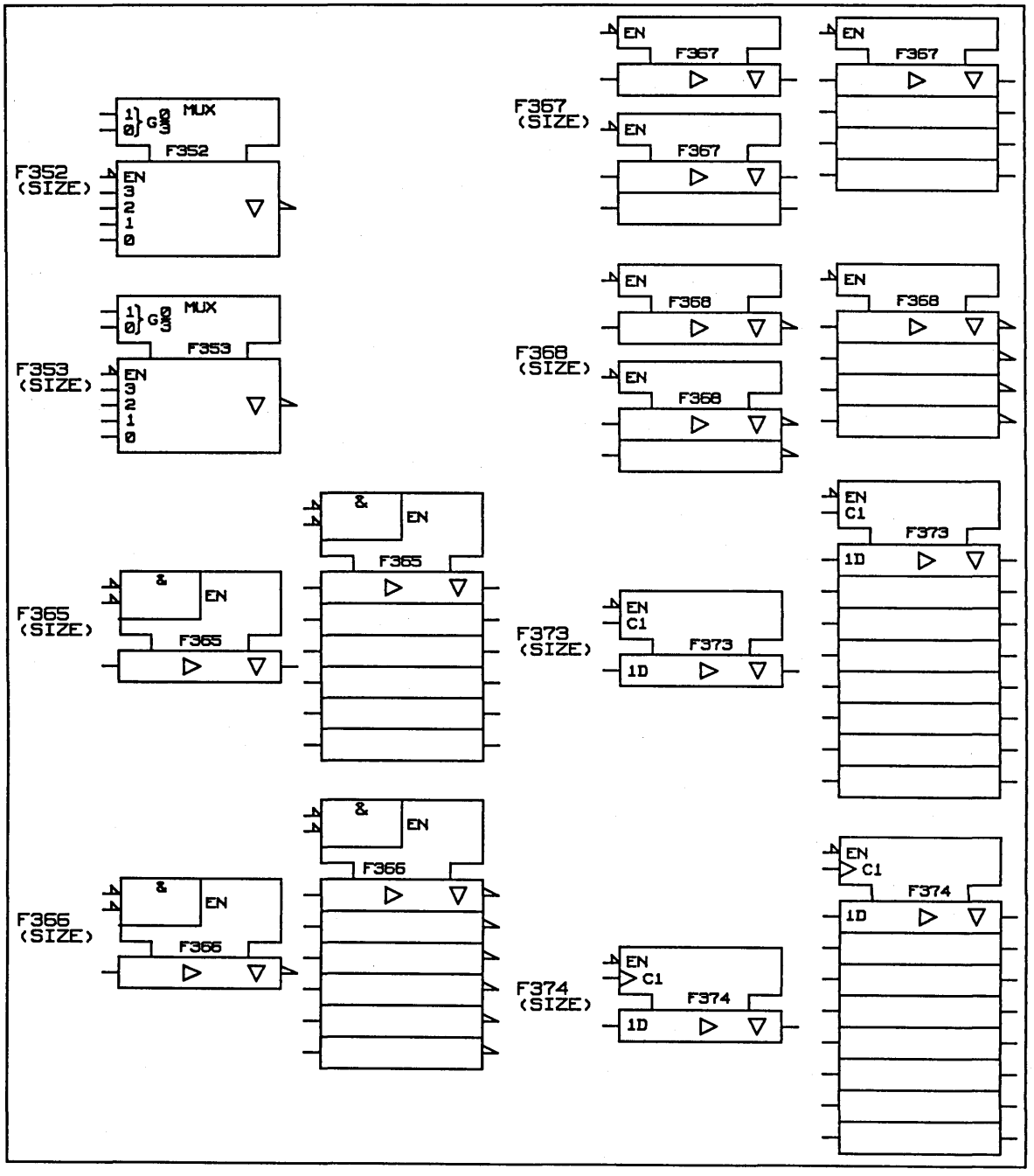


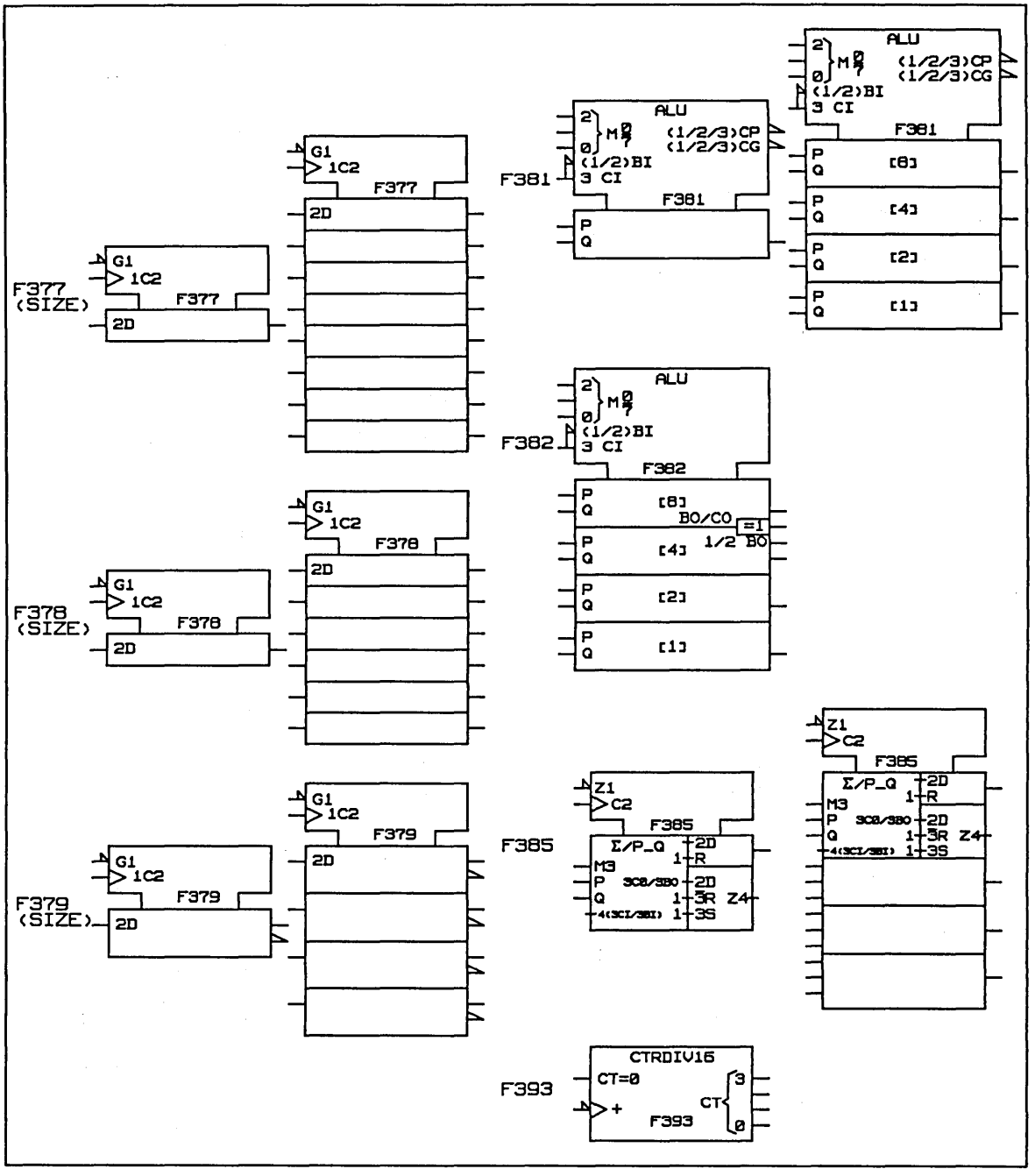
F323

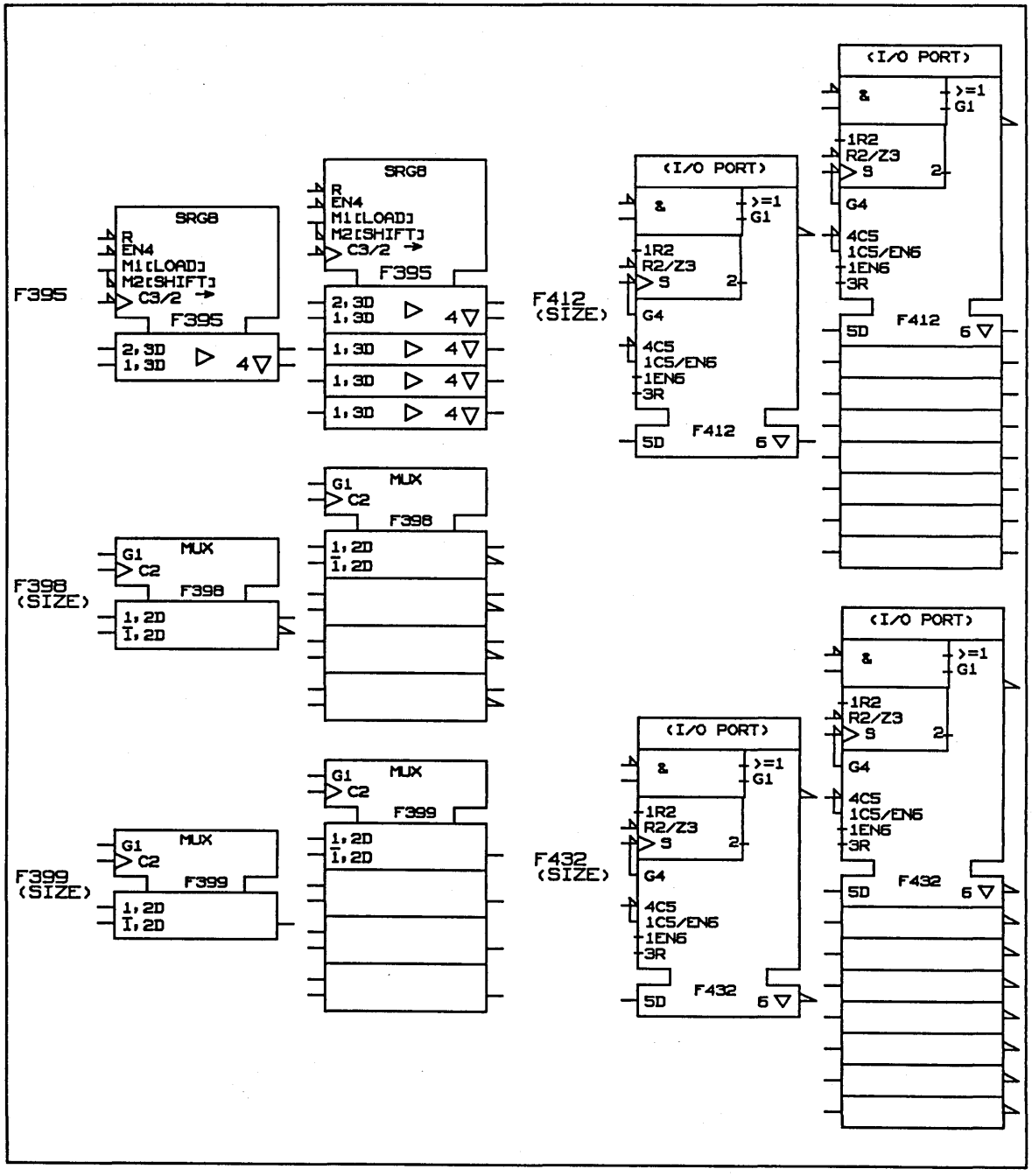


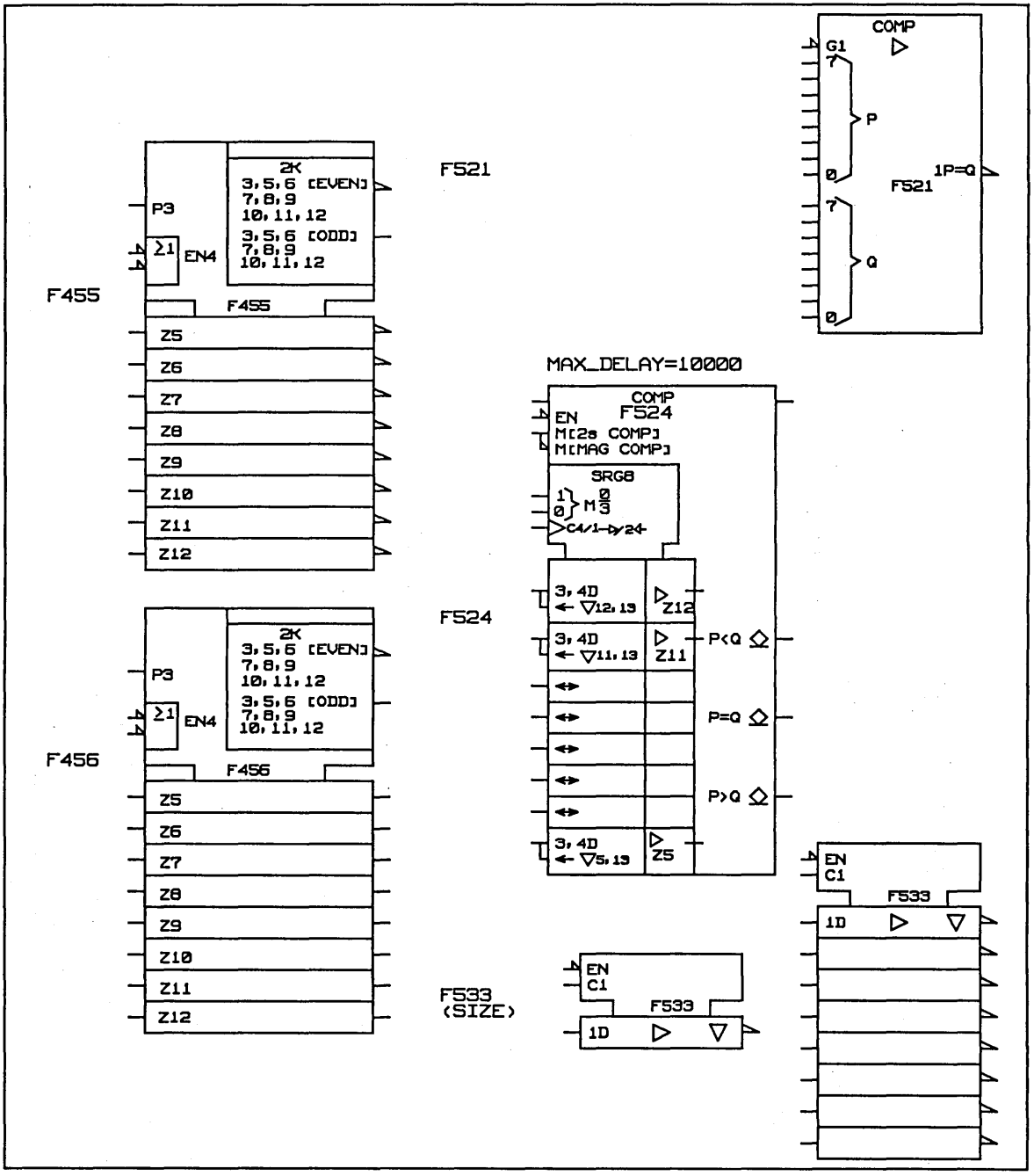
F350

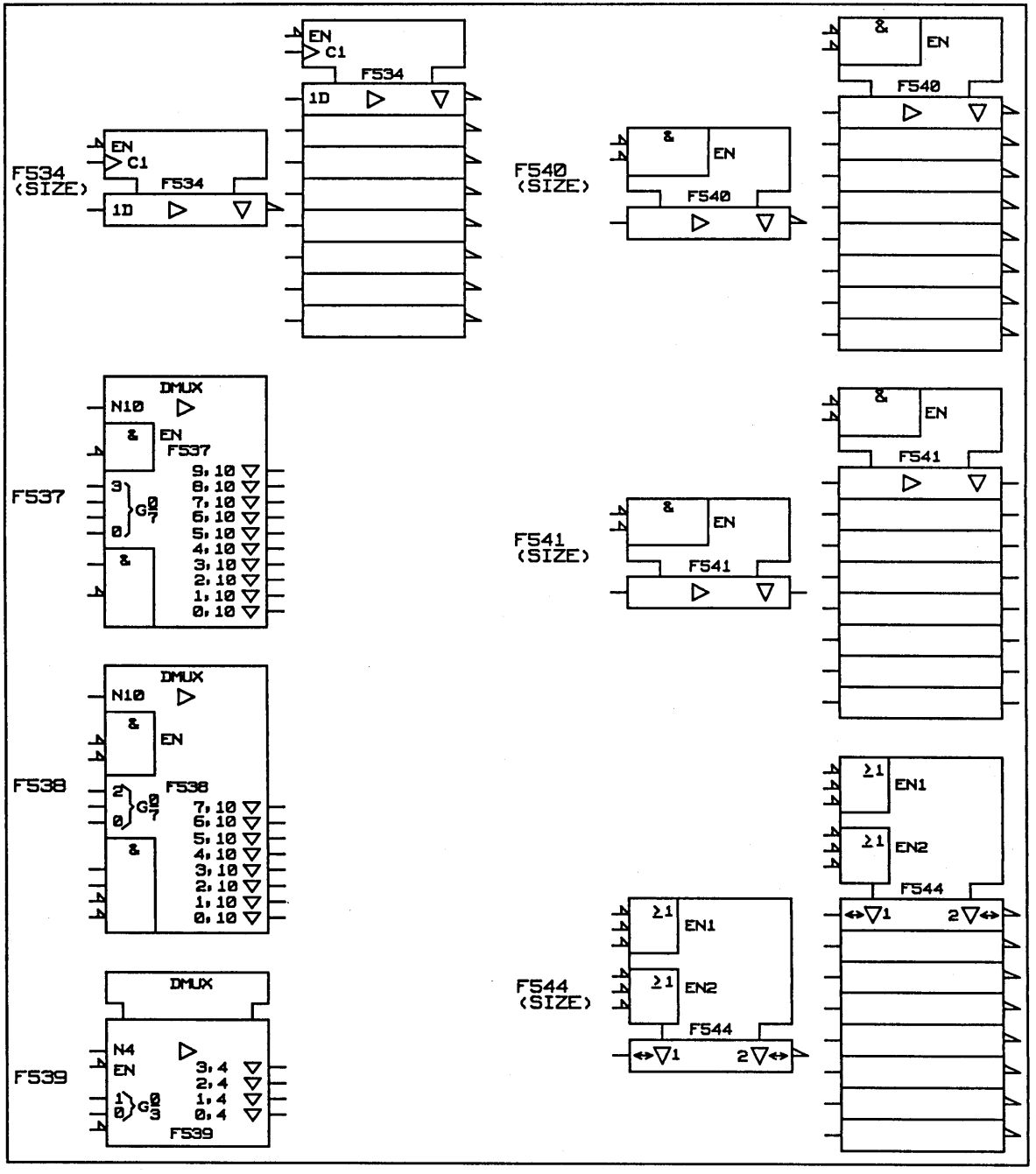


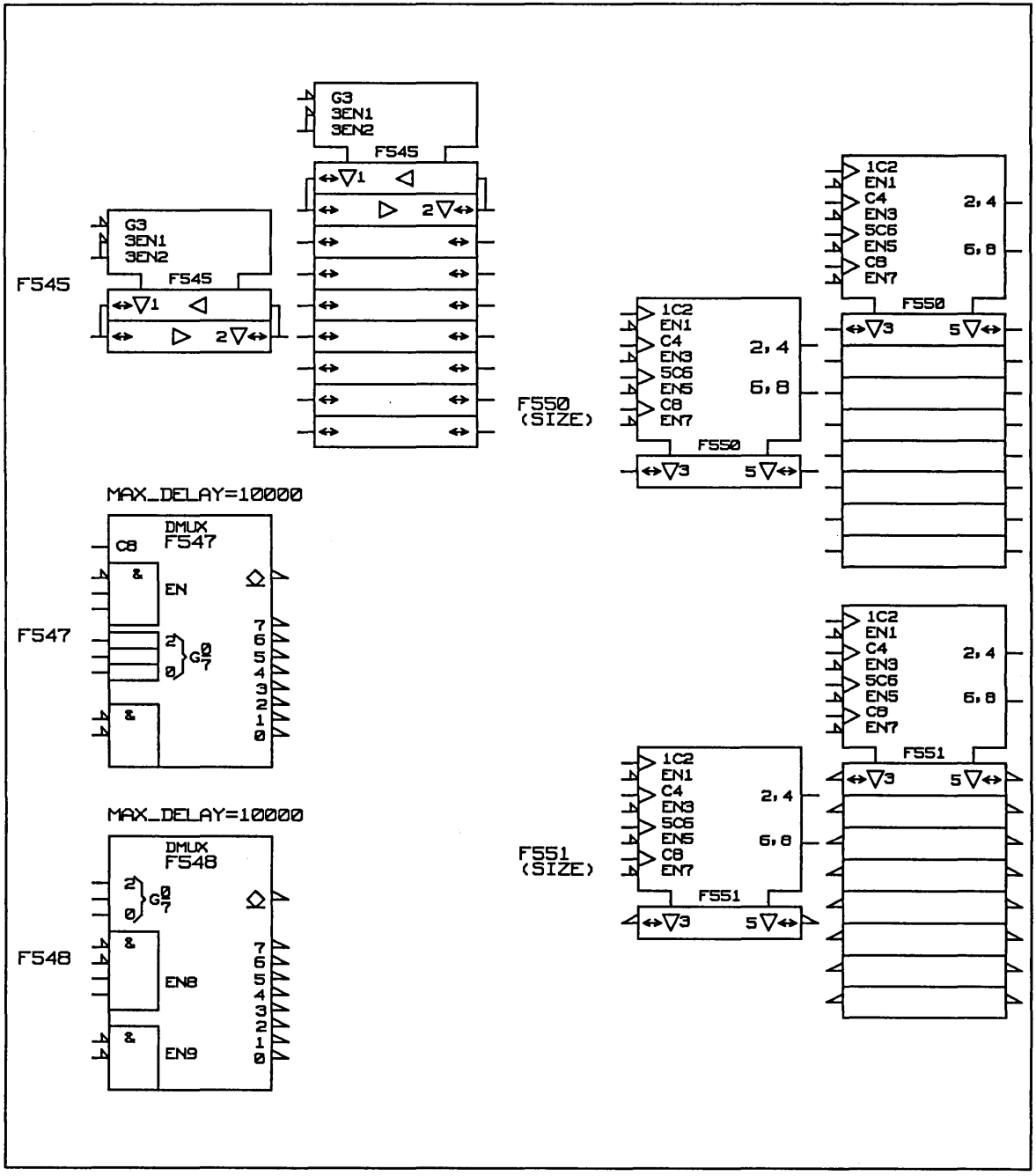

F352
(SIZE)
MUX
F352
EN
3
2
1
0
F353
(SIZE)
MUX
F353
EN
3
2
1
0
F365
(SIZE)
&
EN
F365
F366
(SIZE)
&
EN
F366
F367
(SIZE)
EN
F367
F368
(SIZE)
EN
F368
F373
(SIZE)
EN
C1
F373
1D
F374
(SIZE)
EN
C1
F374
1D

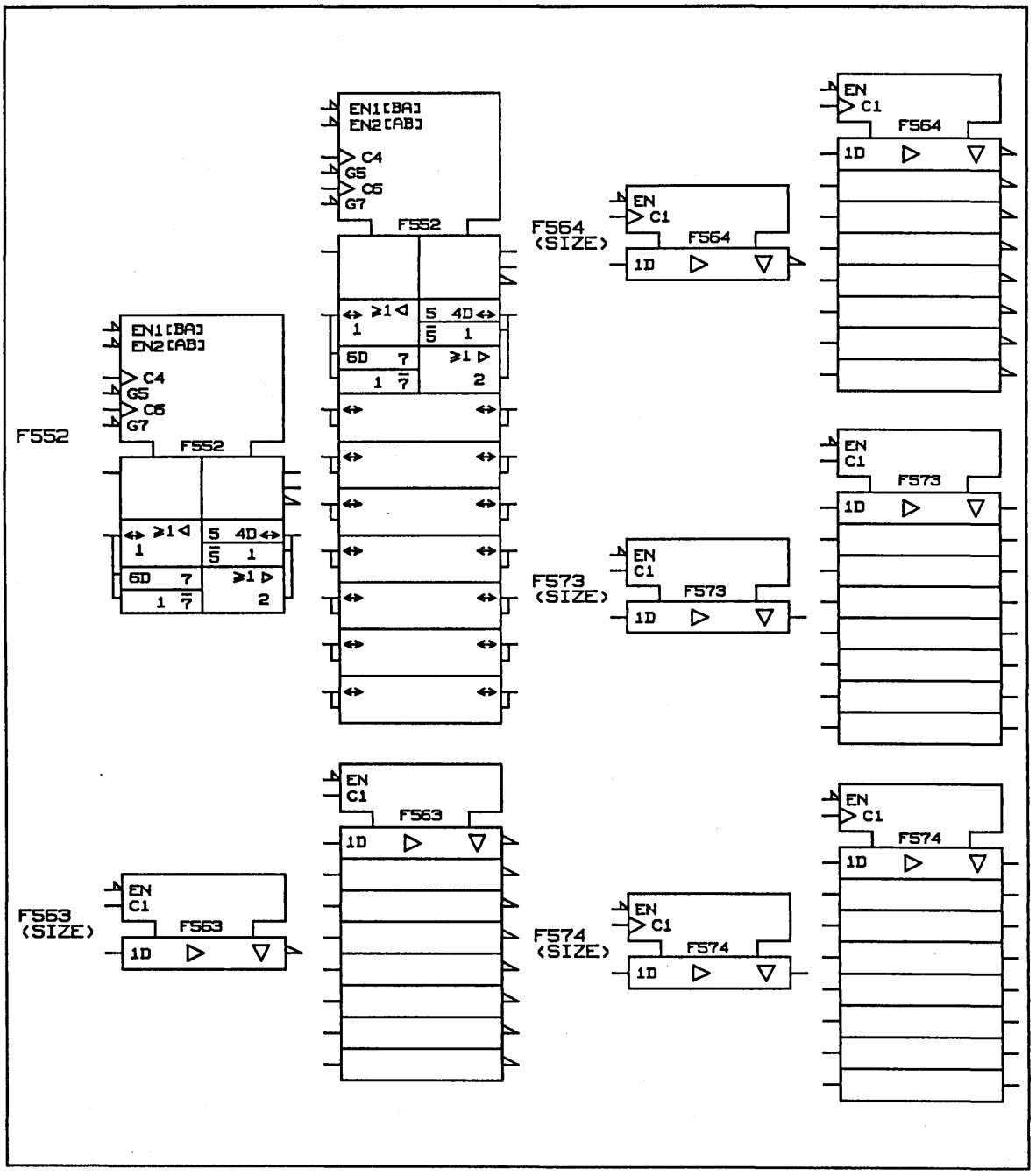

F377
(SIZE)
G1
1C2
2D
F377
F378
(SIZE)
F378
F379
(SIZE)
F379
F381
ALU
2
0
M
(1/2)BI
3 CI
(1/2/3)CP
(1/2/3)CG
P
Q
[8]
[4]
[2]
[1]
F382
BO/CO
=1
1/2 BO
F385
Z1
C2
Σ/P_Q
M3
SCB/SBO
SCI/SBI
R
S
Z4
F393
CTRDIV16
CT=0
CT
3
0

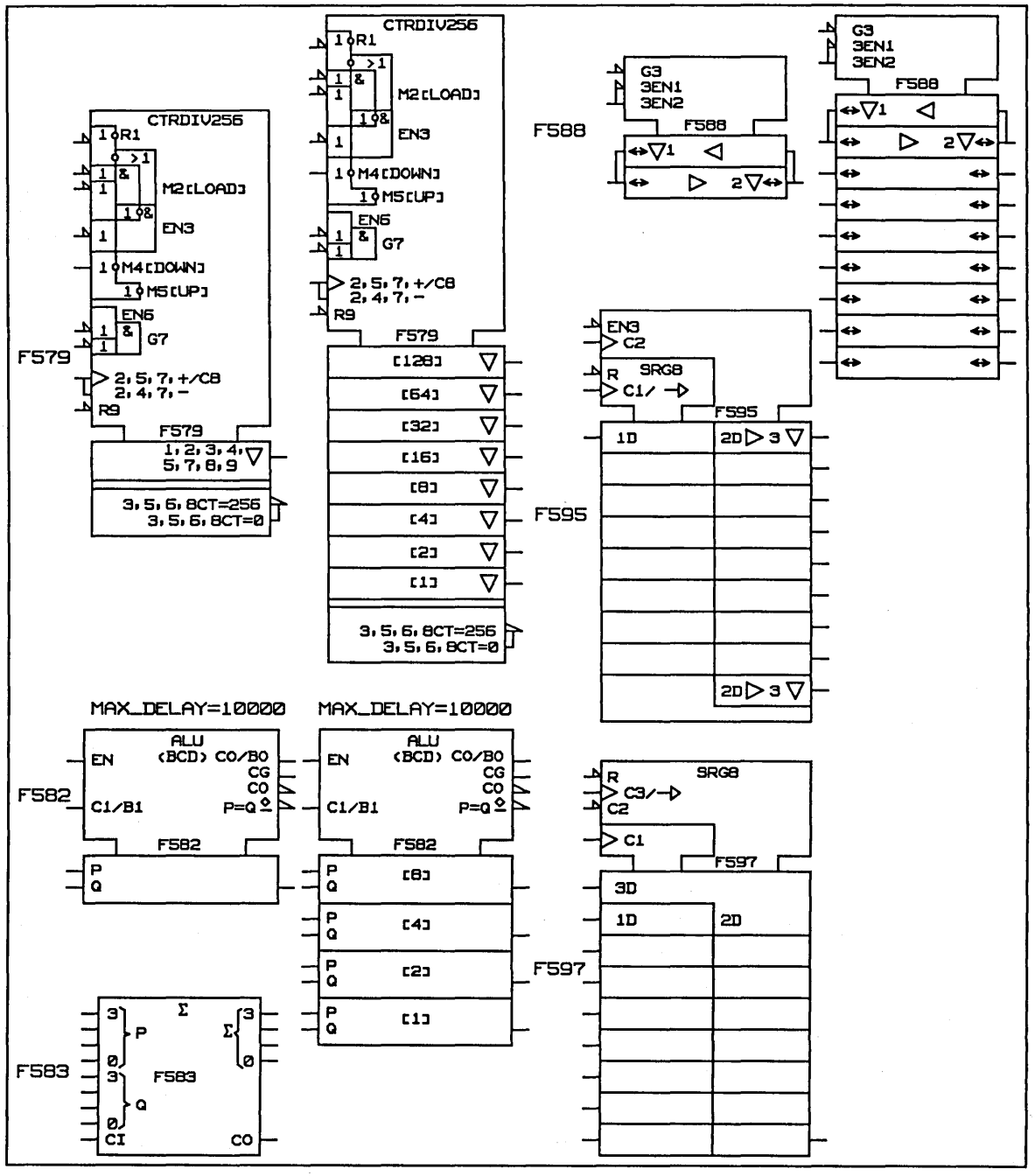

F395
SRG8
R
EN4
M1[LOAD]
M2[SHIFT]
C3/2
F395
2,3D
1,3D
4
SRG8
R
EN4
M1[LOAD]
M2[SHIFT]
C3/2
F395
2,3D
1,3D
1,3D
1,3D
1,3D
4
F398
(SIZE)
G1
C2
MUX
F398
1,2D
I,2D
G1
C2
MUX
F398
1,2D
I,2D
F399
(SIZE)
G1
C2
MUX
F399
1,2D
I,2D
G1
C2
MUX
F399
1,2D
I,2D
F412
(SIZE)
(I/O PORT)
&
>=1
G1
1R2
R2/Z3
S
2
G4
4C5
1C5/EN6
1EN6
3R
5D
F412
6
(I/O PORT)
&
>=1
G1
1R2
R2/Z3
S
2
G4
4C5
1C5/EN6
1EN6
3R
5D
F412
6
F432
(SIZE)
(I/O PORT)
&
>=1
G1
1R2
R2/Z3
S
2
G4
4C5
1C5/EN6
1EN6
3R
5D
F432
6
(I/O PORT)
&
>=1
G1
1R2
R2/Z3
S
2
G4
4C5
1C5/EN6
1EN6
3R
5D
F432
6

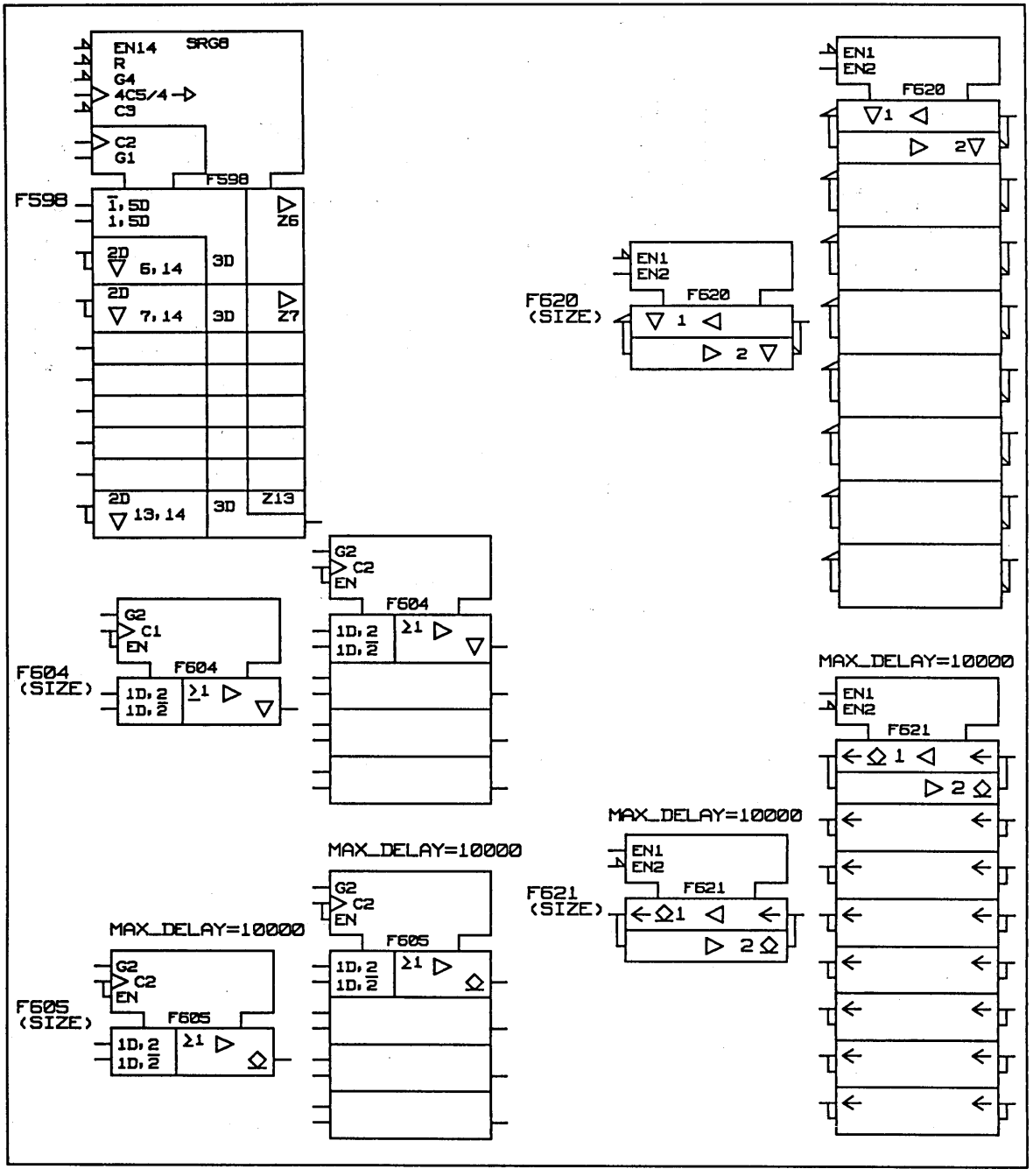

F455
2K
3,5,6 [EVEN]
7,8,9
10,11,12
3,5,6 [ODD]
7,8,9
10,11,12
P3
≥1
EN4
F455
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
F456
2K
3,5,6 [EVEN]
7,8,9
10,11,12
3,5,6 [ODD]
7,8,9
10,11,12
P3
≥1
EN4
F456
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
F521
COMP
G1
P
Q
1P=Q
F521
MAX_DELAY=10000
F524
COMP
F524
EN
M[2s COMP]
M[MAG COMP]
SRG8
M3
C4/1-by24
3,4D
12,13
Z12
3,4D
11,13
Z11
3,4D
5,13
Z5
P<Q
P=Q
P>Q
F533
(SIZE)
EN
C1
F533
1D
EN
C1
F533
1D

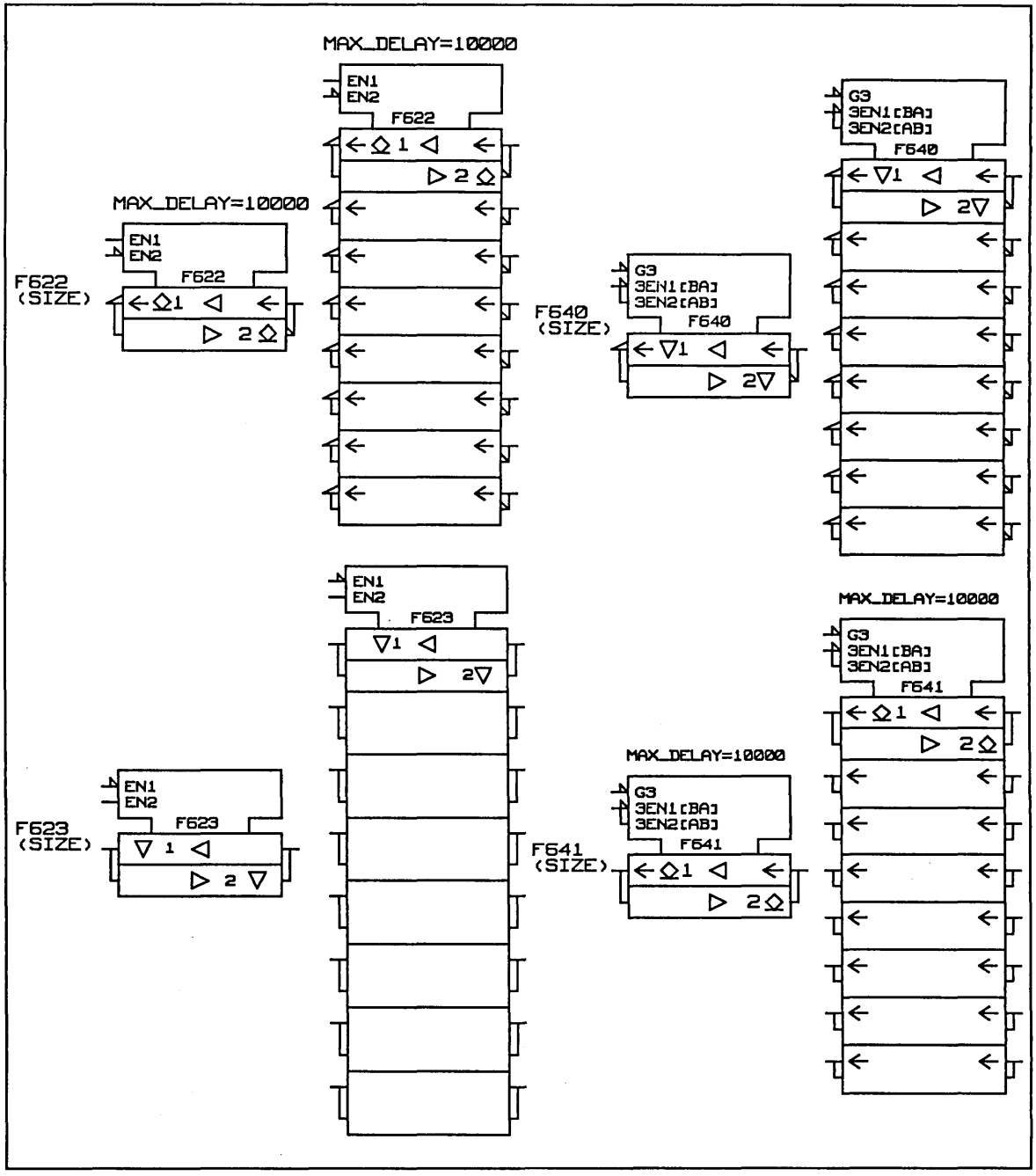

F534
(SIZE)
EN
C1
F534
1D
F540
(SIZE)
&
EN
F540
F537
DMUX
N10
EN
F537
3
0
G
9, 10
8, 10
7, 10
6, 10
5, 10
4, 10
3, 10
2, 10
1, 10
0, 10
F541
(SIZE)
F541
F538
F538
7, 10
6, 10
5, 10
4, 10
3, 10
2, 10
1, 10
0, 10
F544
(SIZE)
≥1
EN1
EN2
F544
1
2
F539
N4
3, 4
2, 4
1, 4
0, 4
F539

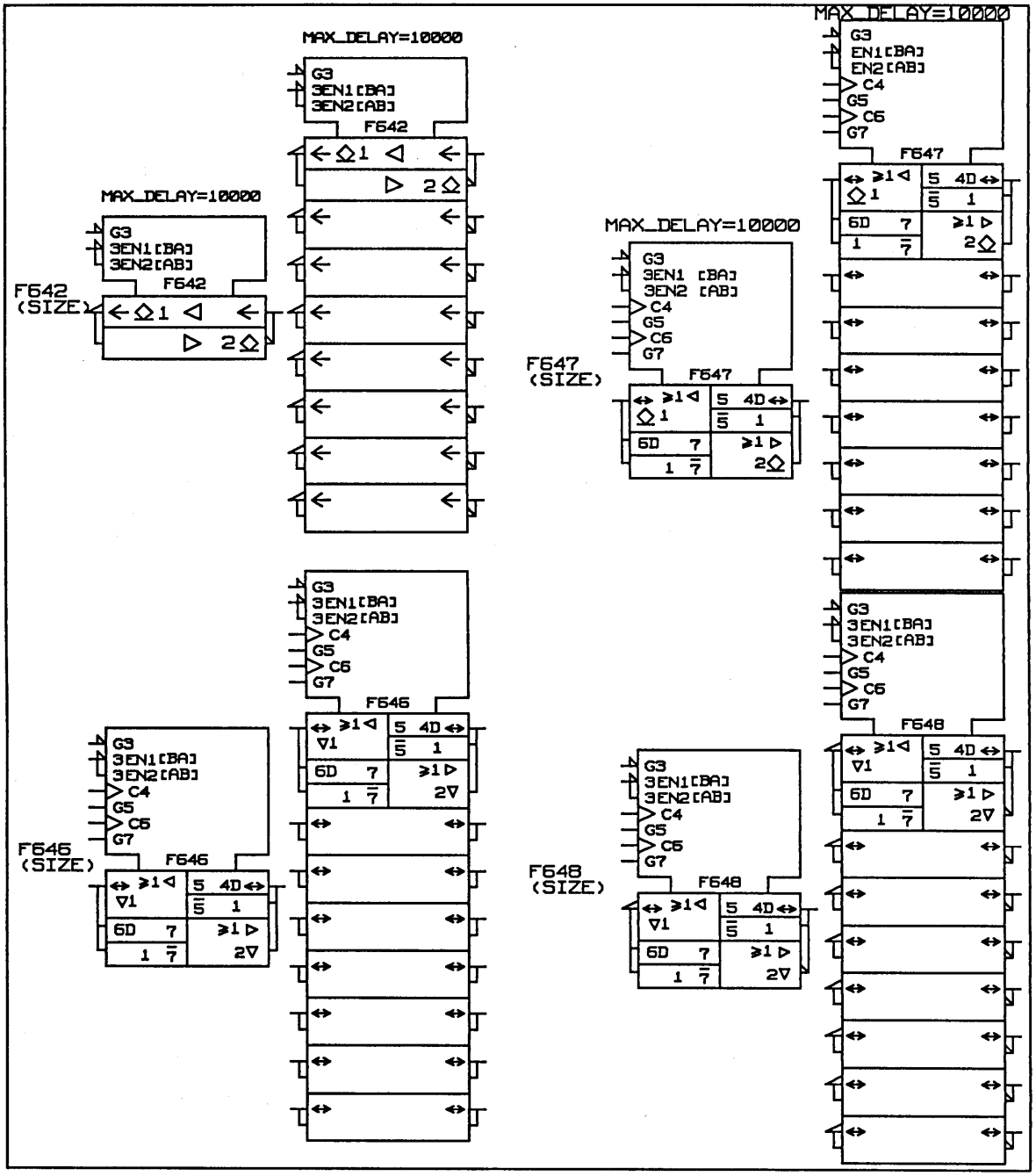

F545
G3
3EN1
3EN2
F545
1
2
F550
(SIZE)
1C2
EN1
C4
EN3
5C6
EN5
C8
EN7
2, 4
6, 8
F550
3
5
F547
MAX_DELAY=10000
DMUX
F547
C8
EN
2
0
G0
7
7 6 5 4 3 2 1 0
F548
MAX_DELAY=10000
DMUX
F548
EN8
EN9
F551
(SIZE)
F551

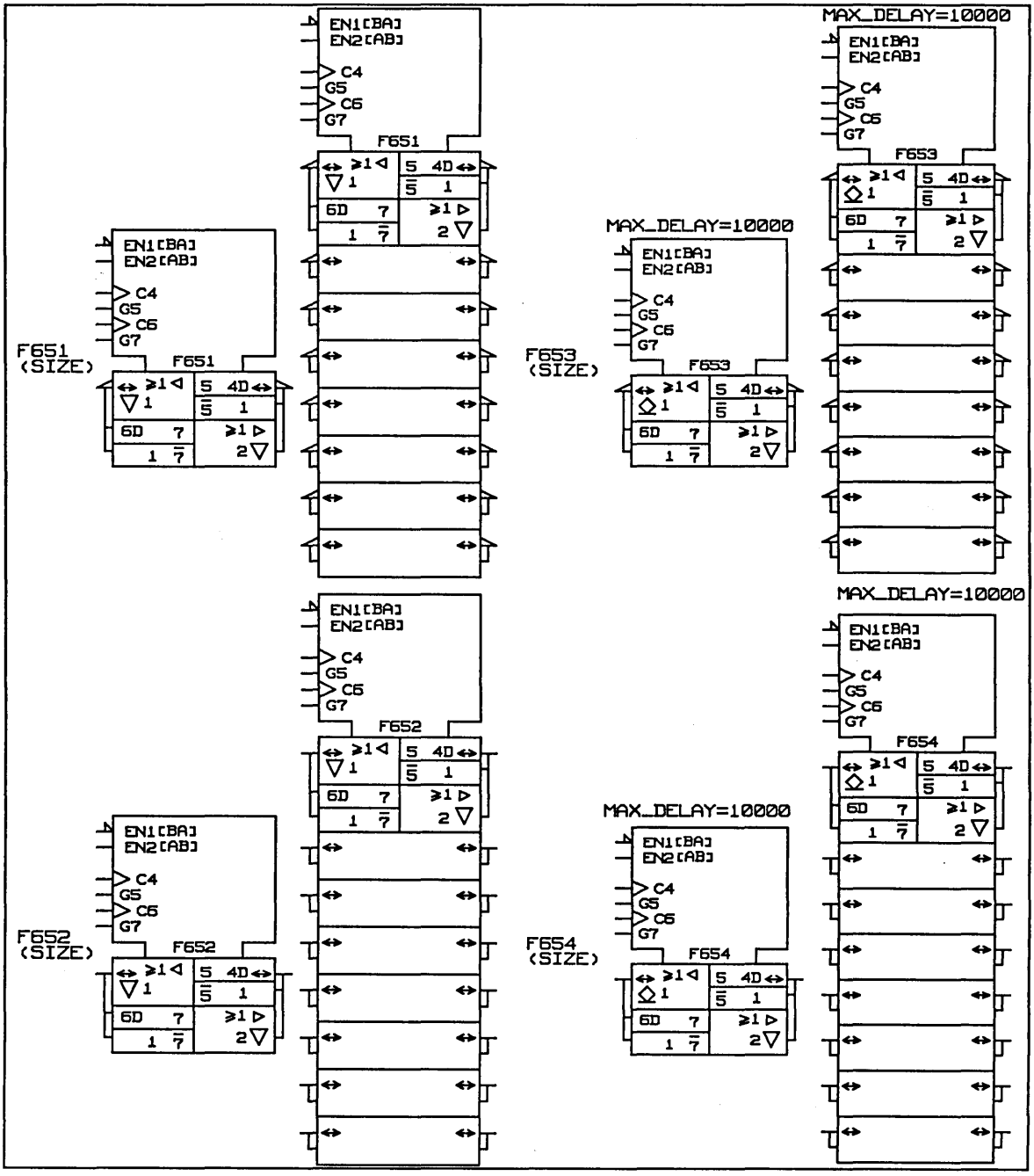

F552
EN1[BA]
EN2[AB]
C4
G5
C6
G7
F552
F563
(SIZE)
EN
C1
F563
1D
F564
(SIZE)
F564
F573
(SIZE)
F573
F574
(SIZE)
F574

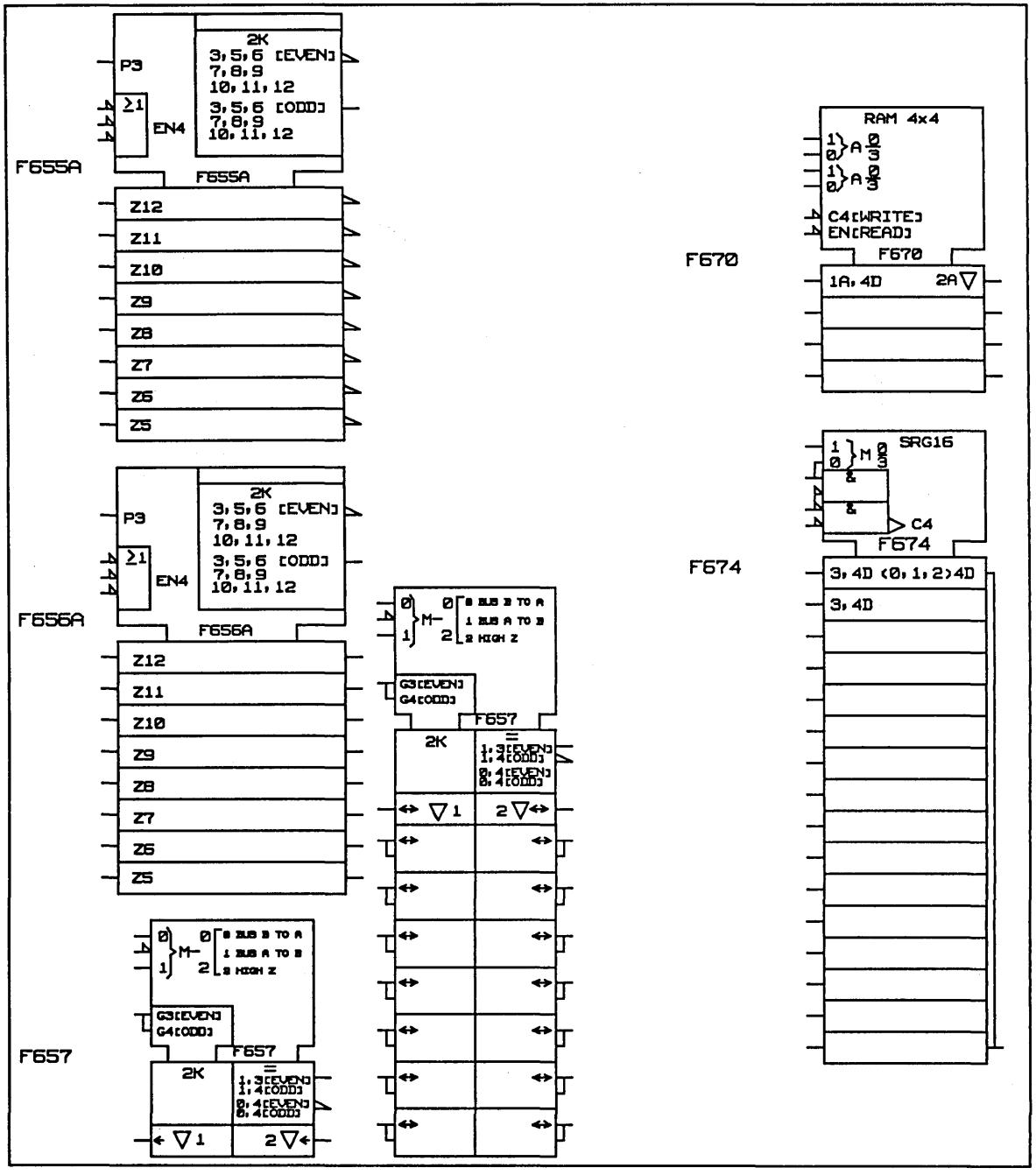

CTRDIV256
R1
>1
&
M2[LOAD]
EN3
M4[DOWN]
M5[UP]
EN6
G7
2, 5, 7, +/C8
2, 4, 7, –
R9
F579
1, 2, 3, 4,
5, 7, 8, 9
3, 5, 6, 8CT=256
3, 5, 6, 8CT=0
[128]
[64]
[32]
[16]
[8]
[4]
[2]
[1]
G3
3EN1
3EN2
F588
1
2
EN3
C2
R
SRG8
C1/
F595
1D
2D
3
MAX_DELAY=10000
ALU
EN
(BCD) CO/BO
CG
CO
C1/B1
P=Q
F582
P
Q
SRG8
R
C3/
C2
C1
F597
3D
1D
2D
Σ
3
0
P
Q
CI
CO
F583

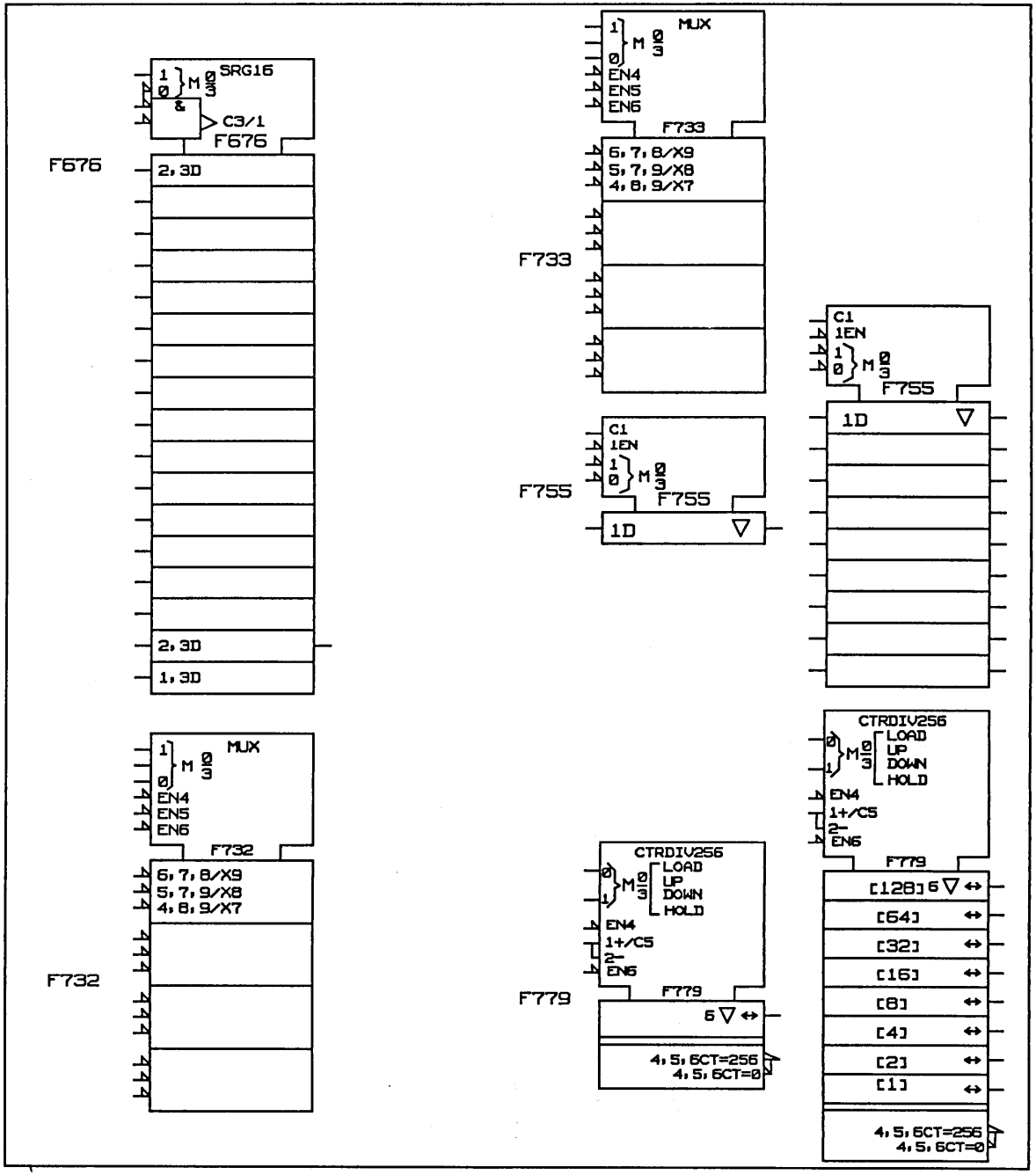

EN14
SRG8
R
G4
4C5/4
C3
C2
G1
F598
F598
1, SD
1, SD
Z6
2D
6, 14
3D
2D
7, 14
3D
Z7
2D
13, 14
3D
Z13
EN1
EN2
F620
1
2
F620
(SIZE)
G2
C2
EN
F604
1D, 2
1D, 2
≥1
G2
C1
EN
F604
F604
(SIZE)
MAX_DELAY=10000
EN1
EN2
F621
1
2
MAX_DELAY=10000
EN1
EN2
F621
F621
(SIZE)
MAX_DELAY=10000
G2
C2
EN
F605
MAX_DELAY=10000
G2
C2
EN
F605
F605
(SIZE)

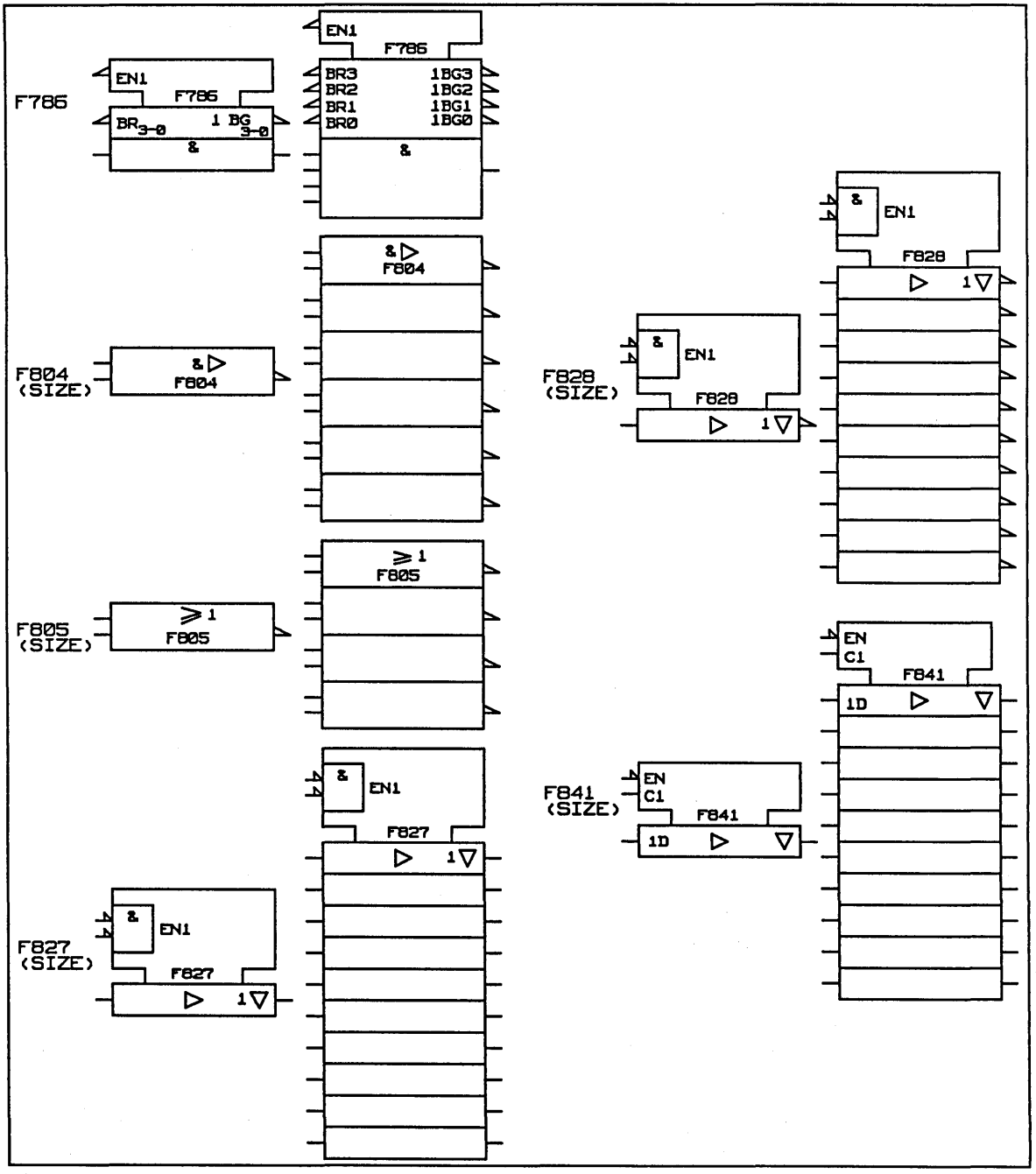

MAX_DELAY=10000
EN1
EN2
F622
1
2
MAX_DELAY=10000
EN1
EN2
F622
F622
(SIZE)
1
2
G3
3EN1[BA]
3EN2[AB]
F640
1
2
G3
3EN1[BA]
3EN2[AB]
F640
F640
(SIZE)
1
2
EN1
EN2
F623
1
2
EN1
EN2
F623
F623
(SIZE)
1
2
MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
F641
1
2
MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
F641
F641
(SIZE)
1
2

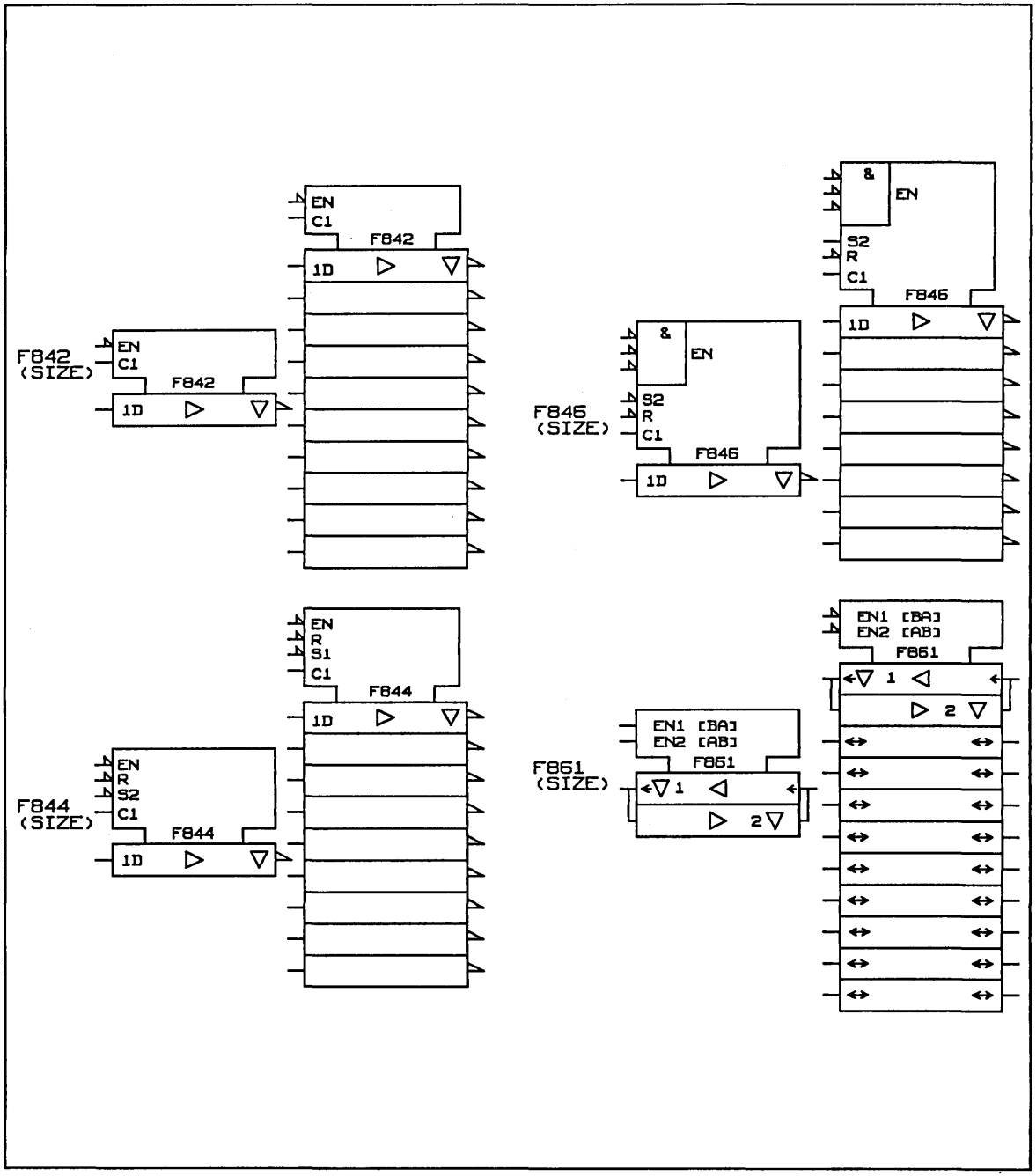

MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
F642
F642
(SIZE)
MAX_DELAY=10000
G3
EN1[BA]
EN2[AB]
C4
G5
C6
G7
F647
MAX_DELAY=10000
F647
(SIZE)
G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
F646
F646
(SIZE)
G3
3EN1[BA]
3EN2[AB]
C4
G5
C6
G7
F648
F648
(SIZE)

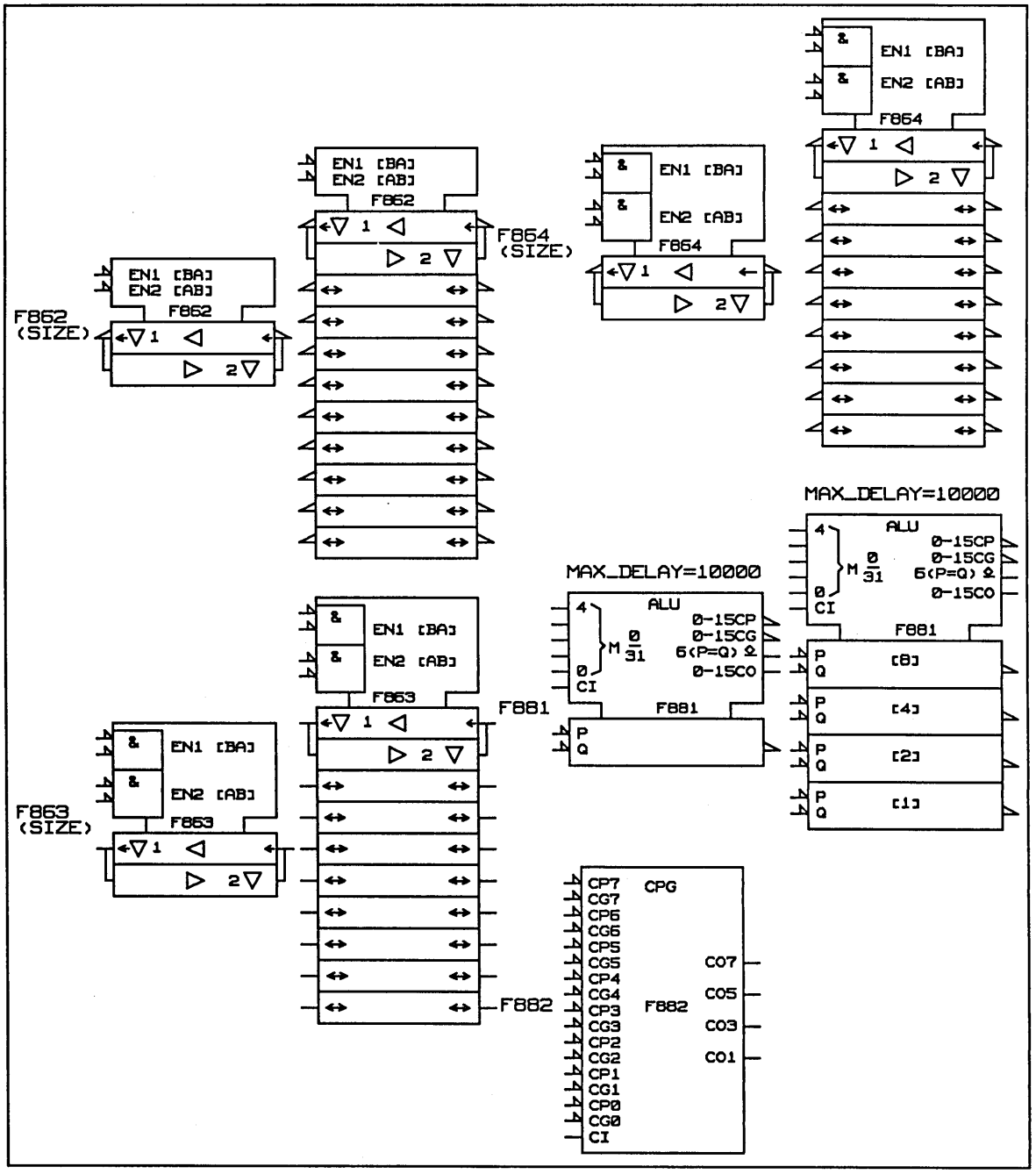

F651
(SIZE)
F652
(SIZE)
F653
(SIZE)
F654
(SIZE)
MAX_DELAY=10000
EN1[BA]
EN2[AB]
C4
G5
C6
G7
F651
F652
F653
F654

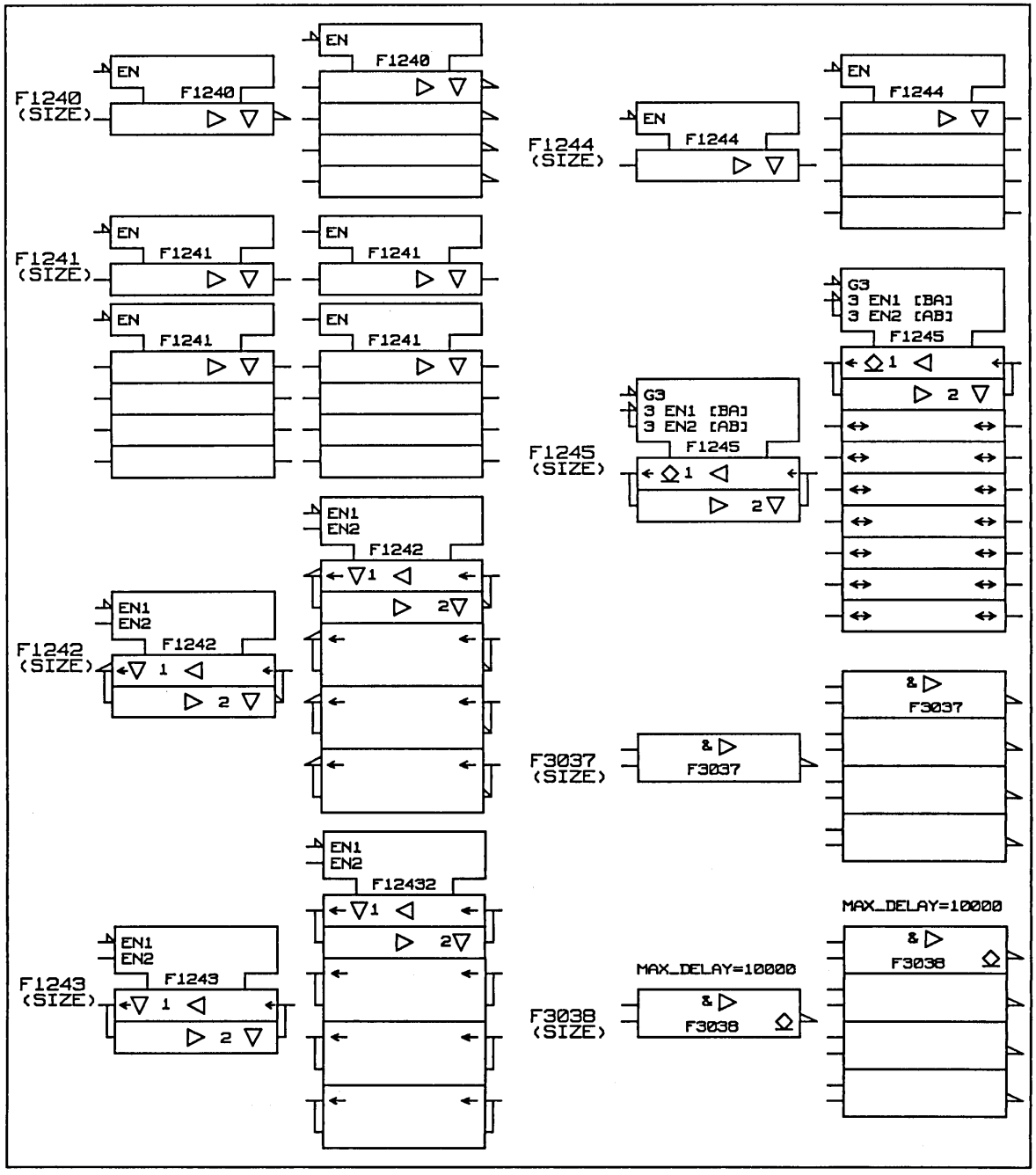

F655A
P3
≥1
EN4
2K
3,5,6 [EVEN]
7,8,9
10,11,12
3,5,6 [ODD]
7,8,9
10,11,12
F655A
Z12
Z11
Z10
Z9
Z8
Z7
Z6
Z5
F656A
P3
≥1
EN4
2K
3,5,6 [EVEN]
7,8,9
10,11,12
3,5,6 [ODD]
7,8,9
10,11,12
F656A
Z12
Z11
Z10
Z9
Z8
Z7
Z6
Z5
F657
M
G3[EVEN]
G4[ODD]
F657
2K
1;3[EVEN]
1;4[ODD]
0;4[EVEN]
0;4[ODD]
1
2
F670
RAM 4x4
A
C4[WRITE]
EN[READ]
F670
1A,4D
2A
F674
SRG16
M
C4
F674
3,4D <0,1,2>4D
3,4D

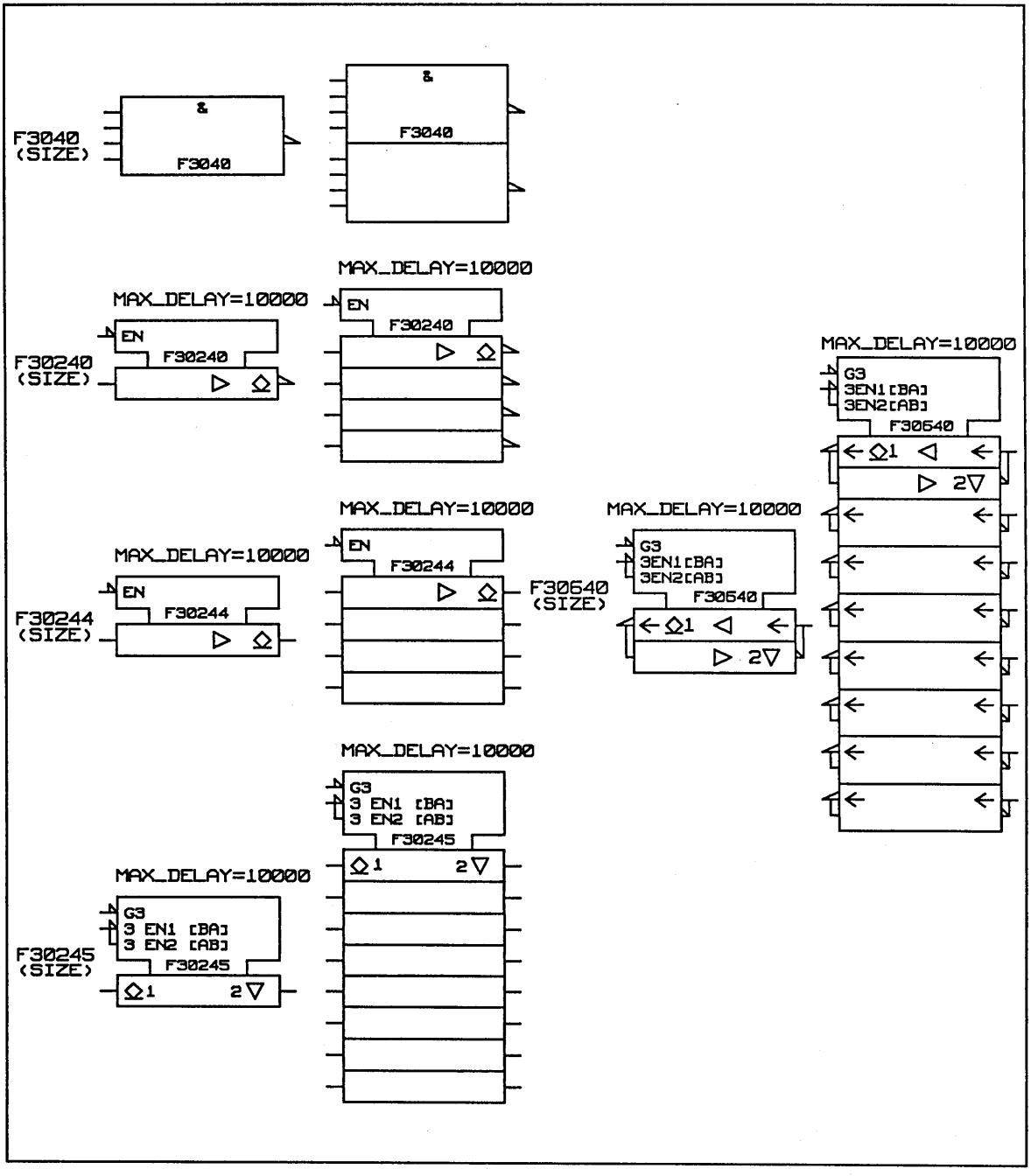

SRG16
M
C3/1
F676
2,3D
1,3D
MUX
EN4
EN5
EN6
F732
6,7,8/X9
5,7,9/X8
4,8,9/X7
F733
C1
1EN
F755
1D
CTRDIV256
LOAD
UP
DOWN
HOLD
1+/CS
EN6
F779
[128]
[64]
[32]
[16]
[8]
[4]
[2]
[1]
4,5,6CT=256
4,5,6CT=0

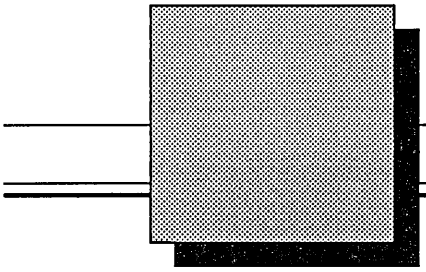

F785
EN1
F786
BR3-0
1 BG3-0
&
EN1
F786
BR3
BR2
BR1
BR0
1BG3
1BG2
1BG1
1BG0
&
F804
(SIZE)
&
F804
&
F804
F805
(SIZE)
≥1
F805
≥1
F805
F827
(SIZE)
&
EN1
F827
1
&
EN1
F827
1
F828
(SIZE)
&
EN1
F828
1
&
EN1
F828
1
F841
(SIZE)
EN
C1
1D
EN
C1
F841
1D
EN
C1
F841
1D


EN
C1
F842
1D
F842
(SIZE)
&
EN
S2
R
C1
F846
F846
(SIZE)
EN
R
S1
C1
F844
F844
(SIZE)
EN1 [BA]
EN2 [AB]
F861
F861
(SIZE)
1
2


EN1 [BA]
EN2 [AB]
F862
F862 (SIZE)
F864 (SIZE)
F864
F863
F863 (SIZE)
MAX_DELAY=10000
ALU
0-15CP
0-15CG
0-15CO
F881
F882
CPG
CO7
CO5
CO3
CO1


F1240
(SIZE)
EN
F1240
F1241
(SIZE)
EN
F1241
F1242
(SIZE)
EN1
EN2
F1242
1
2
F1243
(SIZE)
EN1
EN2
F1243
1
2
F1244
(SIZE)
EN
F1244
F1245
(SIZE)
G3
3 EN1 [BA]
3 EN2 [AB]
F1245
1
2
F3037
(SIZE)
&
F3037
F3038
(SIZE)
MAX_DELAY=10000
&
F3038
EN1
EN2
F12432


F3040
(SIZE)
&
F3040
&
F3040
MAX_DELAY=10000
EN
F30240
F30240
(SIZE)
MAX_DELAY=10000
EN
F30240
MAX_DELAY=10000
EN
F30244
F30244
(SIZE)
MAX_DELAY=10000
EN
F30244
F30540
(SIZE)
MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
F30540
1
2
MAX_DELAY=10000
G3
3EN1[BA]
3EN2[AB]
F30540
1
2
MAX_DELAY=10000
G3
3 EN1 [BA]
3 EN2 [AB]
F30245
1
2
MAX_DELAY=10000
G3
3 EN1 [BA]
3 EN2 [AB]
F30245
(SIZE)
1
2



The TTL and ANSI TTL Libraries

The TTL Library requires approximately 2735 Kbytes of disk storage, and the ANSI TTL Library requires approximately 2845 Kbytes of disk storage. The physical, timing, and simulation models for each library are identical and differ only in their body drawings. The part name for a component in either library is the same; the body drawing used is determined by the first library name encountered in the library search path (*ttl.lib* or *a74ttl.lib*).

The specifications used to construct the models in these libraries were taken from the Texas Instruments data books.

The release level of the TTL and ANSI TTL Libraries is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 85 components:

00	Quad 2–input positive NAND gate
01	Quad 2–input positive NAND gate with open collector output
02	Quad 2–input positive NOR gate
03	Quad 2–input positive NAND gate with open collector output
04	Hex inverter
05	Hex inverter with open collector output
06	Hex inverter buffer/driver with open collector output
07	Hex buffer/driver with open collector output
08	Quad 2–input positive AND gate
09	Quad 2–input positive AND gate with open collector output
10	Triple 3–input positive NAND gate
12	Triple 3–input positive NAND gate with open collector output
13	Dual 4–input positive NAND Schmitt trigger
14	Hex Schmitt–trigger inverter
16	Hex inverter buffer/driver with open collector high–voltage outputs

17	Hex buffer/driver with open collector output
20	Dual 4-input positive NAND gate
22	Dual 4-input positive NAND gate with open collector output
23	Expandable dual 4-input positive NOR gate with strobe
25	Dual 4-input positive NOR gate with strobe
26	Quad 2-input high voltage interface positive NAND gate
27	Triple 3-input positive NOR gate
28	Quad 2-input positive NOR gate
30	8-input positive NAND gate
32	Quad 2-input positive OR gate
33	Quad 2-input positive OR buffer with open collector outputs
37	Quad 2-input positive NAND buffer
38	Quad 2-input positive NAND buffer with open collector outputs
40	Dual 4-input positive NAND buffer
45	BCD to decimal decoder
47	BCD to 7-segment decoder
48	BCD to 7-segment decoder/driver
50	Dual 2-wide 2-input AND-OR-invert gates
51	AND-OR-invert gate
53	Expandable 4-wide AND-OR-invert gates

54	4-wide AND-OR-invert gates
60	Dual 4-input expanders
70	AND-gated JK positive edge triggered flip-flop with preset and clear
72	AND-gated JK master-slave flip-flop with preset and clear
73	Dual JK flip-flop with clear
74	Dual D-type positive edge-triggered flip-flop with preset and clear
75	4-bit bistable latches
76	Dual JK flip-flop with preset and clear
80	Gated full adders
81	Gated full adders
82	2-bit binary full adders
85	4-bit magnitude comparator
86	Quad 2-input exclusive-OR gates
94	4-bit shift registers
96	5-bit shift registers
97	Synchronous 6-bit binary rate multipliers
107	Dual JK flip-flop with clear
109	Dual JK positive edge-triggered flip-flop with preset and clear
110	AND-gated JK master-slave flip-flop with data lockout
111	Dual JK master-slave flip-flop with data lockout

116	Dual 4-bit latches
120	Dual pulse synchronizers/drivers
121	Monostable multivibrators
122	Retriggerable monostable multivibrators with clear
123	Dual retriggerable monostable multivibrators with clear
125	Quad bus buffer gates with three-state outputs
126	Quad bus buffer gates with three-state outputs
128	50-ohm line driver
132	Quad 2-input positive NAND Schmitt triggers
142	Counter/latch/decoder/driver
143	Counter/latch/decoder/driver
144	Counter/latch/decoder/driver
145	BCD-to-decimal decoder/driver for lamps, delays, MOS
147	10-line decimal to 4-line BCD priority encoder
148	8-line to 3-line octal priority encoder
150	1-of-16 data selector/multiplexer
153	Dual 4-line to 1-line data selector/multiplexer
154	4-to-16 line decoder/demultiplexer
155	Decoder/demultiplexer
156	Decoder/demultiplexer with open collector outputs
157	Quad 2-line to 1-line data selector/multiplexer
159	4-to-16 line decoder/demultiplexer
176	35-MHz presettable decade counters/latches
177	35-MHz presettable binary counters/latches
179	4-bit universal shift registers

185	Binary–to–BCD converter
198	8–bit bidirectional universal shift registers
265	Quad complementary output elements
273	Octal D–type flip–flop
376	Quad JK flip–flops

Application Notes

Monostable Multivibrators

The 74121, 74122, and 74123 models fully support the simulation and timing behavior of a retrigerrable multivibrator – infinite retriggering edges and external resettability at any time.

To use the simulation model, logic initialization or initial depositing of the same value (either 0 or 1) to internal signals D0 and D1 must be performed.

To use the timing verification model, the following must be observed:

- The Timing Verifier's directives file *(verifier.cmd)* must include the directive:

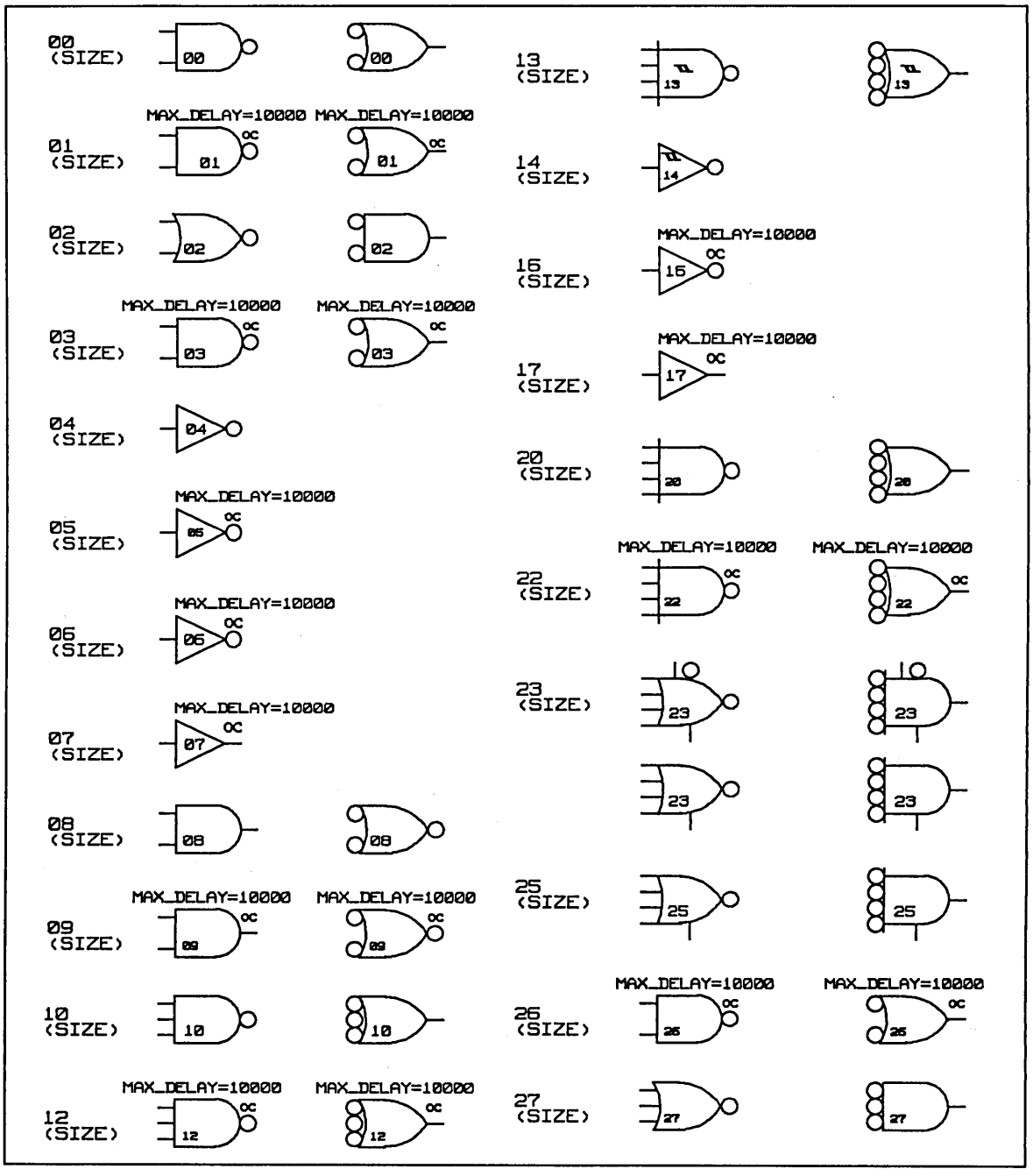
  ```
  LATCH_ERR_MODEL CLOSED;
  ```

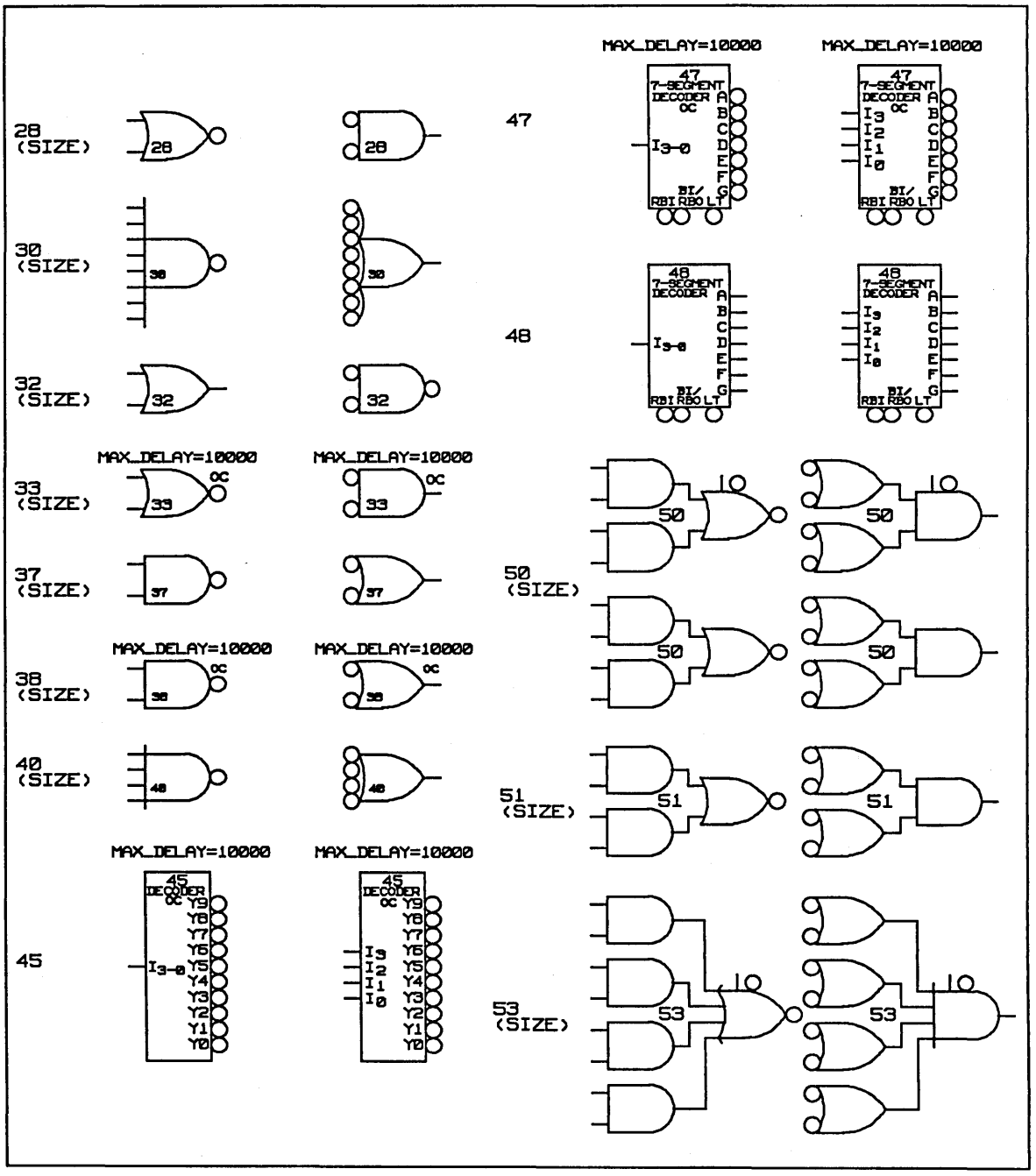
- The first trigger edge must occur after 'PULSE_WIDTH' ns.

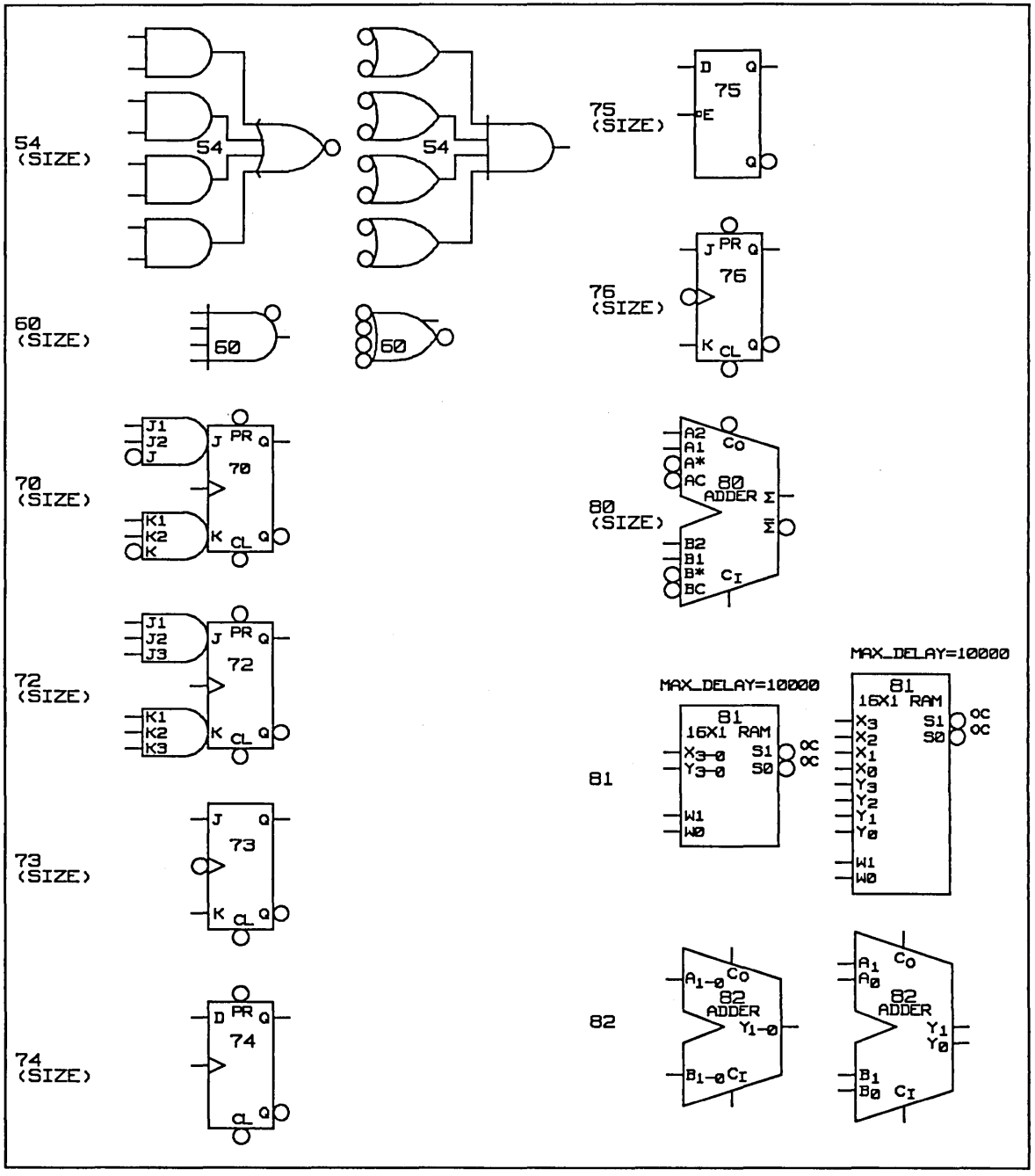
- The maximum trigger frequency is

  ```
  2 * RETRIG_DIV2 -1
  ```

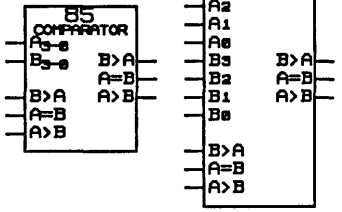
  edges per 'PULSE_WIDTH' ns. Since RETRIG_DIV2 is defined to be 6 in the model, 2*6–1=11 clock edges are permitted in any 'PULSE_WIDTH' ns interval. If an application requires a greater trigger frequency, RETRIG_DIV2 must be redefined in the model.


00 (SIZE)
00
00
MAX_DELAY=10000
MAX_DELAY=10000
01 (SIZE)
01
01
02 (SIZE)
02
02
MAX_DELAY=10000
MAX_DELAY=10000
03 (SIZE)
03
03
04 (SIZE)
04
MAX_DELAY=10000
05 (SIZE)
05
MAX_DELAY=10000
06 (SIZE)
06
MAX_DELAY=10000
07 (SIZE)
07
08 (SIZE)
08
08
MAX_DELAY=10000
MAX_DELAY=10000
09 (SIZE)
09
09
10 (SIZE)
10
10
MAX_DELAY=10000
MAX_DELAY=10000
12 (SIZE)
12
12
13 (SIZE)
13
13
14 (SIZE)
14
MAX_DELAY=10000
16 (SIZE)
16
MAX_DELAY=10000
17 (SIZE)
17
20 (SIZE)
20
20
MAX_DELAY=10000
MAX_DELAY=10000
22 (SIZE)
22
22
23 (SIZE)
23
23
23
23
25 (SIZE)
25
25
MAX_DELAY=10000
MAX_DELAY=10000
26 (SIZE)
26
26
27 (SIZE)
27
27


28 (SIZE)
28
28
30 (SIZE)
30
30
32 (SIZE)
32
32
MAX_DELAY=10000
MAX_DELAY=10000
33 (SIZE)
33
33
37 (SIZE)
37
37
MAX_DELAY=10000
MAX_DELAY=10000
38 (SIZE)
38
38
40 (SIZE)
40
40
MAX_DELAY=10000
MAX_DELAY=10000
45
45
DECODER
OC
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
I3-0
I3
I2
I1
I0
MAX_DELAY=10000
MAX_DELAY=10000
47
47
7-SEGMENT
DECODER
OC
A
B
C
D
E
F
G
I3-0
BI/
RBI RBO LT
I3
I2
I1
I0
48
48
7-SEGMENT
DECODER
50 (SIZE)
50
51 (SIZE)
51
53 (SIZE)
53

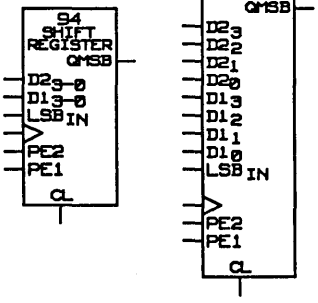

54
(SIZE)
54
54
60
(SIZE)
60
60
70
(SIZE)
J1
J2
J
K1
K2
K
J PR Q
70
K CL Q
72
(SIZE)
J1
J2
J3
K1
K2
K3
J PR Q
72
K CL Q
73
(SIZE)
J Q
73
K CL Q
74
(SIZE)
D PR Q
74
CL Q
75
(SIZE)
D Q
75
E
Q
76
(SIZE)
J PR Q
76
K CL Q
80
(SIZE)
A2
A1
A*
AC
80
ADDER
Σ
Σ
B2
B1
B*
BC
CO
CI
81
MAX_DELAY=10000
81
16X1 RAM
X3-0
Y3-0
S1
S0
W1
W0
MAX_DELAY=10000
81
16X1 RAM
X3
X2
X1
X0
Y3
Y2
Y1
Y0
S1
S0
W1
W0
82
A1-0
CO
82
ADDER
Y1-0
B1-0
CI
A1
A0
CO
82
ADDER
Y1
Y0
B1
B0
CI

85

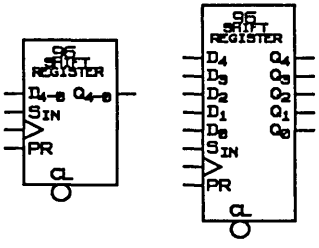


86
(SIZE)

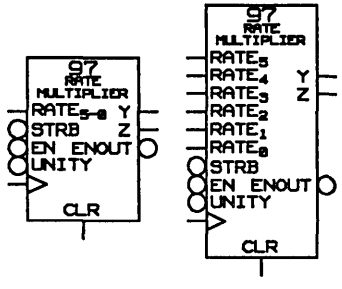
94



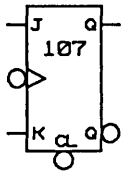
96



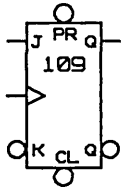
97



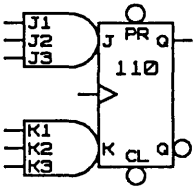
107
(SIZE)



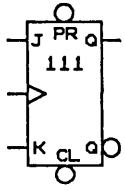
109
(SIZE)



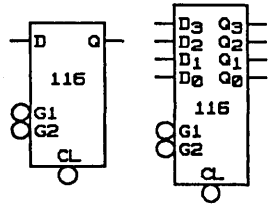
110
(SIZE)



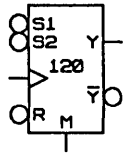
111
(SIZE)



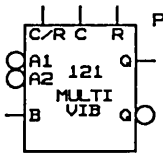
116
(SIZE)



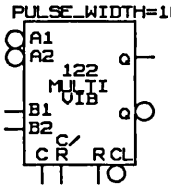
120
(SIZE)



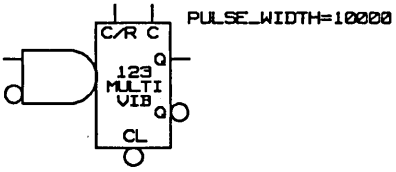
121



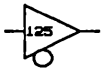
122



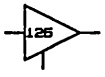
123



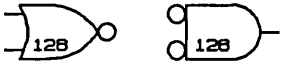
125
(SIZE)



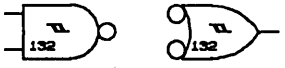
126
(SIZE)



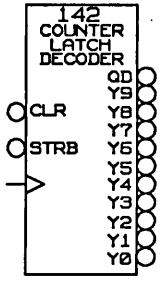
128
(SIZE)



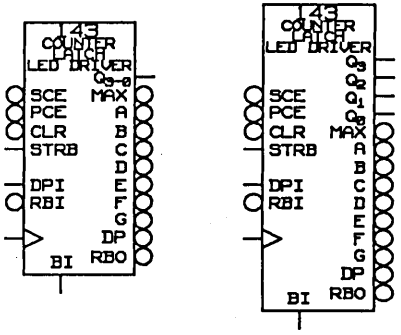
132
(SIZE)



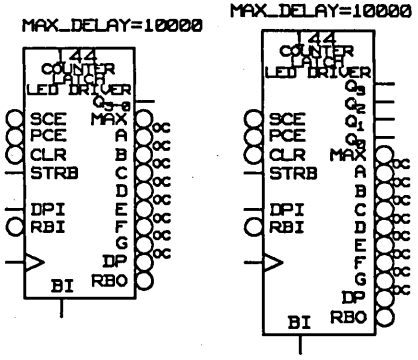
142



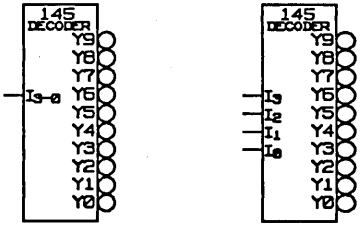
143



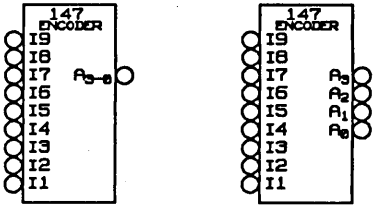
144



145



147



148

155

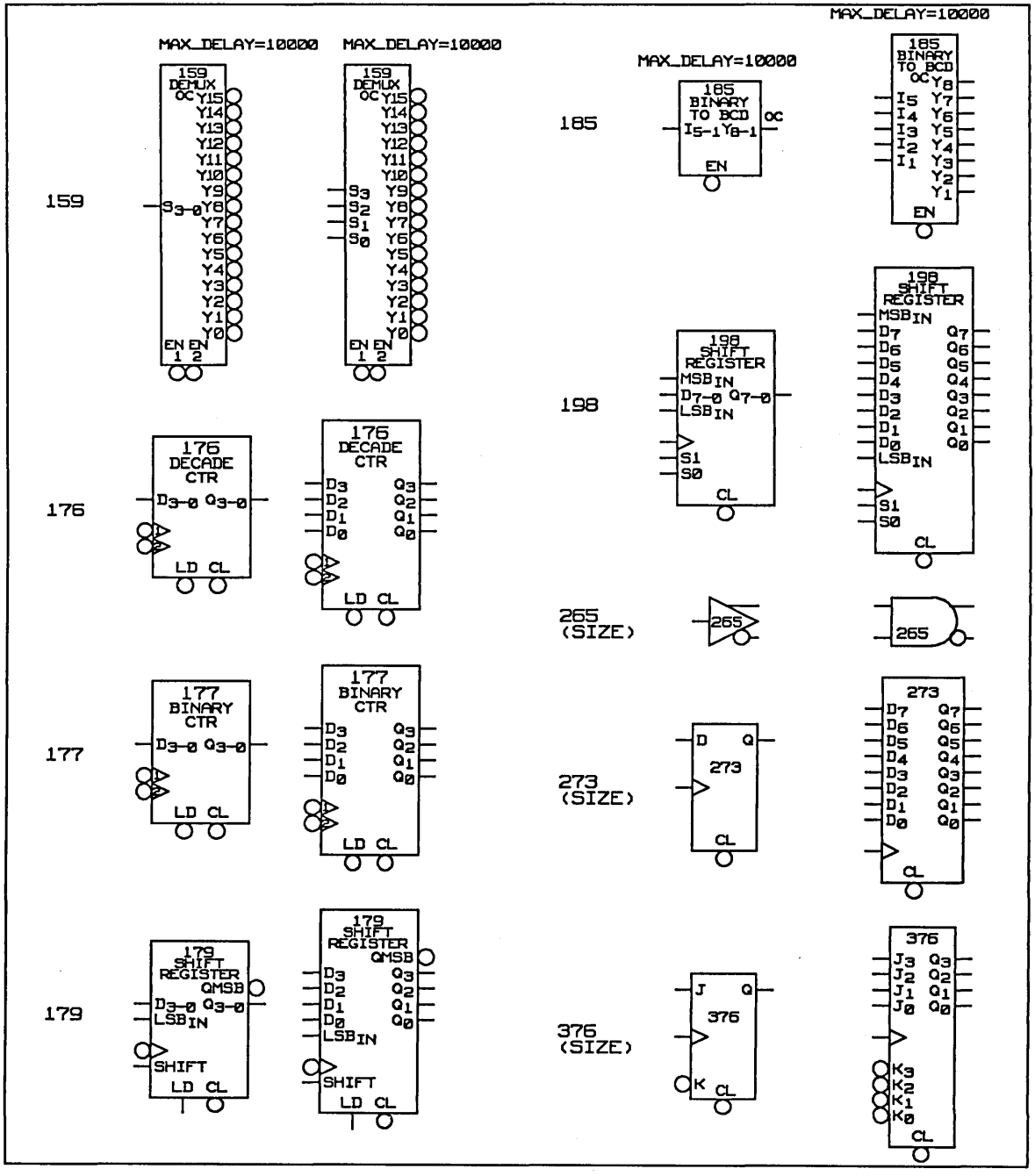
150
(SIZE)

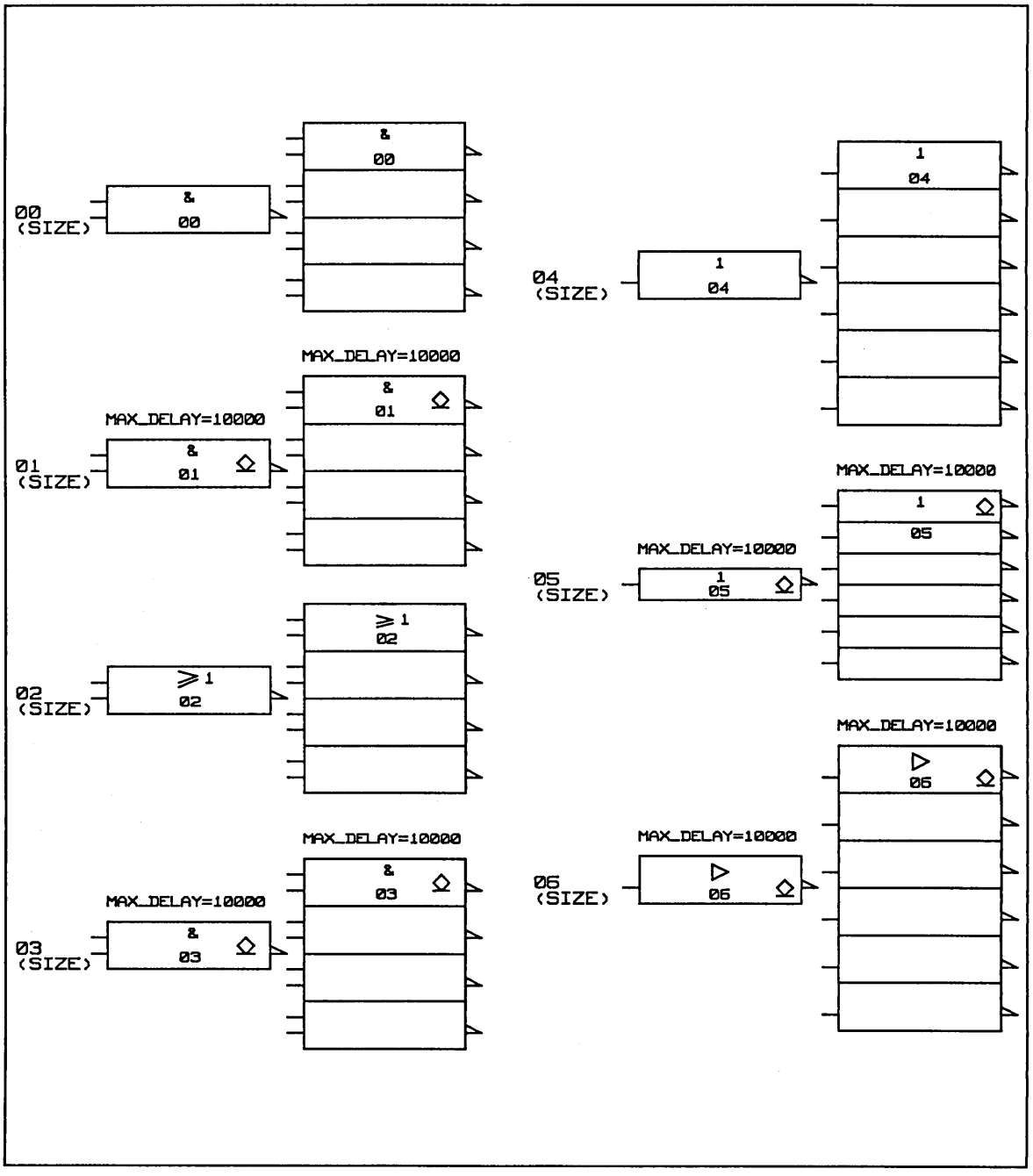
156

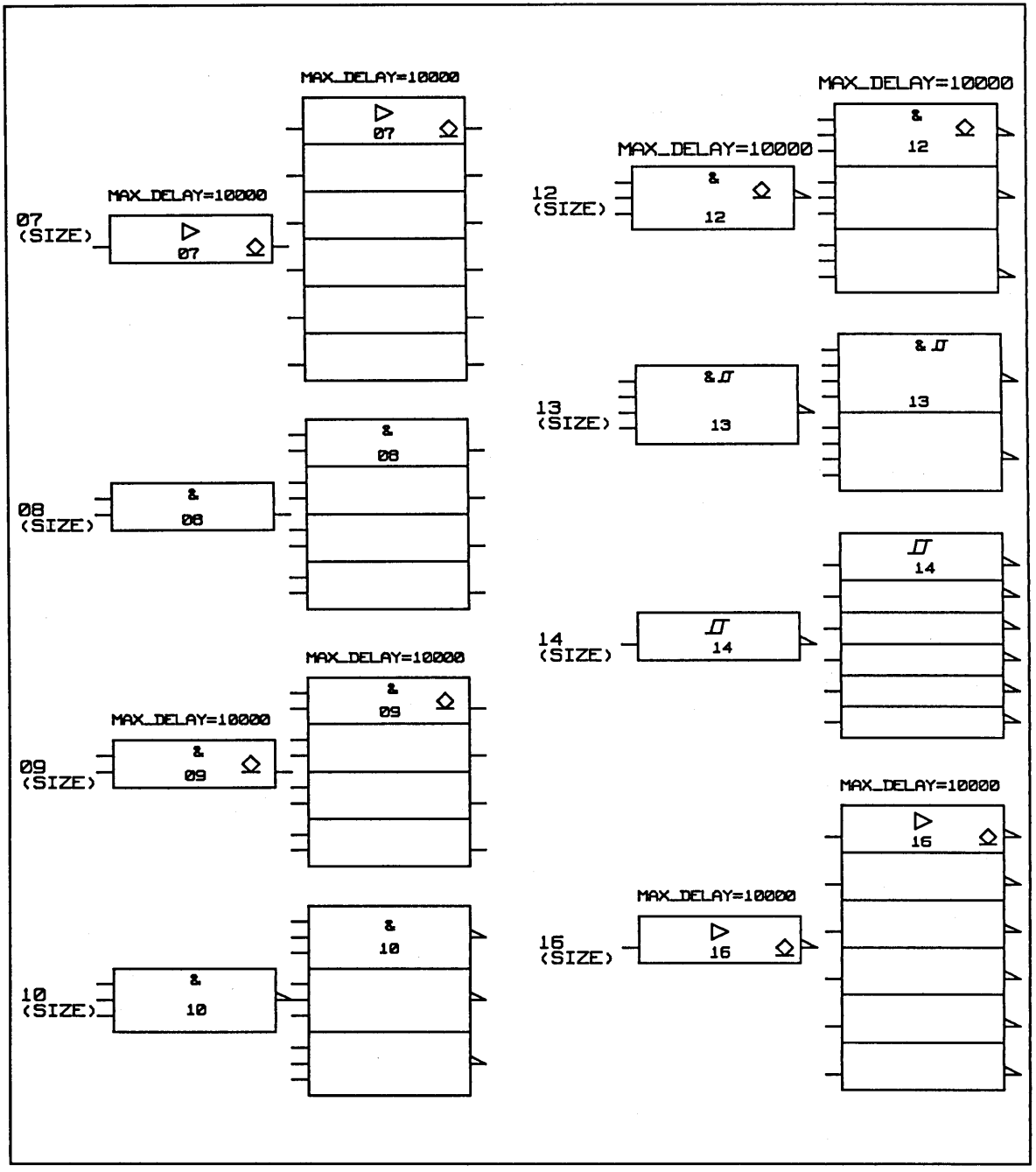
153
(SIZE)

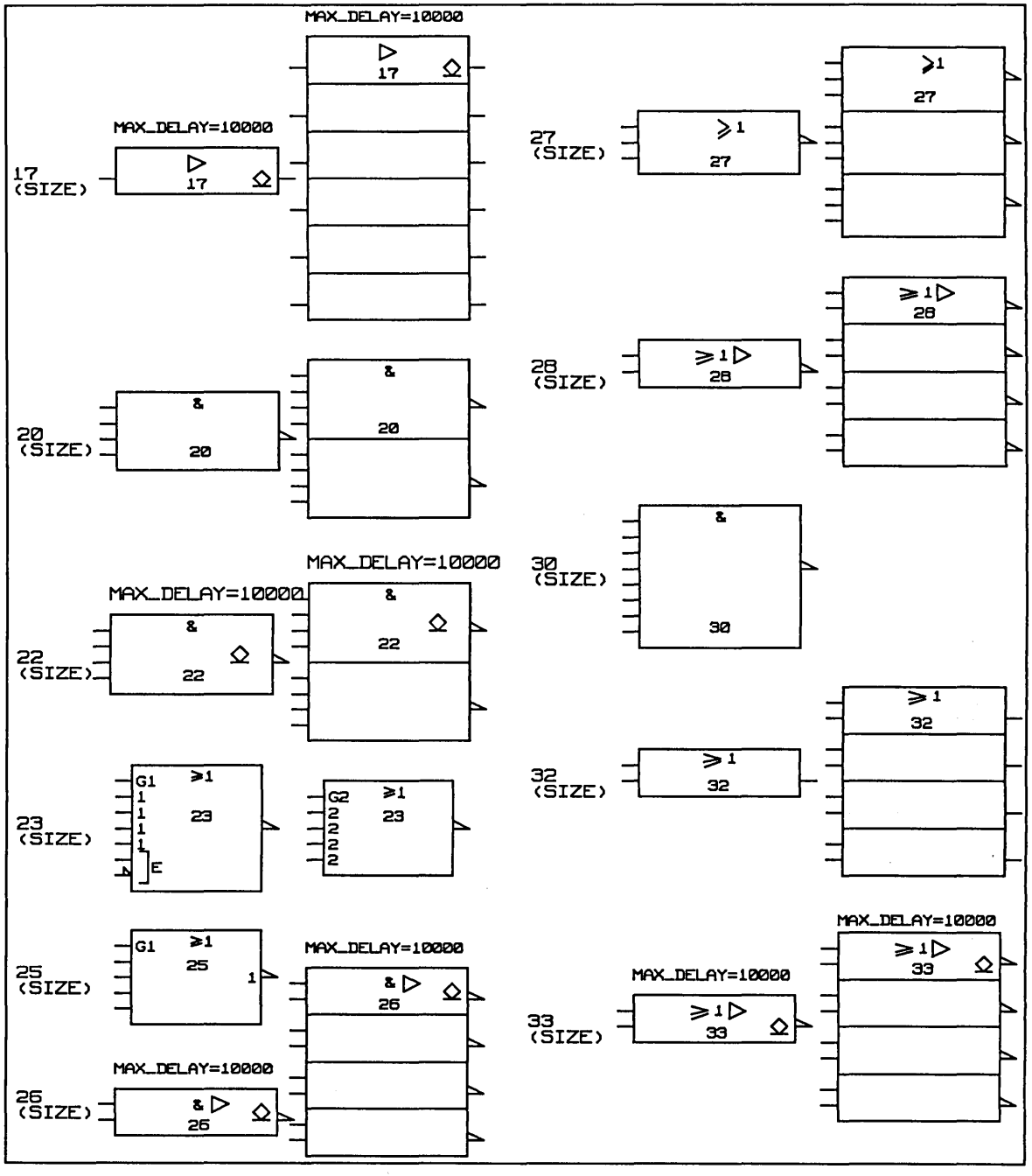
154

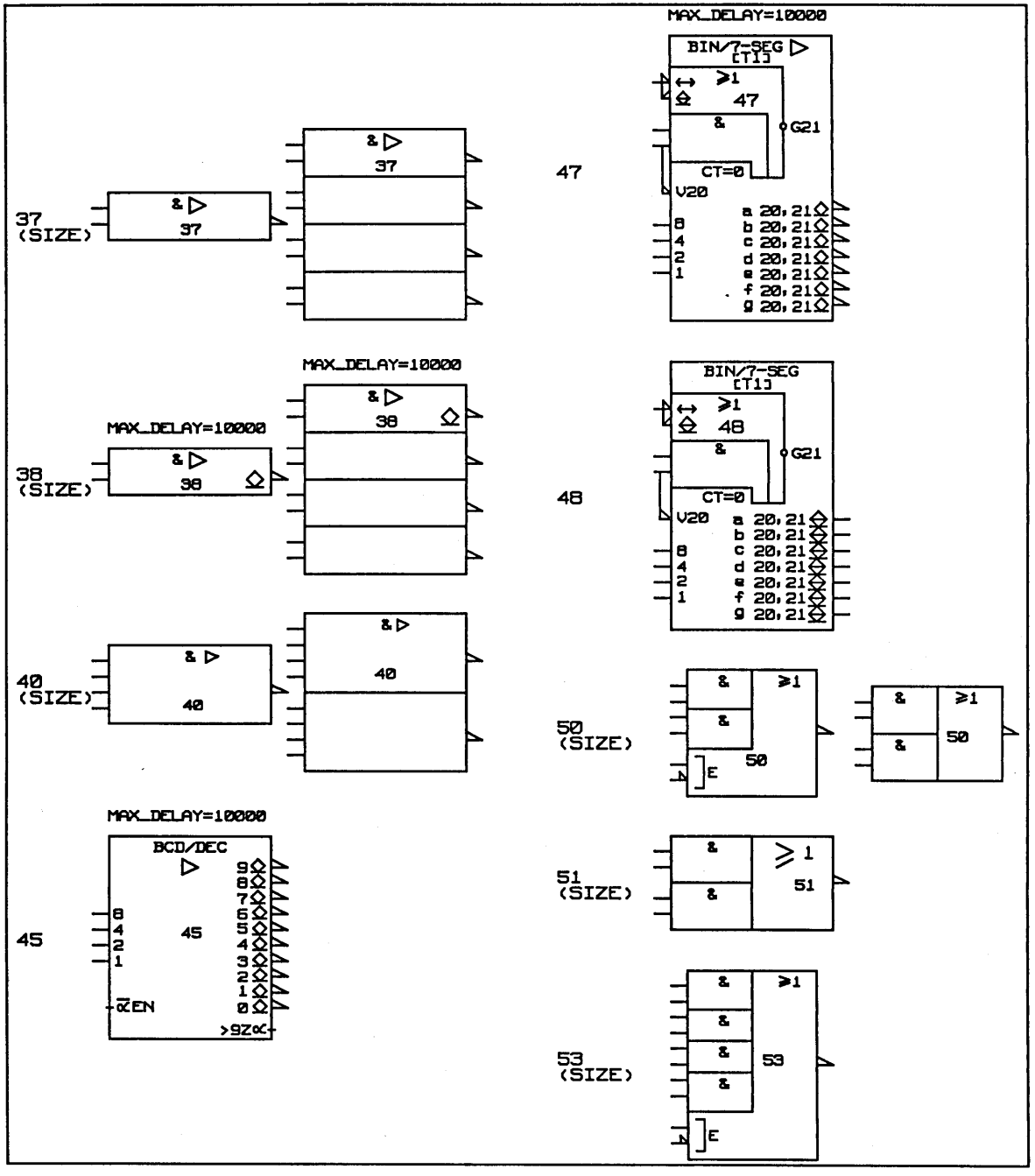
157
(SIZE)

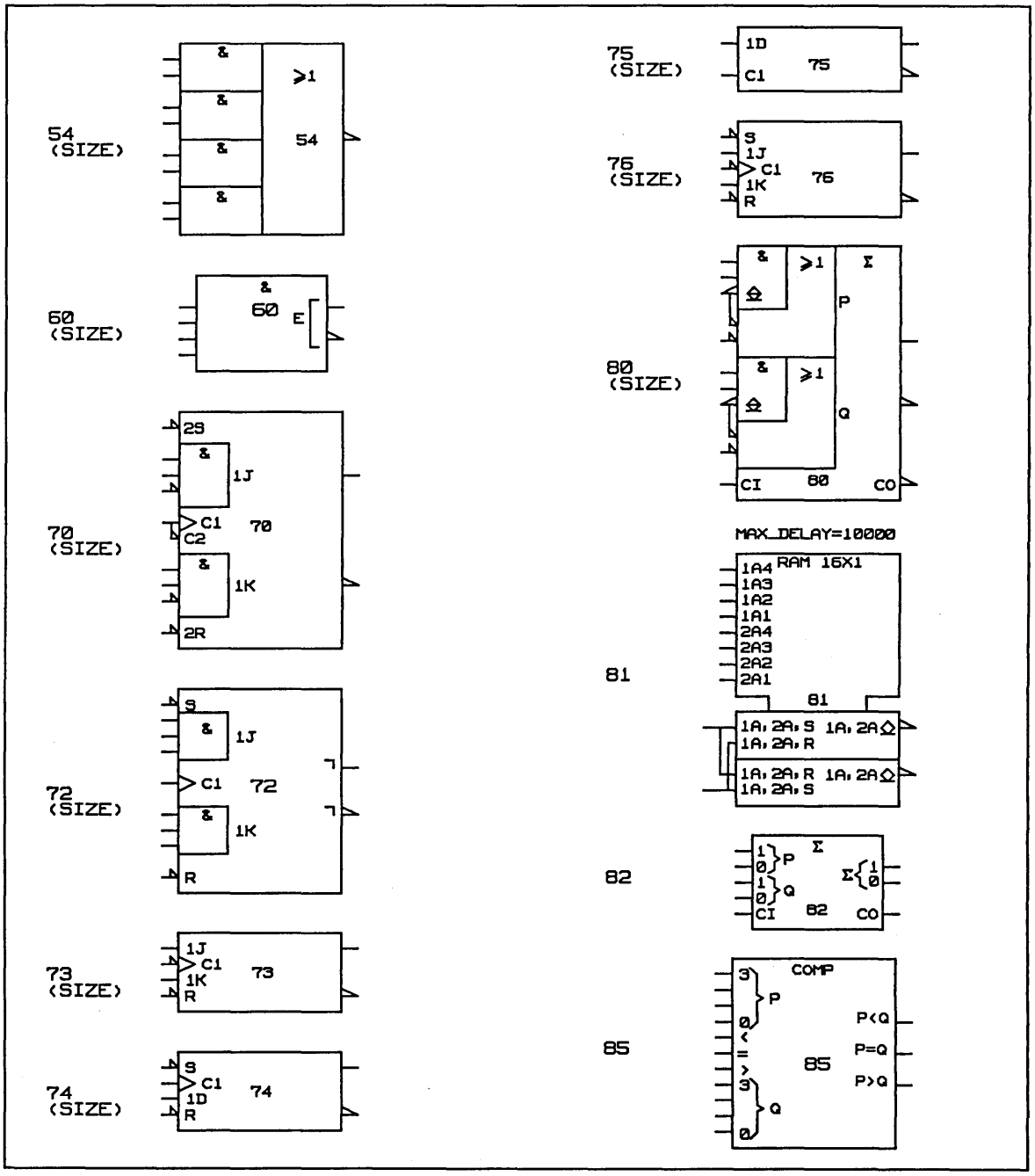

MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
MAX_DELAY=10000
159
159 DEMUX OC Y15 Y14 Y13 Y12 Y11 Y10 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 S3-0 EN EN 1 2
159 DEMUX OC Y15 Y14 Y13 Y12 Y11 Y10 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 S3 S2 S1 S0 EN EN 1 2
185
185 BINARY TO BCD OC I5-1 Y8-1 EN
185 BINARY TO BCD OC Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 I5 I4 I3 I2 I1 EN
176
176 DECADE CTR D3-0 Q3-0 LD CL
176 DECADE CTR D3 D2 D1 D0 Q3 Q2 Q1 Q0 LD CL
198
198 SHIFT REGISTER MSBIN D7-0 Q7-0 LSBIN S1 S0 CL
198 SHIFT REGISTER MSBIN D7 D6 D5 D4 D3 D2 D1 D0 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 LSBIN S1 S0 CL
265
(SIZE)
265
265
177
177 BINARY CTR D3-0 Q3-0 LD CL
177 BINARY CTR D3 D2 D1 D0 Q3 Q2 Q1 Q0 LD CL
273
(SIZE)
D Q 273 CL
273 D7 D6 D5 D4 D3 D2 D1 D0 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 CL
179
179 SHIFT REGISTER QMSB D3-0 Q3-0 LSBIN SHIFT LD CL
179 SHIFT REGISTER QMSB D3 D2 D1 D0 Q3 Q2 Q1 Q0 LSBIN SHIFT LD CL
376
(SIZE)
J Q 376 K CL
376 J3 J2 J1 J0 Q3 Q2 Q1 Q0 K3 K2 K1 K0 CL

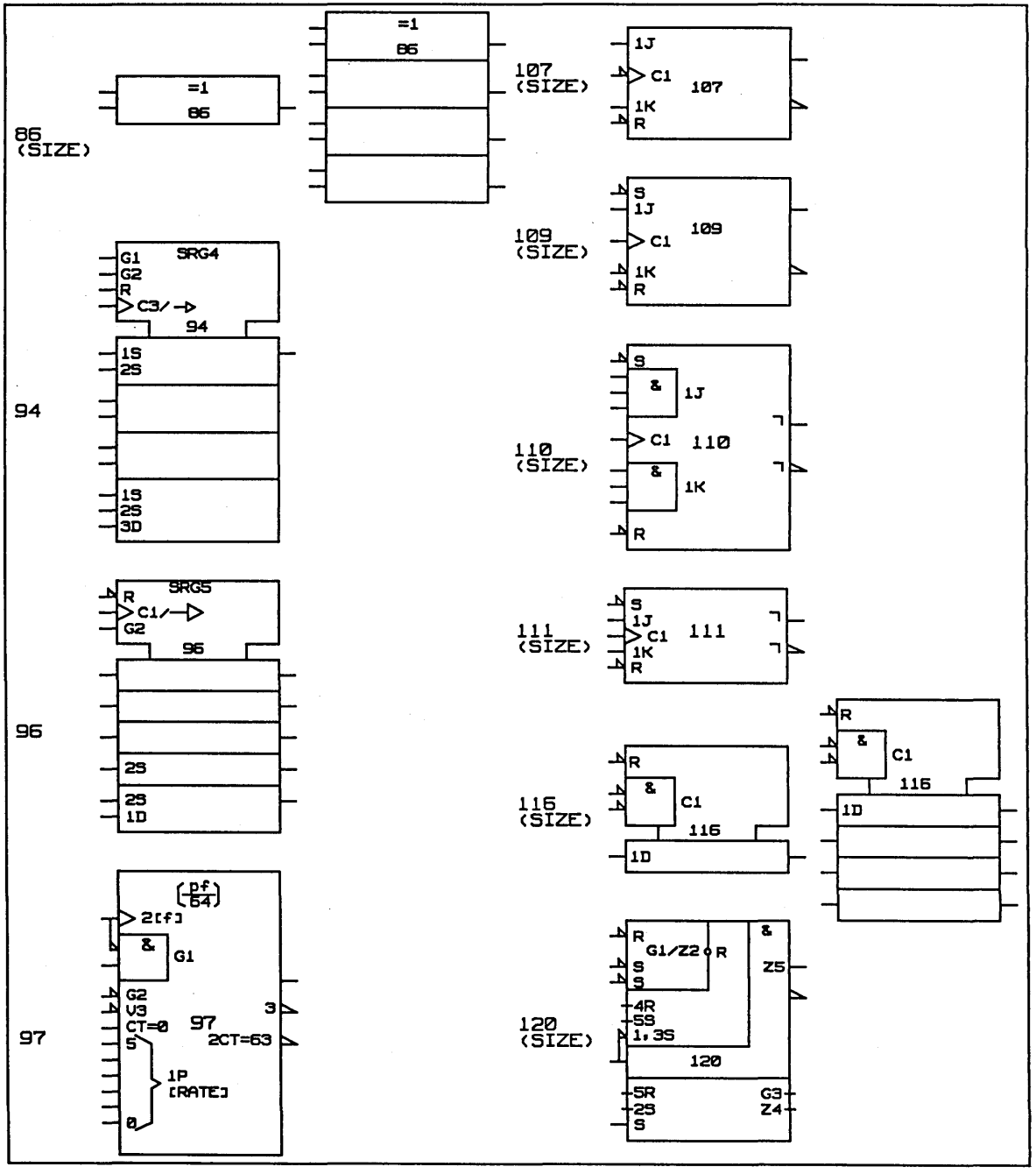

00
(SIZE)
&
00
&
00
01
(SIZE)
MAX_DELAY=10000
&
01
MAX_DELAY=10000
&
01
02
(SIZE)
≥1
02
≥1
02
03
(SIZE)
MAX_DELAY=10000
&
03
MAX_DELAY=10000
&
03
04
(SIZE)
1
04
1
04
05
(SIZE)
MAX_DELAY=10000
1
05
MAX_DELAY=10000
1
05
06
(SIZE)
MAX_DELAY=10000
▷
06
MAX_DELAY=10000
▷
06

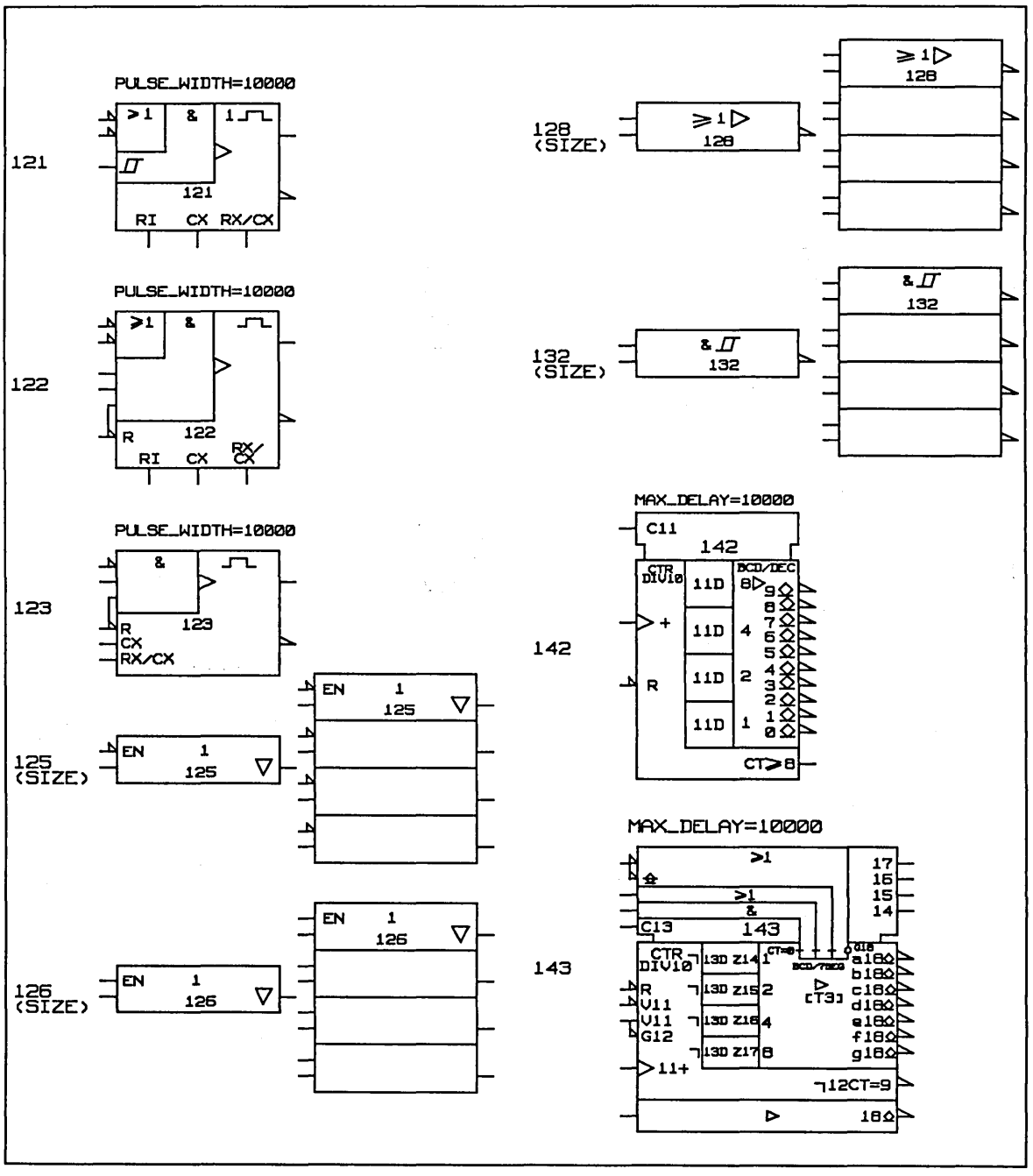

MAX_DELAY=10000
07
07
(SIZE)
MAX_DELAY=10000
07
08
&
08
08
(SIZE)
&
08
MAX_DELAY=10000
09
&
09
MAX_DELAY=10000
09
(SIZE)
&
09
10
&
10
10
(SIZE)
&
10
MAX_DELAY=10000
12
&
12
MAX_DELAY=10000
12
(SIZE)
&
12
13
&
13
13
(SIZE)
&
13
14
14
(SIZE)
14
MAX_DELAY=10000
16
MAX_DELAY=10000
16
(SIZE)
16


MAX_DELAY=10000
17
17
(SIZE)
MAX_DELAY=10000
17
20
(SIZE)
&
20
&
20
MAX_DELAY=10000
22
(SIZE)
MAX_DELAY=10000
&
22
&
22
23
(SIZE)
G1
1
1
1
1
4
≥1
23
E
G2
2
2
2
2
2
≥1
23
25
(SIZE)
G1
≥1
25
1
MAX_DELAY=10000
&
26
26
(SIZE)
MAX_DELAY=10000
&
26
27
(SIZE)
≥1
27
≥1
27
28
(SIZE)
≥1
28
≥1
28
30
(SIZE)
&
30
32
(SIZE)
≥1
32
≥1
32
33
(SIZE)
MAX_DELAY=10000
≥1
33
MAX_DELAY=10000
≥1
33

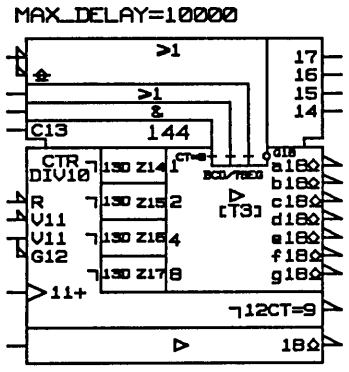

MAX_DELAY=10000
BIN/7-SEG
[T1]
47
G21
CT=0
V20
a 20,21
b 20,21
c 20,21
d 20,21
e 20,21
f 20,21
g 20,21
8
4
2
1
37
(SIZE)
38
(SIZE)
40
(SIZE)
48
50
(SIZE)
51
(SIZE)
53
(SIZE)
45
BCD/DEC
EN
E


54
(SIZE)
&
≥1
54
60
(SIZE)
60
E
70
(SIZE)
2S
1J
C1
C2
70
1K
2R
72
(SIZE)
S
1J
C1
72
1K
R
73
(SIZE)
1J
C1
1K
R
73
74
(SIZE)
S
C1
1D
R
74
75
(SIZE)
1D
C1
75
76
(SIZE)
S
1J
C1
1K
R
76
80
(SIZE)
Σ
P
Q
CI
80
CO
MAX_DELAY=10000
81
RAM 16X1
1A4
1A3
1A2
1A1
2A4
2A3
2A2
2A1
81
1A, 2A, S
1A, 2A, R
82
P
Q
CI
82
CO
85
COMP
P<Q
P=Q
P>Q
85

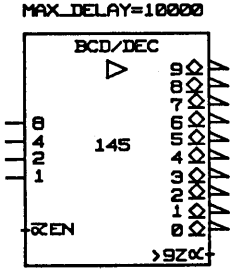

=1
86
86
(SIZE)
=1
86
107
(SIZE)
1J
C1
107
1K
R
S
1J
C1
109
1K
R
109
(SIZE)
G1
G2
R
C3/→
SRG4
94
1S
2S
94
1S
2S
3D
S
&
1J
C1
110
&
1K
R
110
(SIZE)
R
C1/→
G2
SRG5
96
2S
2S
1D
96
S
1J
C1
1K
R
111
111
(SIZE)
R
&
C1
116
1D
R
&
C1
116
1D
116
(SIZE)
(pf)
(64)
2[f]
&
G1
G2
V3
CT=0
S
97
3
2CT=63
1P
[RATE]
0
97
R
G1/Z2
R
S
S
&
Z5
4R
5S
1,3S
120
5R
2S
S
G3
Z4
120
(SIZE)


PULSE_WIDTH=10000
121
RI CX RX/CX
PULSE_WIDTH=10000
122
R
RI CX RX/CX
PULSE_WIDTH=10000
123
R
CX
RX/CX
125
(SIZE)
EN
126
(SIZE)
128
(SIZE)
132
(SIZE)
MAX_DELAY=10000
142
C11
CTR DIV10
BCD/DEC
R
CT>8
MAX_DELAY=10000
143
C13
CTR DIV10
R
V11
V11
G12
12CT=9

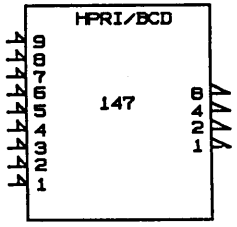
144



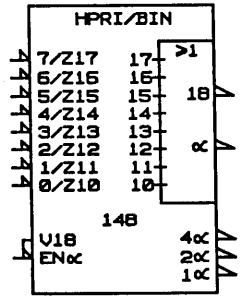
145



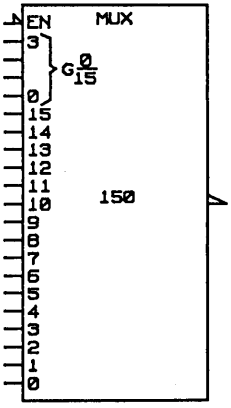
147



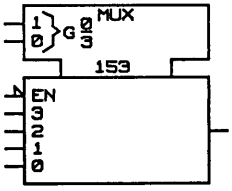
148



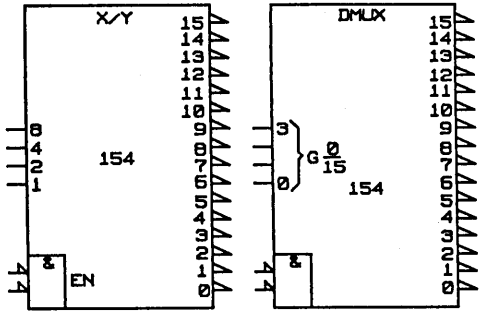
150
(SIZE)



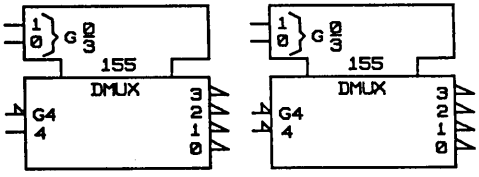
153
(SIZE)

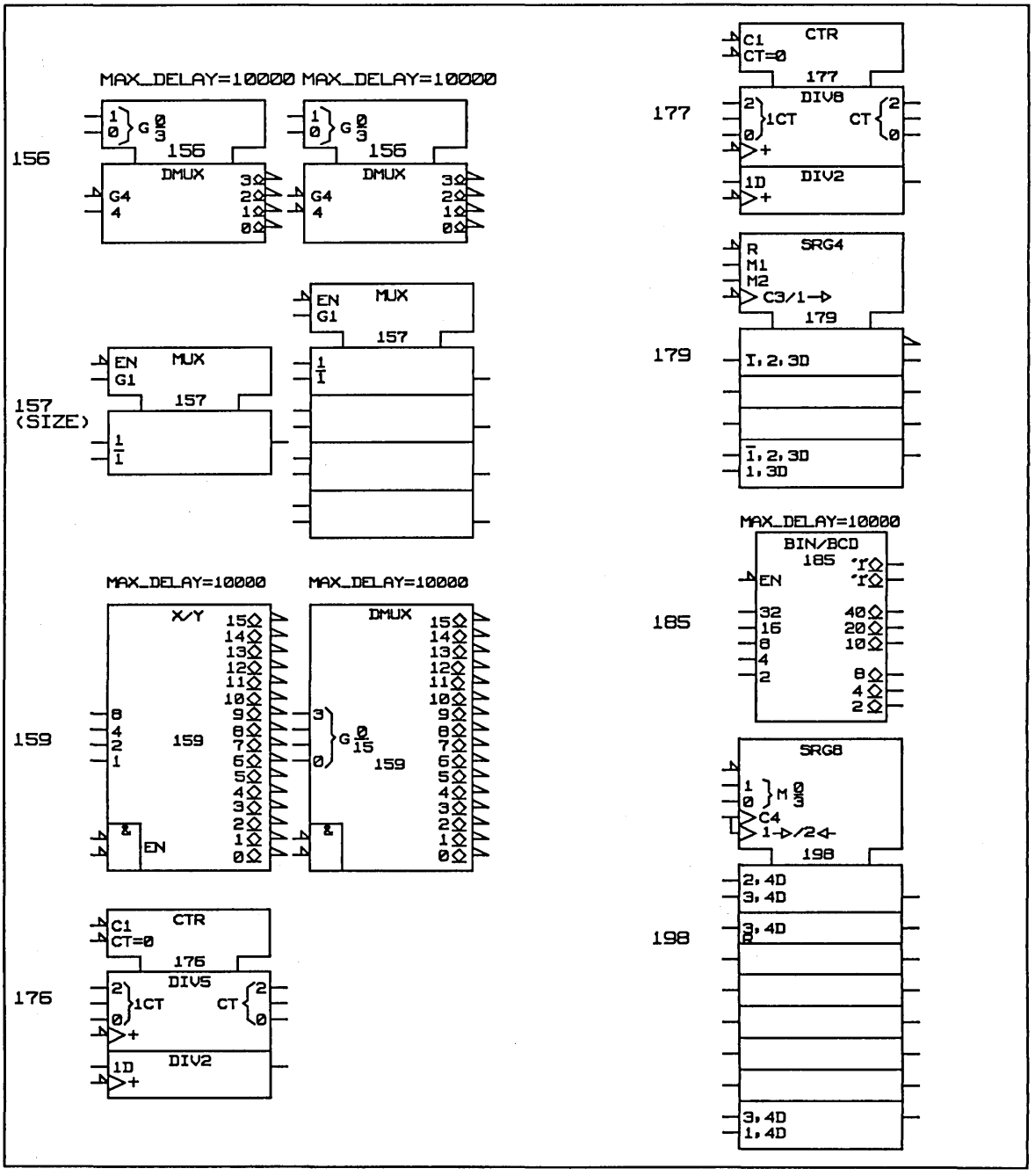


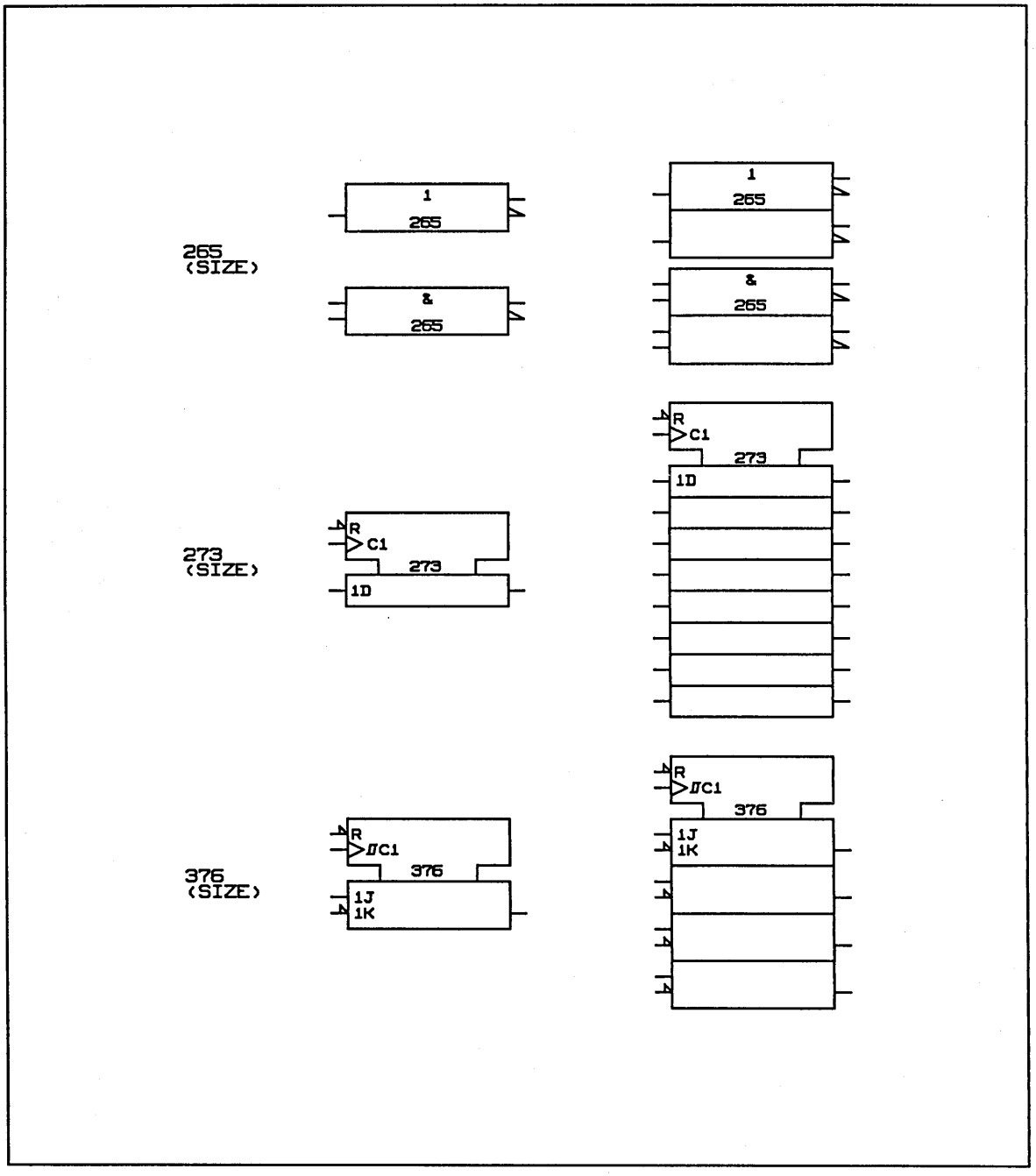
154

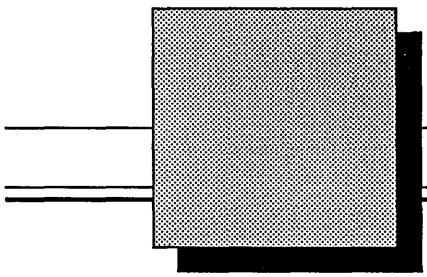


155




156
MAX_DELAY=10000
MAX_DELAY=10000
DMUX
G4
157
(SIZE)
MUX
EN
G1
159
MAX_DELAY=10000
MAX_DELAY=10000
X/Y
DMUX
176
CTR
C1
CT=0
DIV5
DIV2
177
CTR
DIV8
DIV2
179
SRG4
R
M1
M2
C3/1
185
MAX_DELAY=10000
BIN/BCD
198
SRG8
C4
1-/2


265
(SIZE)
1
265
&
265
1
265
&
265
273
(SIZE)
R
C1
273
1D
R
C1
273
1D
376
(SIZE)
R
C1
376
1J
1K
R
C1
376
1J
1K



The FACT Library

The CMOS FACT Library requires approximately 2570 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the Fairchild data books.

The release level of the FACT Library is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 83 components:

AC00	Quad 2-input NAND
AC02	Quad 2-input NOR
AC04	Hex inverter
AC08	Quad 2-input AND
AC10	Triple 3-input NAND
AC11	Triple 3-input AND
AC14	Hex inverter Schmitt-trigger
AC20	Dual 4-input NAND
AC32	Quad 2-input OR
AC74	Dual positive-edge-triggered D flip-flop
AC109	Dual JKbar positive-edge-triggered flip-flop
AC138	3-to-8 line decoders/multiplexers
AC139	Dual 2-to-4 line decoders/multiplexers
AC151	1-of-8 data selectors/multiplexers
AC153	Dual 4-line to 1-line data multiplexer
AC157	Quad 2-to-1-line non-inverting multiplexer
AC158	Quad 2-to-1-line inverting data multiplexer
AC160	4-bit synchronous decade counters with direct clear
AC161	4-bit synchronous binary counters with direct clear
AC163	4-bit synchronous binary counters with synch clear

AC168	4-bit synchronous decade up/down counters
AC169	4-bit synchronous binary up/down counters
AC174	Hex D-type flip-flops
AC175	Quad D-type flip-flops
AC240	Octal inverting 3-state bus transceiver
AC241	Octal non-inverting 3-state bus transceiver
AC244	Octal non-inverting 3-state bus transceiver
AC245	Octal non-inverting 3-state bus transceiver
AC251	3-state data multiplexer
AC253	Dual data selectors/multiplexers
AC257	Quad 3-state non-inverting data multiplexer
AC258	Quad 3-state inverting data multiplexer
AC273	Octal D flip-flop
AC352	Dual 4-input multiplexer
AC353	Dual 4-input multiplexer with 3-state output
AC373	Octal 3-state D-latch with common enable
AC374	Octal 3-state positive-edge-triggered D register
AC377	Octal D-type flip-flops with clock enable
AC378	Hex parallel D register with enable
AC379	Quad D-type flip-flops with enable
AC540	Octal inverting buffer (3-state) broadside pinout 'AC240'
AC541	Octal buffer (3-state) broadside pinout 'AC244'
AC573	Octal D-type latch with 3-state output
AC574	Octal D-type flip-flop with 3-state output
AC646	Octal transceiver/register with 3-state output

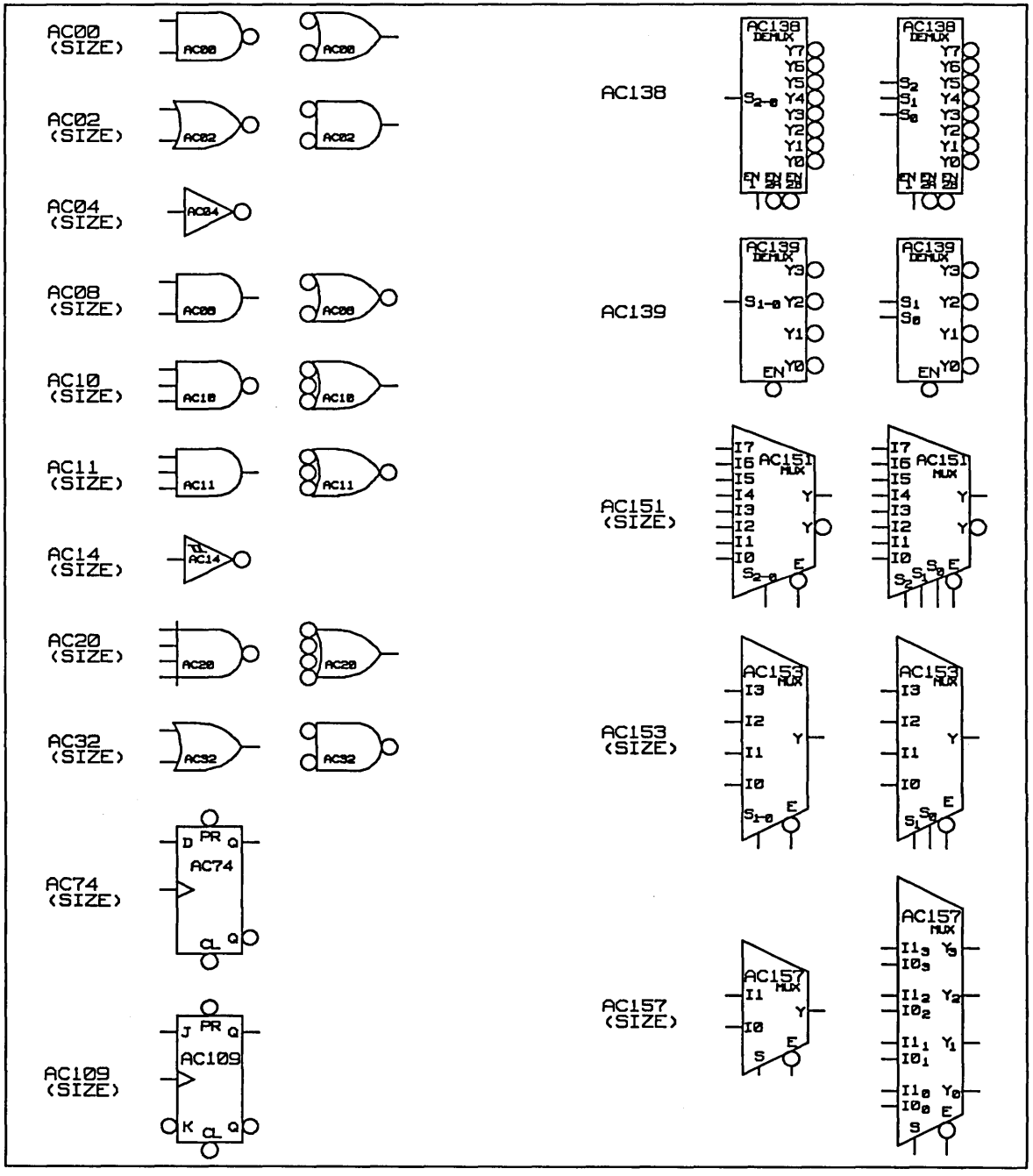
ACT00	Quad 2-input NAND
ACT04	Hex inverter
ACT08	Quad 2-input AND
ACT14	Hex inverter Schmitt trigger
ACT32	Quad 2-input OR
ACT74	Dual positive-edge-triggered D flip-flop
ACT109	Dual JKbar positive-edge-triggered flip-flop
ACT138	3-to-8 line decoders/multiplexers
ACT139	Dual 2-to-4 line decoders/multiplexers
ACT151	1-of-8 data selectors/multiplexers
ACT153	Dual 4-line to 1-line data multiplexer
ACT157	Quad 2-to-1-line non-inverting multiplexer
ACT158	Quad 2-to-1-line inverting data multiplexer
ACT160	4-bit synchronous decade counters with direct clear
ACT161	4-bit synchronous binary counters with direct clear
ACT163	4-bit synchronous binary counters with synch clear
ACT174	Hex D-type flip-flops
ACT175	Quad D-type flip-flops
ACT240	Octal inverting 3-state bus transceiver
ACT241	Octal non-inverting 3-state bus transceiver
ACT244	Octal non-inverting 3-state bus transceiver
ACT245	Octal non-inverting 3-state bus transceiver
ACT251	3-state data multiplexer
ACT253	Dual data selectors/multiplexers
ACT257	Quad 3-state non-inverting data multiplexer

ACT258	Quad 3-state inverting data multiplexer
ACT273	Octal D flip-flop
ACT352	Dual 4-input multiplexer
ACT353	Dual 4-input multiplexer with 3-state output
ACT373	Octal 3-state D-latch with common enable
ACT374	Octal 3-state positive-edge-triggered D register
ACT377	Octal D-type fllip-flops with clock enable
ACT378	Hex parallel D register with enable
ACT379	Quad D-type flip-flops with enable
ACT540	Octal inverting buffer (3-state) broadside pinout 'ACT240'
ACT541	Octal buffer (3-state) broadside pinout 'ACT244'
ACT573	Octal D-type latch with 3-state output
ACT574	Octal D-type flip-flop with 3-state output

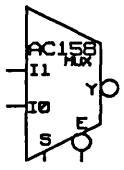
Application Notes

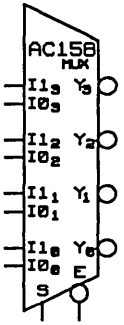
AC168 and AC169

The simulator models of AC168 and AC169 use the pin-to-pin delay property. To get accurate results, be sure to include the PIN_DELAY property in the *simulate.cmd* file.

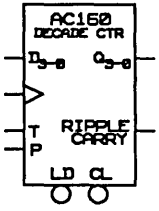

AC00
(SIZE)
AC02
(SIZE)
AC04
(SIZE)
AC08
(SIZE)
AC10
(SIZE)
AC11
(SIZE)
AC14
(SIZE)
AC20
(SIZE)
AC32
(SIZE)
AC74
(SIZE)
AC109
(SIZE)
AC138
AC139
AC151
(SIZE)
AC153
(SIZE)
AC157
(SIZE)

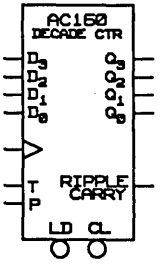
AC158 (SIZE)



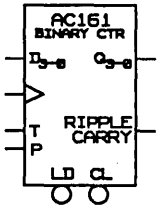


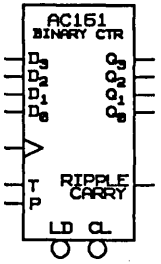
AC160



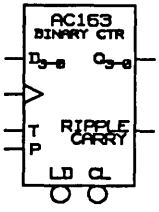


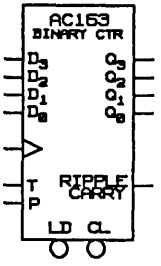
AC161



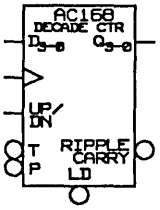


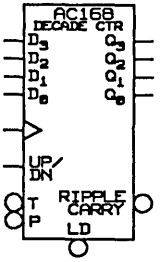
AC163



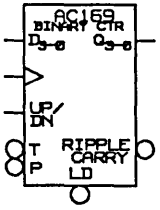


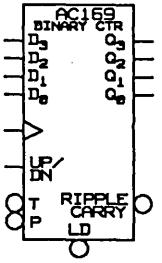
AC168



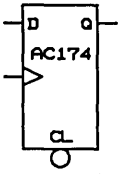


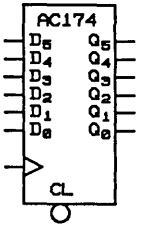
AC169



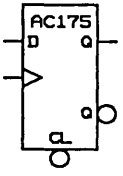


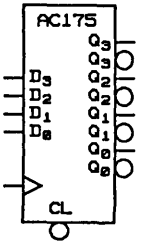
AC174 (SIZE)

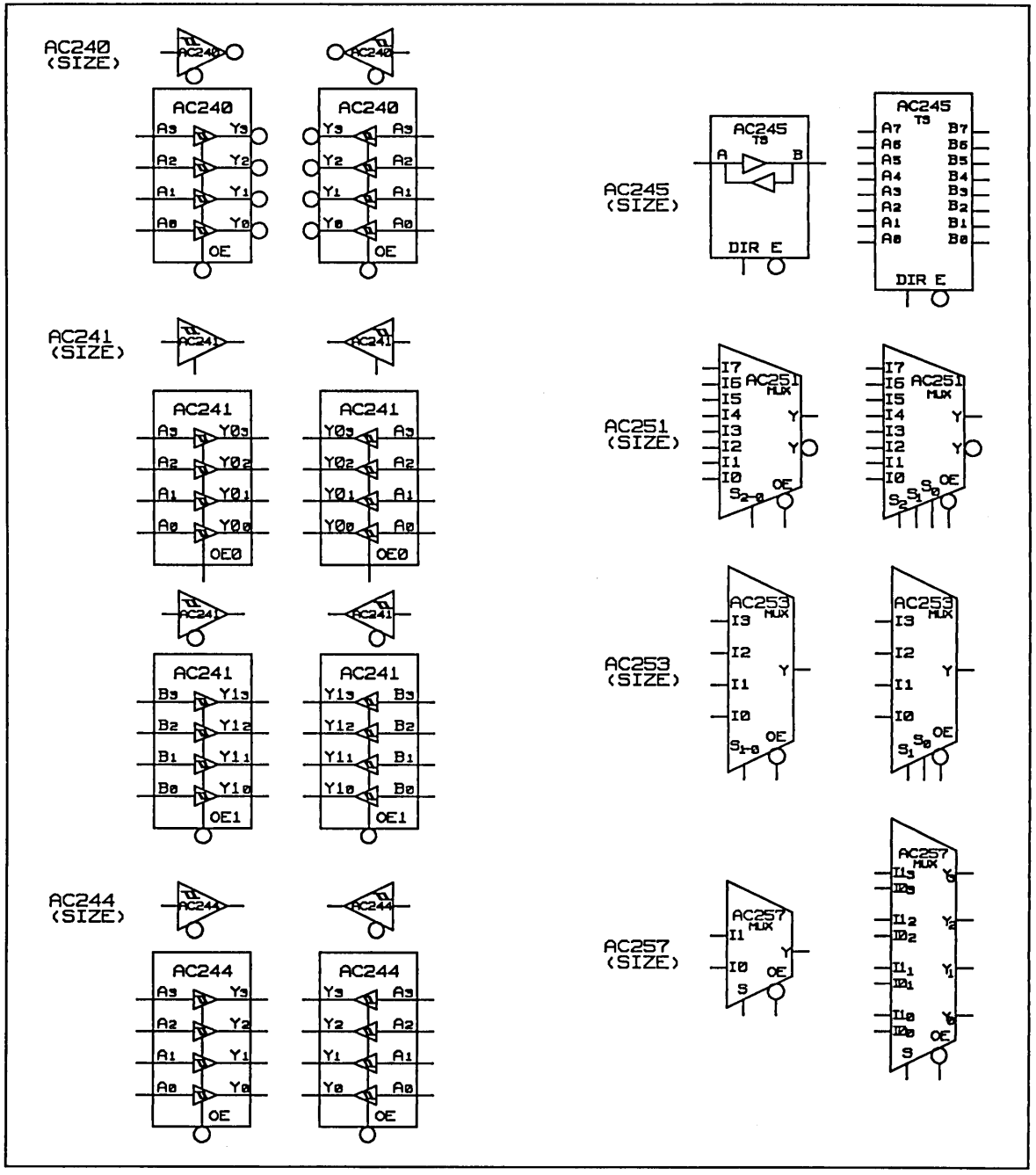


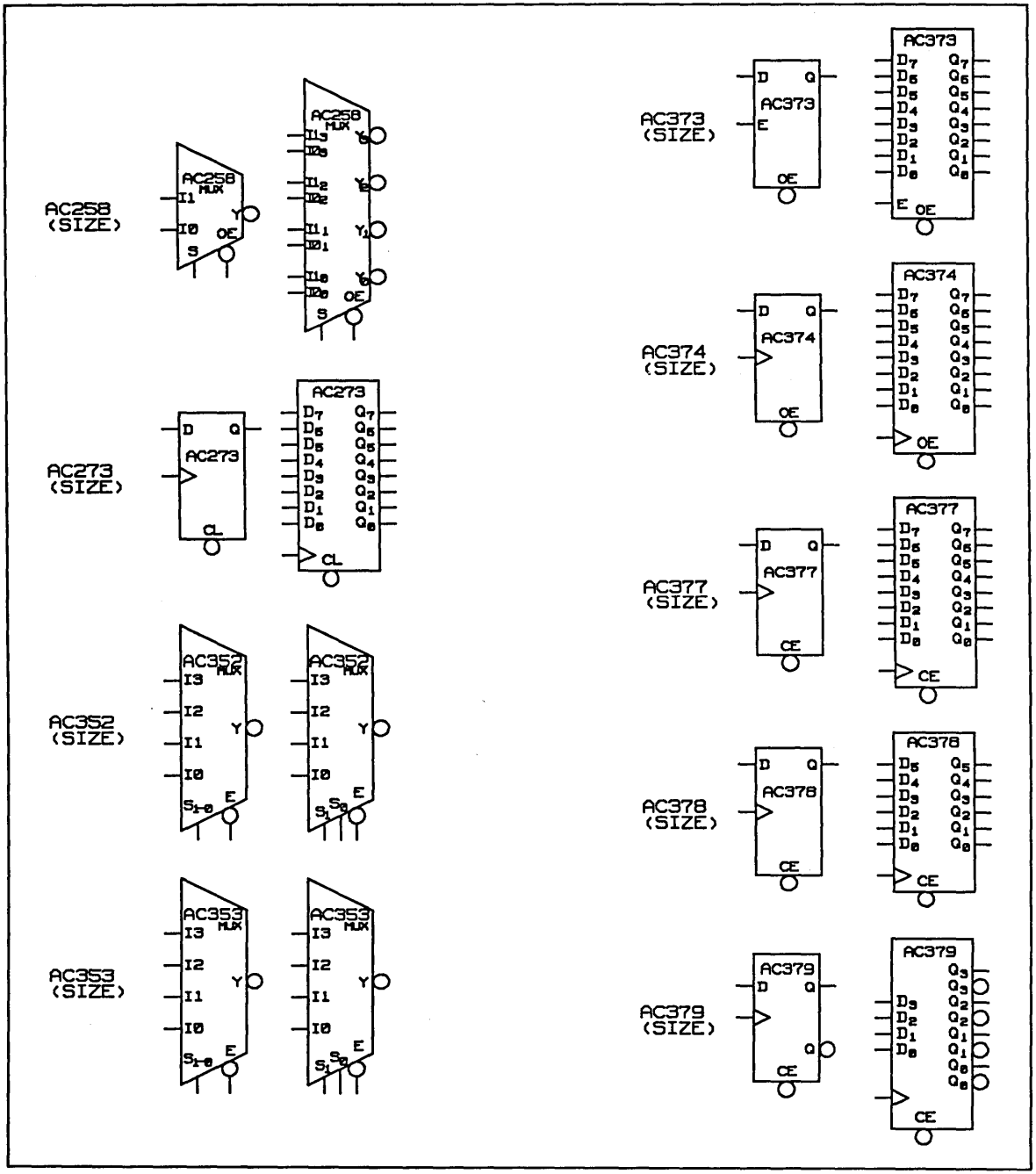


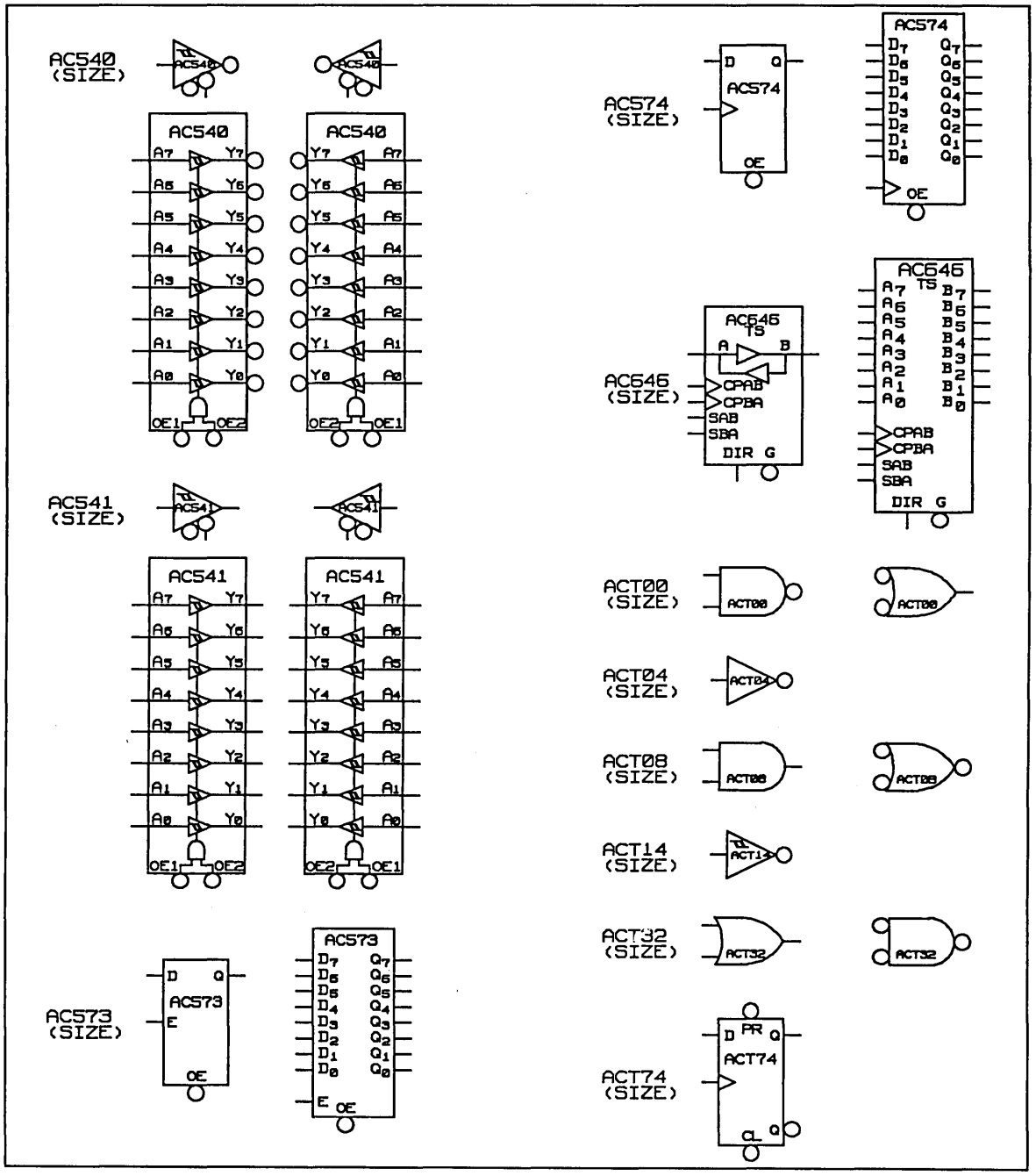
AC175 (SIZE)



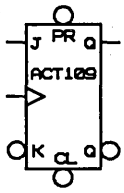



AC240
(SIZE)
AC241
(SIZE)
AC244
(SIZE)
AC245
(SIZE)
AC251
(SIZE)
AC253
(SIZE)
AC257
(SIZE)
DIR
OE
OE0
OE1
MUX
TS

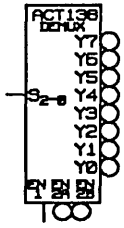

AC258 (SIZE)
AC258 MUX
I1
I0
S
Y
OE
AC273 (SIZE)
D
Q
AC273
CL
AC352 (SIZE)
AC352 MUX
I3
I2
I1
I0
Y
E
AC353 (SIZE)
AC353 MUX
AC373 (SIZE)
AC373
E
OE
AC374 (SIZE)
AC374
AC377 (SIZE)
AC377
CE
AC378 (SIZE)
AC378
AC379 (SIZE)
AC379

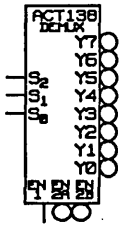

AC540
(SIZE)
AC540
AC540
AC541
(SIZE)
AC541
AC541
AC573
(SIZE)
AC573
AC573
AC574
(SIZE)
AC574
AC574
AC646
(SIZE)
AC646
TS
AC646
TS
ACT00
(SIZE)
ACT00
ACT00
ACT04
(SIZE)
ACT04
ACT08
(SIZE)
ACT08
ACT08
ACT14
(SIZE)
ACT14
ACT32
(SIZE)
ACT32
ACT32
ACT74
(SIZE)
ACT74

ACT109
(SIZE)

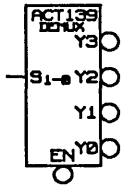


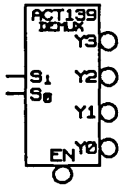
ACT138



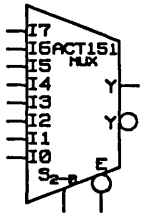


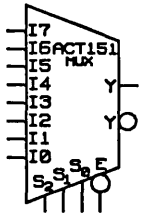
ACT139



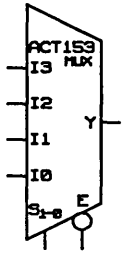


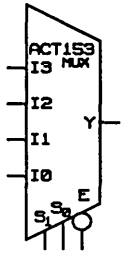
ACT151
(SIZE)



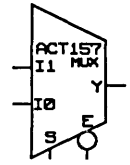


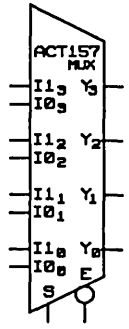
ACT153
(SIZE)



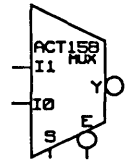


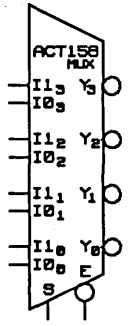
ACT157
(SIZE)



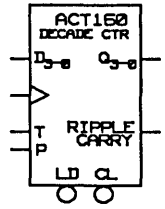


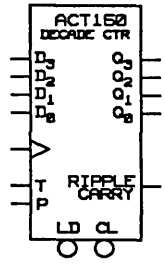
ACT158
(SIZE)



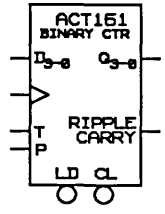


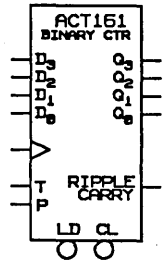
ACT160

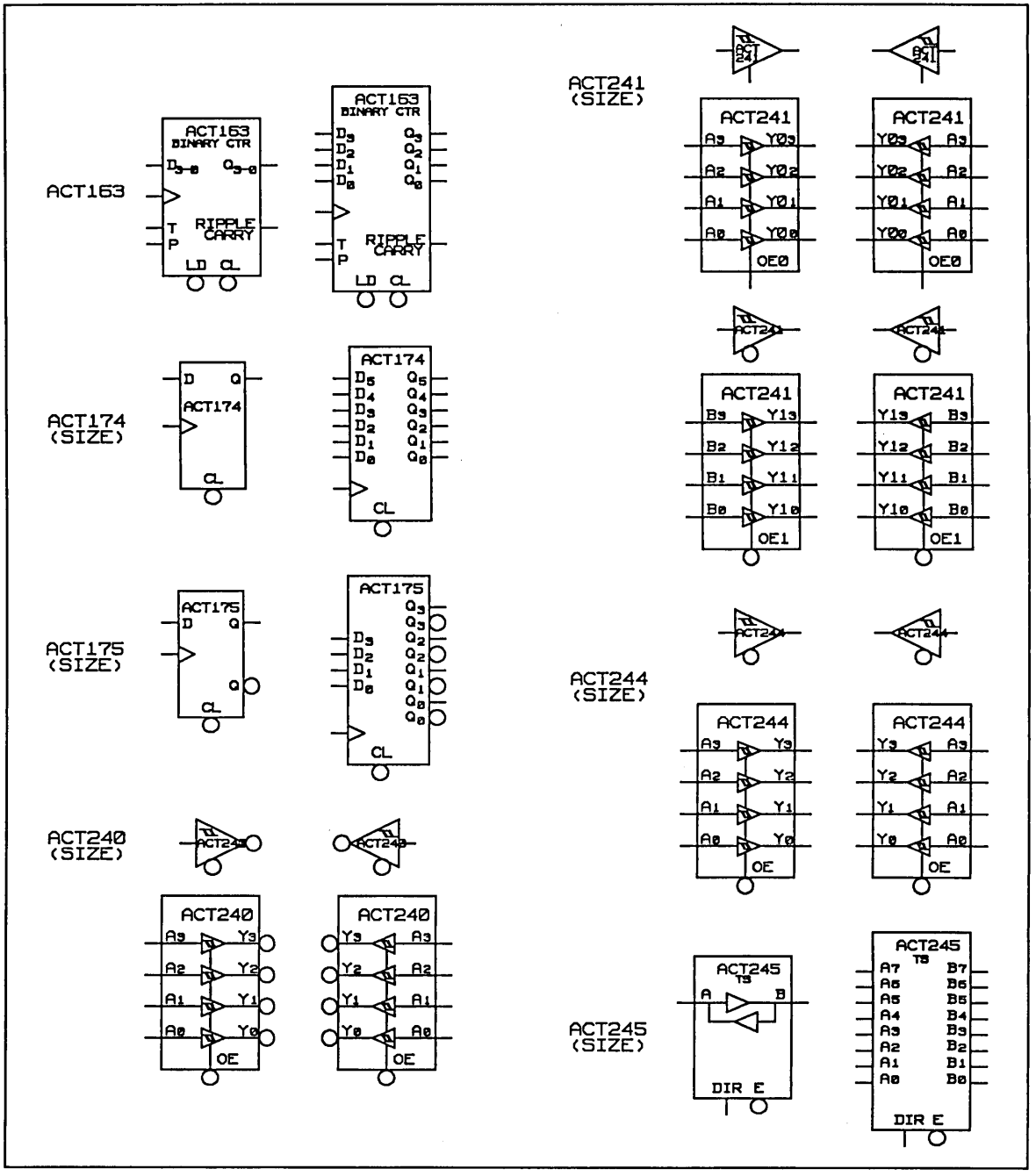




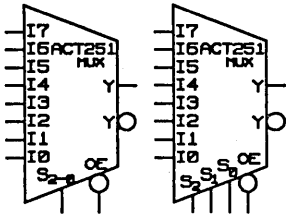
ACT161



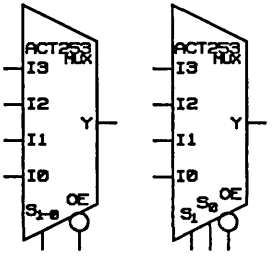



ACT163
ACT163
BINARY CTR
RIPPLE CARRY
LD
CL
ACT174
(SIZE)
ACT174
ACT175
(SIZE)
ACT175
ACT240
(SIZE)
ACT240
OE
ACT241
(SIZE)
ACT241
OE0
OE1
ACT244
(SIZE)
ACT244
OE
ACT245
(SIZE)
ACT245
DIR E

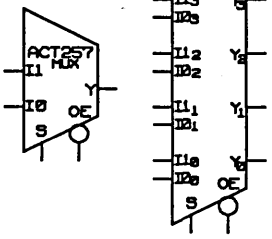
ACT251 (SIZE)



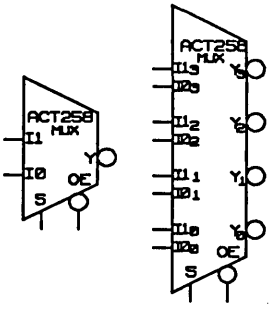
ACT253 (SIZE)



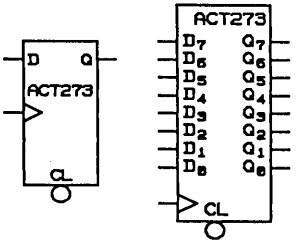
ACT257 (SIZE)



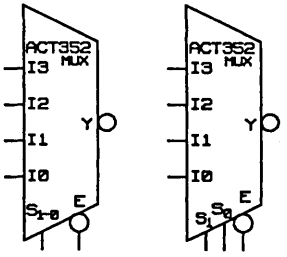
ACT258 (SIZE)



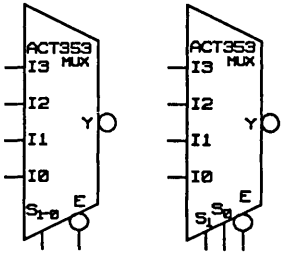
ACT273 (SIZE)



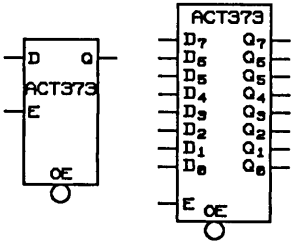
ACT352 (SIZE)



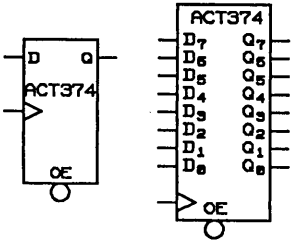
ACT353 (SIZE)

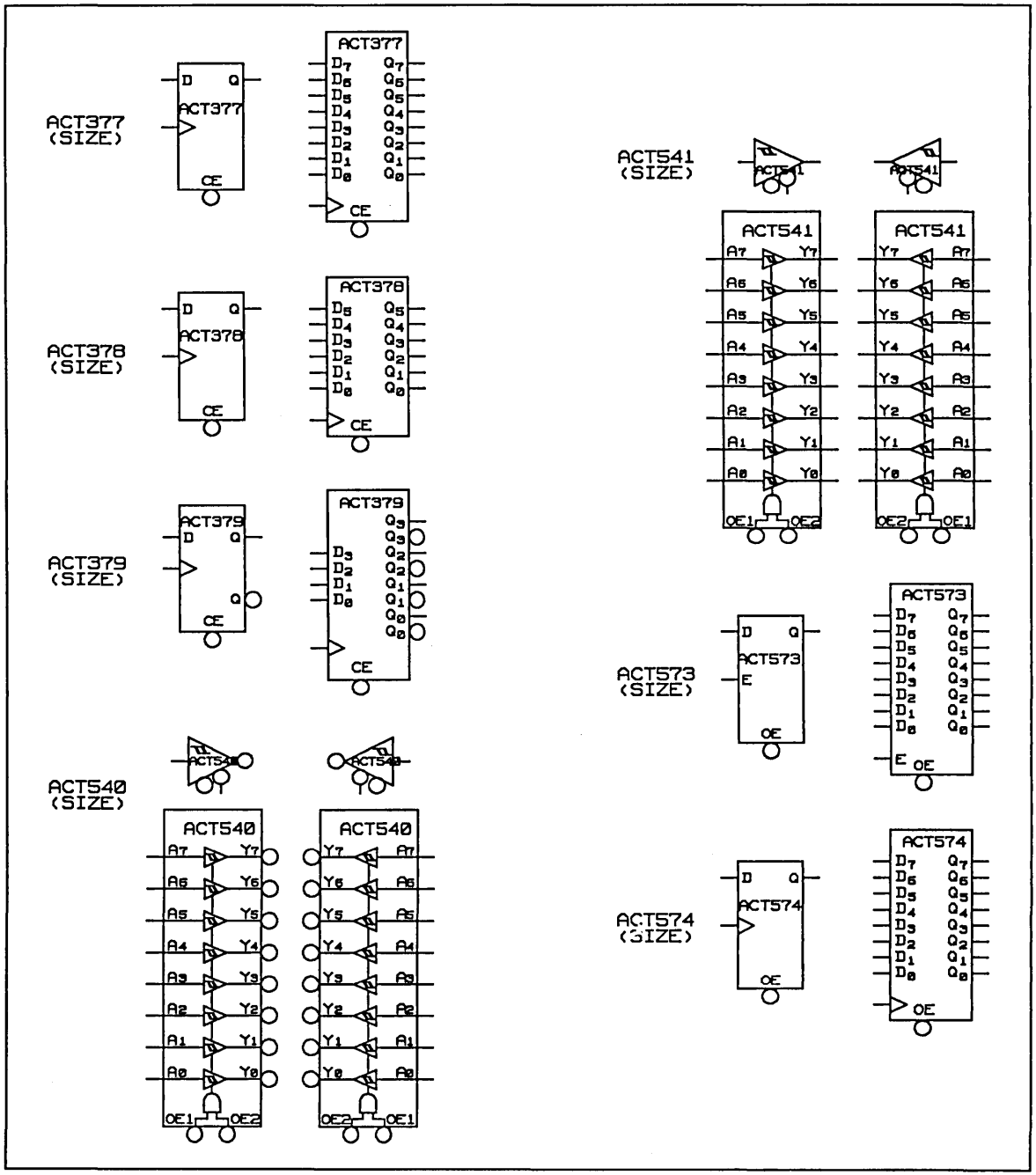


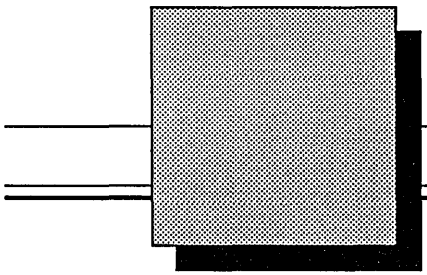
ACT373 (SIZE)



ACT374 (SIZE)




ACT377
(SIZE)
ACT377
D
Q
CE
ACT378
(SIZE)
ACT378
ACT379
(SIZE)
ACT379
ACT540
(SIZE)
ACT540
ACT541
(SIZE)
ACT541
ACT573
(SIZE)
ACT573
E
OE
ACT574
(SIZE)
ACT574



The RCACMOS Library

The RCACMOS Library requires approximately 2855 Kbytes of disk storage.

The specifications used to construct the models in this library were taken from the *GE Solid State: RCA Advanced CMOS Logic ICs* data books.

The release level of the RCACMOS Library is 9.0.

Each library contains body drawings and physical, timing, and simulation models for the following 98 components:

AC00	Quad 2-input NAND
AC02	Quad 2-input NOR
AC04	Hex inverter
AC08	Quad 2-input AND
AC10	Triple 3-input NAND
AC20	Dual 4-input NAND
AC32	Quad 2-input OR
AC74	Dual positive-edge-triggered D flip-flop
AC86	Quad 2-input exclusive-OR
AC109	Dual JKbar positive-edge-triggered flip-flop
AC112	Dual JK negative-edge-triggered flip-flop
AC138	3-to-8 line decoders/multiplexers
AC139	Dual 2-to-4 line decoders/multiplexers
AC151	1-of-8 data selectors/multiplexers
AC153	Dual 4-line to 1-line data multiplexer
AC157	Quad 2-to-1-line non-inverting multiplexer
AC158	Quad 2-to-1-line inverting data multiplexer
AC161	4-bit synchronous binary counters with direct clear
AC163	4-bit synchronous binary counters with synch clear
AC174	Hex D-type flip-flops
AC175	Quad D-type flip-flops
AC238	3-to-8-line decoder/demultiplexer
AC240	Octal inverting 3-state bus transceiver
AC241	Octal non-inverting 3-state bus transceiver
AC244	Octal non-inverting 3-state bus transceiver

AC245	Octal non-inverting 3-state bus transceiver
AC251	3-state data multiplexer
AC253	Dual data selectors/multiplexers
AC257	Quad 3-state non-inverting data multiplexer
AC258	Quad 3-state inverting data multiplexer
AC273	Octal D flip-flop
AC283	4-bit full-adder with fast carry
AC352	Dual 4-input multiplexer
AC353	Dual 4-input multiplexer with 3-state output
AC373	Octal 3-state D-latch with common enable
AC374	Octal 3-state positive-edge-triggered D register
AC377	Octal D-type flip-flops with clock enable
AC378	Hex parallel D register with enable
AC379	Quad D-type flip-flops with enable
AC533	Octal transparent latch (3-state inverting)
AC534	Octal D-type flip-flops, positive-edge trigger (3-state inverting)
AC540	Octal inverting buffer (3-state) broadside pinout 'AC240'
AC541	Octal buffer (3-state) broadside pinout 'AC244'
AC563	Octal transparent latch (3-state inverting)
AC564	Octal D-type flip-flops, positive-edge trigger (3-state inverting)
AC573	Octal D-type latch with 3-state output
AC574	Octal D-type flip-flop with 3-state output
AC623	Octal bus transceiver (3-state)
AC646	Octal transceiver/register with 3-state output
ACT00	Quad 2-input NAND

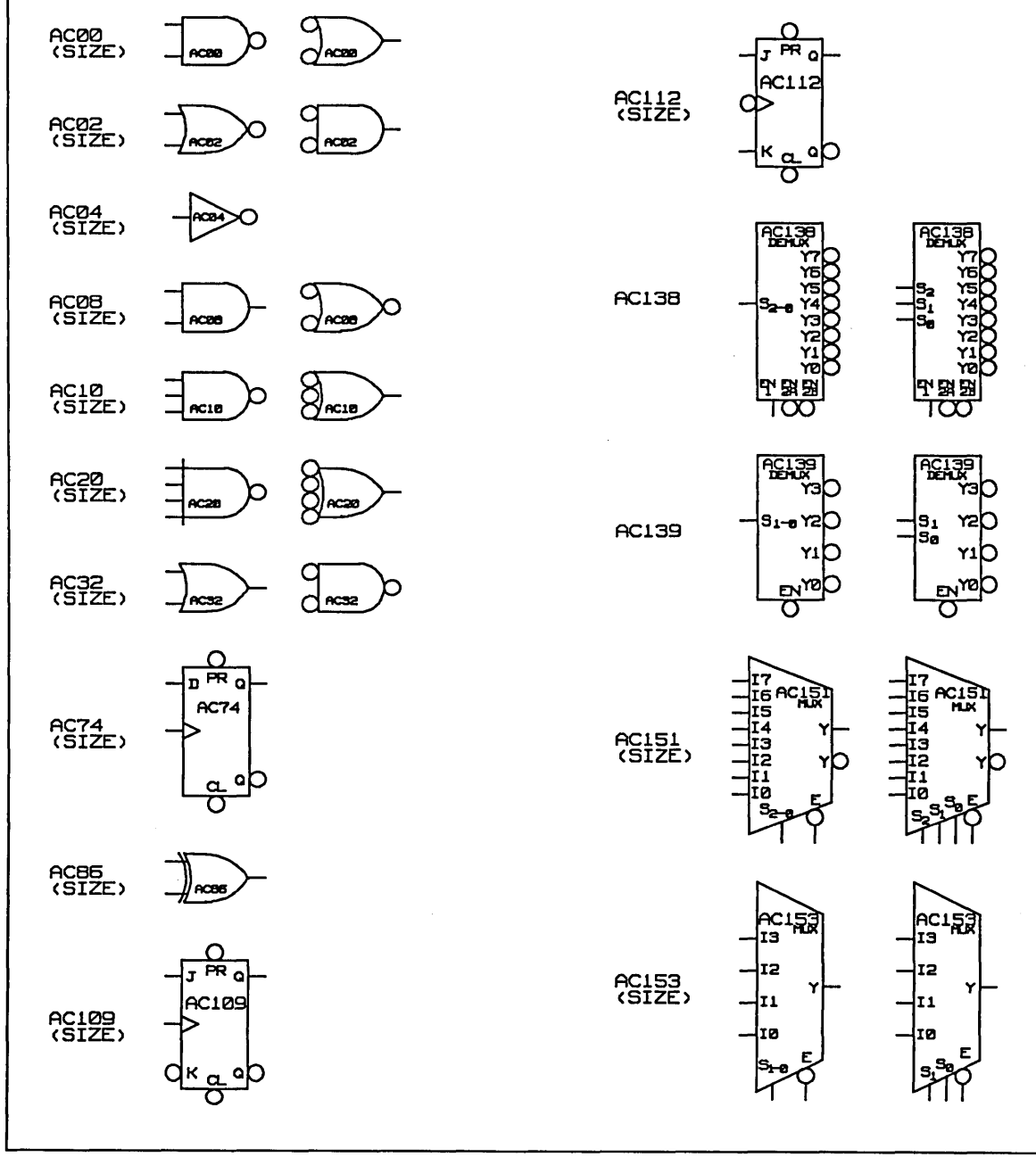
ACT02	Quad 2-input NOR
ACT04	Hex inverter
ACT08	Quad 2-input AND
ACT10	Triple 3-input NAND
ACT20	Dual 4-input NAND
ACT32	Quad 2-input OR
ACT74	Dual positive-edge-triggered D flip-flop
ACT86	Quad 2-input exclusive-OR
ACT109	Dual JKbar positive-edge-triggered flip-flop
ACT112	Dual JK negative-edge-triggered flip-flop
ACT138	3-to-8 line decoders/multiplexers
ACT139	Dual 2-to-4 line decoders/multiplexers
ACT151	1-of-8 data selectors/multiplexers
ACT153	Dual 4-line to 1-line data multiplexer
ACT157	Quad 2-to-1-line non-inverting multiplexer
ACT158	Quad 2-to-1-line inverting data multiplexer
ACT161	4-bit synchronous binary counters with direct clear
ACT163	4-bit synchronous binary counters with synch clear
ACT174	Hex D-type flip-flops
ACT175	Quad D-type flip-flops
ACT238	3-to-8-line decoder/demultiplexer
ACT240	Octal inverting 3-state bus transceiver
ACT241	Octal non-inverting 3-state bus transceiver
ACT244	Octal non-inverting 3-state bus transceiver
ACT245	Octal non-inverting 3-state bus transceiver

ACT251	3-state data multiplexer
ACT253	Dual data selectors/multiplexers
ACT257	Quad 3-state non-inverting data multiplexer
ACT258	Quad 3-state inverting data multiplexer
ACT273	Octal D flip-flop
ACT283	4-bit full-adder with fast carry
ACT352	Dual 4-input multiplexer
ACT353	Dual 4-input multiplexer with 3-state output
ACT373	Octal 3-state D-latch with common enable
ACT374	Octal 3-state positive-edge-triggered D register
ACT377	Octal D-type fllip-flops with clock enable
ACT378	Hex parallel D register with enable
ACT379	Quad D-type flip-flops with enable
ACT533	Octal transparent latch (3-state inverting)
ACT534	Octal D-type flip-flops, positive-edge trigger (3-state inverting)
ACT540	Octal inverting buffer (3-state) broadside pinout 'ACT240'
ACT541	Octal buffer (3-state) broadside pinout 'ACT244'
ACT563	Octal transparent latch (3-state inverting)
ACT564	Octal D-type flip-flops, positive-edge trigger (3-state inverting)
ACT573	Octal D-type latch with 3-state output
ACT574	Octal D-type flip-flop with 3-state output
ACT623	Octal bus transceiver (3-state)
ACT646	Octal transceiver/register with 3-state output

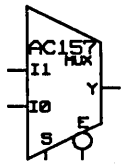
Application Notes

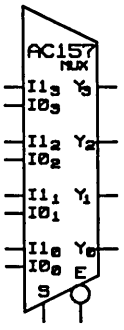
AC168 and AC169

The simulator models of AC168 and AC169 use the pin-to-pin delay property. To get accurate results, be sure to include the PIN_DELAY property in the *simulate.cmd* file.

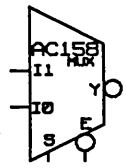

AC00
(SIZE)
AC02
(SIZE)
AC04
(SIZE)
AC08
(SIZE)
AC10
(SIZE)
AC20
(SIZE)
AC32
(SIZE)
AC74
(SIZE)
AC86
(SIZE)
AC109
(SIZE)
AC112
(SIZE)
AC138
AC139
AC151
(SIZE)
AC153
(SIZE)

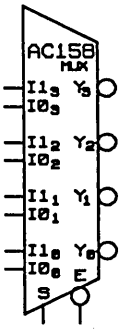
AC157 (SIZE)



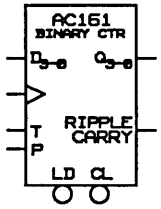


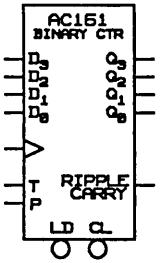
AC158 (SIZE)



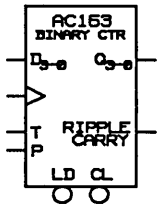


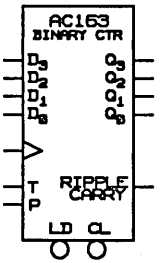
AC161



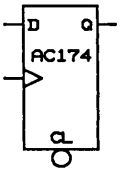


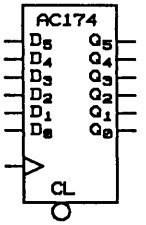
AC163



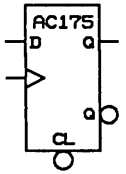


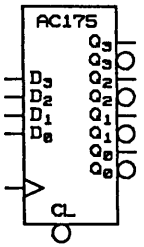
AC174 (SIZE)



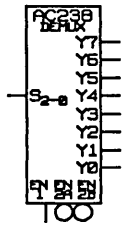


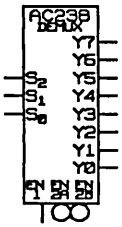
AC175 (SIZE)



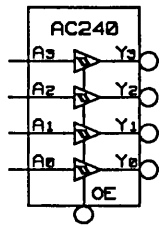


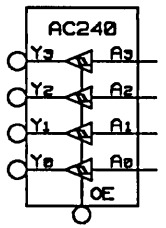
AC238



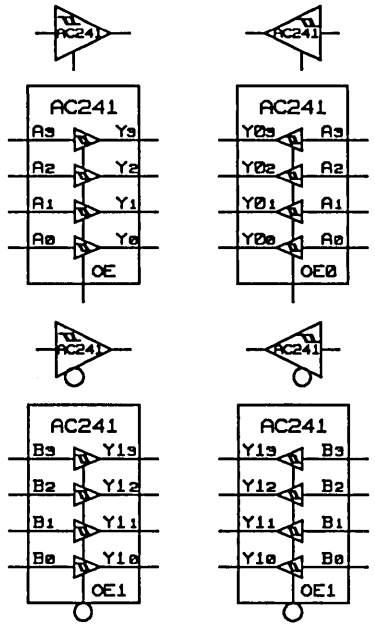


AC240 (SIZE)

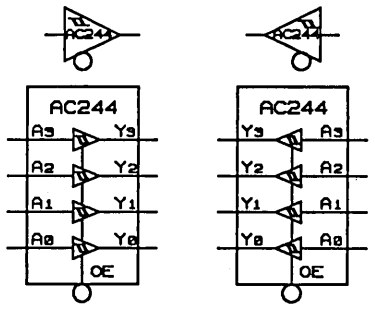




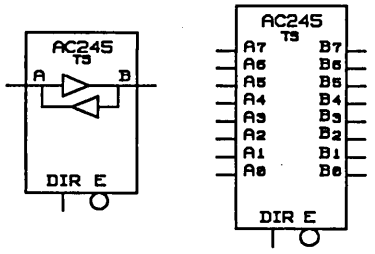
AC241 (SIZE)



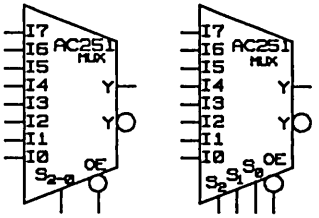
AC244 (SIZE)



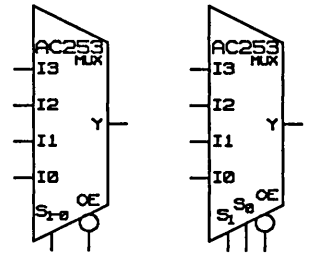
AC245 (SIZE)



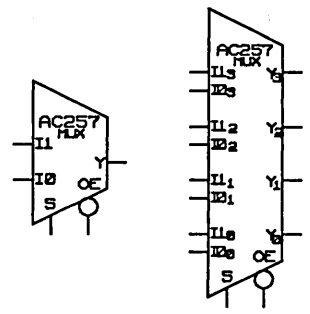
AC251 (SIZE)



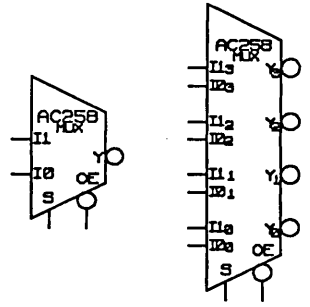
AC253 (SIZE)



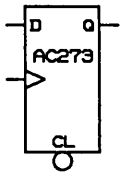
AC257 (SIZE)

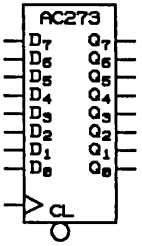


AC258 (SIZE)

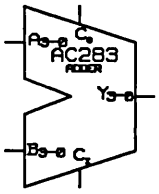


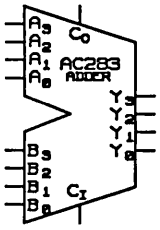
AC273 (SIZE)



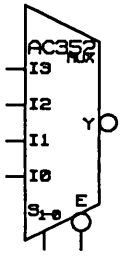


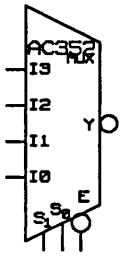
AC283



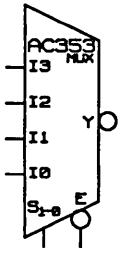


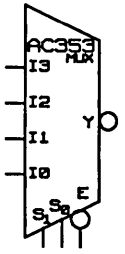
AC352 (SIZE)



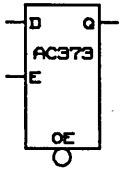


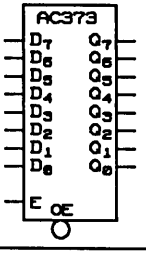
AC353 (SIZE)



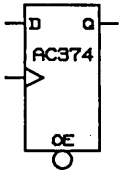


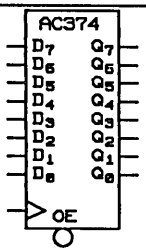
AC373 (SIZE)



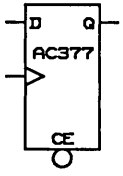


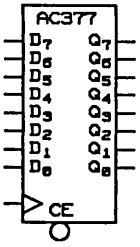
AC374 (SIZE)



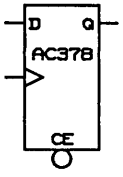


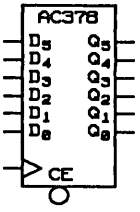
AC377 (SIZE)



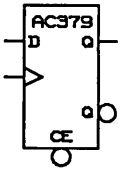


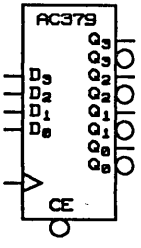
AC378 (SIZE)



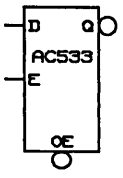


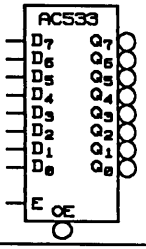
AC379 (SIZE)

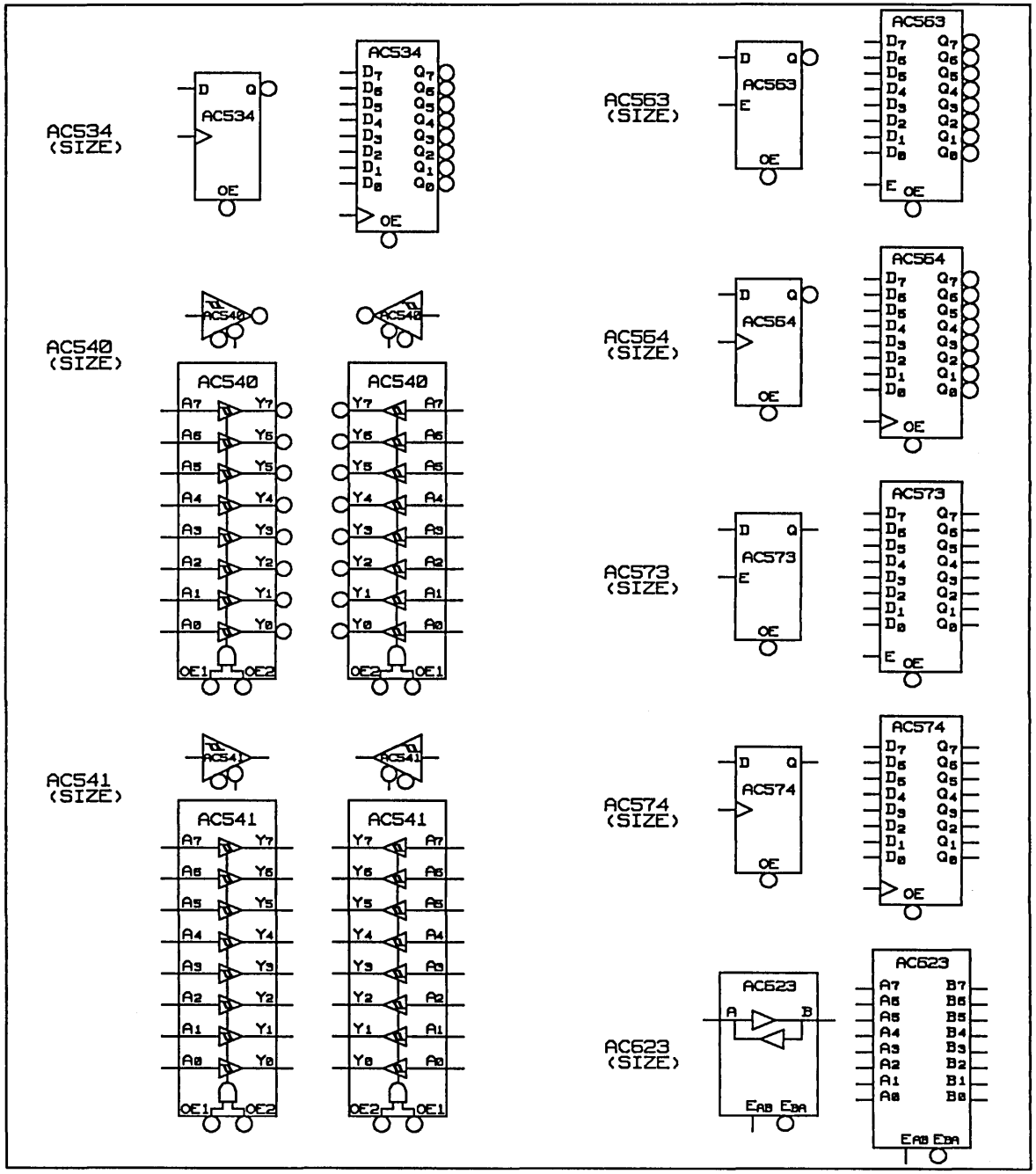




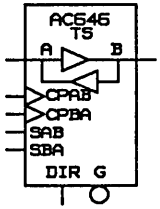
AC533 (SIZE)

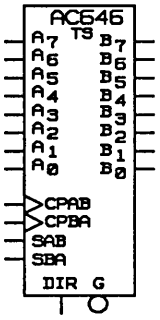





AC534
(SIZE)
AC534
D
Q
OE
AC540
(SIZE)
AC540
A7
A6
A5
A4
A3
A2
A1
A0
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
OE1
OE2
AC541
(SIZE)
AC541
AC563
(SIZE)
AC563
E
AC564
(SIZE)
AC564
AC573
(SIZE)
AC573
AC574
(SIZE)
AC574
AC623
(SIZE)
AC623
A
B
EAB
EBA

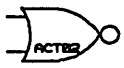
AC545 (SIZE)





ACT00 (SIZE)

ACT02 (SIZE)

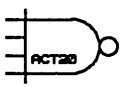


ACT04 (SIZE)

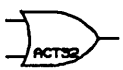
ACT08 (SIZE)

ACT10 (SIZE)

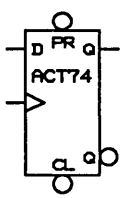
ACT20 (SIZE)



ACT32 (SIZE)

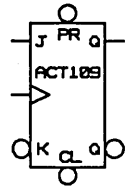


ACT74 (SIZE)

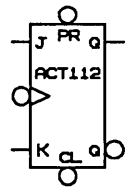


ACT86 (SIZE)

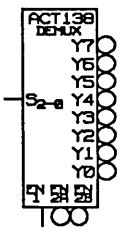
ACT109 (SIZE)

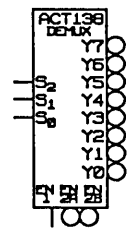


ACT112 (SIZE)

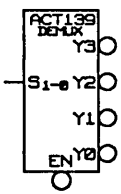


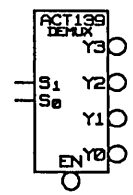
ACT138



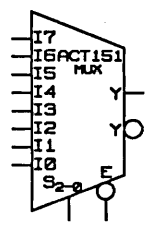


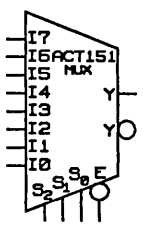
ACT139

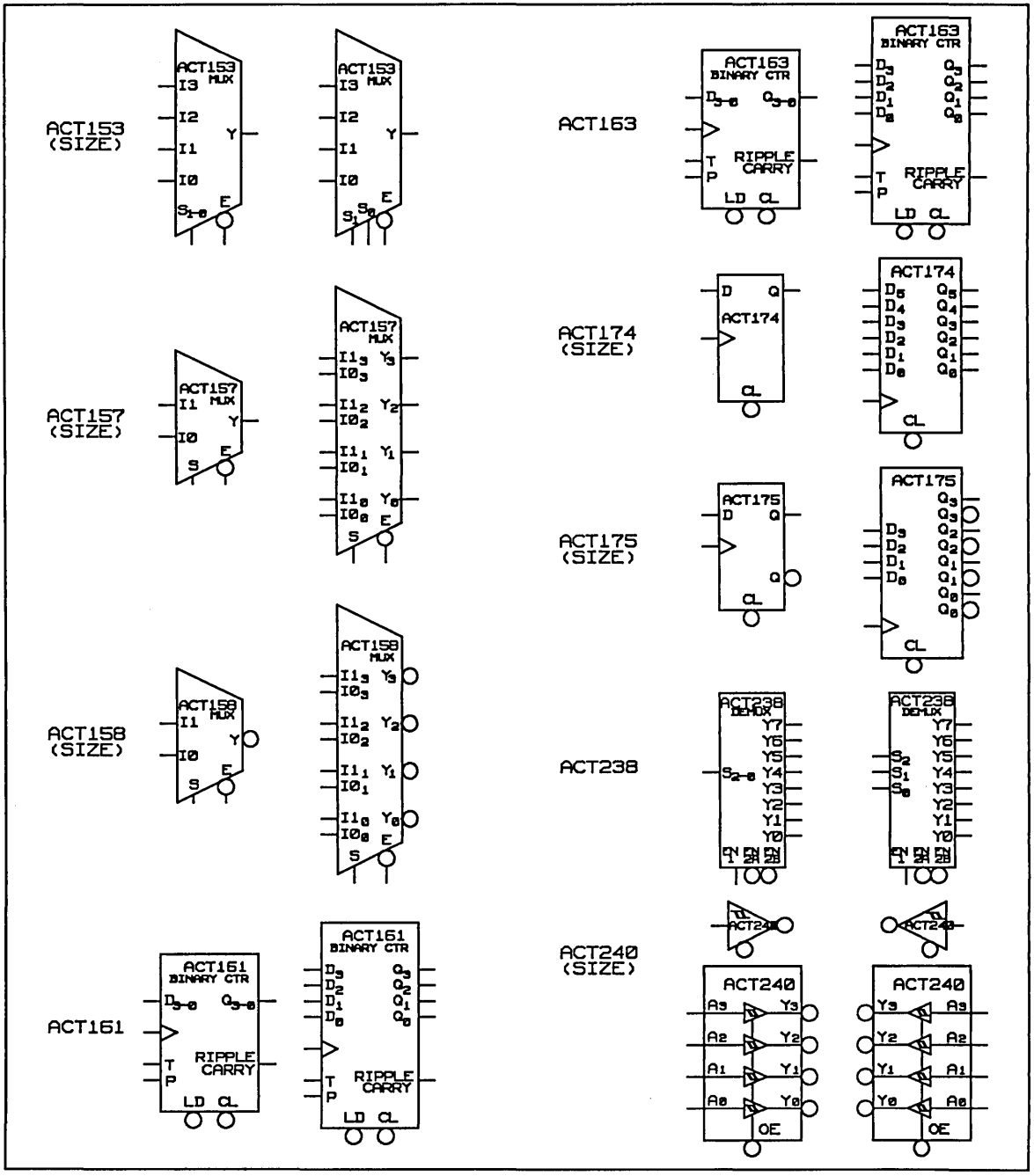




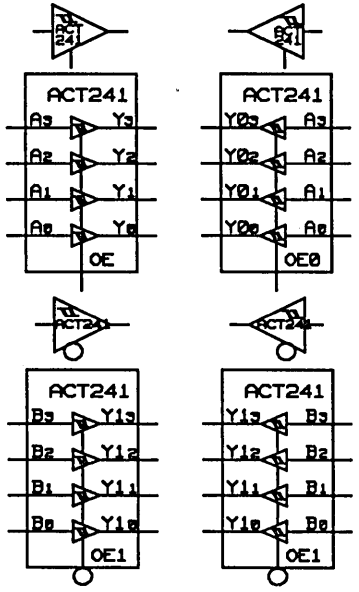
ACT151 (SIZE)



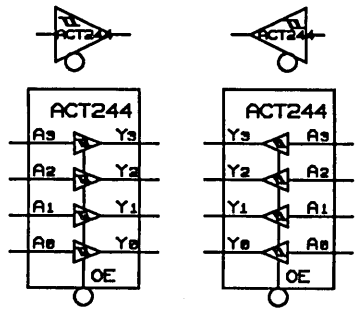



ACT153 (SIZE)
ACT153 MUX
I3
I2
I1
I0
S1-0
E
Y
ACT157 (SIZE)
ACT157 MUX
I1
I0
S
E
Y
ACT158 (SIZE)
ACT158 MUX
I1
I0
S
E
Y
ACT161
ACT161 BINARY CTR
D3-0
Q3-0
T
P
RIPPLE CARRY
LD
CL
ACT163
ACT163 BINARY CTR
D3-0
Q3-0
T
P
RIPPLE CARRY
LD
CL
ACT174 (SIZE)
ACT174
D
Q
CL
ACT175 (SIZE)
ACT175
D
Q
CL
ACT238
ACT238 DEMUX
S2-0
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
ACT240 (SIZE)
ACT240
OE

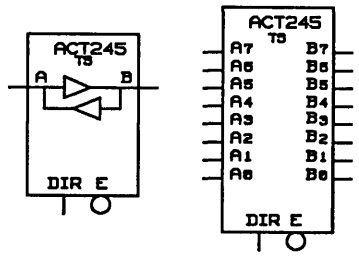
ACT241 (SIZE)



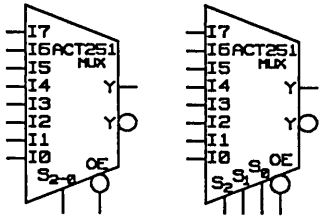
ACT244 (SIZE)



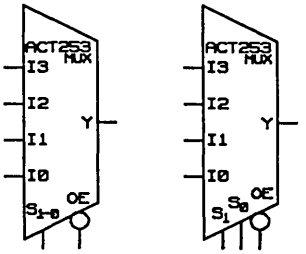
ACT245 (SIZE)



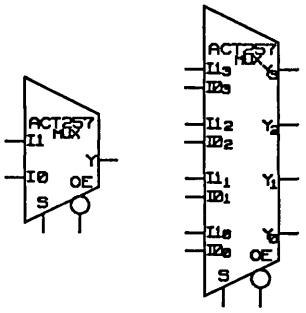
ACT251 (SIZE)



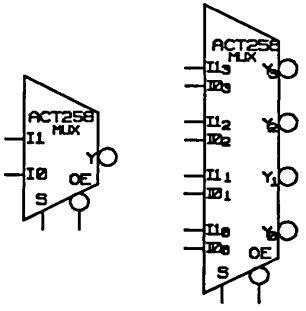
ACT253 (SIZE)



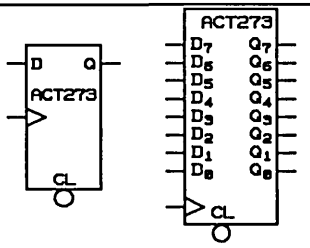
ACT257 (SIZE)



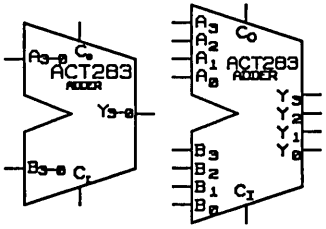
ACT258 (SIZE)



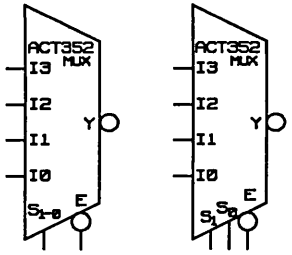
ACT273 (SIZE)



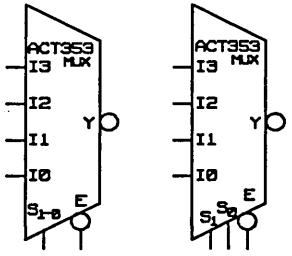
ACT283



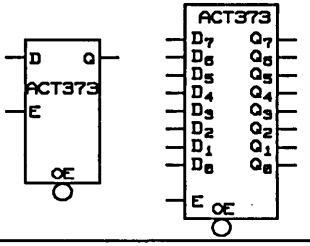
ACT352 (SIZE)



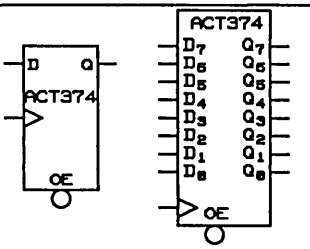
ACT353 (SIZE)



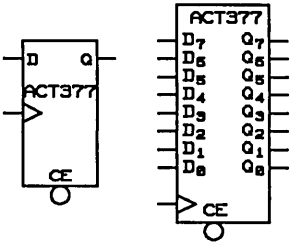
ACT373 (SIZE)



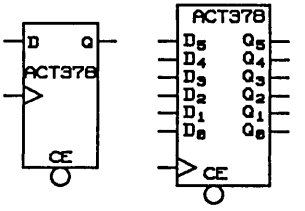
ACT374 (SIZE)



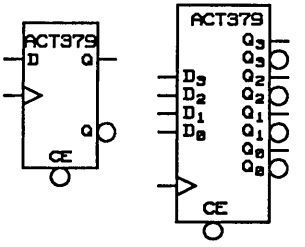
ACT377 (SIZE)



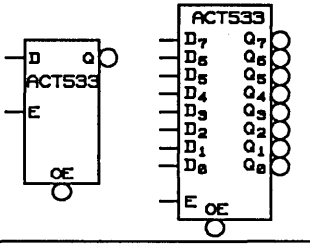
ACT378 (SIZE)

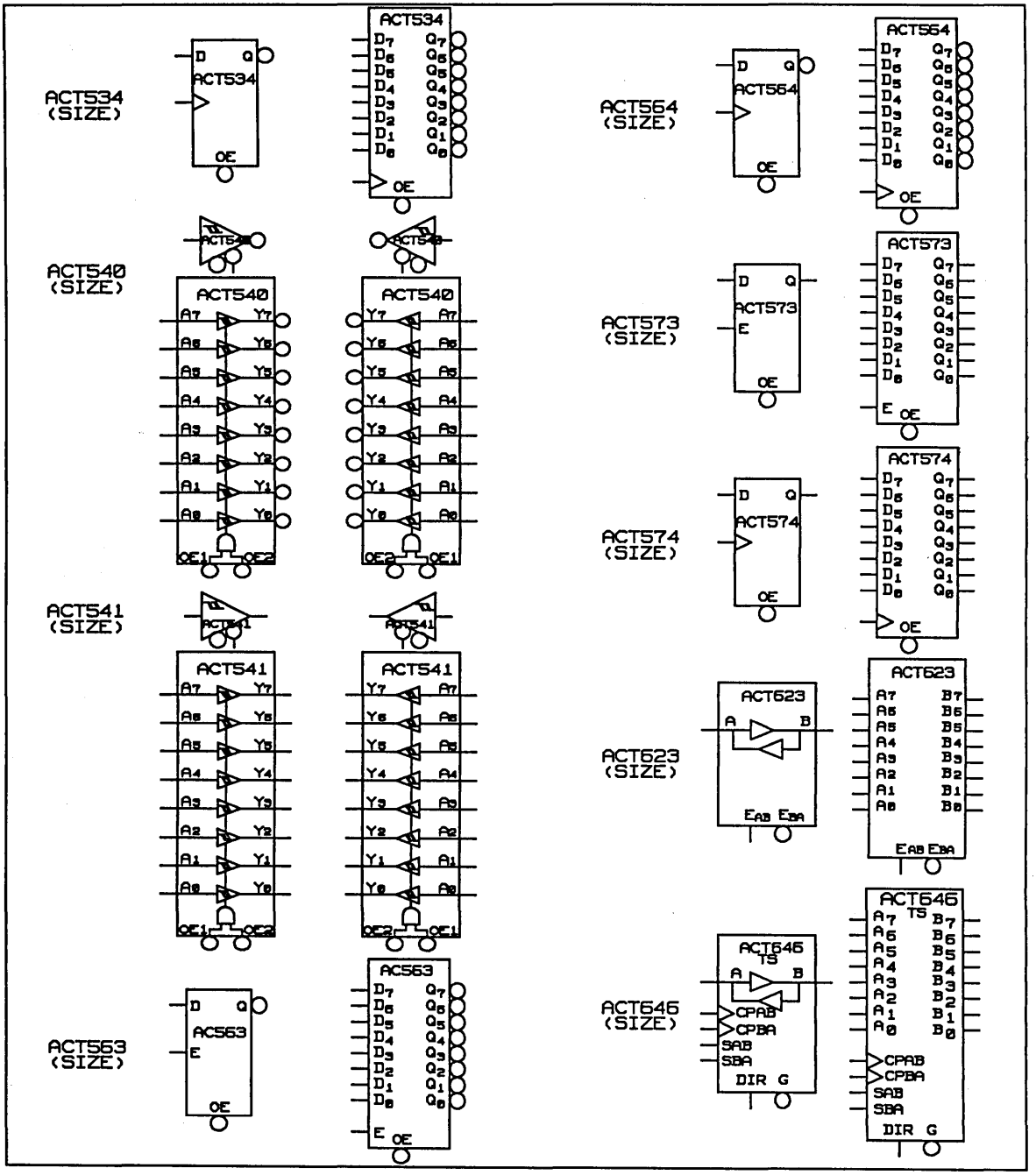


ACT379 (SIZE)



ACT533 (SIZE)




ACT534
(SIZE)
ACT534
D Q
ACT534
OE
ACT564
(SIZE)
ACT564
ACT540
(SIZE)
ACT540
ACT573
(SIZE)
ACT573
E
ACT541
(SIZE)
ACT541
ACT574
(SIZE)
ACT574
ACT623
(SIZE)
ACT623
A B
EAB EBA
ACT563
(SIZE)
AC563
ACT646
(SIZE)
ACT646
TS
CPAB
CPBA
SAB
SBA
DIR G

Index

Numbers

100K library, *Vol II:* 5–23
application notes, *Vol II:* 5–26

10K library, *Vol II:* 5–3
application notes, *Vol II:* 5–8

10KH library, *Vol II:* 5–15
application notes, *Vol II:* 5–16

54 series libraries, *Vol II:* 3–1

54ALSTTL library, *Vol II:* 3–89

54ASTTL library, *Vol II:* 3–71

54FAST library, *Vol II:* 3–171

54HCMOS library, *Vol II:* 3–125
application notes, *Vol II:* 3–133

54LSTTL library, *Vol II:* 3–3
application notes, *Vol II:* 3–11

54STTL library, *Vol II:* 3–53

54TTL library, *Vol II:* 3–193
application notes, *Vol II:* 3–196

74 series libraries, *Vol I:* 2–1

A

A SIZE PAGE border, *Vol I:* 1–4

ADVPAL library, *Vol II:* 6–33
application notes, *Vol II:* 6–34

ALSTTL library, *Vol I:* 2–119

ANSI libraries
10KH, *Vol II:* 5–15
54ALSTTL, *Vol II:* 3–89
54ASTTL, *Vol II:* 3–71
54FAST, *Vol II:* 3–171
54HCMOS, *Vol II:* 3–125
54LSTTL, *Vol II:* 3–3
54STTL, *Vol II:* 3–53
54TTL, *Vol II:* 3–193
ALSTTL, *Vol I:* 2–119
ASTTL, *Vol I:* 2–91
FAST, *Vol I:* 2–201
HCMOS, *Vol I:* 2–153
LSTTL, *Vol I:* 2–3
MEMORY, *Vol II:* 4–29
STTL, *Vol I:* 2–69
TTL, *Vol I:* 2–267

application notes
100K library, *Vol II:* 5–26
10K library, *Vol II:* 5–8
10KH and ANSI 10KH libraries, *Vol II:* 5–16
54HCMOS and ANSI 54HCMOS libraries, *Vol II:* 3–133
54LSTTL and ANSI 54LSTTL libraries, *Vol II:* 3–11
54TTL and ANSI 54TTL libraries, *Vol II:* 3–196
ADVPAL library, *Vol II:* 6–34
CMOS library, *Vol II:* 4–9
DISCRETE library, *Vol II:* 4–25
FACT library, *Vol I:* 2–297
FAST and ANSI FAST libraries, *Vol I:* 2–211

application notes *(continued)*
HCMOS and ANSI HCMOS libraries, *Vol I:* 2–161
IFL library, *Vol II:* 6–40
LSTTL and ANSI LSTTL libraries, *Vol I:* 2–14
MEMORY and ANSI MEMORY libraries, *Vol II:* 4–34
NEWPAL20 library, *Vol II:* 6–18
NEWPAL24 library, *Vol II:* 6–24
RCACMOS library, *Vol I:* 2–314
TTL and ANSI TTL libraries, *Vol I:* 2–273

approximation registers, successive, *Vol II:* 4–10

ASTTL library, *Vol I:* 2–91

B

B SIZE PAGE border, *Vol I:* 1–4

blown fuses, *see* fusemap file

bodies
DEFINE, *Vol I:* 1–4
DRAWING, *Vol I:* 1–4, 1–8
FLAG, *Vol I:* 1–4
MERGE/DEMERGE, *Vol I:* 1–4 *to* 1–5
NOT, *Vol I:* 1–6
ORIGIN, *Vol I:* 1–7
PIN NAME, *Vol I:* 1–7
REPLICATE, *Vol I:* 1–7
SIGN EXTEND, *Vol I:* 1–7
SIM_DIRECTIVES, *Vol I:* 1–9
SLASH, *Vol I:* 1–7

bodies *(continued)*
SYNONYM, *Vol I:* 1–8
and MERGE bodies, *Vol I:* 1–5
and NOT bodies, *Vol I:* 1–6
TAP, *Vol I:* 1–6
TIME_DIRECTIVES, *Vol I:* 1–9
VALID A SIZE PAGE, *Vol I:* 1–9
VALID B SIZE PAGE, *Vol I:* 1–9

borders, page, *Vol I:* 1–4, 1–9

bubble checker, *Vol I:* 1–6

buses, *Vol I:* 1–4

C

capacitive loading effects, *Vol I:* 2–162; *Vol II:* 3–134

CMOS library, *Vol II:* 4–3
application notes, *Vol II:* 4–9

commands, system
expand, *Vol II:* 6–10
genpld, *Vol II:* 6–5 *to* 6–6, 6–9 *to* 6–10, 6–12
makepld, *Vol II:* 6–7
rempld, *Vol II:* 6–10

Compiler and programmable logic devices, *Vol II:* 6–12

config.dat file, *Vol II:* 6–6

connectivity file, *Vol II:* 6–4
creating, *Vol II:* 6–9

creating
connectivity files, *Vol II:* 6–9
JEDEC files, *Vol II:* 6–9
programmable parts, *Vol II:* 6–7

D

DEFINE body, *Vol I:* 1–4

DELAY_EQ property, *Vol I:* 2–211; *Vol II:* 5–18

description file, programmable logic devices, *Vol II:* 6–5 *to* 6–6
  format, *Vol II:* 6–14

design flow, programmable logic devices, *Vol II:* *6–16*

directives
  LIBRARY, *Vol II:* 6–12, 6–13
  USER_EXPRESSION, *Vol II:* 5–18

directories
  pld.sdir, *Vol II:* 6–12
  /tmp, *Vol II:* 6–10

DISCRETE library, *Vol II:* 4–23
  application notes, *Vol II:* 4–25

DRAWING body, *Vol I:* 1–4, 1–8

E

ECL libraries, *Vol II:* 5–1
  100K, *Vol II:* 5–23
  10K, *Vol II:* 5–3
  10KH and ANSI 10KH, *Vol II:* 5–15

equations file tabs, *Vol II:* 6–10

expand command, *Vol II:* 6–10

F

FACT library, *Vol I:* 2–293
  application notes, *Vol II:* 2–297

FAST library, *Vol I:* 2–201
  application notes, *Vol II:* 2–211

files
  config.dat, *Vol II:* 6–6
  connectivity, *Vol II:* 6–4
    creating, *Vol II:* 6–9
  equation, *Vol II:* 6–10
  fusemap, *Vol II:* 6–5
    reading, *Vol II:* 6–9
  JEDEC format, *Vol II:* 6–4
  parts (programmable logic devices), *Vol II:* 6–8
  plds.prt, *Vol II:* 6–8, 6–13
    removing programmable logic devices, *Vol II:* 6–10
  programmable logic device description, *Vol II:* 6–5 *to* 6–6, 6–14
  simulate.cmd
    DELAY_EQ property, *Vol I:* 2–211, 5–18
    PIN_DELAY property, *Vol I:* 2–297, 2–314
  verifier.cmd, *Vol II:* 4–10

FLAG body, *Vol I:* 1–4

format file, JEDEC, *Vol II:* 6–3, 6–4

FPGA, FPLA, FPLS, *see* programmable logic device

fusemap file, *Vol II:* 6–5
  reading, *Vol II:* 6–9

G

gate-level model, *see* programmable logic device

GED
  and programmable logic devices, *Vol II:* 6–11
  commands
    ignore, *Vol II:* 6–11
    library, *Vol I:* 2–1; *Vol II:* 3–1, 4–1
    use, *Vol II:* 6–11

generating programmable logic, *Vol II:* 6–5 *to* 6–6

genpld command, *Vol II:* 6–5 *to* 6–6, 6–9 *to* 6–10, 6–12
  and /tmp directory, *Vol II:* 6–10

H

HCMOS library, *Vol I:* 2–153
  application notes, *Vol I:* 2–161
  capacitive loading effects, *Vol I:* 2–162

I

IFL library, *Vol II:* 6–45

ignore command, *Vol II:* 6–11

implementing programmable logic devices, *Vol II:* 6–5 *to* 6–6

intact fuses, *see* fusemap file

interface signals, *Vol I:* 1–7

I/O pins, *Vol II:* 6–12

J

JEDEC files
  creating, *Vol II:* 6–9
  formatting, *Vol II:* 6–3, 6–4

L

libraries
  100K, *Vol II:* 5–23
  10K, *Vol II:* 5–3
  10KH, *Vol II:* 5–15
  54 series, *Vol II:* 3–1
  54ALSTTL, *Vol II:* 3–89
  54ASTTL, *Vol II:* 3–71
  54FAST, *Vol II:* 3–171
  54HCMOS, *Vol II:* 3–125

libraries *(continued)*
54LSTTL, *Vol II:* 3–3
54STTL, *Vol II:* 3–53
54TTL, *Vol II:* 3–193
74 series, *Vol I:* 2–1
ADVPAL, *Vol II:* 6–33
ALSTTL, *Vol I:* 2–119
ANSI
10KH, *Vol II:* 5–15
54ALSTTL, *Vol II:* 3–89
54ASTTL, *Vol II:* 3–71
54FAST, *Vol II:* 3–171
54HCMOS, *Vol II:* 3–125
54LSTTL, *Vol II:* 3–3
54STTL, *Vol II:* 3–53
54TTL, *Vol II:* 3–193
ALSTTL, *Vol I:* 2–119
ASTTL, *Vol I:* 2–91
FAST, *Vol I:* 2–201
HCMOS, *Vol I:* 2–153
LSTTL, *Vol I:* 2–3
MEMORY, *Vol II:* 4–29
STTL, *Vol I:* 2–69
TTL, *Vol I:* 2–267
ASTTL, *Vol I:* 2–91
CMOS, *Vol II:* 4–3
DISCRETE, *Vol II:* 4–23
ECL, *Vol II:* 5–1
100K, *Vol II:* 5–23
10K, *Vol II:* 5–3
10KH and ANSI 10KH, *Vol II:* 5–15
FACT, *Vol I:* 2–293
libraries *(continued)*
FAST, *Vol I:* 2–201
HCMOS, *Vol I:* 2–153
IFL, *Vol II:* 6–45
LSTTL, *Vol I:* 2–3
manufacturer–supported, *Vol II:* A–1
MEMORY, *Vol II:* 4–29
MM74C, *Vol II:* 4–71
NEWPAL20, *Vol II:* 6–19
NEWPAL24, *Vol II:* 6–27
PHANTOM, *Vol I:* 1–13
RCACMOS, *Vol I:* 2–309
SIM, *Vol I:* 1–25
STANDARD, *Vol I:* 1–3
STTL, *Vol I:* 2–69
TIME, *Vol I:* 1–17
TTL, *Vol I:* 2–267
TUTORIAL, *Vol I:* 1–35
library command, *Vol I:* 2–1; *Vol II:* 3–1, 4–1
LIBRARY directive, *Vol II:* 6–12, 6–13
libutil software support package
ADVPAL library, *Vol II:* 6–34
NEWPAL20 library, *Vol II:* 6–21
NEWPAL24 library, *Vol II:* 6–28
loading effects, capacitive, *Vol I:* 2–162; *Vol II:* 3–134
logic devices, programmable, *Vol II:* 6–3 *to* 6–18
LSB, *see* least significant bit
LSTTL library, *Vol I:* 2–3
application notes, *Vol I:* 2–14

M

makepld command, *Vol II:* 6–7, 6–13

manufacturer-supported libraries, *Vol II:* A–1

MEMORY library, *Vol II:* 4–29
application notes, *Vol II:* 4–34

MERGE/DEMERGE bodies, *Vol I:* 1–4 *to* 1–5

MM74C library, *Vol II:* 4–71

modeling programmable logic devices, *Vol II:* 6–3 *to* 6–18

modifying programmable logic devices, *Vol II:* 6–8

monostable multivibrators
54HCMOS and ANSI 54HCMOS libraries, *Vol II:* 3–133
54LSTTL and ANSI 54LSTTL libraries, *Vol II:* 3–11
54TTL and ANSI 54TTL libraries, *Vol II:* 3–196
CMOS library, *Vol I:* 4–9
HCMOS and ANSI HCMOS libraries, *Vol I:* 2–161
LSTTL and ANSI LSTTL libraries, *Vol I:* 2–14
TTL and ANSI TTL libraries, *Vol I:* 2–273

most significant bit, *Vol I:* 1–6

MSB, *see* most significant bit

multi-bit signals, *see* buses

multivibrators, *see* monostable multivibrators

N

NEWPAL20 library, *Vol II:* 6–19
application notes, *Vol II:* 6–18

NEWPAL24 library, *Vol II:* 6–27
application notes, *Vol II:* 6–24

NOT bodies, *Vol I:* 1–6

O

open collector and emitter technology, *Vol I:* 1–14

ORIGIN body, *Vol I:* 1–7

overwriting programmable logic device descriptions, *Vol II:* 6–9

P

Packager and programmable logic devices, *Vol II:* 6–13

PAL, *see* programmable logic device

PALASM program, *Vol II:* 6–10

parts file, programmable logic devices, *Vol II:* 6–8

PHANTOM library, *Vol I:* 1–13

PIN_DELAY property, *Vol I:* 2–297, 2–314

PIN NAMES body, *Vol I:* 1–7

pins, I/O, *Vol II:* 6–12

pld.sdir directory, *Vol II:* 6–12

PLDs, *see* programmable logic devices

plds.prt file, *Vol II:* 6–8, 6–13
removing programmable logic devices, *Vol II:* 6–10

programmable logic devices, *Vol II:* 6–3 *to* 6–18
and SCALD software, *Vol II:* 6–11 *to* 6–13
chips information, *Vol II:* 6–8
creating
connectivity files, *Vol II:* 6–9
new parts, *Vol II:* 6–7
description file format, *Vol II:* 6–14
design flow, *Vol II:* 6–16
implementing, *Vol II:* 6–5 *to* 6–6
modeling scheme, *Vol II:* 6–4
modifying, *Vol II:* 6–8
overwriting previous descriptions, *Vol II:* 6–9
PLD description file, *Vol II:* 6–5 *to* 6–6
removing, *Vol II:* 6–10
tabs in PALASM equation file, *Vol II:* 6–10

programs
PALASM, *Vol II:* 6–10
user interface, *Vol II:* 6–7 *to* 6–10

PROMs, *see* programmable logic devices

properties
DELAY_EQ, *Vol I:* 2–211; *Vol II:* 5–18
PIN_DELAY, *Vol I:* 2–297, 2–314
SIZE, *Vol I:* 1–7
and programmable logic devices, *Vol II:* 6–4
and TAP bodies, *Vol I:* 1–6
WIRE-GATE, *Vol I:* 1–15

R

RCACMOS library, *Vol I:* 2–309
application notes, *Vol I:* 2–314

reading fusemap files, *Vol II:* 6–9

registers, successive approximation, *Vol II:* 4–10

removing programmable logic devices, *Vol II:* 6–10

rempld command, *Vol II:* 6–10

REPLICATE body, *Vol I:* 1–7

S

SCALD software and programmable logic devices, *Vol II:* 6–11

SIGN EXTEND body, *Vol I:* 1–7

signals
interface, *Vol I:* 1–7
vectored, *Vol I:* 1–4

SIM library, *Vol I:* 1–25

SIM_DIRECTIVES body, *Vol I:* 1–9

simulate.cmd file
DELAY_EQ property, *Vol I:* 2–211; *Vol II:* 5–18
PIN_DELAY property, *Vol I:* 2–297, 2–314

Simulator
and programmable logic devices, *Vol II:* 6–12
directives, USER_EXPRESSION, *Vol II:* 5–18

SIZE property, *Vol I:* 1–7
and programmable logic devices, *Vol II:* 6–4
and TAP bodies, *Vol I:* 1–6
SLASH body, *Vol I:* 1–7
software support, *libutil* package
ADVPAL library, *Vol II:* 6–34
NEWPAL20 library, *Vol II:* 6–21
NEWPAL24 library, *Vol II:* 6–28
STANDARD library, *Vol I:* 1–3
STTL library, *Vol I:* 2–69
successive approximation registers, *Vol II:* 4–10
SYNONYM body, *Vol I:* 1–8
and MERGE bodies, *Vol I:* 1–5
and NOT bodies, *Vol I:* 1–6
system commands
expand, *Vol II:* 6–10
genpld, *Vol II:* 6–5 *to* 6–6, 6–9 *to* 6–10, 6–12
makepld, *Vol II:* 6–7
rempld, *Vol II:* 6–10

T

tabs in PALASM equation file, *Vol II:* 6–10
TAP bodies, *Vol I:* 1–6
TIME library, *Vol I:* 1–17
TIME_DIRECTIVES body, *Vol I:* 1–9
Timing Verifier and programmable logic devices, *Vol II:* 6–13
/tmp directory, *Vol II:* 6–10
TTL library, *Vol I:* 2–267
application notes, *Vol I:* 2–273
TUTORIAL library, *Vol I:* 1–35

U

unprogrammed devices, *see* programmable logic devices
use command, *Vol II:* 6–11
USER_EXPRESSION directive, *Vol II:* 5–18
user interface programs, *Vol II:* 6–7 *to* 6–10

V

VALID A SIZE PAGE body, *Vol I:* 1–9
VALID B SIZE PAGE body, *Vol I:* 1–9
vectored signals, *Vol I:* 1–4
verifier.cmd file, *Vol II:* 4–10

W

WIRE-GATE property, *Vol I:* 1–15