VARIAN DATA 620/i
MAINTENANCE
MANUAL
VOLUME 1

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INTRODUCTION

This manual contains maintenance information for the Varian Data 620/i Computer. The manual describes the central processor in chapter 2, the memory in chapter 3, and the teletype controller in chapter 4. Chapters 5 through 7 present timing waveforms, a mnemonic index, and a diagnostic program package. In addition, useful reference material is included in the appendices following chapter 7.

Documents such as assembly drawings, logic diagrams, and wire lists are provided in volume 2 of this manual.

With the exception of the teletype controller, the peripheral device controllers for the 620/i computer are not described in this manual. However, individual manuals are available for each of the controllers. Table 1-1 lists other 620/i manuals that may provide background information for maintenance personnel.

Maintenance information for the peripheral devices used with the 620/i computer, such as the teletype, is contained in the manufacturer's reference manuals supplied with the equipment.

Table 1-1
620/i Reference Manuals

Publication Stock Number	Title
98 A 9902 003	System Reference Manual
98 A 9902 015	Interface Reference Manual
98 A 9902 024	Programming Reference Manual
98 A 9902 031	FORTRAN Reference Manual
98 A 9902 043	Subroutine Description
98 A 9902 303	Integration and Installation Manual

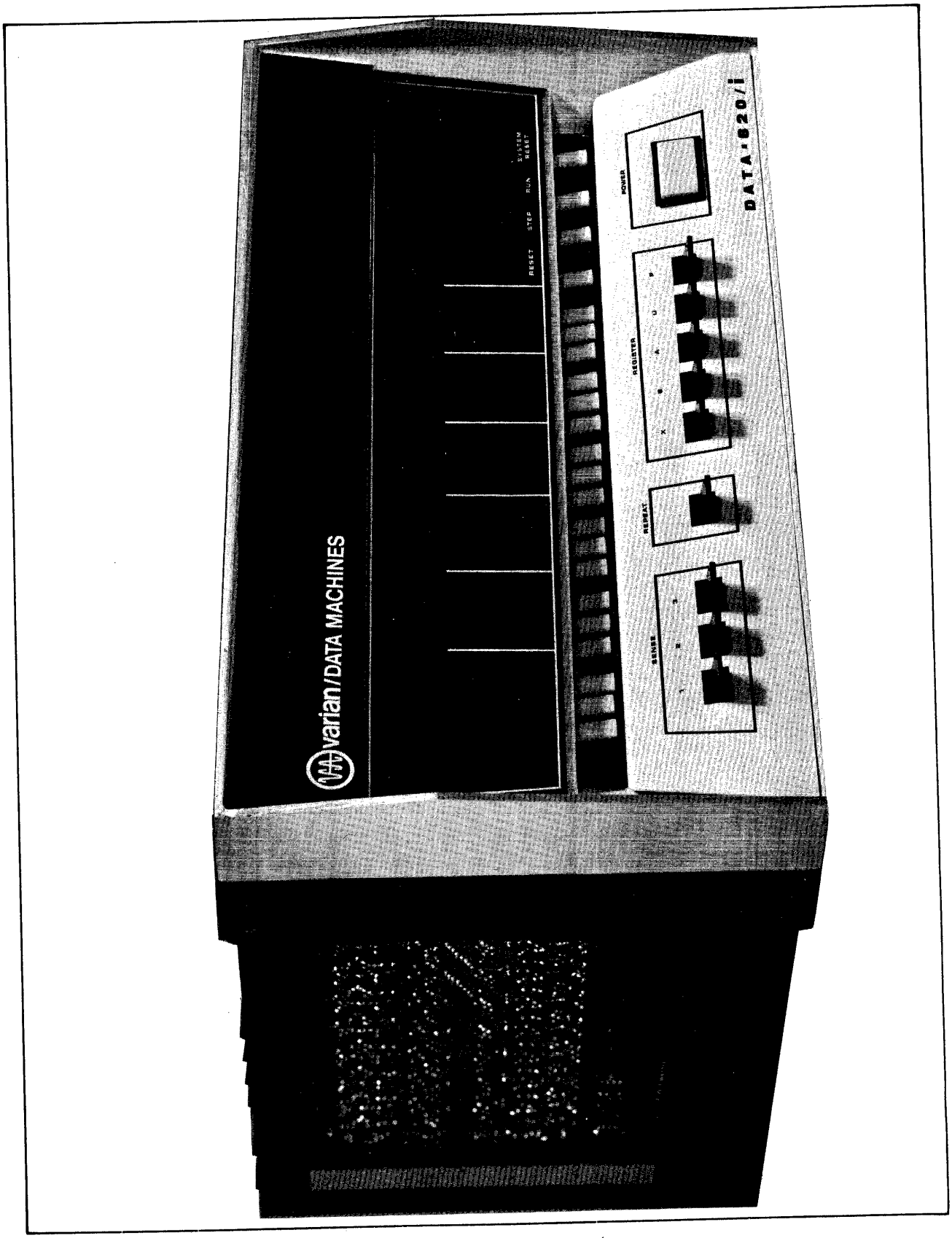


Figure 2-1. Varian Data 620/i Computer

CHAPTER 2
CENTRAL PROCESSOR

1.1 INTRODUCTION

The central processor of the DATA 620/i computer system is shown in figure 2-1. It is a high-speed, parallel, binary computer and is designed for flexibility. Modular packaging with integrated-circuit components make it ideal for use as a general-purpose machine and for application as an on-line system component.

Features of the computer include a modular 1.8-microsecond memory that is expandable to 16,384 words in blocks of 4096 words (on special order to 32,768), a large instruction set, six addressing modes and an extensive software library. The computer has a flexible input/output (I/O) system with a single I/O bus that allows direct data transfers to or from memory and which may be operated with up to 64 peripheral devices.

The unique design of the computer makes it easy to program, operate and maintain. The computer includes the console control-indicator panel, computer options, a 4096-word core memory and the power supply (mounted externally behind the mainframe). Only 17 circuit cards of 11 different types are used in the basic 16-bit configuration.

Power supplies (for the central processor and up to 8192 words of core memory) are mounted behind the mainframe of the central processor in a separate, chassis of the same height as the mainframe. The entire computer therefore requires only 10-½ inches of height in a standard 19-inch wide equipment rack. Installation is easy, requiring no special mounting, cabling or air-conditioning provisions.

Front access to all central processor wiring enhances maintainability by making module removal from the mainframe rack unnecessary until after a problem source is located.

1.2 SPECIFICATIONS

Specifications for the central processor are listed in table 2-1.

Table 2-1
Central Processor Specifications

Specification	Characteristics	
Type	General-purpose digital computer for on-line data system applications. Magnetic core memory; binary, parallel, single-address, with bus organization.	
Memory	See chapter 3.	
Arithmetic	Parallel, binary, fixed point, 2's complement.	
	Word Length	16 bits standard; 18 bits optional.
	Speed (fetch and execute)	
	Add or Subtract	3.6 microseconds.
	Multiply (optional)	16-bits: 18.0 microseconds.
		18-bits: 19.8 microseconds.

Table 2-1 (continued)
Central Processor Specifications (continued)

	Divide (optional)	16-bits: 18.0 to 25.2 microseconds.
		18-bits: 19.8 to 27.0 microseconds.
	Register Change	1.8 microseconds.
	Input/Output	From A or B register: 3.6 microseconds.
		From memory: 5.4 microseconds.
Registers	A Register	High-order accumulator, input/output, 16 or 18 bits.
	B Register	Low-order accumulator, input/output, index register, 16 or 18 bits.
	X Register	Index register, multipurpose register, 16 or 18 bits.
	P Register	Program counter, 16 or 18 bits.
	U Register	Instruction register, 16 bits.
	L Register	Memory address register, 16 bits.
	W Register	Memory word register, 16 or 18 bits.
	S Register	Shift register, 5 bits.
	R Register	Operand register, 16 or 18 bits.
Control	Addressing Modes	Six as follows:
	Direct: to 2048 words.	
	Relative to P register: to 512 words.	
	Index with X register hardware: to 32,768 words (does not add to execution time).	
	Index with B register hardware: to 32,768 words (does not add to execution time).	
	Immediate: operand immediately follows instruction.	
	Multilevel indirect: to 32,768 words.	
	Extended (optional): operand address or indirect address immediately follows instruction; (optional) to 32,768 words.	
Instruction Types	Four, as follows:	
	Single word, addressing.	
	Single word, nonaddressing.	
	Double word, addressing.	
	Double word, nonaddressing.	

Table 2-1
Central Processor Specifications (continued)

Instructions	107 standard commands, approximately 200 microinstructions, plus 18 optional.
Control Panel	Selectable display and data entry switches, three SENSE switches, instruction REPEAT, single STEP, RUN, POWER on/off, and SYSTEM RESET switches.
Input/Output	
Program Sense	Up to 512 status lines may be sensed.
External Control	Up to 512 external control lines may be selected.
Data Transfer	Three types as follows: Single word to/from memory (program control). Single word to/from A and B registers (program control). Optional direct memory access (cycle steal).
Physical Characteristics	
Dimensions	10-$\frac{1}{2}$ inches high, 13 inches deep, and 19 inches wide.
Weight	90 pounds, including power supplies, less than 35 pounds without power supplies.
Power	360 watts, single phase, 115 vac ± 10 vac, 48 to 62 Hz. Power supplies are regulated. Additional regulation is not required with normal commercial power sources.
Environment	10°C to 45°C, 10% to 90% relative humidity (without condensation).
Accessibility	All wiring for the central processor is located behind the swing-away console control-indicator panel at the front of the unit. Printed circuit modules are easily removed from the rear.
Expansion Capability	The central processor contains the console control-indicator panel, the main frame, a 4096-word memory, and space for processor options. Additional memory requires the addition of a standard DATA 620/i expansion frame for the first additional 4096 words and one for each 8192 words of additional storage. Therefore, peripheral device controllers are mounted in an expansion frame external to the processor main frame.
Installation	Central processor and power supply packages require 10-$\frac{1}{2}$ inches of height in a standard 19 inch wide equipment rack. No air-conditioning, subflooring, special wiring or site preparation is required.
Logic and Signals	The logic of the central processor uses DTL and TTL integrated circuits which operate at a logic level of 5 volts. The logic level on the I/O bus is reduced to 3 volts to lessen cross talk and current requirements. Internal logic convention is +5 volts for logical ONE, and 0 volts for logical ZERO. I/O bus logic convention is +3 volts for logical ZERO, and 0 volts for logical ONE.

1.3 USE OF THIS CHAPTER

This chapter provides the basic information required for maintaining the central processor. The information includes design and construction, theory of operation, maintenance procedures and troubleshooting techniques. See chapters 5 through 7 for timing waveforms, mnemonic, and diagnostic programs.

2.1 GENERAL

The main frame contains the central processor, memory and associated options. The control console is a swing-away panel hinged to the front of the main frame. Opening the panel exposes all wiring for check-out.

There are 26 slots for the printed circuit cards. Each card fits into a 122-pin connector at the front of the main frame. The cards are removed from the rear of the main frame. The 122-pin card connectors are interconnected by wiring as required. All connections on these connectors are accomplished by wire wrap or push-pin jumpers; no soldering is employed. The interframe wiring is harnessed into cabling. Part of the cabling is connected to the motherboard and control switches at the back of the swing-away console control-indicator panel. The cabling is also brought out to cable connectors at the rear of the main frame to provide a party line I/O cable and other essential buses for expansion frame assemblies. Cable connections are soldered. Circuit card slot assignments are shown in table 2-2.

The power supply is normally mounted in a swing-down chassis hinged at the rear of the main frame. Its output cable connects to the J30/P30 connector at the rear of the main frame. This cabling is brought to the front of the main frame and the console control-indicator swing-away panel where it is included in the wire harness and connected in accordance with the applicable assembly wiring diagrams.

Table 2-2
Central Processor Circuit Card Slot Assignments

Slot	Card Type	Card Name	Slot	Card Type	Card Name
1	DM 120*	Memory regulator	14	DM 108	Register card
2	DM 161	Memory parity	15	DM 106	Memory timing and control
3	DM 103	Matrix decoder Y	16	DM 109	Processor control #1
4	Stack	4096-word memory	17	DM 110	Processor control #2
5	Stack	4096-word memory	18	DM 111	Processor control #3
6	DM 103-1	Matrix decoder X	19	DM 112	Processor control #4
7	DM 104	Memory driver/switch X	20	DM 122	Multiply/divide and extended address
8	DM 104	Memory driver/switch Y	21	DM 121	Interrupt trap
9	DM 1190-5	Memory data card	22	DM 123	Power fail/restart and real-time clock
10	DM 1196-11	Memory data card	23	DM 124	Priority interrupt module
11	DM 11912-19	Memory data card	24	DM 113	Teletype controller
12	DM 108	Register card	25	DM 125	Micro-EXEC
13	DM 1086-1	Register card	26	DM 114	Negative I/O

*In earlier 620/i configurations, DM 120 card is installed in slot 2 and slot 1 is vacant.

2.2 DESIGN FEATURES

The central processor incorporates two design features which provide unique wiring simplicity and greatly simplified troubleshooting operations. These are the "bit-slice" design concept in the structural organization of the gating and storage elements, and the transmission bus technique for data transfers.

2.2.1 Bit-Slice

Register circuit cards (DM 108) contain six bits of all registers (except the L and S registers) together with their respective input and output gates. The L register is contained on circuit card DM 109 and the S register is contained on circuit card DM 112 .

All register bits are used in the 18-bit system. In the 16-bit system, register bits 17 and 18 are not wired into the ground plane and C bus. The register circuit boards are therefore interchangeable with each other. This greatly simplifies troubleshooting operations since isolation of a malfunctioning bit-slice may be accomplished without regard to which functional area has failed.

2.2.2 Transmission Bus

A transmission bus technique is employed throughout the central processor. The term bus, as used in this manual, is any group of parallel signal paths. It may be any part or combination of the following:

> Circuit paths on a printed circuit board or group of boards which carry the same parallel bits of data words or related control signals.
>
> An entire wire harness assembly or a group of wires in such an assembly which carries parallel bits of data words or related control signals.
>
> An entire cable or a group of wires in a cable which carries parallel bits of data words or related control signals. A group of jumper wires or patch cords which carry parallel bits of data words or related control signals.

The transmission bus organization is shown in figure 2-2.

2.3 INSTALLATION

The central processor is designed for installation in a standard 19-inch wide equipment rack. Outline dimensions are shown in figure 2-3 and installation data is presented in table 2-3.

Table 2-3
Central Processor Installation Data

Requirement	Installation Data
Space Requirements	10-½ inches of height in a standard 19-inch wide equipment rack. The first additional 4096 word memory and each 8,192 additional words of memory need an additional 10-½ inches of rack space.
Weight	With 4096-word memory and power supplies: 90 pounds. With 4096-word memory and no power supplies: less than 35 pounds.
Installation	Four mounting screws on each side. No air conditioning, subflooring, special wiring or site preparation is required.

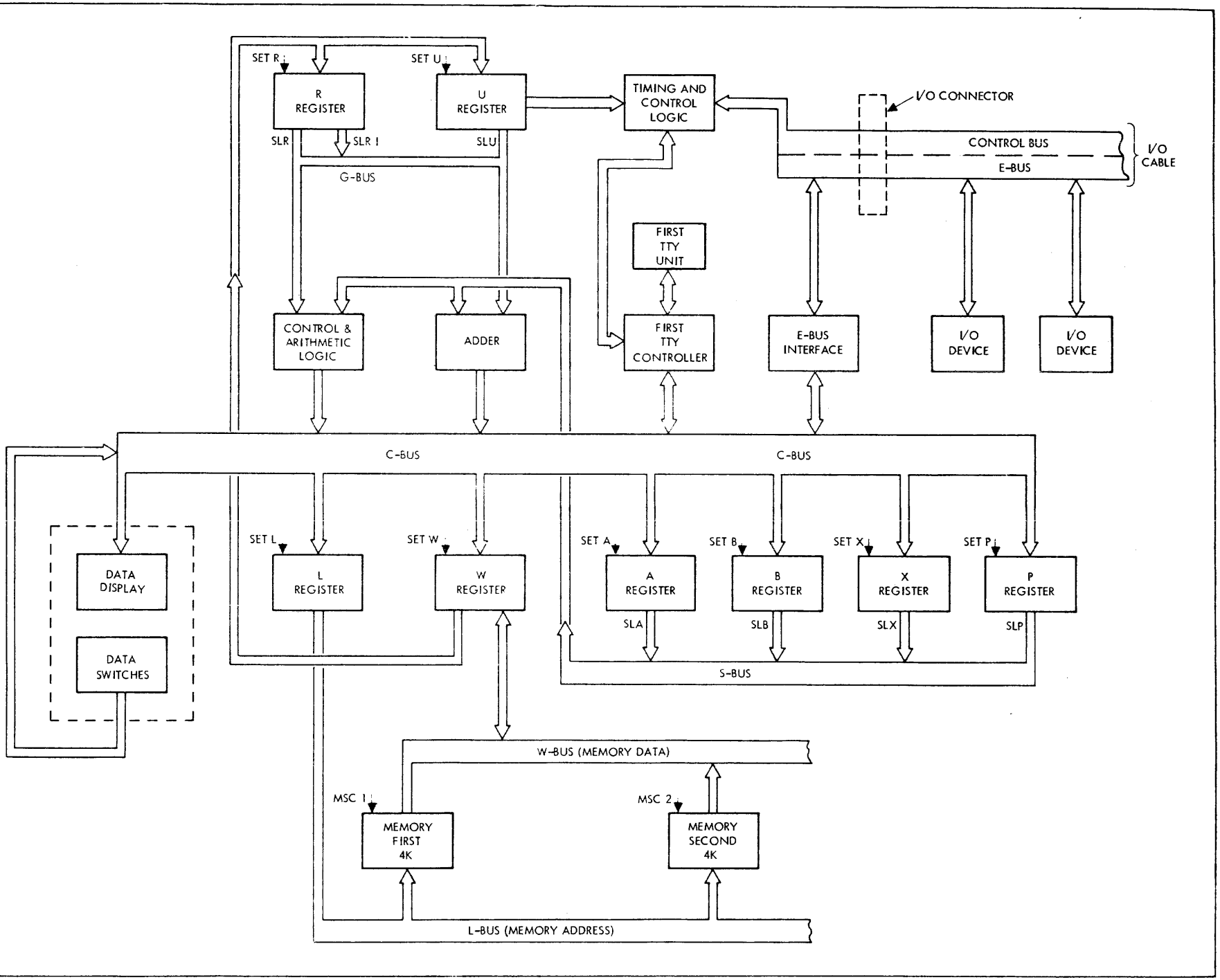


Figure 2-2. DATA 620/i Organization.

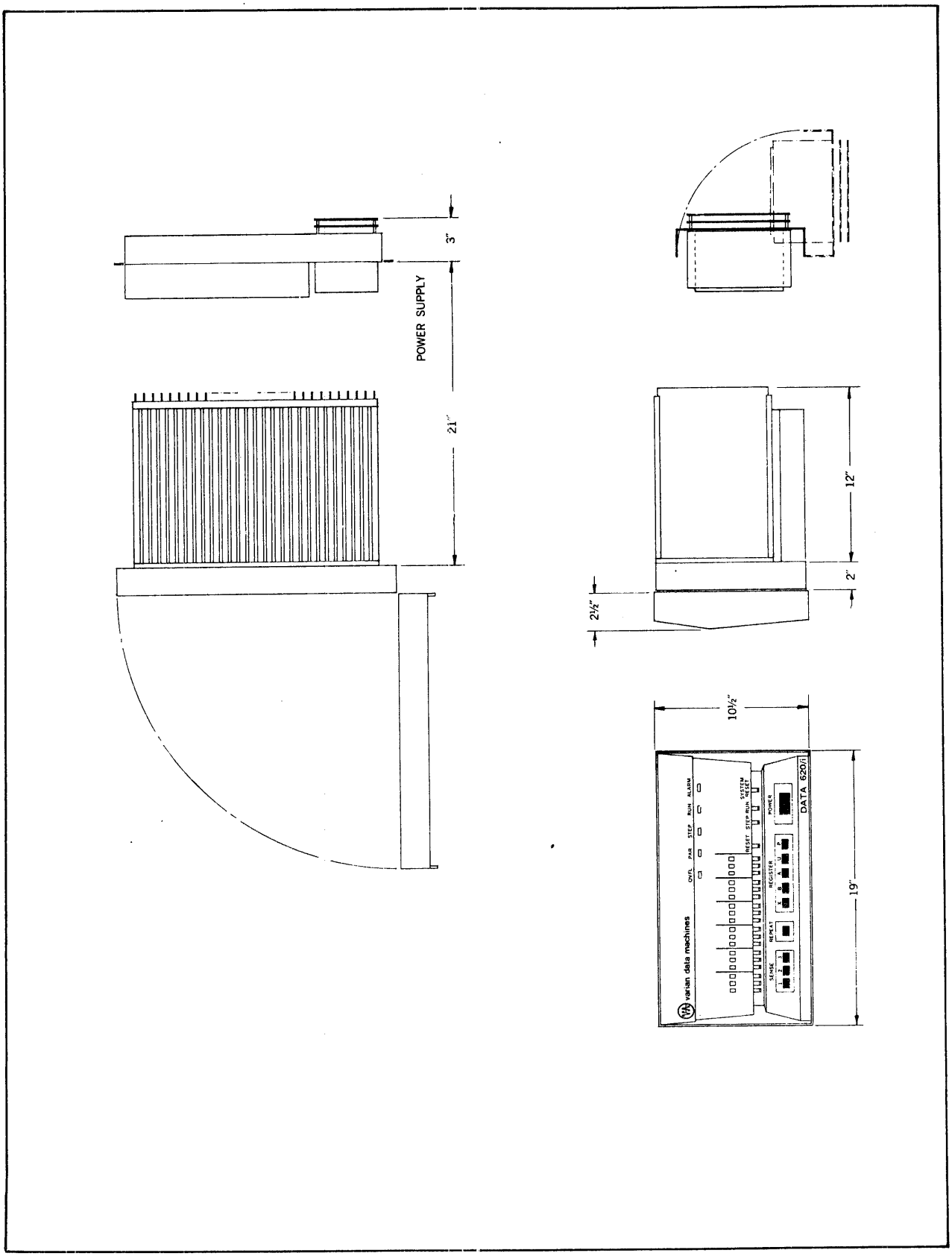


Figure 2-3. Varian Data 620/i Computer Outline Dimensions

Table 2-3
Central Processor Installation Data (continued)

Requirement	Installation Data
Power	Power source is 115 vac±10 vac, 48 to 62 Hz, 360 watts. Power supply connects to J30 and is normally mounted in hinged, swing-down chassis at the rear of the mainframe. Power supplies may be mounted up to five feet from powered units.
Circuit Cards	7-3/4 inches x 12 inches, printed circuits each side, components on one side only, edge connector mounted.

2.4 OPERATION

The control console of the central processor is a swing-away type control-indicator panel providing switching controls and displays for operator communication with the computer.

2.4.1 Control Switches

Control switches allow the operator to manually alter normal program operation. These switches provide considerable control flexibility and are useful for maintenance, troubleshooting and program debugging.

The SENSE switches are useful in normal program operation to allow selection of particular program sequences to be executed.

Data entry into a selected operational register is accomplished in the step mode (computer halted) by momentary-contact level-action switches. In the run mode, these switches are deactivated to prevent accidental alteration of the register contents.

MEMORY ENABLE/DISABLE Switch

The MEMORY ENABLE/DISABLE switch is included in this switch description even though its physical location is not on the console control-indicator panel. It is mounted on the main frame in the lower left corner and is accessible when the panel is swung away from the main frame. This switch serves the following purposes:

The ENABLE position enables all DATA 620/i memory (main frame and expansion frame) for control by the central processor. No program or manual operation can have access to the memory until the switch has been placed in the ENABLE position.

The DISABLE position disables all DATA 620/i memory from control of the central processor without disturbing the stored memory program. If the stored memory program is required to be retained, the computer should never be shut down without this switch being placed in the DISABLE position prior to shut down. (Note: The central processor must be placed in the step mode before placing the switch in the disable position. The memory can be disabled while the remainder of the central processor is enabled. This allows the operator to perform manual operations from the console not requiring memory access and is therefore an additional aid to troubleshooting.

Later configurations of the DATA 620/i computer do not contain the MEMORY ENABLE/DISABLE switch. Instead, they contain an automatic memory enable/disable (AMED) circuit. The AMED circuit automatically protects the contents of the 620/i memory during manual power turn on/off. Before initiating a power turn-off, however, the computer must be placed in the step mode (i.e. must be halted).

2.4.2 Displays

The console control-indicator panel can display, in binary-octal form, the contents of the instruction register and all the operational registers.

During normal operation (run mode) the contents of the C bus are continuously displayed.
Separate displays are provided to indicate operation in the run and step modes, and to indicate overflow and alarm conditions. Control switches and indicators on the console control-indicator panel are described in table 2-4.

Table 2-4
Console Control-Indicator Panel Functions

Control or Indicator	Function
Register Display	In-line display of 16 (or 18) bits of the C bus. Register bits are numbered from right to left with the sign bit appearing on the far left side of the display. Lights are grouped in an octal arrangement. Selection of the register to be displayed is accomplished by the register select switches which place the contents of the selected register on the C bus.
Status Display	Four, as follows: OVFL indicator; lights when the overflow flip-flop is set. STEP indicator; lights when the computer is in the step mode and the Micro-EXEC optional facility is not being used. RUN indicator; lights when the computer is in the run mode. ALARM indicator; lights when an over-temperature condition exists in the computer memory.
REGISTER Select Switches	Five alternate-action switches used to select one of five registers (X, B, A, U or P) onto the C bus for display. Only one register may be selected at a time. Simultaneous selection of more than one register disables the selection logic.
Bit Setting Switches	18 momentary-contact switches used to set bits of the selected operational register. When a bit is set, the corresponding register display lamp is illuminated.
RESET Switch	The RESET switch causes the selected register to be cleared. This switch is disabled when the computer is in the run mode.
STEP Switch	The STEP switch is a momentary-contact switch that causes the instruction in the U register to be executed if the computer is in the step mode. If the computer is in the run mode, pressing the STEP switch causes the computer to halt at the completion of the instruction being executed.
RUN Switch	The RUN switch causes the program to run at the location specified by the program counter after first executing the instruction in the instruction register.
SYSTEM RESET Switch	The SYSTEM RESET switch is a system-clear control that places the computer in the halt mode and initializes control flip-flops in the central processor. In addition, all peripheral devices are initialized by SYSTEM RESET.
REPEAT Switch	The REPEAT switch is an alternate-action switch that permits manual repeat of an instruction in the U register. Pressing the STEP switch executes instruction and advances the P register; however, the contents of the U register are left unchanged. This switch on the console control-indicator panel is activated only when the STEP light is lit (operation halted).

Table 2-4
Console Control-Indicator Panel Functions (continued)

Control or Indicator	Function
SENSE Switches 1,2,3	Three alternate-action switches that permit manual program control whenever the sense switch jump, jump-and-mark or execute instructions (JSS1, JSS2, JSS3, JS1M, JS2M, JS3M, XS1, XS2, XS3) are performed. The indicated jump and execute operations are performed only if the corresponding SENSE switch is on.
POWER On/Off Switch	The POWER on/off switch is an alternate-action press type switch/indicator that turns the power supplies on and off. The indicator lamp is illuminated when power is on and extinguished when power is off. This switch should not be placed in the off condition without first placing the MEMORY ENABLE/DISABLE switch in the DISABLE position (see 2.4.1). As described in paragraph 2.4.1, the MEMORY ENABLE/DISABLE switch is not included in later 620/i configurations.

2.4.3 Manual Program Entry and Execution

When the central processor is halted (step mode), programs and data may be read from memory and entered into memory, and a prestored program may be manually executed. Load, display and execute operations are as follows:

To load words into memory (either instructions or data), set the desired word in the A, B or X register. Set the appropriate store-type instruction (STA, STB, STX) with the desired operand address in the U register and press the STEP switch to execute the store operation.

To display any selected memory word in the A B, or X register; set the appropriate load-type instruction (LDA, LDB, LDX) with the proper memory address in the U register and press the STEP switch to load the selected word into the selected operational register.

To manually execute a program stored in memory, set the starting location of the program in the program counter (P register). When the STEP switch is pressed, the instruction contained in the U register is executed, and the instruction of the selected location is transferred to the U register. Repeated actuation of the STEP switch will then step through the program one instruction at a time. All address mode operations, such as multilevel indirect addressing, will be performed for each instruction each time the STEP switch is actuated. I/O instructions involving an asynchronous device, such as the teletype, which transfers data into a block, cannot be executed using the step mode.

Instruction Repeat

In the step mode, the U register contains the next instruction to be executed when STEP is pressed. The P register contains the location of the next instruction to be transferred to the U register after the current instruction is executed.

In some cases, it is desirable to manually execute an instruction several times. When the REPEAT switch is on, U register loading (when STEP is pressed) is inhibited even though the P register is advanced each time. This mode is particularly useful for loading words into sequential memory locations or for displaying the contents of sequential memory locations.

To load a group of sequential memory locations, set the appropriate store-type instruction (STA, STB, STX) in the U register with the relative address mode in the M field and the base address in the A field. Repeated operation of the STEP switch will store the contents of the selected A, B or X register into the appropriate sequential memory locations. The word loaded on each step may be changed by entering the desired value into the selected operational register for each step.

To display the contents of a group of sequential memory locations, set the appropriate load-type instruction (LDA, LDB, LDX) into the U register in the relative address mode (see table 2-5) and with the base address in the A field of the instruction register. The contents of the sequential locations will be displayed in the selected operational register with each actuation of the STEP switch.

SENSE Switches

The SENSE switches allow the operator to dynamically alter a program sequence in either the run or step mode. The three SENSE switches 1, 2 and 3 provide a logical-AND function with bits 6-8 of the instruction word respectively, and consequently can be used for various logical program deviations.

Table 2-5
Addressing Modes

M-Field Bit	Addressing Mode	Operation
0 X X	Direct	The A field is combined with bits 9 and 10 to form effective address (0000-2047).
1 0 0	Relative	The A field is added to contents of P register to form effective address.
1 0 1	Index (X)	The A field is added to contents of X register to form effective address.
1 1 0	Index (B)	The A field is added to contents of B register to form effective address.
1 1 1	Multilevel Indirect	The A field specifies location of an indirect address.

3.1 INTRODUCTION

This section presents the basic organization of the DATA 620/i central processor. The information presented is intended to familiarize the user with a general knowledge of the processor functions. The DATA 620/i includes the following functional elements:

a. Timing and control section

b. Arithmetic/logic section

c. Operational register section

d. Input/output section

e. Memory section

f. Console control-indicator panel

A basic organization diagram is shown in figure 2-2. It will be noted that the functional elements are connected by means of a bus structure. Explanation of bus content is contained within the paragraphs describing the various computer sections.

Computer options available for use in the DATA 620/i provide easy assembly of a customized system to fit each customer's needs. These options are covered in separate publications.

3.1.1 Timing and Control Section

This section provides timing for all computer functions, and buffers and decodes program instructions, coordinating timing and control sequences.

3.1.2 Arithmetic/Logic Section

This section contains the circuitry required for desired data manipulation under supervision of the timing and control section.

3.1.3 Operational Register Section

This section includes the A, B, X and P registers. All operational registers are full-length registers. The A, B and X registers are directly accessable to the computer programmer, while contents of the P register are available to the programmer through instructions which modify the program sequence (basically jumps). The A and B registers comprise the computer accumulator, the X register serves as an indexing register for operand addresses, and the P register holds the address of the next instruction to be executed. The P register is incremented before the present instruction is executed. The A register is the accumulator storing the results of logical and addition/subtraction operations. During multiplication and division, the A register forms the upper half of the accumulator storing the most significant half of the double length product in multiplication and the remainder in division. The B register forms the lower half of the accumulator, storing the least-significant half of the double-length product in multiplication and the quotient in division. Both the A and B registers may be used for input-output transfers under program control. The B register may also be used for indexed address modifications, if desired. Using the B or X registers for address modifications adds no time to instruction execution.

3.1.4 The Input/Output Section

This section provides for data and control signal transmission between the computer and any peripheral device connected to the I/O cable. Up to 64 such devices may be addressed on the I/O cable. Capabilities of the I/O section include:

a. Data transfer under program control

b. Data transfer under external control

c. Sensing of external input devices

d. Transmitting control signals to peripheral devices

3.1.5 Memory Section

A basic internal memory composed of 4,096-word storage is provided in the DATA 620/i. This memory is expandable by addition of 4096-word memory modules (to 16K standard; 32K on special request), without an increase in computer operational time. One L (address) register and one W (data word) register are included in the basic computer. Only one L and one W register are required, regardless of the number of memory modules.

A MEMORY ENABLE/DISABLE switch is located behind the front panel. This switch is used to prevent loss of memory storage during power change.

3.1.6 Control Console

The manually operated console control-indicator panel, containing a visual display of the content of the operational registers and the instruction register, is provided on the front face of the DATA 620/i. In addition to the normal POWER on/off switch, provision is made on the console to change the contents of any register, to restart or reset an optional peripheral controller, and to sense the status of any peripheral device. In addition, provision is made to operate a program in a one-step mode or to repeat any instruction for the purpose of diagnosis or troubleshooting.

3.2 COMPUTER WORD FORMATS

There are two basic word formats used in the DATA 620/i: data and instruction. The instruction word format is further divided into four types: single-word addressing, single-word non-addressing, double-word addressing and double-word non-addressing.

3.2.1 Data Word Format

Data words may contain operands, operand addresses or indirect addresses, depending upon the instruction or addressing mode in process. The data word format is shown in figure 2-4.

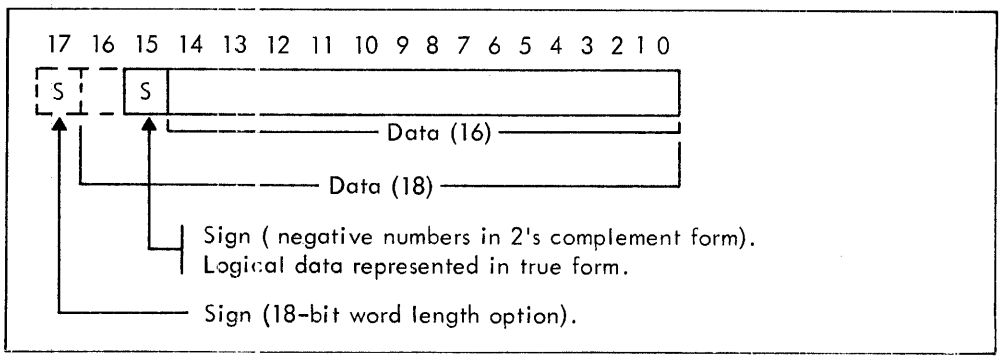


Figure 2-4. Data Word Format

The data word may be either 16 or 18 bits depending upon the word length configuration of the particular machine. In the 16-bit format, data occupy bit positions 0-14, with the sign in position 15. In the 18-bit format, data occupies bits 0-16, with the sign in position 17. Negative numbers are represented in 2's complement form.

3.2.2 Indirect Address Word Format

A data word may contain an indirect address. An example of an indirect address word format is shown in figure 2-5.

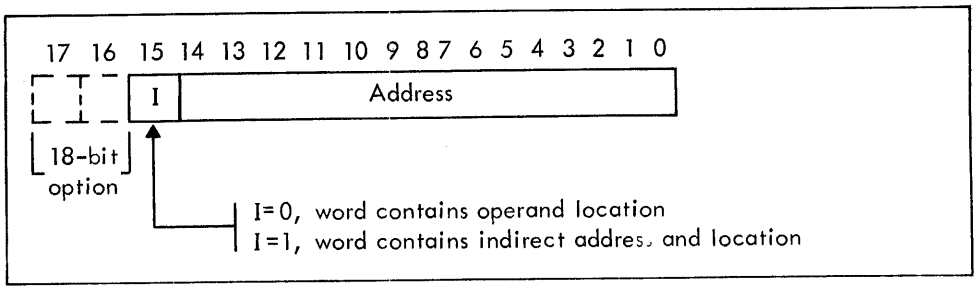


Figure 2-5. Indirect Address Word Format

This word occupies a location in memory which is accessed by an instruction in the indirect address mode. Bit 15 contains the I bit, which designates whether the memory location being addressed contains (I=0), or contains the location of the operand or of yet another indirect address word (I=1). Indirect addressing may be extended to any desired level. Each level of indirect addressing adds one cycle (1.8 microseconds) to the basic execution time of an instruction.

3.2.3 Instruction Word Formats

Instruction words may be either addressing or non-addressing. The instruction word format is shown in figure 2-6.

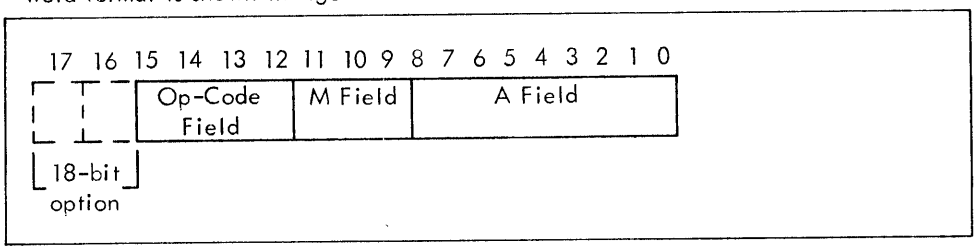


Figure 2-6. Instruction Word Format

The format shown is applicable to all instruction words. For double-word instructions, the format shown applies to the first instruction word. The instruction word is divided into three fields; op-code field, M field and A field. The function of the three fields varies according to the type of instruction, but may generally be defined as follows:

Op-code field	bits 12-15	Designates type of instruction (e.g., single-word addressing, I/O instructions or other).
M field	bits 9-11	Designates address mode or mode of operation.
A field	bits 0-8	Contains a variety of information depending upon the type of instruction (see following paragraphs and appendix G).

3.2.4 Single-Word Instructions

Addressing Instructions. Addressing instruction groups applicable to this type of instruction are: LOAD/STORE, ARITHMETIC and LOGICAL. These instruction groups are designated by octal numbers 01 through 07, and 11 through 17 in the op-code field. The M field contains one of the following addressing modes:

Mode	M-Field
Direct	0 X X
Relative mode	1 0 0
Index (X)	1 0 1
Index (B)	1 1 0
Indirect	1 1 1

For direct addressing, bits 9 and 10 of the M field are combined with the A field to form a direct address to any of 2048 locations. (Table G-1(d), in appendix G explains use of the A field in conjunction with the addressing modes shown above).

Non-addressing instructions. Instruction groups applicable to this type instruction are: SHIFT, CONTROL, REGISTER CHANGE and INPUT/OUTPUT. The op-code field contains octal 00 except for the last type, INPUT/OUTPUT, which is designated by octal 10. The M field designates the mode of operation, and the A field specifies the action to be performed by the computer such as:

a. Number of shifts

b. Kind of register change as well as source and destination registers

c. Input/output

3.2.5 Double-Word Instructions

Double-word addressing. This instruction format is shown in figure 2-7.

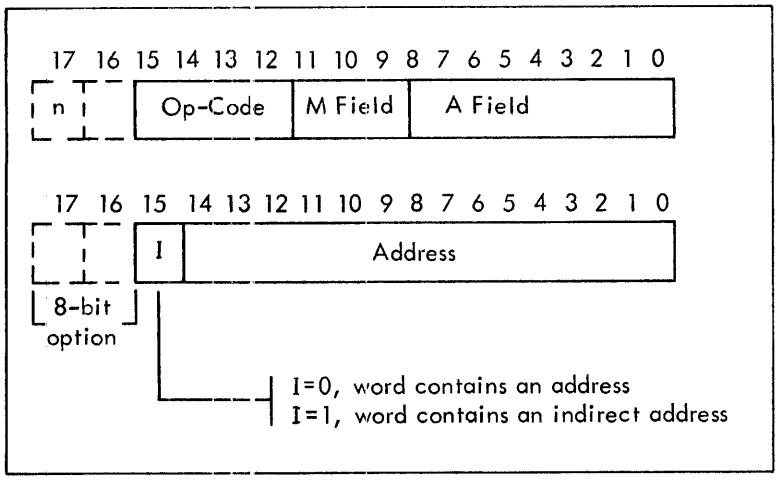


Figure 2-7. Double-Word Addressing Instruction Format

This format is used for the following types of instructions:

JUMP

JUMP AND MARK

EXECUTE

EXTENDED ADDRESS

For all of the above types of instructions, the op-code field contains octal 00; the M field an octal one, two, three or six, designating the mode of instruction to be performed; and the A field (except for EXTENDED ADDRESS) defines a set of nine logical states which condition execution of the instruction. The second word contains the instruction address, or the location of the instruction to be executed if the condition is met. Indirect addressing is permitted.

For extended address type instructions, the A field is further divided into two sub-fields. Bits 0-2 are coded as shown in figure 2-8 to indicate the address mode. Bits 3-8 contain any single-word operation instruction which, in a single word instruction ordinarily appear in the op-code field. The second word contains the effective address which may be direct or indirect depending upon the condition established by bit 15.

A-Field Bits	Address	Effective Address
1 0 0	Relative to P	Contents of second word plus (P register plus 1).
1 0 1	Indexed with X	Contents of second word plus X register.
1 1 0	Indexed with B	Contents of second word plus B register.
1 1 1	Direct or Indirect	Contents of second word is the direct address if bit 15 is ZERO. Contents of second word is an indirect address if bit 15 is ONE.

Figure 2-8. Address Modes for Extended Address

Double-Word non-address instruction. This is an immediate type instruction, which uses the same word format as described for the extended type instruction. The op-code field contains octal 00 and the M field contains an octal 6. The A field contains the operation mode (octal 0) in bits 0-3, and bits 3-8 contain a single word operation instruction. Since indirect addressing is not permitted, the second word always contains an operand.

4.1 INTRODUCTION

This section presents the general theory of operation of the various sections of the central processor, and is intended to familiarize the user with the method of handling data and instructions by these sections.

A discussion of timing and control logic, decoding logic and arithmetic logic, is followed by the theory of operation of the various registers, input and output circuitry and internal memory interface, followed by a discussion of transfer operations and typical operating sequences.

4.2 TIMING AND CONTROL LOGIC

All operations performed by the DATA 620/i system are controlled by the timing logic generated in the timing and control section. Basic timing signals are derived from a master clock circuit located on processor control card #4 (DM112). The master clock is generated by a crystal controlled oscillator operating at a frequency of 8.8 MHz which is counted down and passed through a pulse-width adjustable one-shot to produce a continuous train of pulses typically 56 nanoseconds wide, spaced 450 nanoseconds apart. This output (MCLX+), is used to generate the various clock signals shown in figure 2-9.

The DATA 620/i has a basic machine cycle of 1.8 microseconds. A full memory cycle (read/restore or clear/write) is performed within this period, except for special cases which are described in subsequent paragraphs. All operations performed by the computer are accomplished in some multiple of the master clock timing cycle. In execution of various instructions, up to four suboperations may be performed during the basic machine cycle of 1.8 microseconds.

Functions performed by the DATA 620/i are divided into two basic phases:

a. Operation upon words read from memory or storing words into memory (execute phase)

b. Transfer of instructions or operand addresses into memory (address phase)

These phases are related to the basic clocks as described in table 2-6. Timing of the basic clocks and the two basic phases may be determined by referring to figure 2-9.

4.2.1 Sequence Control

The basic clocks generated from the master clock are used to time three operating sequences: instruction cycle, address cycle and operand cycle. All operations performed by the computer are timed by one or more of these sequences.

Instruction cycle (ICYX+). During this cycle, the next instruction to be executed is read from memory and transferred to the instruction register (U register) in the control section. The instruction cycle period is equal to a complete memory cycle (1.8 microseconds) and consists of two phases: instruction execute (IEPX+) and instruction address (IAPX+). These phases are synchronous with the basic address and execute phases (EPHX+ and EPHX-) respectively. During the first half of the instruction cycle, the execute phase, an operation specified by a previous instruction word is performed (e.g., add, load operational register, etc.). Although this phase is normally 0.9 microseconds, it may be extended by a clock modifier. Such modification of phase timing is explained in a subsequent paragraph.

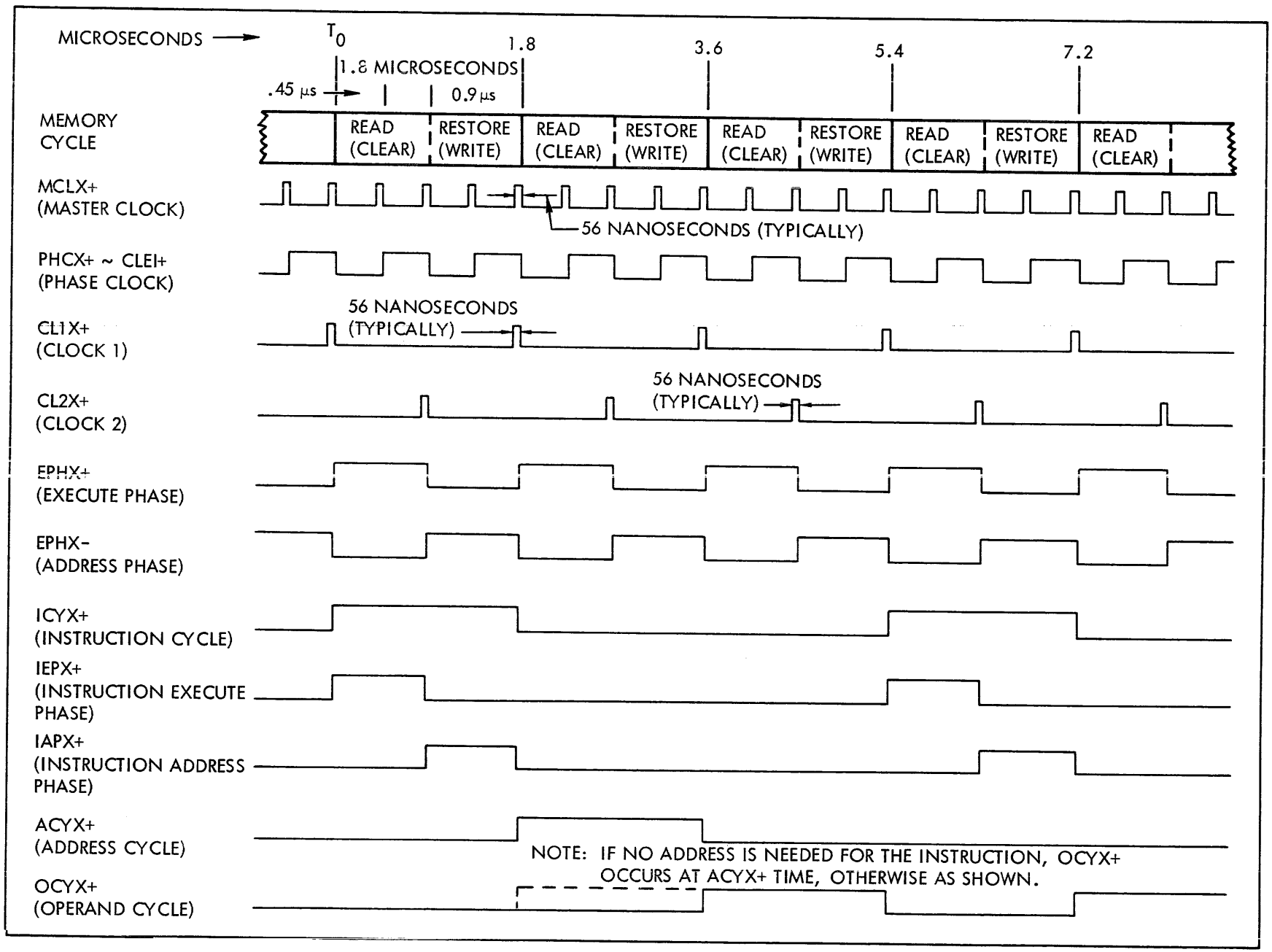


Figure 2-9. Clock and Phase Timing

Table 2-6. Timing Signals

Signal	Description
Master Clock (MCLX+)	Basic 2.2-MHz crystal-controlled timing signal for the entire system.
Phase Clock (PHCX+)	1.1-MHz timing signal derived from and in phase with the master clock. This clock is used to time the address and execute phases.
Address Phase (EPHX-)	Timing signal synchronous with the restore or write half cycle of memory. This signal is used to time all transfers of instruction and operand addresses to memory.
Execute Phase (EPHX+)	Timing signal synchronous with the read or clear half cycle of memory. This signal is used to time all transfers of data to and from memory, and execution of instructions.
Clock 1 (CL1X+)	Timing signal used to initiate a memory cycle and all operations synchronous with the start of a memory cycle.
Clock 2 (CL2X+)	Timing signal used to initiate all operations synchronous with the start of a memory write or restore half cycle.

During the instruction address phase, the location of a word in memory (if specified by the current instruction in the U register) is generated and transferred to the memory L register. Generation of the address may involve modification of a basic address contained in the instruction (e.g., indexing, relative address, etc.).

Address Cycle (ACYX+). The address cycle is of 1.8 microseconds duration and is synchronous with the basic memory cycle. When a single-word instruction indirectly addresses an operand, the instruction specifies the location of an address word in the memory. The same is true for double-word instructions where the second word is an address (such as jump instructions). This address word may contain the location of the operand, or it may contain another indirect address.

During the first half of the address cycle, the address word is read from memory and transferred to the R register. During the second half, the sign (I) bit (bit 15) is examined to determine whether the next word accessed will be another indirect address or an operand. Several address cycles may be performed between instruction and operand cycles.

Operand Cycle (OCYX+). This 1.8 microsecond cycle follows the instruction cycle, unless the final operand is indirectly addressed, in which case, the operand cycle follows the address cycle. After the previous two cycles have determined that the data referenced in the current instruction is an operand and not an indirect address, the operand so referenced is either read from memory and stored in the R register or is transferred from the computer to the W register and stored in the memory.

4.2.2 Clock Modifiers

The execute or address phase may be modified by certain program instructions or by signals received from devices external to the computer. The conditions under which the clocks are modified are as follows:

Shift: During shifting operations with words contained in the A or B register, the execute phase (EPHX+) is extended by the number of master-clock periods (0.45 microseconds) equal to the specified number of shifts.

Interrupt: When an external interrupt is received, the address phase (EPHX-) is extended 0.9 microseconds to accommodate delays in receiving the interrupt address from the external device.

Trap: When a buffer interlace controller requests a transfer to or from memory, the address phase (EPHX-) is extended 3.15 microseconds to permit the execution of the full trap sequence (routing of address and data from the external device).

Halt: On a halt instruction, clocks CL1X+ and CL2X+ are inhibited. This prevents further computer operations until the STEP or RUN switch is operated.

Modification of the execute phase of an instruction is illustrated in figure 2-10. This modified sequence is typical of a shift instruction. At time T_0, the instruction is accessed from memory. Starting at time $T_{1.8}$, the instruction is executed; however, the normal 0.45-microsecond execute phase is extended 0.45 microseconds for each shift (four, in this illustration). Note that clocks 1 and 2 (CL1X+ and CL2X+) are inhibited during the extended execution period. In a similar manner, the address phase is extended when required by the conditions defined above.

4.3 DECODING LOGIC

The basic word structure used in the DATA 620/i is described in section 3. Words stored in the instruction register (U register), must be decoded in order to determine program processing requirements. This decoding procedure is accomplished on processor control cards #'s two and three (DM-110 and DM-111). Outputs are used to enable arithmetic and logical operations, memory access and input and output circuits according to results of the decoding operation. (Reference to section 3 for word format, and to the logic diagrams in chapter 7 for operational circuits, will provide an understanding of the decoding procedure.)

As may be seen from the word formats described in section 3, the sixteen bits of an instruction word are divided into three fields. These are; op-code field (bits 12-15), M field (bits 09-11) and A field (bits 00-08). Each of these fields contains information which directs the various computer processes.

4.3.1 Op-Code Field Decoding

Information contained in this field is decoded in three functional categories: class, set and group.

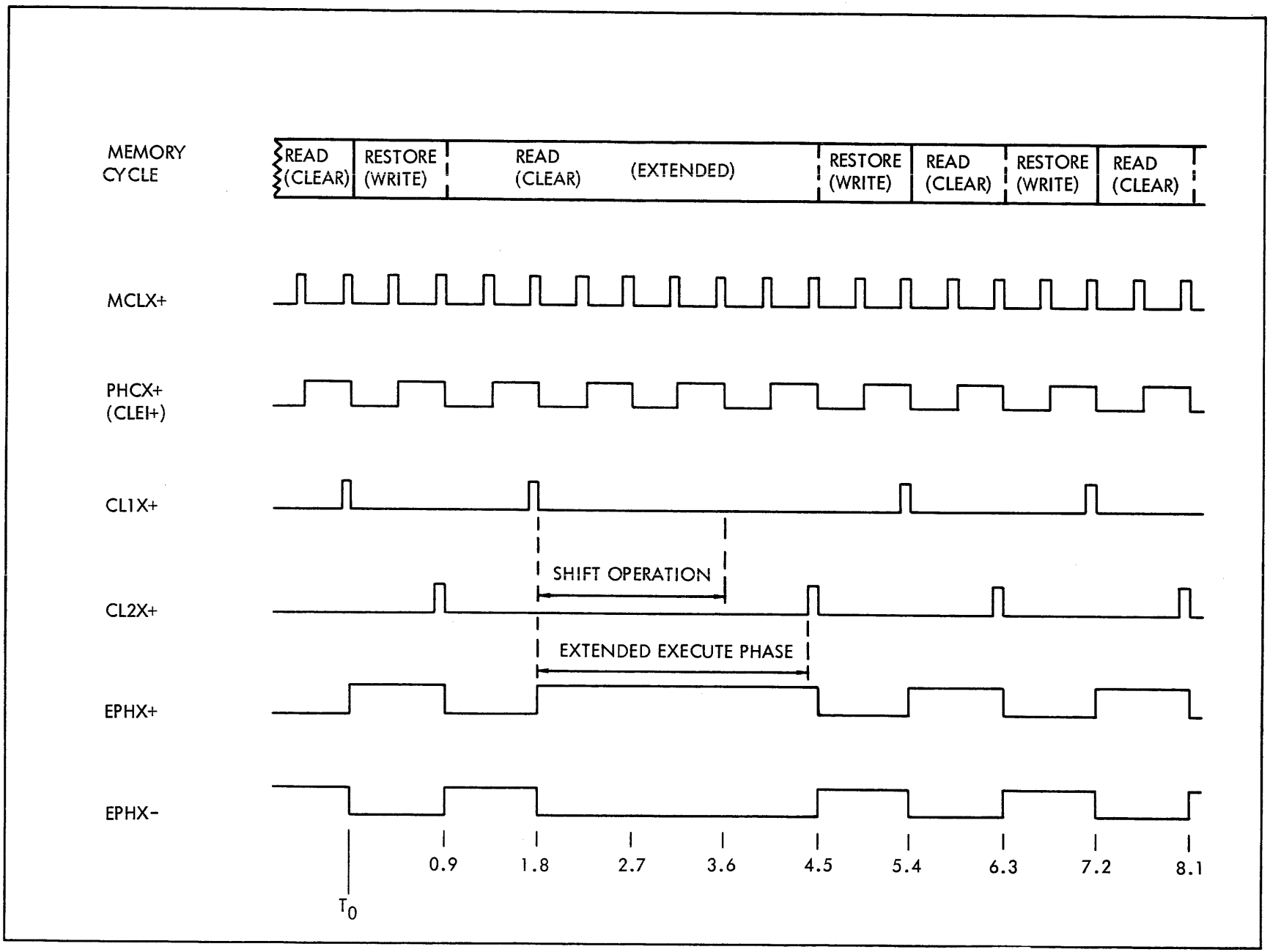


Figure 2-10. Example of Modified Clock Sequence

Class decoding separates instructions into the following classes:

a. Single-word addressing instructions

b. Input/output instructions

c. Other (includes single-word non-addressing, and double-word)

Table 2-7 lists op-code field codes, signal names derived by decoding these codes and a description of the class.

Table 2-7. Op-Code Classes

Codes (Bits 12-15)	Signal Names	Description
01-07 11-17	K1XX+	All single-word addressing instructions.
00	K2XX+	Single-word non-addressing and double word instructions.
10	K3XX+	All I/O instructions.

Set decoding divides the single-word addressing type instructions into sub-categories: load, store and arithmetic and logic types. Table 2-8 lists these sets, along with the signal name derived from decoding and a description of the set.

Table 2-8. Op-Code Sets

Codes (Bits 12-15)	Signal Names	Description
00-03	H1XX+	Instruction cycle execute phase of all load-type instructions.
04-07	H2XX+	Operand cycle execute phase of all store-type instructions and INR.
11-15 16-17	H3XX+ H4XX-	Instruction cycle execute phase of all arithmetic and logic type instructions (except INR).

Group decoding is structured to gate various computer operations, according to the function desired. Table 2-9 lists these groups, signal names derived from decoding and type of instruction. One of these groups is true for all single-word addressing type instructions.

Table 2-9. Op-Code Groups

Codes (Bits 12-15)	Signal Names	Instruction Type
01, 05, 11, 15	G1XX+	LDA, STA, ØRA, ANA
02, 06, 12, 16	G2XX+	LDB, STB, ADD, MUL (*)
03, 07, 13, 17	G3XX+	LDX, STX, ERA, DIV (*)
04, 14	G4XX+	INR, SUB

4.3.2 M-field Decoding

The M field (bits 9-11) of the instruction word is decoded to determine the addressing mode for class K1 (single-word addressing instructions) and the instruction type for all other instructions. Note that class K3 contains all I/O instructions and the M field specifies a subtype. Address modes or instruction types which are determined by decoding the M field are listed in table 2-10 arranged by op-code class.

Table 2-10. M-Field Decoding

Class	M-field Code	Signal Name	Address Mode or Instruction Type
K1 (K1XX+)	0-3	AC0X+ to AC3X+	Direct address
	4	AC4X+	Relative address
	5	AC5X+	Index X
	6	AC6X+	Index B
	7	AC7X+	Indirect address
K2 (K2XX+)	0	AC0X+	Control (HLT only)
	1	AC1X+	Jump
	2	AC2X+	Jump and mark
	3	AC3X+	Execute
	4	AC4X+	Shift
	5	AC5X+	Register change
	6	AC6X+	Immediate or extended (optional)
	7	AC7X+	Set or reset overflow
K3 (K3XX+)	0	AC0X+	External control
	1	AC1X+	Sense
	2	AC2X+	Data input
	3	AC3X+	Data output
	4	AC4X+	Auxiliary External Control

4.3.3 A-field Decoding

For single-word addressing type instructions, the A field is decoded to provide:

a. An effective address, or

b. A number, which when combined with the content of the B, X or P register, provides an effective address.

For single-word non-addressing type instructions, the A field specifies additional details for the instruction type determined by the M field. (See tables 2, 3 and 4, appendix G, for types of additional instructions determined by the A field.)

For double-word addressing type instructions, the A field determines conditions to be met if the instruction is to be executed. (Tables 5, 6, 7 and 8 of appendix G list the A field content for these conditions.)

For extended address option type double-word instructions, bits 0-2 of the A field determine the address mode. Octal codes for this bit group are the same as the M field for single-word addressing instructions. Bits 3-8 contain the same octal codes specified in table 2-9 for op-code groups, for single-word addressing type instructions. (Note that for this set of codes, the most-significant digit is never greater than one; consequently bits seven and eight are always zero.)

Double-word non-addressing instructions are of the immediate type, and are identical with extended address optional instructions described above, except that bits 0-2 always contain an octal zero. The A field is used in I/O instructions to specify the logical unit number (bits 6-8) and device address (bits 0-5). See table 9 of appendix G for details of this assignment.

4.4 ARITHMETIC AND LOGICAL SECTION

The arithmetic and logical section consists of several sub-sections: The R register, R-register gates, arithmetic bus (A bus), adder, logic gates and the S register. Physically, all of these circuits except the S register are located on the three register cards (DM 108), six bits per card. The S register, or shift register is located on processor control card # 4 (DM112).

The R register receives operands from memory via the W register and holds these words during execution of an arithmetic or logical instruction. The R register gates enable either the set or reset output of the R register or the output of the U register onto the G bus, depending on whether an operand stored in the R register or the A field of the instruction word stored in the U register is to be used. The G bus provides this data to the adder, in the case of arithmetic operations, or through a set of logic gates, to the C bus, depending on the operation in progress. An additional input to the adder is from the S bus, carrying data from the operational registers. The adder may provide the logical product of the contents of the R register and one of the operational registers, if required by the program instruction being executed. S register outputs are provided to the logic gates, allowing shifting of the data either right or left as specified.

The arithmetic bus (A bus) is an intermediate bus used for arithmetic output to the C bus or for external data input to the logic gates and operational registers. It also provides an alternate path for transferring memory words to the C bus. Outputs from the adder and from the logic gates are provided to the C bus.

4.5 REGISTERS

The central processor contains nine registers. Each register bears a letter reference designation to facilitate identification. These are: U, R, A, B, X, P, X, L and W.

4.5.1 U Register

The U register is the instruction register in the control section of the central processor. It is a full-word register, 16 bits long, and is physically located on circuit card DM108. (DM108 contains six bits each of all registers except the S and L registers. The three cards are interchangeable.) The U register is clocked by SETU+ from pin 31 of circuit card DM111, which occurs at the leading edge of the instruction execute phase (IEPX+). The bits of the U register are set or reset by the corresponding output bits from the W register.

This register receives each instruction from memory through the W bus and holds the instruction during its execution. The control fields of the instruction word are routed to the decoding and timing logic where the codes determine the required timing and control signals. The address field from the U register, used for various addressing operations, is routed to the arithmetic/logic section of the central processor.

Information Transfer from Memory to U Register

During the instruction cycle, the instruction word located by the address in the L register is read out to the W register and transferred to the U register through the W bus.

Information Transfer from U Register to Memory

For many instructions requiring an operand, the address of the operand is contained in the instruction word held in the U register. This operand address is transferred to the L register through gates in the arithmetic logic section and the C bus. The address from the U register may be modified during transfer to the L register as follows:

a.	Direct address:	No modification; bits 0-10 transferred from the U register (SLU1 and SLU2 true) to the L register directly. Addresses the operand in the first 2048 memory locations.
b.	Relative address:	The effective operand address transferred to the L register is formed by adding bits 0-8 (SLU1 true) from the U register to the contents of the P register. Addition is performed by selecting contents of the P and U registers and bringing them into arithmetic logic. This permits addressing any word up to 511 locations ahead of the current program location.
c.	Index address:	The effective operand address transferred to the L register is formed by adding bits 0-8 from the U register (SLU1 true) to the contents of either the X or the B register.
d.	Indirect address:	Same transfer as direct address except the word read from memory will be the address of an operand instead of the operand.

4.5.2 R Register

The R register is the operand register in the arithmetic/logic section of the central processor. It is a full-word register, 16 or 18 bits long and is physically located on circuit card DM108. The R register is clocked by SETR+ (pin 2 of circuit card DM111) which occurs during the time of instruction cycle not (ICYX-) and clock 2 (CL2X+). The bits of R register are set or reset by the corresponding outputs from the W register.

This register receives data words read from memory through the W bus and holds these words during execution of an arithmetic or logical instruction.

Information Transfer from Memory to R Register

Operands are stored in the R register while an arithmetic or logical operand is being performed. For indirect addressing and for instructions with operand address stored in the memory location following the instruction word, the operand address is read from memory into the W register and then transferred to the R register. The operand address is then routed to the L register through gates in the arithmetic logic section and the C bus. I/O transfers bypass the R register. This allows momentary halting of the multiply and divide operations while the I/O transfer proceeds, without disturbing the multiplier held in the R register.

4.5.3 A Register

The A register is the accumulator register. For multiply operation, it forms the high-order half of the accumulator. It is one of the four operational registers. It is a full-word register, 16 or 18 bits long, and is physically located on circuit card DM108.

The A register is clocked by SETA+ (pin 56 of DM111 card) which occurs during program data in, load A register, shift and certain register change instructions, and during the instruction cycle execute phase of all arithmetic and logic instructions. The bits of the A register are set or reset by the corresponding bits of the input words from the E, A and C buses.

This register accumulates the results of logical and addition/subtraction operations, the most significant half of the double-length product in multiplication and the remainder in division. It may also be used for I/O transfers under program control.

Information Transfer

Input words may be transferred directly to the A register through the E, A and C buses. These transfers are always controlled by an instruction. Output words may be transferred from the A register to the I/O cable through the S, A and C buses. These transfers are controlled by an instruction which selects the A register onto the S bus.

4.5.4 B Register

The B register is the low-order half of the accumulator. It is one of the four operational registers. It is a full-word register 16 or 18 bits long, and is physically located on circuit card DM108. The B register is clocked by SETB+ (pin 38 of

DM111 card) which occurs during program data in, load B register, shift and certain register change instructions. The bits of the B register are set or reset by the corresponding bits of the input words from the E, A and C buses.

This register accumulates the least significant half of the double-length product in multiplication and the quotient in division. It may also be used for I/O transfers under program control and as a second hardware index register.

Information transfer to and from the B register is accomplished in the same way as described for the A register.

4.5.5 X Register

The X register is the index register. It is one of the four operational registers. It is a full-word register, 16 or 18 bits long, and is physically located on circuit card DM108. The X register is clocked by SETX+ (pin 11 of DM111 card) which occurs during load X register and certain register change instructions. The bits of the X register are set or reset by the corresponding bits of the input words from the E, A and C buses.

This register permits indexing of operand addresses without adding time to execution of indexed instructions by holding the value which modifies a base address contained in an instruction.

4.5.6 P Register

The P register is the program instruction counter. It is one of the four operational registers. It is a full-word register, 16 or 18 bits long, and is physically located on circuit card DM108. The P register is clocked by SETP+ (pin 12 of DM111 card) which occurs during the instruction cycle execute phase of I/O, execute immediate, single word non-addressable and double word instructions. SETP+ also occurs during mark, fetch instructions and execute jump or sense conditions. The bits of the P register are set or reset by the corresponding bits of the input words from the E, A and C buses.

This register holds the address of the current instruction and is incremented before each new instruction is fetched. The P register contents may be modified directly by a word received from the memory during a jump instruction.

Information Transfer from P Register to Memory

Before the next instruction cycle begins, the location of the next instruction is transferred from the P register to the L register. The contents of the P register are transferred through the S bus to arithmetic/logic. Arithmetic/logic increments the location address with the arithmetic gates and transfers the incremented count to the C bus. The incremented count is then restored to the P register and to the L register. At this time, the L register contains the address of the next instruction word to be fetched from memory and the P register holds the updated address.

4.5.7 S Register

The S register is the shift counter in the arithmetic/logic section of the central processor. It is a five-bit register and is physically located on the DM112 card. The S register is reset by reset shift register (RSHX+) from pin 29 on circuit board module DM110. The S register is set by shift control pulses derived from the U register.

This register controls the length of shift instructions in combination with the U register.

4.5.8 L Register

The L register is the memory word location register in the memory section of the central processor. It is a full-word register, 16 bits long, and is physically located on circuit board module DM109. The L register is clocked by SETL+ (pin 29 of the DM112 card) which occurs on every clock 1 (CL1XT) except during increment memory and replace. The L register is set by CB00+ thru CB15+ bits from the C bus.

This register contains the location of the word to be accessed in memory during either a clear/write or read/restore cycle.

Information Transfer to and from Memory

Input data from the E bus can be routed directly to memory through the A, C and W buses. Data transfer must be preceded by an address transfer instruction to load the memory location into the L register. When the transfer is under the control of an instruction, the memory address will be generated as a normal operand address. Output words may be transferred directly from memory to the I/O cable through the A, C and W buses, but a storage address must first be transferred to the L register by an address transfer instruction or from the peripheral device.

4.5.9 W Register

The W register is a word register in the central processor which holds data words for transmission to the memory and stores data words transmitted to the central processor from the memory. It is a full-word register, 16 bits long, and is physically located on the DM108 card. The W register is clocked by SETW+ (pin 26 of the DM112 card) which occurs during the operand cycle execute phase of all store type instructions and during the operand cycle of a program data in instruction. The bits of the W register are set or reset by the corresponding bits of the C bus. They are also collector-set independent of the SETW+ clock by the true bits from memory on the W bus during a memory read/restore cycle.

4.5.10 Register Change Instructions

The contents of an operational register may replace or modify the contents of itself or another register. The process of incrementing and restoring the contents of the P register has been described in 4.5.6. The contents of the A, B and X registers may be transferred, incremented, complemented, decremented or shifted. All these operations involve selecting the register onto the S bus, processing in the arithmetic/logic section, and transferring the new data through the C bus to the proper registers. Shifting is also performed in this transfer path.

The contents of the selected register are shifted left or right as they are gated from the control and arithmetic logic to the A bus.

Note that this transfer path is involved in all register change instructions.

The register change instruction format is shown in figure 2-11.

The op code = 00 and M = 5_8 for this type of instruction. The A field enables the register change operation to be micro-programmed by arbitrary selection of source, destination and type of transfer. The types of transfer, designated by the control function in bits 6-8, are summarized in table 2-11.

The normal operation involves designating one source and one or more destinations (note that if no source is designated, the selected destinations will be cleared). If more than one source is designated, the result will involve the logical OR of the sources; complementing will produce the NOR of the selected sources. This micro-programmed register change type of instruction provides 64 combinations of sources and destinations, each of which may occur in eight different ways. Thus, a total of 512 different register change operations may be executed.

4.6 INPUT/OUTPUT SECTION

The central processor has input/output communication with the console control-indicator panel, the memory and the peripheral options.

4.6.1 Console Control-Indicator Panel

The console control-indicator panel receives manual control inputs through the control switches and transfers them to the central processor through the A bus. The panel receives data and instructions from the central processor through the C bus and displays the data or instructions on the face of the panel. Interface connections are described in detail in 2.1.

4.6.2 Memory

The central processor communicates with the memory through the L and W buses (see figure 2-2). Memory communications are described in detail in paragraph 4.7 and in chapter 3.

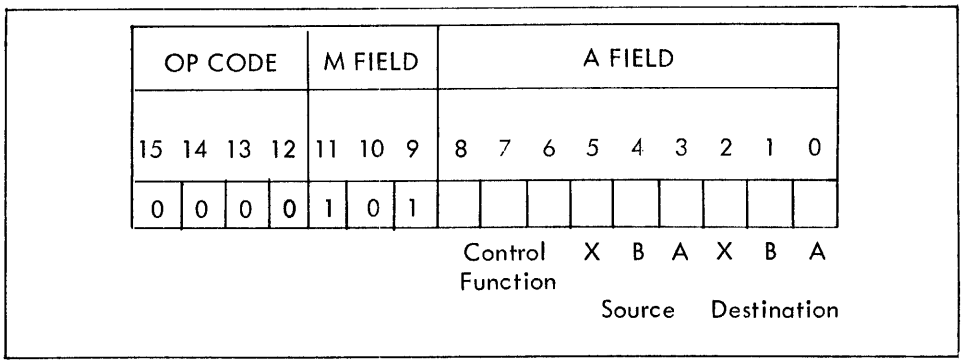


Figure 2-11. Register Change Instruction Format

Table 2-11. Transfer Control Function Codes

BIT 8	7	6	Control Function
0	0	0	Transfer source, unconditional.
0	0	1	Increment source and transfer, unconditional.
0	1	0	Complement source and transfer, unconditional.
0	1	1	Decrement source and transfer, unconditional.
1	0	0	Transfer source, if overflow is set.
1	0	1	Increment source and transfer, if overflow is set.
1	1	0	Complement source and transfer, if overflow is set.
1	1	1	Decrement source and transfer, if overflow is set.

4.6.3 Peripheral Options

The central processor communicates with the peripheral options through the input/output section. This section contains the E bus drivers and receivers which transfer data and control instructions to and from the peripheral options through the E bus portion of the I/O cable. Output words from the C bus are transmitted over the E bus. Input words from the E bus are transmitted to the C bus through the A bus. Control and timing signals to and from the control section are transmitted through the external I/O control bus of the I/O cable as shown in figure 2-2. The E bus and I/O control bus constitute the I/O cable to which peripheral option controllers and the peripheral options are attached.

4.6.4 I/O Cable Connections

The I/O cable contains 37 twisted-pairs of 24-gauge stranded wires and is segmented as follows:

The first segment extends from cable plug P32 at the rear of the central processor main frame to cable receptacle J32 at the rear of the first expansion frame.

The second segment extends from cable plug P32 at the rear of the first expansion frame to cable receptacle J32 at the rear of the second expansion frame.

Succeeding expansion frames may be added, as required, by cabling in the same manner as the second segment. The last expansion frame added is terminated in a terminating shoe mounted on cable receptacle J32. Similarly, when special external equipment is connected to the I/O cable, the terminating shoe is mounted on the special equipment.

The total length of the I/O cable is limited to 20 feet. The I/O cable connector pin assignments are shown in table 2-12. For a detailed description of the I/O system, see section 2 of the interface reference manual.

Table 2-12. I/O Cable Connector Pin Assignments

Line	Pin	Function
1	1	EB00-I
2	2	R
3	3	EB01-I
4	4	R
5	5	EB02-I
6	7	R
7	8	EB03-I
8	10	R
9	11	EB04-I
10	12	R
11	13	EB05-I
12	14	R
13	15	EB06-I
14	16	R
15	17	EB07-I
16	18	R
17	20	EB08-I
18	21	R
19	22	EB09-I
20	23	R
21	24	EB10-I
22	25	R
23	26	EB11-I
24	27	R
25	28	EB12-I
26	29	R

Line	Pin	Function
27	30	EB13-I
28	31	R
29	32	EB14-I
30	33	R
31	34	EB15-I
32	35	R
33	36	EB16-I
34	37	R
35	38	EB17-I
36	39	R
37	40	FRYX-I
38	41	R
39	42	DRYX-I
40	43	R
41	44	SERX-I
42	45	R
43	46	TPIX-I
44	47	R
45	48	TPOX-I
46	49	R
47	50	PR1X-I
48	51	R
49	52	PR2X-I
50	53	R
51	54	PR3X-I
52	55	R

Table 2-12. (Continued)

Line	Pin	Function
53	56	PR4X-I
54	57	R
55	58	SYRT-I
56	59	R
57	60	IUAX-I
58	62	R
59	63	IUCX-I
60	64	R
61	65	IURX-I
62	66	R
63	67	IUJX-I
64	70	R

Line	Pin	Function
65	71	
66	72	
67	73	
68	74	
69	75	
70	76	
71	77	
72	78	
73	79	
74	80	
75	82	GND

4.7 MEMORY SECTION

The memory section of the central processor consists of one to eight memory blocks each consisting of a stack assembly mounted between two DM103 matrix/decoder printed circuit cards plus associated control, driver and regulator cards. Only one memory block is contained in the main frame of the central processor. Within each memory block are two DM104 driver/switch cards containing L-register decoding and X and Y drive circuits, three DM119 data cards containing six bits each of sense and inhibit circuits, one DM120 regulator card to regulate the stack drive currents, and one DM106 timing and control card which generates the control pulses for DM104 and DM119 cards (see table 2-2). Each memory block is a basic 4096-word unit having the following characteristics:

Full-cycle time of 1.8 microseconds.
Half-cycle time of 1.35 microseconds.
Access time of 750 nanoseconds.
Random access.
Magnetic core, with four wire, 3-D memory.

Normal operation is full-cycle; either read/restore or clear/write. Half-cycle is used only in write operations and is required only with the DMA/I option.

The memory blocks share the L and W registers (see figure 2-2); only one memory block at a time is cycled. The memory blocks connect to the L and W buses and to four memory control lines. Each memory block has a unique start pulse allowing the central processor to select the memory block to be cycled.

4.7.1 Memory Address

The memory is addressed through the L bus. This is a 15-line (positive = true) bus the first 12 bits of which are used to directly address up to 4096 words in a memory block. The next two upper-order bits of the memory address word from the L register are transferred to the memory control logic of the central processor where they are decoded to determine which 4096-word memory block within the first 16K of memory is to be cycled. (Note: 16K is the largest memory available as a standard.) The decoded memory block address is transferred to the appropriate memory block as the memory start pulse (MSCn+).

4.7.2 Control Lines

In addition to the memory start pulse, three other control lines are used in the memory. These are the read-restore/clear-write, the full/half cycle and the data guard control lines.

The read-restore/clear-write control line enables selected operating functions of the memory to be performed.

The full/half cycle control line enables selected cycling of the operating sequence to be performed.

The data guard control line inhibits memory drive current, preventing the memory core stack from being disturbed. This control line can be activated in the following two ways:

Manually by the memory enable/disable switch (see 2.4.1).
Automatically by the power fail/restart optional module.

4.7.3 Word Transfer

Word transfer to and from the memory is accomplished through the W bus. This is a 16- or 18-line (ground = true) bus. Figure 2-12 shows a memory data electronics interface with a W-register flip-flop. On a read-restore cycle, the W register is cleared at the beginning of a memory cycle. The switch on the output of the sense amplifier is closed if a ONE is detected, causing the W-register flip-flop to be collector-set to the ONE state.

4.8 TYPICAL OPERATING SEQUENCES

There are three typical operating sequences:

Access operand in memory.
Store operand in memory.
Indirect operand access.

An understanding of these operating sequences will enable the technician to quickly understand the timing and wave forms of each individual instruction sequence shown in chapter 6. Variations to these operating sequences may occur which are dependent on the particular instruction being executed.

4.8.1 Access Operand in Memory

The access operand in memory is the simplest and most basic operating sequence. In this sequence, a single-word directly addressed operand is read from memory. This

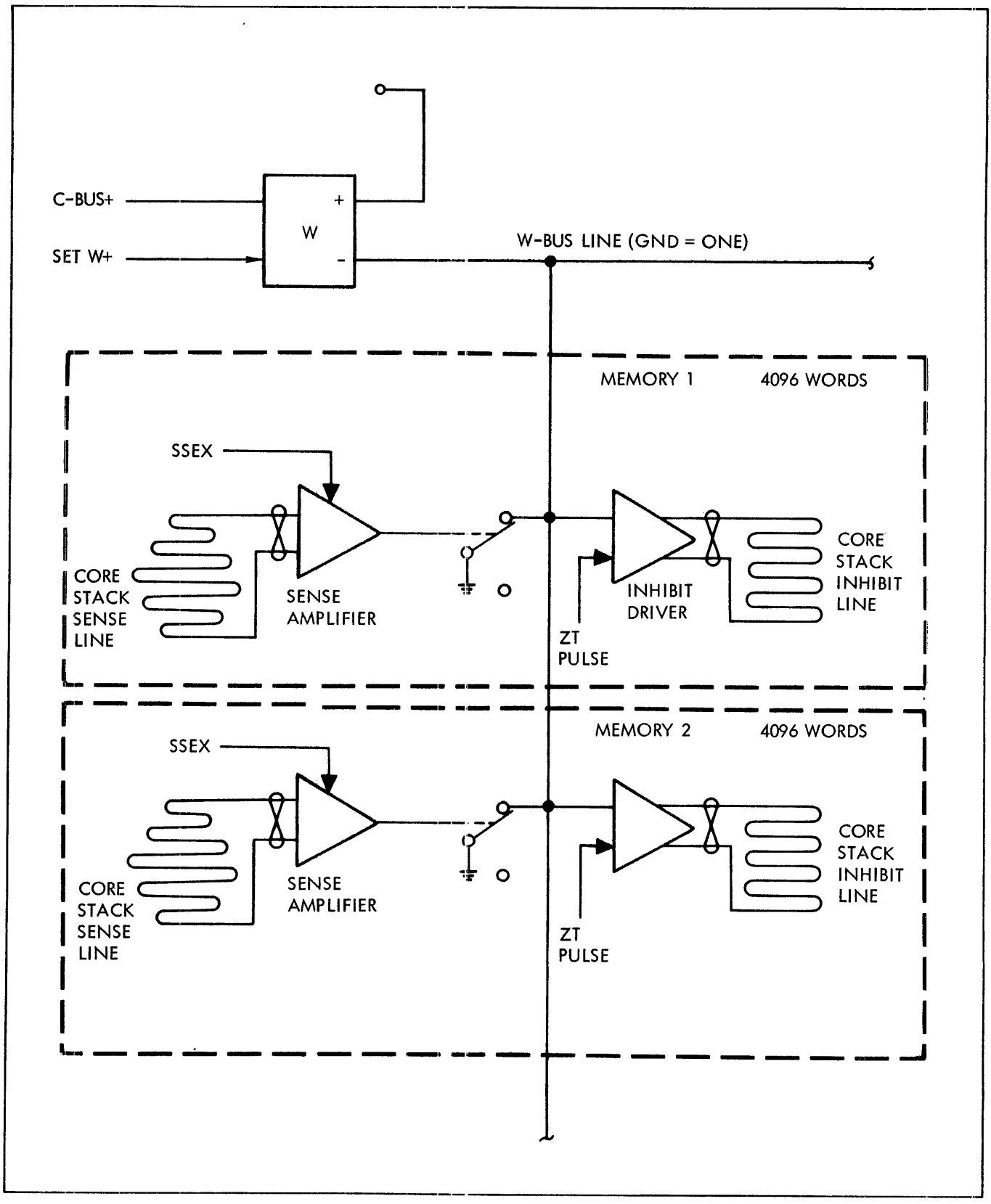


Figure 2-12. Memory and W-Register Interface

operating sequence is used for load, logic and arithmetic (except multiply and divide) instructions. The timing of the sub-operations of this sequence is illustrated in figure 2-13.

At time 0 (in microseconds), the instruction cycle (ICYX+) for the nth instruction is initiated. The n-1 instruction is being executed (IEPX+) while the current instruction (n) is being read from the memory. At time 0.9, n instruction is transferred to the U register. The instruction address phase (IAPX+) occurs while the n instruction is being restored in memory. The operand address is generated during IAPX+.

The operand cycle (OCYX+) is initiated at time 1.8 . After the operand has been read from memory and stored in the R register, the address of the next instruction (n+1) is generated (normally by adding 1 to the P register) and transferred to the memory L register. This sub-operation is performed while the operand is being restored in memory. ICYX+ for n+1 is then initiated at time 3.6 .

The operation to be performed upon the operand now contained in the R register occurs during the IEPX+ part of the ICYX+ for n+1. This operand operation could be an ADD instruction such as adding the operand value to the A register and storing the result in the A register or simply a transfer of the operand to one of the operational registers (LDA, LDB or LDX).

4.8.2 Store Operand in Memory

The store operand in memory (STA, STB or STX) sequence is essentially identical to that for accessing an operand except the addressed memory cell is cleared and the operand is written into it. The timing of the sub-operations of this sequence is illustrated in figure 2-14.

The nth instruction is accessed and the operand address generated during ICYX+ as before; execution of the n-1 instruction occurs during IEPX+ of the nth cycle as indicated. However, during the operand cycle (OCYX+), the operand is transferred to memory while the referenced cell is being cleared. During the last half of the cycle, the operand is stored into the cell just cleared. During this time, the address for the next instruction is generated. Note that there is no execution, as such, for this type of instruction (indicated by dashed lines) because the execution has already been accomplished, in effect, by the transfer and storage of the operand in memory.

4.8.3 Indirect Operand Access

The indirect operand access operating sequence involves indirectly accessing an operand in memory by a single-word instruction. In this case, an address cycle (ACYX+) is required to read the indirect address word from memory before OCYX+ can be initiated. The timing of the sub-operations of this sequence is illustrated in figure 2-15.

The sequence of sub-operations is illustrated in figure 2-15. During ICYX+, the nth instruction is read from memory and stored in the U Register as before. The previous instruction, n-1, is executed during IEPX+. During IAPX+, the location of the (indirect) address word is generated. This address word is read from memory and stored in the R register as indicated in the timing diagram. For the case illustrated, the address word accessed contains the address of the operand (otherwise, another address cycle would be initiated to access a second address word, and so on). The operand address is transferred to the memory L register during the last half of ACYX+ to locate the operand read out during the succeeding OCYX+.

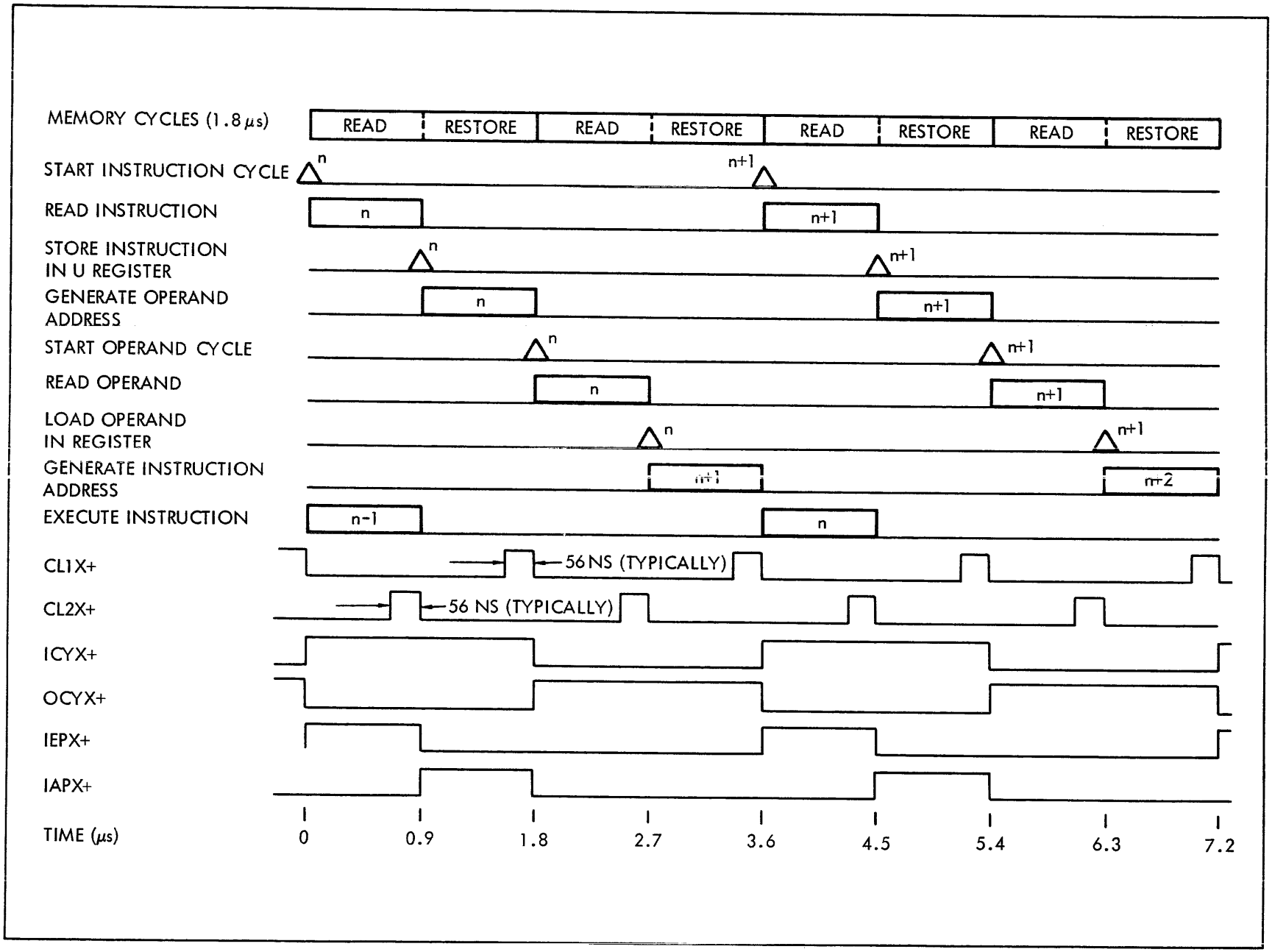


Figure 2-13. Sequence for Operand Access from Memory

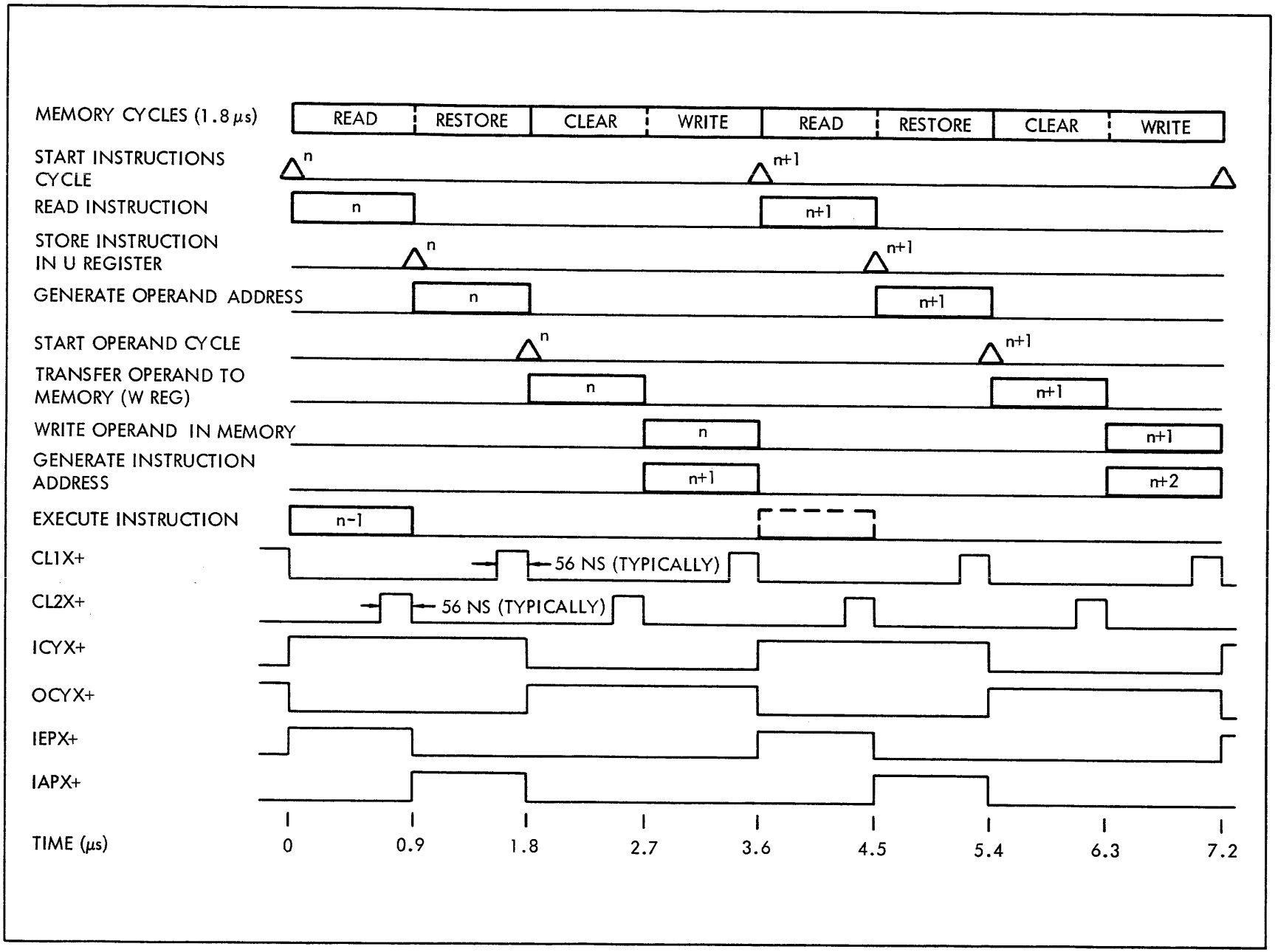


Figure 2-14. Sequence for Operand Storage in Memory

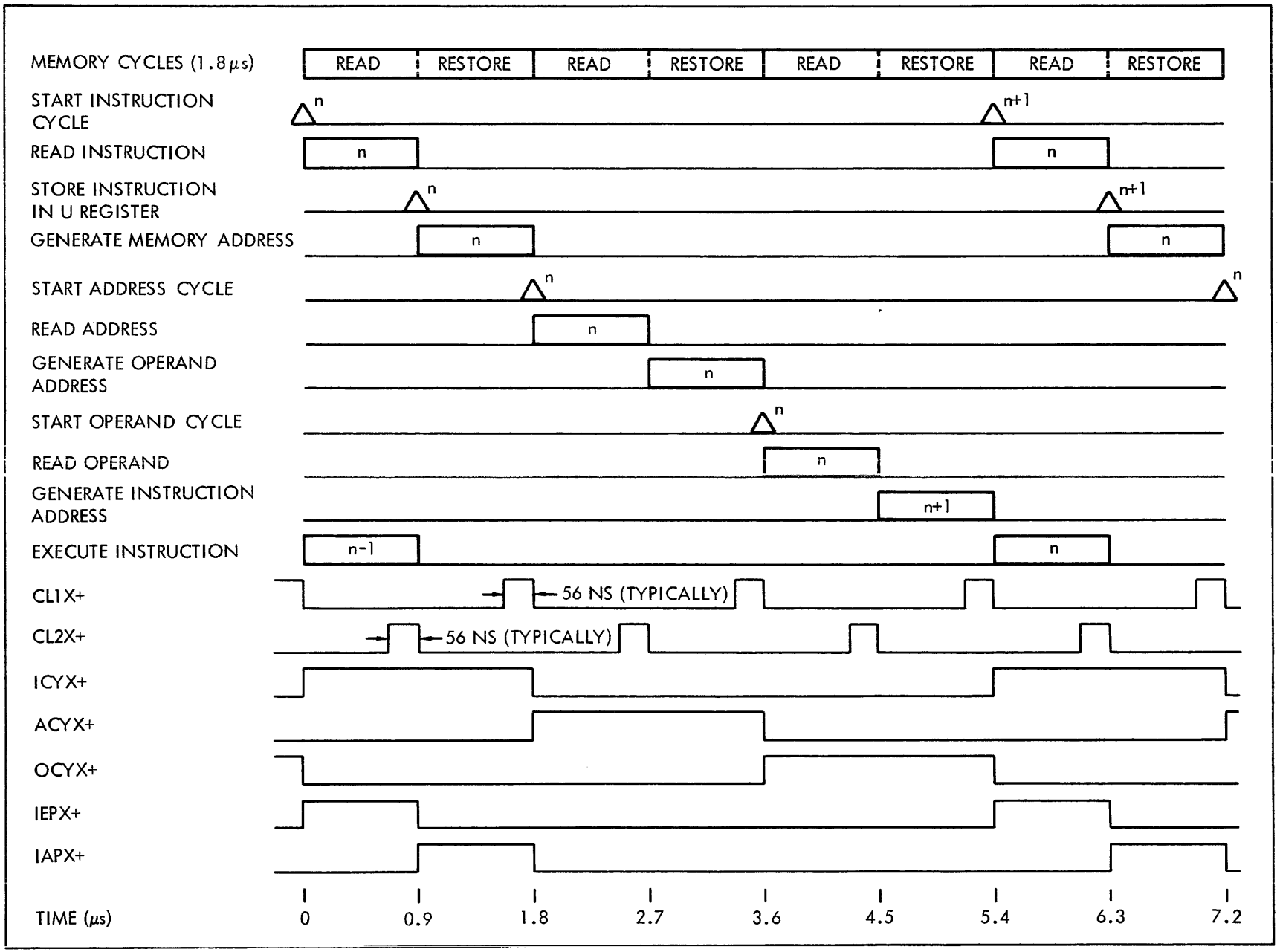


Figure 2-15. Sequence for Indirect Operand Access

The generation of the address for instruction n+1 and the execution of instruction are then performed as in the case for the simple operand access considered previously.

5.1 INTRODUCTION

This section describes maintenance and troubleshooting procedures. The reliability of the central processor will be considerably enhanced if specified environmental conditions are maintained and recommended maintenance procedures are followed.

Maintenance and troubleshooting of the DATA 620/i computer are simplified by the packaging of the central processor. Circuit cards are accessible from the rear of the central processor by swinging down the power supply chassis which is hinged to the rear of the main frame (see figure 2-3). The card connector pins and wiring are accessible from the front of the central processor by swinging out the console control-indicator panel.

To ensure efficient maintenance of the central processor, the user should:

Become thoroughly familiar with the computer by studying all published information furnished with the equipment.

Use the available maintenance aids.

Use adequate test equipment to assess system performance.

Follow the recommended maintenance procedures.

Use orderly and logical troubleshooting techniques.

Published reference information for all phases of DATA 620/i computer application is summarized in chapter 1.

CAUTION

When working underneath the computer mainframe or expansion frames, maintenance personnel should proceed with caution in the area of the fan blades. The computer mainframe contains a fan mounted in the area below circuit-card slots 5, 6, and 7. There may be as many as three fans mounted underneath the computer expansion frames.

5.2 TEST EQUIPMENT REQUIRED

Table 2-13, lists the test equipment and tools required to maintain the central processor. These items also satisfy all maintenance requirements for the peripheral device controllers.

Table 2-13
Test Equipment Required

Equipment	Description
Oscilloscope	Tektronix 453 or 547, or equal
Dual-Trace Preamplifier	Tektronix 1A2 or equal (Note: 453 requires no plug-in pre-amp.)
Multimeter	Simpson 260 or equal
Card Extender	DM 115 card
Card Puller	A shaped wire card pulling device
Wire Wrap Gun	Denver-Gardener 14R2 or equal
Soldering Iron	39 watt pencil type
Wire Stripper	Thermo-strip type
Assorted Hand Tools	Screwdrivers, spin-tight wrenches, long-nosed pliers, etc.

5.3 MAINTENANCE AIDS

The primary aids for maintaining the central processor are the diagnostic programs, connector pin assignment lists, logic diagrams and assembly drawings and the console controls and displays.

5.3.1 Diagnostic Programs

The diagnostics are programs which exercise the computer and its associated peripheral devices with sequences of instruction. The results of these sequences are checked against the proper responses. If an instruction or other operation is improperly executed, the program ends the sequence and causes printing of information indicating which instruction or operation failed. The technician may then repeat, continue or halt the diagnostic routine until the fault is isolated and corrected.

The diagnostics serve two essential purposes:

They verify whether or not the computer is properly operating.

They determine the specific area location of a detected malfunction.

The use of diagnostics and error outputs are described in chapter 7.

5.3.2 Integrated Circuit Terminals

Observation of electrical waveforms is essential for locating specific malfunctioning components. For monitoring waveforms, accessibility to integrated circuit terminals on the circuit board modules may be obtained by using a standard DATA 620/i board extender. The location of the integrated circuits is shown on the assembly drawings in volume 2 and integrated circuit terminal locations are shown on the logic drawings in volume 2.

5.3.3 Short Circuit Protection

Outputs of all standard logic circuits are internally protected against damage from short circuiting to other logic outputs or to ground; however, short circuiting the outputs to any supply voltage source will cause damage.

5.3.4 Console Controls and Displays

The console control-indicator panel shown in figure 2-3 provides the controls and displays required for operator communication with the computer. This communication is useful in detecting and locating malfunctions.

Individual functions of the console facilities are described in table 2-4. The following two controls are particularly useful for maintenance and troubleshooting:

STEP	Permits execution of a program sequence one instruction at a time. The central processor halts after each step execution, permitting the results to be observed.
REPEAT	Permits repeated execution of the instruction in the U register, in the step mode.

The console displays permit observation of the contents of the U, A, B, X and P registers in the step and repeat modes. The 16 (18) bit-setting switches permit setting and alteration of the individual bit positions in these registers.

5.4 ROUTINE MAINTENANCE

The central processor requires no routine maintenance. The core memory has three central potentiometers on the regulator module located in slot two of the main frame. These controls are adjusted and sealed at the factory and should not be changed without prior consultation with factory field-service personnel.

Routine maintenance procedures for peripheral electro-mechanical devices in the DATA 620/i input/output system are contained in the manufacturer's instruction manuals supplied with the equipment.

5.5 TROUBLESHOOTING

The speed and ease with which the computer technician may detect, locate and correct a malfunction and return the machine to proper operation is a measure of the efficiency of the DATA 620/i system. The central processor is designed electrically and mechanically to ease the tasks of maintenance and malfunction correction.

The time required to correct system malfunctions will depend upon the efficiency of the procedures used. Although various specified techniques may be applied, there is no real substitute for an ordered, logical analysis of the problem and isolation of the cause to the level of the replaceable component. Such an analysis can be based only upon knowledge of the equipment design. These trouble-shooting procedures first describe general techniques applicable to all operations, and then present specific procedures recommended for the central processor.

5.5.1 General Troubleshooting Techniques

The general steps in troubleshooting are shown in figure 2-16 and described in succeeding paragraphs.

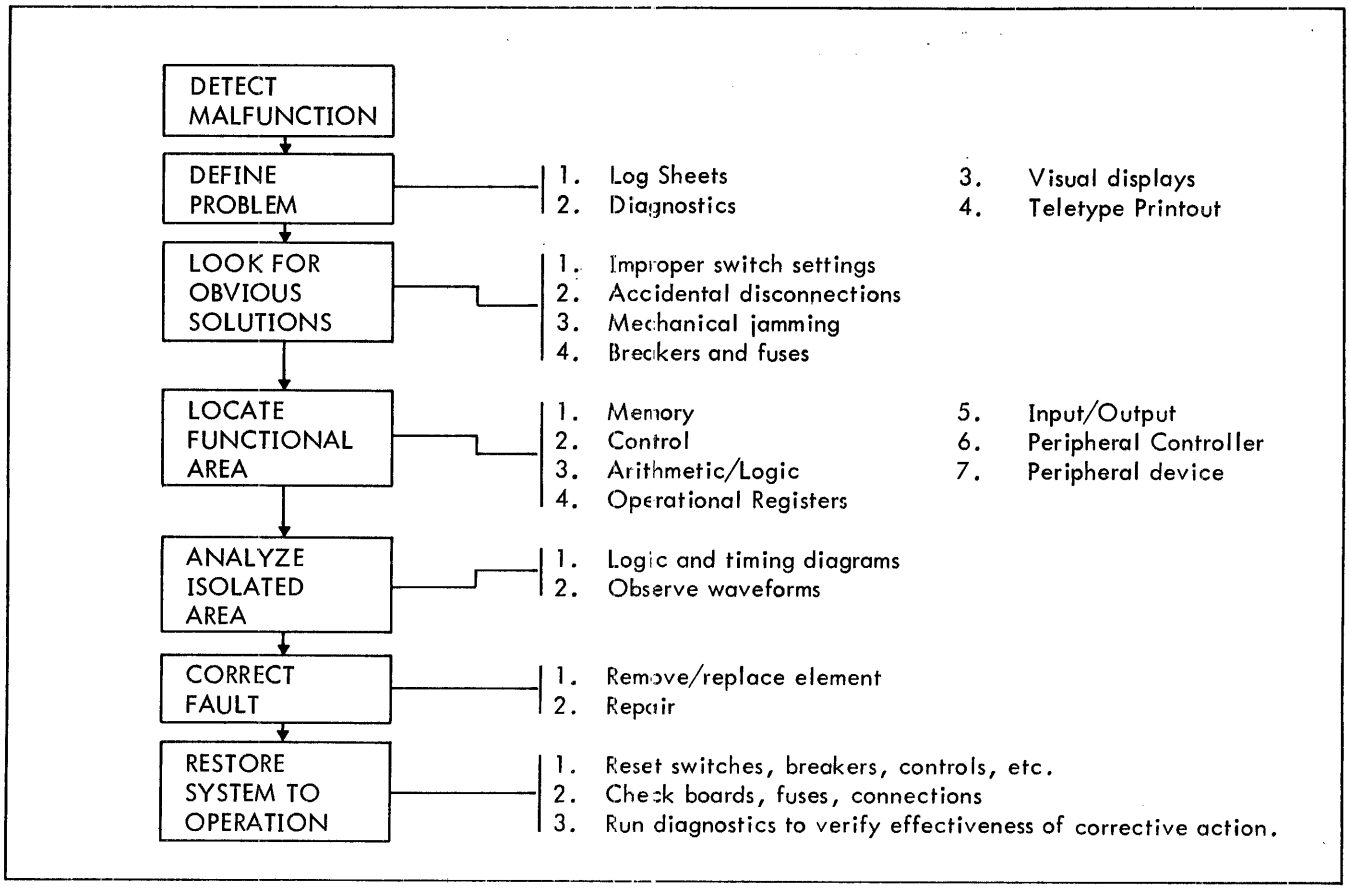


Figure 2-16. General Troubleshooting Steps

Define the Problem

Take time to thoroughly define the problem. For example, if the ADD instruction does not produce correct results, is the fault a function of the sign (plus or minus), of the carries or of some other element? Are the operational registers being properly loaded? Use the displays, connector pins and integrated circuit terminations for gathering the necessary data.

Look for Obvious Solutions

Make sure that a malfunction has actually occurred. Relate problems to recent events such as cleaning or servicing. Look for improperly set controls or test equipment and accidental disconnections of plugs, etc. Consider miscellaneous temporary failures, such as mechanical jamming of peripheral equipment. Remember, if it is necessary to remove the input power, the MEMORY ENABLE/DISABLE switch must be placed in the DISABLE position before turning off the power.

Isolate to a Functional Area

Isolate the fault to a functional area: that is; memory, control, arithmetic/logic, operational register, input/output, peripheral controller or peripheral device. The process of isolating the malfunctioning area is generally a straightforward process of eliminating the functional areas which are operating properly, when the faulty area is not immediately obvious.

Analyze the Area

When the fault has been isolated to a functional area, the rest of the system may generally be temporarily ignored. Use the logic and timing diagrams, and observe circuit waveforms to quickly isolate the problem to an individual replaceable element.

Correct the Fault

Replace the faulty circuit board or other element. Attempt to analyze the cause of the failure before restoring power to prevent the possibility of the failure occurring again.

Restore System to Normal Operation

When the system appears to be operating properly, make sure it is returned to normal operating conditions. If circuit boards have been unseated, be sure all are properly reseated in the connectors. Set all panel controls and place power on/off switch in the ON position. Finally, verify proper operation by running the diagnostic tests.

5.5.2 Specific Troubleshooting Procedures

The specific troubleshooting procedures outlined in the following paragraphs may be used when it has been determined that the computer is not operating properly. This is determined, typically, by various programmed maintenance routines which have been proved reliable. A typical failure in the central processor will produce failures in a large percentage of routines. For this reason, determining a computer failure is quite simple. Memory failures of a single bit or word are quite rare and will generally require special test procedures which may result in clearing the section of memory involved.

The following procedures assume a detailed knowledge of the operating characteristics of the central processor including familiarity with its internal organization.

Locating the Fault

The general characteristics of the failure will, in most cases, immediately indicate the failed section. The central processor contains the following four major sections:

a. Timing and decoding section

b. Arithmetic and register section

c. Memory section

d. I/O section

If the failure is catastrophic and all instructions fail, the cause is usually in the timing and decoding section.

Inability to correctly perform arithmetic operations or to correctly increment the P register is evidence of a failure in the arithmetic and register section.

Memory failures may be indicated by a repeated occurrence of the halt instruction or by completely random sequencing of instructions. I/O failures are restricted to I/O instructions and are associated only with the logic of the I/O device. An I/O failure is easily recognized by noting failures in various I/O routines which do not occur in internal routines.

A general procedure for using the console control-indicator panel to locate the basic problem area is presented in the following step outline:

a. Using the register select switches and the bit-setting switches on the console control-indicator panel, set ONE, into all bit positions of the A, B, X, P and U registers; then reset the registers to display ZERO in all bit positions by pressing the RESET switch. This operation checks the basic set and reset functions for all register flip-flop circuits in the central processor but it does not check the gating into these registers from the internal buses (see figure 2-2).

b. Set all ONEs into the A register. Single-step STA to location ZERO, then single-step LDA from location ZERO and check for agreement. Next, implement on Increment Memory and Replace instruction. Finally, increment a location that is all ZEROs. These operations check communication between the A register and memory.

c. Set the U register to increment the A register and place the central processor in the repeat mode by pressing the REPEAT switch. Then:

   Set the A register to all ONEs except the least significant bit (LSB). Press STEP switch twice and note results. On the second step, the A register contents should be changed to all ZEROs.

   Set the U register to all ZEROs and set the P register to all ONEs except the LSB. Press STEP switch twice and note results. On the second step, the P register contents should be changed to all ZEROs.

   This operation provides a major check of the arithmetic section of the central processor.

d. Set all ONEs into the A, B and X registers and complement each by using the appropriate register change instruction (see 4.5.10). This operation checks the A, B and X set functions and gates (STA, STB and STX), the A, B and X select functions and gates (SLA, SLB and SLX) and the operation of the shift (S) register.

e. Set all ONEs into memory location ZERO by setting all ONEs into the A register and storing. Then, AND memory location ZERO with the A register contents. The A register contents should remain all ONEs. Next, EXOR memory location ZERO with the A register contents. The A register contents should be changed to all ZEROs. Finally, OR memory location ZERO with the A register contents. The A register contents should be changed to all ONEs.

   These operations check the gates in the arithmetic unit of the central processor.

f. Set a repetive 101010...pattern into the A register. Shift the A register left one bit and note change. The pattern should be 010101...Shift left again and note change. The pattern should again be 101010...Follow this by shifting right one bit and note change The pattern should be 010101...Shift right again and note change. The original 101010...pattern should again be present in the A register display. This operation checks the shift gates in the arithmetic unit of the central processor.

g. Load all ONEs into the highest-numbered memory location. Set all ONEs into the P register and press the STEP switch. The U register contents should be all ONEs. Load all ZEROs into the highest-numbered memory location. Set all ONEs into the P register and press the STEP switch. The U register contents should now be all ZEROs because all ONEs were stored in memory location ZERO in step e.

h. To perform repeat operations in the run mode (normally only the first panel switch in the step mode controls repeat operations), connect a jumper between GND (pin 1) and pin 24 of ground plane row 18. Grounding this pin inhibits setting of the U register in the run mode.

CHAPTER 3
MEMORY

1.1 GENERAL

The DATA 620/i computer memory is a parallel, random-access, coincident-current, ferrite core memory used to store all instructions and data. The memory is composed of 4096-word increments and is expandable to 32,768 words. Each word contains 16 or 18 binary bits.

Full-cycle operations provided by the memory are clear/write and read/restore. Either full-cycle mode requires 1.8 microseconds. The clear/write cycle is used to load the memory. The clear operation prepares the addressed cores to accept the new word, and the write operation loads the information into the addressed cores. The read/restore cycle is used to read information from the memory. The read operation unloads the addressed word from the memory. Access times is 750 nanoseconds. Because reading the word destroys the information in the cores, a restore operation immediately reloads the word into the same core location.

The DATA 620/i memory has overcome the requirement for a stack heater and inconvenient warm-up period. The memory allows stack temperature to follow ambient temperature, but compensates by controlling drive currents with a simple servo. This servo senses stack temperature and automatically adjusts drive and inhibit currents to optimum values. Each DATA 620/i memory can be expanded up to the maximum of 32,768 words in increments of 4096 words. Each increment is a kit of matched core stack and circuit modules.

1.2 USE OF THIS CHAPTER

This chapter presents general description, theory of operation and maintenance information for the DATA 620/i core memory. Timing waveforms, logics, mnemonics and diagnostic routines are presented in chapters five through eight.

2.1 GENERAL

Each 4096-word memory module consists of the following elements:

a. A core stack mounted between two DM 103 matrix decoder circuit cards.

b. Two DM 104 driver/switch circuit cards which decode memory address (L register) bits and provide X and Y drive signals.

c. Three DM 119 data cards which sense data bits from the core stack and provide bit inhibit currents to the stack.

d. A DM 106 timing and control circuit card which generates all necessary control signals for the memory module.

e. A DM 120 regulator circuit card which controls drive currents into the stack. This card includes temperature compensating circuits for the regulators.

Each circuit card in a module is 7-3/4 inches by 12 inches and plugs into a 122-pin printed circuit socket.

Each module has unique operating characteristics, and must be considered as a kit with matched circuit cards. A circuit card from a module should not be replaced or exchanged for a similar card without having the module readjusted.

2.2 INSTALLATION

The first memory module of a DATA 620/i computer mounts in card slots 1 through 11 and 15 of the main frame. Additional modules mount in peripheral expansion chassis. Up to two 4096-word memory modules may be mounted in an expansion chassis, which requires only 10-$\frac{1}{2}$ inches of space in a standard 19-inch rack.

Memory modules interface with the L and W buses of the central processor to obtain address and data words. Control signals governing the mode of operation and selection of each module are provided by memory control logic in the central processor.

For installation of the memory module in the main frame, all data and control signals are prewired onto the printed circuit connectors. To install memory modules in expansion chassis, the chassis must be ordered with back planes wired for the memory.

The power supply for the DATA 620/i main frame can drive two memory modules in addition to the central processor. To power additional memory modules, additional power supplies must be ordered.

3.1 GENERAL

This section presents information on the magnetic core storage technique used in the DATA 620/i memory, the addressing technique used, and descriptions of the circuit cards used in a memory module. A block diagram of the memory is shown in figure 3-1.

3.2 MAGNETIC CORE STORAGE

3.2.1 Magnetic Core Operation

The basic information storage element of the DATA 620/i memory is the magnetic core.

The magnetic core is a toroid of ferrite that can be magnitized in one of two discrete directions representing the presence or absence of a binary bit. The core is magnetized by current passing through the core. Total current must reach a certain minimum strength before the core becomes magnetized. The direction of current flow through the core determines the direction of magnetization.

The two possible directions of current flow are called read and write.

The 620/i memory uses the coincident current technique to magnetize cores. Two perpendicular wires called X drive and Y drive pass through each core. During memory operations, the current on any drive wire is approximately one half of the current necessary to magnetize a core. Because of the orientation of the cores and wires in a plane, only the core at the intersection of two activated drive wires becomes magnetized. For simple analysis, a three core by three core matrix is shown in figure 3-2. The figure indicates the total driving current received by each core when wires X2 and Y2 are activated. Only the center core is magnetized since it is the only one that receives the full driving current, I.

3.2.2 Magnetic Core Stack

Magnetic cores are arranged in planes having four groups of 4096 cores each. Each group of 4096 cores is a square array, 64 rows by 64 columns, used to store one bit of 4096 words. The DATA 620/i memory uses 16- or 18-bit words, requiring four or five core planes. When five core planes are used, two quadrants of the fifth plane are spare. The required number of planes is called a stack and is bolted to matrix decoder circuit cards to form a plug-in module.

3.2.3 Memory Core Control Wires

Through each core in a stack pass three control wires and a sense wire as shown in figure 3-3. The control wires change the state of core magnetization. These wires include:

a. An X-drive wire that passes through all the cores in the same row. The value of the current on this wire may be zero or one half of the current required to change the state of magnetization of a core. Current may be in the read or write direction.

b. A Y-drive wire that passes through all the cores in the same column. The value of the current on this wire may be zero or one half of the current required to change the state of magnetization of a core. Current may be in the read or write direction.

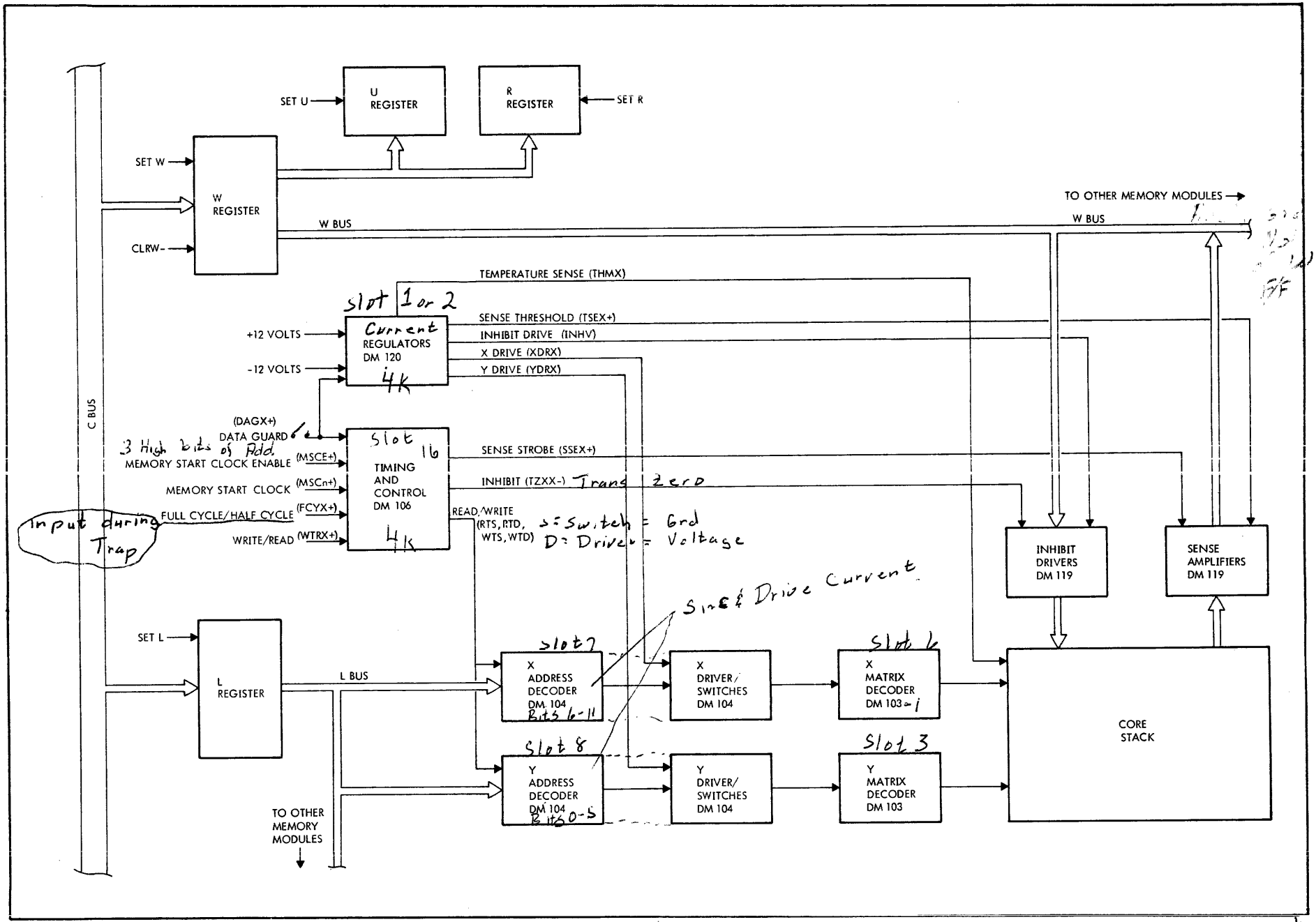


Figure 3-1. DATA 620/i Core Memory, Block Diagram

Appx 375 Mils = ½ current

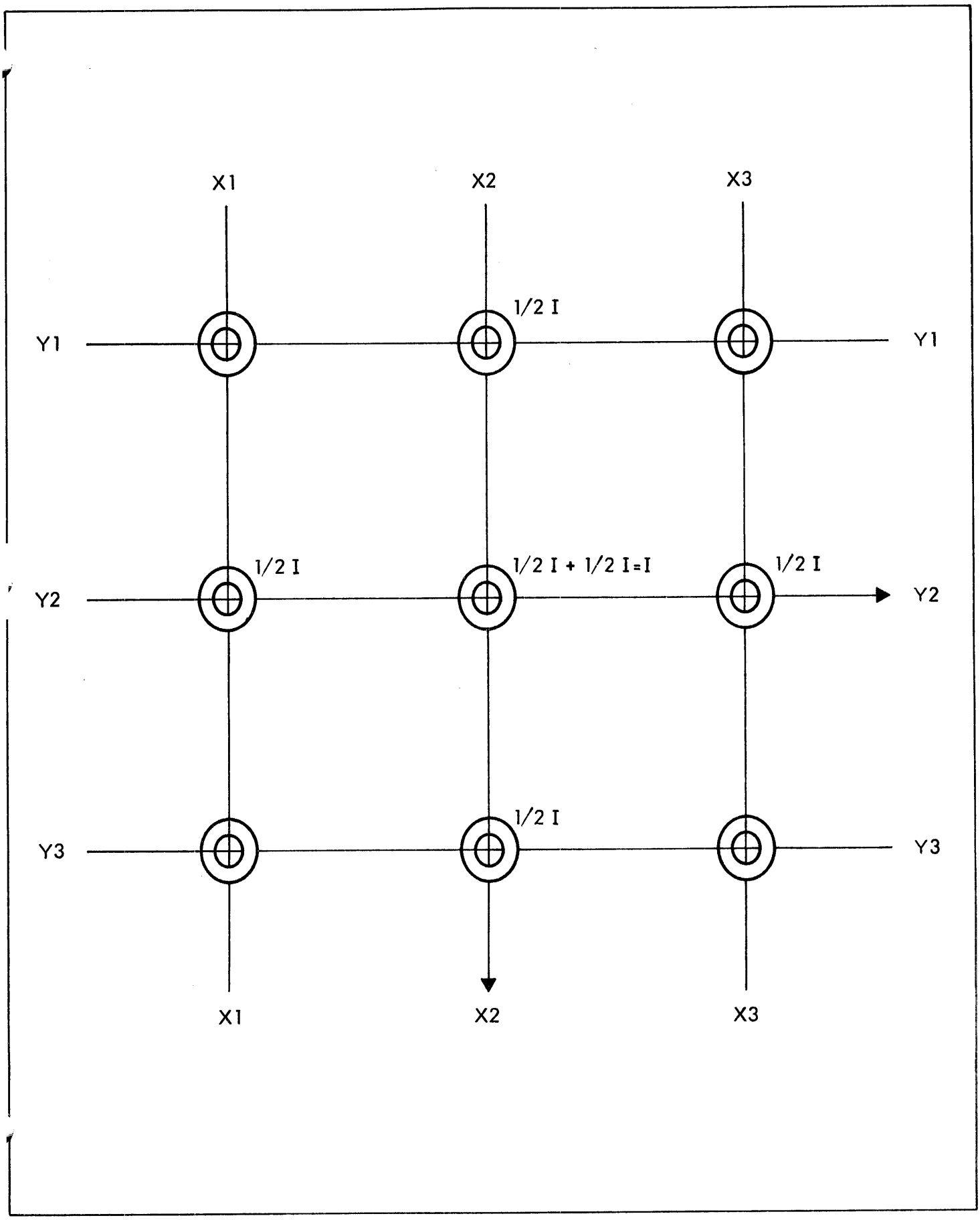


Figure 3-2. Three Core By Three Core Matrix

c. An inhibit wire that passes through all cores in one 4096-core matrix. The value of the current on this wire may be zero or one half of the current required to change the state of magnetization of a core. Current on this wire always opposes X-drive write current.

The sense wire passes through all cores in one 4096-core matrix, but does not control the cores. When any core in a matrix experiences a flux reversal, a voltage is induced in the sense wire. The wire is passed through the matrix in a special orientation to reduce the effect of voltages induced by cores which have not been addressed. These undesireable voltages are called sense noise and cannot be entirely eliminated. The ratio of flux-reversal induced voltage to sense noise is called the signal-to-noise ratio and is a measure of memory margins. The sense wire is interrogated only during read operations.

3.2.4 Memory Cycles

All memory operations include a read/clear cycle, a write/restore cycle, or both. During a read/clear cycle, the X and Y drive wires of an addressed word are activated (read current) to magnetize the cores to a binary ZERO state. If an addressed core already contains a ZERO, no voltage is induced in the associated sense wire. If an addressed core contains a ONE, a voltage is induced in the associated sense wire as the core switches to ZERO. The sense voltage is interrogated at the proper time and amplified to provide a memory read bit. This sequence is a read cycle. A clear cycle is similar, except that the sense wire is not interrogated.

During a write/restore cycle, the X and Y drive wires of an addressed word are activated (write current) to magnetize the cores to a binary ONE state. If an addressed core must remain ZERO, the associated inhibit wire is activated. Inhibit current cancels X-drive current, preventing the core from switching. The addressed cores are assumed to contain ZEROs before the write cycle. Inhibit currents are generated based on the bits of the word to be stored.

If the word to be stored has been obtained from the preceeding read cycle, the sequence described is a restore cycle. If the word to be stored is from outside the memory, the sequence is a write cycle.

3.3 ADDRESSING

In the DATA 620/ computer, the L register holds the address of the location to be accessed. The L register stores 16 bits, 12 of which are transferred to every memory module via the L bus. These 12 bits are decoded to directly address one of 4096 words in a memory module. The particular module containing the addressed word is selected by a memory start clock from the central processor. Up to eight memory start clocks can be provided and are generated by decoding of the higher order bits of the L register.

3.3.1 Memory Start Clocks

The eight memory start clocks that can be generated control up to 32,768 words of memory. Only one clock is true at any time, enabling one 4096-word module.

Four start clocks are generated in the timing and control section of the central processor. These are generated by decoding bits 12 and 13 of the L register, as described in chapter 2 of this manual. The remaining start clocks are produced by an auxiliary clock decoding circuit card used for memory expansion above 16,384 words.

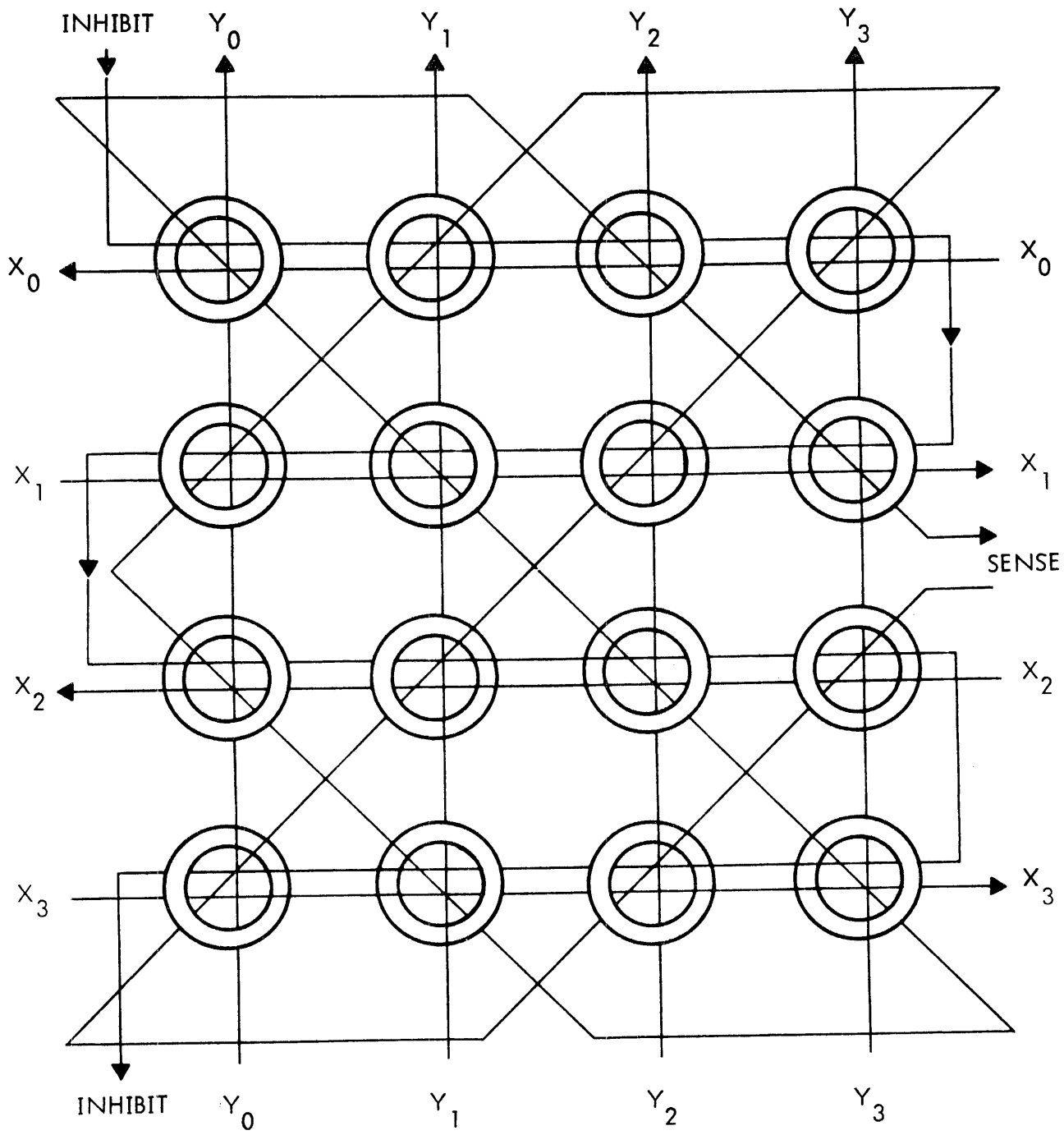


Figure 3-3. Typical Core Plane Wiring

3.3.2 Address Decoding

The 12 L-register address bits to each memory module are decoded in four groups of three bits each. Bits 00 through 05 select one of 64 Y-drive lines, while bits 06 through 11 select one of 64 X-drive lines. The word at the intersection of the X- and Y-drive lines is addressed.

Decoding circuits for X and Y drive are identical. Three of the six L-register bits to be decoded are applied to eight gates. Each gate detects one of the possible combinations of the three applied bits. The output of each gate controls a driver/switch circuit. Each driver/switch circuit can act as a source of stack drive current or a sink for current, depending on whether a read or write operation is required. The outputs of the eight driver/switch circuits are applied to one side of a square array (8 x 8) of decoding diodes and transformers providing 64 drive wires to the core stack. Also applied to the diode decoder array are the outputs of eight driver/switch circuits controlled by the remaining three L-register bits. Each diode decoder is located at the junction of perpendicular pairs of driver/switch outputs.

Each diode decoder is connected so that the perpendicular driver-output/switch-input pair selected by the decoded L-register bits causes current to flow into the core stack, as shown in figure 3-4. For any given L-register bit combination, only two drive lines are energized; one X and one Y.

The flow of current through a drive line may be in a read or write direction. This is controlled by the timing and control card as specified by the required mode of operation.

3.4 CIRCUIT CARDS

There are five circuit card types associated with the memory. These are:

a. Driver/switch.

b. Matrix decoder.

c. Data card.

d. Timing and control.

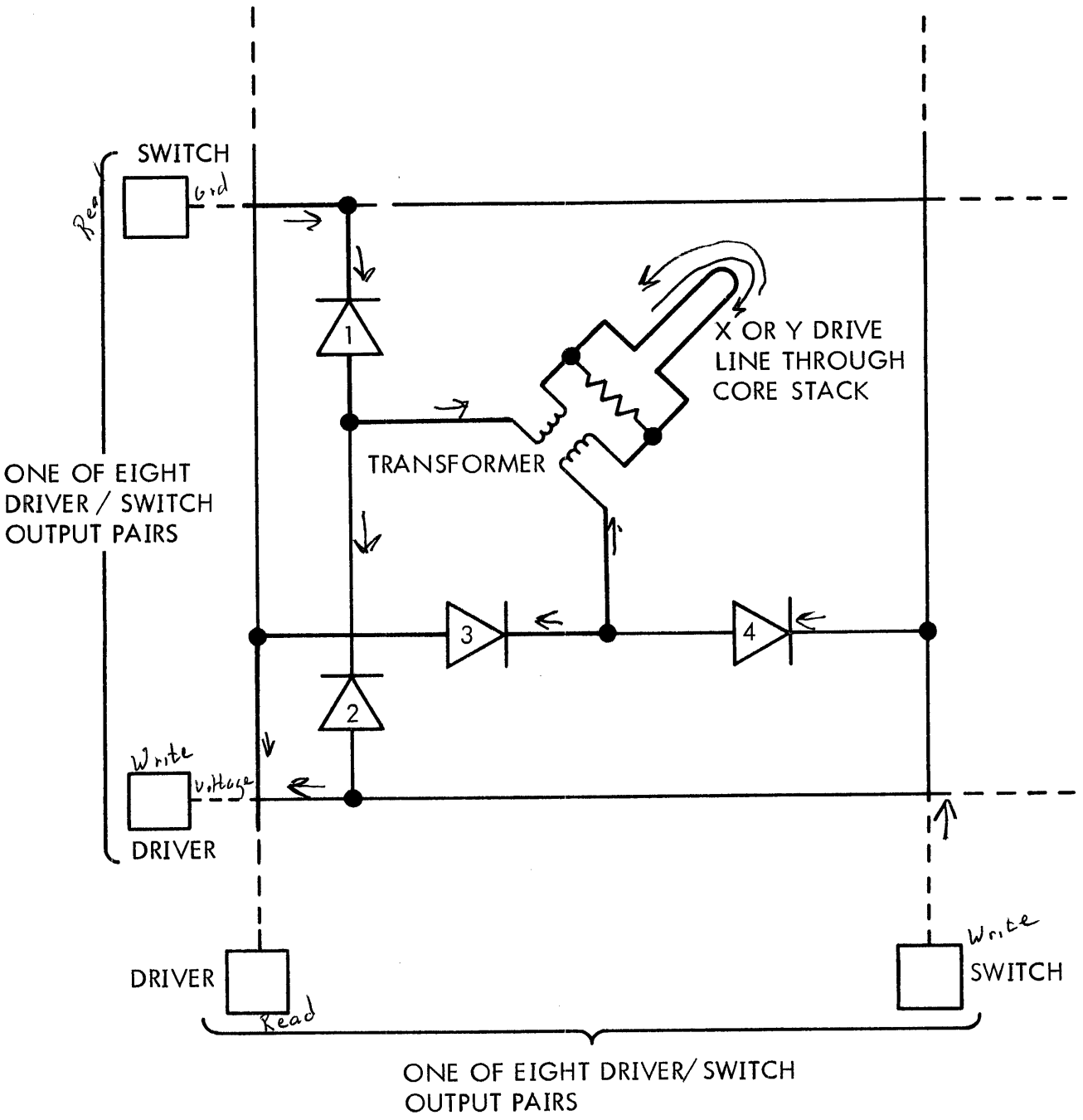
e. Memory regulator.

The core stack is mounted between two matrix decoder cards.

3.4.1 Driver/Switch Card

This card (DM104) decodes six L-register address bits to provide 16 pairs of driver/switch outputs to the matrix decoder. Either the driver or switch circuit is activated by an associated read or write timing signal. Whether a switch or driver is activated by the read or write signal depends on the L-register bits decoded. For L-register bits 00, 01, 02, 06, 07 and 08, the driver circuits are activated by a read command, while the switch circuits are activated by a write command. For L-register bits 03, 04, 05, 09, 10 and 11, the driver circuits are activated by a write command, while the switch circuits are activated by a read command. This arrangement guarantees read current to be in phase with inhibit current.

When a driver circuit is activated, X- or Y-drive current from the memory regulator is applied to the matrix decoder through the driver. The current seeks to find a path through the matrix decoder to an activated switch circuit. The switch circuit provides a sink for drive current.



HEAVY LINE SHOWS PATH OF CURRENT DURING A READ OR WRITE OPERATION.
CURRENT FLOWS THROUGH DIODES 2 AND 4 DURING ALTERNATE OPERATION

Figure 3-4 Typical Diode Decoder With Transformer

3.4.2 Matrix Decoder Card

This card (DM103) accepts 16 pairs of driver/switch lines from the DM104 card. The lines are arranged in an eight by eight matrix with 64 identical diode decoders.

Driver/switch lines to each side of the matrix are provided by separate groups of L-register decoding circuits. When a driver line is activated in one row of the matrix, a switch line is always activated in one column. Current provided by a driver is directed by diodes through a transformer, into the core stack, back through the transformer and to the activated switch (see figure 3-4).

3.4.3 Data Card

This card (DM119) contains six sense amplifiers and six inhibit drivers. Each amplifier accepts a sense line from a 4096-core matrix of the stack, amplifies voltage signals on the wire and provides a sense control signal to an associated inhibit driver and a bit of the W register. The amplifier can detect positive or negative (bipolar) signals from the stack and is enabled by a strobe signal (SSEX). The strobe occurs at the proper time in a read memory cycle. The strobe prevents amplified noise from providing erroneous signals to the inhibit driver and W register. The threshold (trigger) level of the amplifier is determined by a voltage from the memory regulator.

Each inhibit driver accepts a bit signal from an associated sense amplifier or W-register stage and provides an inhibit pulse to a 4096-core matrix of the stack. The driver is enabled (by $\overline{\text{TZXX}}$) at write time.

During a clear/write memory operation, the W-register bit to an inhibit driver determines whether an inhibit pulse is generated (inhibit is generated for a ZERO bit); the sense signal to the driver is not interrogated. During a read/restore operation, the sense signal determines whether an inhibit pulse is generated. The sense amplifier outputs and the W-register stages interface so that the sense signals always set the state of corresponding W-register stages. In this way, bits of a word read from any location are restored without change and are available to the central processor in the W register.

3.4.4 Timing and Control Card

This card (DM106) accepts a memory start clock and operational control signals from the central processor, and provides all required control signals to perform the specified operation. Precise timing of control signals generated on this card is accomplished by a tapped delay line. When a memory start clock is received, a pulse is sent into the delay line. At precise intervals along the line, the pulse is tapped off. Selected tap signals are combined with operational control signals to generate read or write signals for driver/switch circuits, an inhibit timing signal and a sense strobe. The signals generated are for one half cycle of a memory operation. During a full-cycle operation, the last tap of the delay line initiates a second delay-line start pulse to time the second half cycle of a full-cycle memory operation. The relationship between typical timing signals on the DM106 card is shown in figure 3-5.

Operational signals from the central processor include memory start clock, data guard, full cycle and write. Data guard is an optional signal that inhibits the memory start clock, thereby preventing accidental alteration of memory contents. A detailed description of this signal is included in the reference manual for the data guard option.

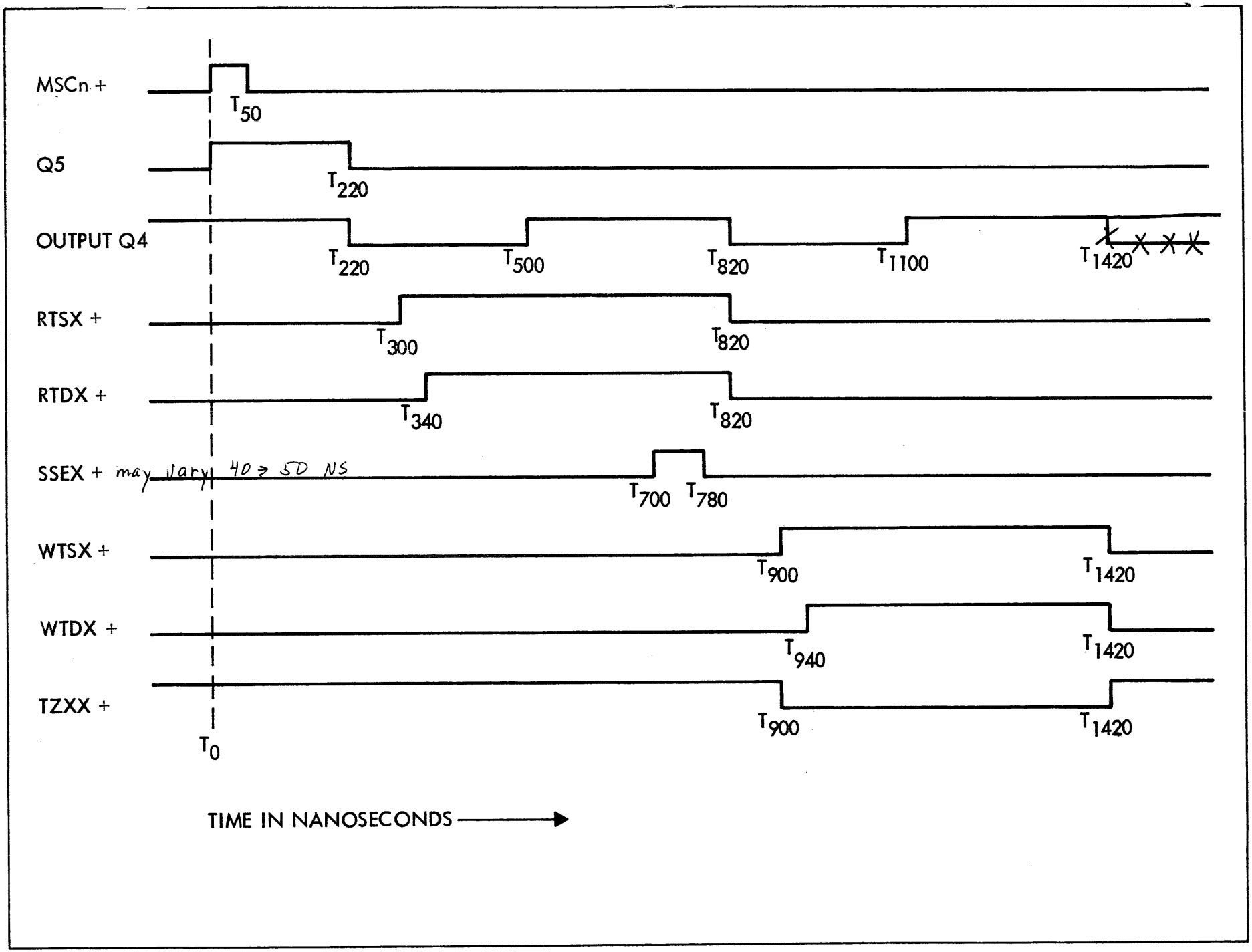


Figure 3-5 Typical Waveforms, Timing and Control Card DM 106

The full-cycle signal controls a flip-flop on the timing and control card, indicating whether a full-cycle or half-cycle memory operation is to be performed. In the field, only full-cycle operations are performed. The full-cycle output of the flip-flop is applied to a trigger flip-flop that forces a read operation to be performed on the first half cycle. Part of the way through the half cycle, the triggered flip-flop is switched so that on the second half cycle, a write operation is performed.

The write signal from the central processor controls a flip-flop on the timing and control card, indicating whether a read/restore or clear/write operation is to be performed. The only difference between the operations is that during the first half cycle, sense strobe is generated for read/restore, but is inhibited for clear/write. The sense strobe causes sensed data to be set into the W register. On the second half cycle, the bits of the W register generate inhibit signals, restoring the accessed word or writing the word previously loaded into the W register by the central processor.

3.4.5 Memory Regulator Card

This card (DM120) accepts ±12 volt power from the main frame and a thermistor temperature signal from the core stack, and generates four closely regulated currents and voltages. These are:

a. X current.

b. Y current.

c. Inhibit voltage.

d. Sense threshold voltage.

Although the circuits for the signals are somewhat different, the same basic principles are used. Each regulator includes a differential amplifier followed by a series regulator. Feedback is provided from the regulator to the amplifier so that the regulator output closely follows the reference input to the differential amplifier. The same reference input is used for all of the amplifiers. This input is generated by a constant current source applied to a voltage divider network.

The divider includes a fixed resistor and a thermistor that senses stack temperature. As stack temperature varies, the resistance of the thermistor varies. This changes the reference input to the differential amplifiers. The result is that the outputs of the regulator circuits vary in a direction to optimize the electrical operating point of the memory. This technique allows considerable variance of memory temperature without loss of operating reliability.

3.5 LOADER PROTECT FEATURE

The loader protect feature prevents writing into memory locations which are used by the bootstrap and binary load/dump routines. These locations are normally the last 400 octal addresses of the core memory. The loader protect circuit is located on the timing and control card (DM 106). The card contains jumper pads for the three most significant address terms (L12X+, L13X+, and L14X). Jumpers are installed at the factory or in the field when the system memory capacity exceeds 4k.

A toggle switch* located at the rear of the timing and control card is used to enable the loader protect circuit. When the switch is in the disable position, all memory locations are available for storage. However, when the switch is in the enable position, the loader protect feature prevents writing into memory the locations used by the bootstrap and binary load/dump routines. This is described in the following two paragraphs and illustrated in the timing waveforms in figure 3-6.

3.5.1 Store or Increment Memory Instructions

When executing the store or increment memory instructions with the loader protect circuit enabled, if the memory location to be stored into is the bootstrap and binary load/dump area, the following events occur. The Read/Write command (WRTX+) is forced to the low state. When the Set R Register signal (SETR+) changes to a high state, the SQP2 signal is at a low state and causes the computer to go into a step operation by generating the Stop control signal (SØPX+).

3.5.2 Trap In Operations

When executing a trap in request with the loader protect circuit enabled, if the memory address provided by the trapping device is in the bootstrap and binary load/dump area, the following events occur. The Read/Write command (WRTX+) and the Memory Start Pulse (MSPX+) are inhibited. When the Set W Register signal (STW1-) changes to a low state, the SQP2 signal is at a low state and causes the computer to go into a step operation by generating the Stop control signal (SØPX+).

*Later 620/i versions have the toggle switch located behind the control panel in the lower left corner.

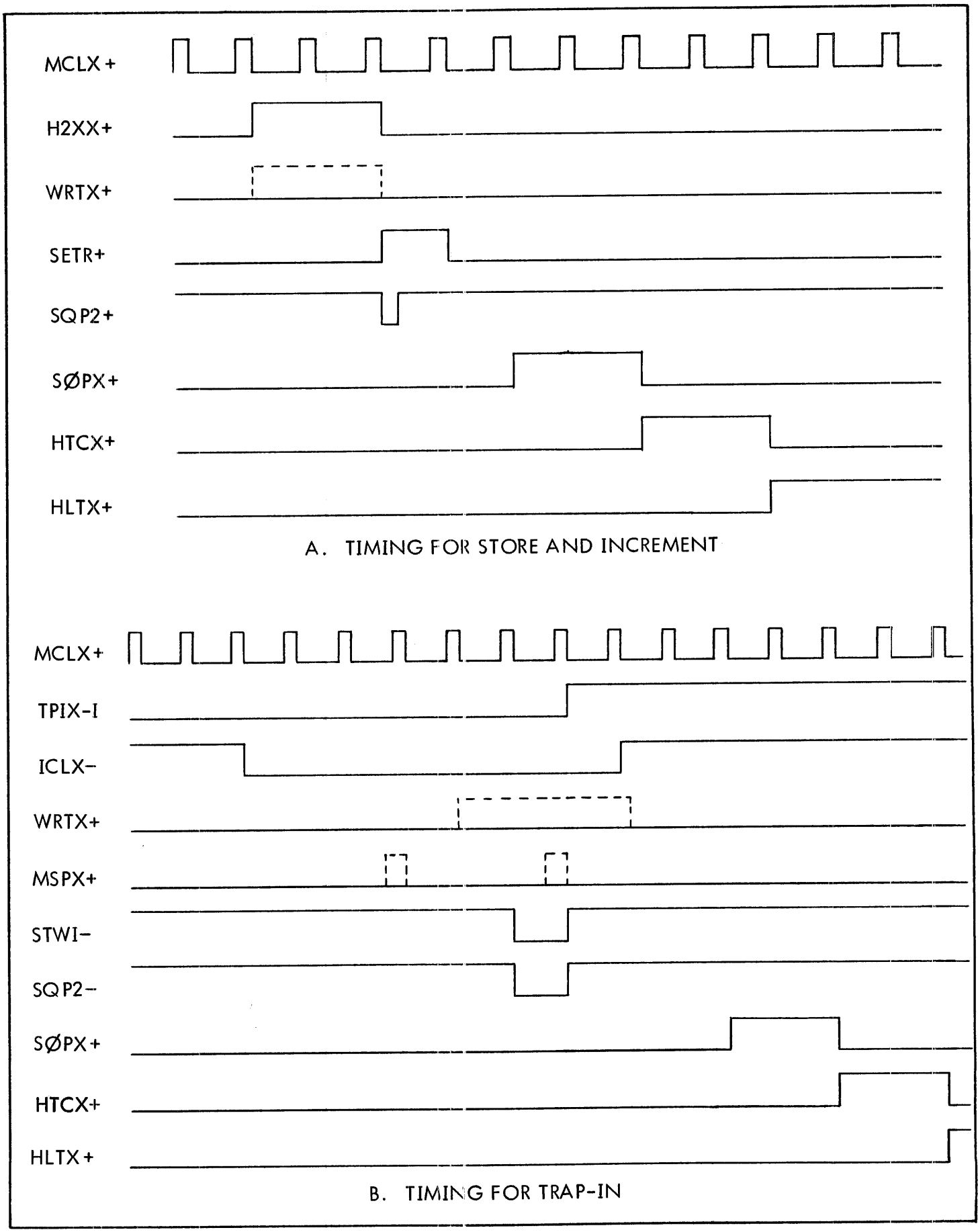


Figure 3-6. Loader Protect Feature Timing

4.1 GENERAL

This section contains instructions for maintaining and troubleshooting the DATA 620/i memory, including procedures for routine preventive maintenance and general procedures for troubleshooting.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance procedures for the memory consist primarily of inspection and cleaning. When operating schedules permit, check the following:

a. Check memory input/output connectors for proper seating.

b. Remove dust and dirt from interior of memory, using a stream of low-velocity air. (Use extreme care when cleaning in the area of the core stack).

c. Check for proper power supply voltages (-12v and +12v). Check and adjust power supply voltages using a voltmeter accurate to within two percent.

4.3 REMOVING AND INSTALLING CIRCUIT CARDS

To remove a card, pull gently on the desired card or use a card extractor. To install a card, insert the card into the proper channel and push gently until it seats properly in the connector.

CAUTION

Never remove or install any module, or remove or connect any connector, while power is applied to the memory.

4.4 CALIBRATION AND ADJUSTMENT

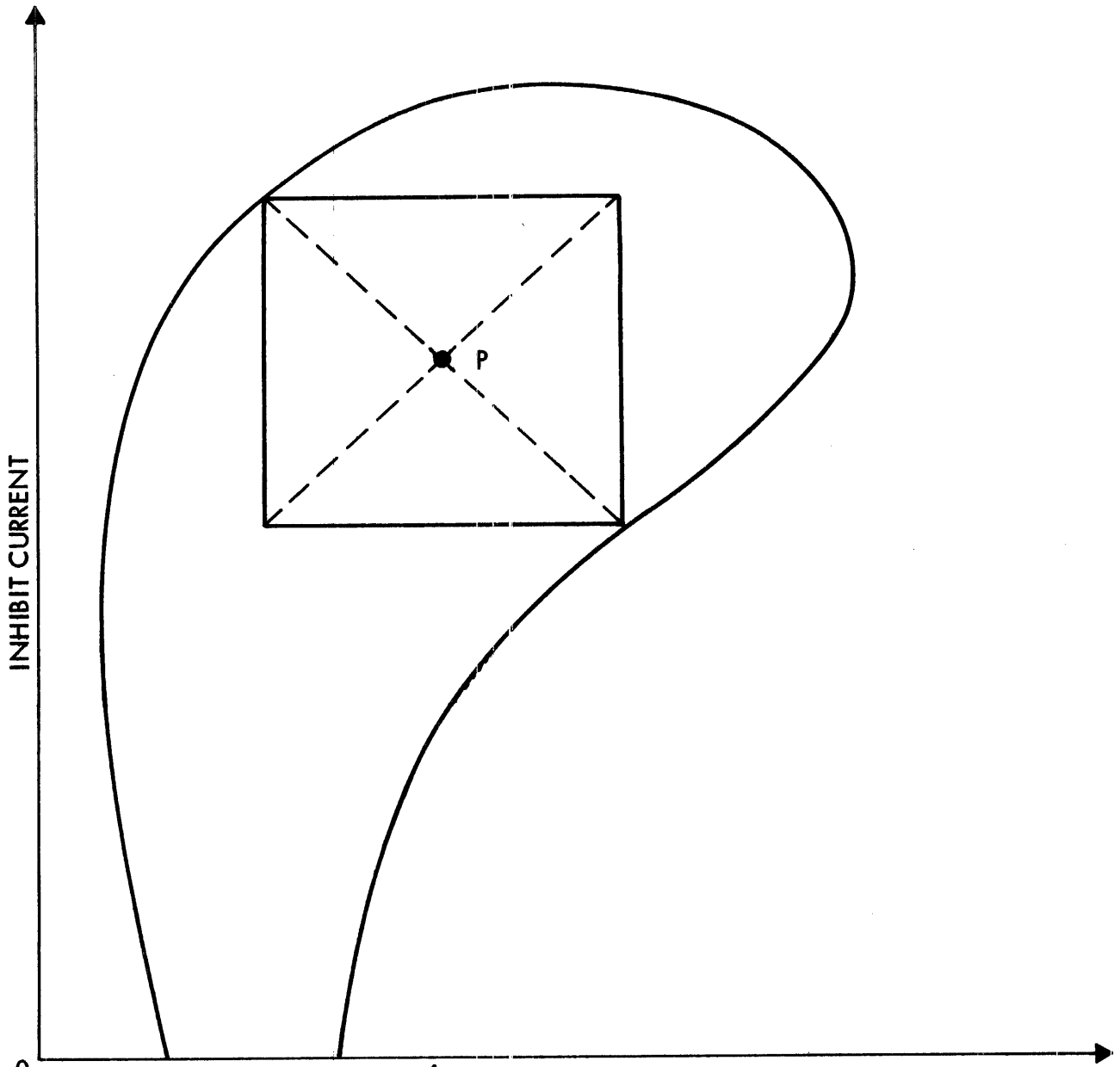
The circuits of the memory are carefully adjusted at the factory and must be considered as a matched set. Adjustment of the memory circuits should not be attempted in the field.

4.4.1 Schmoo Diagrams

To assure the level of performance of a memory, "schmoo" diagrams are generated at the factory. These diagrams indicate the extreme operating points of a memory stack and the actual adjustment point of the memory electronics.

The schmoo diagram is plotted by setting the X and Y drive currents to a fixed value and varying the inhibit current until a memory failure is produced. Various failure points of inhibit current versus X and Y drive current show the range of operation of the core stack. As shown in figure 3-7, the optimum operating point, P, for the module may be determined graphically.

The schmoo diagrams provided with each module are valuable troubleshooting aids. By checking actual operating points of the memory electronics and comparing these points with the schmoo diagrams, the degree of adjustment can be determined.



P IS OPTIMUM OPERATING POINT

Figure 3-7 Typical Schmoo Diagram

CHAPTER 4
TELETYPE CONTROLLER

SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

Model 620/i-06-A Teletype Controller (TC) controls the command and information transfer between the DATA 620/i computer and the factory modified teletype models 33 and 35.

The TC (or DM 113 card) is an optional component of the DATA 620/i computer. When used, it is normally installed in slot 24 of the computer mainframe and controlled directly by the central processor. However, the TC can also be controlled by the buffer interlace controller (BIC) option, DM 126, (when available in a given computer) or it can be controlled indirectly on the I/O bus by the computer using a special buffer card. In either case a special I/O expansion frame is required.

Each TC can control one teletype. If additional teletypes are required, the additional TCs are installed in a special expansion frame and controlled by a BIC or indirectly by the computer as described above.

1.2 SCOPE

This section contains description material, specifications, and the theory of operation, and includes instructions for installation, operation and maintenance of the TC. Operation is described with DATA 620/i control, and with the BIC feature. Asynchronous transmission is also described.

The TC specifications are listed in table 4-1. A simplified block diagram of the TC is shown in figure 4-1. The TC organization is shown in figure 4-2. For general teletype information, refer to the vendor manuals supplied with the teletype unit.

Table 4-1. Teletype Controller Specifications

Specification	Description
General:	The TC controls command and data transfer between the central processor and factory-modified teletype models 33 and 35.
Peripheral devices and cables:	Teletype models are 33-ASR, 35-ASR, and 35-KSR (keyboard send/receive). A cable is included with each unit.
Organization:	The TC contains the send and receive registers, and the timing control circuitry for simultaneous two-way transmission.
Speeds:	TC operation is controlled by teletype speed. Rate is 10 characters per second (cps) maximum - 100 milliseconds per character - at either random or sustained rate.
Packaging and environment:	One TC per DM 113 card. The TC shares the power and environment of the mainframe or expansion frame in which it is installed.
Modes:	Input from keyboard or paper tape (ASR only). Output to typewriter or paper tape (ASR only).
Device address:	Normally is 01.
Sense response:	Two standard sense responses: Ready to read (input) and ready to write (output).

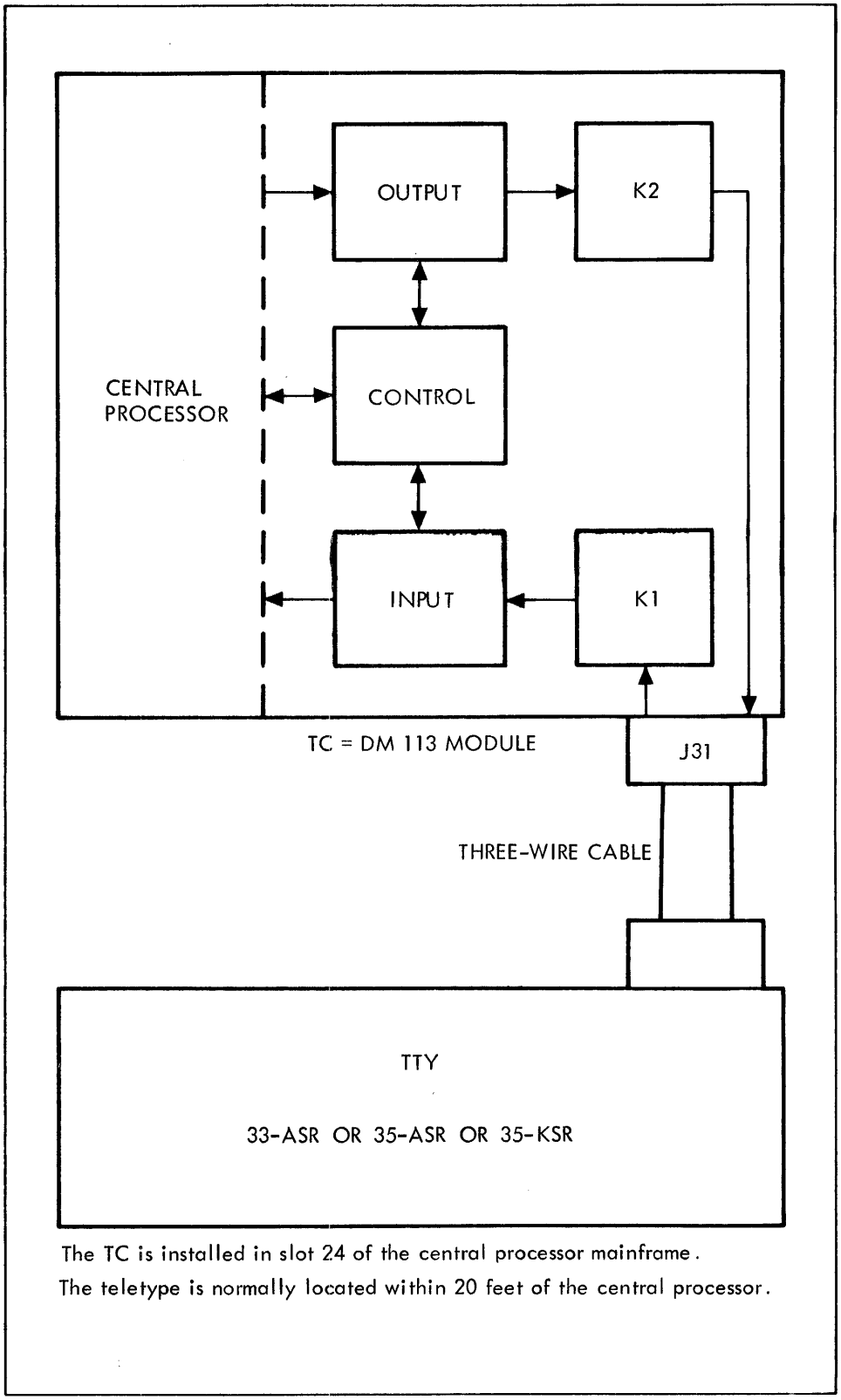
Table 4-1. Teletype Controller Specifications (continued)

Specification	Description
BIC control:	The TC is normally controlled directly by the central processor but it can be adapted at the user's option to BIC control or, with a buffer card, to indirect control on the I/O bus by the central processor.
Interrupt control:	The TC can provide "write ready" and "read ready" interrupts to a priority interrupt (PIM) option if the PIM is included as a feature of the computer.

1.3 PHYSICAL DESCRIPTION

The TC module is packaged on one standard DATA 620/i circuit card designated as DM 113. The following drawing is included in volume 2 of the 620/i Maintenance Manual:

44D0013 - assembly, DM 113, teletype controller.



The TC is installed in slot 24 of the central processor mainframe.
The teletype is normally located within 20 feet of the central processor.

Figure 4-1. Simplified Teletype Controller Block Diagram

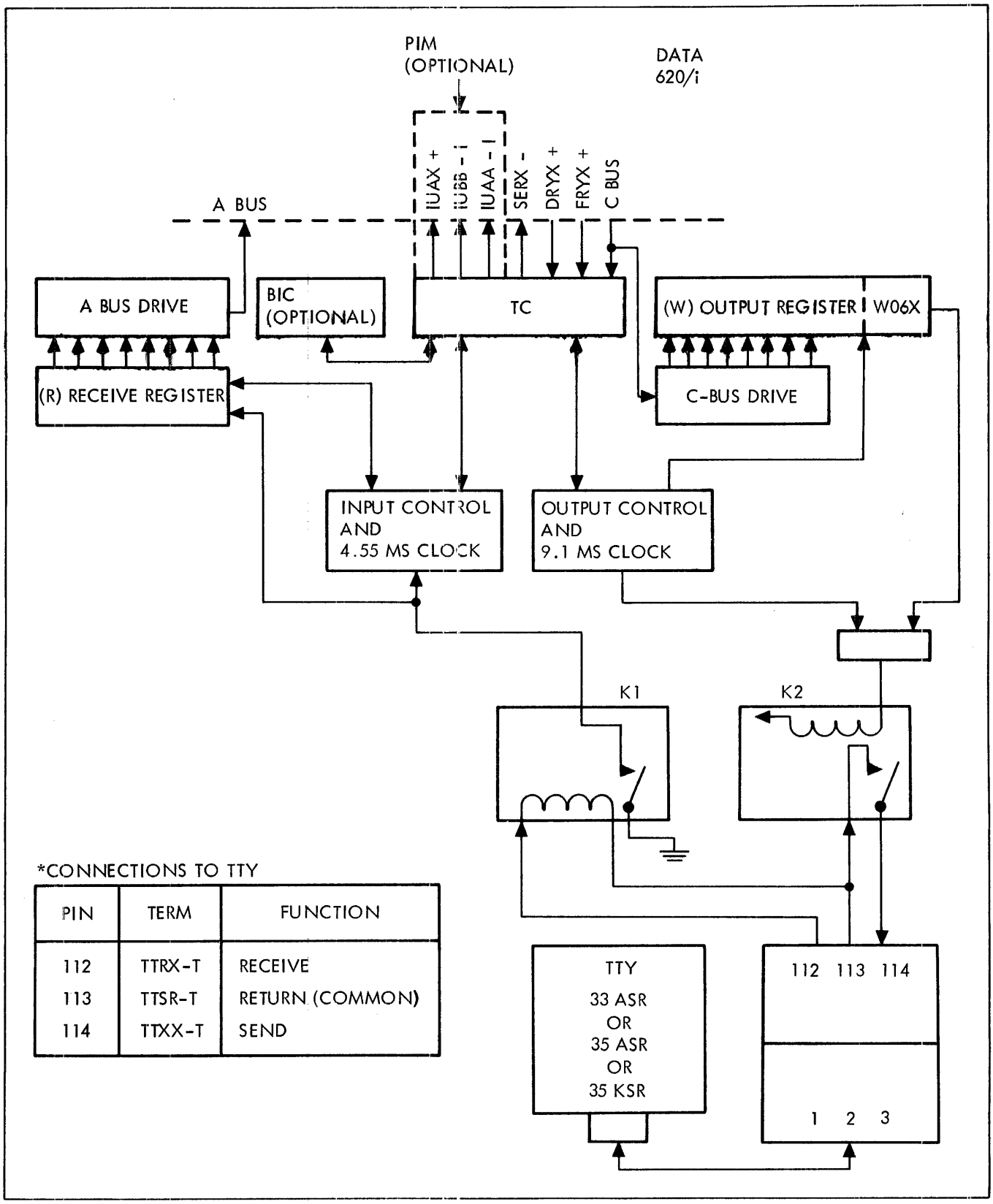


Figure 4-2. Teletype Controller Organization

2.1 INSTALLATION

The TC is installed in slot 24 of the central processor mainframe. Three wires lead from push-on terminals on pins 112, 113 and 114 of slot 24 to connector J31 located at the rear of the central processor mainframe. This wiring is included as part of the basic central processor and does not constitute part of the TC. The teletype is connected by a three-wire cable to connector J31.

2.2 OPERATION

There are no special switches on the computer or on the DM 113 module for operation of the TC. However, the SYSTEM RESET switch enables the initialize command (see 3.2) which prepares the TC for acceptance of central processor commands and for monitoring of incoming data from the teletype.

The teletype has line power and motor ON/OFF switches which are self explanatory (see section 4).

NOTE

If the teletype motor switch is in the ON position when the computer power switch is off, an open circuit or run command will be transmitted to the teletype. In this case, the teletype motor switch should be placed in the OFF position.

3.1 INTRODUCTION

The TC can be programmed directly by central processor control (with or without using interrupts) or indirectly through a BIC.

3.1.1 Interrupt

The TC can supply interrupts to the priority interrupt module (PIM) when this option is used in the computer. This saves considerable computing time and simplifies software since programmed delay and sense loops can be avoided. With this feature, the program running in the central processor is interrupted at the proper time.

3.2 COMMANDS

A list of commands for the teletype controller as well as the teletype unit are listed in table 4-2.

Table 4-2. Teletype Controller and Teletype Command Codes

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0101	100101	Connect Write Register to BIC
EXC 0201	100201	Connect Read Register to BIC
EXC 0401	100401	Initialize
B. Transfer		
OAR 01	103101	Transfer A Register to Write Register
OBR 01	103201	Transfer B Register to Write Register
OME 01	103001	Transfer Memory Register to Write Register
INA 01	102101	Transfer Read Register to A Register
INB 01	102201	Transfer Read Register to B Register
IME 01	102001	Transfer Read Register to Memory Register
CIA 01	102501	Transfer Read Register to Cleared A Register
CIB 01	102601	Transfer Read Register to Cleared B Register
C. Sense		
SEN 0101	101101	Write Register Ready
SEN 0201	101201	Read Register Ready

D. Teletype Command Codes

Function	Symbol	Code	Typed As
Print Enable	SOM	201	Control and A
Print Suppress	EOT	204	Control and D
Reader On	XON	221	Control and Q
Punch On	TAPE	222	Control and R
Reader Off	XOFF	223	Control and S
Punch Off	TAPE OFF	224	Control and T

Note: External control instructions are for use only with the BIC.

3.2.2 Initialize Command

This command performs the same function as the SYSTEM RESET switch on the computer console. The TC is prepared to accept central processor output and to monitor for teletype input. This command should not be issued while the TC is communicating with the teletype.

3.2.3 Sense Commands

These commands are the sense-ready-to-read and the sense-ready-to-write commands which enable the central processor to determine TC status. If the sense condition is met, a data transfer can proceed. If the sense condition is not met, the central processor must wait to perform data transfer. A sense command can be issued at any time and will normally precede any data transfer command.

3.2.4 Data Transfer Commands

These commands are the read (input) and load (output) commands which cause the transfer of data between the central processor and the TC through the read and write registers. Issuing a read or load command at the wrong time will result in incorrect data transfer.

3.2.5 External Control Commands

These commands are additional commands for use with the BIC. (See table 4-2)

3.2.6 Teletype Command Codes

(See table 4-2.)

3.2.7 Teletype ASCII Code

(See table 4-3.)

3.3 OPERATION WITHOUT THE BIC

3.3.1 Normal Operation - Start of Day

The software initializes the TC (same as pressing the SYSTEM RESET switch on the computer console.)

The TC is then ready to accept output from the central processor and is also capable of accepting an input character from the teletype. The software normally issues a sense command and, if a sense-ready condition exists, follows it with a read (input) or load (output) command to enable the data transfer of one character between the TC and the central processor.

Except for interrupts (see 3.1), the TC operates within the following general timing restrictions:

Output: Maximum data transfer rate is 10 cps. There is no minimum rate. The central processor can output a single character, discontinue output for an indefinite period of time (longer than 100 milliseconds) and then output another character without loss of data or synchronization.

Table 4-3. Teletype ACSII Code

Teletype Symbol	ASCII Code	Teletype Symbol	ASCII Code
@	300	X	330
A	301	Y	331
B	302	Z	332
C	303	[	333
D	304	/	334
E	305	]	335
F	306	↑	336
G	307	←	337
H	310	blank	240
I	311	!	241
J	312	"	242
K	313	#	243
L	314	$	244
M	315	%	245
N	316	&	246
O	317	'	247
P	320	(	250
Q	321	)	251
R	322	*	252
S	323	+	253
T	324	,	254
U	325	-	255
V	326	.	256
W	327	/	257

Input: Maximum data transfer rate is 10 cps (100 milliseconds per character). The central processor must read the input character transferred from the teletype by the TC during the last (second) 9.1 millisecond stop-bit period. If the central processor fails to read the character input during this time and before the teletype inputs again, the character will be lost.

3.4 OPERATING WITH BIC

The TC uses two additional commands when used with BIC (see table 4-2).

After initializing the TC, the program sets up the TC input or output buffer areas in the BIC and issues the connect read register or the connect write register command to the BIC. The TC is then under BIC control. This sequence is done only once for each new message area and thereby saves considerable software time.

NOTE

The TC, even though physically cabled to the BIC, can still be operated under direct control from the central processor.

3.5 TEST PROGRAMS

Diagnostic routines for TC and teletype are provided as part of the regular diagnostic package for the computer. Normally these are in the fourth program on the

MAINTAIN tape paper tape format. Instructions and other information for operation are included with this tape.

NOTE

One section of the teletype diagnostic for ASR models includes a print suppression test. The ASR-33 does not perform this function, so this diagnostic test should be bypassed when testing the ASR-33.

3.5.1 Basic Input/Output Test

If for some reason, such as paper tape reader failure, the diagnostic tape routines cannot be read, a simple input/output program for verification and troubleshooting of the teletype-TC operation can be entered through the computer console. This program tests keyboard input and printer output in the following way:

a. Operator enters the program through the computer console.

b. Turn the teletype to on-line.

c. Program starts at location 00000.

d. Now, any character input from the teletype will be transferred back to the teletype as an output from the central processor-TC almost immediately. Various character patterns and functions of the teletype can be checked by this "echo" method.

Table 4-4. Basic Input/Output Test Program.
ECHO Loop

Location	Command	Description
00000	101201	Sense read ready.
00001	000004	If yes, jump to 00004.
00002	001000	Jump back to 00000.
00003	000000	
00004	102501	Clear and input teletype character to A register.
00005	101101	Sense write ready.
00006	000011	If yes, jump to 00011.
00007	001000	Jump back to 00005.
00010	000005	
00011	103101	Output A register (to TC).
00012	001000	Jump back to 00000.
00013	000000	

4.1 FUNCTIONAL ORGANIZATION

The TC is designed to control the command and transfer of information between the central processor and a factory-modified model 33 or 35 teletype. The TC has the following major sections (see drawing 91D0005):

Section	Where Located on Drawing 91D0005
Central processor-TC interface	Sheet 1 of 4, left side.
Output (to teletype) timing control	Sheet 1 of 4, upper right side.
9.1 milliseconds clock	Sheet 4 of 4, left side.
Output register	Sheet 2, of 4, upper half.
TC-teletype interface	Sheet 2 of 4, K1, lower left. K2, lower right. J31, lower center.
Input (from teletype) timing control	Sheet 1 of 4, lower left side.
4.55 milliseconds clock	Sheet 4 of 4, right side.
Input register	Sheet 2 of 4, lower half.
BIC control	Sheet 3 of 4, left side.

NOTE: TC backpanel wiring is also shown on sheet 3 of 4, right side.

4.2 TELETYPE DESCRIPTION

4.2.1 Reference Material

This sub-section deals with the teletype interface in a general manner. The manuals and reference material supplied with the teletype equipment should be referred to for specific information.

4.2.2 General

The TC interfaces a factory-modified model 33 or 35 teletype. Factory modification of the teletype units is done prior to delivery to the customer. Modification of the model 33-ASR teletype entails the following 6 steps:

1. Set the teletype for 20-milliampere operation. This includes the addition of a wire which enables the teletype to supply "battery" for the send and receive data loops to the TC. This makes the teletype the current source for the teletype-TC relay driver interface.
2. Set teletype for full duplex operation.
3. Disable WRU contacts.
4. Disable parity on keyboard.

5. Modify answer-back drum.

6. Install the 180801 function lever.

The model 35 modification is similar to the above model 33-ASR modification. Model 33 and 35 teletypes are electrically interfaced and cabled to the TC in almost the same manner, although they are physically quite different in appearance and in their internal operation.

4.2.3 Model 33-ASR

The model 33-ASR is primarily designed for light to medium use. Normally, it is the basic central processor input/output device and is the most widely used unit. Its full-duplex operating mode allows simultaneous input and output.

4.2.4 Model 35-ASR

This unit performs the same function as the model 33-ASR, but it is designed for heavy, sustained use.

4.2.5 Model 35-KSR

This unit is used for keyboard send receive only and lacks the paper tape punch (PTP) and paper tape reader (PTR) capability of the ASR teletypes. The operating characteristics are similar to model 33 keyboard operation. This unit is also designed for heavy, sustained use.

4.2.6 Input Methods and Description

Keyboard: Operator types at a random rate not greater than 10 cps.

Paper tape reader: Standard eight-level tapes are input at a 10 cps, maximum rate.

Input may be random or constant at the 10 cps, maximum rate.

4.2.7 Output Methods and Description

Printer: The central processor transmits control codes or data at a random rate, or at a constant 10 cps maximum rate. Data is printed out or control functions such as line feed or carriage return are performed.

PTP: The central processor transmits, via the TC, control codes or data at a random rate or at a constant 10 cps maximum rate. Control codes and data are punched into eight-level paper tape.

Teletype control switches. Model 33-ASR:

ON/OFF switch turns the motor on or off, but the teletype power supply and battery for interface relays and cable stays on independent of the motor switch. Line switch ON-LINE position completes TC and teletype interface and places teletype under central processor control.

Line switch OFF-LINE position disconnectes teletype from TC interface and enables teletype to be used for printing or tape preparation independent of central processor control.

The START/STOP/FREE switch on the PTR is used as follows:

START position causes reader to move tape. STOP position stops the tape. FREE position frees tape from the sprocket drive wheel, enabling easy positioning of the tape by the teletype operator. Backspace control is on the PTP.

Activiation of the BSP control will backspace the tape one character.

Release control is on the PTP.

Activation of the REL control removes pressure from the tape.

LOCK ON control on the PTP locks the punch on and prevents status change of the punch by external control.

UNLOCK control on the PTP unlocks the punch and enables punch status change by central processor or by keyboard.

Model 35-ASR:

This teletype has the ON/OFF motor switch, line switch, and the START/STOP/FREE switch all of which function the same as on the model 33-ASR. The model 35-ASR also has a mode switch mechanism which enables the following operating modes:

Position	Keyboard	Reader	Printer	Punch
K	On line	Disabled	On line	Off line
KT	On line	On line	On line	On line
T	Off line	On line	On line	Off line
TTS	Off line	On line	Disabled	Off line
TTR	Off line	Disabled	Disabled	On line

Model 35-KSR:

This teletype lacks the PTR, PTP, so related control switches are not included.

Teletype controlcodes:

Certain codes sent to teletype will cause the unit to perform functions. These control codes have the seventh bit on at all times. Control codes used with factory-modified teletypes also have the eighth bit on at all times. The following teletype control codes are used in the in central processor-TC-teletype system:

Code	Bit Format	Function
Control A	10000001	Enable printer
Control D	10000011	Disable printer
Control R	10010010	Enable punch
Control T	10010100	Disable punch
Control Q	10010001	Enable reader
Control S	10010011	Disable reader

Care must be token that a disable code is followed by an enable code for a mechanism to be used. Codes R, T, Q and S are not applicable to model 35-KSR teletype.

4.3 TELETYPE TRANSMISSION

This description is valid for teletype models 33 and 35. Relays K1 and K2 (see drawing 91D0005) perform the actual interface between the TC and the teletype. The relays are used to electrically and physically isolate the two units.

4.3.1 Interface Loops

K1 is the receiving relay and is driven by the teletype. K2 is the sending relay and is driven by the TC. The relays are used to switch approximately 20 milliamperes of current on or off the line. This method of interface is called "make-break". Each relay can be said to drive or to be driven by a current loop. When there is current flowing through a relay coil, the relay contacts are closed and the current loop is closed. The line is then in the make condition (also referred to as the mark condition). When no current flows through the relay coil, the relay contacts are open and the current loop is open. The line is then in the break condition (also referred to as the space condition). The steady state of the loops is the mark condition when both the computer and teletype power is on, and both K1 and K2 relays are energized. When either the computer or teletype power is off, the steady state of the loops is in the break condition, and neither K1 or K2 is energized.

Except for the difference in switching control location, the send and receive loops have identical function. The loops are shown in full-duplex configuration in figure 4-3. The factory-modified system is full-duplex to provide simultaneous transmission of data in both directions.

The current source for the two loops originates in the teletype and is sometimes referred to as "battery". The central processor and TC use no loop source current, since they are isolated by the K1 and K2 relay contacts. Typical current in a factory-modified teletype interface loop is 20 milliamperes.

This relay-controlled current loop method of interface enables the central processor-TC and the teletype to be placed quite far apart without noise interference, ground loops, etc., affecting the system. Normally, the teletype cable is 20 feet long.

4.3.2 Data Transfer

When either teletype or TC sends data, K1 or K2 operate (make or break) to conform to the character pattern being sent. The maximum relay switching rate is 9.1 milliseconds per bit. Characters are sent or received serially by the current loop.

4.4 CHARACTER AND BIT FORMAT - ASYNCHRONOUS

Each teletype character or command is serial and is divided into eleven periods or bits consisting of one start bit, eight data bits (the eighth bit is always mark), and two stop bits (see figure 4-4).

The bit pattern is shown for the character in figure 4-4 is 10101011. The bit length is 9.1 milliseconds, and the bit rate is 110 bits per second (bps). The character length is 100 milliseconds, and the character rate is 10 cps. The start bit is always a space = zero bit = no current in loop = loop open. Data bits are either mark or space. A mark = one bit = current in loop = loop closed.

In the factory-modified system, the eighth data bit is always mark. It might be used by the teletype as an even parity bit on an optional basis. The stop bit(s) is

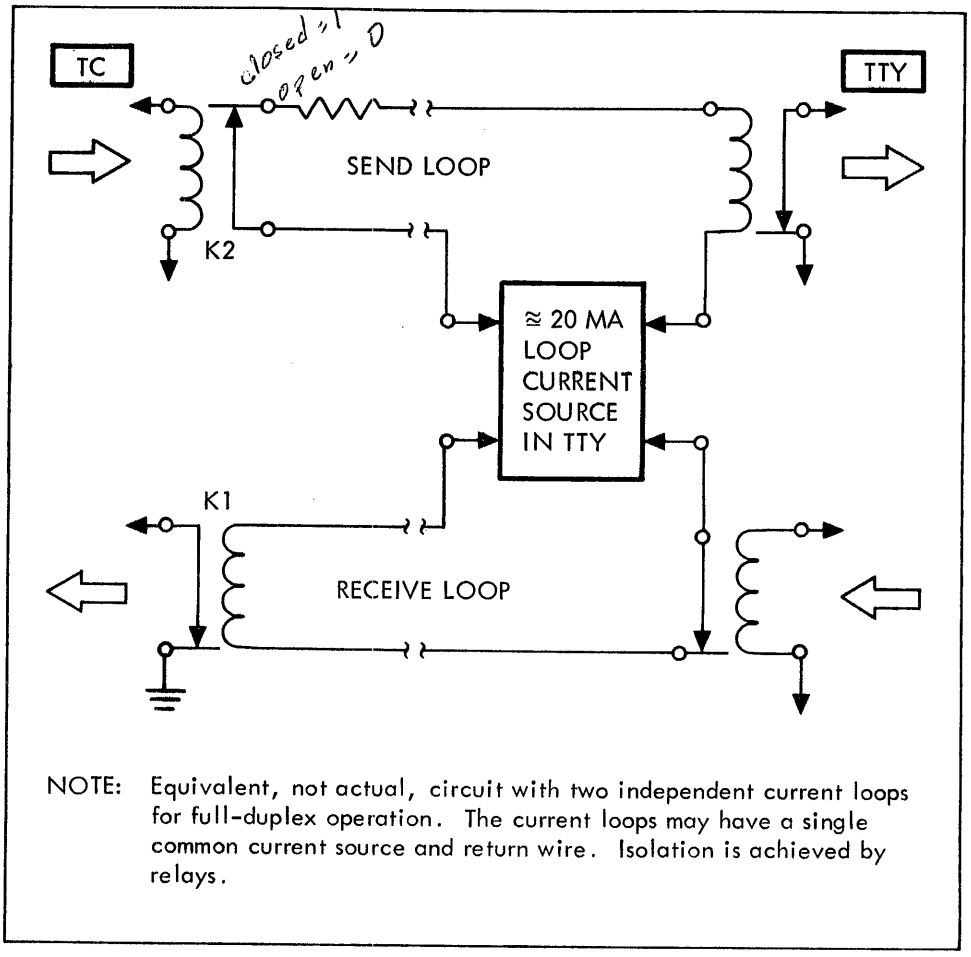


Figure 4-3. Typical Full-Duplex Teletype-TC Connection for Model 33-ASR in Factory-Modified System

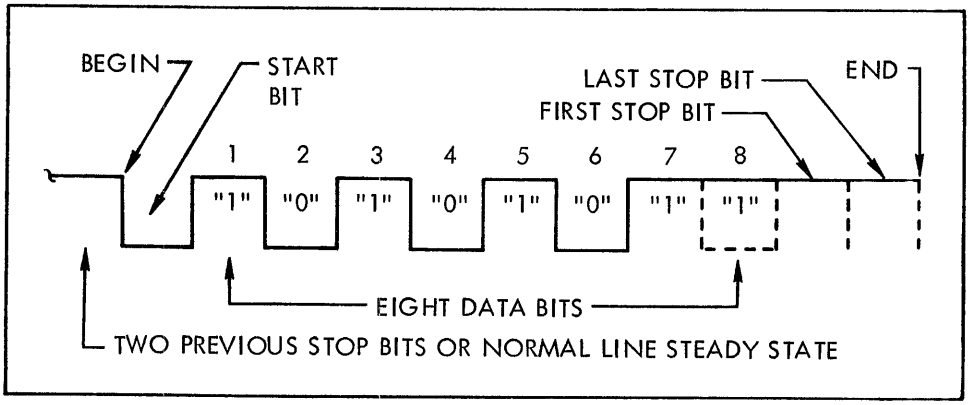


Figure 4-4. Typical Teletype Character

always mark. The line may remain at mark level or a new start bit may occur following the last stop bit.

The start and stop bits in the character bracket the data bits. This simplifies the design and operation of the TC receiving circuitry.

NOTE

The expression "teletype is running open" means the send loop to the teletype lacks current = steady spacing condition. This occurs if relay K2 remains open, or if the loop current source fails, or if the send loop opens at any point.

4.5 INPUT CHARACTER RECEPTION - TYPICAL

The receiving circuitry synchronizes itself at start-bit time. The TC receiving oscillator (4.55 milliseconds clock) normally begins to run at the leading edge of the start bit. Sampling and shifting of the bit pattern then occurs in the center of the start bit and continues at the center of each data bit through the eighth data bit. Normally each sampled bit is shifted into a register. When the last data bit has been sampled and shifted, the character is ready for transfer to permanent storage (computer, etc.). The TC enables transfer to the central processor at the beginning of the last stop bit. The stop bit(s) period is used for transfer of the character to the central processor, therefore, these bits are not sampled. Typically, the TC receiving oscillator stops after the data bits and the first stop bit are transferred and will not start again until a new start bit is received (see figure 4-5).

To keep the receiving unit synchronized with the sending teletype, the receiving oscillator or equivalent timing circuit must be allowed to stop and restart when the start bit for the next character occurs. If the sending device outputs a new start bit before the receiving oscillator has time to stop and recover, the two units are out of synchronization and erroneous data result. The next new character start bit may occur immediately after the stop bit(s) or may not occur for an indefinite time interval. This is typical of asynchronous transmission. The receiving unit must be able to receive and synchronize to new data at any time.

4.6 OUTPUT CHARACTER TRANSMISSION - TYPICAL

The teletype is assumed ready to receive data at any time. The TC output sequence is:

An output character is loaded into the output register. An oscillator circuit starts and sends a start bit. (All bit times start, data and stop are equal, and each bit takes one oscillator period.) The oscillator enables shifting of the succeeding bits through the output register. The last stage in the register drives the TC send circuitry (K2). The oscillator continues to run and shift until all eight data bits are out.

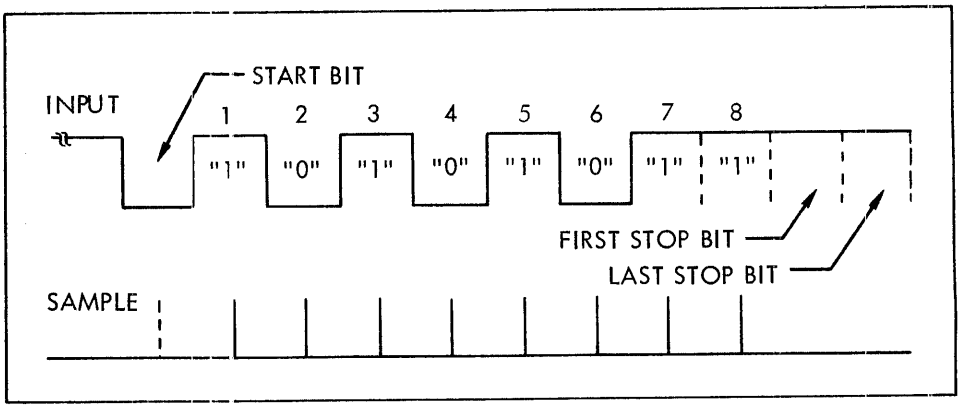


Figure 4-5. Input Character Sampling

When the last data bit is sent, the TC obtains a new character from the central processor in preparation for the next character transmission. The oscillator in the TC continues to run during the stop bit(s). Typically, the TC obtains a new character during the last stop bit. If there are no more output characters, the TC oscillator stops and places a steady one-bit level on the output line. The teletype can then await a new start bit which occurs on the next output character.

4.7 ASYNCHRONOUS TRANSMISSION

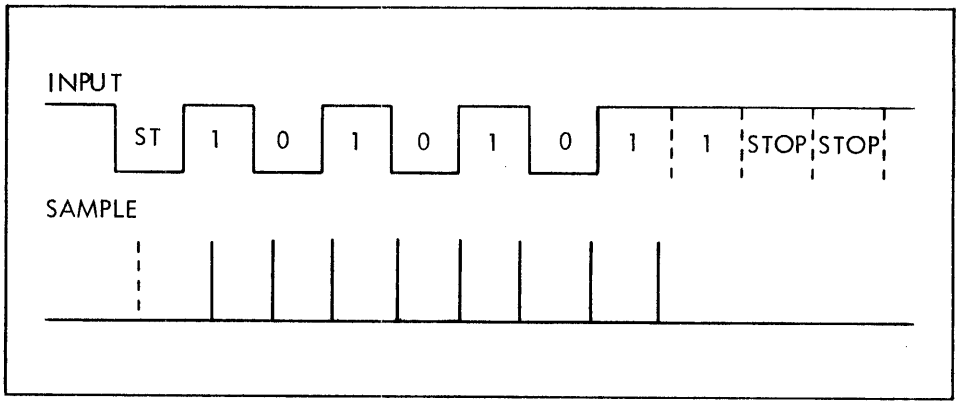
The previous subsections detailed basic input and output. Several points should be stressed again:

Sending unit sends at a full or random rate at any time.

Receiving unit must be able to accept data at any time and at a full or random rate.

Receiving unit must resynchronize with every new start bit (every character) to maintain proper synchronization. The oscillator used for this purpose is called a start-stop or gated synchronizable oscillator.

The length of the output character must be carefully maintained. The receiving circuit can normally tolerate some distortion (less than 1/2 bit per total character), so the length of output character and each of its bits is important. If the length of output characters is short or long and cannot be corrected, the receiving sampling circuitry can sometimes be adjusted to compensate. The following waveforms illustrate an example of proper output character length but misadjusted input timing.



Note that the first few samples are tolerable but the sample clock (oscillator) is set short so sampling is faulty on the last few bits of a character.

If the sample clock is set too long, a worse condition may occur. The oscillator may be on when a new start bit occurs, causing synchronization to be completely lost.

5.1 GENERAL DESCRIPTION

The TC serves as an interface device between the DATA 620/i and a factory-modified model 33 or 35 teletype. Operation between TC and teletype is full-duplex, serial, asynchronous, and uses a pair of printed circuit board relays for interfacing and isolating the two units (see 4.3).

The TC interface with the central processor is through back-panel wiring in slot 24 of the computer mainframe. Data and control leads as well as various test points are available at this interface.

Data lines to the TC are driven from the C bus, and data lines from the TC to the central processor enable the A bus. Control lines between the central processor and the TC are driven directly into logic.

NOTE

To gain more from the following discussion, drawing 91D0005 and the function index list in chapter 6 should be referenced.

5.2 INITIAL (SYSTEM RESET) CONDITION

When DATA 620/i power is first turned on, the TC and the central processor circuitry may be in an undefined state. Activation of the SYSTEM RESET switch on the computer console initializes the TC (and the computer) to properly perform various functions under program control. Basically, this enables the TC to monitor the teletype for input characters and to accept output characters from the central processor to the teletype. When initialized, the TC also transmits a steady mark to the teletype by keeping relay K2 energized.

NOTE

An initialize command performs the same function as activation of the SYSTEM RESET switch.

Either system reset (SYRT) or initialize command (EXCX, CB08) perform the following functions (INZX true):

RESET	SET
RRDY RDDX DTOX DTIX RRCX CDCX	RECX WRDY RSCX W00X TR0X

The 9.1 milliseconds clock and the 4.55 milliseconds go off if turned on initially.

Note that W01X through W10X and R01X through R09X are not cleared initially. W00X, being set energizes the K2 relay thus assuring that a mark is sent on the send loop to the teletype. If teletype power is on, the teletype will energize relay K1 and the TC will receive a steady mark.

The TC is then in a line monitoring state.

5.3 CENTRAL PROCESSOR-TC INTERFACE CONTROL

The central processor communicates to the TC via the C bus with direct logic terms, such as FRYX and DRYX. When the central processor issues commands to the TC via the C bus, the following device address sequence occurs for any command.

DAXX (device address) is true during EBDX if proper address configuration is put on C bus (the TC responds to address 01). The term EBDX (E-bus drive) enables generation of DAXX and occurs during the address setup portion of all commands. In turn, DAXX enables the command generation gates.

The following C-bus functions occur at the control section:

CB00 through CB05 = enable DAXX

CB06 = enable output ready sense response

CB07 = enable input ready sense response

CB08 = enable initialize sequence

CB11 = enable execute (initialize) sequence

CB13 = enable input command sequence

CB14 = enable output command sequence

The central processor may issue any of several commands. All of the following commands are accompanied by DAXX and some are also accompanied by a FRYX-DRYX sequence:

Sense write ready (CB06)	No FRYX or DRYX
Sense read ready (CB07 & CB13)	No FRYX or DRYX
Execute (Initialize) (CB08 & CB11)	FRYX only
Output (Load/write registers) (CB13)	FRYX and DRYX
Input (Read/read register) (CB13)	FRYX and DRYX

Input and output timing diagrams in figures 4-6 and 4-10 illustrate the FRYX-DRYX sequence.

5.3.1 SERX -, DTIX and DTOX Functions

SERX- is sense response and is at ground level if a sense condition is met. The central processor normally issues a sense command before input or output. The ground level is enabled by the term RRDY (read ready) or WRDY (write ready) which signify the TC has an input character or is in condition to accept an output character.

In the initialized condition, WRDY is set in the TC to enable immediate output under central processor control. The RRDY is not set until the teletype has inputted a complete character.

DTOX is data transfer out and is set and reset by a FRYX-DRYX sequence when the central processor issues an output command (see figure 4-6). DTIX is data transfer in and is set and reset by a FRYX-DRYX sequence when the central processor issues an output command (see figure 4-10).

5.4 OUTPUT DESCRIPTION

The TC output section has several control flip-flops, a group of gates enabled by the C bus, a 9.1-millisecond oscillator, an 11-bit write register, an output relay (K2) to teletype and associated drive circuitry. Loading of output from the central processor to the teletype is illustrated in figures 4-6 and 4-7.

The following output sequences occur:

5.4.1 Sense Response

Assume initialized condition. Normally, the central processor issues a sense-write-buffer-ready command and the TC, if ready to write, enables SERX-. The central processor then issues a load/write register command.

5.4.2 Load/Write Register Sequence

When the load/write register command is issued, the following sequence of events occurs:

C bus signals enable DAXX, FRYX comes true, and at the end of FRYX, flip-flop DTOX sets. WRIX- goes to ground, resetting WRDY and setting W09X and W10X which hold the two stop bits of the output character.

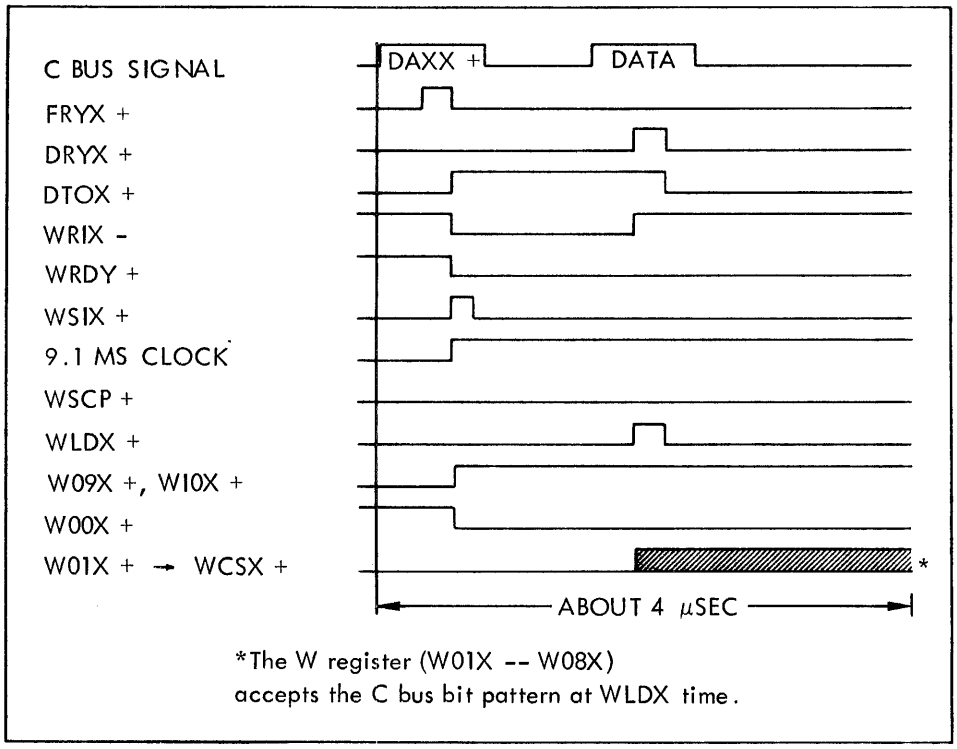
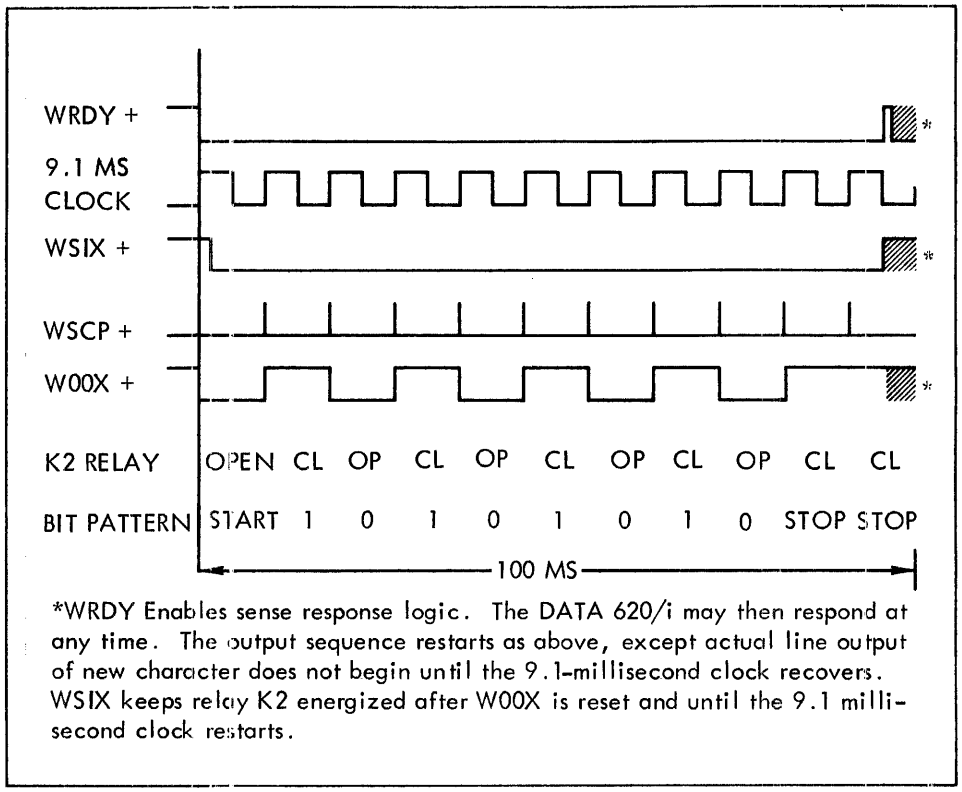


Figure 4-6. Data and Control Timing Output Waveforms from DATA 620/i to the TC



*WRDY Enables sense response logic. The DATA 620/i may then respond at any time. The output sequence restarts as above, except actual line output of new character does not begin until the 9.1-millisecond clock recovers. WSIX keeps relay K2 energized after W00X is reset and until the 9.1 millisecond clock restarts.

Figure 4-7. Data and Control Output Waveforms from TC to Teletype

WRIX- also clears W00X through W08X. W00X, being reset, causes the send relay (K2) to release. This causes the start bit to be sent for 9.1 milliseconds to the teletype. When WRDY is reset, WSIX is set, and the 9.1-millisecond oscillator starts. (WSIX set prevents (the first) WSCP which prevents the W09X and W10X flip-flops from shifting.) WSIX will reset about 80 nanoseconds after the 9.1-millisecond clock starts and will remain reset until after the next sequence.

When DRYX comes true, WRIX- goes true (+5V), and also WLDX goes true (for about 200 nanoseconds). WLDX true enables the output bit pattern, placed by the central processor on the C bus, to be loaded into W01X through W08X for output under TC timing control. No further computer action is necessary until the next output character. At this point, with the load/write register loaded, the central processor can proceed with other functions for about 95 to 100 milliseconds before the TC will require a new output character. The 9.1-millisecond clock has already started (at WRIX). When WSIX is reset, the next WSCP releases the K2 relay and sends the start bit (no current condition) to the teletype. The teletype detects the start bit and begins a receive sequence.

The foregoing sequence takes about 300 nanoseconds.

5.4.3 Output to TTY Sequence

This sequence is illustrated by figure 4-7. The 9.1-millisecond clock (started in previous sequence) continues to run and the start bit is transmitted. At the end of the first 9.1-millisecond clock period, the following sequence of events occurs:

The first WSCP pulse (about 80 nanoseconds) occurs, causing the W register to shift right one place. The least significant bit (in W01X) is now shifted into W00X. Depending on the bit pattern, relay K2 energizes if the shifted bit is a ONE bit, or remains deenergized if a ZERO bit is shifted. The 9.1-millisecond clock continues to run, enabling WSCP at the start of each clock period. Relay K2 "follows" the bit pattern originally set into the W register. During the tenth clock period, the first stop bit is sent. At the start of the tenth clock period, the WSCP shifts the last (second) stop bit into W00X. At this time, K2 is energized by the first and last stop bits. When the last WSCP occurs (at the start of the tenth clock period), W00X becomes true and all other W register flip-flops are then reset, enabling the end-of-character sequence.

Pin 6 of IC21 is grounded, enabling pin 8 of IC15 to become true. This partially enables the clock input gate (IC1) on WRDY. When the 9.1-millisecond clock is midway through the eleventh period, the IC1 gate is enabled and WRDY sets. This signifies that the TC is ready to accept another output character from the central processor.

NOTE

The 9.1-millisecond clock could be enabled immediately, but will not start a new clock period until the present 9.1-millisecond period ends.

The computer is normally sensing for a write ready (output buffer ready) condition and can now issue another output command.

NOTE

The WRDY becomes true at T=95.45 milliseconds (of the 100 millisecond character), which gives the central processor 4.55 milliseconds to load a new output character and maintain a full rate of 100 milliseconds per character.

5.4.4 Central Processor Response

If the central processor responds within 4.55 milliseconds the load/write register sequence occurs. The 9.1-millisecond clock does not restart until the previous 100 millisecond character period has elapsed (see notes above); hence, WSIX stays set. This causes the TC to keep relay K2 energized, forcing the last stop bit to finish. When the 9.1-millisecond clock recovers; WSIX resets, and the output proceeds as for the previous character.

If the central processor responds after 4.55 milliseconds; the load/write register sequence will be performed exactly as described in the preceding paragraphs because the 9.1-millisecond clock has recovered. W00X is still set, keeping a mark on the line to the teletype through the K2 relay. The central processor may not respond at all, in which case the above condition remains indefinitely until a CPU response occurs. In any case, the teletype remains ready to accept a new (start bit) character at any time.

Figures 4-6 and 4-7 describe the data and control timing output waveforms. In these figures, assume the following: initialized condition, central processor has sensed write ready and issued an output command, and output character is 01010101.

The waveforms shown in figure 4-7 occur after the sequence shown in figure 4-6.

5.5 INPUT DESCRIPTION

The TC input section has several control flip-flops, a group of gates to enable the A bus, a 4.55-millisecond oscillator, a 10-bit read register, and an input relay (K1) for the teletype.

This description is divided into three sections: Input control during start bit, data input from the teletype, and data transfer to the central processor. Waveforms of these sectional functions are illustrated in figures 4-8, 4-9, and 4-10.

The following input sequences occur:

5.5.1 Input Control During Start Bit (see figure 4-8)

Assume initialized condition. The teletype begins to send (input) the start bit of an input character. The start bit cause the receive loop to open, no current flows in the loop, and relay K1 deenergizes. After the K1 relay switching delay, term TTRX is grounded. TTRX false causes RDDX to set, starting the 4.55-millisecond clock. The 4.55-millisecond clock enables the IC20 and IC42 delay network. Pin 6 of IC42 becomes true for about 80 nanoseconds, causing RRCX to become true. This enables RRCP- to become false for about 80 nanoseconds, and sets all receive register flip-flops R01X through R09X.

The 4.55-millisecond clock continues to run, and at the end of its first period (when T=4.55 milliseconds), the following sequence occurs:

> Pin 6 of IC42 again becomes true for about 80 nanoseconds, causing RSCX to reset. This causes the first RSCP to become true for about 80 nanoseconds, shifting the start bit (TTRX = ground), into R09X. This shift occurs in the middle of the start bit. The 4.55-millisecond clock continues to run, and at the end of the second period (when T = 9.1 milliseconds), pin 6 of IC42 becomes true again to set RSCX. At this time, the teletype begins to transmit the first data bit of the character.

5.5.2 Data Input from the Teletype (see figure 11-12)

At the end of the start bit sequence (when T = 9.1 milliseconds), the teletype transmits the first data bit. The TC has shifted the start bit into R09X and is set up to receive the eight bits. The 4.55-millisecond clock continues to run and at the end of the third period, pin 6 of IC42 becomes true, RSCX resets, RSCP becomes true, and the first data bit is shifted into R00X causing the start bit in R09X to shift to R08X, etc.

This sequence continues through for each data bit. The 4.55-millisecond clock runs two periods for each bit. The RSCX flip-flop is triggered each 4.55 millisecond, enabling RSCP to occur in the center of each bit so that sample and shift pulses can occur.

When the last data (eighth) bit is accepted (followed by the first stop bit), an end-of-character sequence begins in the center of the bit. When the eighth data bit is shifted into R09X, the start bit resets R01X. Two clock periods later, in the center of the first stop bit, the next RSCP occurs, to reset RECX. This pulse also shifts the start bit out of R01X and shifts the first stop bit into R09X.

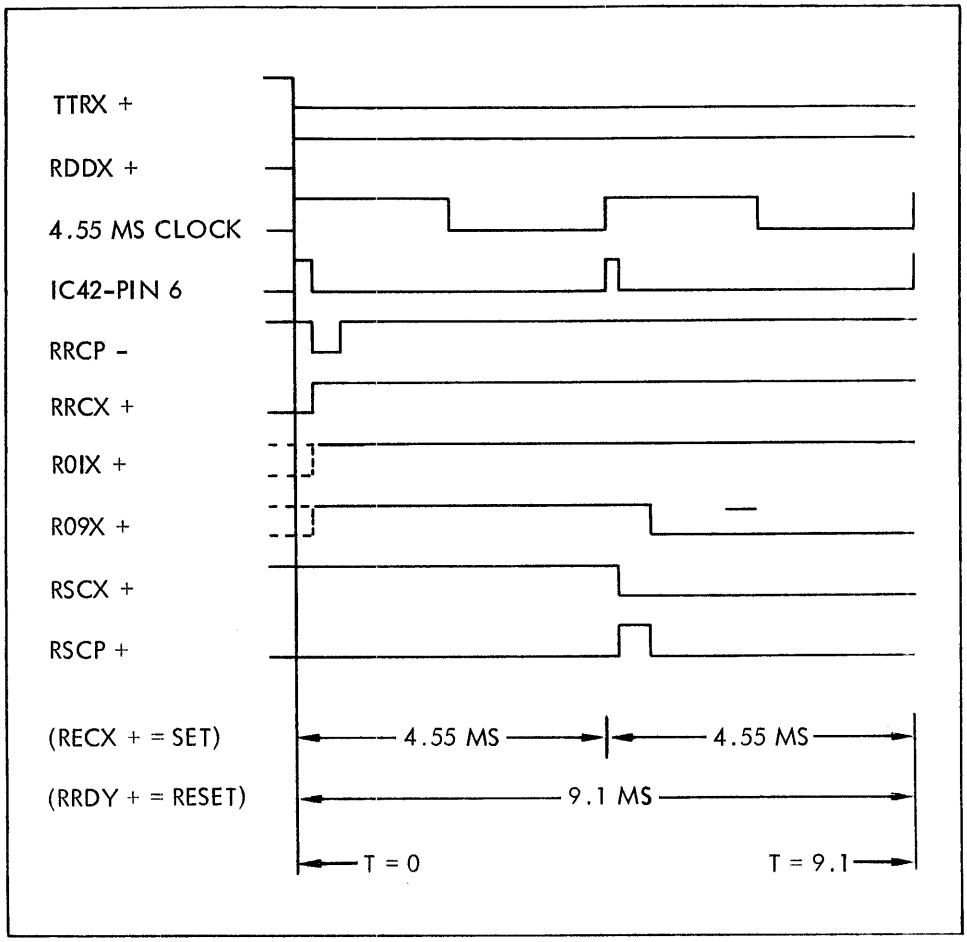


Figure 4-8. Data and Control Input Waveforms During Start Bit

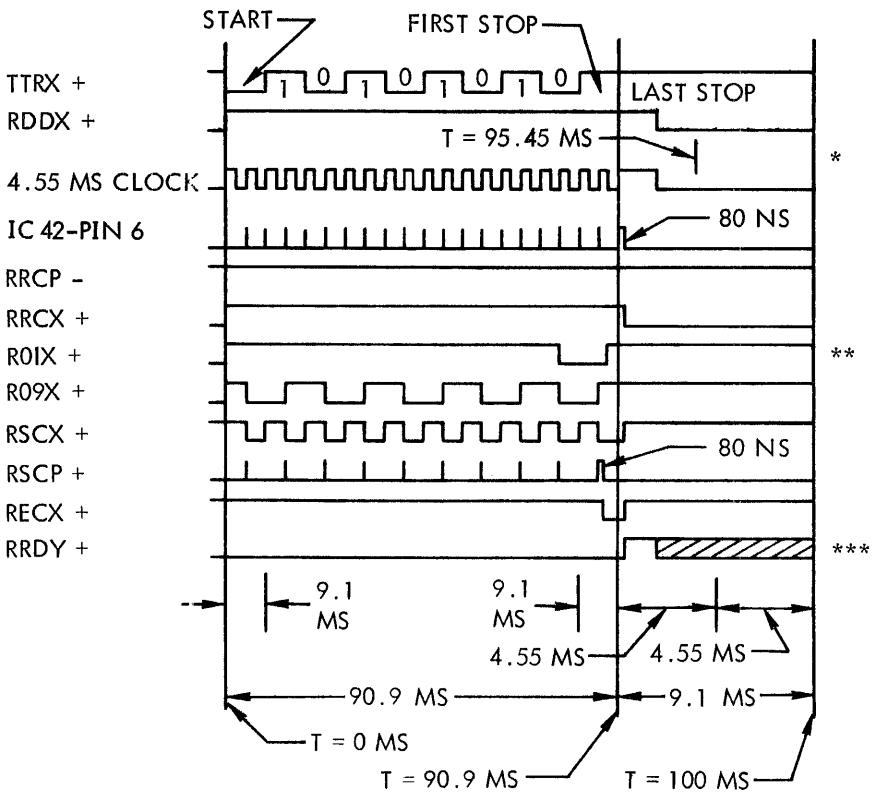
At this time the character is completely in the receive register. The TC is preparing to enable character transfer to the central processor and the teletype is transmitting the second half of the first stop bit.

The 4.55-millisecond clock continues to run. At the end of the period that ends the first stop bit (when T = 90.9 milliseconds), pin 6 of IC42 becomes true for about 80 nanoseconds, RRCX resets via RECX, and RECX is set. RRCX partially disables input to RDDX to stop the 4.55-millisecond clock. Before being reset by RRCX, RECX causes RRDY to set. This enables a read/read sense response to the central processor (see discussion of next sequence).

The 4.55-millisecond clock continues to run for one more period. Half way through this last 4.55-millisecond period the RDDX flip-flop resets, removing the clock start enable.

NOTE

The 4.55-millisecond clock does not recover until T = 95.45 milliseconds. Prior to this time it cannot be accurately restarted with a new start bit from the teletype. If a new start bit from the teletype occurs before T = 95.45 milliseconds, the resulting out-of-sync condition causes erroneous data sampling and errors.

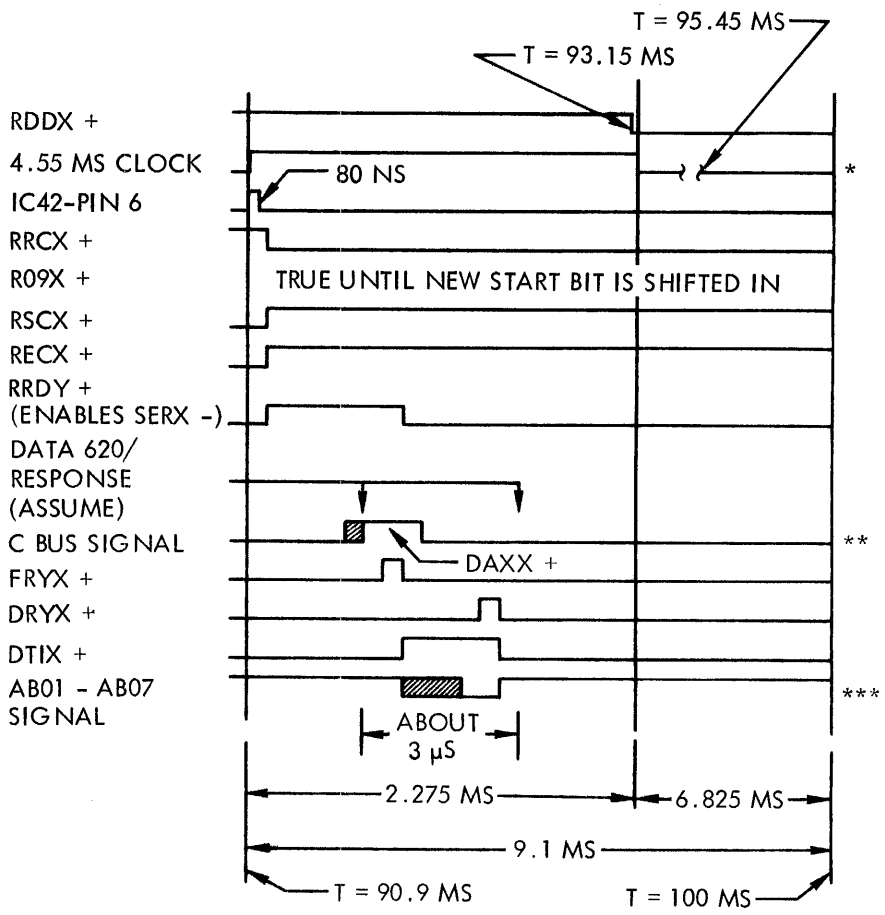


*The 4.55-millisecond clock may be restarted and synchronization established any time after T = 95.45 milliseconds.

**R01X is set if lsb is a one bit, reset if lsb is a zero bit.

***RRDY is set (enabling sense response) until the central processor issues an input command. The central processor must respond before a new start bit is transferred through the TC or character is lost.

Figure 4-9. Data and Control Input Waveforms During Data Input from the Teletype



*New start bit can occur any time after T = 95.45 milliseconds and synchronization with the teletype is maintained. Data transfer to the central processor must occur before a new start bit or the character in the receive register is lost. If a new start bit occurs before T = 95.45 clock synchronization with the teletype will be lost.

**C bus signals are for device address (normally device 01).

***The AB00 - AB07 lines are enabled by EBRX from the central processor.

Figure 4-10. Data and Control Input Waveforms During Data Transfer to the Central Processor

5.5.3 Data Transfer to Central Processor (see figure 4-10)

At the end of the first stop bit (when T = 90.9 milliseconds), RRDY sets to enable a sense-ready-to-read response in the data processor.

> **NOTE**
>
> At a continuous 10 cps (100 milliseconds per character) rate, the central processor has less than 9.1 milliseconds to read the character out of the read register. If an input data command is not issued before 9.1 milliseconds, the character is lost. The start bit of the next character resets RRDY, preparing the read register and TC for a new character.

After the central processor senses the read ready condition, it issues an input data command. With DAXX true at the end of FRYX, DTIX sets and RRDY resets. The central processor makes EBRX true. EBRX and DTIX enable the A bus gates driven by the R01X through R08X registers. Therefore, during DRYX time, the character is on the A bus lines to the central processor. When DRYX ends, the DTIX flip-flop resets and input to the central processor is complete. As noted before, the character transfer to the central processor must occur before the start bit of a new character to avoid losing the character.

The TC input section now waits for a new start bit which may occur at any time. Until a new start bit occurs, the K1 relay remains energized and the 4.55-millisecond clock and RDDX remain off.

Figure 4-8, 4-9, and 4-10, describe data and control timing input waveforms.

In these figures, assume the following:

Initialized condition.

TTY has just begun to transmit a character.

Relay K1 is beginning to deenergize.

After relay switching, pins 3 and 4 of relay K1 are open.

The waveforms shown in figure 4-9 occur after the sequence shown in figure 4-8. These waveforms include the complete character. Input to the central processor is enabled during the last stop bit. This last stop bit is shown extended for clarity.

The waveforms shown in figure 4-10 occur after the sequence shown in figure 4-9. With these waveforms, assume the following.

Data bits of character have been shifted into receive register.
TC is receiving last stop bit.
The central processor issues an input command.

The time from T = 90.9 milliseconds to T = 93.175 milliseconds is shown extended for clarity.

5.6 OPERATION WITH BIC AND PIM

The previous paragraphs describe TC operation via direct computer control. Optionally, the TC may be operated under BIC control.

5.6.1 BIC

In this mode of operation, the start and stop addresses of data are placed in the BIC. Command and data transfer is under supervision of the BIC. This frees the computer to do other tasks while data transfer is in progress.

5.6.2 Wiring for BIC

The wiring for slot 24 of the DATA 620/i mainframe is modified for operation in the BIC. The modified wiring connects the BIC drive signals such as TR0X-B to the TC. (See drawing 91D0005 sheet 3, and the function index list in chapter 6.)

5.6.3 Operational Change

The output and input function to and from the teletype is unchanged. The transfer to and from the computer is accomplished with the following changes:

Output: The computer-BIC combination sets TR0X and CDCX. This enables CDCX-B and TR0X-B. If WRDY is set, TRQX-B is also enabled. These signals enable the BIC. The BIC responds with TAKX-B, and DOEX- is enabled. This causes DTOX to set, and the output character is taken from the C bus. Output to the teletype then proceeds under TC control.

Input: The computer-BIC combination sets CDCX and resets TR0X. This enables CDCX-B. When RRDY becomes true, TRQX-B is enabled. When the BIC responds with TAKX-, DIEX- is enabled to set DTIX. This enables transfer of the input character onto the A bus.

5.6.4 PIM Drivers

The PIM Drivers are as follows:

IUAA-I = write priority interrupt, enabled by WRDY

IUBB-I = read priority interrupt, enabled by RRDY

The PIM drivers are wired from the TC to the computer PIM logic (module DM 124) and are used to generate interrupt requests. This saves considerable computer time. The DATA 620/i computer must be equipped with the PIM in order to use these drivers.

This section describes maintenance and troubleshooting procedures.

6.1 TEST EQUIPMENT REQUIRED

The same equipment as required for DATA 620/i maintenance can be used – i.e. oscilloscope, meters, and tools. No special equipment is required.

6.2 MAINTENANCE AIDS

The teletype is the best diagnostic aid because the data being sent are printed out and can be analyzed. Also, known input patterns can be generated (via keyboard or paper tape) and data can be analyzed in the computer or returned to the teletype for printed analysis (see 3.5.).

6.3 ROUTINE MAINTENANCE

The condition of the teletype unit should be periodically checked by using diagnostic routines (see 3.5).

The time settings of the 4.55-millisecond (receive) clock and the 9.1-millisecond (transmit) clock should be periodically checked and adjusted.

6.3.1 Clock Adjustments

The time period of the clocks can be monitored and adjusted (if required) while running teletype diagnostics or by using the following procedure:

Place the computer in the step mode.

Extend the DM 113 circuit board if the presence of other DATA 620/i option boards prevents direct access to the oscillator circuitry.

Place teletype motor ON/OFF switch in the OFF position.

4.55-Millisecond Clock. Temporary jumper the clock input to ground at pin 8 of IC26. The clock will now run until the SYSTEM RESET switch on the computer console is pressed.

Scope setup: Set TIME to 1 or 2 milliseconds/centimeter
Set SYNC to positive internal
Set voltage amplitude to (.2) 2 or (.5) 5 volts/centimeter

Place the oscilloscope probe at the junction of C7 and C8 near the bottom rear of the TC. Adjust the oscilloscope to obtain one full square wave period. This should have a time duration of 4.55 milliseconds. If the observed full square wave period is not 4.55 milliseconds, adjust the bottom (R6) trimmer potentiometer until the correct period is obtained; then switch the scope to observe 22 periods. Twenty-two periods should take exactly 100 milliseconds. This will allow fine timing adjustment (see figure 4-11). After completing adjustment, the 4.55-millisecond clock can be stopped by removing the temporary jumper (if still installed) and pressing SYSTEM RESET switch.

For troubleshooting purposes, the DM 113 circuit board can be extended by using a standard DATA 620/i board extender.

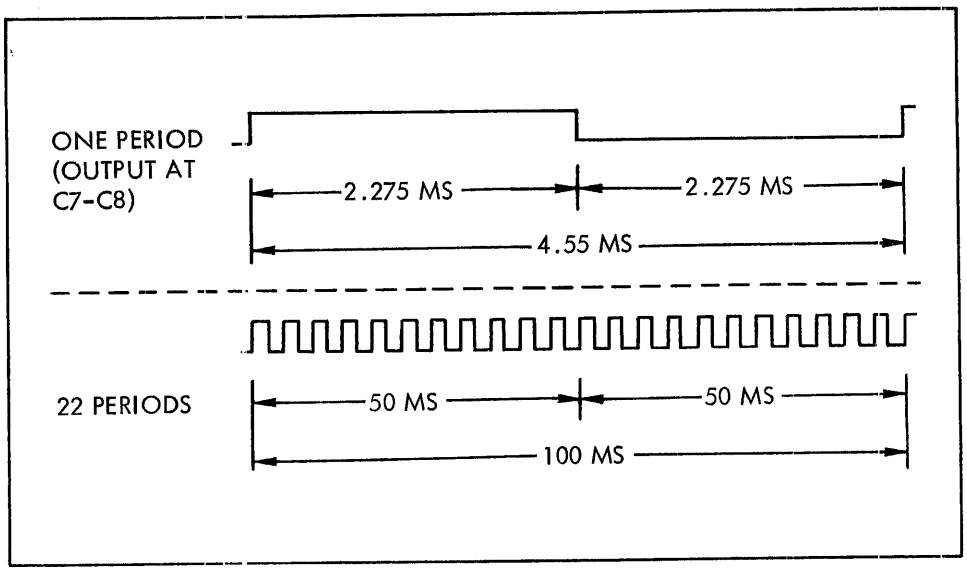


Figure 4-11. Scope Pattern of Waveforms for 4.55-Millisecond Clock Adjustment

9.1-millisecond clock. Temporarily jumper the clock input to ground at pin 9 of IC 10 or at TC pin 33. The clock will run until the SYSTEM RESET switch on the computer is pressed.

Oscilloscope setup: Set TIME to 1, 2, 5, or 10 millisecond/centimeter
Set SYNC to positive internal

Set voltage amplitude to (.2) 2 or (.5) 5 volts/centimeter.

Place the oscilloscope probe at the junction of C3 and C4 near the top rear of TC or at TC, pin 35. Adjust oscilloscope to obtain one full square wave period. This should have a time duration of 9.1 milliseconds. If the observed square wave period is not 9.1 milliseconds, adjust the top (R1) trimmer potentiometer until the correct period is obtained; then switch the scope time base to observe 11 periods. Eleven periods should take exactly 100 milliseconds.

Switch the scope to observe 22 periods. This should take exactly 200 milliseconds. Switching the scope to observe many periods is important because adjustment of the 9.1-millisecond clock is critical. Observing many periods allows the adjustment to be more accurately timed (see figure 4-12). After completing adjustment, the clock can be stopped by removing the enabling jumper (if still installed) and by pressing the SYSTEM RESET switch on the computer console.

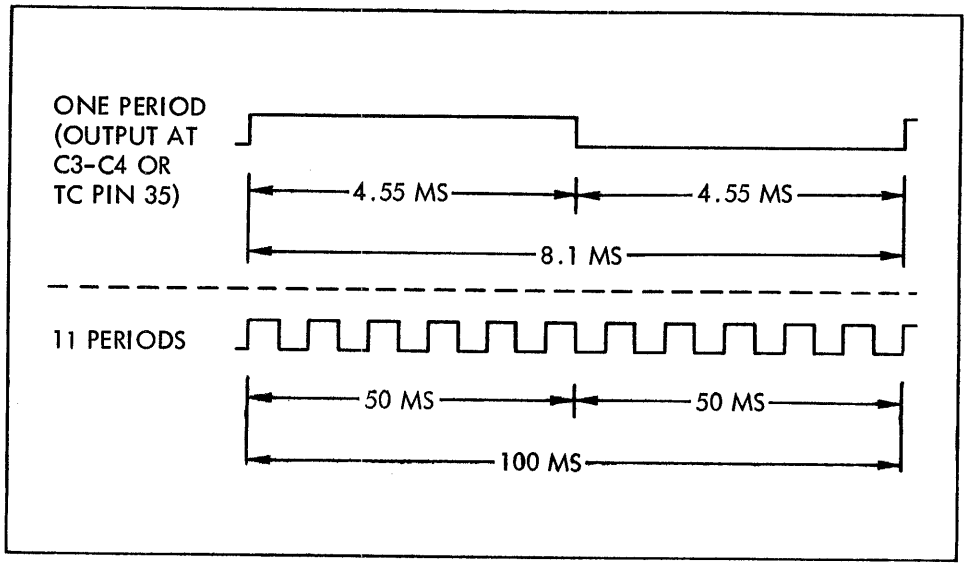


Figure 4-12. Scope Pattern of Waveforms for 9.1-Millisecond Clock Adjustment

6.4 TROUBLESHOOTING PROCEDURES

The teletype units are normally trouble-free and require little attention; however, if faulty operation occurs, the following troubleshooting procedures are suggested.

6.4.1 Visual

Inspect for broken belts, loose cams or components, loose or poorly seated connectors, blown fuses or burned out components.

> **NOTE**
>
> The teletype casework is cast, and therefore somewhat fragile. Care should be taken when removing and reinstalling it.

6.4.2 Garbling

The following are possible sources of intermittent character change (printing or sending wrong characters):

Teletype	Incorrect power supply output.
Teletype	Incorrect motor speed.
Teletype	Incorrect range adjustment.
TC	Incorrect 9.1 or 4.55-millisecond clock frequency (see 6.3).
Teletype-TC	Incorrect loop current (too low or too high).

6.4.3 Motor Speed Check

The teletype character output rate must be 100 milliseconds per character. The motor speed, which is not adjustable can be checked as follows:

Check RDDX (IC26/pin 9) of DM113 (see drawing 91D0005 sheet 1 of 4) with an oscilloscope. Set oscilloscope SYNC to positive internal and set scope time to 10 or 20 milliseconds/centimeter.

Now hold down the RUBOUT and REPEAT keys on the teletype keyboard. Adjust scope to observe RDDX waveform. RDDX should set on every start bit and remain set until stop bit time; resetting on each new start bit. The time from set to set should be exactly 100 milliseconds. Switch scope to observe that 10 characters occur each second. If single character time is off by more than two milliseconds, the teletype motor may require change, overhaul, readjustment or other maintenance.

6.4.4 Range Adjustment

The teletype receive section has a compensating RANGE knob (model 35) or lever (model 33) that may require occasional adjustment. The purpose of range adjustment is to compensate for receive loop distortion and to position the receiving loop mechanism for optimum sampling of the incoming signal. Before attempting range adjustment, verify proper TC output character length (see 6.3).

Full range adjustment is from 0 to 120. Factory-modified teletype model 33-ASR optimum range adjustment is at or near the center; normally 60 to 65. If range adjustment is required, send an alternate pattern such as period...from the central processor. Loosen the range set screw (model 33) or pull out range knob (model 35) and slowly vary the setting of the knob or lever while observing the pattern being printed. When the characters begin to change (garble), one end of the effective range has been reached. Note the location of this point on the adjustment knob or lever. Move the adjustment in the opposite direction. The printed characters should clear up and then begin to garble when the other end of the range is reached.

Note the position of this point on the adjustment knob or lever, and position the range knob or lever midway between the observed range limit points. Tighten down set screws, if applicable.

Range adjustment and motor speed should be checked if intermittent failures are occurring, or after any major overhaul is performed on the teletype.

6.4.5 Teletype-TC Interface Signal Checks

Teletype-TC interface signal through relays K1 and K2 can be checked as follows:

Receive (K1 relay)

Attach scope reference to DM113 pin 113 and put scope probe on DM113 pin 112. The bit pattern observed on the scope should be essentially rectangular and free from distortion when the TC is receiving for the teletype.

Send (K2 relay)

Attach scope reference to DM113 pin 113 and put scope probe on DM113 pin 114. The bit pattern observed on the scope should be essentially rectangular and free from distortion when TC is sending to the teletype.

6.4.6 Voltage Measurements (33-ASR)

Approximate voltages for model 33-ASR teletype-TC interface at DM113 module pins 112, 113 and 114 can be checked with the method shown in table 4-5.

6.4.7 Teletype Cable (see section 7)

Table 4-5. Model 33-ASR TTY-TC Interface Voltages

Setup Conditions		DC Meter Connections		Approximate Voltage
DATA 620/i Power	TTY Line Mode	Common	Hot	
ON (K2 relay contacts closed)	On-line	Pin 113 (green wire at J31)	Pin 114 (yellow wire at J31)	0 vdc
		Pin 113 (green wire at J31)	Pin 112 (violet wire at J31)	45 vdc
	Off-line	Pin 113 (green wire at J31)	Pin 112 (violet wire at J31)	35 vdc
OFF (K2 relay contacts open)	On-line (teletype running open)	Pin 113 (green wire at J31)	Pin 114 (yellow wire at J31)	0-2 vdc
		Pin 113 (green wire at J31)	Pin 112 (violet wire at J31)	42 vdc
	Off-line	Pin 113 (green wire at J31)	Pin 112 (violet wire at J31)	42 vdc

6.4.8 Troubleshooting Check List

If the TC and teletype are not operating:

Check voltages.
Check cable connections and board setting.
Check that 9.1 and 4.55-millisecond clock oscillators start and stop.
Check that relays K1 and K2 are energized in normal static nonoperating condition. If not, the source of the problem may be the teletype, the relay loop supply, or a relay.

If the TC and teletype have intermittent problems:

Check voltages.
Check cable connections and board seating.
Remove and inspect TC board for loose components, poor solder connections, and wrong value components.
Check the 9.1 and 4.55-millisecond clock timing and if necessary adjust.
Observe the send and receive signals across the teletype relay lines.

NOTE

The K1 and K2 relays occasionally fail. Symptoms are excessive contact bounce and degraded make–break characteristics. Loop current provided by the teletype may be too high or too low. Loop current should be checked and should be about 20 milliamperes.

6.4.9 Test Points

The following are some common test points on the TC module DM113:

Section	Term	Test Points	Note
Output	WRDY	Pin 33	See synchronization points also.
	9.1-millisecond clock	C3 and C4	
	9.1-millisecond clock	Pin 35	(WCKX) inversion of 9.1-millisecond clock.
	WSCP	IC25-8	
	Output to teletype	IC44-8 or K2-2	Drives K2 relay.
	Output to teletype	Across pins 114 and 113	Send loop to teletype.
	WLDX	IC39-8	
	WSIX-	IC10-13 or IC43-5	See synchronization points also.

Section	Term	Test Points	Note
Output	W00X- WRIX-	IC26-6 IC40-6	
Computer-TC	DAXX FRYX DRYX SERX- DROX DTIX EXCX EBRX	Pin 100 Pin 5 Pin 3 Pin 2 IC41-9 IC41-12 IC4-6 Pin 29	
Input	RRDY- 4.55 ms clock RSCP RRCP- RECX- RDDX RRCX TTRX Input from teletype	Pin 101 C7 and C8 IC25-6 IC40-8 IC36-9 IC26-9 IC31-9 IC43-11 K1-4	See S.C. points also. See S.C. points also. Input data from teletype. Driven from teletype.
Input	Input from teletype	Across pins 113 and 112	Receive loop from teletype.

6.4.10 Synchronization points

The following are some good synchronization points on the TC module (DM113):

Output to teletype = Start bit of output character begins when WSIX- becomes true.

Sync = (positive) on IC10-13.

Input from teletype = start bit of input character begins when RDDX becomes true.

Sync = (positive) on IC26-9.

Input to teletype = Input charzcter sequence can begin any time after RRDY becomes true.

Sync = (negative) on pin 101 (RRDY-)

Output from computer = Output loading can begin any time after WRDY becomes true.

Sync = (positive) on pin 33.

All (DM 113) pin assignments are found on sheet 3 of 4 of the teletype controller logic diagram in volume 2 of the 620/i Maintenance Manual.

7.1 TELETYPE CABLES - ASR-33

The cable used for TC to ASR-33 Interface runs from the S connector plugs in the teletype to J31 at the rear of the central processor.

The S (connector) is labled as (2) in the teletype unit and is located at the right rear, top row, second connector from the right.

The cable drawing is 0100001. The cable is normally 20 feet long, 3 leads in a cable. Colors shown in the chart below are normally used.

TC-Pin	P31 (J31) End	(Color)	P2 (S Conn) End	Function
113	1	Violet	9	Receive
112	2	Green	6	Return
114	3	Yellow	8	Send

The teletype (S connector) end of the cable has two other wires in it. Pins 7, 4 and 5 are connected. These connections tie internal teletype leads together brought into the S connector plug as part of teletype wiring.

Note that both ends of the cable are keyed to insure proper mating.

7.2 TELETYPE CABLE - ASR AND KSR-35

The cable between model-35 teletype and TC runs from J31 at the rear of the central processor to a power terminal block in the teletype.

This terminal block is located at the right lower rear of the cabinet behind the teletype printing mechanism.

The cable drawing used is also 01D001, but cable is modified: plug (P2) is cut off and the three leads are directly wired to the teletype at the power terminal block: (TB).

TC-Pin	P31 (J31) End	Color	TTY-TB	Function
112	1	Violet	Terminal 4	Receive
113	2	Green	Terminal 5	Return
114	3	Yellow	Terminal 7	Send

NOTE

The teletype cable is normally installed at the teletype by Varian Data Machines before customer delivery.

The model-33 teletype requires about three amperes of ac power.

The model-35 teletype requires about six amperes of ac power.

CHAPTER 5
TIMING WAVEFORMS

5.1 INTRODUCTION

This chapter contains timing waveforms for various instructions and operations executed by the DATA 620/i.

Each page includes an identification of the instructions or operation involved, followed by waveforms of individual signals associated with the instructions or operation.

5.2 CONTENTS

Table 5-1 lists instructions and operations for which waveforms are provided in this chapter.

Table 5-1
Waveform Index

INSTRUCTION: START SEQUENCE

MNEMONIC:(NONE)

OCTAL CODE:(NONE)

SINGLE - WORD ADDRESSABLE

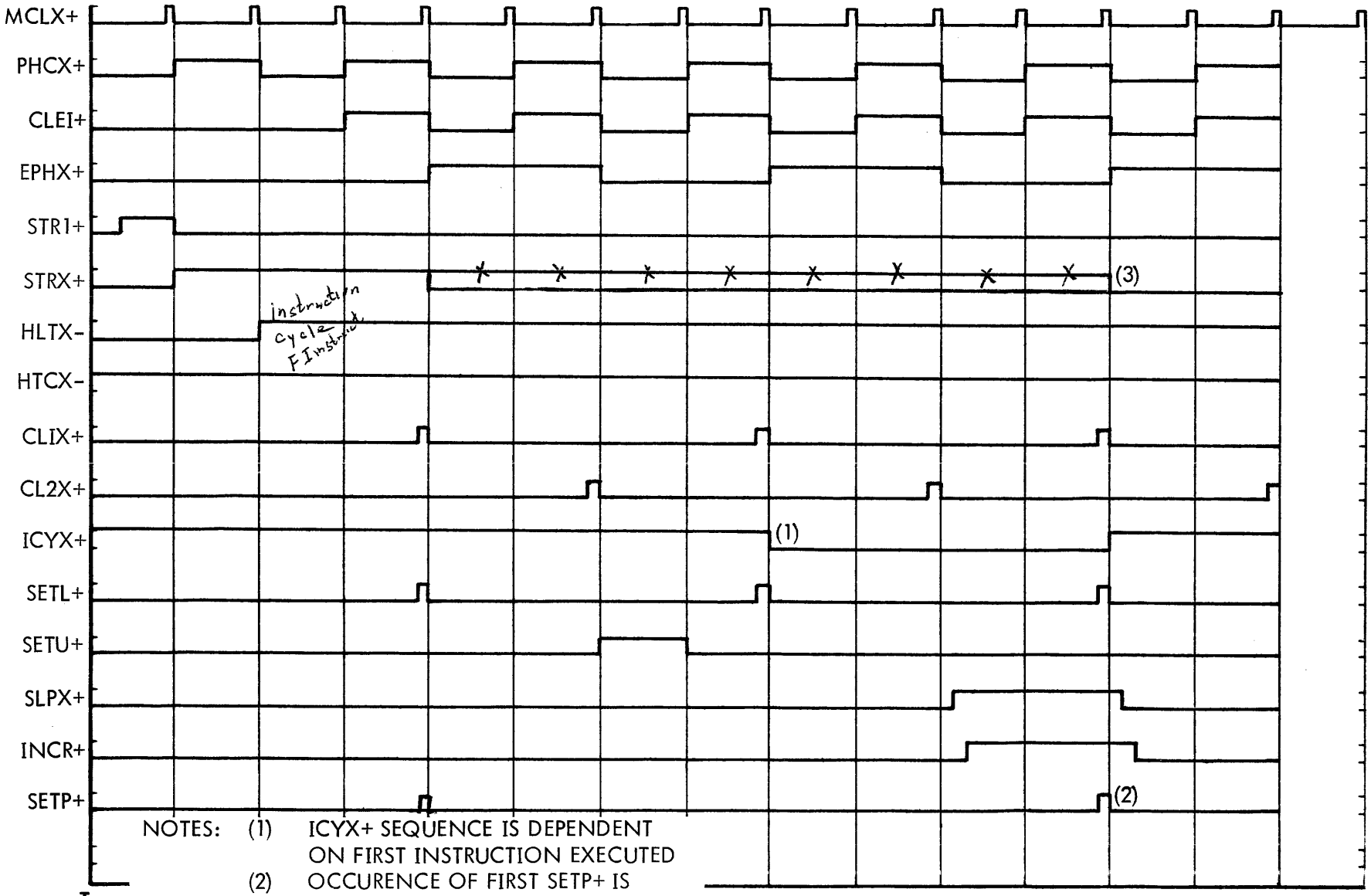
DIRECT-ADDRESSABLE

Logic levels: True = +5 vdc.

False = 0 vdc.

U reg = 0

Time between master clock pulses = 450 nanoseconds.



NOTES:

(1) ICYX+ SEQUENCE IS DEPENDENT ON FIRST INSTRUCTION EXECUTED

(2) OCCURENCE OF FIRST SETP+ IS DEPENDENT ON INSTRUCTION

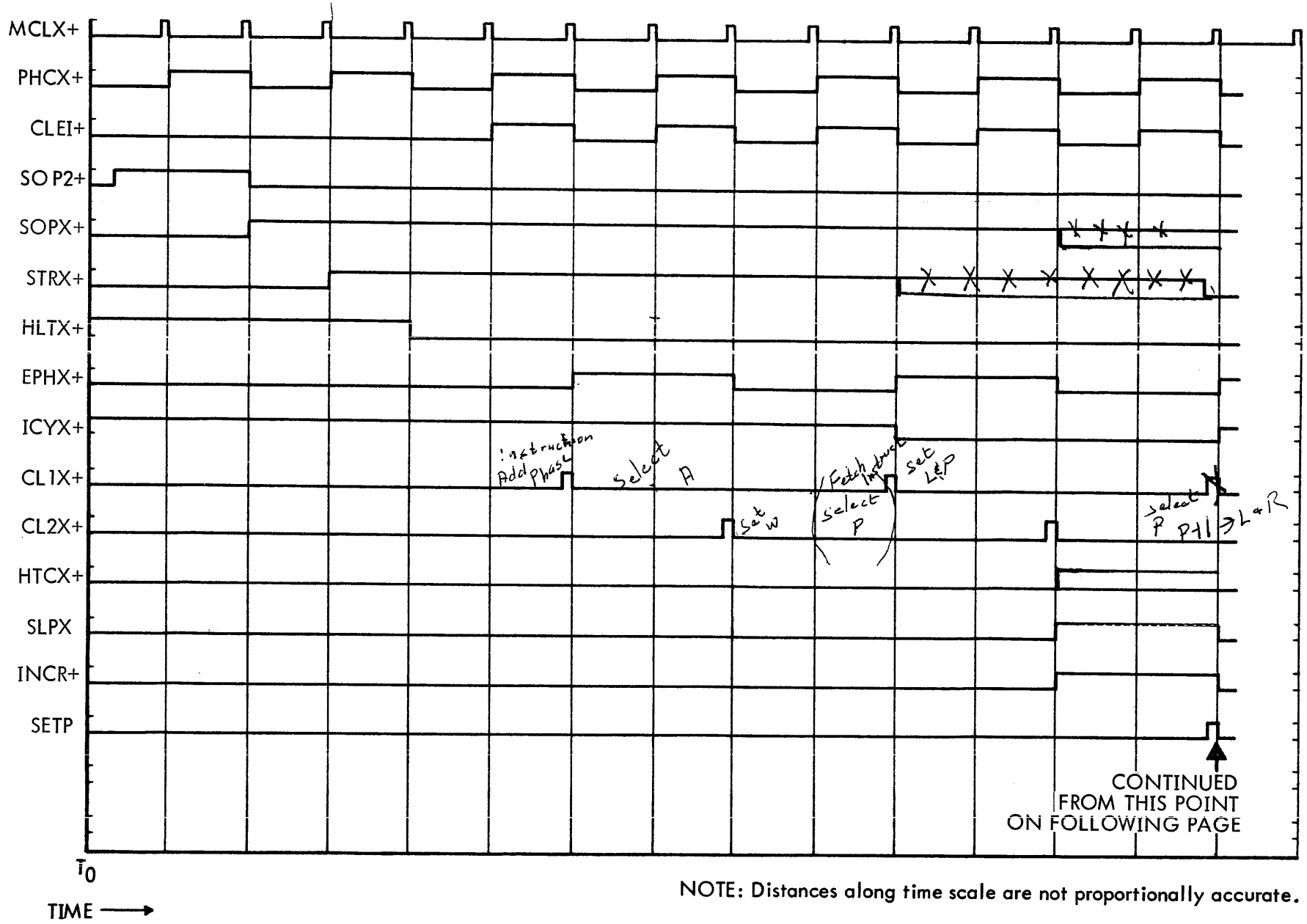
(3) RESETTING OF STRX+ IS DEPENDENT ON FIRST SETP+

NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: STEP SEQUENCE
MNEMONIC:(NONE)
OCTAL CODE:(NONE)
SINGLE - WORD ADDRESSABLE SHOWN

Logic levels: True = +5 vdc.
False = 0 vdc.

U Reg = STO A Direct
Time between master clock pulses = 450 nanoseconds.

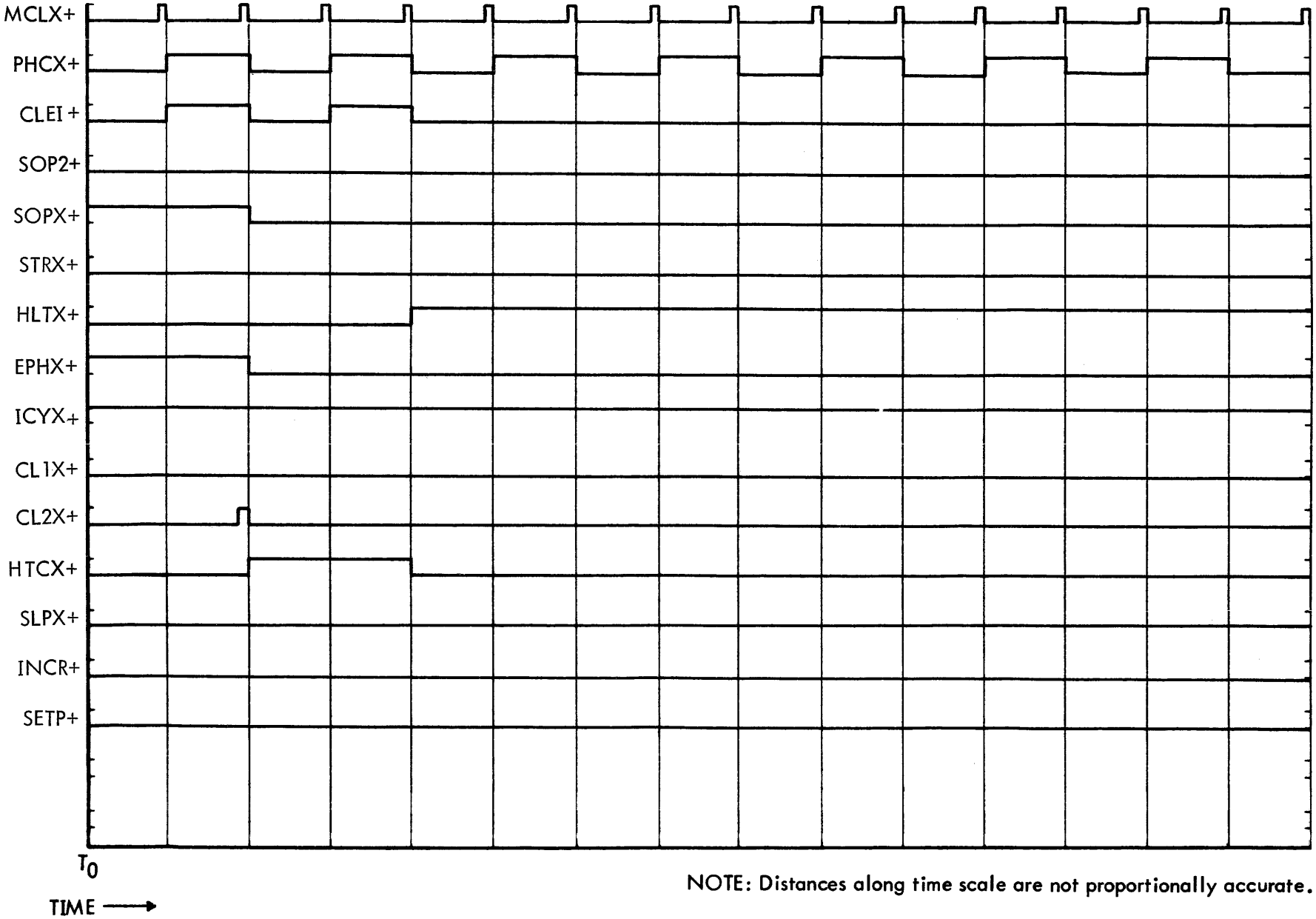


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: STEP SEQUENCE (CONT'D)
MNEMONIC: (NONE)
OCTAL CODE: (NONE)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

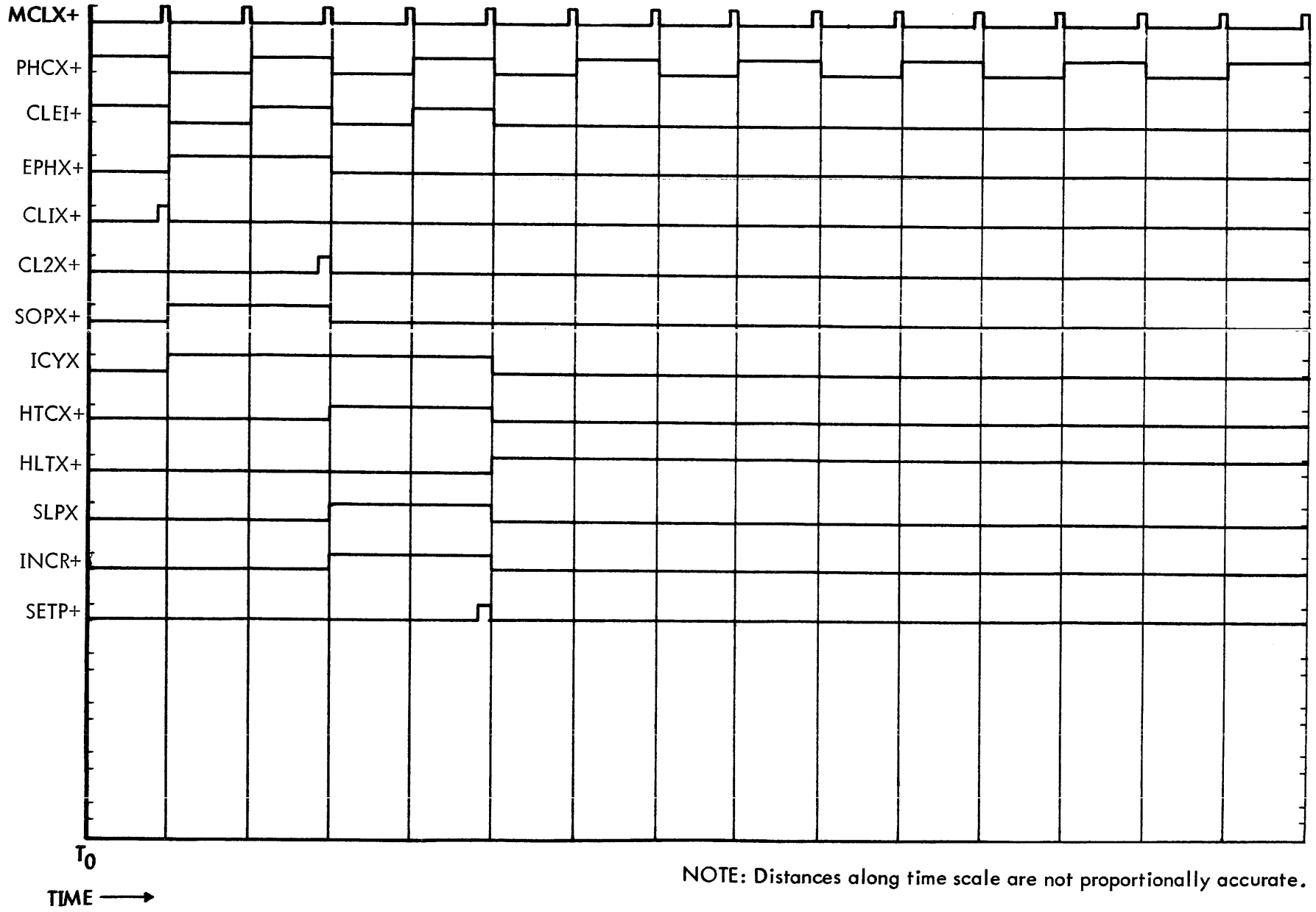


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: MANUAL HALT SEQUENCE
MNEMONIC: (NONE)
OCTAL CODE: (NONE)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

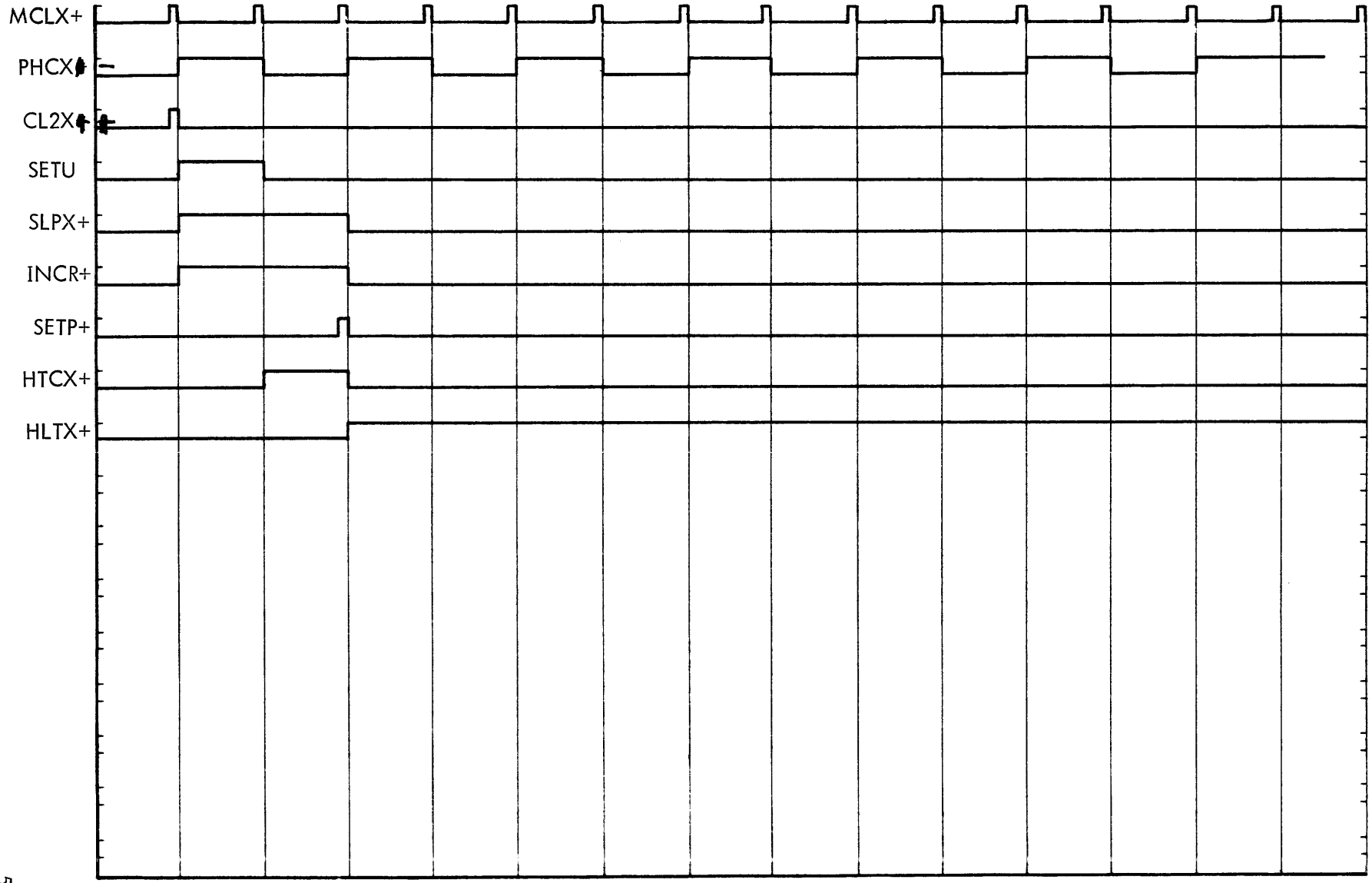


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: PROGRAM HALT SEQUENCE
MNEMONIC: HLT
OCTAL CODE: 000XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

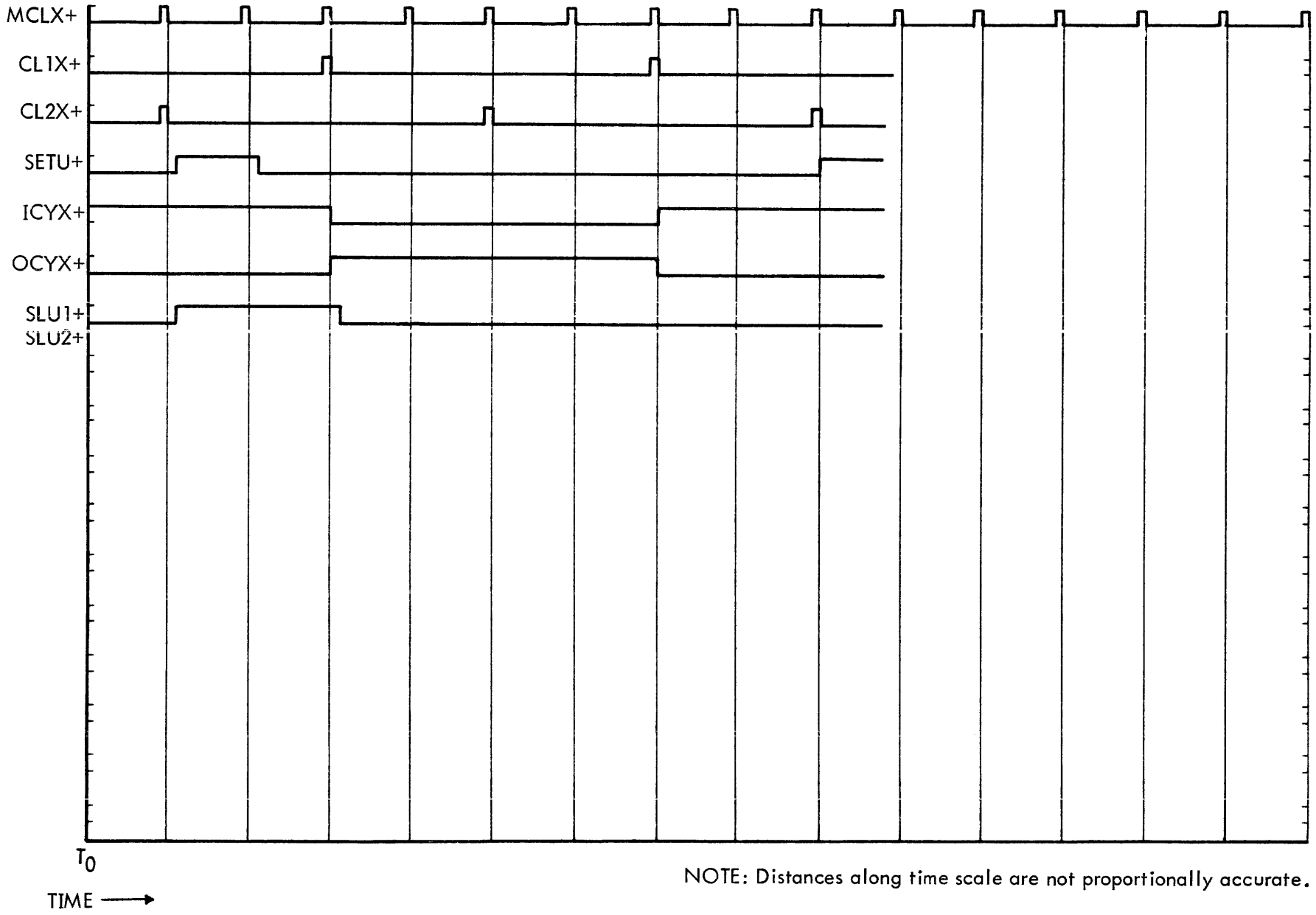


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: OPERAND ADDRESSING (DIRECT)
MNEMONIC: LDA DIRECT IS TYPICAL
OCTAL CODE: 01ZXXX (Z = $0XXX_2$)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

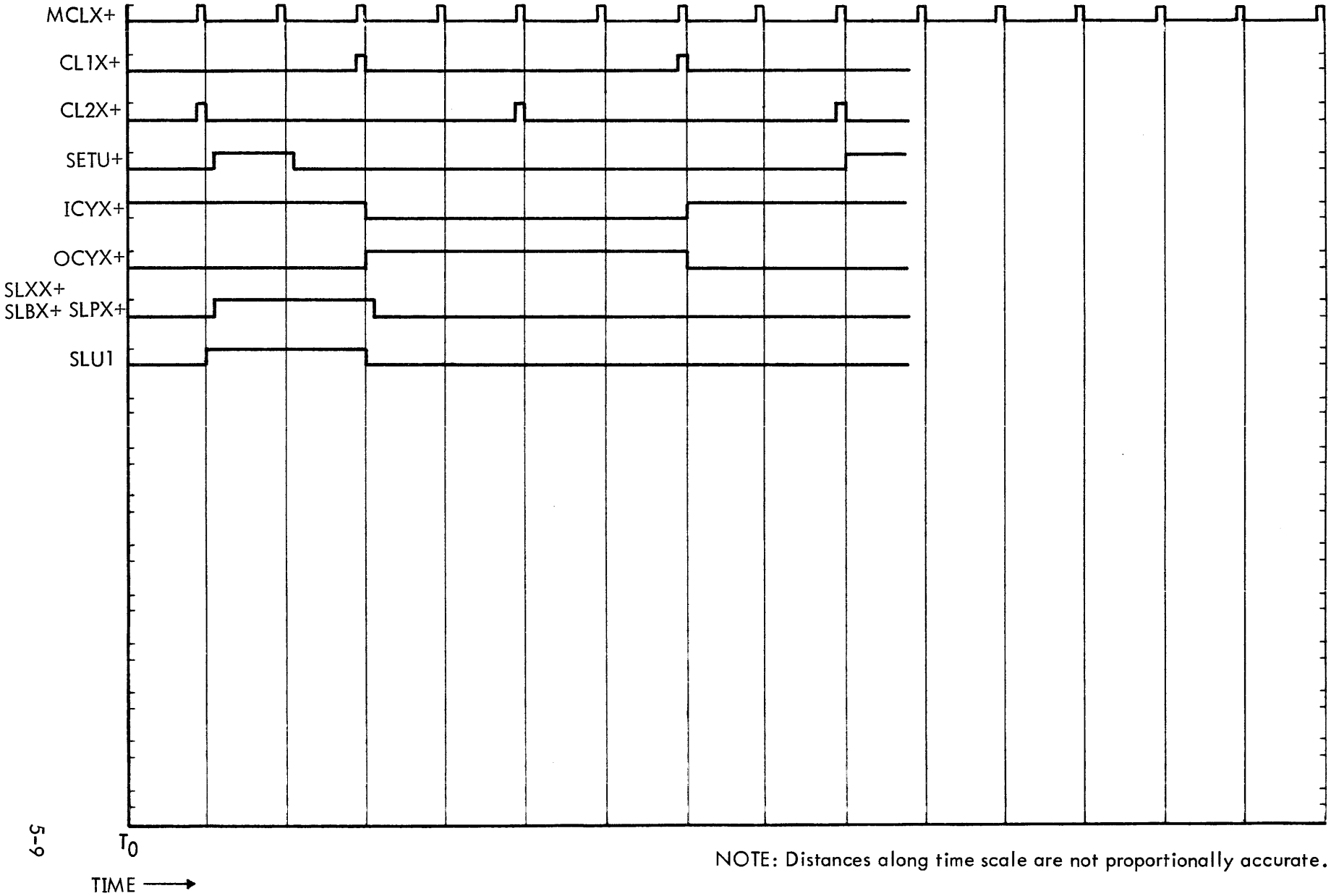


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INDEX ADDRESSING
MNEMONIC: LDA INDEXED IS TYPICAL
OCTAL CODE: 015XXX (INDEX X)
016XXX (INDEX B)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

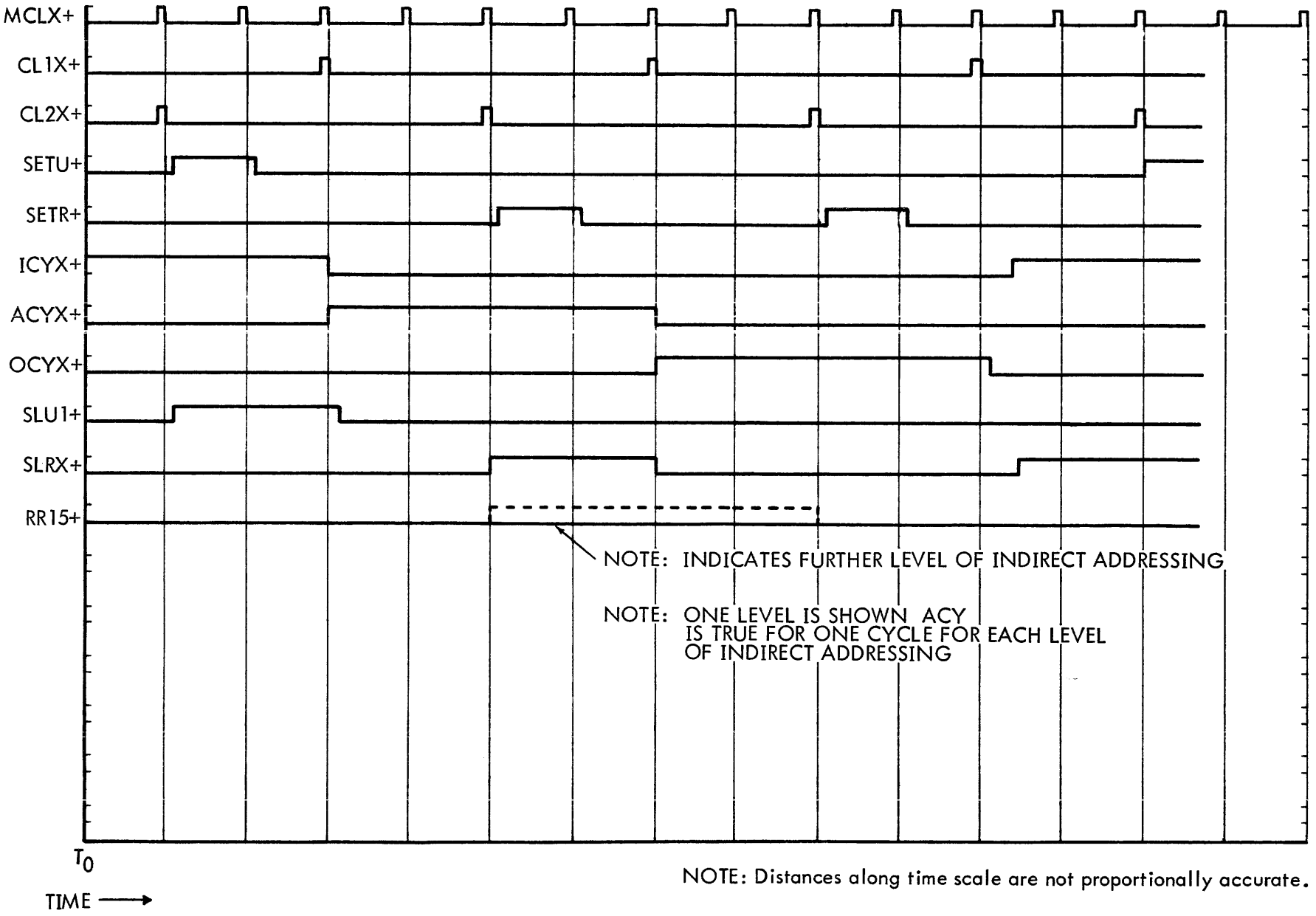


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INDIRECT ADDRESSING
MNEMONIC: LDA
OCTAL CODE: 017000
} LOAD A REG INDIRECT IS TYPICAL

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.



NOTE: Distances along time scale are not proportionally accurate.

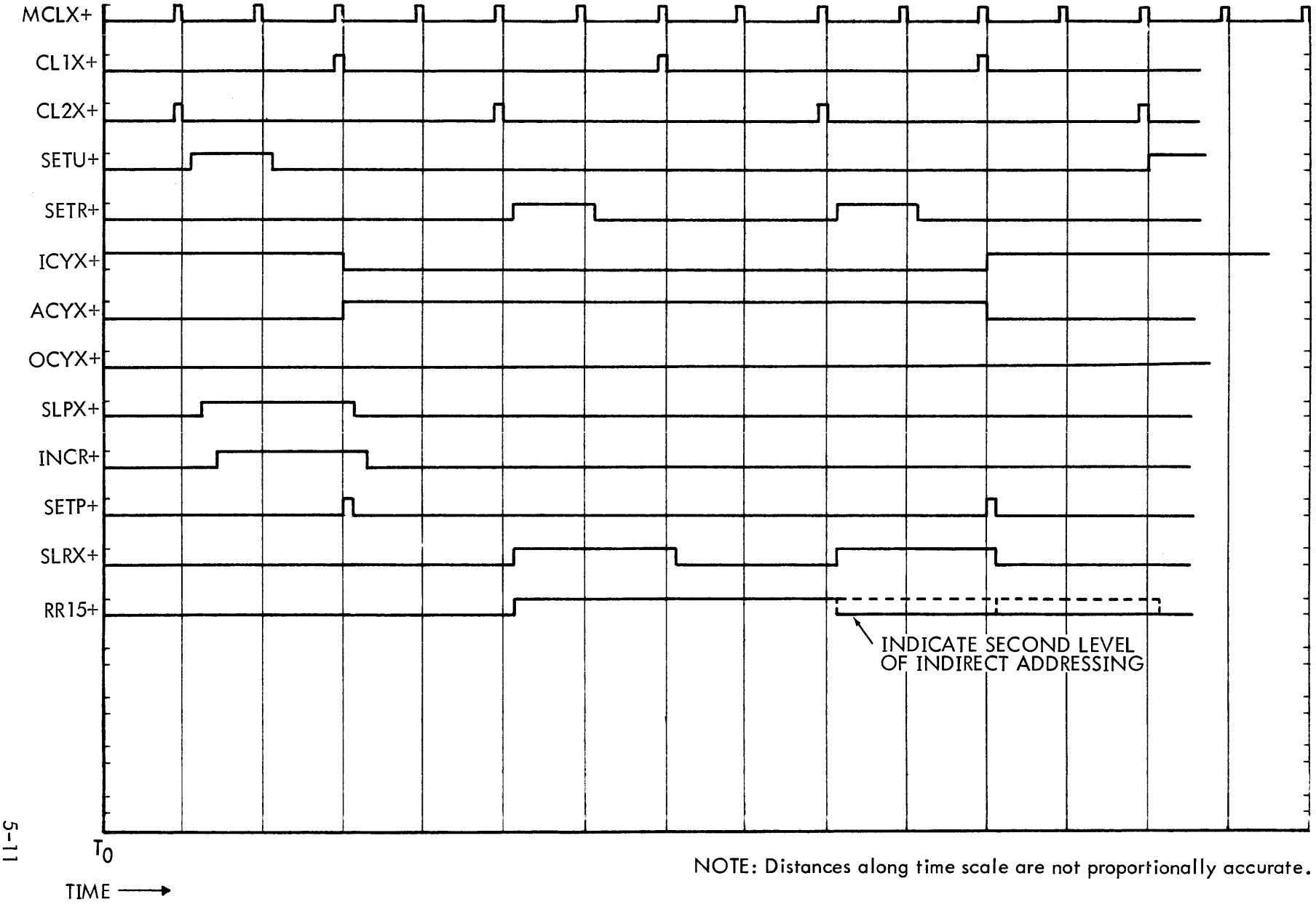
INSTRUCTION:	INDIRECT ADDRESSING DOUBLE-WORD INSTRUCTION
MNEMONIC:	JMP
OCTAL CODE:	001000 1XXXXX

JMP UNCOND IS TYPICAL

Logic levels: True = +5 vdc.

False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

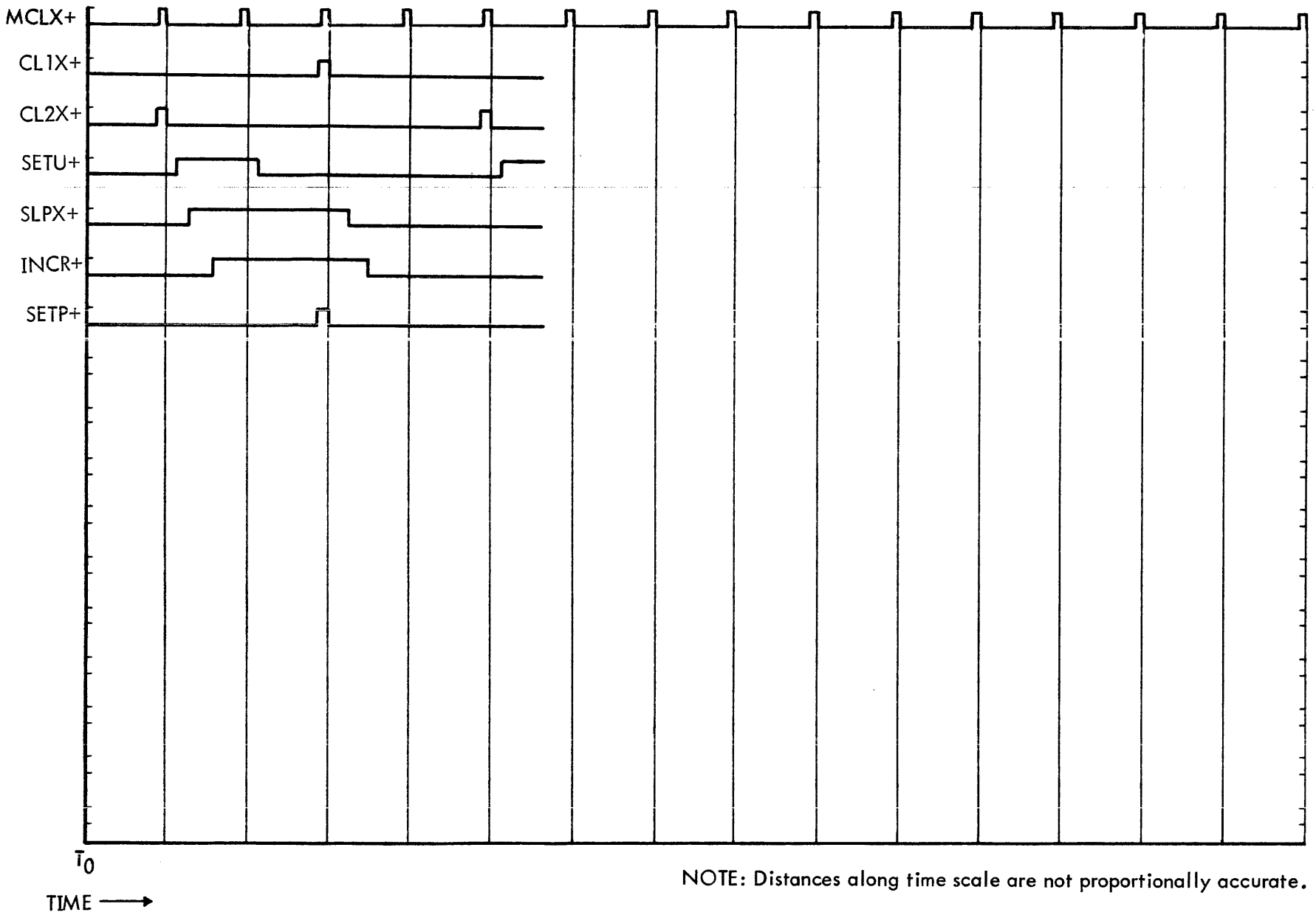


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: NO OPERATION
MNEMONIC: NOP
OCTAL CODE: 005000

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

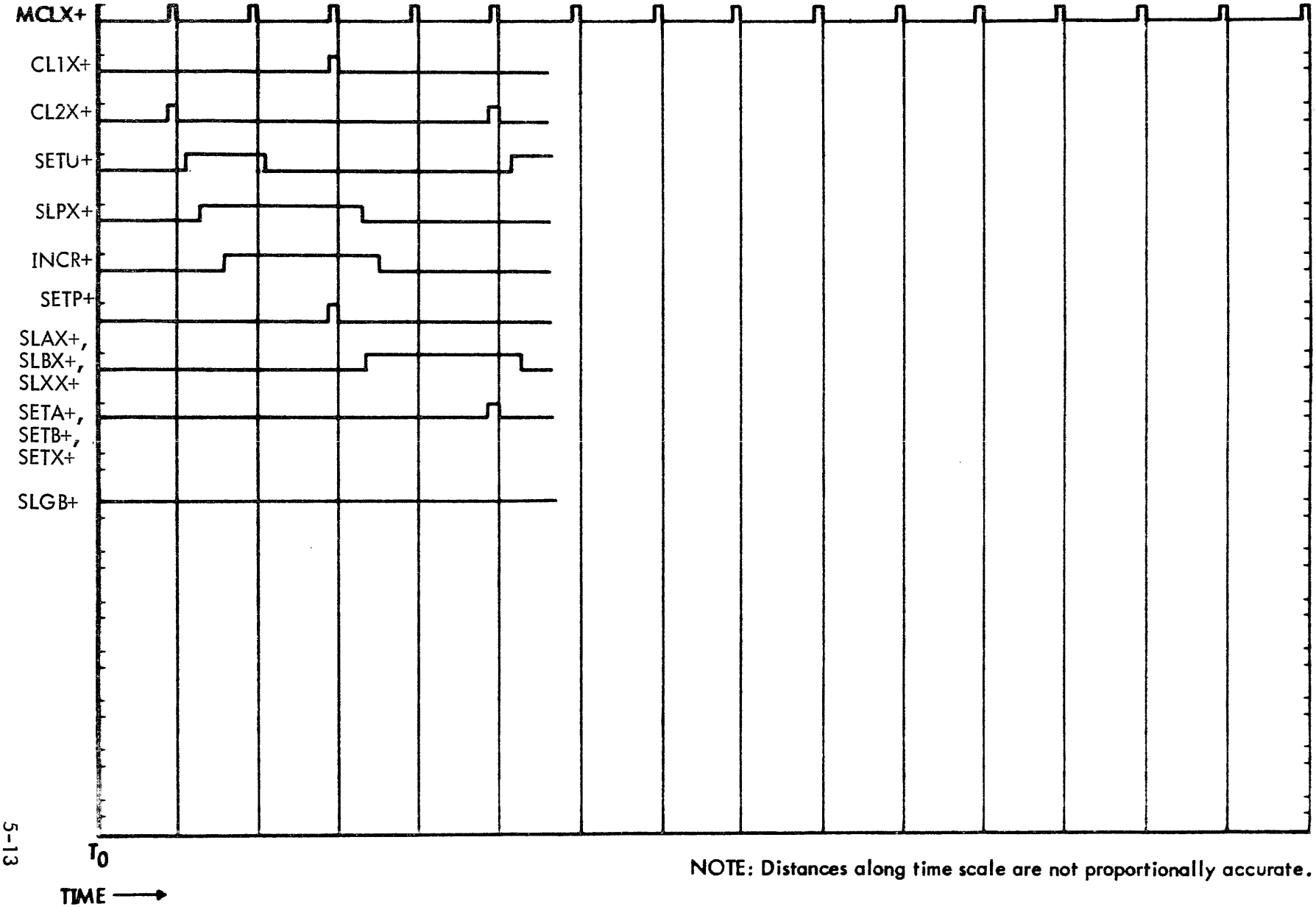


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: REGISTER CHANGE (TRANSFER)
MNEMONIC: T - - (SEE SYSTEM REFERENCE MANUAL)
OCTAL CODE: 0050XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

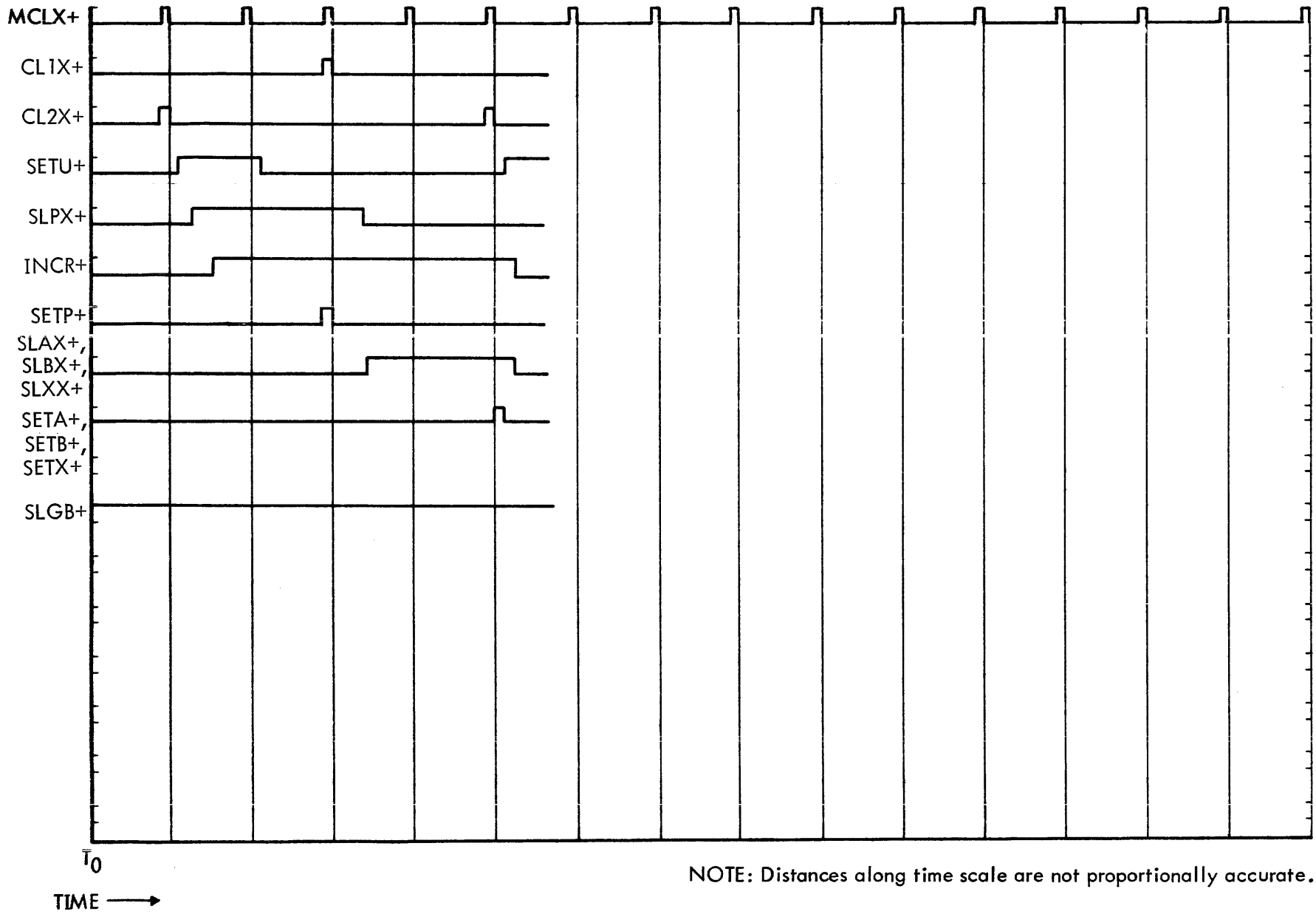


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: REGISTER CHANGE (INCREMENT)
MNEMONIC: IAR, IBR, IXR
OCTAL CODE: 0051XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

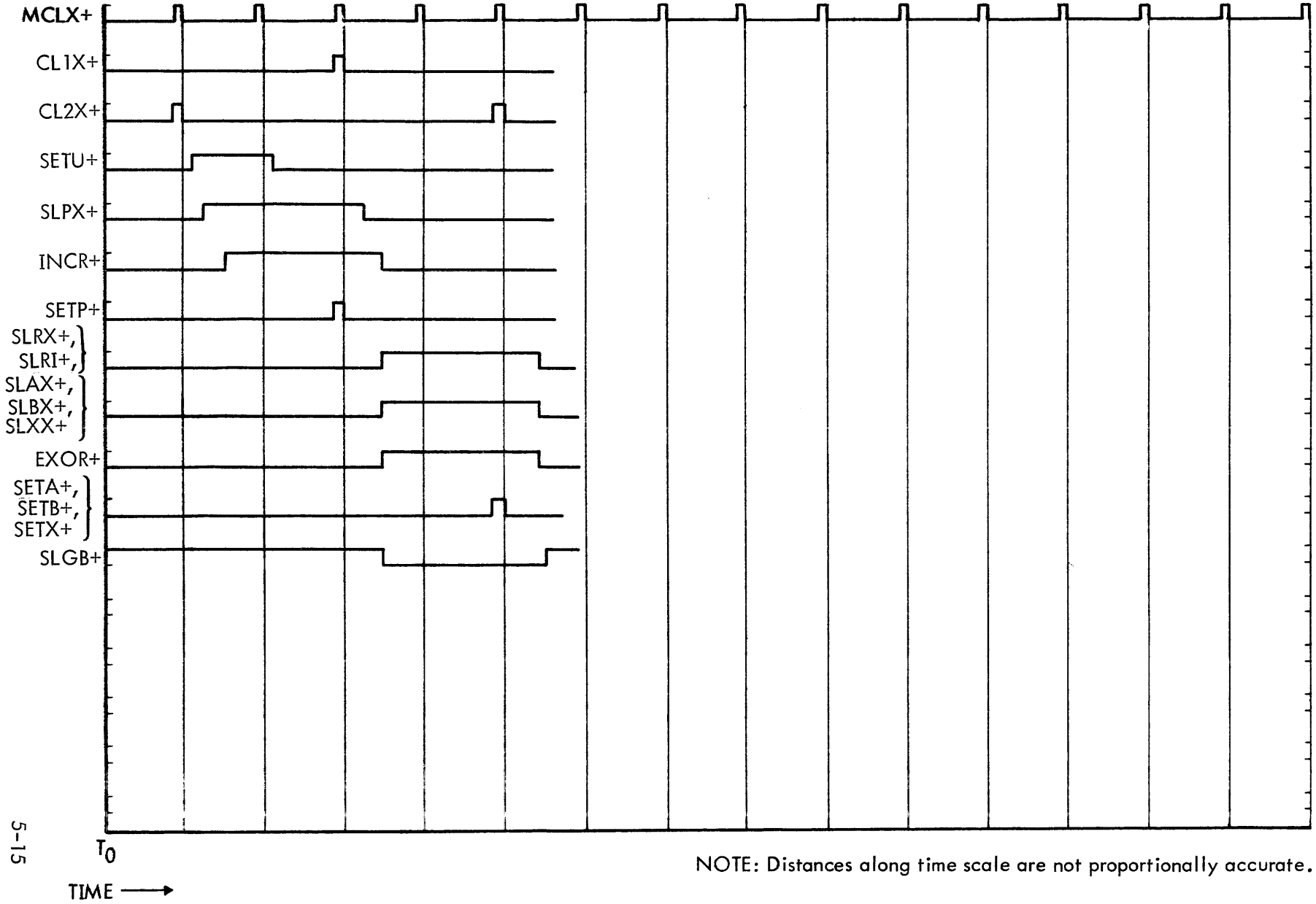


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: REGISTER CHANGE (COMPLEMENT)
MNEMONIC: CPA, CPB, CPX
OCTAL CODE: 005211, 005222, 005244

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

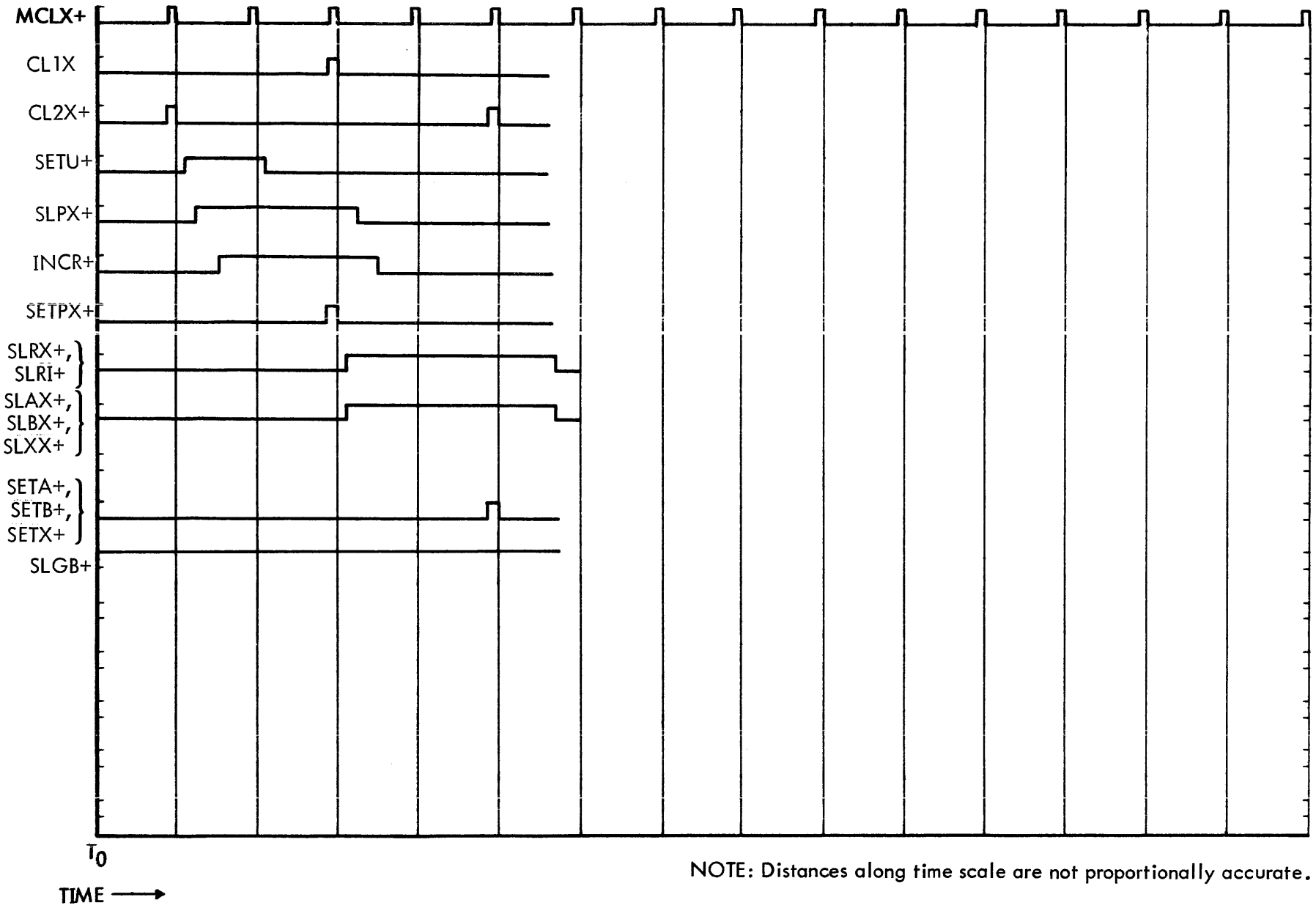


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: REGISTER CHANGE (DECREMENT)
MNEMONIC: DAR, DBR, DXR
OCTAL CODE: 005311 005322, 005344

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

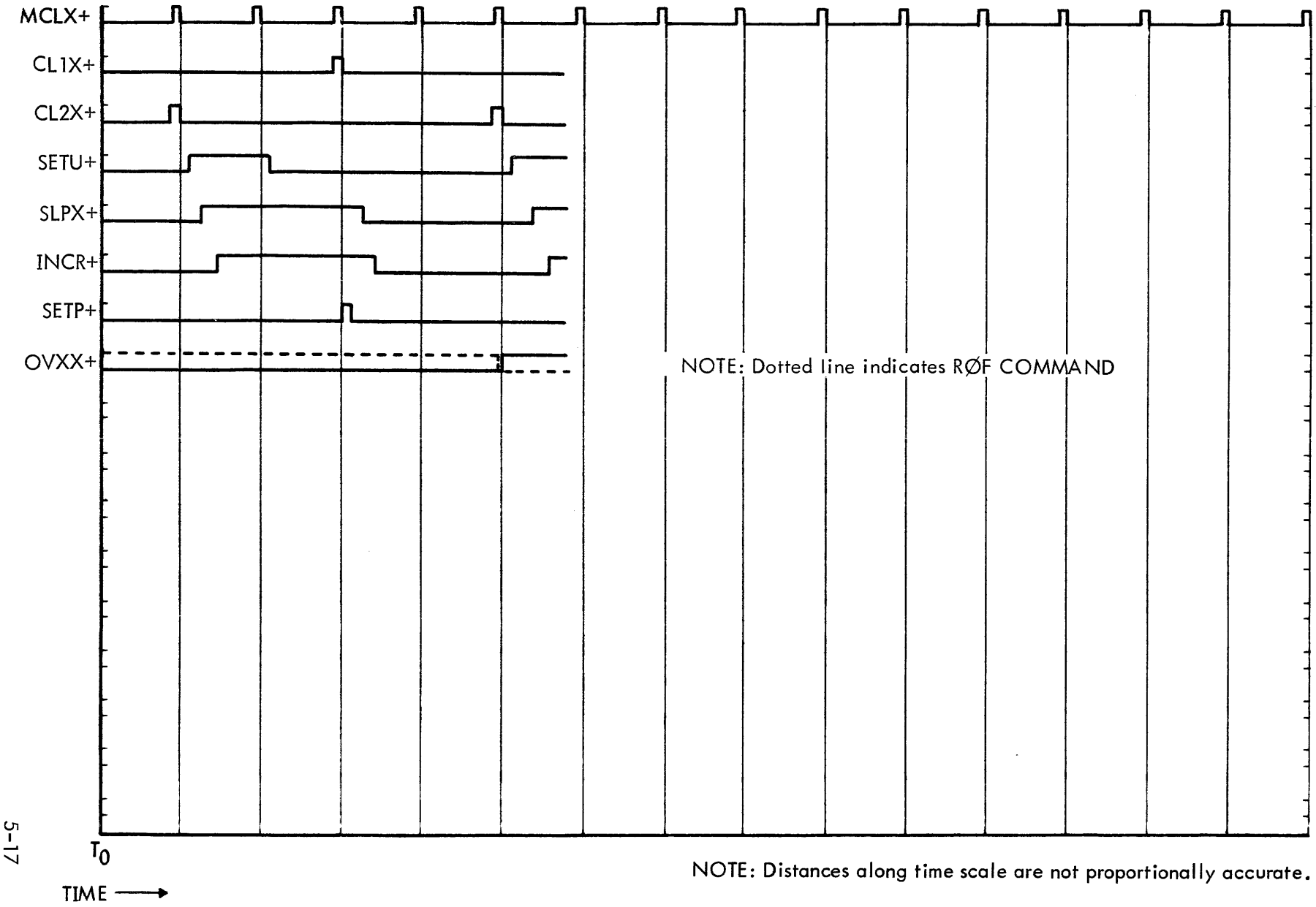


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SET/RESET OVERFLOW
MNEMONIC: SOF/ROF
OCTAL CODE: 007401/007400

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

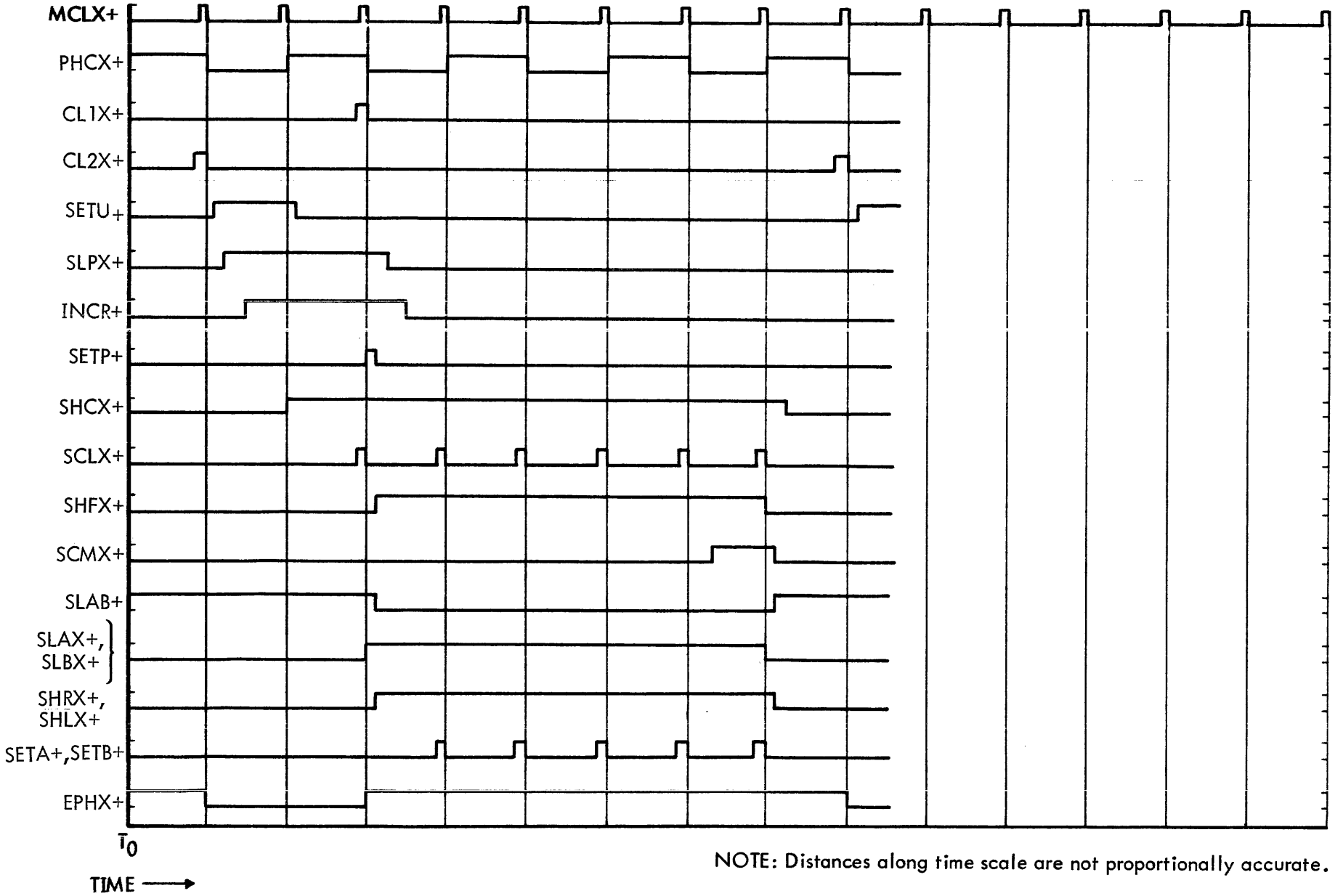


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SHIFT SINGLE REGISTER
MNEMONIC: LRLA
OCTAL CODE: 004245
} LOGICAL ROTATE LEFT A (5 PLACES) IS TYPICAL

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

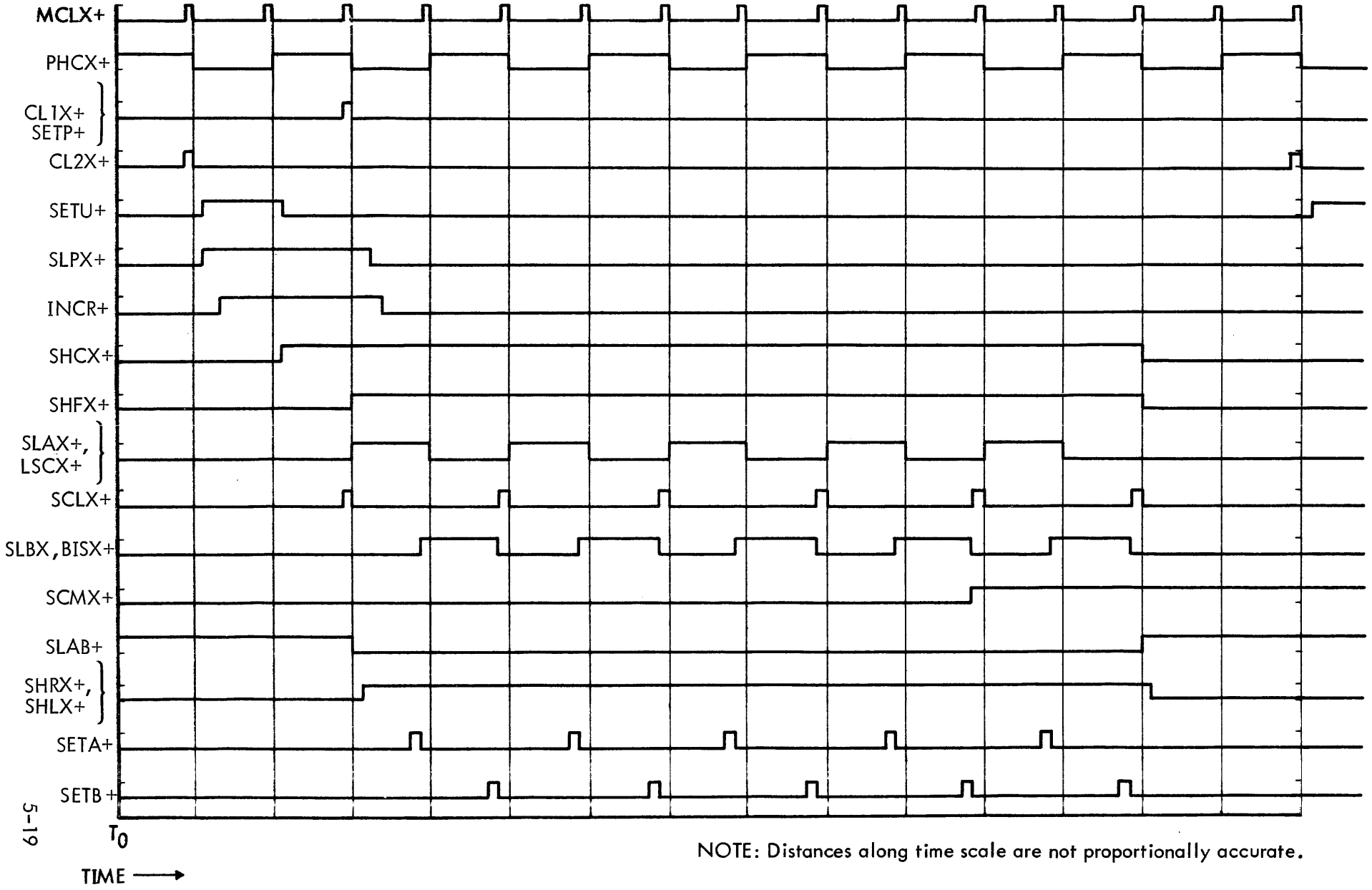


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SHIFT DOUBLE REGISTER
MNEMONIC: LLRL } LONG LOGICAL ROTATE LEFT (5 PLACES) IS TYPICAL
OCTAL CODE: 004445 }

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

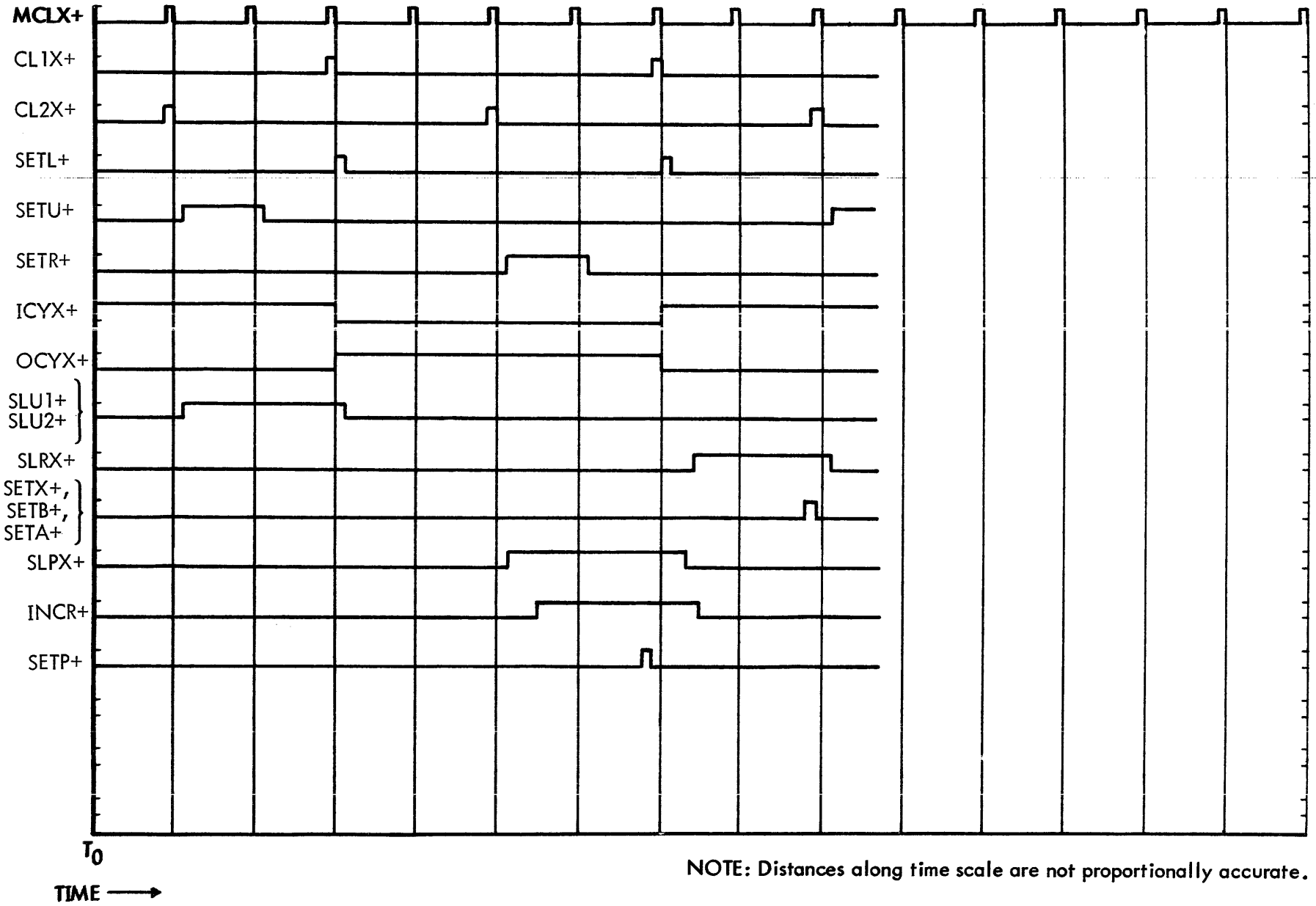


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: LOAD A (B,X) REGISTER
MNEMONIC: LDA (LDB,LDX)
OCTAL CODE: 010XXX (020XXX, 030XXX)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

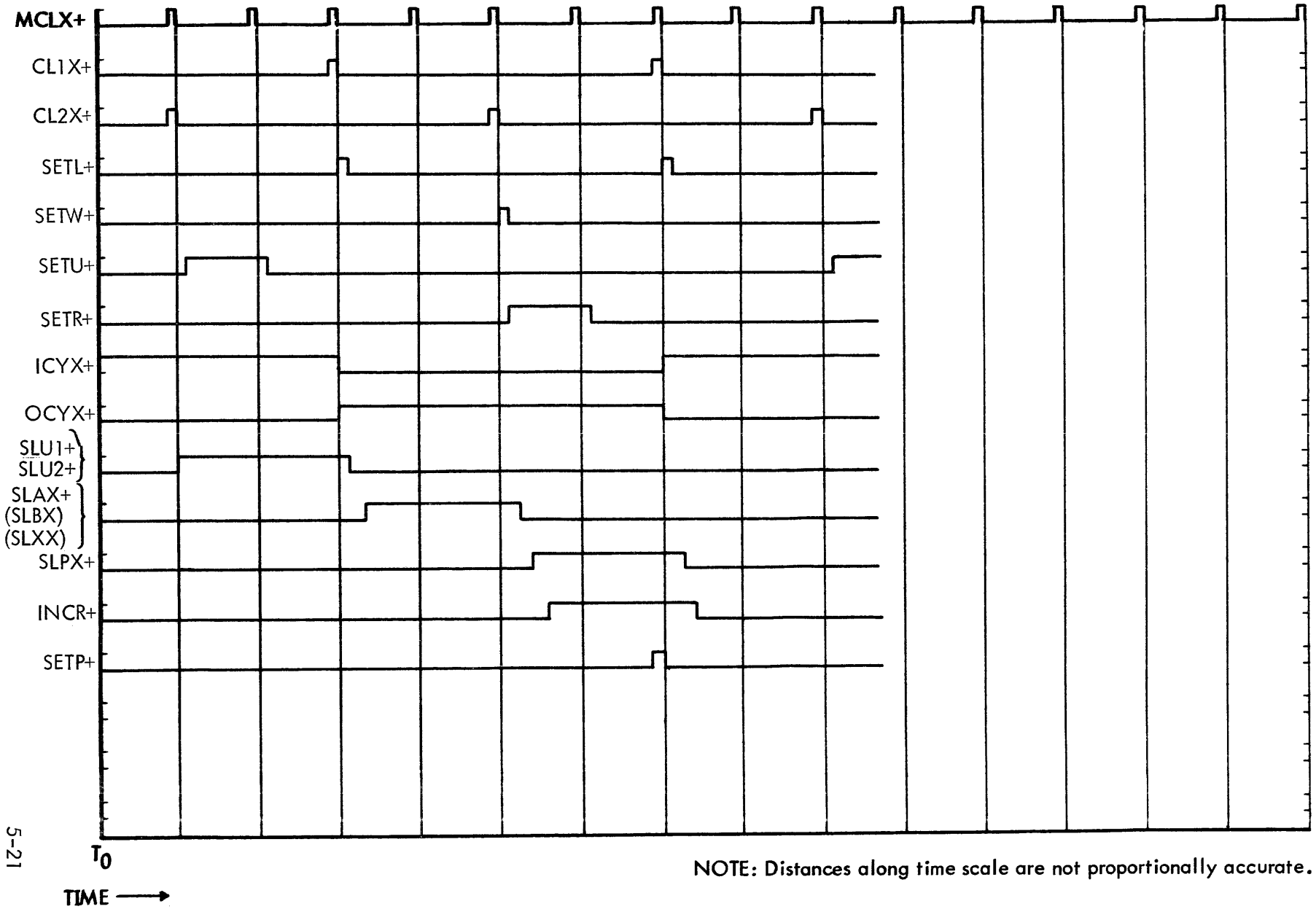


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: STORE A (B, X) REGISTER
MNEMONIC: STA (STB, STX)
OCTAL CODE: 050XXX (060XXX, 070XXX)

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

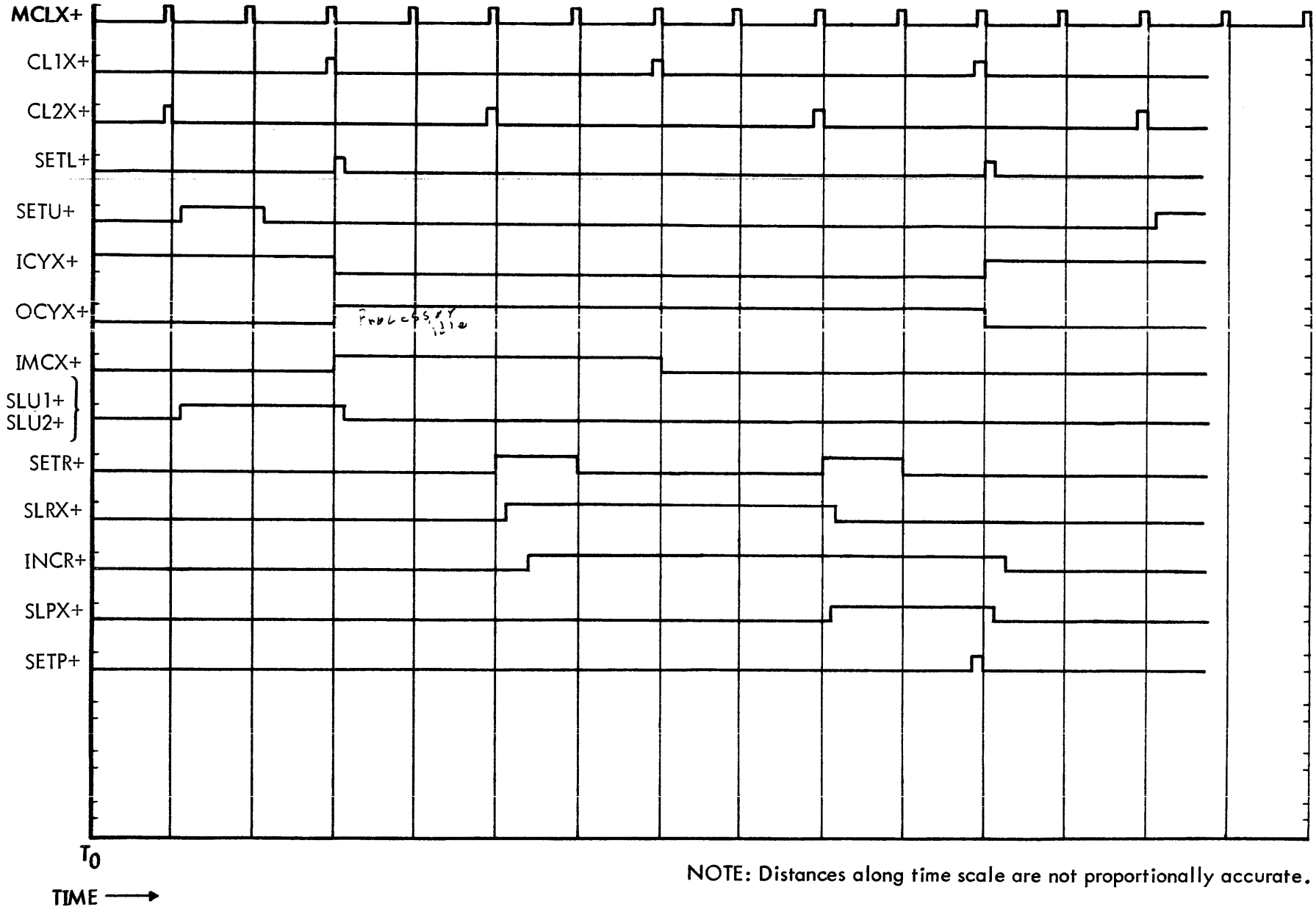


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INCREMENT AND REPLACE
MNEMONIC: INR
OCTAL CODE: 040XXX Direct

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

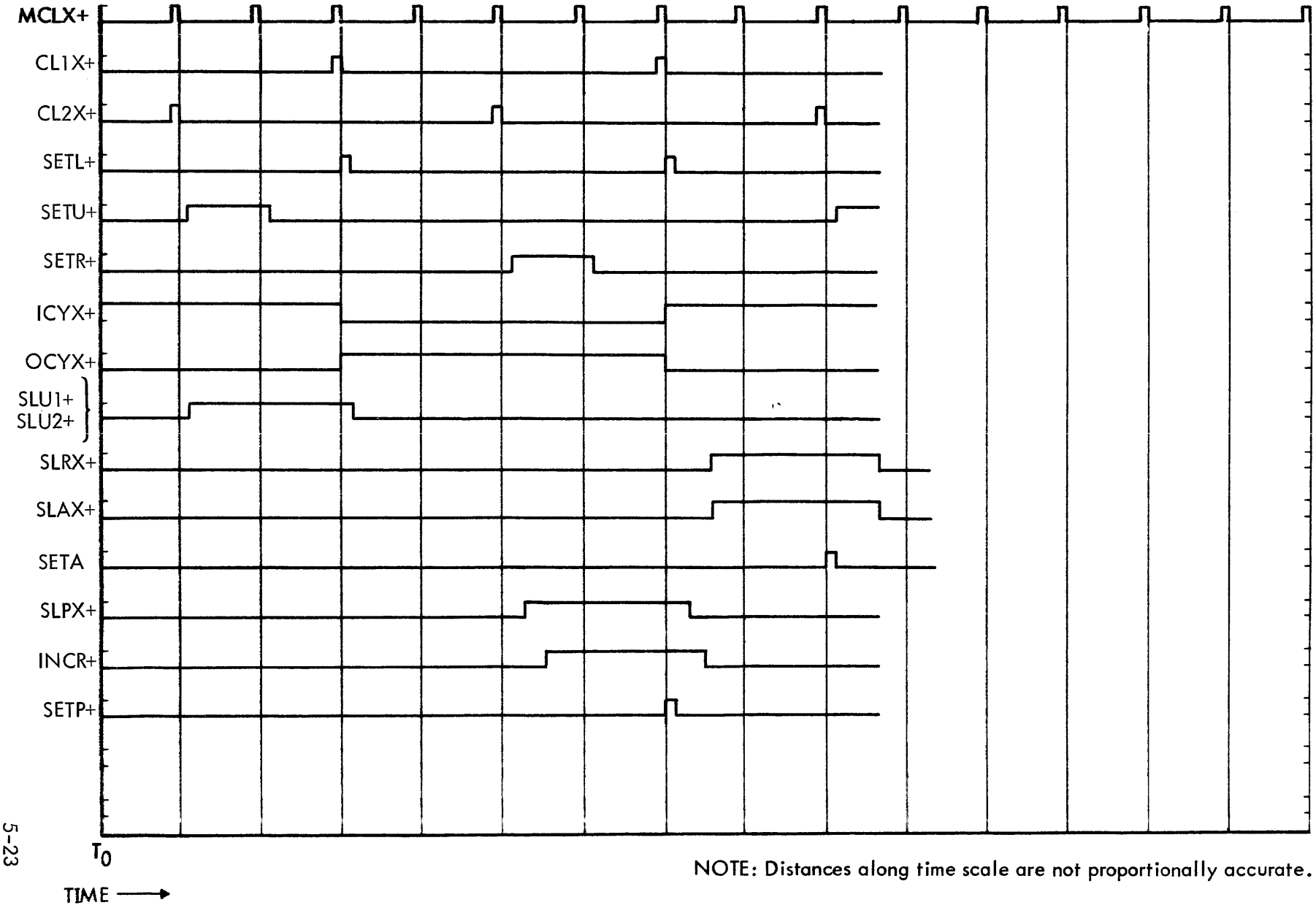


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: ADD TO A REGISTER
MNEMONIC: ADD
OCTAL CODE: 120XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

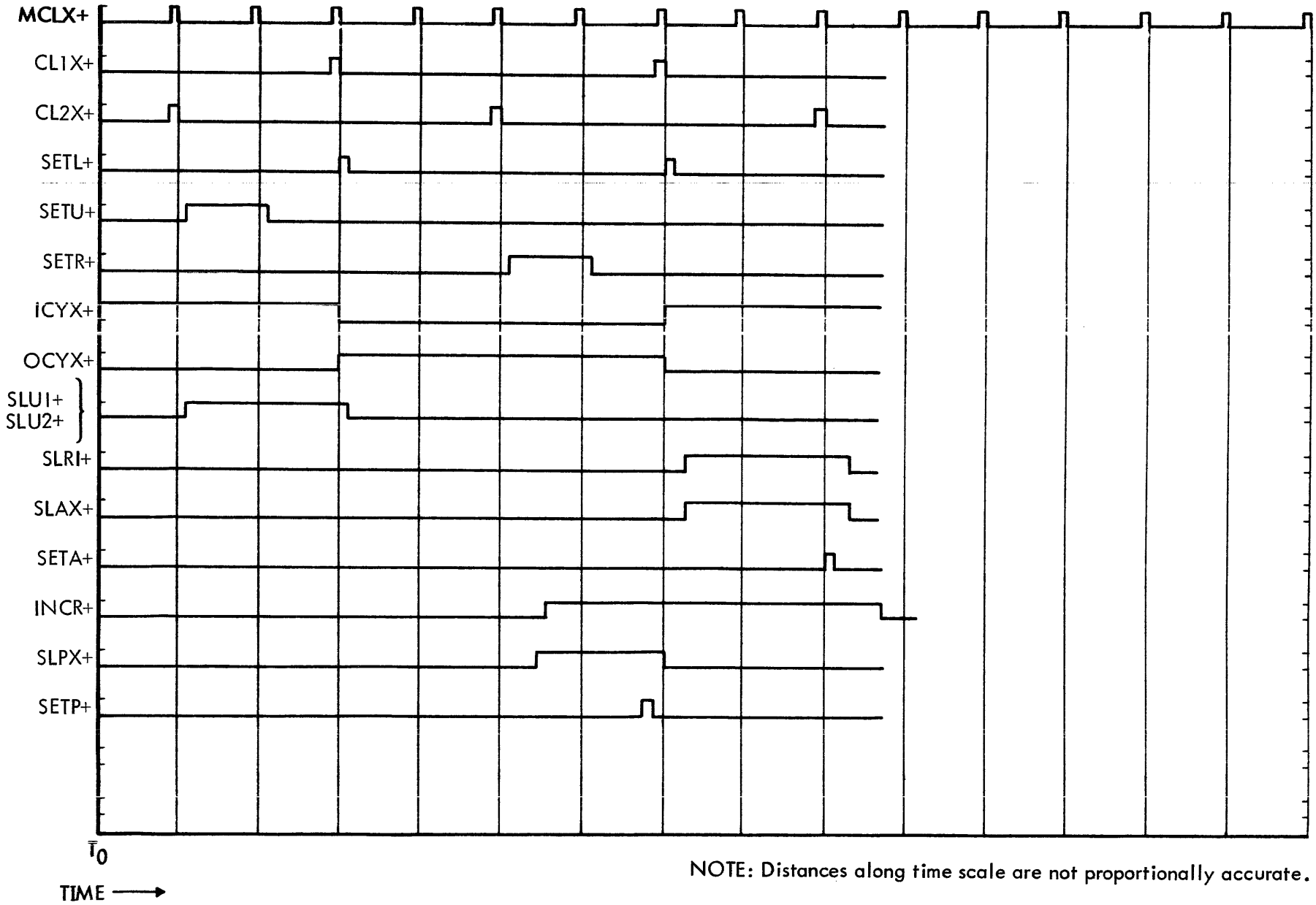


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SUBTRACT FROM A REGISTER
MNEMONIC: SUB
OCTAL CODE: 140XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

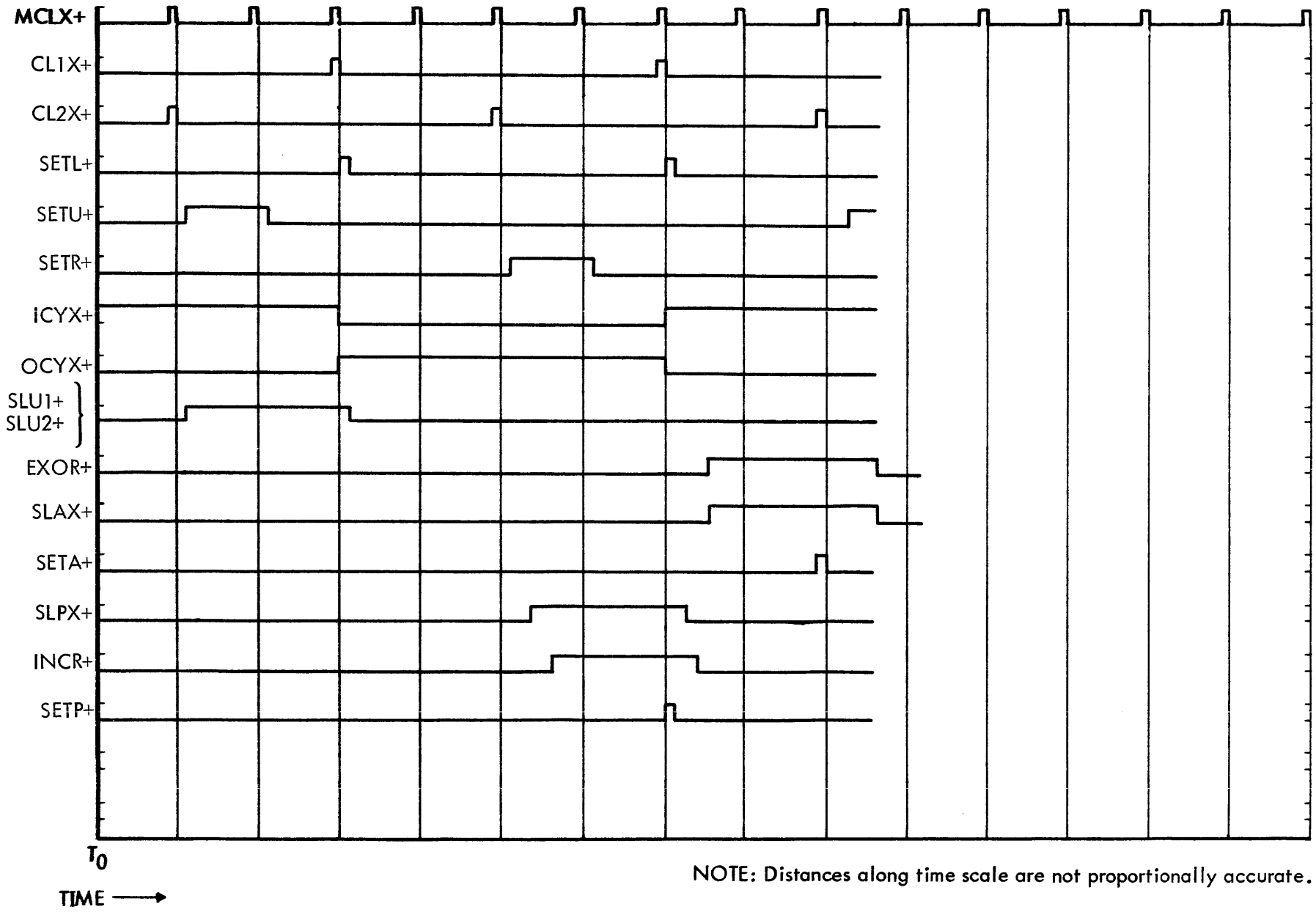


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: EXCLUSIVE OR TO A REGISTER
MNEMONIC: ERA
OCTAL CODE: 130XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

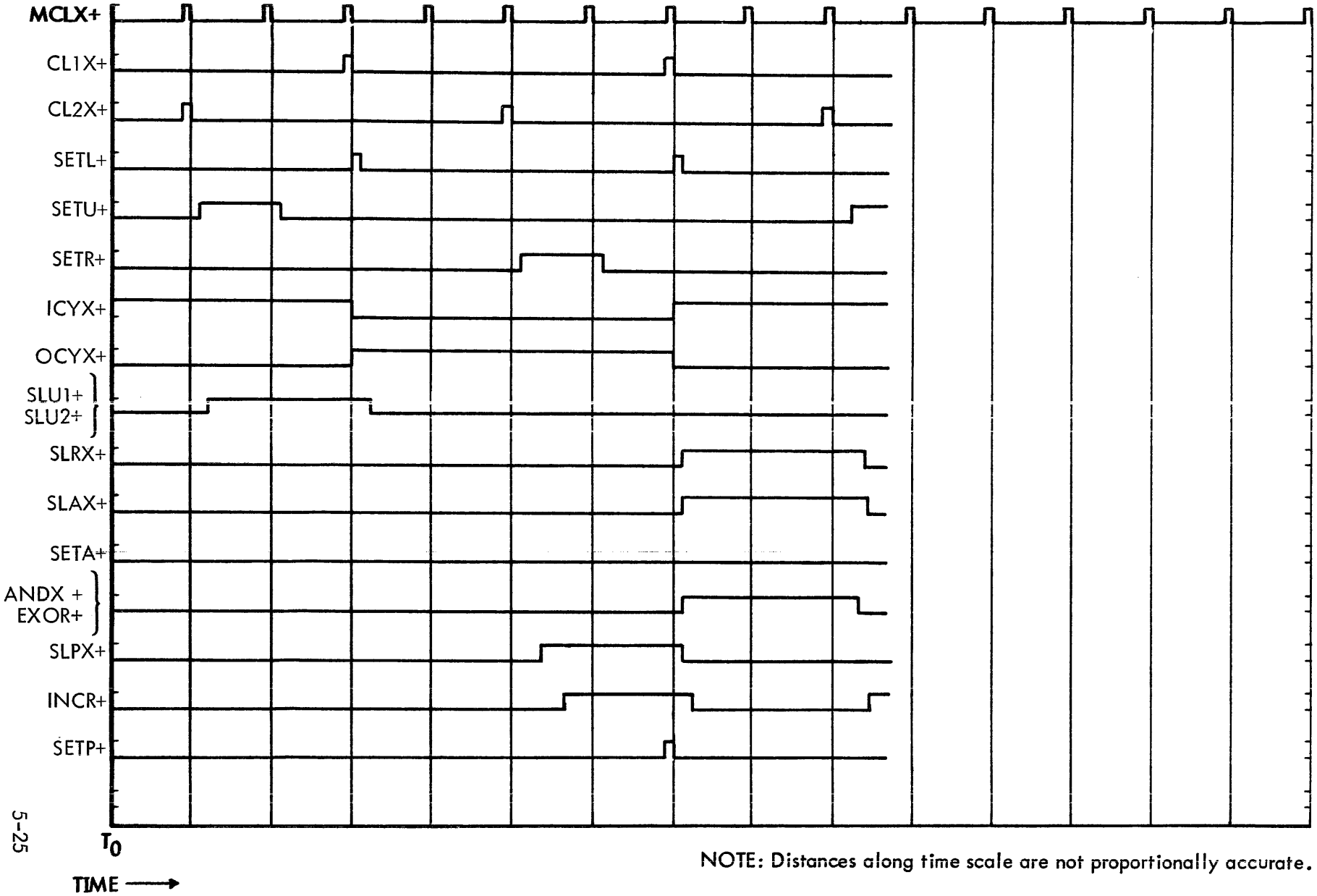


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INCLUSIVE OR TO A REGISTER
MNEMONIC: ORA
OCTAL CODE: 110XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

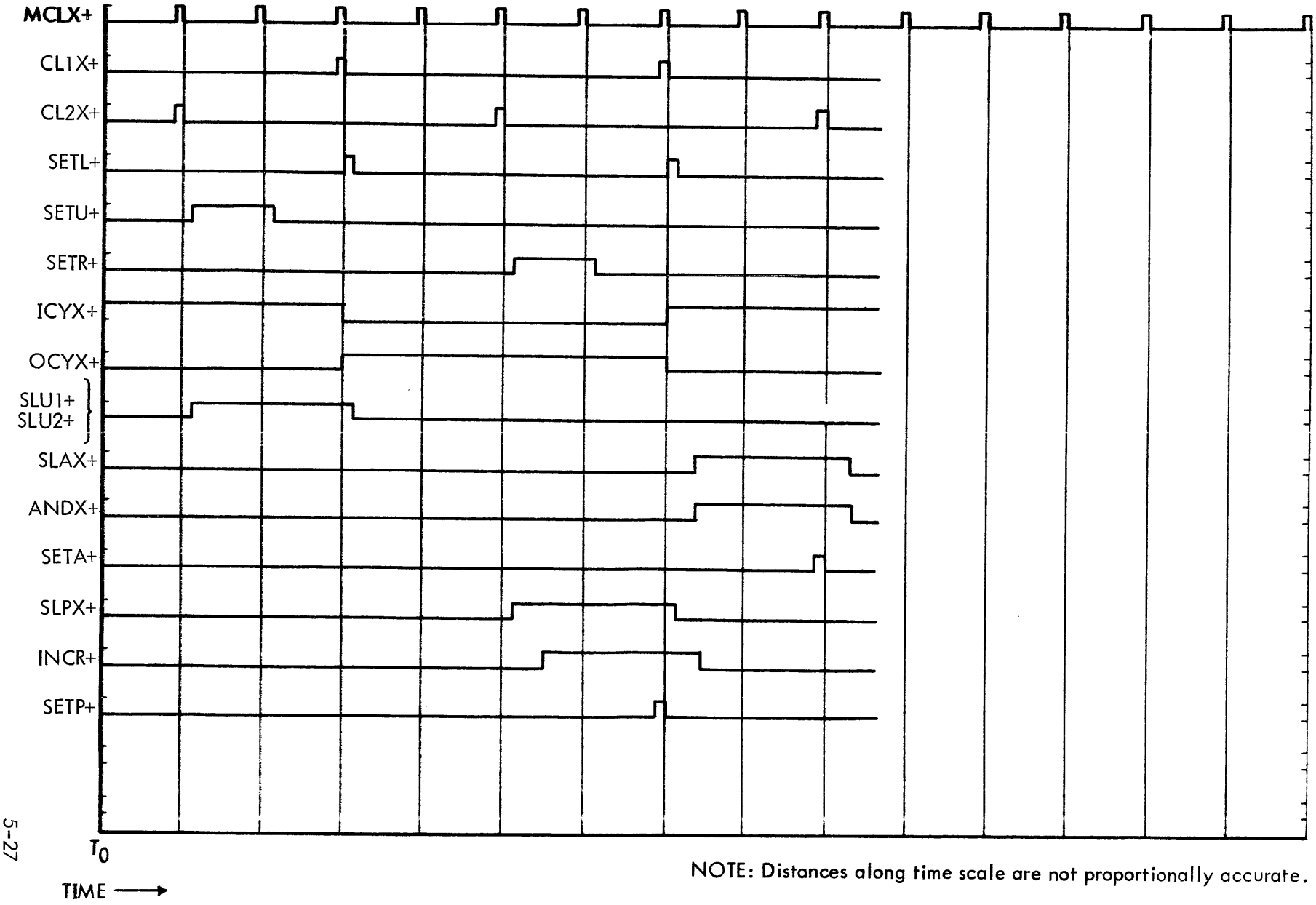


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: AND TO A REGISTER
MNEMONIC: ANA
OCTAL CODE: 150XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.



NOTE: Distances along time scale are not proportionally accurate.

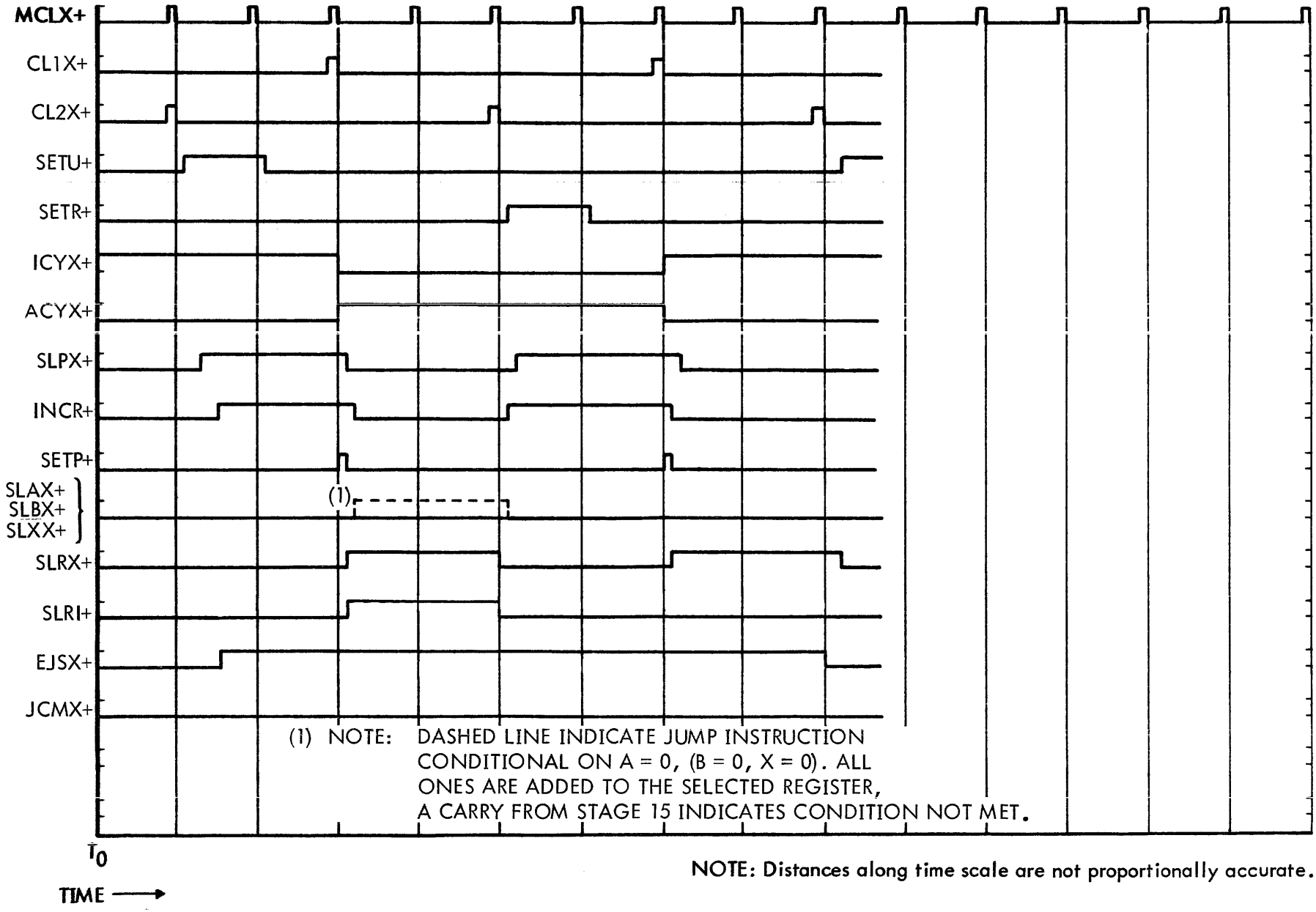
INSTRUCTION: JUMP CONDITION NOT MET, JUMP-AND-MARK CONDITION NOT MET, EXECUTE CONDITION NOT MET

MNEMONIC: JMP, JMPM, EXEC

OCTAL CODE: 001XXX 002XXX 003XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

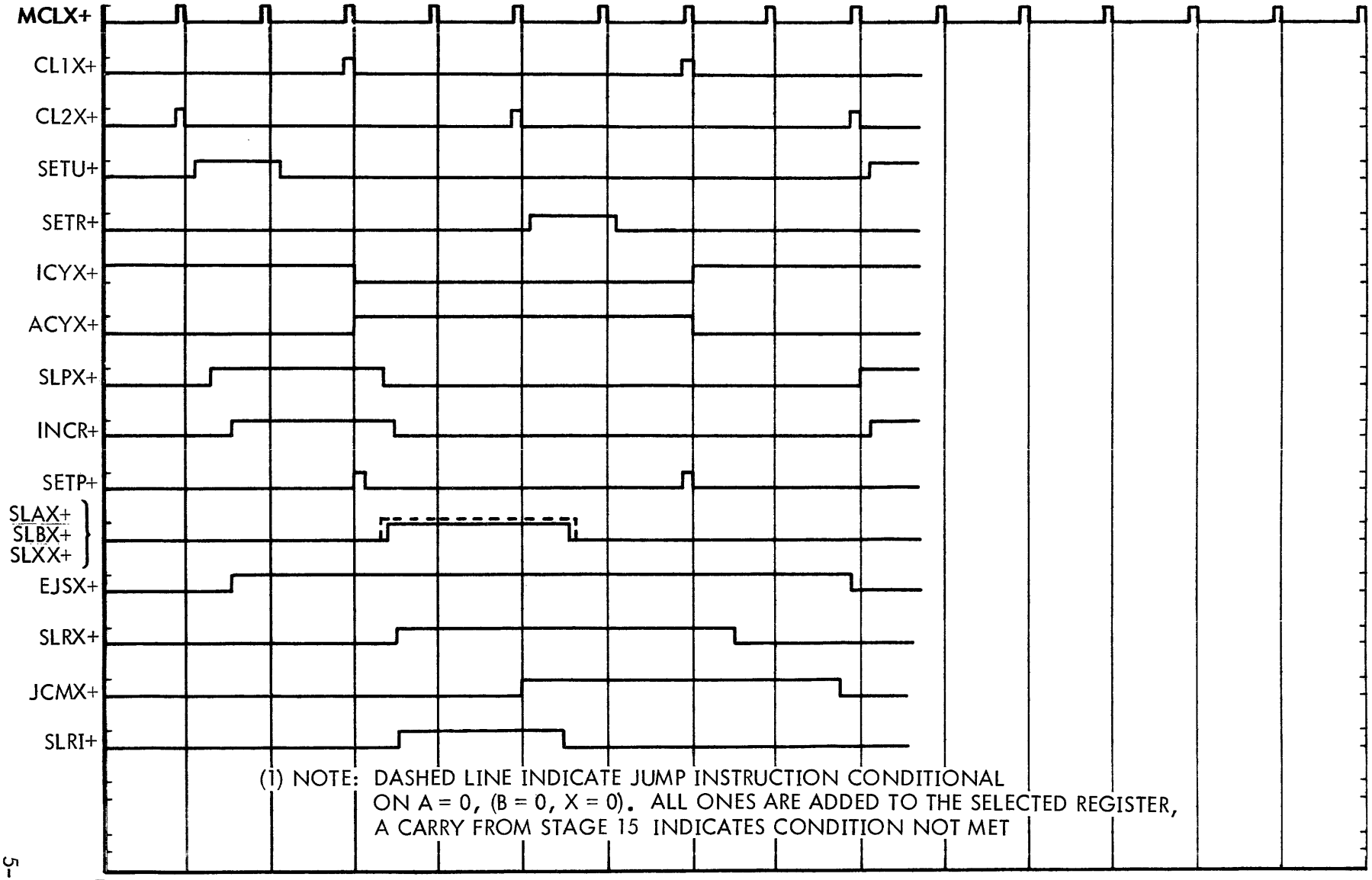


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: JUMP CONDITION MET
MNEMONIC: JMP } JUMP UNCOND.
OCTAL CODE: 001XXX } IS TYPICAL

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

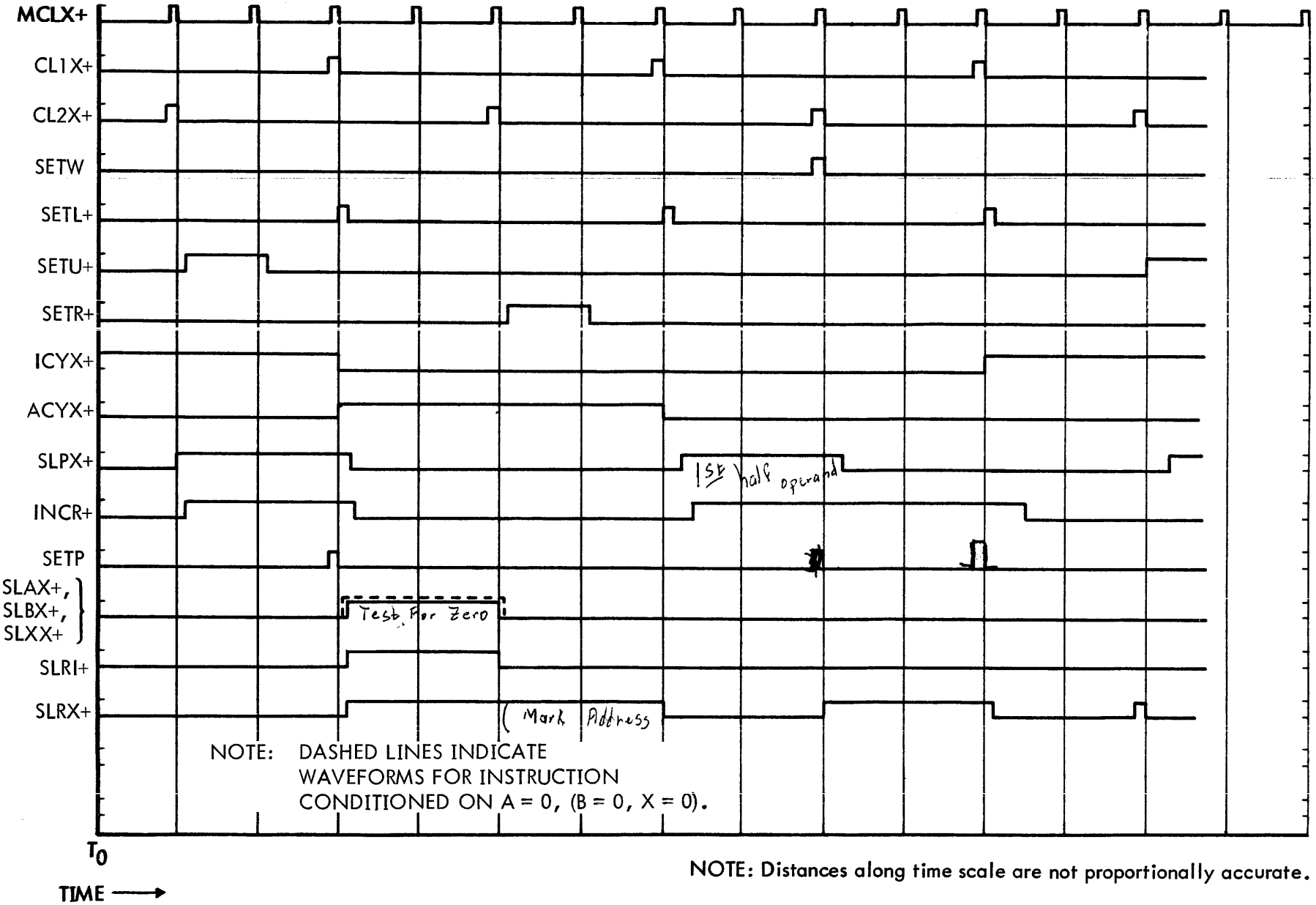


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: JUMP-AND-MARK CONDITION MET
MNEMONIC: J--M
OCTAL CODE: 002XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

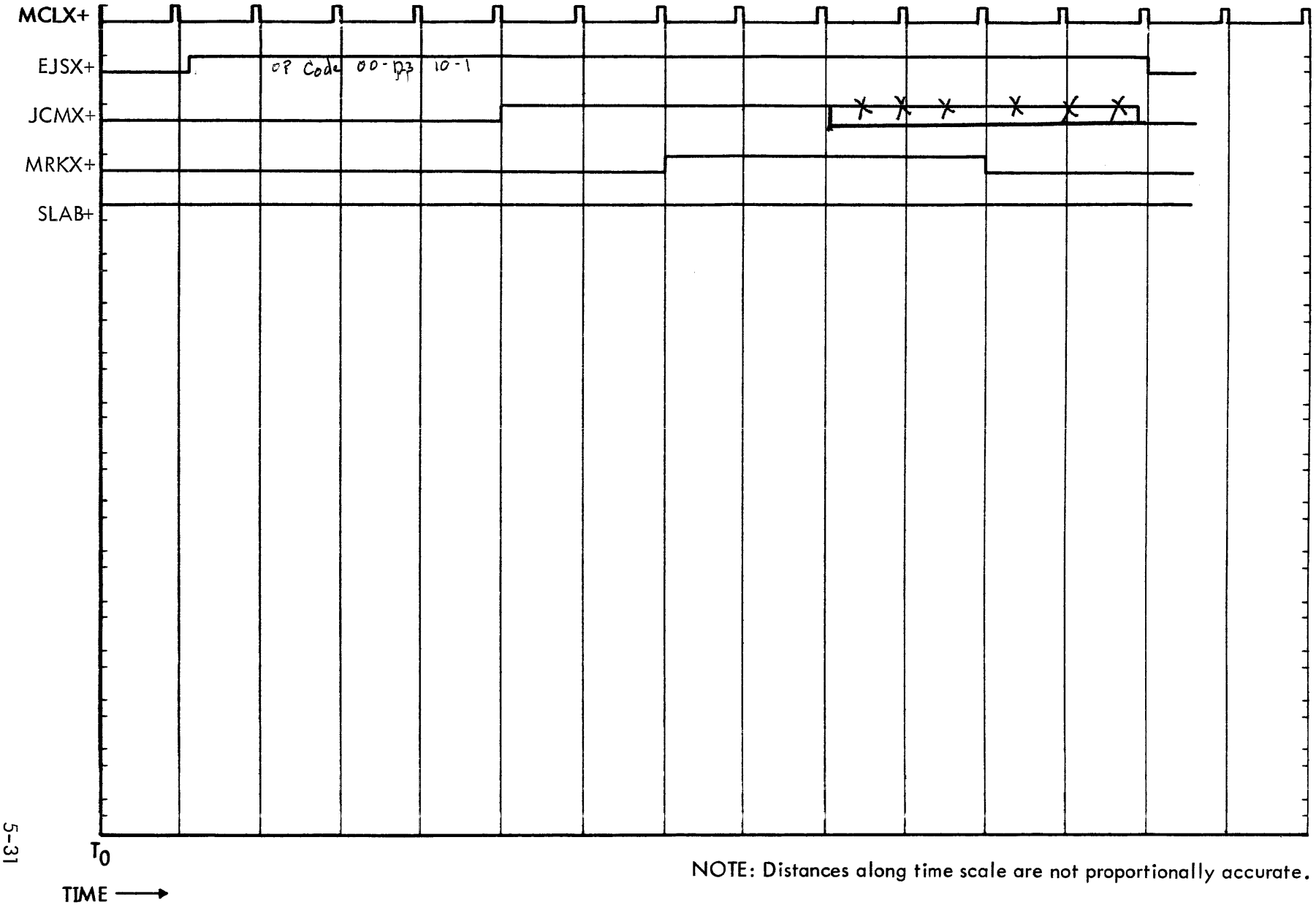


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: JUMP-AND-MARK CONDITION MET
MNEMONIC: J--M (CONT'D)
OCTAL CODE: 002XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

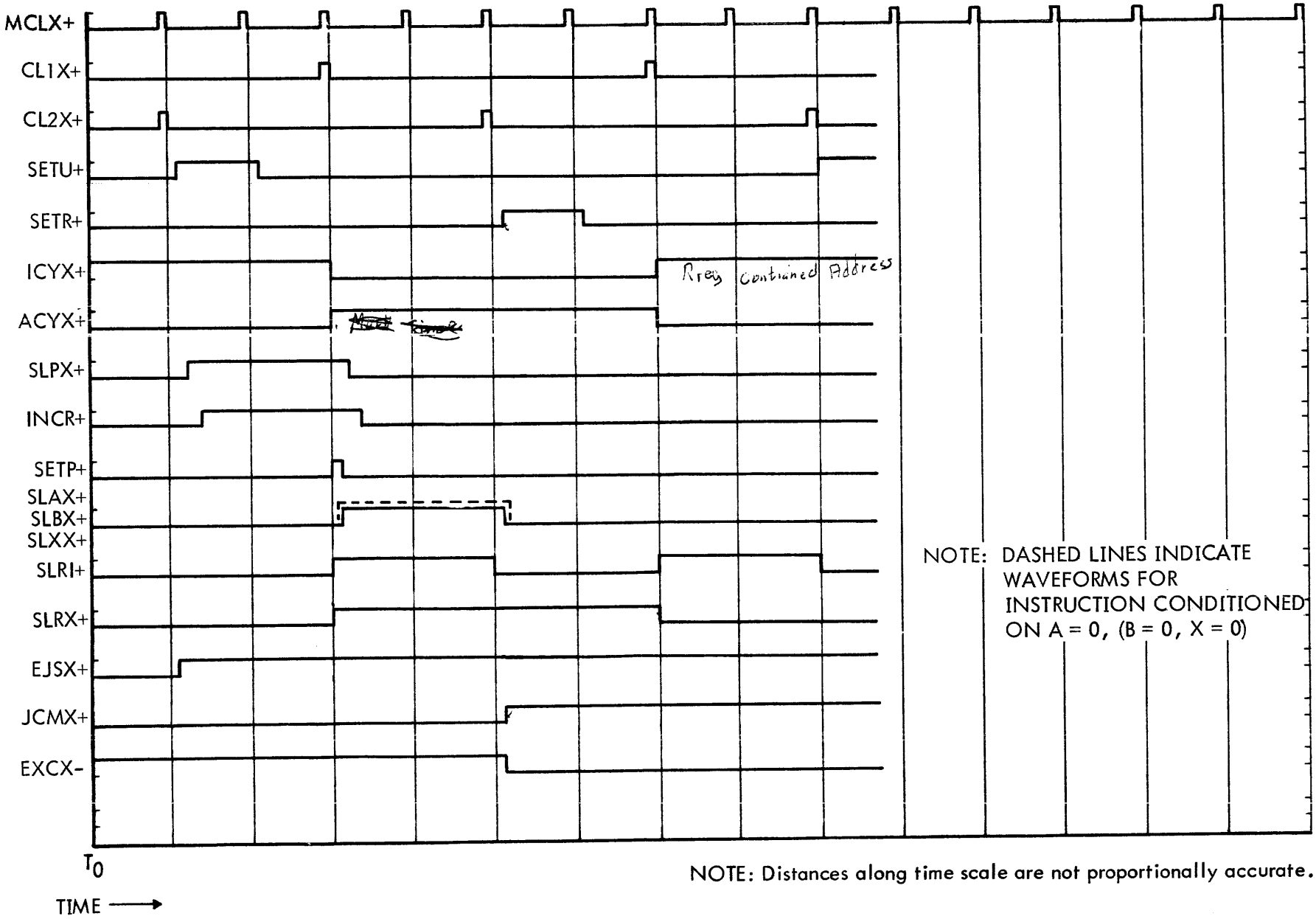


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: EXECUTE INSTRUCTION
MNEMONIC: X--
OCTAL CODE: 003XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

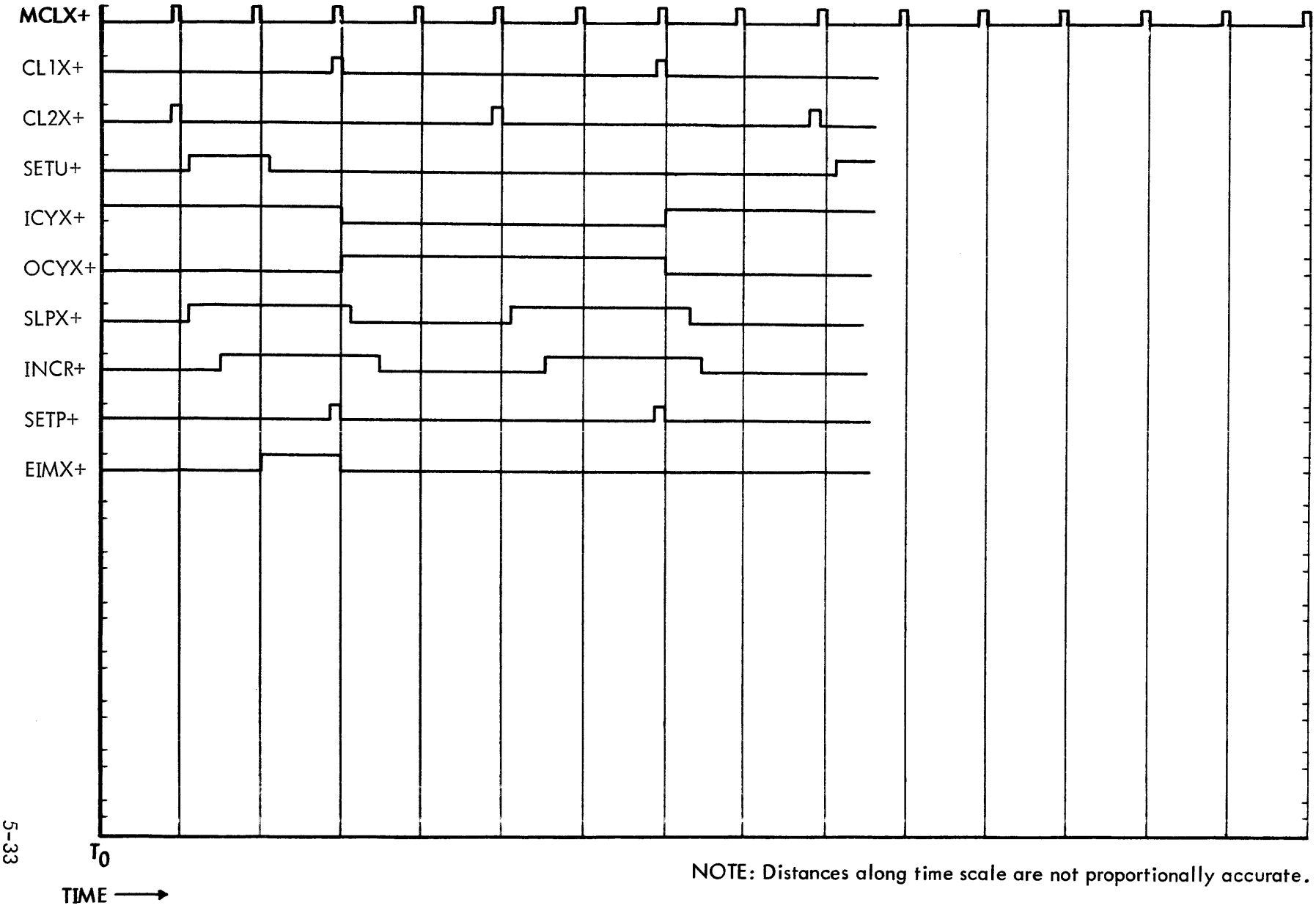


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: IMMEDIATE INSTRUCTION
MNEMONIC: LDAI
OCTAL CODE: 006010
} LOAD A REGISTER IMMEDIATE IS TYPICAL

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

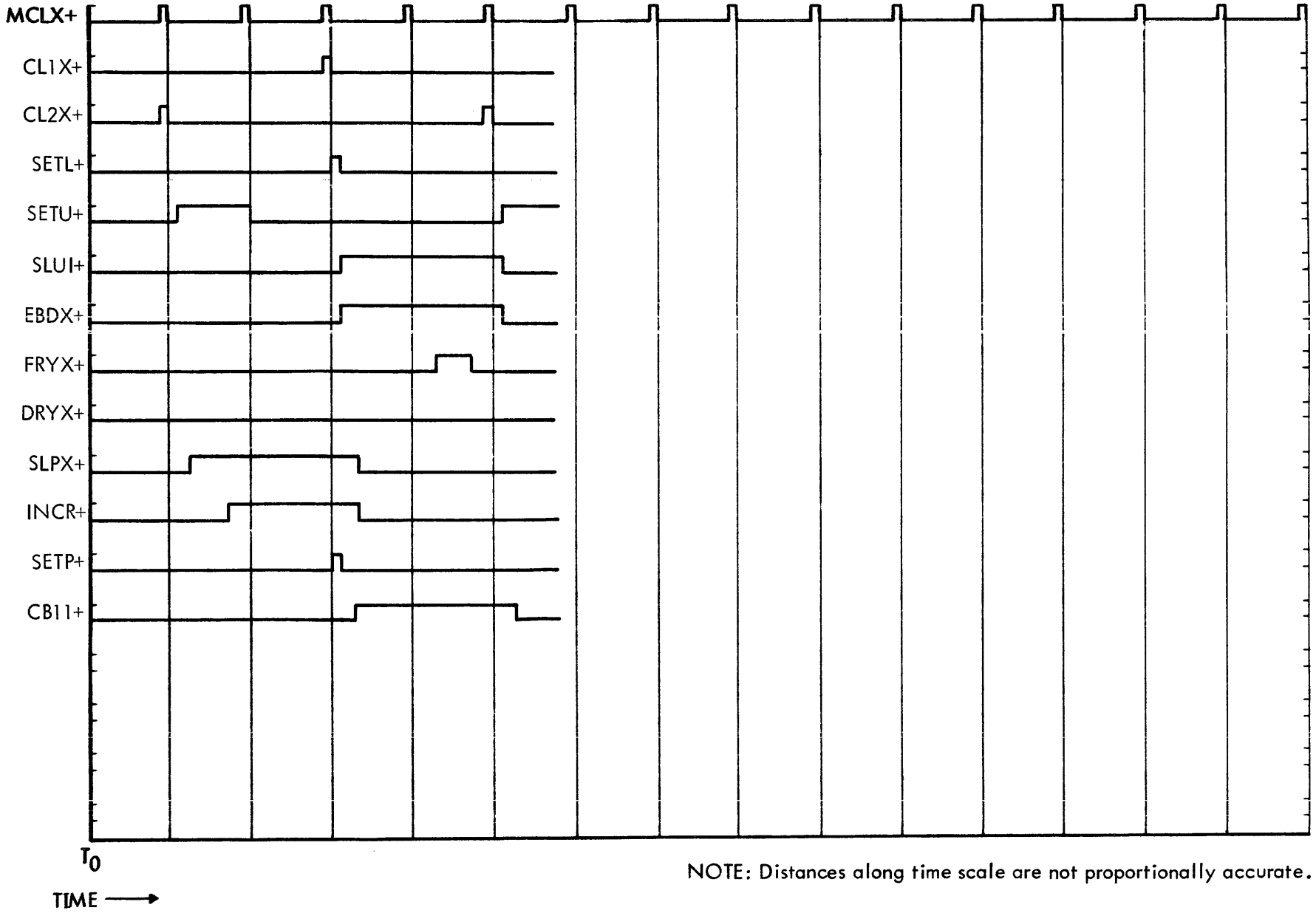


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: EXTERNAL CONTROL
MNEMONIC: EXC
OCTAL CODE: 100XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

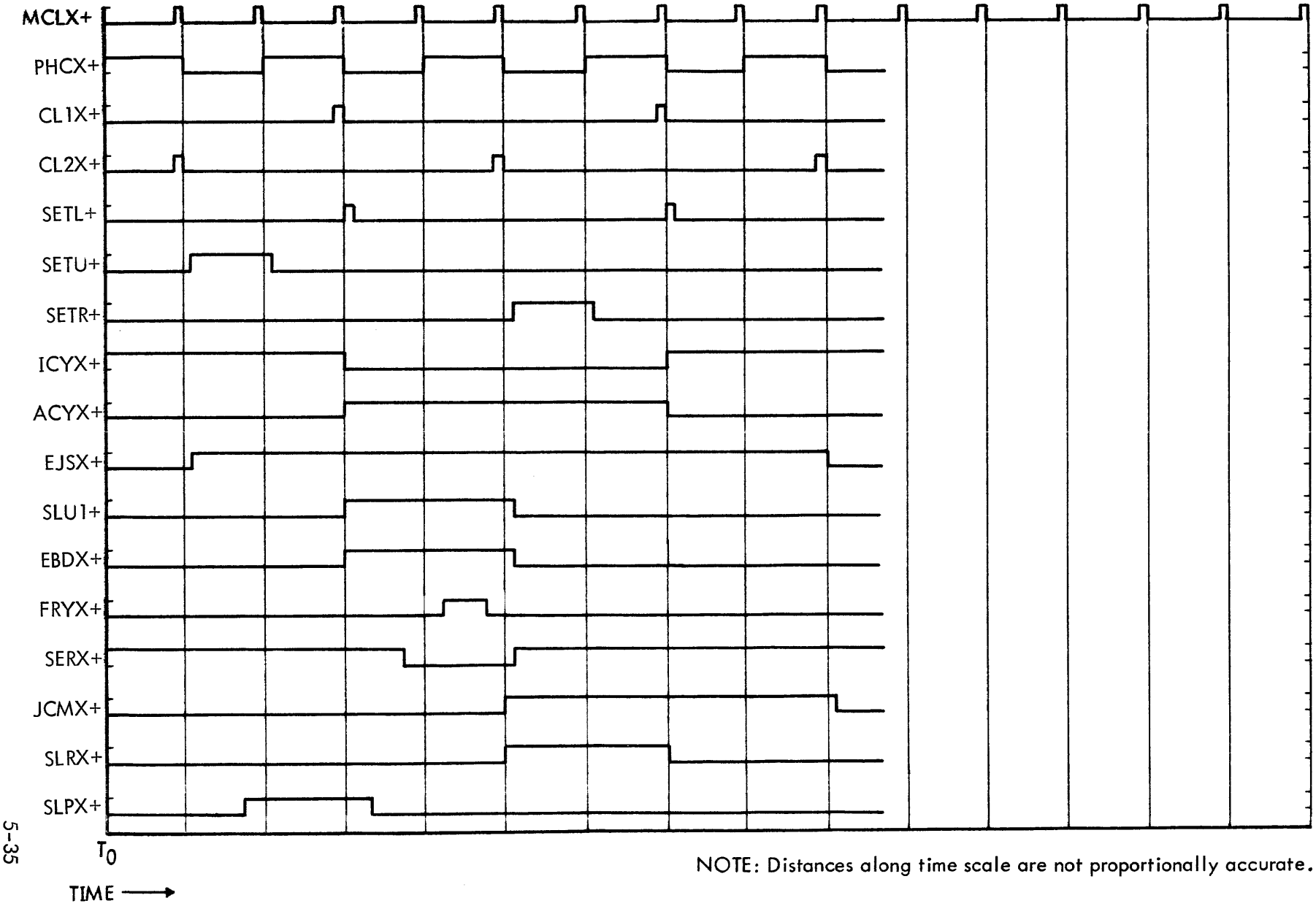


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SENSE (WITH RESPONSE)
MNEMONIC: SEN
OCTAL CODE: 101XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

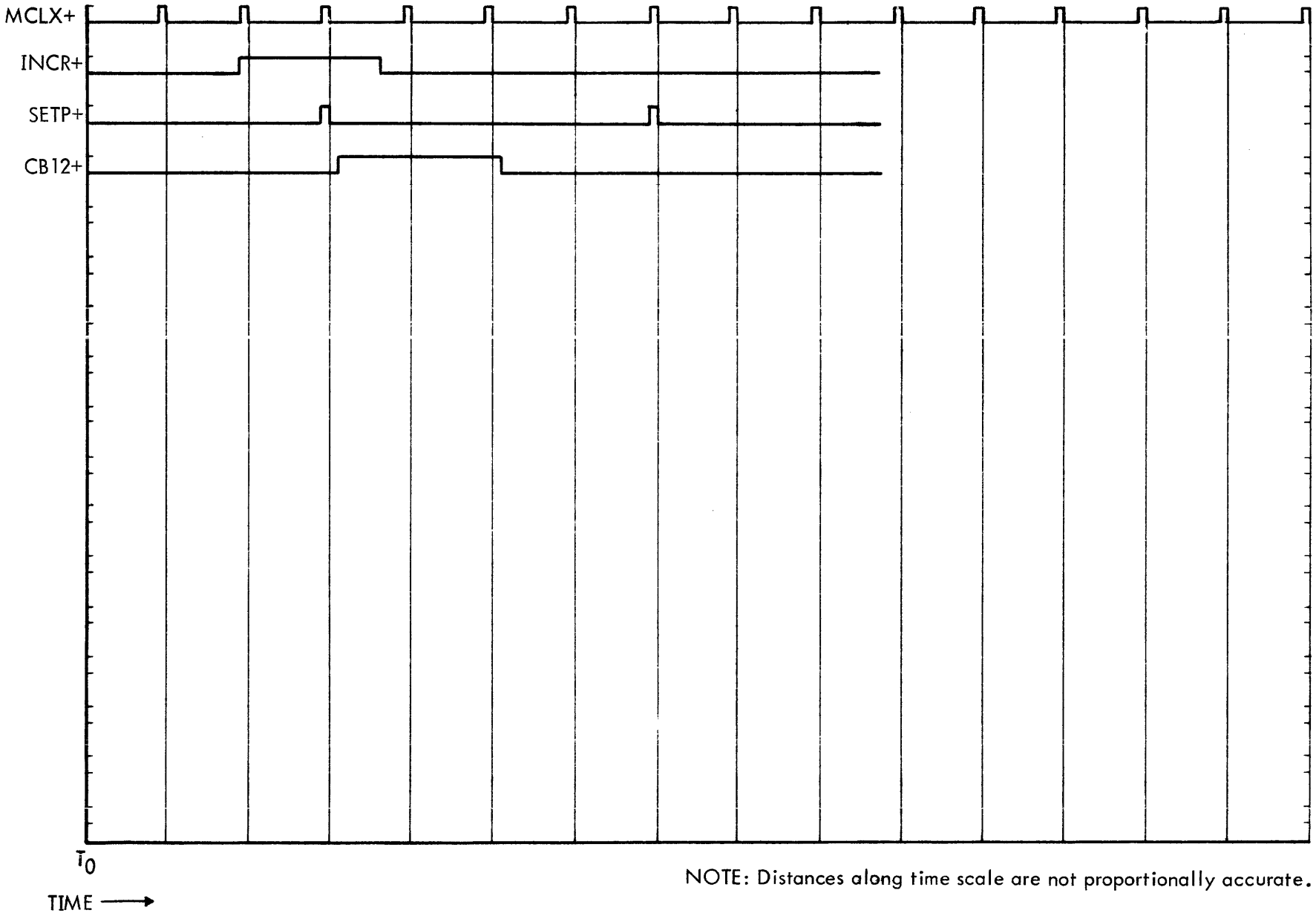


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SENSE (WITH RESPONSE)
MNEMONIC: SEN (CONT'D)
OCTAL CODE: 101XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

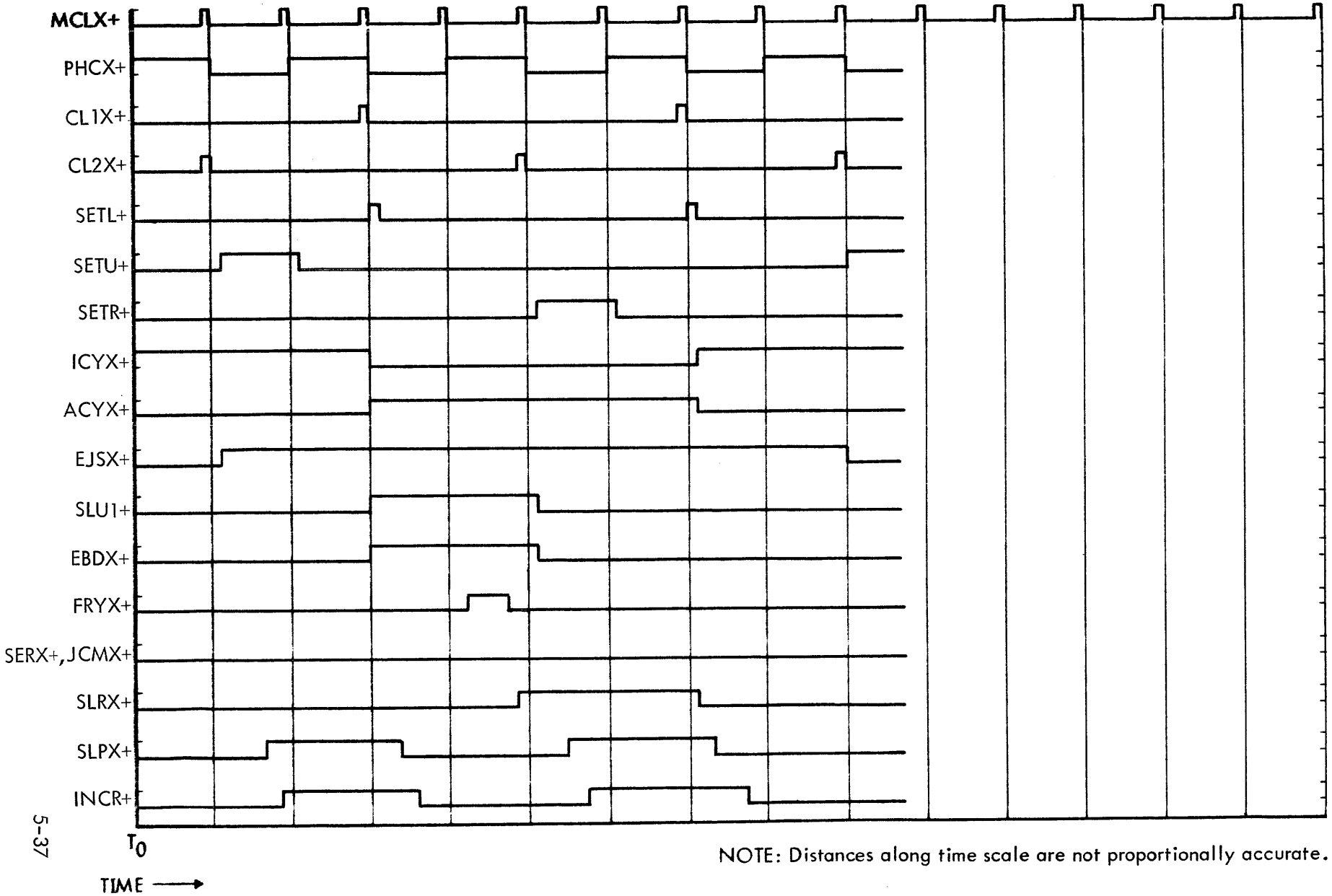


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SENSE (NO RESPONSE)
MNEMONIC: SEN
OCTAL CODE: 101XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

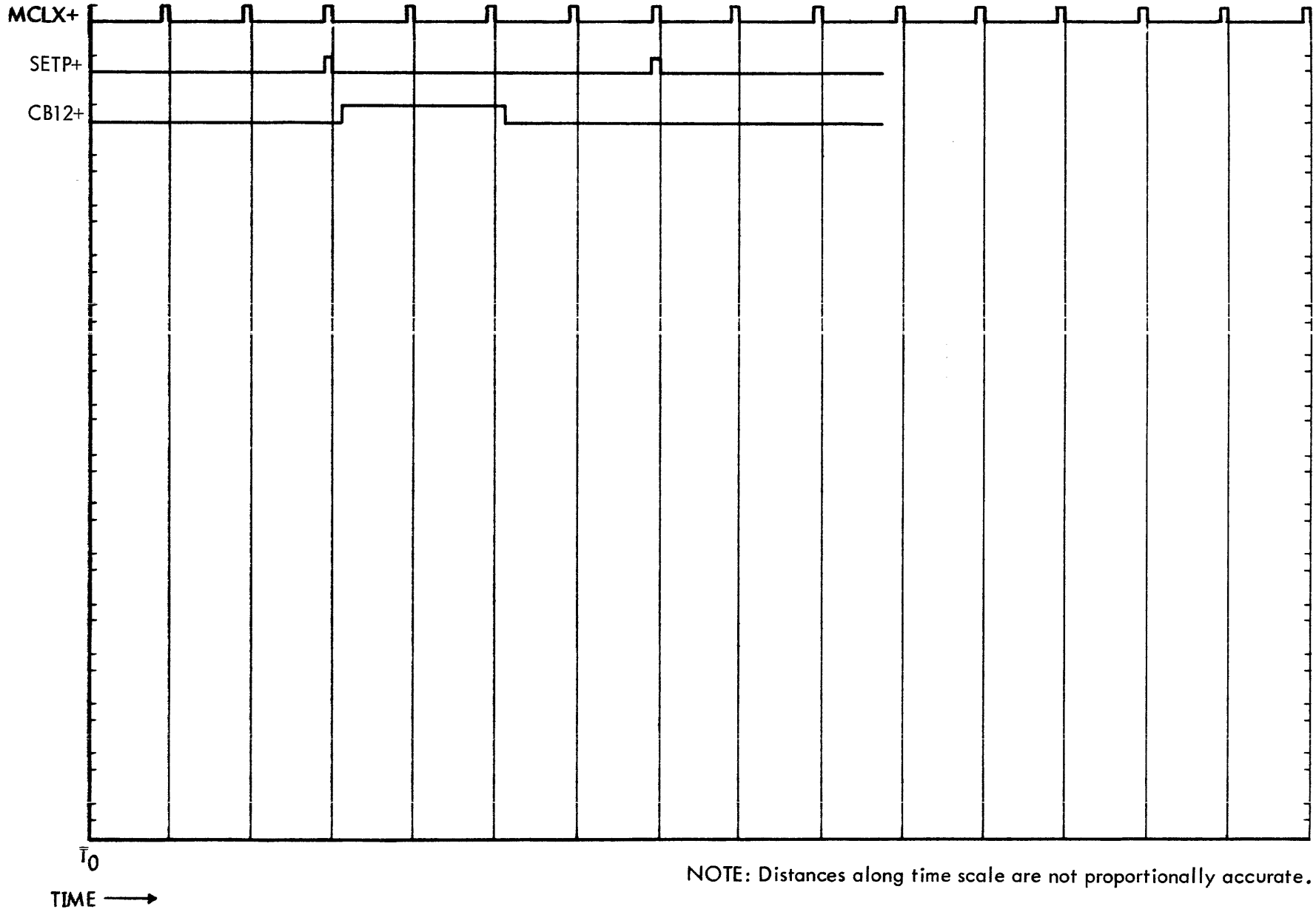


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: SENSE (NO RESPONSE)
MNEMONIC: SEN (CONT'D)
OCTAL CODE: 101XXX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

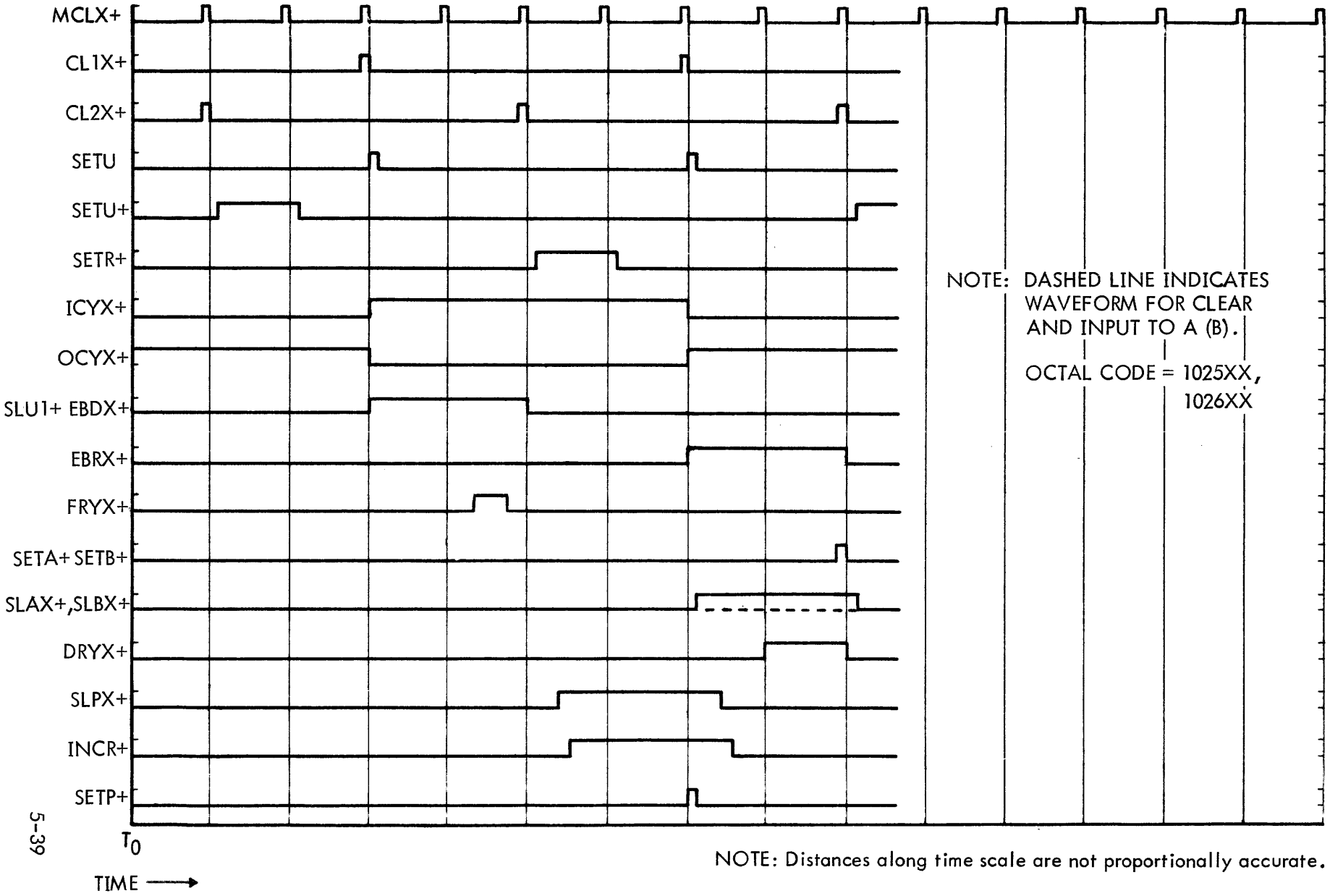


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INPUT TO (A,B) REGISTER
MNEMONIC: INA,INB
OCTAL CODE: 1021XX, 1022XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

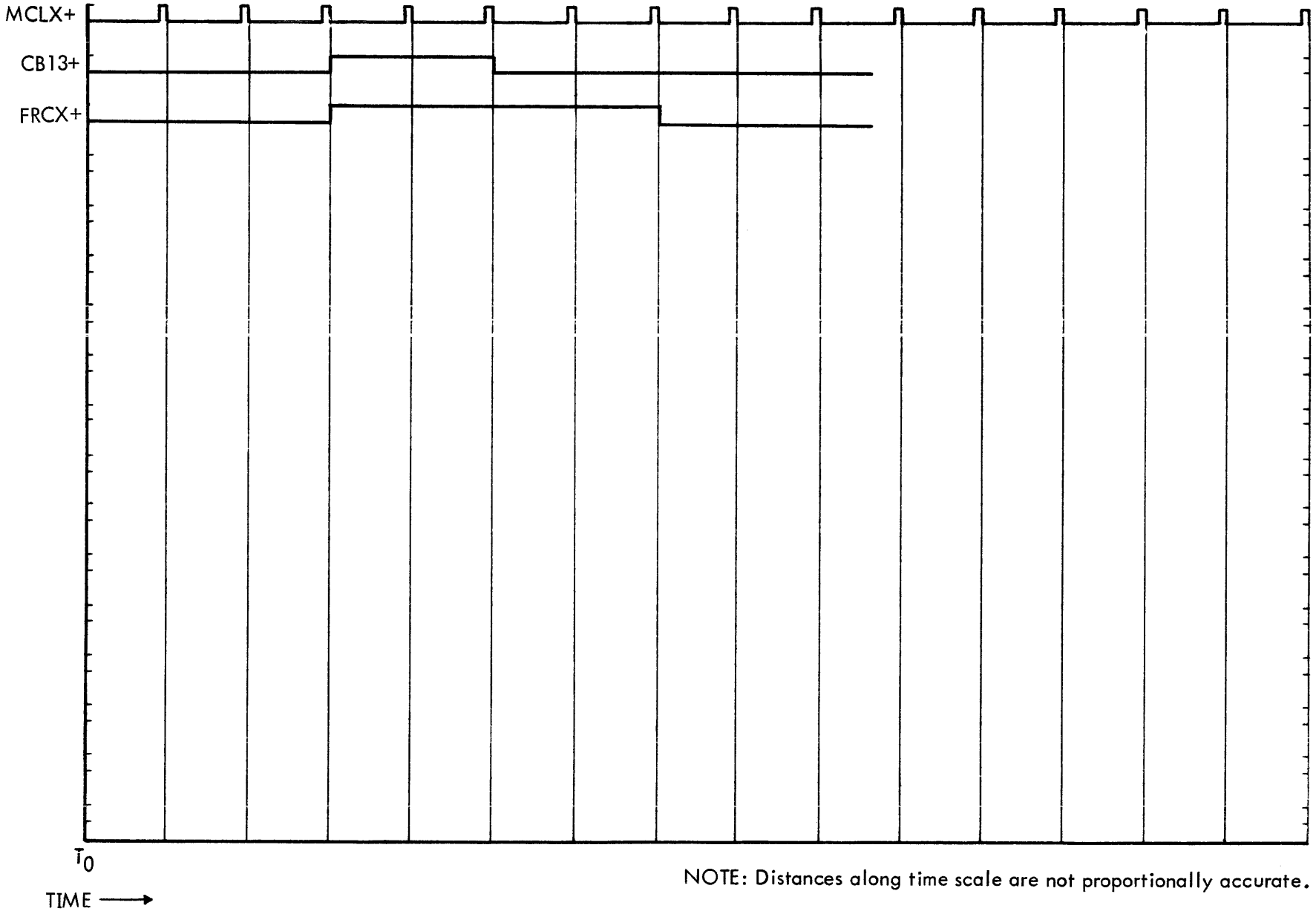


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INPUT TO (A,B) REGISTER (CONT'D)
MNEMONIC: INA, INB
OCTAL CODE: 1021XX, 1022XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

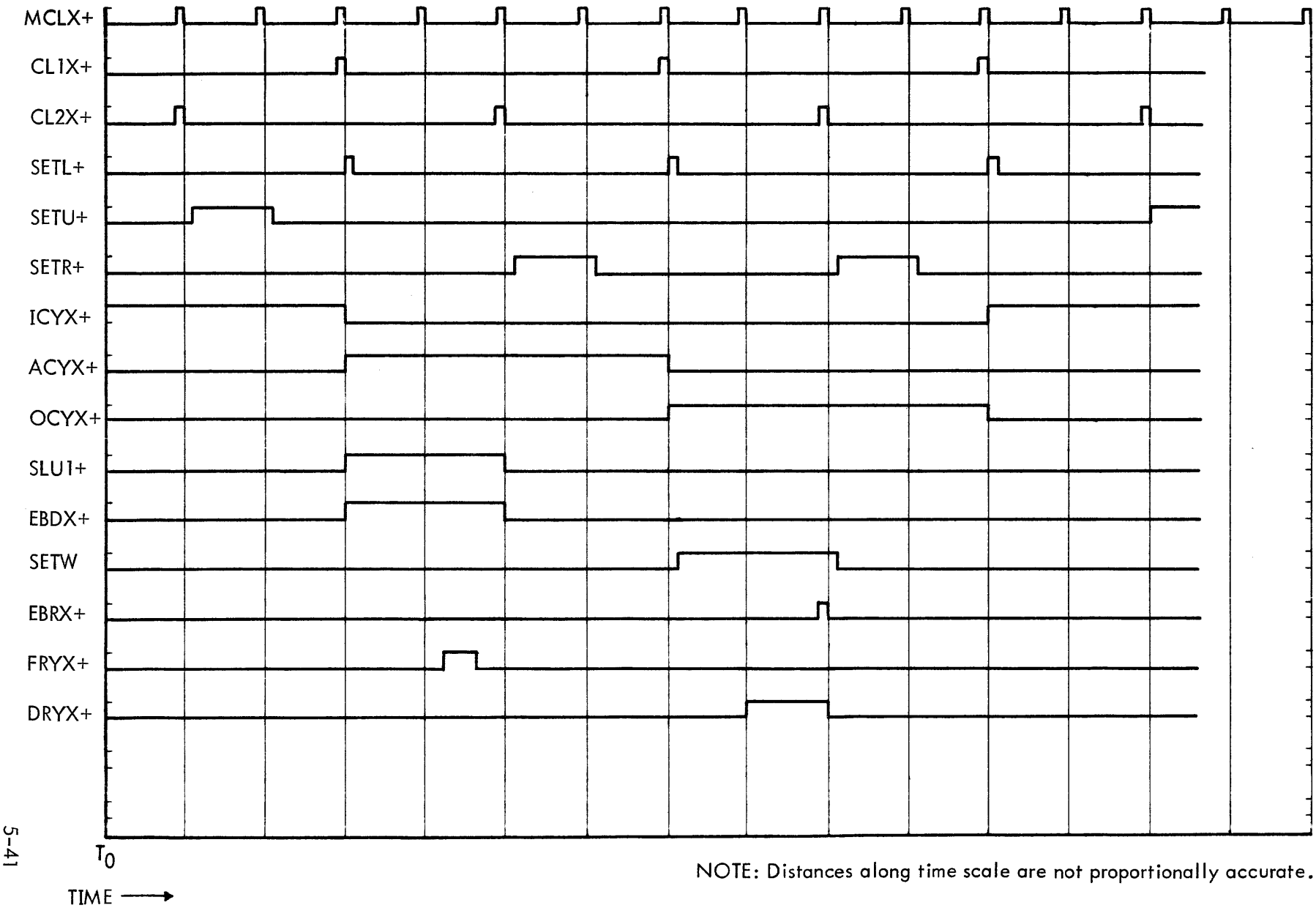


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INPUT TO MEMORY
MNEMONIC: IME
OCTAL CODE: 1020XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

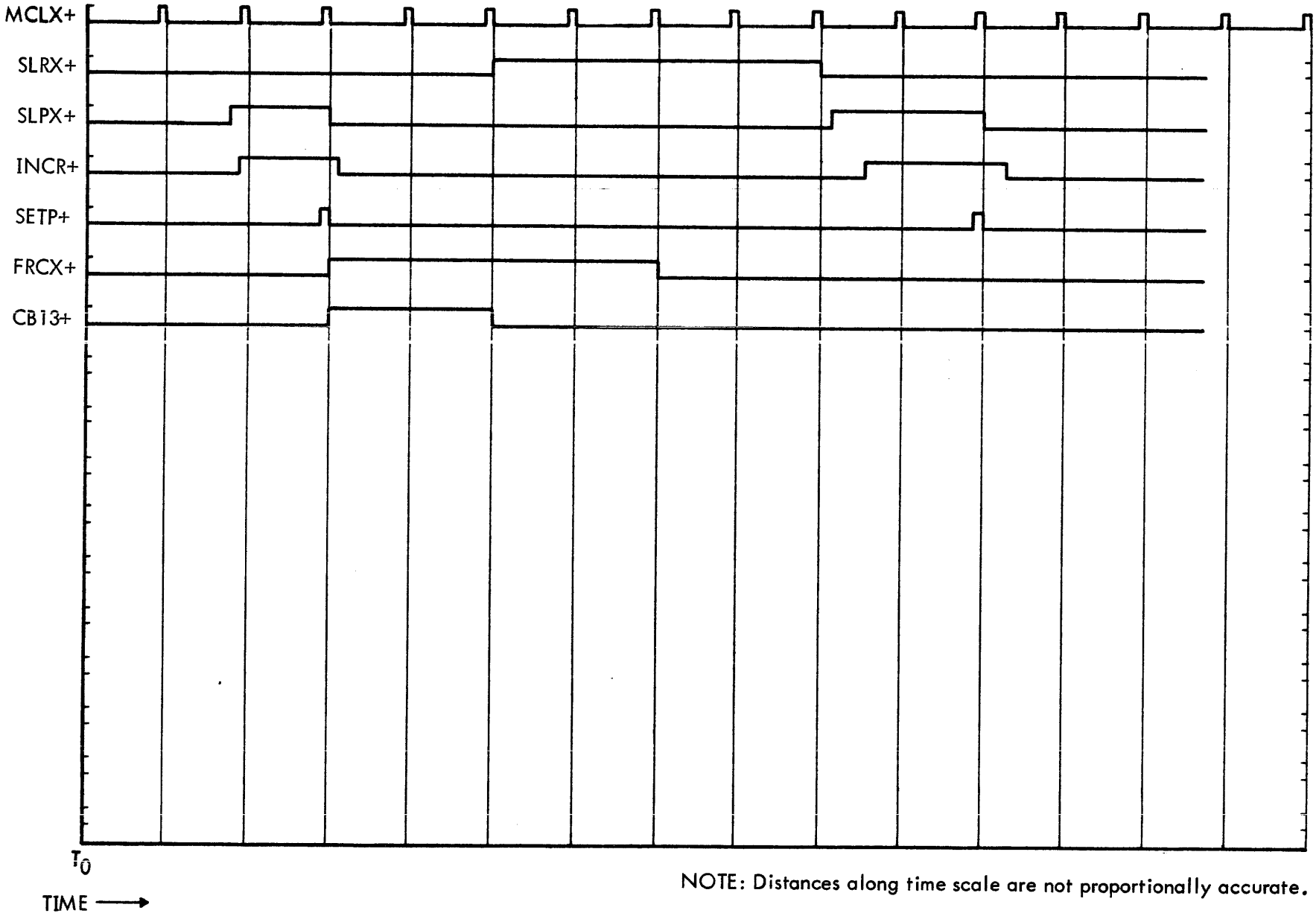


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: INPUT TO MEMORY (CONTINUED)
MNEMONIC: IME
OCTAL CODE: 1020XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

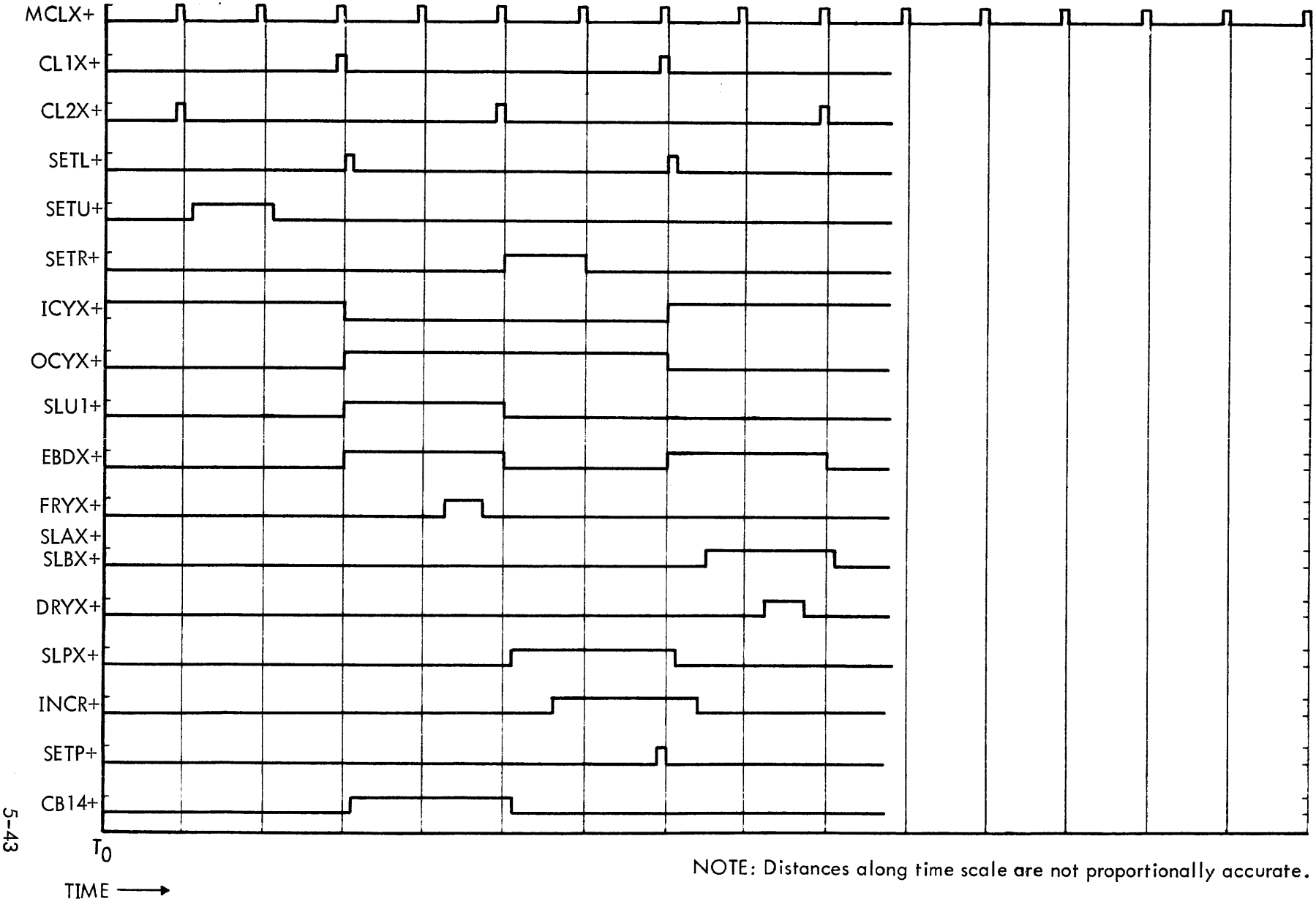


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: OUTPUT FROM A, B REGISTER
MNEMONIC: OAR, OBR
OCTAL CODE: 1031XX, 1032XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

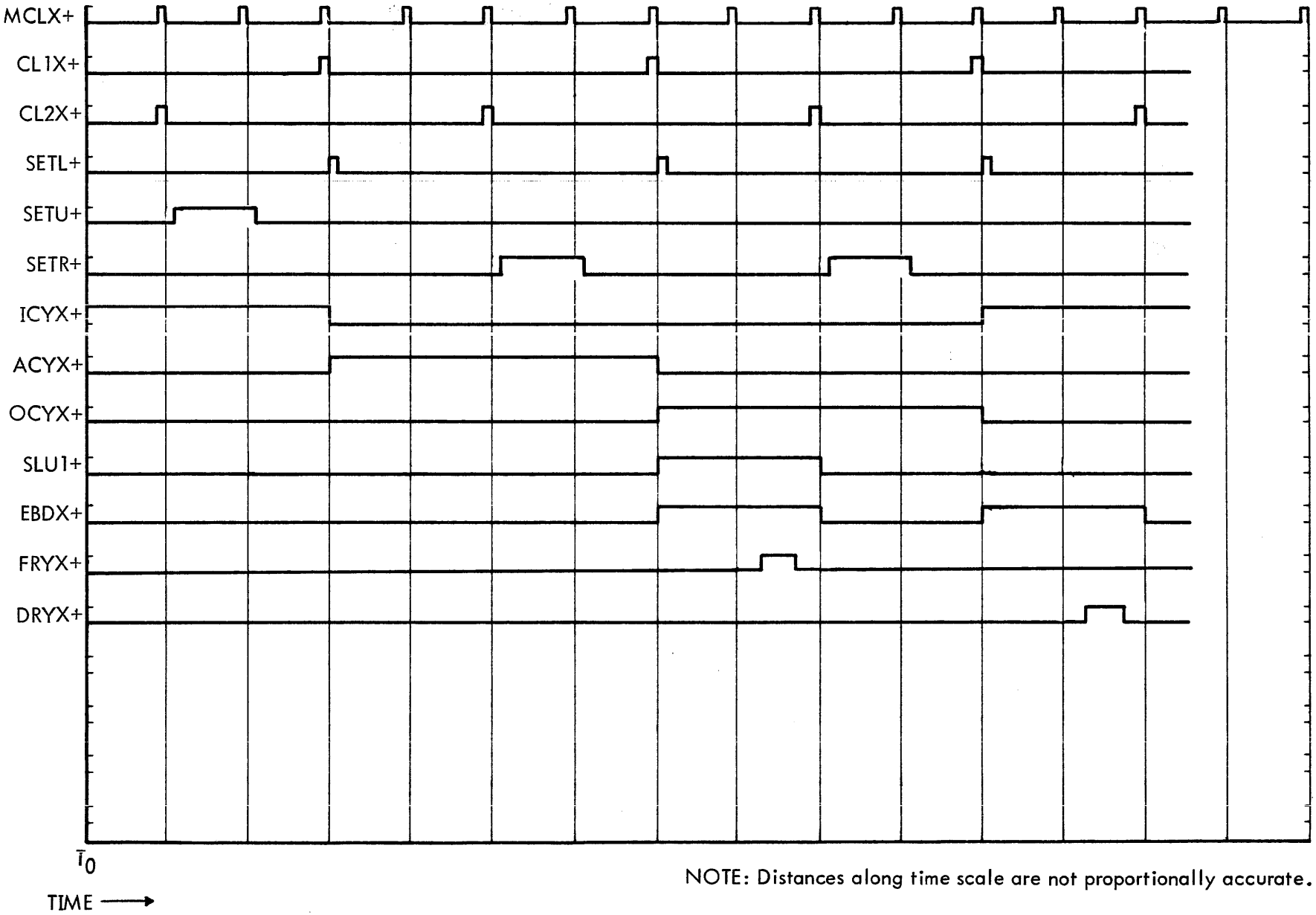


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: OUTPUT FROM MEMORY
MNEMONIC: OME
OCTAL CODE: 1030XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.

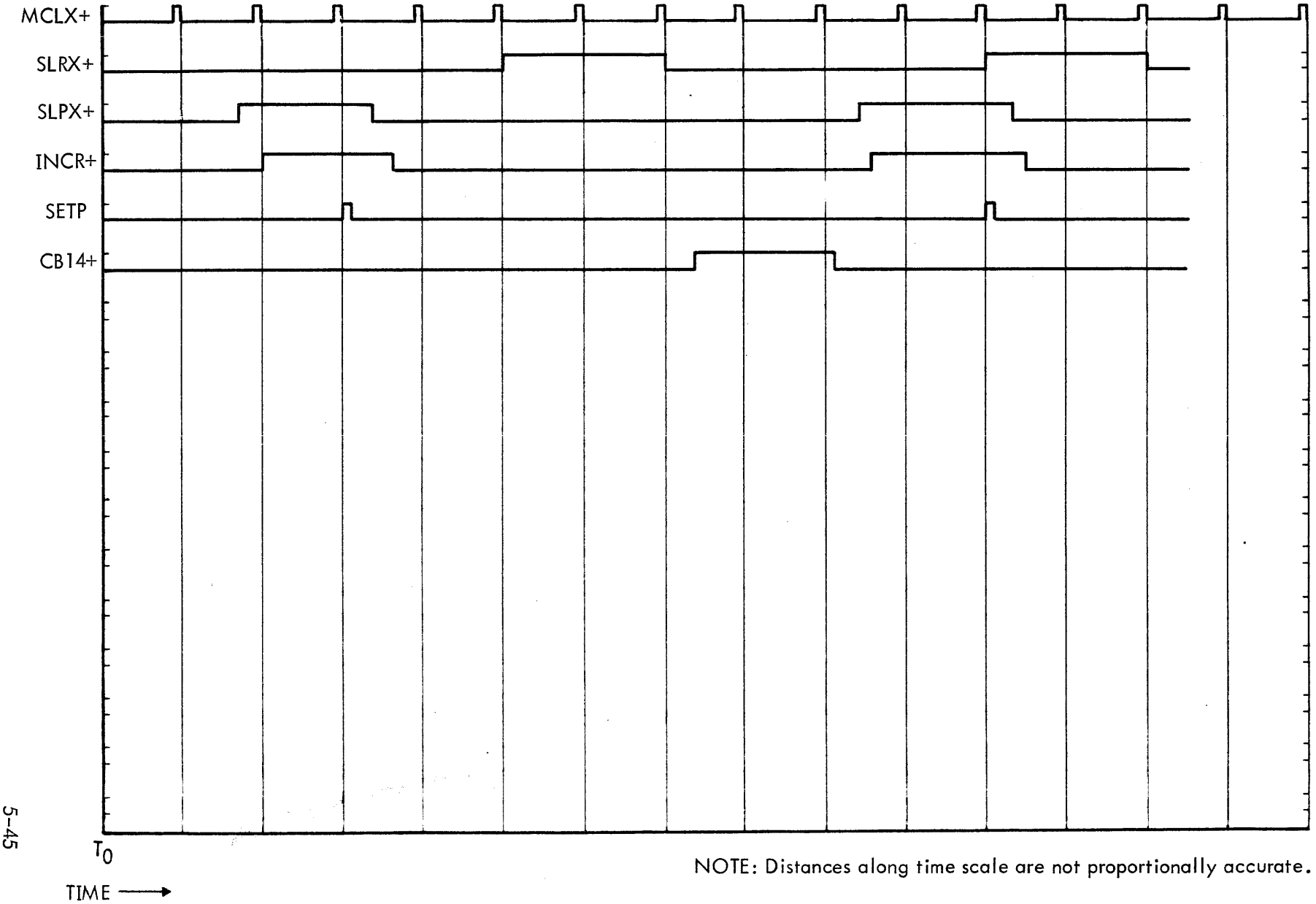


NOTE: Distances along time scale are not proportionally accurate.

INSTRUCTION: OUTPUT FROM MEMORY
MNEMONIC: OME (CONT'D)
OCTAL CODE: 1030XX

Logic levels: True = +5 vdc.
False = 0 vdc.

Time between master clock pulses = 450 nanoseconds.



NOTE: Distances along time scale are not proportionally accurate.

CHAPTER 6
MNEMONIC INDEX

6.1 INTRODUCTION

This chapter presents an alphabetized list of the mnemonic terms which appear on the logic drawings. Functions of the mnemonics are provided as well as locations. The location information is in parentheses and includes the circuit card number and the sheet number of the logic diagram.

AB00- (DM108)	to AB17-	A-Bus Bits 0 to 17 - Common bus where outputs of adder, shift logic, E bus input and console are ORed to drive the C bus (CB00+ to CB17+).
ACYX+ (DM110-1)		Address Cycle - Timing function identifying memory cycles used to obtain an address word, i.e., jump, input and output memory, indirect addressing.
AC0X+ (DM110-1)	to AC6X+	Address Code 0 - Address Code 6 - Decodes M field (U register bits 9-11).
ANDX+ (DM110-2)		AND - Decodes U register for AND instruction and inclusive OR.
BISE- (DM112-1)		Bit Store Enable - Ground true signal to set BISX on a long shift to transfer A0 or A17 to the B register.
BISX (DM112-1)		Bit Store - Provides storage of A register bit for transfer to B register during long shifts and multiply or divide.
CALX+ (DM108)		Carry - Last bit of adder - bit 17 or 15.
CANL+ (DM108)		Carry Next to Last - Bit 16 or 14 of adder.
CA05+ (DM108)		Carry Bit 5 - Output of bit 5 to bit 06.
CA11+ (DM108)		Carry Bit 11 - Output of bit 11 to bit 12.
CB00+ (DM108)	to CB17+	C-Bus Bits 0 to 17 - Data bus in computer that supplies data to operational registers, console and output to E bus.
CBLX+ (DM110-3)		Last C-Bus Bit - Last bit of C-bus. CB15+ for a 16-bit machine. CB17+ for an 18-bit machine.
CLEI+ (DM112-1)		Clock Enable - Enables primary system clock. Provides synchronization with PHCX, off during HALT, and ICLX.
CLRW- (DM112-3)		Clear W Register - Pulse that clears the memory data register at the start of a memory operation.
CLIX+ (DM112-3)		Clock 1 - Major clock function, used to identify the start of a memory cycle.
CL2X+ (DM112-3)		Clock 2 - Major clock function, identifies the midpoints a memory cycle when data is available, or when data can be set into the W register.
DAGS- (DM107)		Data Guard - Disables outputs of memory regulator card (DM107) during power turn on/off. Controlled by memory enable/disable switch and/or power fail restart option.
DIVX- (DM112-1)		Divide - Indicates that a divide operation is occurring.
DRYX+ (DM112-2)		Data Ready - Provides data ready pulse to I/O bus. Used to gate output data in external controllers.

DRYX-1 (DM112-2) — Data Ready - Pulse on I/O line that is used in external controllers to gate in data and to terminate the data phase.

DSCX- (DM111) — Divide Sign Check - Result of a sign check during a divide operation.

EB00-I to EB17-I (DM108) — E Bus Bit 0 to 17 - Main input/output lines in computer.

EBDX+ (DM112-2) — E Bus Drive - Enable for E bus drivers. Outputs C bus to E bus.

EBRX+ (DM112-2) — E Bus Receive - Enables E bus to be ORed on to the C bus.

EIMX+ (DM110-3) — Execute Immediate - Controls the transfer of U3-6 to U12-15 during an immediate instruction.

EJIX- (DM110-3) — Execute Jump Instruction - Decodes jump, jump-and-mark, and execute instructions.

EJRX+ (DM111-3) — Execute Jump or Register Change - Logical OR of ERCX- and EJIX-.

EJSX+ (DM110-3) — Execute Jump or Sense - Logical or of EJ1X- and ES1X-

EMRX- (DM121) — E and W Bus Receive - Normally zero volts when trapping in or out with DMA.

EPHX- (DM112-1) — Execute Phase - Major control function separates memory cycle into execute and address phase. Execute phase when EPHX+ is 5 volts.

ERCX+ (DM110-2) — Execute Register Change - Provides timing and selection for register change instructions.

ESIX- (DM110-3) — Execute Sense Instruction - Decode for sense instruction.

EXCX- (DM109-1) — Execute - Provides selection of operand cycle during execute instruction.

EXOR+ (DM110-2) — Exclusive OR - Provides decoding of exclusive OR, inclusive OR and register change complement instructions.

FCDX- (DM112-2) — First Count Detect - Indicates that shift counter SC00X to SC03X has reached a

FCOX+ (DM110-1) — Function Code Zero - Denotes that U register bits 6, 7, and 8 are equal to zero.

FCYX+ (DM106) — Full Cycle Command - Enables a read or clear memory cycle followed by a restore or write memory cycle.

FEAI (DM110-1) — Fetch Address - Enable for ACYX+ on all instructions that require an address cycle.

FEIX+ (DM110-1) — Fetch Instruction - Enable for ICYX.

FEOX+ (DM110-1)	Fetch Operand - Enable for OCYX.
FRCX- (DM112-2)	Function Ready Control - Detects and controls programmed function out sequence.
FRYX-I (DM112-2)	Function Ready Control - Pulse used to terminate the address phase on the I/O line.
FRYX+ (DM112-2)	Function Ready - Provides function ready to I/O bus.
G1XX+ to G4XX+ (DM110-2)	Group Decoding 1 to 4 - Decodes U register bits 12 and 13.
HLTX+ (DM109-2)	Halt - Controls execution (run) or nonexecution (step) modes of computer operation.
HTCX- (DM109-2)	Halt Control - Initiates halting of computer operation.
H1XX+ to H4XX+ (DM110-2)	Set Decoding 1-4 - Decodes U register bits 14 and 15.
IAPX+ (DM110-1)	Instruction Address Phase- Provides timing function for address operations. Occurs during last half of instruction cycle.
ICLX- (DM112)	Inhibit Clock - Inhibits CL1X+ and CL2X+ during an interrupt or trap operation.
ICYX+ (CM110-1)	Instruction Cycle - Timing function identifying memory cycles used to obtain instruction words.
IEPX+ (DM110-1)	Instruction Execute Phase - Provides timing function for instruction execution. Occurs during first half of all instruction cycles.
IHTC- (DM109)	Inhibit Halt Control - Used by Micro-EXEC option to inhibit setting of the halt control flip-flop.
IIAX- (DM112-2)	Increment Interrupt Address - Adds one to interrupt address when interrupting to double word instructions.
IMCX- (DM110-3)	Increment Memory Control - Provides control of INR instruction.
INCR+ (DM112-1)	Increment - Provides increment signal to adder; adds one to data at adder.
INHV+ (DM119)	Inhibit Voltage - For regulated power source for inhibit drivers.
JCMX+ (DM109-1)	Jump Condition Met - Stores detection of jump-condition-met on jump, jump-and-mark, execute and sense instructions.
JCN1+ (DM109-1)	Jump Condition Met, Gate 1 - Logical OR of all tests for Jump, Jump and Mark, and Execute condition-met.
K1XX+ (DM110-2)	Class 1 - Decodes U register bits 12, 13, 14 for all single word addressable instructions.

K2XX+ (DM110-2)	Class 2 - Decodes U register op-code 00, selects all jump, jump-and-mark, execute and shift, register change, immediate and set/reset overflow instructions.
K3XX+ (DM110-2)	Class 3 - Decodes and selects all I/O instructions.
K23X+ (DM110-2)	Class 23 - Provides decoding for K2 or K3 instructions.
LSCX+ (DM112-2)	Long Shift Control - Provides control of long shift, multiply and divide sequences. A register selected when LSCX is on, B register when LSCY is off.
L00X+ to L15X+ (DM109-3)	Memory Address Register - Contains address of data memory is reading or writing.
MCLX+ (DM112-3)	Master Clock - Basic crystal controlled 2.2MHz clock for system.
MC2X+ (DM112-3)	Master Clock 2 - Controlled 2.2MHz clock. Gated off by inhibit clock (ICLX) and halt functional (HTCX, HLTX).
MDN2+ (DM110)	Multiply/Divide Not - Selects A bus during interrupt, trap, or divide operations.
MRKX+ (DM110-2)	Mark - Provides timing and control function for jump-and-mark instructions.
MRSX+ (DM109-2)	Manual Register Select - Enable for setting registers in the manual mode.
MSAX- (DM111-1)	Manual Select A Register - Manual select of A register from console.
MSBX- (DM111-1)	Manual Select B Register - Manual select of B register from console.
MSCE+ (DM106)	Memory Start Clock Enable - Enables the memory start clock pulse into the timing and control circuitry (DM106).
MSC1+ (DM112-3)	Memory Start Clock 1 - Initiates memory operation for first 4K of memory.
MSPI- (DM109)	Memory Start Pulse Inhibit - Used in memory parity option to disable the setting of the memory start pulse flip-flop.
MSPX+ (DM109-1)	Memory Start Pulse - Delayed clock 1 for starting memory.
MSPX- (DM111-1)	Manual Select P Register - Manual select of P register from console.
MSUX- (DM111-2)	Manual Select U Register - Ground true when selecting U register from the console.

MSXX- (DM111-3)	Manual Select X Register - Manual select of X register from console.
OCYX+ (DM110-1)	Operand Cycle - Timing function identifying memory cycles used to obtain an address word.
OVXX+ (DM110-3)	Overflow - Detects and stores the overflow condition on all arithmetic operations.
PDIX (DM112-2)	Program Data In - Provides timing function for all programmed input operations.
PDTX+ (DM112-2)	Program Data Transfer - Provides timing function for all input/output instructions.
PFOX- (DM112-2)	Program Function Out - Timing function that controls the output of function code of all I/O instructions.
PHCX- (DM112-1)	Phase Clock - Basic timing function used to control basic clock functions such as CL1X+ and CL2X+.
REPT- (DM109)	Repeat - Controlled by the instruction REPEAT switch on console. Used to enable setting of RPCX flip-flop.
ROHX+ (DM109-2)	Reset On Halt - Reset line to control flip-flops on halt.
RPCX- (DM109-2)	Repeat Control - Control function which inhibits set U register (SURX+) when stepping in repeat mode.
RR15+ (DM110-3)	Repeated R15 - Monitors bit 15 of the R register.
RSHX+ (DM110-3)	Reset Shift Function - Resets shift functions on halt and CL2.
RSTX (DM110)	Reset - Controlled by the display register reset switch on console. Resets the bits of any register being displayed while in step.
RTDX+ (DM104)	Read Driver Timing - Timing signal which enables read drivers during memory read operation.
RTSX+ (DM104)	Read Switch Timing - Timing signal which enables read switches during a memory read operation.
RUNX+ (DM109)	Run - Output of RUN switch on the console. Used to form a pulse which places the computer in the run mode.
SABX- (DM110-2)	Select A Bus - Used by MicroOEXEC option to select A bus.
SBAX+ (DM110-3)	Sign Bit of A Register - Stores sign bit of A register for jump, multiply and divide instructions.
SBLX+ (DM110-3)	Select Bus Last Bit - Bits 15 or 17 on S bus.

SCMX+ (DM112-2)	Shift Count Met - The count in the shift counter equals that in the U register bits U0 to U4.
SC0X+ to SC4X+ (DM112-2)	Shift Counter, Stages 0 to 4 - Counts shift cycles during multiply and divide instructions.
SELA+ (DM109)	Select A Register - Output of A register select switch on the console. Used to select A register during the step mode.
SELB+ (DM109)	Select B Register - Output of B register select switch on the console. Used to select B register during the step mode.
SELP+ (DM109)	Select P Register - Output of select P register switch on the console. Used to select the P register during the step mode.
SELU+ (DM109)	Select U Register - Output of select U register switch on the console. Used to select the U register during the step mode.
SELX+ (DM109)	Select X Register - Output of select X register switch on the console. Used to select X register during the step mode.
SERX- (DM109)	Sense Response - Signal returned by a peripheral device to indicate the status of the device. Occurs in response to a sense command.
SETA+ (DM111-1)	Set A Register - Clock used to set C bus data into A register.
SETB+ (DM111-2)	Set B Register - Clock used to set C bus data into B register.
SETL+ (DM112-3)	Set L Register - Clock used to set C bus data into L register.
SETP+ (DM111-2)	Set P Register - Clock used to set C bus data into P register.
SETR+ (DM111-2)	Set R Register - Clock used to set W bus data into R register.
SETU+ (DM111-2)	Set U Register - Clock used to set W bus data into U register.
SETW+ (DM112-3)	Set W Register - Clock used to set C bus data into W register.
SETX+ (DM111-2)	Set X Register - Clock used to set C bus data into X register.
SGAX+ (DM112-1)	Shift Gate A - Provides bit 0 to shift left gates of arithmetic unit on shift left and multiply instructions.
SGBX+ (DM112-1)	Shift Gate B - Provides bit 14 to shift right gates of arithmetic unit on shift right and multiply instruction.
SGCX+ (DM112-1)	Shift Gate C - Provides bit 15 to shift right gates to arithmetic unit on shift right and multiply instructions.

SGDX+ (DM112-1) — Shift Gate D - Provides bit 15 to shift left gates on arithmetic unit on shift left and divide instructions.

SHCX+ (DM112-2) — Shift Control - Provides basic timing and control of shift, multiply and divide instructions.

SHFX- (DM112-2) — Shift - Enables shift operation on shift, multiply and divide.

SHLX+ (DM112-1) — Shift Left - Enable shift left gates on shift left and divide instruction.

SHRX+ (DM112-1) — Shift Right - Enables all shift right gates for shift right and multiply instructions.

SLAB+ (DM110-2) — Select Arithmetic Bus - Selects output of adder to C bus.

SLAX+ (DM111-1) — Select A Register - Gates A register on to the S bus.

SLBX+ (DM111-1) — Select B Register - Gates B register on to the S bus.

SLGB+ (DM110-2) — Select G Bus - Selects G bus in to the adder.

SLPX+ (DM111-1) — Select P Register - Gates the P register on to the S bus.

SLRI+ (DM111-3) — Select R Inverted - Gates the output of R inverted to the G bus.

SLRX+ (DM111-3) — Select R - Gates the output of the R register to the G bus.

SLU1+
SLU2+
SLU3+
(DM111-1) — Select U - Selects the U register on to the G bus.
SLU1+ - Selects U0-U8
SLU2+ - Selects U9-U10
SLU3+ - Selects U11-U15

SLXX+ (DM111-3) — Select X Register - Gates the X register onto the S bus.

S00X to S17X (DM119) — Sense Lines 0 to 17 - Sense line outputs 0 through 17 from memory core stack.

S0P2 (DM109) — Step Pulse - Pulse initiated from step switch on console which allows one instruction to be performed.

SOPX+ (DM109-2) — Stop - Provides control for manual halt and step operations.

SRSX+ (DM109-1) — Single Register Selected - Enables setting of MRSX when single register is selected.

SSAX+ (DM109-1) — Switch Select A Register - Flip flop set by A register switch on console used to manual select the A register.

SSBX+ (DM109-1)		Switch Select B Register - Manual select of B register from console.
SSEX (DM106)		Sense Strobe - Timing signal which strobes the sense outputs of the core stack into the W register.
SSPX+ (DM109-1)		Switch Select P Register - Manual select P register from console.
SSUX+ (DM109-1)		Switch Select U Register - Manual select U register from console.
SSXX+ (DM109-1)		Switch Select X Register - Manual select X register from console.
STB5- (DM111)		Set B Register - Pulse from multiply/divide option which is used to set the B register.
STEP+ (DM109)		Step Command - Output of step switch on console. Used to initiate the step mode.
STL1- (DM112-3)		Set L Register - Signal used by Micro-EXEC option to set the L register.
STP1- (DM111-2)	(PEN17)	Set P Register - Signal used by Micro-EXEC option to set P register.
STP1- (DM111-2)		Set P Register - Output of set gates to select P register.
STRX+ (DM109-2)		Start - Provides control for manual step and run operations.
STW1- (DM112-3)		Set W Register - Signal used by Micro-EXEC option to set W register.
SU00+ SU17+ (DM108)		Sum 00 to 17 - Output of adder.
SYRT-I (DM109-1)		System Reset - Ground true signal in computer and on I/O bus to reset computer and I/O devices.
TAIX- (DM112-3)		Trap Address Input - Signal from DMA/I option (DM121) which selects time when an address is inputted during a trap or interrupt operation.
TCRX- (DM106)		Timing and Control Reset - Reset to memory timing and control circuitry.
TD1W- (DM112-3)		Trap Data In Write - Signal from DMA/I option which initiates a write signal (WRTX+) to the memory on the second half cycle of trap in.
TOSX (DM112-1)		Trap On Shift - Signal from DMA/I option which detects and stores trap command on a shift, multiply or divide instruction.
TRSC (DM109)		Trap Start Clock - Signal from DMA/I option which initiates a memory start pulse.

TSEX+
(DM120)

Threshold Voltage - Reference voltage used in the sense amplifiers to discriminate between ONEs and ZEROs on the memory core stack sense lines.

TZXX+
(DM106)

Inhibit-Timing Pulse - Enables inhibit drivers during a memory write operation.

U00X+
U17X+
(DM108)

U Register Bits 0 to 17 - Provides storage of all instructions during the execute cycle.

W00X+
W17X+
(DM108)

Memory Data Register - Holds data for memory read/write instructions.

WRTX+
(DM112-3)

Read/Write Command -

A. For Full Cycle - When true, enables clear/write operation of the memory. When false, enables read/restore operation.

B. For Half Cycle - When true, enables a write (only) operation. When false, enables a read (only) operation.

WTDX+
(DM104)

Write Driver Timing - Timing signal which enables write drivers during a memory write operation.

WTSX+
(DM104)

Write Switch Timing - Timing signal which enables write switches during a memory write operation.

XDRX
(DM120)

X Drive Current - Half-select current for X drive lines.

YDRX
(DM120)

Y Drive Current - Half-select current for Y drive lines.

Z00X to Z17X
(DM119)

Inhibit Drive Outputs 00 Through 17 - Inhibit line outputs 0 through 17 to the core stack.

CHAPTER 7
DIAGNOSTIC PACKAGE

1.1 INTRODUCTION

The DATA 620/i diagnostic program package is designed to check instructions, memory and input/output devices, and to isolate errors. Maintenance time can be minimized in testing for malfunctions if the diagnostic routines are used. The diagnostic package can be used in either the preventive or the corrective mode of operation. The preventive mode of operation determines whether a malfunction exists and, in most cases, isolates the error. The corrective mode of operation is used when a malfunction is known to exist, and the preventive mode of operation does not decisively show the trouble.

Diagnostic routines, and preventive/corrective modes of operation are discussed in the following paragraphs.

1.1.1 Diagnostic Routines

The diagnostic routines included in this manual are the memory test routine, the instruction test routine, the model 33/35 (type B) teletype test routine (check model number for proper routine), the disc test routine, the paper tape system test routine, the line printer test routine, the card reader test routine, and the model 33 (type A) test routine. All routines are completely self-contained, and may be run independently of any other routines when used in the corrective mode of operation. Each routine provides several basic tests and combinations of basic tests. The magnetic tape diagnostic program is not considered part of the diagnostic package, but as a diagnostic program in itself. Since it cannot be executed from the driver, it must be loaded and executed from the console.

1.1.2 Preventive Mode of Operation

In the preventive mode of operation, a specific diagnostic program is loaded into memory, and the teletype keyboard is used to initiate tests or a sequence of tests.

The diagnostic teletype driver routine for preventive mode of operation (section 3) interprets the keyboard input and calls each of the designated diagnostic routines the number of times specified in the sequence.

1.1.3 Corrective Mode of Operation

In the corrective mode of operation, a diagnostic routine may be loaded and run independently of any other routine. Each diagnostic test is manually initiated from the DATA 620/i console. A unique entry address is provided within the diagnostic routine for each test. Parameters are manually supplied in the A, B and X registers. SENSE switch 2, if selected at the completion of a test ~~(except the basic and sense switch instruction tests)~~, causes the test to be repeated using the same parameters. Regardless of errors

1.2 STORAGE

The memory test routine destroys the lower 2048_{10} words of each 4096_{10} words of memory. The instructions test routine can destroy portions of memory including $0\text{-}40_8$ words. The magnetic tape diagnostic, since it can write and read variable length records, may destroy any core location where it is not itself occupied. The disc test uses $0\text{-}1777_8$ and $4000\text{-}5777_8$, as INPUT-OUTPUT BUFFERS.

1.3 ERROR INDICATIONS

Error messages on the teletype are normally provided by the instructions test routine and the memory test routine. However, if SENSE switch 1 is selected at the time of error detection, the printout is suppressed and a halt occurs.

The model 33 teletype (type A) test routine accumulates the read errors in a table, and a special entry address allows this table to be printed. In addition, if SENSE switch 1 is selected at the time of error detection, a halt occurs, displaying the bits in error, the expected result and the read address in the A, B and X registers, respectively.

The teletype (type B) test routine accumulates read errors and prints total at completion of test. SENSE switch 1 has no effect on this test.

The paper tape system test routine halts upon detection of a read error if SENSE switch 1 is set, otherwise the errors are counted and the routine proceeds.

The line printer test routine prints the message PARITY on the line printer each time a parity error is detected. A halt will follow this printout if SENSE switch 1 is set.

The card reader test routine accumulates read errors and number of cards read and prints out totals at completion of test. If SENSE switch 1 is set, an error causes a halt with bits in error displayed in the A register.

The disc memory test routine has many error messages. Reference to the error messages can be found in the disc memory test routine section.

1.4 THE MAINTAIN PACKAGE

The MAINTAIN package is designed to assist the maintenance engineer in verifying correct operation of the computer system and detecting failures or potential failures. A MAINTAIN tape is provided with the DATA 620/i computer. The tape contains all tests necessary for any of the system options. The tests occur in the following order in the tape: (1) teletype driver, (2) memory, (3) instruction and (4) teletype. Any additional peripheral tests follow these with their order appearing on the test tape label. Each diagnostic program is separated from the others by a section of tape with only level 8 punched (level 8 is not used in binary format except for leader and trailer).

1.4.1 Loading the MAINTAIN Package

Position the MAINTAIN tape so that level-8 punches are over the read station. Using the binary load program at X7600, with A>0 (load and execute) the MAINTAIN driver program can be read into memory. All other programs may be read into memory by using the function RUN b X7600. RUN is the function which transfers program control to the point described by the octal number that follows the b (blank). Control is returned to the driver when loading is completed.

Each program segment, (1) memory, (2) instructions, (3) etc, should be read into memory and executed separately. When the program completes loading, the teletype prints $. Any legal function may then be requested. If a format error is made, the teletype takes control and prints MSG followed by $. Another operator request may then be made.

1.4.2 Requesting Function

Each legal function may be called by typing the correct mnemonic (function name) on the teletype. A list of function names is contained in appendix J .

1.4.3 Running a Test

The following list describes a step-by-step procedure for testing a central processor and teletype unit. This procedure can serve as a guide for using the diagnostic routines included in this manual.

a. Place the LINE/OFF/OFF-LINE switch to the LINE position.

b. Load the driver via the binary loader. If the mode of loading was LOAD AND HALT, entry to the driver is gained through the following sequence:

   1. Set P register to 06000.
   2. Set U register to 0.
   3. Press the SYSTEM RESET and RUN switches. This results in the printout of $.

   To load a test program, type RUN b X7600. This calls the binary loader and returns to the driver upon completion of loading.

c. To run the memory test for all of memory, type the call name MEMO. This tests the complete memory. If an error is found, the program location of the detected error is printed along with the value of the A, B and X registers at that time. Since this test repeats sequences 30 times per 2048-word block, the listing can get large. Therefore, upon detection of an error, terminate this test and refer to the memory test routine for the corrective mode of operation. Proper completion of this test results in the print-out of the words END MEMO. Total time required for this test is about 35 seconds for each 4096-word run.

d. Using the RUN function described in section 5.3, type RUN b X7600 to load the instructions test. The entire instructions test can be executed by typing INST. This test finishes in less than one second and proper operation results in immediate print-out of END INST. Detection of an error causes a print-out of the program location of the detected error and the values of the A, B and X registers at that time.

e. Using the RUN function, type RUN b X7600 to load the teletype test. The teletype test is a divided program consisting of several sections for testing individual operations or groups of operations. Included are page printer, keyboard, tape reader and tape punch. Each test is executed separately since it is not possible to execute all tests with one call. The following procedure describes the test sequence:

   To test the page printer, type PPAC. The resulting print-out is a rotating pattern of the complete character set. Upon completion, the words END PPAC are printed. Visually inspect the printed listing for errors.

To test keyboard accuracy, type KBAC. This results in print-out of all lower case characters followed by a wait for the operator to type all lower case characters. Then, all upper case characters are printed followed by a wait for operator typing of all upper case characters. The test ends with print-out of the words END KBAC.

Refer to the model 33/35 teletype test routine (section 6) for testing of the paper tape reader and punch.

The above tests describe a step-by-step routine which can be followed for general preventative maintenance purposes.

2.1 INTRODUCTION

Table 2-1 lists symbolic entry addresses. Transfer actual octal addresses from assembly listings to this table. For future reference, these addresses permit execution of a specific section within a test.

Table 2-1
Entry Addresses

Codes:

P Preventive mode of operation only

C Corrective mode of operation only

Entry Address		
Symbolic	Code	Explanation
GENT	P	Diagnostic teletype driver routine for preventive mode of operation.
		Model 33 (type A) teletype test routine·
TP	C	Punch/print test
TRH	C	Read paper tape (high speed)
TRL	C	Read paper tape (low speed)
TRK	C	Read keyboard test
TRHP	C	Read paper tape (high)/punch/print test
TIK	C	Teletype transfer instructions test (keyboard input)
TRKP	C	Print error table
		Memory test routine:
MADR	C	Memory address verification test
MPAT	C	Memory pattern test
MEMO	C	MADR and MPAT for all of core
		Instructions test routine:
IBAS	C	Basic and SENSE switch instructions test
IREG	C	Register change instructions test

Table 2-1 (continued)

Entry Address		
Symbolic	Code	Explanation
ILOD	C	Load/store instructions test
ILOG	C	Logical instructions test
IOVF	C	Overflow instructions test
IJMX	C	Jump/execute instructions test
ISHF	C	Log/arithmetic shift instructions test
IARS	C	Standard arithmetic instructions test
IARO	C	Optional arithmetic instructions test
IEXA	C	Extended addressing test
INST	C	Sequence of test except IBAS
		Paper tape system test routine:
PRH	C	Read paper tape (high speed)
PRS	C	Read paper tape (step)
PP	C	Punch paper tape
		Line printer test routine:
LPRD	C	Diagonal format test
LPRL	C	Line and slew test
LPRB	C	Combination diagonal and line/slew
LPRS	C	Character test
		Model 33/35 (type B) teletype test; ASR and KSR models:
PPAC	C	Page printer accuracy

Table 2-1 (continued)

Entry Address		
Symbolic	Code	Explanation
		ASR models:
PTSP		Print suppress
RDCT	C	Reader control
PCTL	C	Punch control
RPCA	C	Reader/punch accuracy
		Card reader test:
RDAC	C	Read cards
		Disc memory test routine:
DPAT	C	Disc pattern test
DISC	C	Full disc test

3.1 IDENTIFICATION

This section describes the following diagnostic routine:

Title: MAINTAIN teletype driver routine for preventive mode of operation, diagnostic package.

Identification: DIAG.

Category: G, E3, C3, D3.

3.2 PURPOSE

This routine provides the operator a means to run a diagnostic test or a series of diagnostic tests. The user must provide the appropriate test identifiers and parameters through the teletype keyboard. This routine interprets input and call signals through appropriate diagnostic routines the number of times, and in the sequence specified, to accomplish test functions. Diagnostic tests which can be run, and a summary of test identifiers and parameters required for each test, are listed in appendix A. A halt function is performed by this routine and allows the user to select the teletype OFF. The routine is activated again by pressing the RUN switch on the DATA 620/i console. Run is the function that will aid in loading test programs. Typing RUN b X7600 will call the binary loader and return control to the driver upon completion of loading.

3.3 USAGE

Operational procedures: To run a diagnostic package, the operation proceeds as follows:

a. The user loads the diagnostic driver and initiates the routine by running at symbolic location GENT.

b. This routine prints the carriage return, line feed, $, and space characters to indicate it is ready to accept keyboard input.

c. The user types the desired diagnostic control message on the keyboard.

e. If the control message is acceptable, the routine calls the diagnostic routines to accomplish the requested test functions. At the completion of each test, the routine prints the carriage return, line feed, E, N, D and space characters followed by the test identifier characters. The procedure then continues with step b.

Arguments or parameters: Some diagnostic tests require parameters furnished by the operator through the teletype.

Space required: Approximately 421 words.

Temporary storage requirements: Not applicable.

Alarms or printouts:	See operational procedure.
Error returns or error codes:	Not applicable.
Error stops:	An error halt occurs at symbolic location G98 if the teletype does not respond favorably to the sense-teletype-not-busy or the sense-buffer-ready instructions within a reasonable time. If this occurs, the preventive mode of operation should be discontinued.
Input and output devices:	Input is obtained from the teletype keyboard and output is provided to the page printer of the teletype.
Input and output formats:	Rules regarding the format of the diagnostic control message are listed below:

a. The user types the diagnostic test identifier immediately following $ and space characters provided by the routine.

b. If parameters are required, they are typed following the identifier. Each parameter is provided as an octal number preceded by a space.

c. An optional repeat count may be provided next as an octal number preceded by a space. This will cause the test to be repeated the specified additional number of times.

d. Additional sets of diagnostic test identifiers, parameters, and repeat counts are optional. These sets are separated by comma and space characters.

e. Following the last diagnostic set, a repeat count of the entire sequence may be specified as an option. This repeat count is provided as an octal number preceded by semicolon and space characters.

f. Each diagnostic control message must be terminated by a period.

g. The leading zeros of an octal number may be omitted. Only the low-order bits (word size) of the octal number are used. This feature is provided to facilitate correction of a typing error. Examples of some typical teletype printouts are given below:

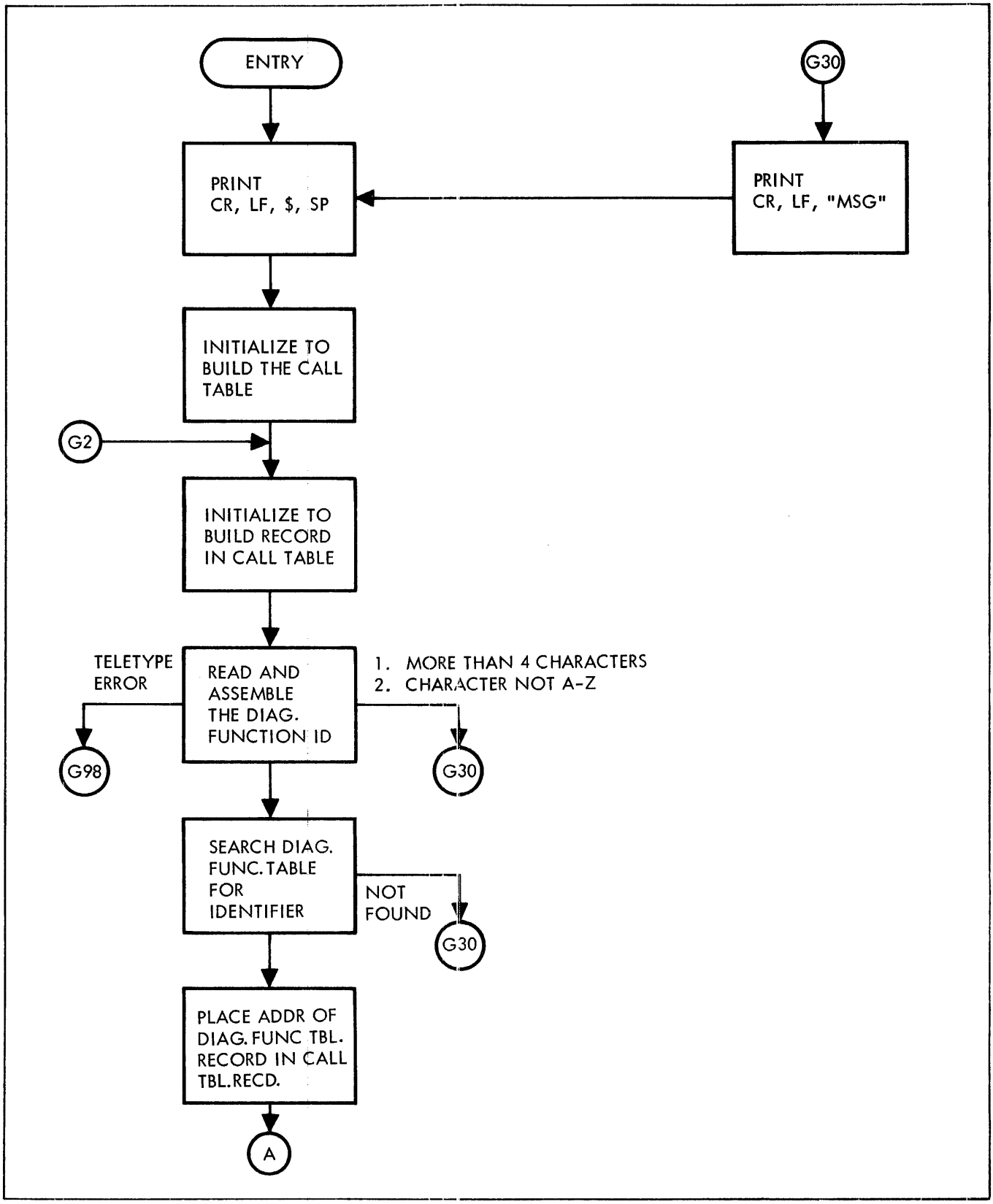
Printout	
$ IREG. END IREG $	Run the register change instructions test one time.
$ MPAT 4000 242. 004171 111111 177777 001777 END MPAT $	Run the memory pattern test one time. Error printout provided by memory test.
$ IREG 2, ILOD;1.	Run IREG three times followed by ILOD once. Then repeat the sequence once.

```
END IREG
END IREG
END IREG
END ILOD
END IREG
END IREG
END IREG
END ILOD
$                                   Ready to accept another diagnostic
                                    control message.
```

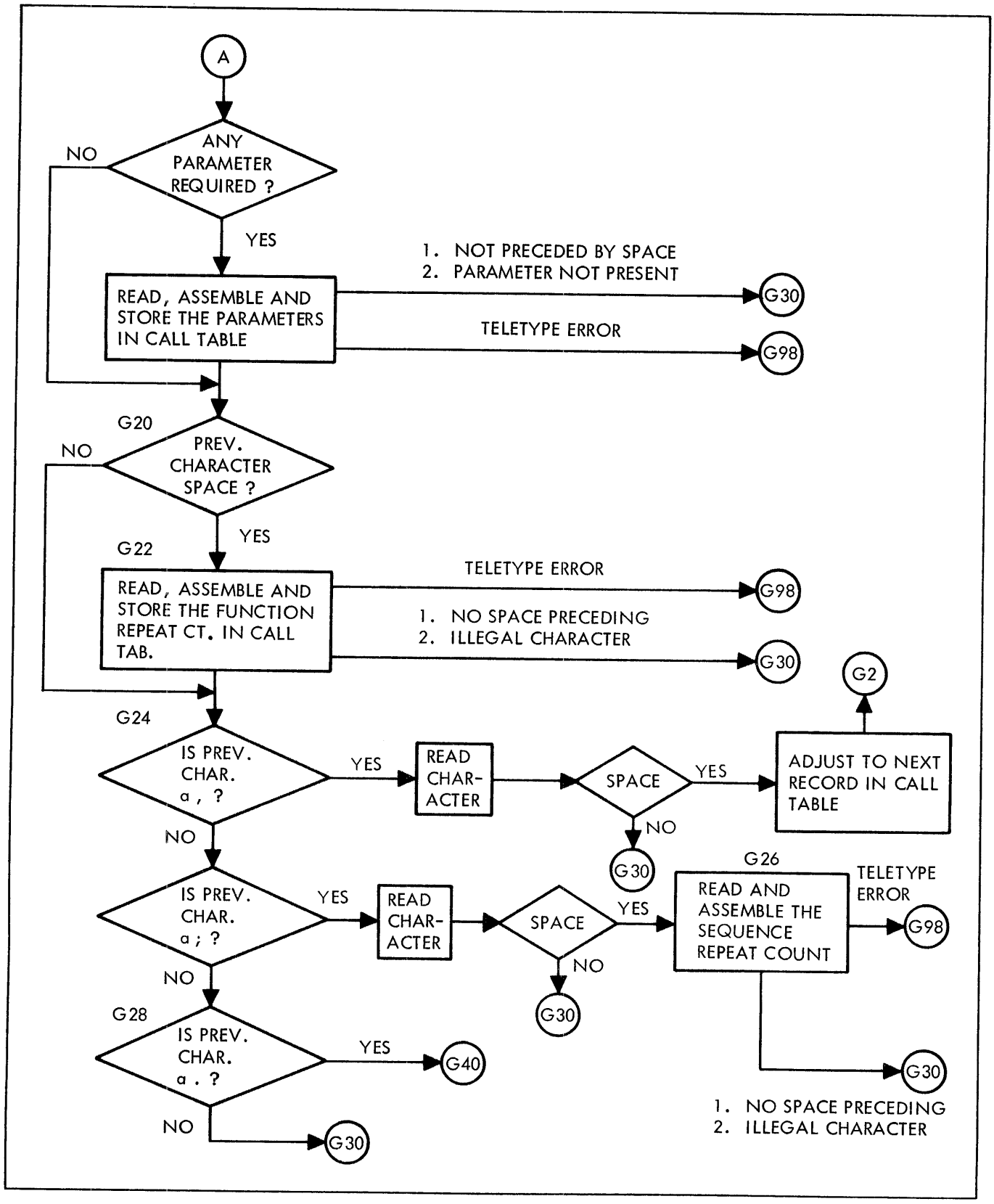
SENSE switch settings:	SENSE switch settings do not affect this routine, but may affect the diagnostic routines which are called.
Timing:	Not applicable.
Accuracy:	Not applicable.
Cautions to users:	This program must be loaded before the test program to operate properly in the preventative mode. Each test routine supplies the driver with its function name table. If the driver is not in memory, proper communication linkage is not made.
Equipment configuration:	Minimum configuration is with model 33 teletype (type A) or a model 33/35 teletype (type B).
References:	Not applicable.

3.4 METHOD

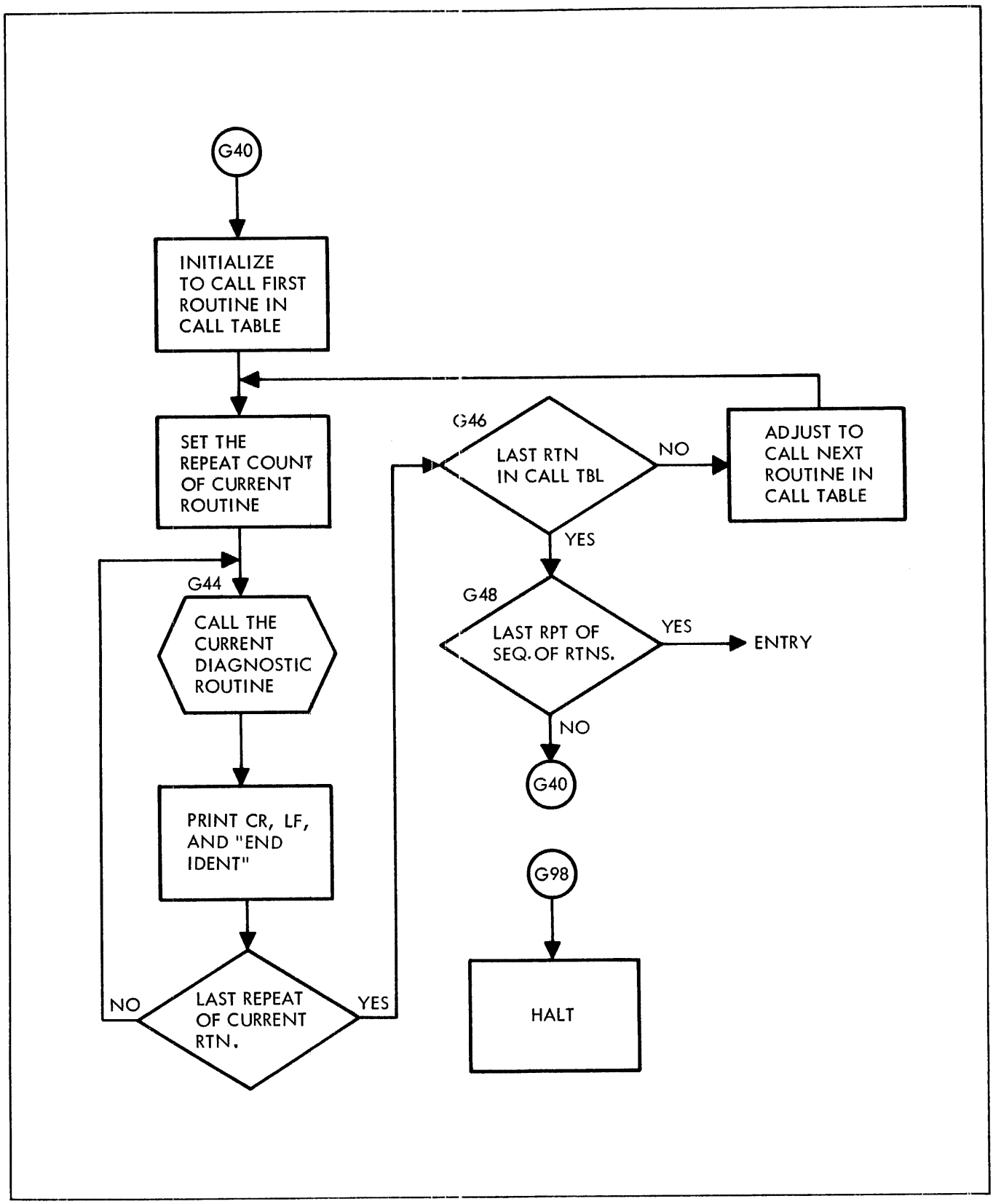
The methods used in this diagnostic routine are illustrated in the flow charts on the following pages.



MAINTAIN Teletype Driver Routine



MAINTAIN Teletype Driver Routine



MAINTAIN Teletype Driver Routine

4.1 IDENTIFICATION

The following paragraphs describe the operational procedure followed in a memory test routine:

Title: Memory test routine, diagnostic package.

Identification: MEMO.

Category: G2

4.2 PURPOSE

This routine contains a memory address verification test and a memory pattern test with separate entries provided for each test. The test stores, reads back and tests data within a specified block of the core memory. Two calls are required to test a full memory bank*. The routine also provides an entry which causes both the memory tests to be run for each block of core memory. Flow charts illustrating these tests are found at the end of this section.

The memory address verification test determines if a unique address exists for each cell in a specified block of core memory. The memory pattern test allows a data pattern to be written in a specified block so that noise generated during write and read operations indicates memory problems.

4.3 USAGE

Operational procedure: The procedure for the preventive mode of operation is described in section 3, MAINTAIN teletype driver routine for preventive mode of operation, diagnostic package. The following procedures are for the corrective mode of operation:

a. Memory address verification test:

1. Place parameter 1 in the A register.
2. Select SENSE switches as desired.
3. Run at symbolic location MADR.

reads twice

b. Memory pattern test:

1. Place parameter 1 in the A register.
2. Place parameter 2 in the B register.
3. Select SENSE switches as desired.
4. Run at symbolic location MPAT.

P- 4000
1 or 2
4006 - Corrective Mode

c. Sequence of the above tests for each block of core memory:

1. Select SENSE switches as desired.
2. Run at symbolic location MEMO.

4015 - Corrective Mode

*For purposes of this publication, a memory bank is defined as 4096 words, with consecutive addresses and with the low-order 12 bits of the address in the range 0 - 4095. A block is defined as either the lower or upper half of a memory bank.

Arguments or parameters:

a. Memory address verification:

Parameter 1 is the address of the core block to be tested.

b. Memory pattern test:

1. Parameter 1 is the low order address of the core block to be tested.
2. Parameter 2 is a mask of selected bits which govern the word pattern stored at a given address.

Space required: Approximately 430 words are required for storing this routine.

Temporary space requirements: The block of memory being tested is filled with its own addresses (MADR), or with words of all ones and all zeros (MPAT).

Alarms or printouts: A printout normally occurs when an error is detected. The user may bypass this printout and cause a halt by selecting SENSE switch 1. The error printout consists of: an error address, the A register contents, the B register contents and the X register contents.

The error address is the octal equivalent of symbolic location N12 + 2 for a memory address verification error. It is the octal equivalent of symbolic location P20 + 2 for a memory pattern error.

The A register contains the bits of the data word in error. The error is determined by performing an exclusive-OR operation on the word read from memory and the expected result.

The B register contains the expected result of the read operation.

The X register contains the address of the data word in error.

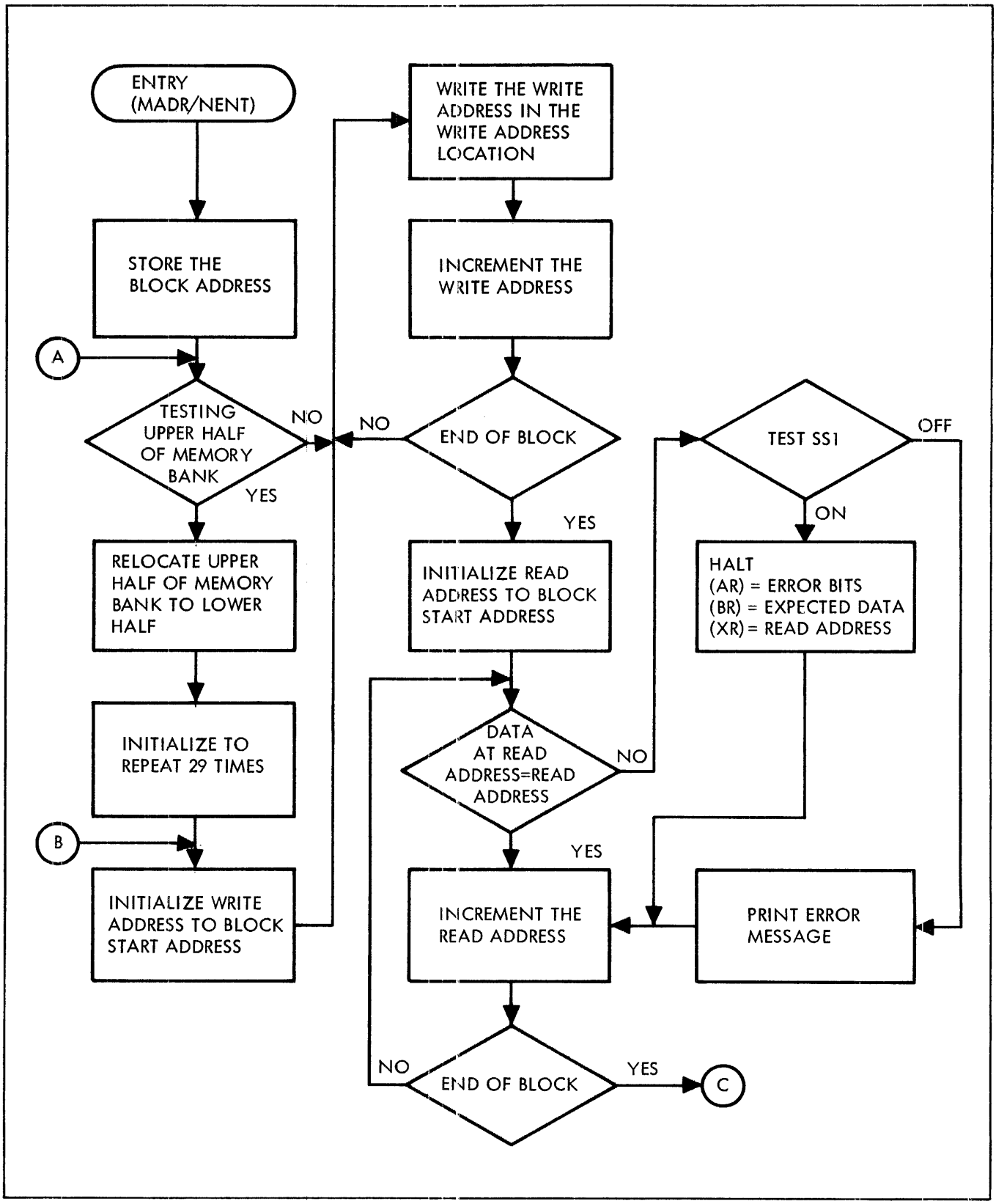
Error returns or error codes: See error stops and alarms or printouts for a description of error codes.

Error stops: An error halt occurs when an error is detected if SENSE switch 1 is selected. The error code, displayed in the instruction counter, contains the address of symbol N13 + 1 for a memory address verification error, or of symbol P21 + 1 for a memory pattern error. The A, B and X registers contain the same information as defined in alarms and printouts. To continue, following an error halt, press the RUN button.

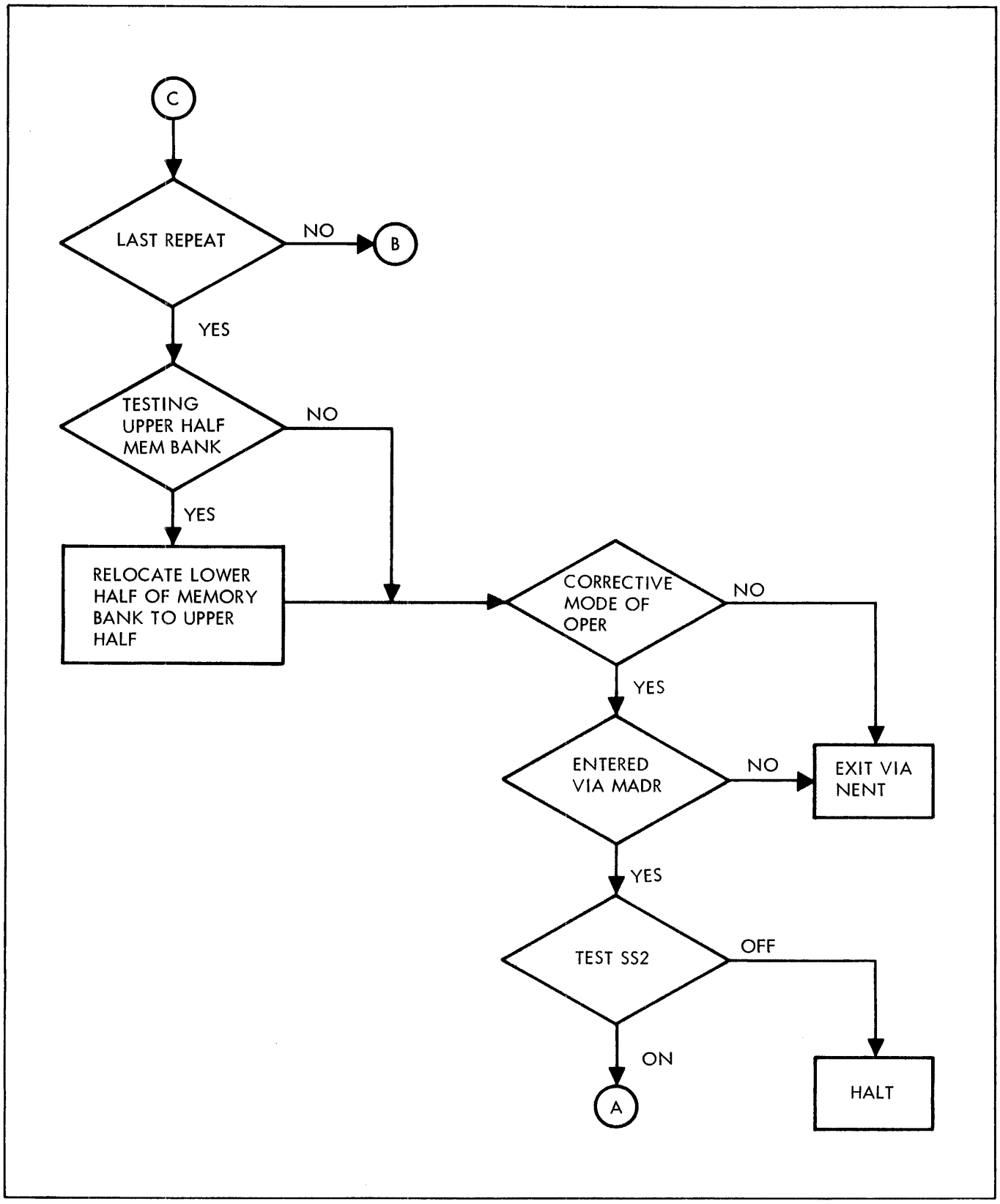
An error halt occurs at symbolic location MQ98 if the teletype does not respond favorably to the sense-teletype-not-busy or the sense-buffer-ready instructions within a reasonable time when trying to print an error message.

Input and output devices: The model 33/35 teletype is used to print error messages.

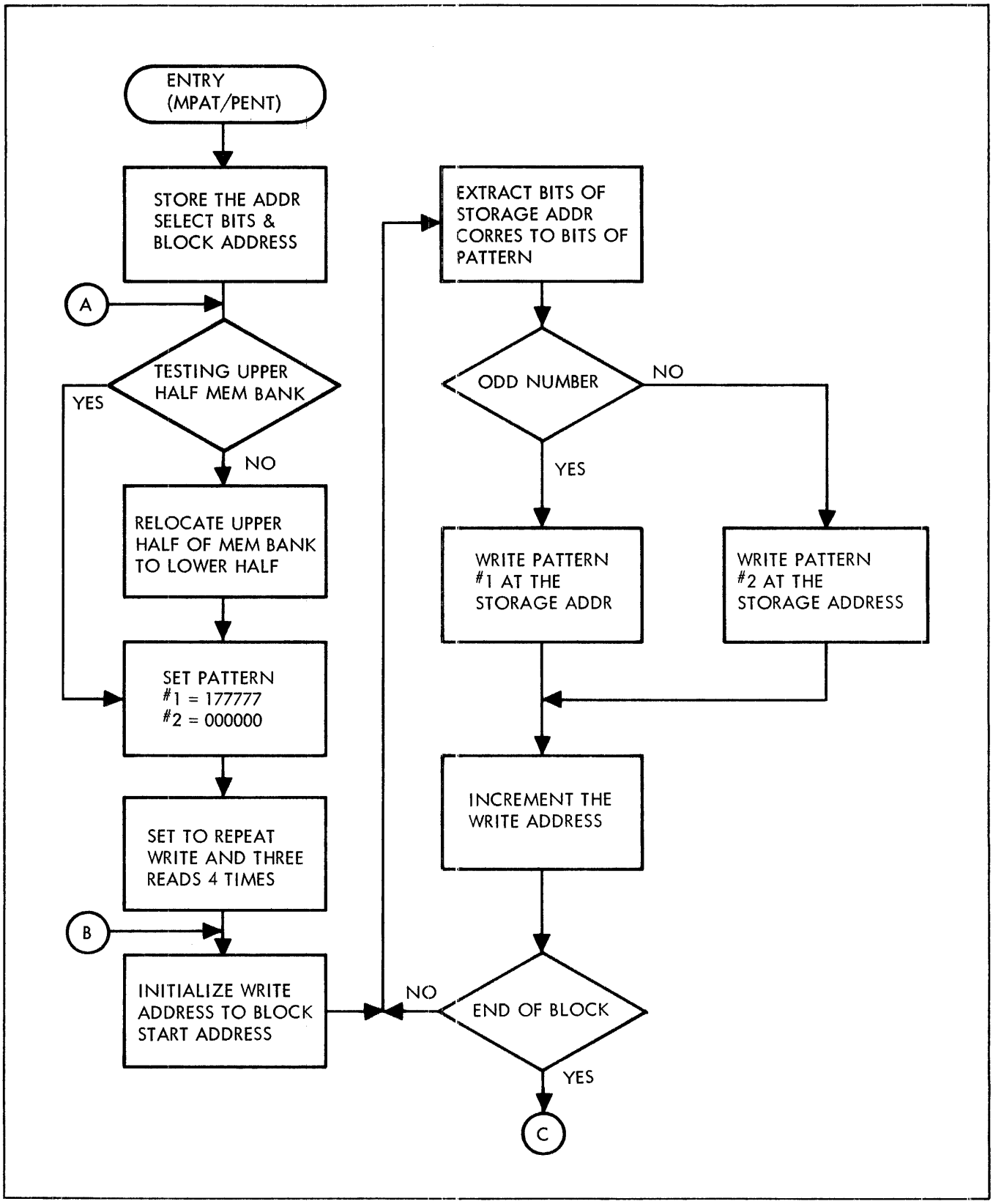
	Input and output formats:	See alarms or printouts.
	SENSE switch settings:	SENSE switch 1, if selected, causes an error halt instead of error print upon detection of an error. If SENSE switch 2 is selected at the completion of the test, and if the user is operating in the corrective mode, the same test is repeated using the same parameters.
	Timing:	Not applicable.
	Accuracy:	Not applicable.
	Cautions to operators:	The contents of the lower half of the memory bank being tested are destroyed. This routine is assembled to operate in the upper half of a memory bank.
	Equipment configuration:	Minimum configuration. The model 33/35 teletype is required to obtain error printouts.
	References:	Not applicable.
4.4 METHOD	Memory address verification test:	The address of the cell is written in each cell of the specified core memory. The contents of each cell in the block is read and tested to verify that a unique address exists for each cell. This process is repeated 29 times.
	Memory pattern test:	The test sequence writes, in each cell of the specified core block, a word of all ones or all zeros, depending on whether there is an odd or even number of bits selected in specified bit positions of the cell address (i.e., the cell address is ANDed with parameter 2 and the resulting one bits are counted for an odd or even number). All data in the block are then read and tested three times. The write and three reads are repeated four times, alternating the word written in each given cell between all ones and all zeros. Before testing the upper half of a memory bank, all data from the upper half are moved to the lower half. Upon completion of the test, the data are restored to the upper half of the memory bank. This routine is capable of operating in the lower half of a memory bank as well as the upper half, so that both halves of a memory bank may be tested.



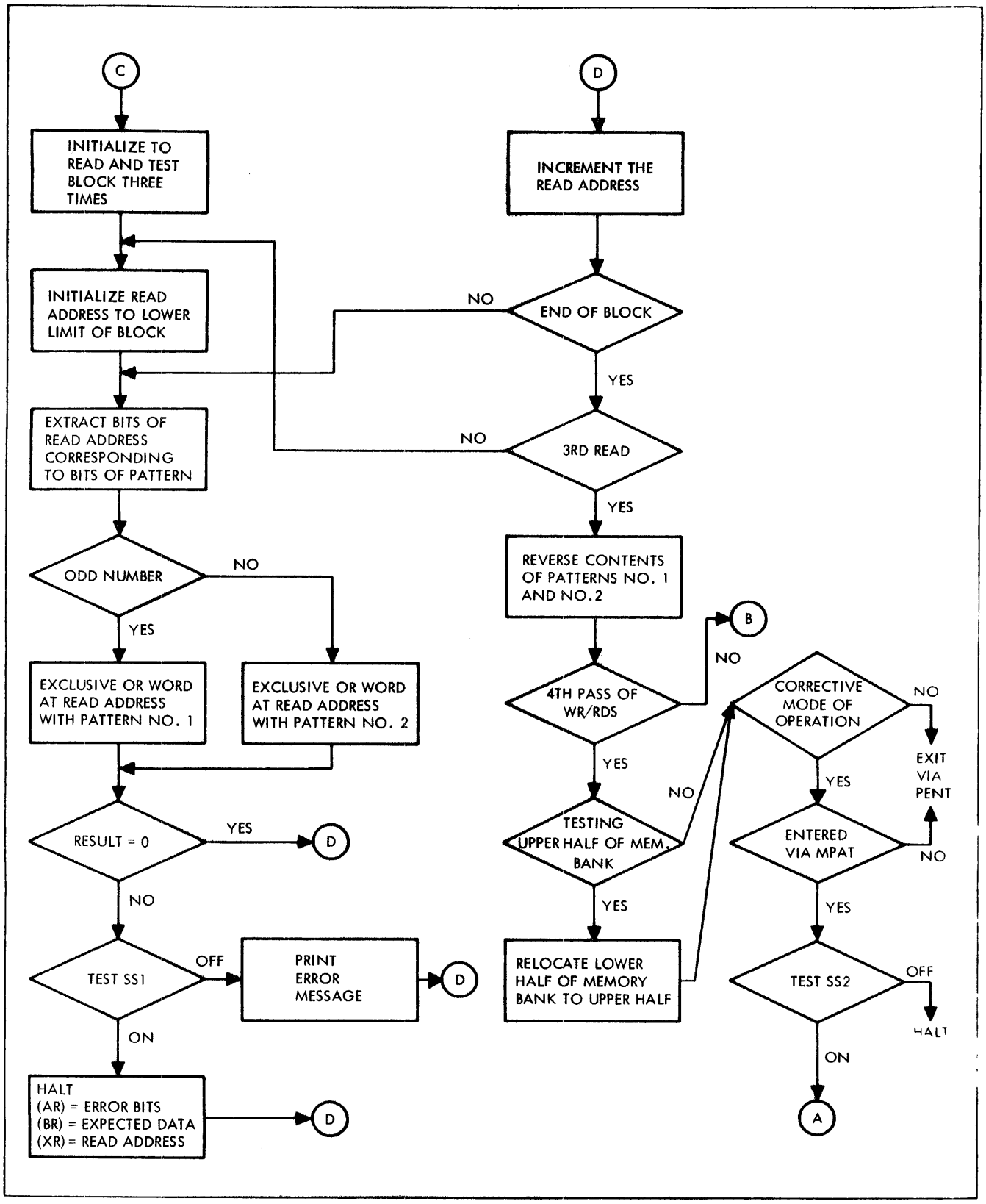
Memory Address Verification Test



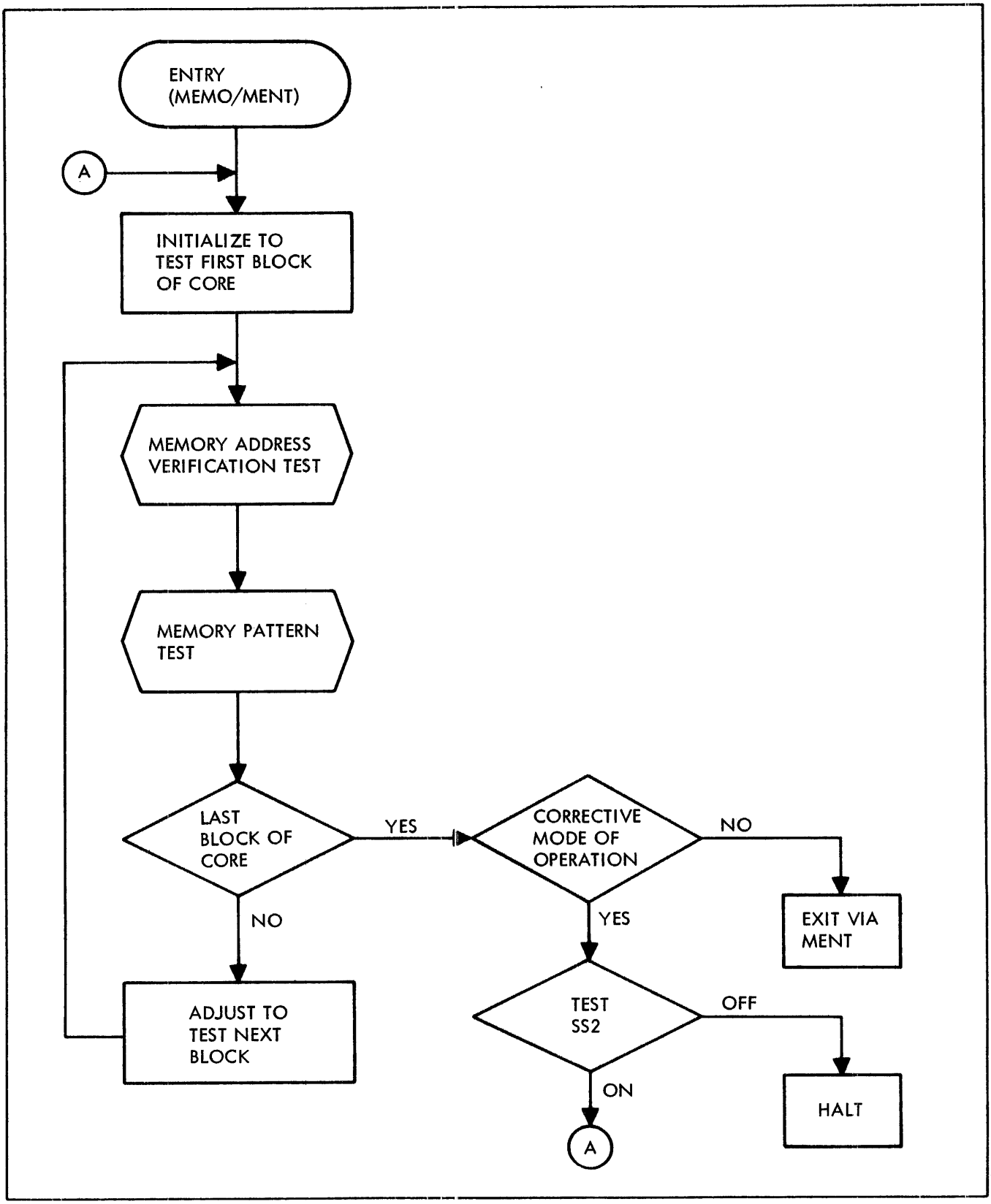
Memory Address Verification Test



Memory Pattern Test



Memory Pattern Test



Memory Test Sequence

5.1 IDENTIFICATION

The following paragraphs describe the procedures used in the instructions test routine:

Title: Instructions test routine, diagnostic package.

Identification: INST.

Category: G1.

5.2 PURPOSE

This routine can be used to test all DATA 620/i machine instructions except input/output instructions. The instructions have been classified as:

a. [redacted] SENSE switch.

b. Register change.

c. Load/store.

d. Logical.

e. Overflow.

f. Jump execute.

g. Logical and arithmetic shifts.

h. Standard arithmetic.

i. Optional arithmetic.

j. Extended addressing.

Separate entries for testing each class of instruction are provided. Also provided is an entry for testing in series, all classes of instructions. Instructions i and j are optional, and are included only as required by the DATA 620/i computer.

The basic and SENSE switch instructions test can be used only in the corrective mode of operation, since setting and resetting of SENSE switches must be done through the DATA 620/i console. All other instruction tests are available in both modes of operation.

The recommended sequence for testing instruction classes in the corrective mode of operation is as listed in the first paragraph of this section. When used in this sequence with SENSE switch 1 selected, any instruction used to test another instruction has already been tested. The only instruction assumed to work properly is the HLT instruction.

5.3 USAGE

Operational procedures: The procedures used for the preventive mode of operation are described in section 3, MAINTAIN teletype driver routine for preventive mode of operation, diagnostic package.

The corrective mode of operation is as follows:

a. Select SENSE switches as desired.

b. Set the instruction counter to the octal address associated with one of the following symbolic locations:

~~IBAS~~	~~Basic and SENSE switch~~
IREG	Register change 1504 = P
ILOD	Load/store 1511 = P
ILOG	Logical 1516 = P
IOVF	Overflow 1523 = P
IJMX	Jump/execute 1530 = P
ISHF	Logical and arithmetic shifts 1535 = P
IARS	Standard arithmetic 1542 = P
IARO	Optional arithmetic 1547 = P
IEXA	Extended addressing 1554 = P
INST	Series of tests 1561 = Option 1547 = No Option

P/N 2.2 Optional
2.0 standard

c. Run.

Arguments or parameters: Not applicable.

Space required: Approximately 1550 words.

Temporary space requirements: Not applicable.

Alarms or printouts: Normally, a printout occurs upon detection of an error. The user may bypass this printout and cause a halt by selecting SENSE switch 1. The error printout consists of: an error address, the A register contents, the B register contents and the X register contents, respectively.

Error returns or error codes: The error address which is either printed (SENSE switch 1 off), or left in the instruction counter (halt caused by SENSE switch 1 being on), identifies the type of error. The register contents may or may not be significant.

	Error stops:	An error halt occurs upon detection of an error if SENSE switch 1 is selected. An error halt occurs at symbolic location IQ99 if the teletype does not respond favorably to the sense-teletype-not-busy or the sense-buffer-ready instructions within a reasonable length of time when trying to print an error message.
	Input and output devices:	The model 33/35 teletype is used to print error messages.
	Input and output formats:	See alarms or printouts.
	SENSE switch settings:	SENSE switch 1, if selected, causes an error halt instead of an error print upon error detection. If SENSE switch 2 is selected at the completion of a test, and if the user is operating in the corrective mode, the same test is repeated.
	Timing:	Not applicable.
	Accuracy:	Not applicable.
	Cautions to users:	Not applicable.
	Equipment configuration:	Minimum configuration. The model 33/35 teletype is required to obtain the error printouts.
	References:	Not applicable.
5.4 METHOD	Basic and SENSE switch instructions test:	The basic instructions tested are the JMP, JMP*, LDA (instruction counter modified), JAZ, ERA (instruction counter modified), IAR and JMPM. These are the instructions which are assumed to work properly in other instruction class tests. Instructions tested with the SENSE switches ON are: XS1, XS2, XS3, JSS1, JSS2, JSS3, JS1M, JS2M and JS3M. Instructions tested with the SENSE switches OFF are: JSS1, JSS2, JSS3, XS2 and XS3.
	Register change instructions test:	Instructions tested are: TZA, TZB, TZX, TAB, TBA, TAX, TBS, TXA, TBX, DAR, CPA, IAR, DBR, CPB, IBR, DXR, CPX and IXR.
	Load/store instructions test:	The LDA, STA, LDB, STB, LDX and STX instructions are tested using all addressing modes (i.e., instruction counter modified, X register modified, B register modified, direct and indirect). The LDAI, STAI, LDBI, STBI, LDXI and STXI instructions are also tested.
	Logical instructions test:	Instructions tested are the ERA, ORA and ANA using the instruction counter modified addressing mode; and the ERAI, ORAI and ANAI.

Overflow instructions test:	Instructions tested are the SOF, ROF, AOFA, AOFB, AOFX, SOFA, SOFB and SOFX.
Jump-and-execute instructions test:	The JOF, JAP, JAN, JAZ, JBZ and JXZ instructions are tested using direct jump addresses with jump conditions both true and false.
	The JMP, JOF, JAP, JAN, JAZ, JBZ and JXZ instructions are tested using indirect jump addresses with jump conditions true.
	The JOFM, JAPM, JANM, JAZM, JBZM and JXZM instructions are tested using direct jump addresses with jump conditions true.
	The XEC, XOF, XAP, XAN, XAZ, XBZ and XXZ instructions are tested using direct operand addresses with execute conditions both true and (with the exception of XEC) false.
	The JMPM and XEC instructions are tested using indirect operand addresses.
Logical and arithmetic shift instructions test:	The logical shift instructions LRLA, LSRA, LLSR, LSRB and LLRL are tested. The arithmetic shift instructions ASRA, ASRB, LASR, ASLA, ASLB and LASL are tested.
Standard arithmetic instructions test:	The instructions ADD, ADDI, SUB and SUBI are tested with positive and negative operands and with operands which do and do not cause overflow.
	Also tested are the INR and INRI. INR is tested with and without operands causing overflow.
Optional arithmetic instructions test:	The instructions MUL, DIV, MULI and DIVI are tested. A table of values (in the memory) is used in this test sequence as parameters and check values specifying the initial contents of the A and B registers, a multiplier, a divisor, the final contents of the A and B registers and the final status of the overflow indicator.
Extended addressing instructions test:	The instructions LDAE (X register modified), LDAE (B register modified), LDAE (direct) and ERAE (indirect) are tested.

6.1 IDENTIFICATION

Title: Model 33/35B test routine diagnostic package.

Identification: TTY-B

Category: G3.

6.2 PURPOSE

This test routine exercises critical points of operation of the teletype to insure proper performance.

6.3 USAGE

Operational procedures:

Place ON LINE/OFF/OFF LINE switch in ON LINE position. In addition, on model 35 ASR, place mode switch to KT mode.

Keyboard accuracy test will print all lower case printable characters and wait for operator to type all lower case printable characters. Teletype will then print all printable upper case characters and wait for operator to type all printable upper case characters.

Reader control test requires a test loop consisting of a continuous pattern of: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, CR, LF. . . be placed into the reader and reader turned on.

Punch control test will halt with instruction register at 700 after punching tape to permit removal of tape.

Insert tape into reader and press RUN button on console to examine for errors.

Reader/punch accuracy test will pause after punching a leader to permit operator to insert the tape and turn on reader.

Refer to MAINTAIN teletype driver routine for preventative mode of operation.

a. Entries for corrective mode of operation. Run at symbolic locations listed below, this is the recommended sequence.

PPAC	Page printer accuracy test	2000 = P
KBAC	Keyboard accuracy	2005 = P
	Echo test	

b. Model ASR only:

PTS?	Print suppress	35 rum 2012=P 33 N/A
RDCT	Reader control	2012=P coast 2 or 3 char
PCTL	Punch control	2024=P
RPCA	Reader/punch accuracy	

Arguments or parameters: Not applicable.

Space required: ASR, approximately 876 words.

KSR, approximately 245 words.

Temporary space requirements: Not applicable.

Alarms or printouts: All numbers are printed in octal.

a. Reader control. The following totals are printed at completion.

1. Number of stops within 2 characters.
2. Number of stops within 3 characters.
3. Number of errors.

Anything less than 2 or more than 3 characters is an error.

b. Punch control: Total number of errors are printed at completion.

c. Reader/punch accuracy. Total number of errors are printed on a channel basis at completion; channel 1 first, channel 8 last.

Error returns or codes: See error stops for description of error codes.

Error stops:

a. Reader control. Will stop upon detection of an error to permit inspection. Instruction register = 777, A register = 1. If there was no error, clear the A register and press RUN button on console.

Input and output devices: Model 33/35B teletype.

Input and output formats: All inputs and outputs in the form of 8 channel codes or a printout of the characters which these codes represent.

SENSE switch settings: SENSE switch 2, if selected and if the user is running in the corrective mode, causes the same test to be repeated.

Timing:

Test	Approximate Time
Page printer accuracy test	7 minutes
Keyboard accuracy	Not applicable
Print suppress	12 minutes
Reader control	13 minutes
Punch control	10 minutes
Reader/punch accuracy	10 minutes

Accuracy: Not applicable.

Cautions to user: Not applicable.

Equipment configuration: Minimum configuration with model 33/35B teletype.

References: Not applicable.

6.4 METHOD

a. Page printer accuracy test, ASR and KSR. Tests the page printing function of the teletype by outputing the printable characters of the ASCII code set in a defined pattern. Error detection is by visual examination.

b. Keyboard accuracy, ASR and KSR. Tests for proper operation of the keyboard. Error detection is by visual examination.

c. Print suppress ASR. Tests for proper operation of the print suppression function by printing a message with extraneous characters suppressed. Error detection is by visual examination.

d. Reader control, ASR. Tests for proper operation of reader XON/XOFF control functions by reading a fixed pattern tape loop and recording the number of characters which can be read following the issue of an XOFF code. Errors are recorded by test program.

e. Punch/control, ASR. Tests for proper operation of TAPE control function by outputing alternate TAPE and TAPE codes and then reading the generated tape through the reader to check for errors. Errors are recorded by test program.

f. Reader/punch/accuracy, ASR. Tests the reader and punch for accuracy in producing and reading an all-channel pattern. The pattern is punched and subsequently read by the reader and checked for correctness. Errors are counted per channel and totals are printed at completion of test.

7.1 IDENTIFICATION

The following paragraphs describe the operational procedure followed in the disc test routine.

Title: Disc test routine, diagnostic package.

Identification: DISC.

Category: G12.

7.2 PURPOSE

This routine contains a disc pattern test and a full disc test with separate entries provided for each test. The disc pattern test operates with a user-specified pattern or a program-generated random pattern. It will use supplied disc memory addresses so as not to destroy valuable data. The full disc test checks all available disc memory. The write and read operations may be under program control or control of the optional buffer interlace controller.

7.3 USAGE

Operational procedures:

a. Preventive mode of operation.

1. Disc pattern test:

Refer to diagnostic driver section for its operation.

Type mnemonic call name DPAT.

Type space and initial disc address.

Type space and final disc address.

Type space, pattern code and section number.

Type a period to start test.

If pattern code is a one, program will print message PATTERN IS and will wait to accept a six-digit octal pattern terminated by a period. Any time before a period is typed, error recovery is initiated by typing a slash.

2. Full disc test:

Refer to diagnostic driver section for its operation.

Type mnemonic call name DISC.

Type space and appropriate disc size (32, 65, 131, 262).

Type a period to start test.

b. Corrective mode of operation.

1. Disc pattern test:

Place parameter 1 in the A register.

Place parameter 2 in the B register.

Place parameter 3 in the X register.

Select SENSE switches as desired.

Run at symbolic location DPAT.

If parameter 3 has sign bit set, program will halt with A, B, and X registers set to zero.

Enter desired pattern into A register and press RUN button on console.

2. Full disc test:

Place parameter in the A register.

Select SENSE switches as desired.

Run at symbolic location DISC.

Arguments or parameters:

a. Disc pattern test:

1. Parameter 1 is the starting address on the disc*.

2. Parameter 2 is the ending address on the disc*.

Both of the above are full 16-bit addresses to form directly addressable 65K word areas.

3. Parameter 3 contains the pattern code and disc sector number.

Pattern code:

If sign bit of X register is set, the test will accept a pattern.

If sign bit of X register is zero, test will generate a random pattern.

Disc sector - If low order two bits are set to:

0 = 0 - 65K.
1 = 65 - 131K.
2 = 131 - 196K.
3 = 196- 262K.
Numbers larger than 3 are truncated to two bits.

*Starting address may be greater than final address. See section 7.4, disc memory map.

b. Full disc test.

1. Parameter to be placed in A register is the storage capacity in the range of 32, 65, 131, 262. Numbers outside this range are reset to 32.

Space Required:	Approximately 1360_8 words are required for storing this routine.
Temporary Space Requirements:	Locations: 0 - 1777_8 are reserved for pattern buffer. 4000 - 5777_8 are reserved for read buffer.
Alarms or Printouts:	A printout normally occurs when a data content, parity, or abnormal device stop is detected. The user may bypass this printout, accumulate errors, and cause a halt if SENSE switch 1 is selected; or may bypass the printout, accumulate the number of errors and continue the run if SENSE switch 2 is selected.
Parity error:	The error printout consists of the words PARITY ERROR INITIAL DISC ADDRESS = followed by the sector code and initial address of the current block tested.
Data content error:	The error printout consists of the disc sector code and address, the good pattern and the bad pattern.
Abnormal device stop:	The error printout consists of ABNORMAL STOP WHILE WRITING (or READING) INITIAL REGISTER = followed by the initial address from the buffer interlace controller.
Error totals:	At the end of the disc pattern test (DPAT) when error printout has been suppressed, the words TOTAL DATA CONTENT ERRORS TOTAL PARITY ERRORS are printed followed by the number of errors. If no errors are detected, this printout is suppressed. All error printouts are in octal.
Error Returns or Error Codes:	See alarms and printouts, and error stops for a description of error codes.
Error Stops:	An error halt occurs when a data error is detected if SENSE switch 1 is selected. The A register contains the good pattern; the B register contains the bad pattern. To continue, following the error halt, press the RUN button on the DATA 620/i console, and the program continues with the next pattern to be compared. If an abnormal device stop is detected when operating under control of a buffer interlace controller, the initial address register is printed and the program halts. This error is non-recoverable.
Input and Output Devices:	The model 33/35 teletype is used to input a specified pattern and to print error messages. The magnetic disc memory is the device to be tested.
Input and Output Formats:	16- or 18-bit binary words to and from disc memory.

SENSE Switch Settings: SENSE switch 1, upon detection of a data content error, suppresses printout, accumulates errors, displays good and bad patterns and halts. SENSE switch 2, if selected at the completion of the test, and if the user is operating in the corrective mode, repeats the same test using the same parameters. Error printout is suppressed and error count accumulated.

SENSE switch 3, if selected, permits reading and writing under BIC control.

Timing (approximate): Full test of 32K disc memory: 2 seconds.

Full test of 262K disc memory: 15.5 seconds.

Accuracy: Not applicable.

Cautions to Operators: None.

Equipment Configuration: Minimum configuration with model 33/35 teletype magnetic disc, memory and buffer interlace controller, if available.

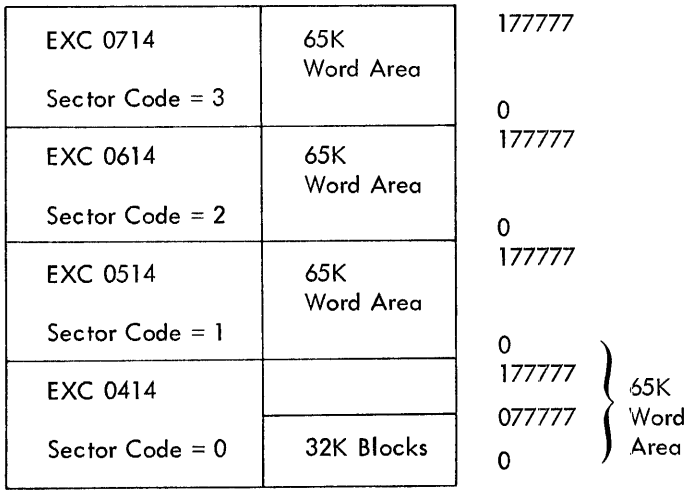
References: Not applicable.

7.4 METHOD

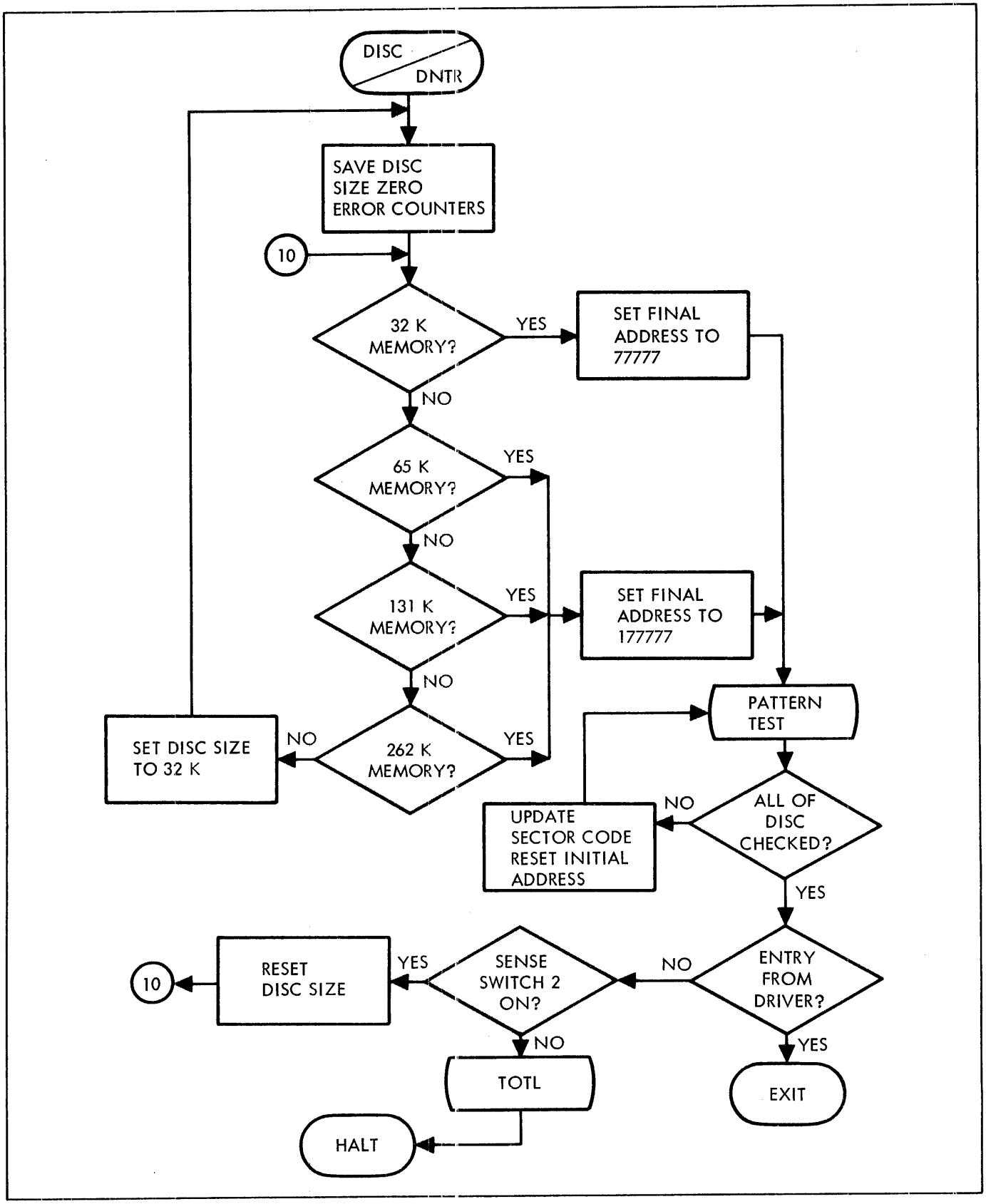
The area specified is tested in 2000_8 word blocks. A maximum area of 65000 (0177777_8) may be tested at one time. The type of pattern to be written is designated by the status of the X-register sign bit, and a negative condition permits the user to control the pattern to be written. The pattern buffer is generated and written on the disc. The same area on the disc is read back and stored in the read buffer. Parity is checked after each read. If parity error is detected, a message is typed and the next 2000_8 word block is written. Each word is compared and checked for data content. If an error is detected, a message is typed and checking is continued.

Full Disc Test: The test described above is performed in 2000_8 word blocks for the full disc size which may be 32K, 65K, 131K or 262K. Any number outside this range will be set to the 32K size.

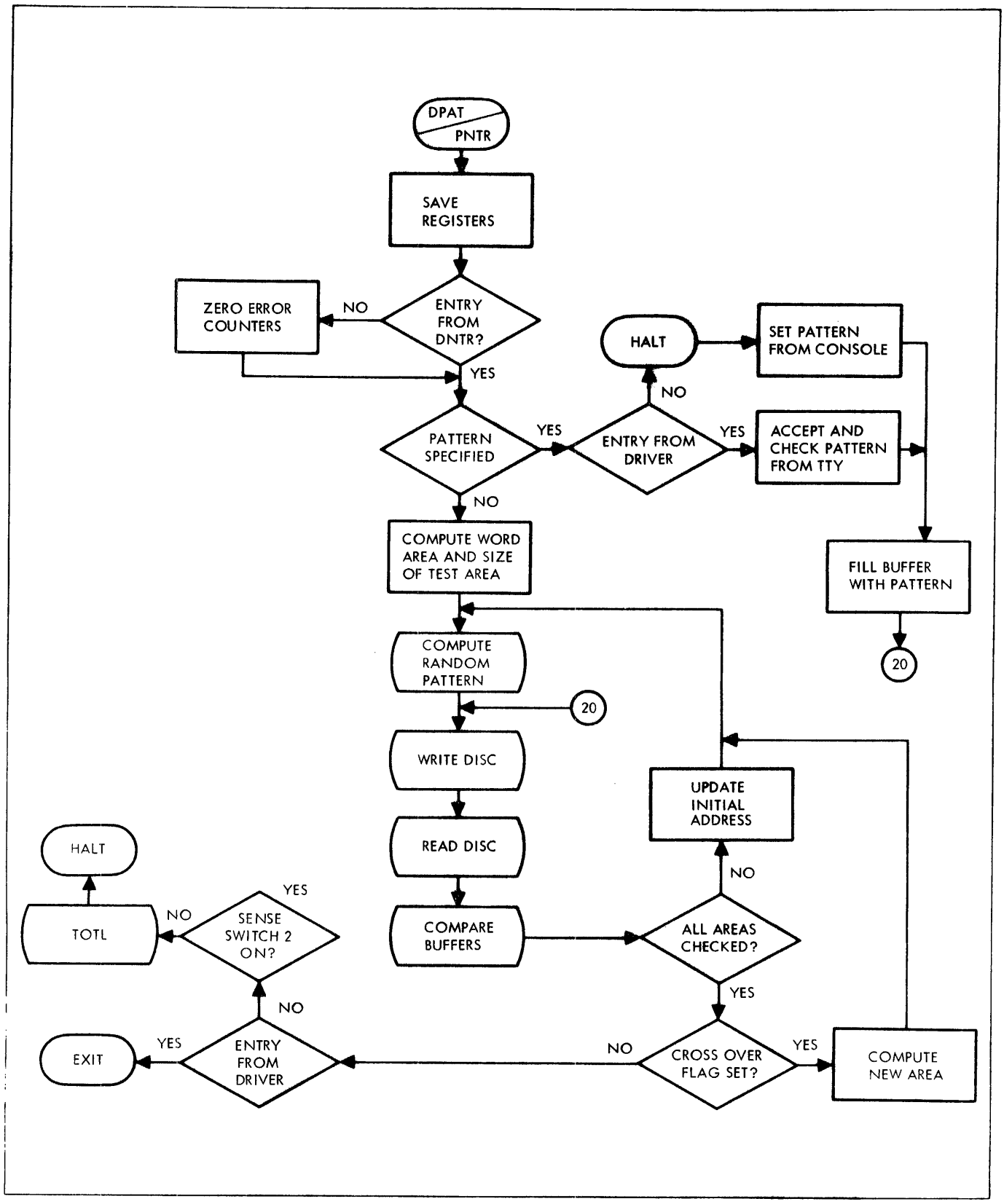
Disc Memory Map:



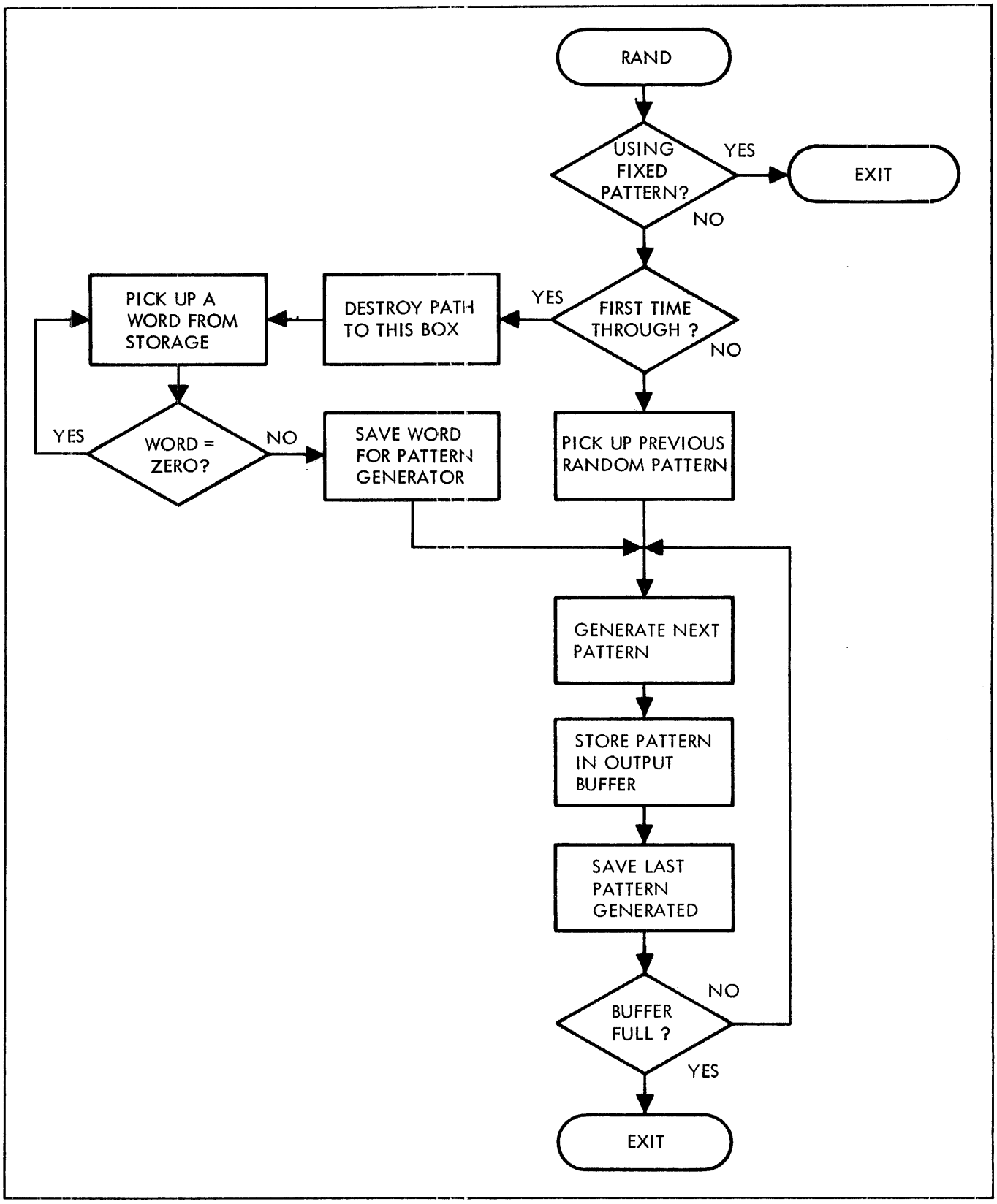
A write may be initiated in one disc word area and cross over to the next area, in which case the initial address is greater than the final address and the sector code is program updated.



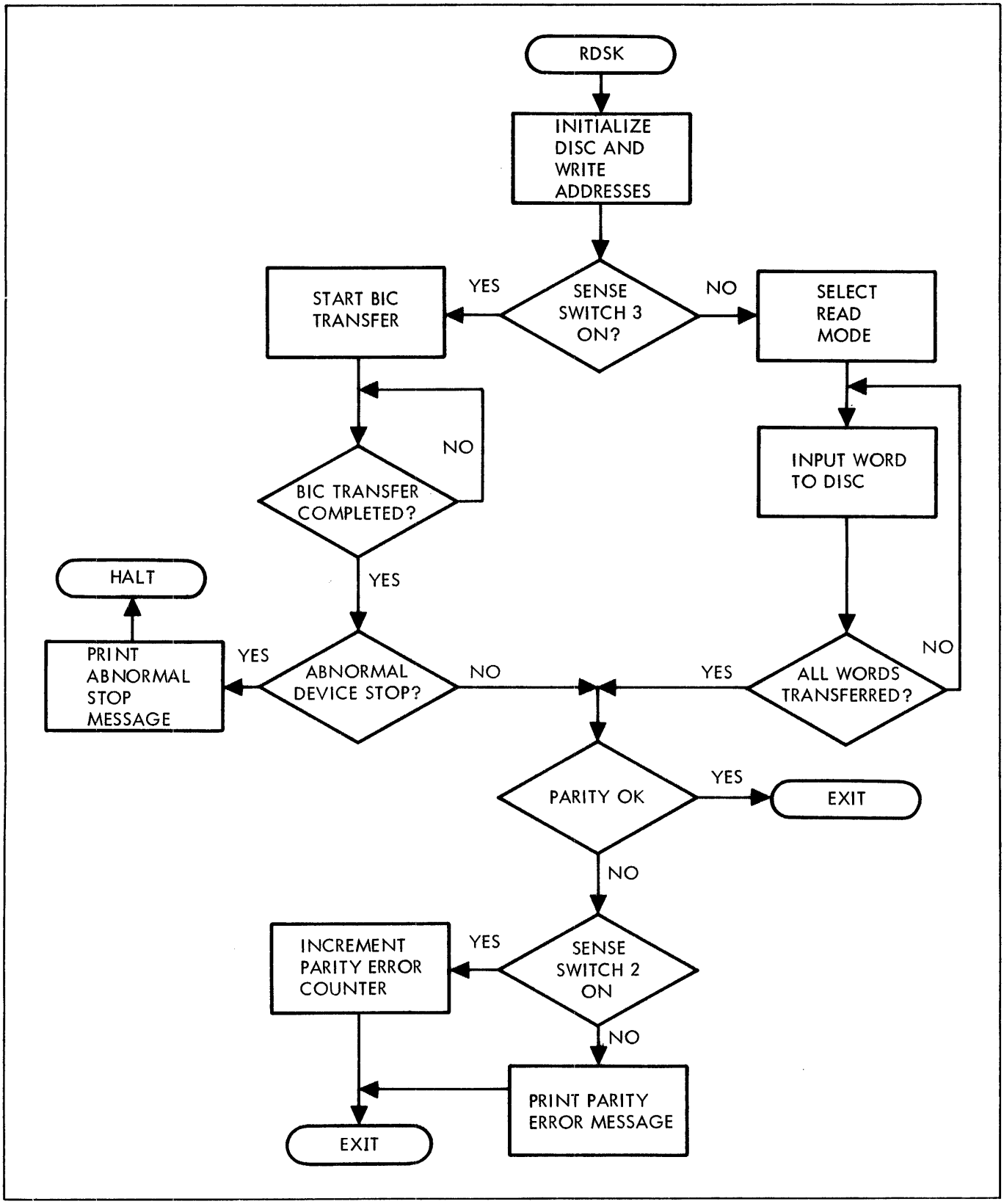
Full Disc Test



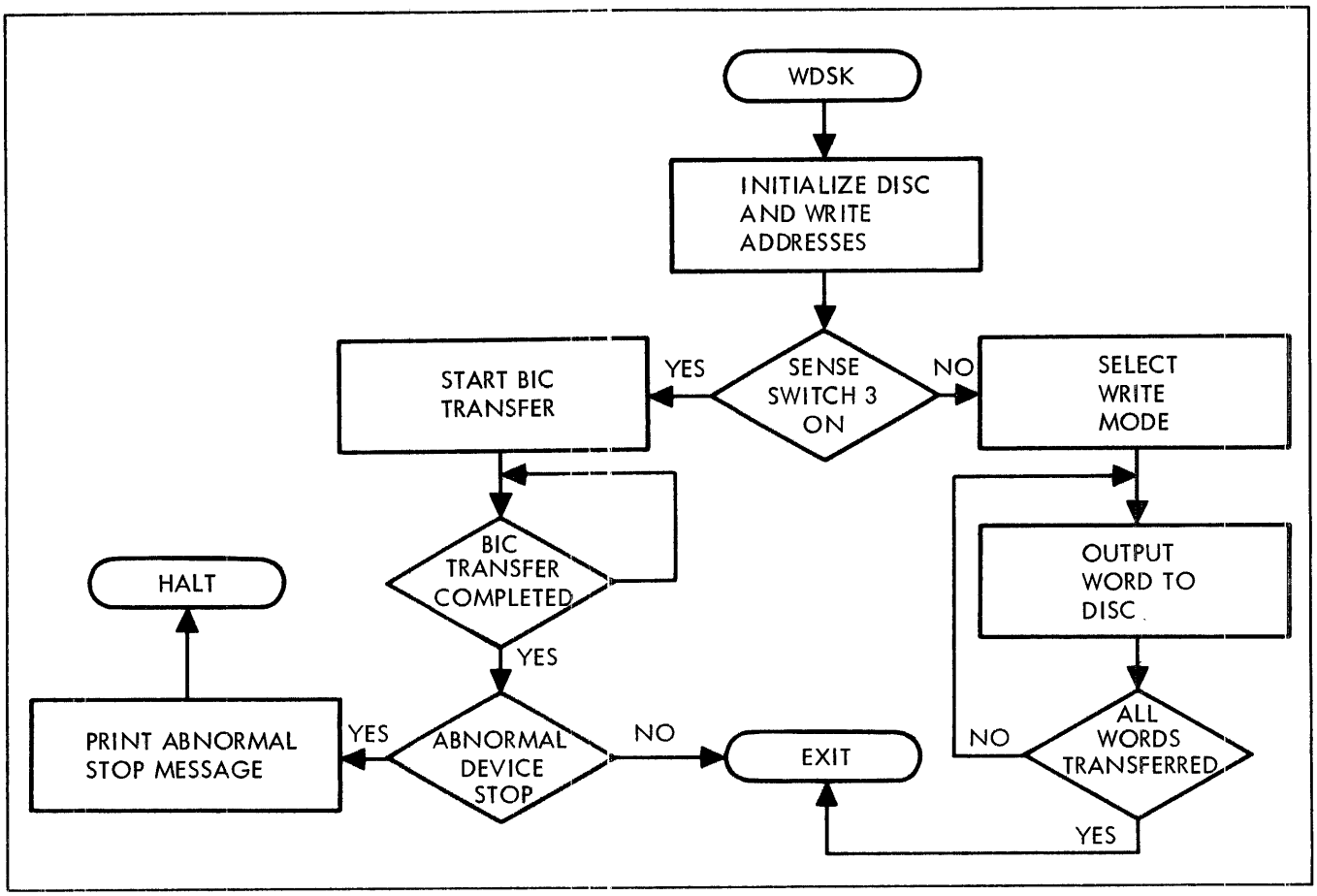
Disc Pattern Test

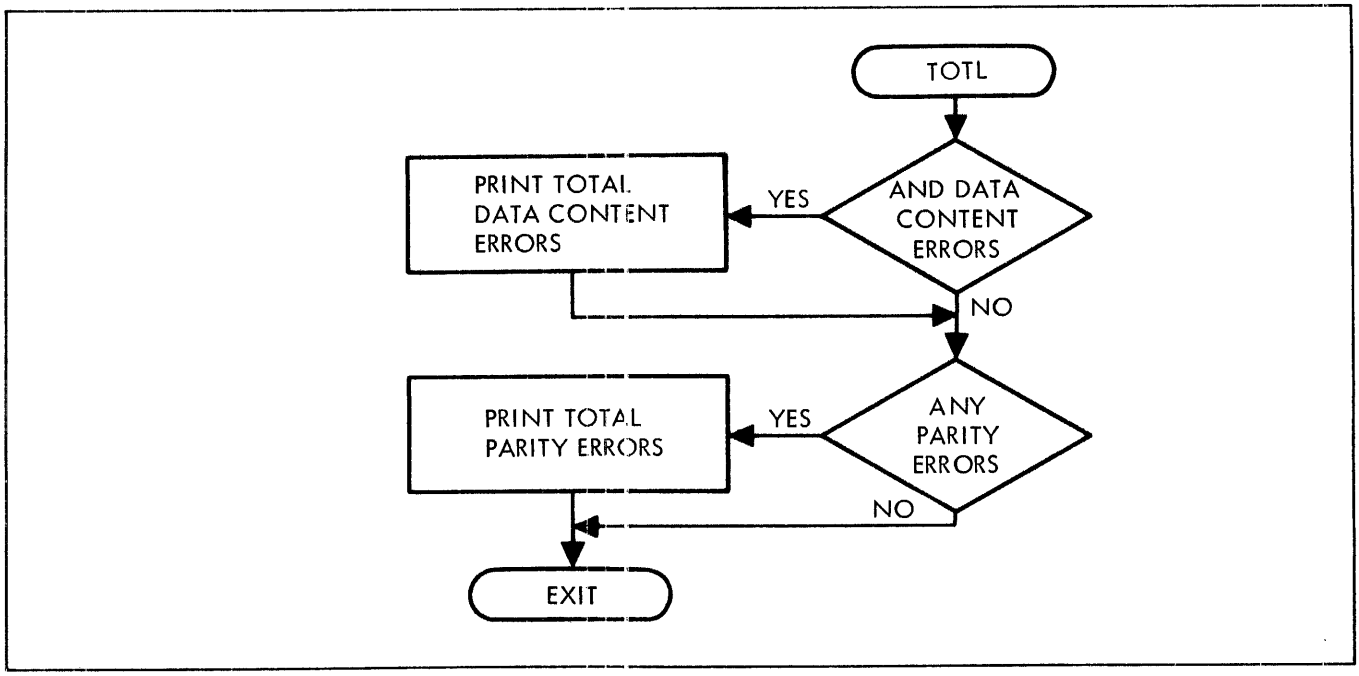


Random Pattern Generator

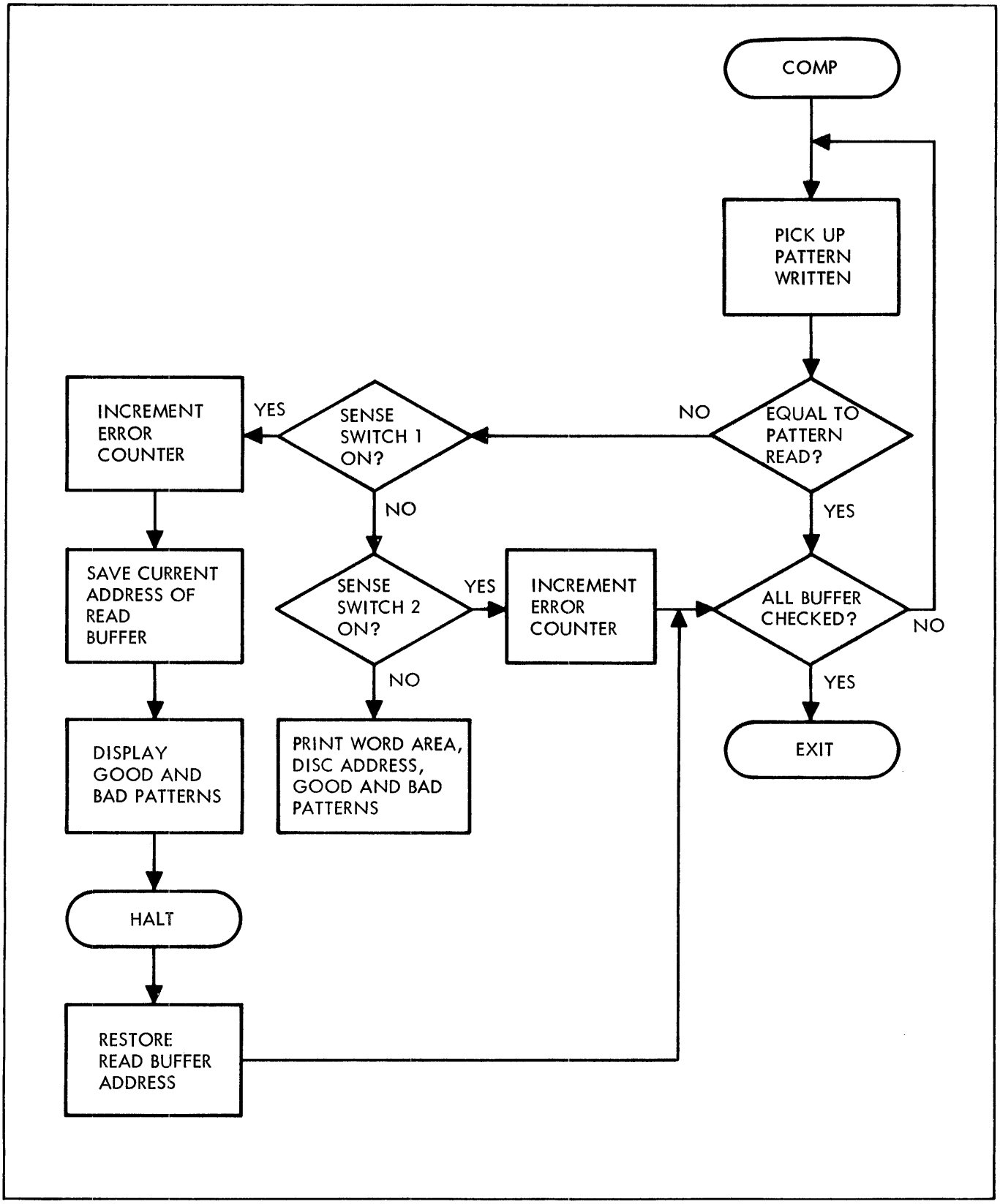


Disc Read Routine





Output Error Totals



Compare Buffers

8.1 IDENTIFICATION

The following paragraphs describe the procedures used in the paper tape system test routine.

Title: Paper tape system test routine, diagnostic package.

Identification: PTAPE.

Category: G3.

8.2 PURPOSE

The paper tape system test routine contains a punch paper tape test and a read paper tape test (high speed or step mode). These routines punch or read a block of codes starting with the specified minimum code (parameter 1) and continuing until the specified number of codes (parameter 3) have been punched or read. After using the specified maximum code (parameter 2) and before reaching the end of the block, the test reverts back to the minimum code and repeats the pattern.

All input/output transfer instructions are used. The input transfer instructions are executed in CIA, CIB, INA, INB and IME order for each successive group of five codes read in a block. The output transfer instructions are executed in OME, OAR and OBR order for each successive group of three codes punched in a block.

An error count is maintained for read errors since the expected code is always known. The punched tape may be checked visually for errors or may be read back and checked by the read paper tape test.

8.3 USAGE

Operational procedures: The procedures used in the preventive mode of operation are described in section 3, diagnostic teletype driver routine for the preventive mode of operation, diagnostic package. The following procedures are for the corrective mode of operation:

a. Prepare the paper tape punch or the paper tape reader. If using the read paper tape test, position a paper tape with the appropriate codes in the reader so that the first code read will be the initial code of the block. All codes are in binary. A blank frame is a zero code.

b. Provide the following parameters in the indicated registers:

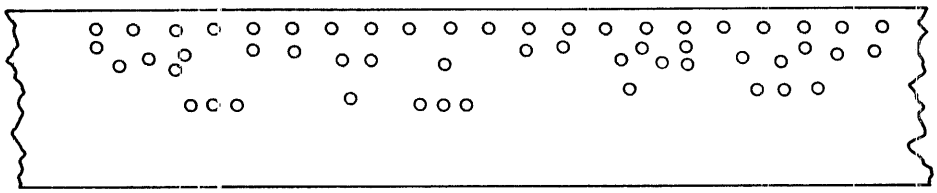
$(\text{A register})_{7-0}$	Lower limit of the code range
$(\text{B register})_{7-0}$	Upper limit of the code range
(X register)	Number of codes in the block

c. Run at one of the following symbol locations:

PRH	Read paper tape test (high speed)
PRS	Read paper tape test (step/read)
PP	Punch paper tape test

As an example of what the parameters will produce, the tape below could be produced by setting the registers as follows:

A-REG = 1, B-REG = 12, X-REG = 41.



Parameters: Parameter 1 is the minimum code in the block of data to be punched or read. This code must be in the range 0 through 377 octal.

Parameter 2 is the maximum code in the block of data to be punched or read. This code must be in the range 0 through 377 octal.

Parameter 3 is the number of codes in the block of data to be punched or read.

Space required: Approximately 231 words.

Temporary space requirements: Not applicable.

Alarms or printouts: At the completion of each read test, the total number of errors found are printed. If this number is not zero, eight more totals will be printed. These represent the total errors per channel, and are listed channel 1 through channel 8.

Error codes: See error stops.

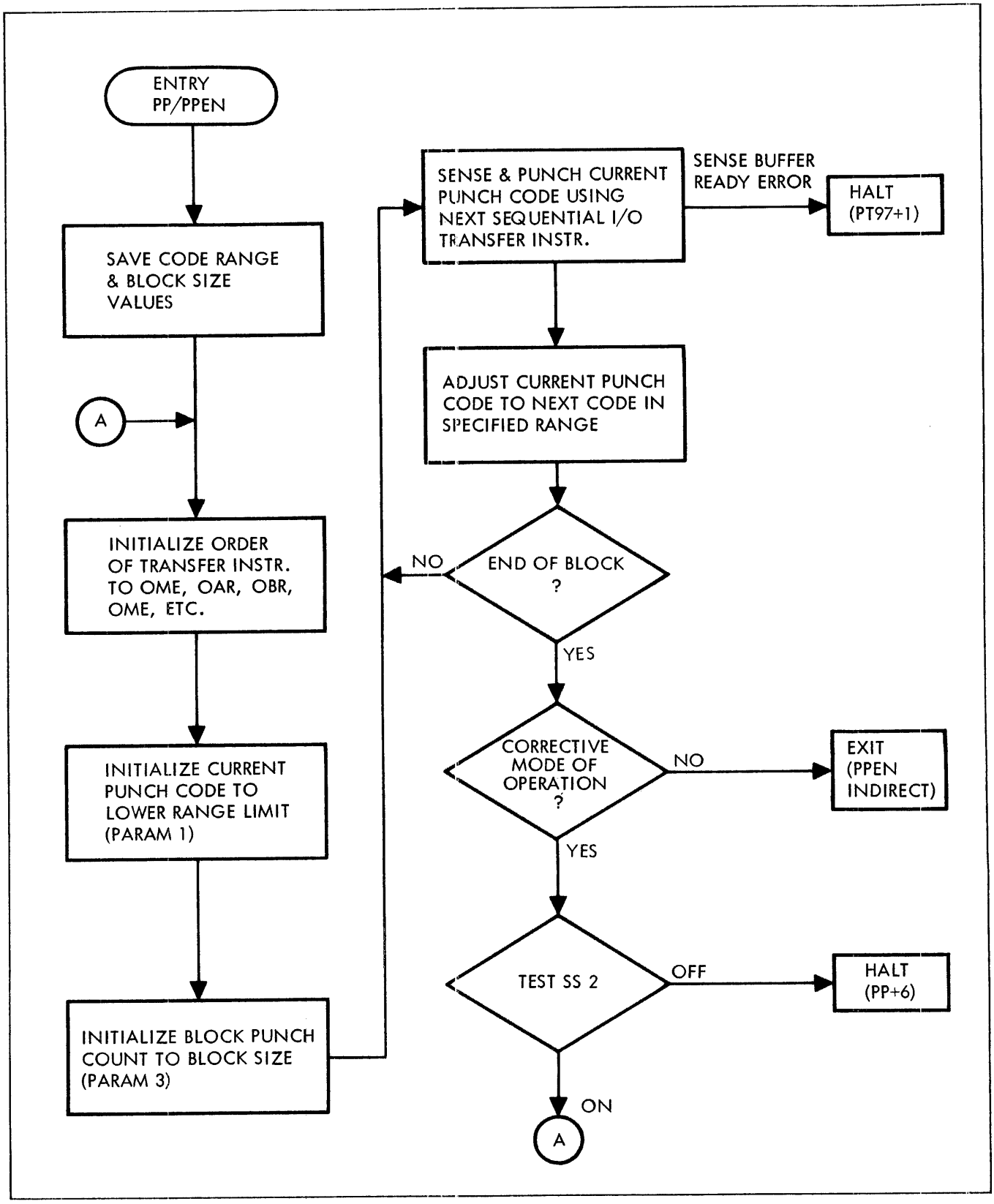
Error stops: An error halt occurs upon detection of a read error if SENSE switch 1 is selected. The registers are set at the halt as follows:

(A register)	Error bits in the code just read
(B register)	Expected read code
(instruction counter)	The octal equivalent of symbolic location PR18+1
(X register)	Total number of codes read in error

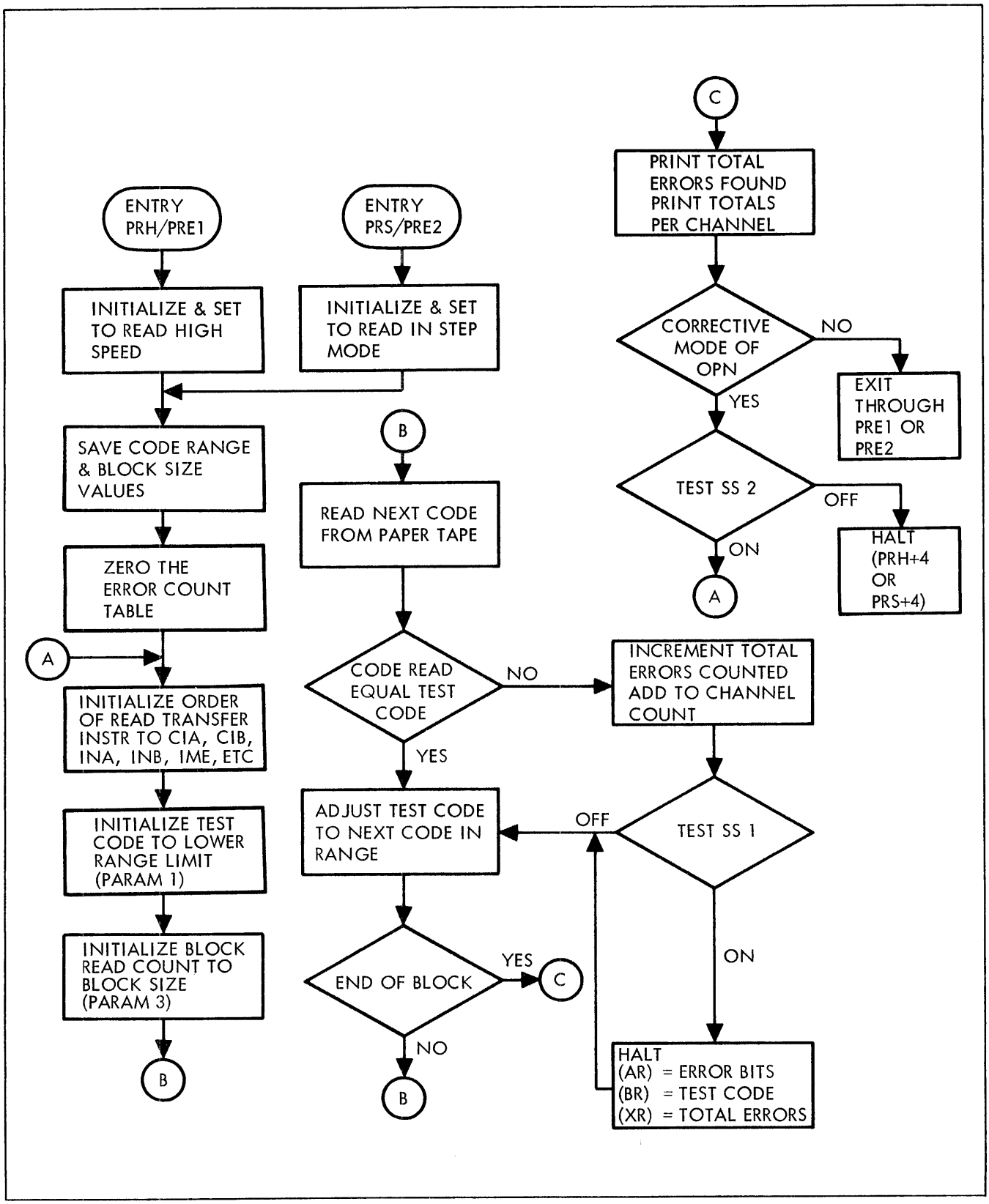
	An error halt occurs if the reader or punch does not respond favorably to the sense buffer ready instruction within a reasonable length of time. The instruction counter will contain the octal equivalent of symbolic location PT97+1.
Input and output devices:	There are two input/output devices, the high speed paper tape punch and the optical paper tape reader.
Input and output formats:	All inputs and outputs are in the form of eight-bit codes (one paper tape frame of data).
SENSE switch settings:	If SENSE switch 1 is selected at the time a read error is detected, the machine halts.
	If SENSE switch 2 is selected at the completion of a read or punch test and if the user is operating in the corrective mode, the same test is repeated using the same parameters. The error count is not cleared before repeating the test.
Timing:	Not applicable.
Accuracy:	Not applicable.
Cautions to users:	Not applicable.
Equipment configuration:	Minimum configuration with optical paper tape reader and high speed paper tape punch.
References:	Not applicable.

8.4 METHOD

The method used in the paper tape system test routine is illustrated in the flow charts on the following pages.



Punch Paper Tape Test



Read Paper Tape Test

9.1 IDENTIFICATION

The following paragraphs describe the procedures used in the line printer test routine. This covers two types of line printers, buffered and console.

Title: Line printer test routine, diagnostic package.

Identification: PRINT.

Category: G3.

9.2 PURPOSE

The line printer test routine contains a diagonal format test, a line/slew test, a combination diagonal format and line/slew test and a character test.

The diagonal format test prints 64 single-spaced lines with 120 characters per line. Each character is printed once at each of the 120 print positions, and is offset one position to the right from the same character on the previous line.

The line/slew test prints the same character at all 120 print positions on a line. Slew control is tested by printing five pages featuring spacings of two, four, eight, 16, 32 and 64 lines, respectively, between lines printed.

The character test prints a specified character at each of the 120 print positions on one line. Single spacing occurs before the print.

Buffered: All three of the output transfer instructions are used alternately for each line printed in OAR, OBR and OME order. The line printer is sensed for a parity error following each line printed. If a parity error signal is received, the character PARITY is printed on the next line.

Console: This line printer transfers codes from core memory in the trap mode.

9.3 USAGE

Operational procedures: The procedures used in the preventive mode of operation are described in section 3, MAINTAIN teletype driver routine for the preventive mode of operation, diagnostic package. The following procedures are for the corrective mode of operation. Line printer codes are listed in the system reference manual.

a. Prepare the line printer.

   Buffered:

b. If using the character test, set the A register with the seven-bit code (including the parity bit) of the character to be printed.

Console:

c. If using the character test, set the A register with the six-bit code of the character to be printed.

Set the instruction counter to the octal equivalent of one of the following symbolic locations:

LPRD	Diagonal format test
LPRL	Line/slew test
LPRB	Combination of diagonal format test and line/slew test
LPRS	Character test

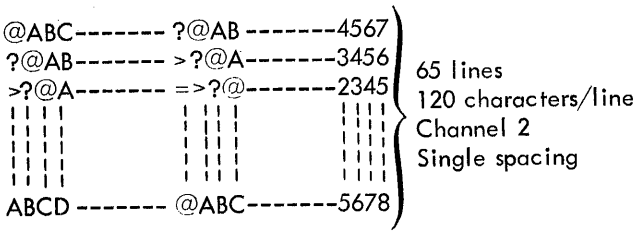
d. Run.

Arguments or parameters:

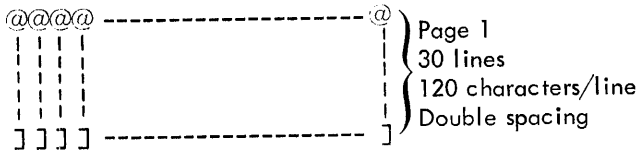
Buffered printer:	The character test requires the seven-bit code (including parity) of the character to be printed, for use as a parameter.
Console printer:	The character test requires the six-bit code of the character to be printed, for use as a parameter.
Space required:	Approximately 277 words.
Temporary space requirements:	Not applicable.
Alarms or printouts:	Buffered printer: if a parity error is sensed, the message PARITY is printed on the next line.
Console printer:	Not applicable.
Error returns of error codes:	Not applicable.
Error stops:	Buffered printer: a halt occurs upon detection of a parity error and following the printout of the message PARITY, if SENSE switch 1 is selected. A halt occurs if the printer does not respond favorably to the sense-printer-ready or the sense-buffer-ready instructions within a reasonable length of time. The instruction counter will contain the octal equivalent of symbolic location LP97+1 (printer not ready) or LP92+1 (buffer not ready).
Console printer:	All error checking is visual.
Input and output devices:	The line printer is used as the output device.

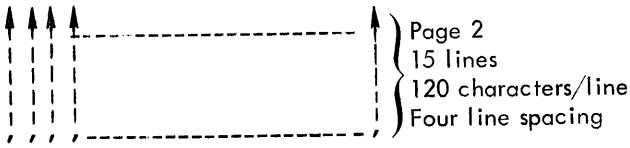
Input and output formats: The four input/output formats are as follows:

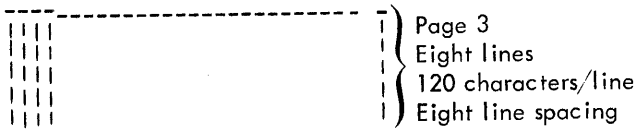
a. Diagonal format test

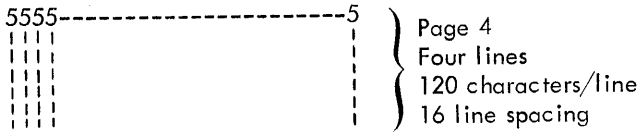


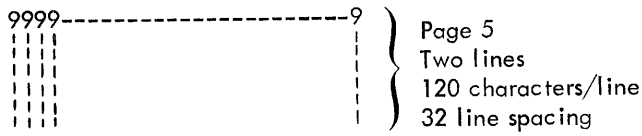
b. Line/slew test

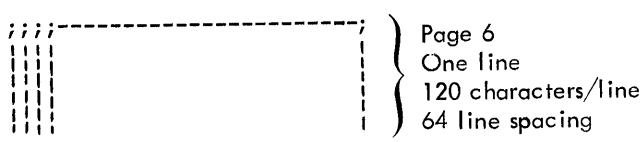








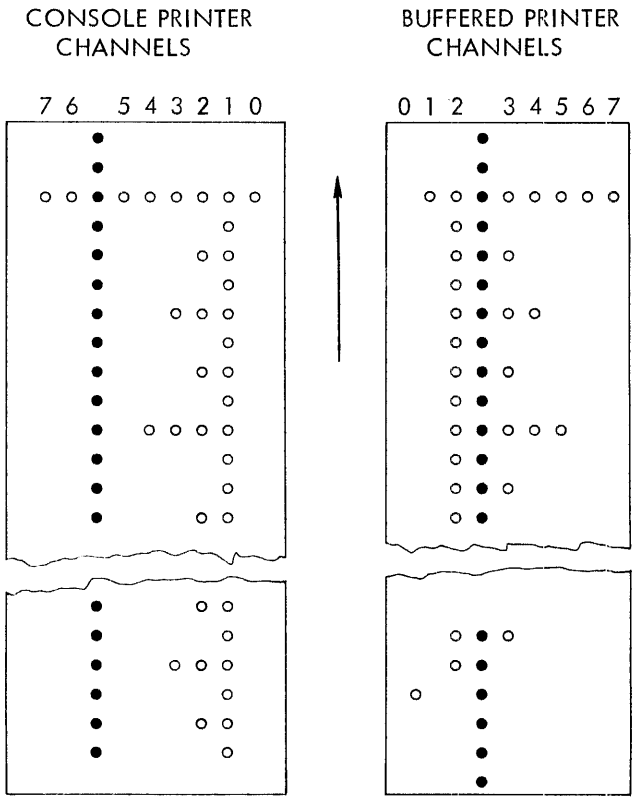




c. Character test: The specified character is printed in all 120 print positions using single spacing.

d. The assumed line printer control paper tape is as follows:

	BUFFERED	CONSOLE
Channel 0	Bottom of page	Top of page
Channel 1	Top of page	Single spacing
Channel 2	Single spacing	Two spaces
Channel 3	Two spaces	Four spaces
Channel 4	Four spaces	Eight spaces
Channel 5	Eight spaces	16 spaces
Channel 6	16 spaces	32 spaces
Channel 7	32 spaces	Bottom of page



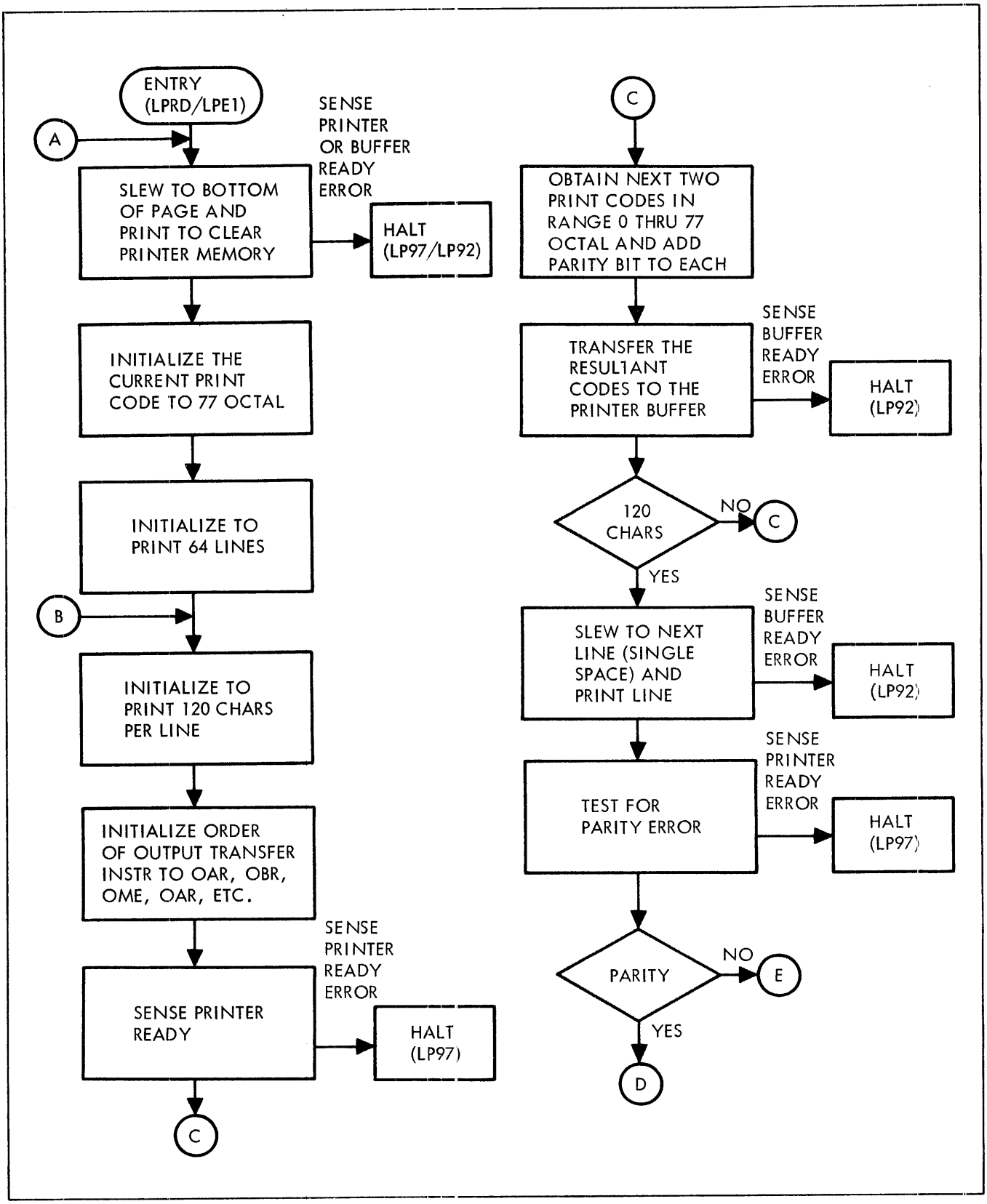
SENSE switch settings:

A halt occurs if SENSE switch 1 is selected after the parity error is detected and the error message is printed. The test continues after the RUN switch has been pressed. The same test is repeated if SENSE switch 2 is selected at the completion of a test and if the operator is using the corrective mode. The same parameter is used as in the character test.

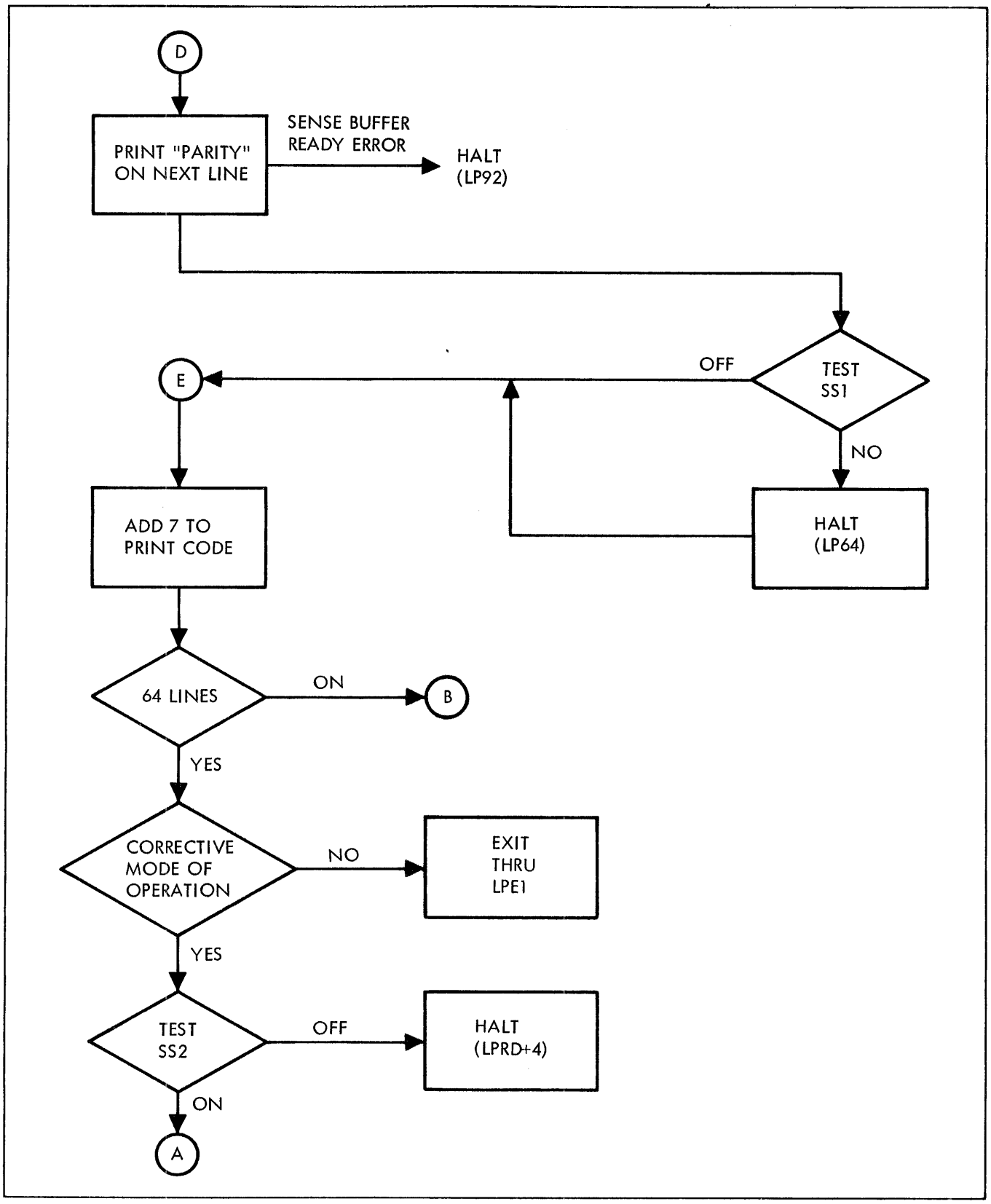
Timing:	Not applicable.
Accuracy:	Not applicable.
Cautions to users:	Not applicable.
Equipment configuration:	Minimum configuration with line printer.
References:	Not applicable.

9.4 METHOD

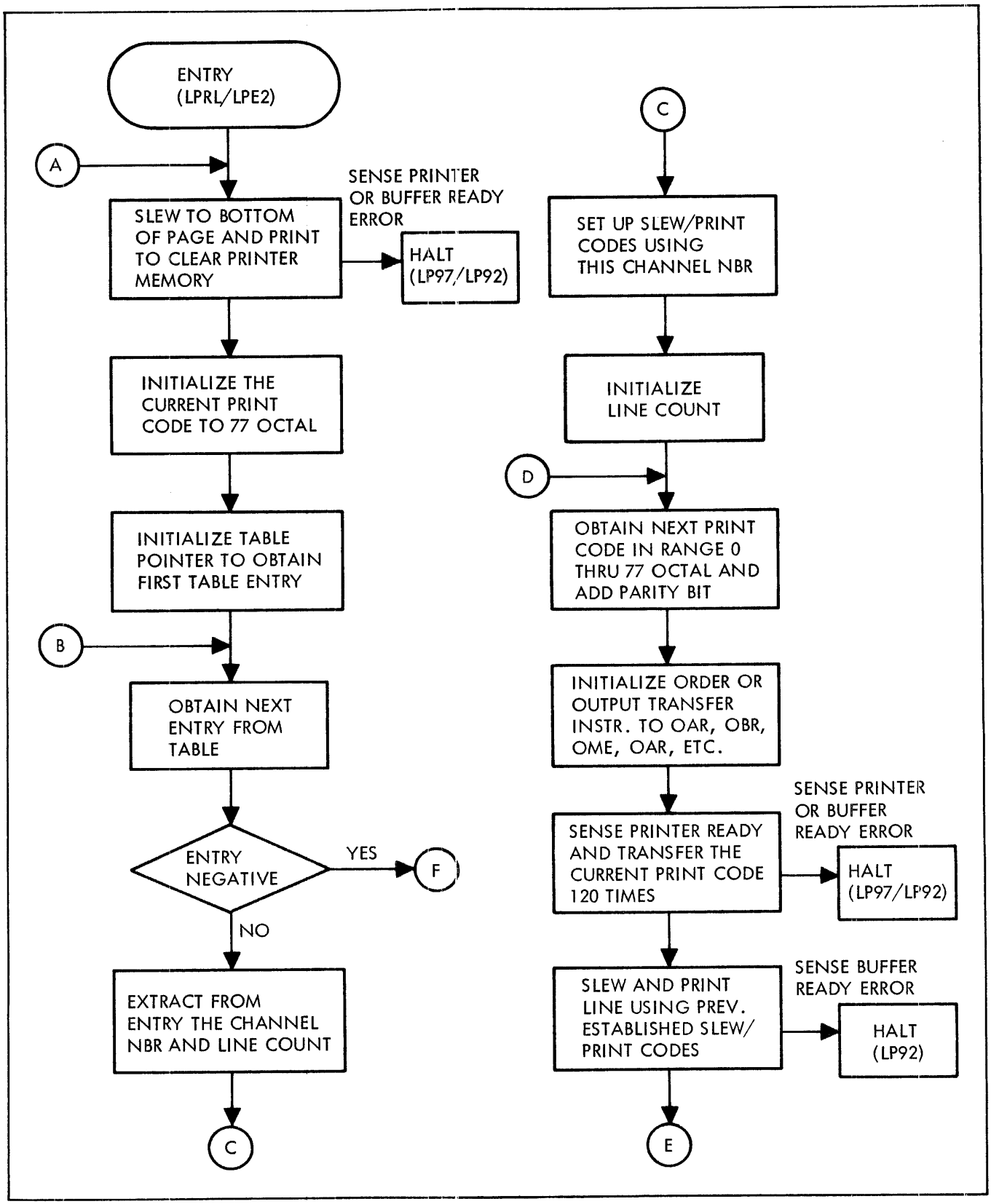
The method used in the buffered line printer test routine is illustrated in the flow charts on the following pages.



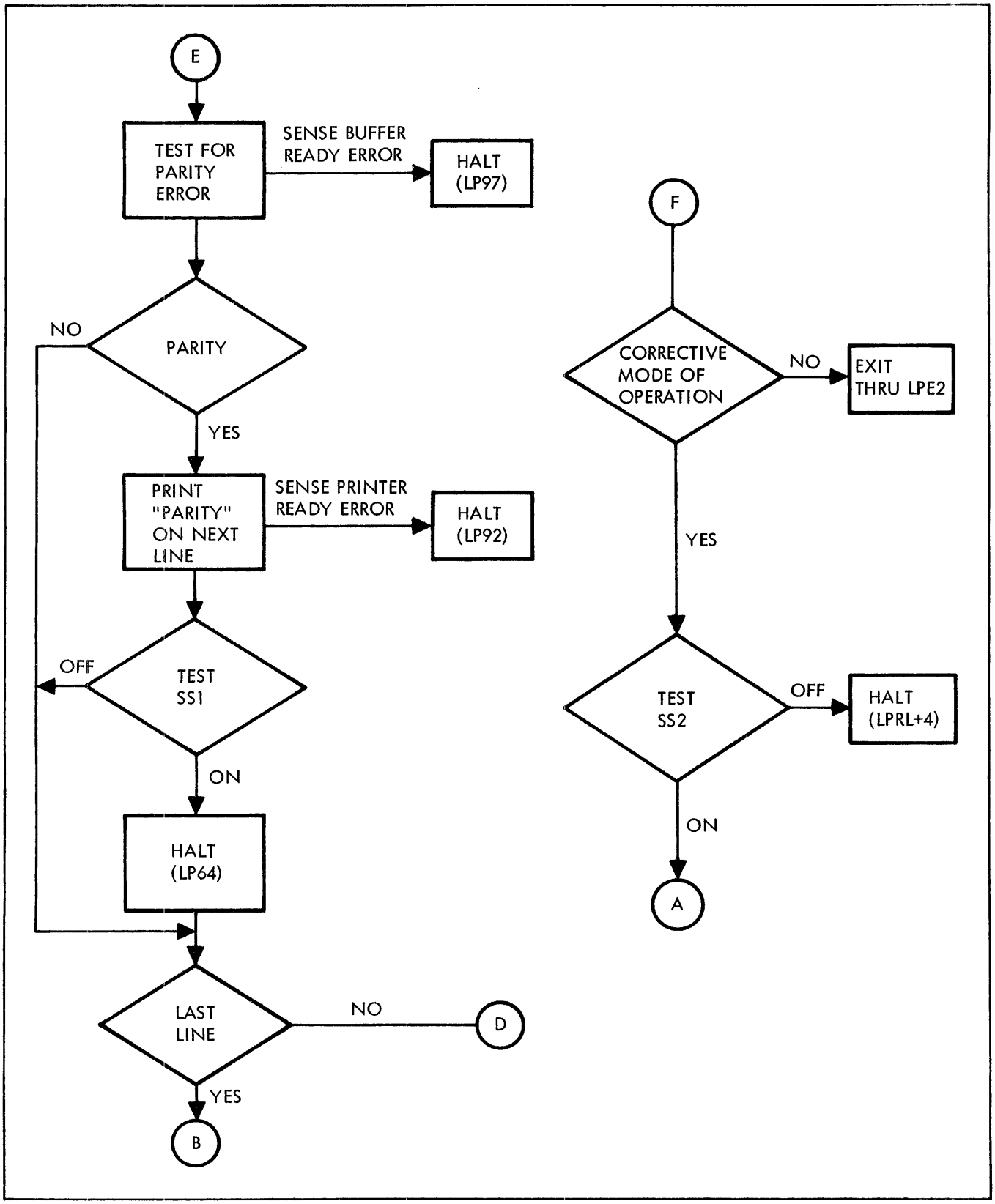
Diagonal Format Test



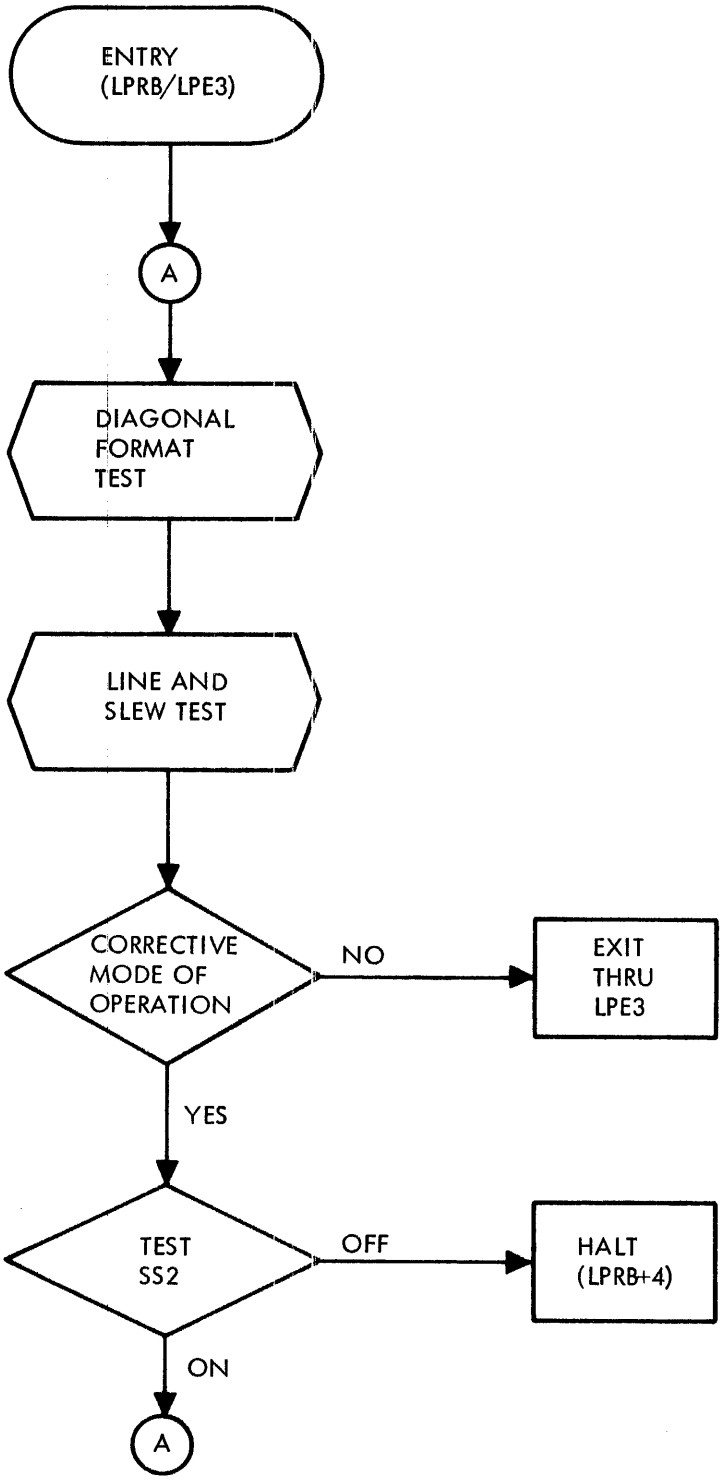
Diagonal Format Test



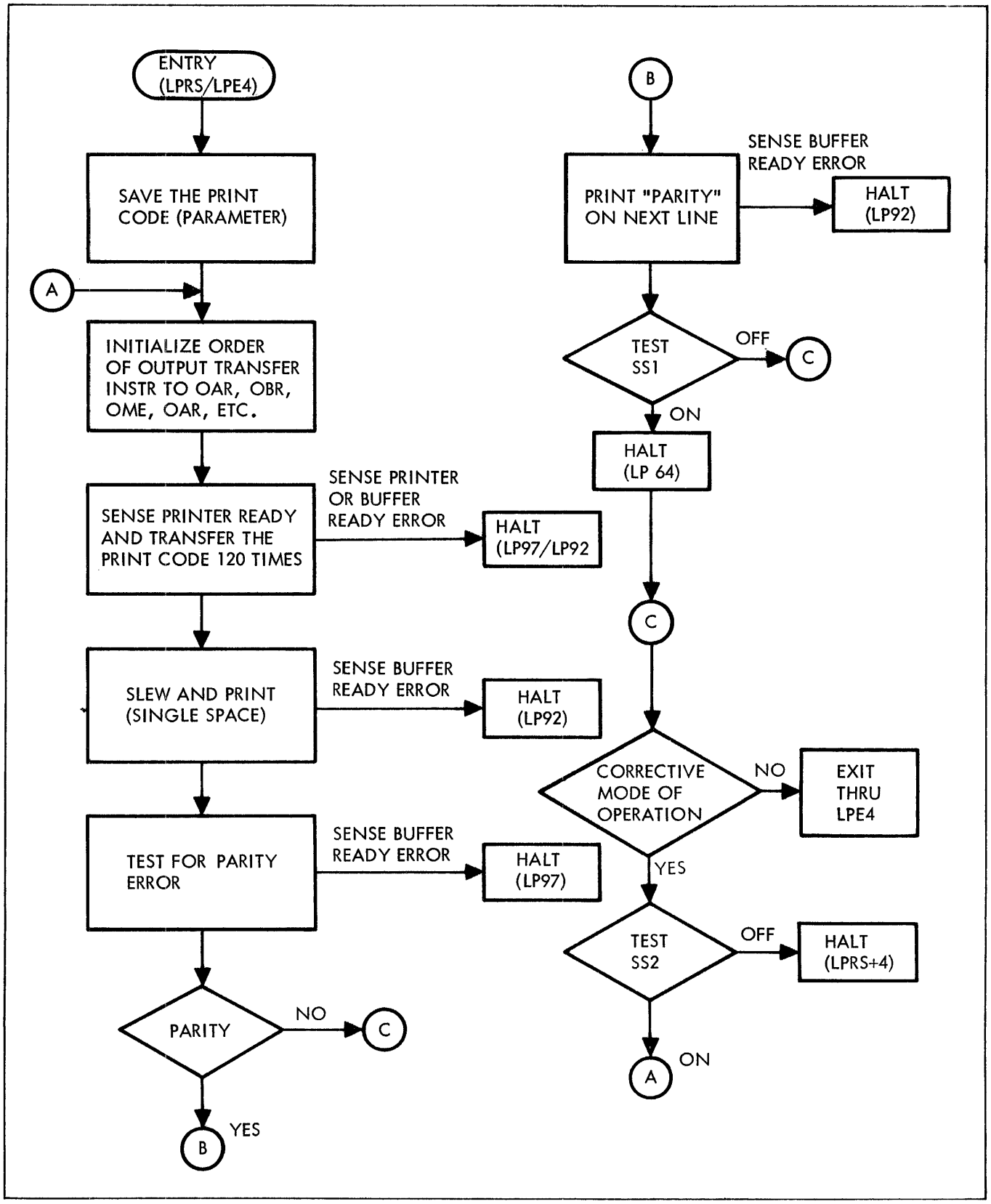
Line And Slew Test



Line And Slew Test



Diagonal And Line/Slew Test



Character Test

10.1 IDENTIFICATION

Title: Card reader test routine.

Identification: CDRD.

Category: GS.

10.2 PURPOSE

The card reader test routine operates the reader at maximum reading speed checking every column for a specific pattern.

10.3 USAGE

Operational procedures: Place the test deck in the read hopper and ready the card reader. SENSE switches may be selected as desired, see SENSE switch settings.

a. Preventive mode of operation: Refer to section 3, maintain teletype driver routine, diagnostic package.

b. Corrective mode of operation: Select SENSE switches 1 and 2, set instruction counter equal to 02000, and press RUN. Error codes are explained in error stops.

Arguments or parameters: Produce a test deck from master card included with program. Recommended size of test deck is about 1000 cards.

Space required: Approximately 212 words.

Temporary storage required: Not applicable.

Alarms or printouts: At the completion of the test, totals are printed indicating number of errors found and number of cards read. All numbers are printed as a six digit octal number.

Error returns or codes: See error stops for a description of error stops.

Error stops: An error halt occurs upon detection of a read error if SENSE switch 1 is selected. At this time the A register contains the punches in error.

A register bit: 11 10 9 8 7 6 5 4 3 2 1 0

Punch: 12 11 0 1 2 3 4 5 6 7 8 9

If cards stop reading and SENSE switch 2 is selected, the overflow indicator should be on. This indicates the reader is waiting to read additional cards. Selecting SENSE switch 2 off at this time will permit totals to be printed. To continue reading cards, fill hopper, empty stacker and ready the card reader.

If overflow was not on, then the reader was mechanically in error.

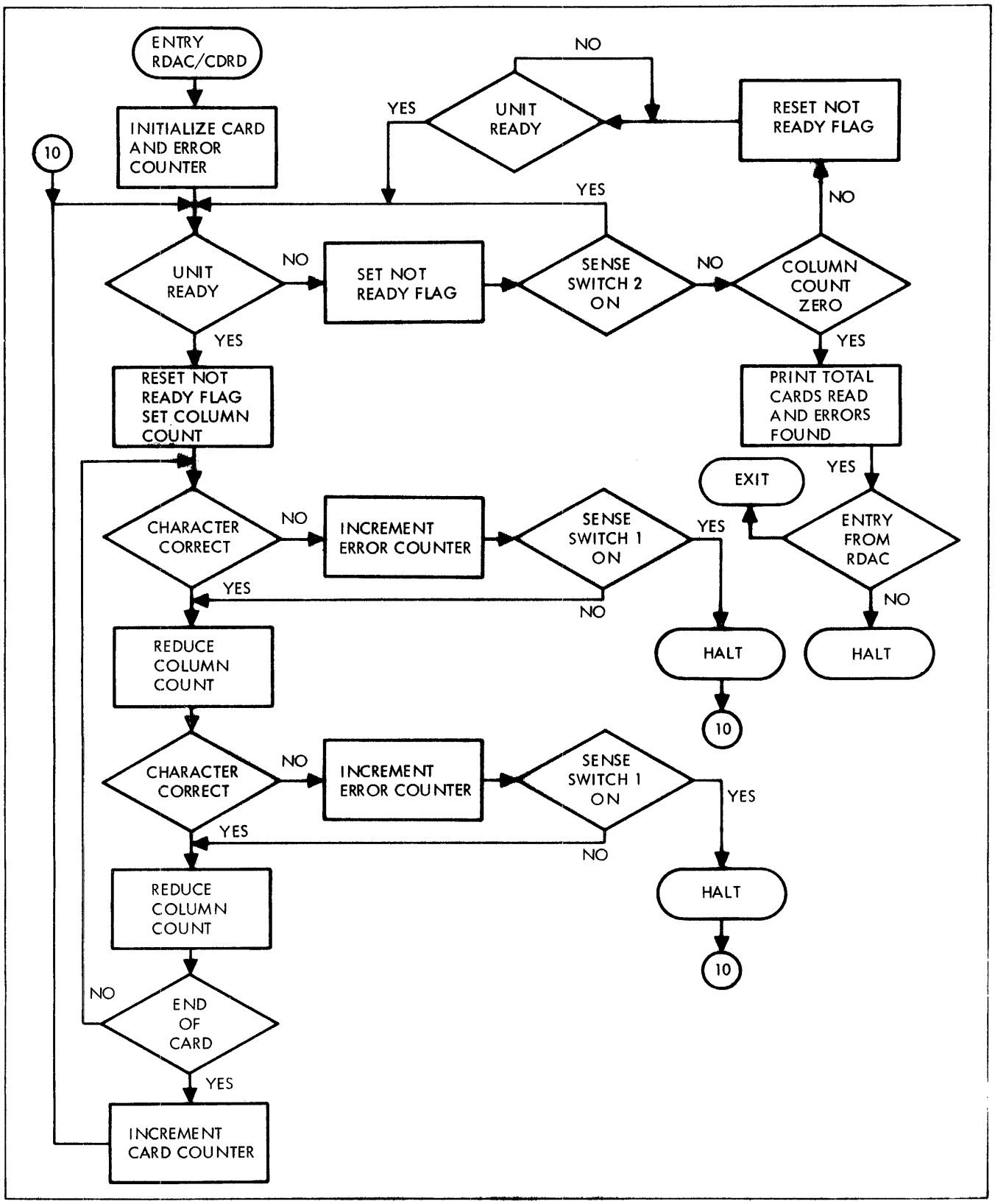
Input and output devices:	Teletype and card reader.
Input and output formats or tables:	Input from card reader is a fixed combination of the 12 possible punches that can be contained in one column. A 9 punch would be brought into memory or registers as a one in bit position zero.
Subroutines required:	None.
SENSE switch settings:	SENSE switch 1 causes a halt upon detection of an error, otherwise errors are accumulated in the B register. SENSE switch 2 suppresses total printing to allow additional cards to be read following a stacker full or hopper empty condition.
Timing:	Not applicable.
Accuracy:	Not applicable.
Cautions to user:	Not applicable.
Equipment configuration:	Minimum configuration with card reader.
References:	Not applicable.

10.4 METHOD

A card is read and all odd numbered columns are compared for 12-0-2-4-6-8 punches and even numbered columns are compared for 11-1-3-5-7-9 punches. If an error is found and SENSE switch 1 is selected, a halt occurs and the A register contains the punches in error. Bit 11 = 12 punch, bit 0 = 9 punch. Errors are accumulated in the B register with the number of the cards read in symbolic location CDCT. After the cards in the hopper are read, the total number of errors found and the total number of cards read are printed. All numbers printed are in octal. If SENSE switch 2 is selected, this printout is suppressed so that additional cards may be read.

NOTE

Occasionally it may be desirable to read blank cards and check for input of extraneous bits. This may be accomplished by storing zeros in symbolic locations MSK1 and MSK2. These are the column bit masks. Their actual locations may be found by referring to the card reader test assembly listing.



Card Reader Test

11.1 IDENTIFICATION

The model 33A teletype test routine procedure is described in the following paragraphs (refer to the end of this section for flow charts).

Title: Model 33A teletype test routine, diagnostic package.

Identification: TTY.

Category: G3.

11.2 PURPOSE

The model 33A teletype test routine allows an operator to test all input/output features associated with the teletype machine. Tests provided are: read paper tape test (high- or low-speed read), read keyboard test, punch/print test, read paper tape/punch/print test (high-speed read), read keyboard punch/print test and teletype transfer instructions test (keyboard or paper tape input).

All tests, except the teletype transfer-instructions test, work as follows: The operator specifies a minimum and a maximum code in the range 0 through 377_8 and the number of codes to make up a block. Data are read, punched, and printed, starting with the minimum code and continuing until the block is complete. After using the minimum code within the range, and before reaching the end of the block, the test returns to the minimum code. Error counts are maintained for read errors since the expected read code is always known by these test sequences. The total number of frames in error, and the number of errors in each of the eight code positions are maintained in an error table. A special entry to this routine allows the operator to obtain a print of this table.

The teletype transfer-instructions test permits the operator to type information from the keyboard or to enter data through a low-speed paper tape reader. These characters are stored in a buffer until the end of the message is specified by a period. The data are then punched and printed. All of the teletype transfer instructions are used.

The printer output should be visually checked for errors. The punched paper tape may be visually checked or may be read using the read paper tape test. The punched paper tape produced by the read paper tape/punch/print test is automatically tested by reading the punched data.

11.3 USAGE

Operational procedures: The procedures used in the preventive mode of operation are described in section 3, maintain teletype driver routine for the preventive mode of operation, diagnostic package. The following procedures are used in the corrective mode of operation.

a. Prepare the paper tape reader and paper tape punch as follows:

   1. Read paper tape test: Load paper tape with appropriate codes on the teletype reader and ready the reader. This tape must be positioned so that the initial code of the block is the first code read.
   2. Punch/print test: Ready the teletype paper tape punch.

3. Read paper tape/punch/print test: Ready the teletype punch and reader. Punch a leader of null characters and, without tearing the paper from the punch, insert the leader into the reader.
4. Read keyboard/punch/print test: Ready the teletype punch.
5. Teletype transfer-instructions test: Ready the teletype punch if punching is desired. Prepare and insert a paper tape (unless keyboard input) into the teletype reader.

b. Provide the parameter as follows for all tests except the teletype transfer-instructions test:

$(\text{A register})_{7-0}$	Lower limit of the code range.
$(\text{B register})_{7-0}$	Upper limit of the code range.
(X register)	Number of codes in the block.

c. Run at the symbolic locations listed below:

TRH	Read paper tape test (high-speed read).
TRL	Read paper tape test (low-speed read).
TRK	Read keyboard test.
TP	Punch/print test.
TRHP	Read paper tape/punch/print test (high-speed read).
TRKP	Read keyboard/punch/print test.
TIRK	Teletype transfer-instructions test (keyboard input).
TIRL	Teletype transfer-instructions test (paper tape input).

d. For the teletype transfer-instructions test, provide the input message from the teletype keyboard or from the paper tape. The number of characters entered must not exceed the number of words reserved for the area TBUF. The message must be terminated with a period.

e. To print the error table, run at symbolic location TPRN.

Arguments or parameters: Parameter 1 is a minimum code in the block of data read or written. This code must be in the range 0 through 377_8. Parameter 2 is the maximum code in the block of data read or written. This code must be in the range 0 through 377_8. Parameter 3 is the number of codes in the block of data.

Space required: Approximately 608 words.

Temporary space requirements: Not applicable.

Alarms or printouts:

The error table printout consists of the total number of frames in error and the number of read errors in each bit position, 7 through 0, respectively. All numbers are printed as five octal digits and all are on one line:

TOTAL	BIT 7	BIT 6	BIT 0
XXXXX	XXXXX	XXXXX--------XXXXX	

Error returns or error codes:

See error stops for a description of the error codes.

Error stops:

An error halt occurs upon detection of a read error if SENSE switch 1 is selected. The registers are set at the halt as follows:

(Instruction counter)	The octal equivalent of symbolic location X18+1.
(A register)	Error bits in the code just read.
(B register)	Expected code.
(X register)	Total error count, in octal.

An error halt occurs if the teletype does not respond favorably to the sense-teletype-not-busy or the sense-buffer-ready instructions within a reasonable length of time. The registers are set at the halt as follows:

(Instruction counter)	The octal equivalent of symbolic location Z100-1.
(A register)	The sense instruction.
(B register)	177777 octal.

Input and output devices:

Model 33 teletype.

Input and output formats:

All inputs and outputs are in the form of eight-bit codes, or a printout of the characters which these codes represent.

SENSE switch settings:

SENSE switch 1, if selected, causes an error halt upon error detection.

If SENSE switch 2 is selected at the completion of the test, and if the user is operating in the corrective mode, the same test is repeated using the same parameters. The error table is not cleared before repeating the test.

Timing:

Not applicable.

Accuracy:

Not applicable.

Cautions to user:

Not applicable.

Equipment configuration: Minimum configuration with model 33 teletype (type A).

References: Not applicable.

11.4 METHOD

The read paper tape test reads one block of data each time the test is called. The teletype is selected OFF only once after the complete block is read.

The punch/print test punches one block of data each time the test is called. The teletype is selected OFF only once after the complete block is punched and printed.

The read keyboard/punch/print test alternately reads one block from the keyboard and punches and prints the code until the specified block is read and punched. The teletype is selected OFF after each code is read or punched.

The read paper tape/punch/print test sequence is as follows. (All reading is done at high speed.)

a. Punch 41 rubs out codes and selects the teletype OFF.

b. Read through the first rubout character for synchronization.

c. Punch and print the specified block of data and select teletype OFF.

d. Punch 40 nulls characters and selects teletype OFF.

e. Alternately read and punch one rub-out code at a time until 40 codes are read and punched. The teletype is selected OFF after each code is read or punched.

f. Alternately read, punch, and print a code of the specified block until the complete block is read, punched, and printed. The teletype is selected OFF after each code is read or punched and printed.

g. Alternately read and punch one null code at a time until 40 codes are read and punched. The teletype is selected OFF after each code is read or punched.

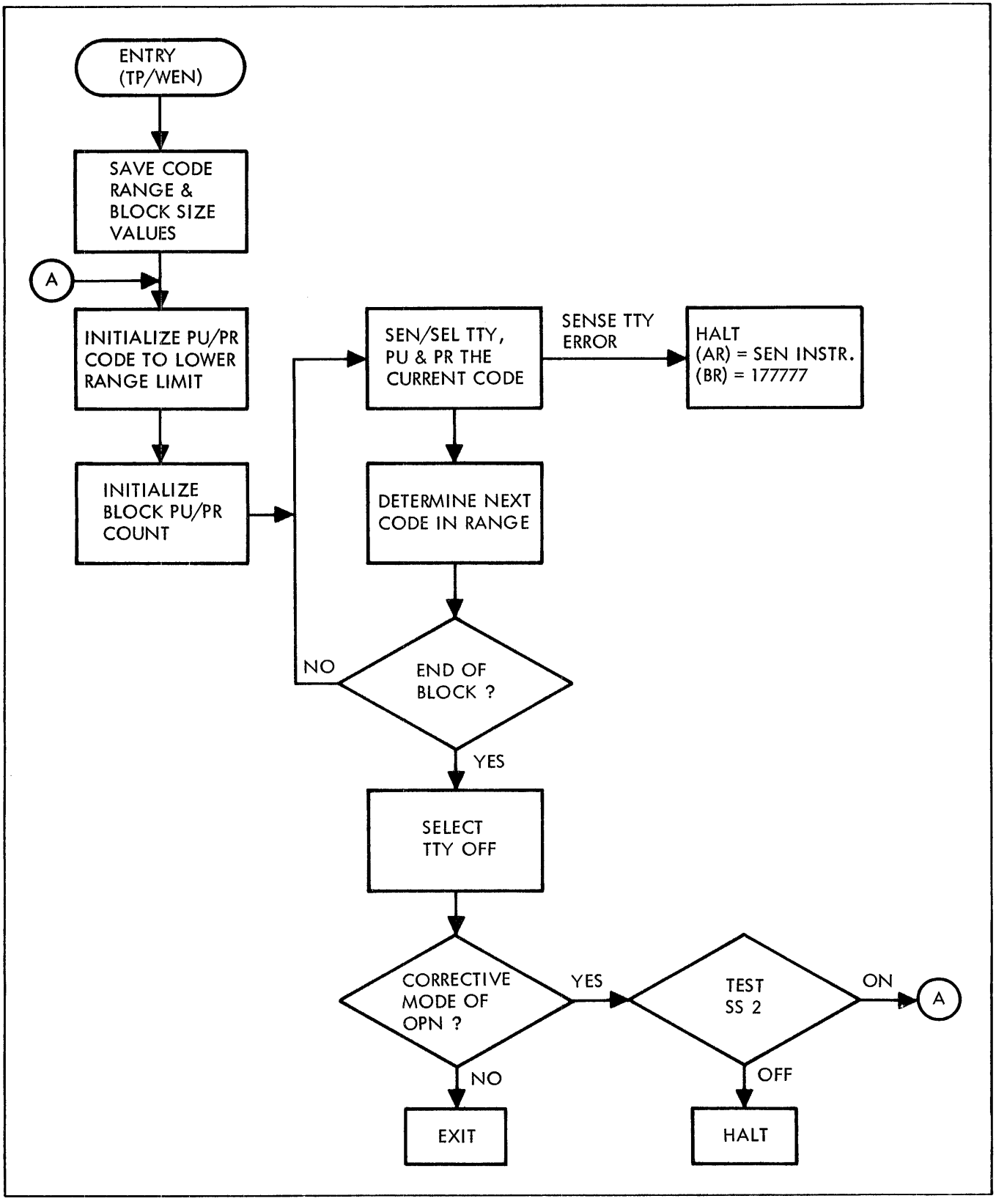
h. Punch 40 nulls codes and selects teletype OFF.

i. Read 40 rubs out codes and selects teletype OFF.

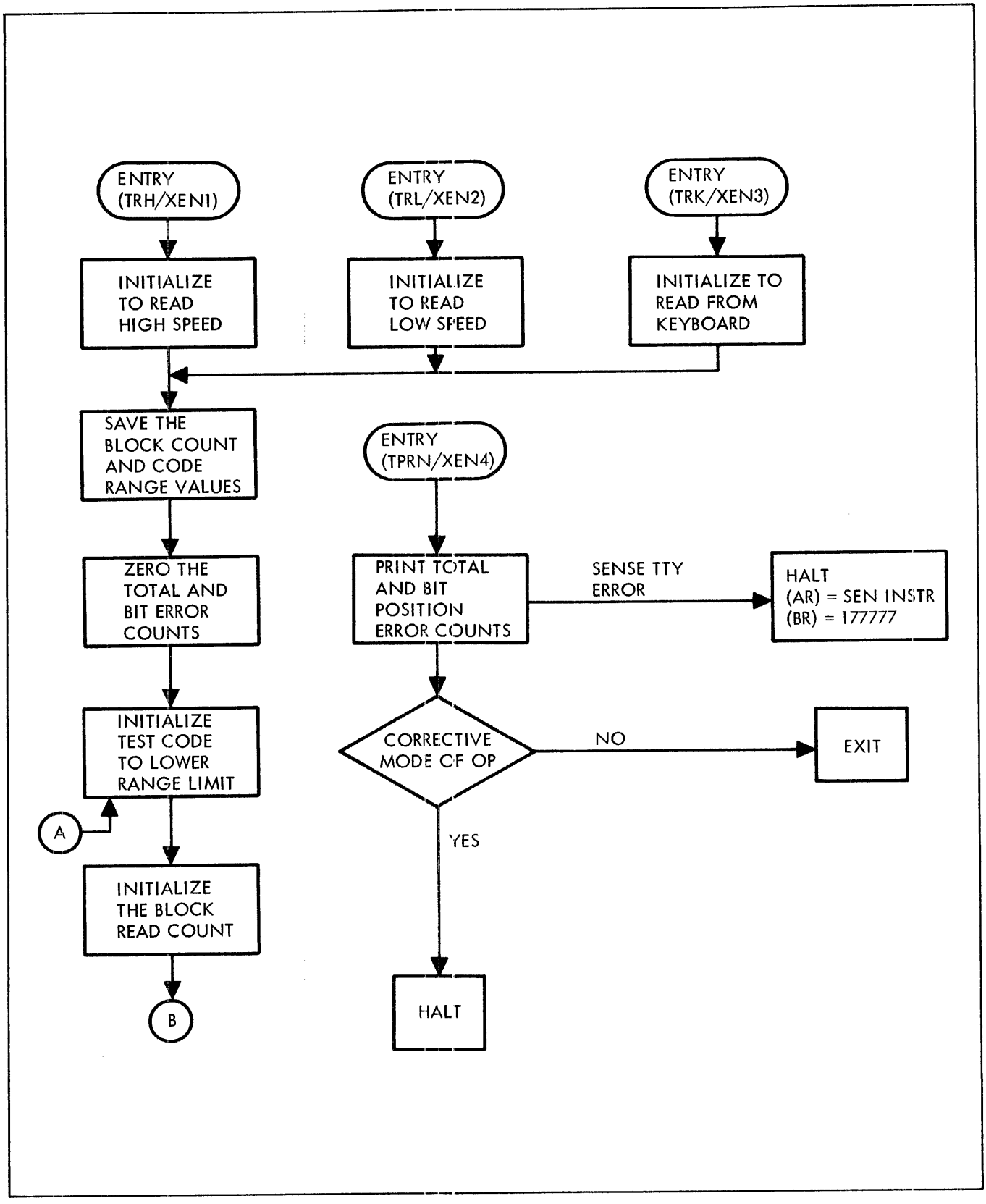
j. Read the specified block of data and select teletype OFF.

k. Read 40 nulls characters and selects teletype OFF.

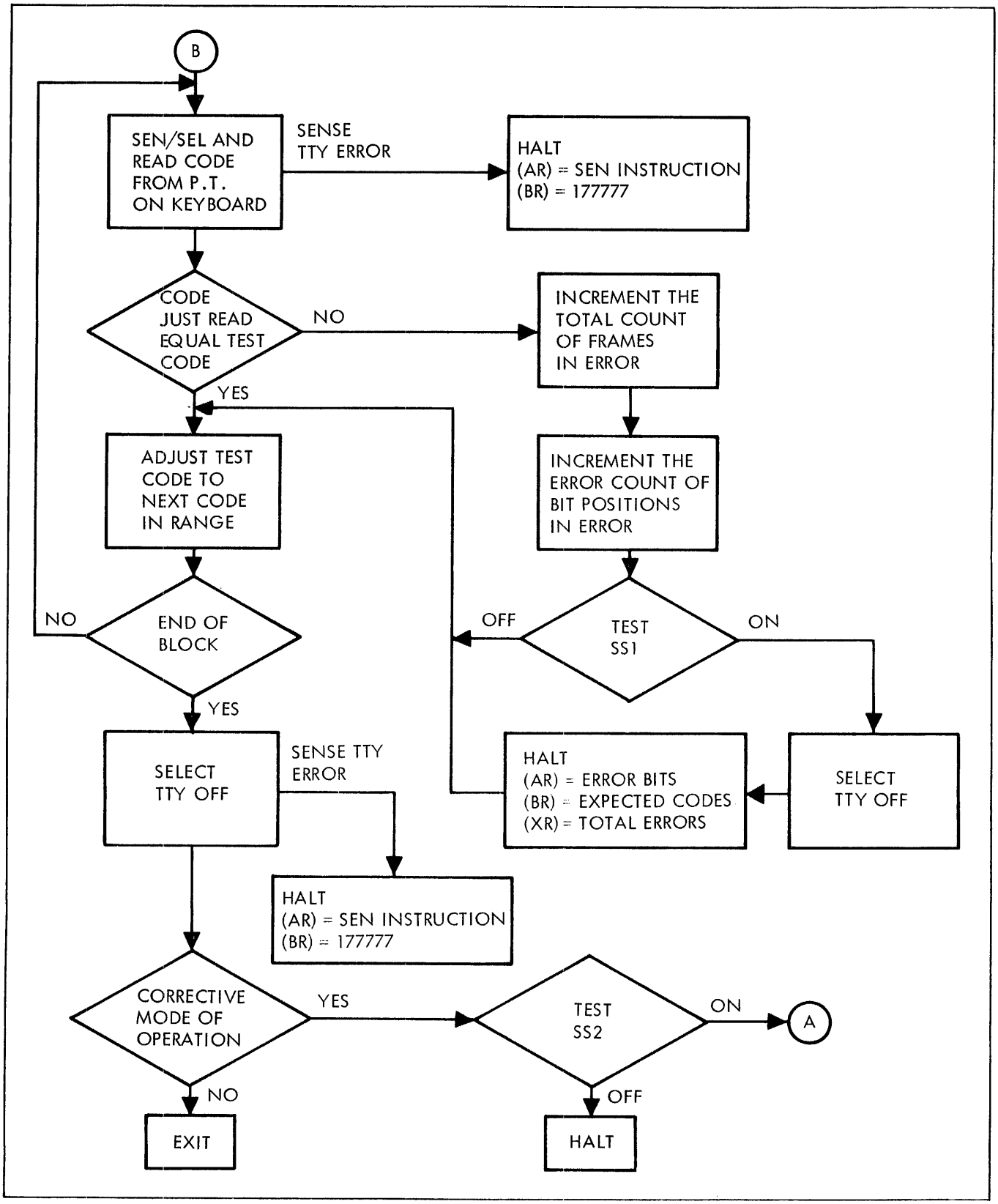
l. If any read errors occur, print the error table.



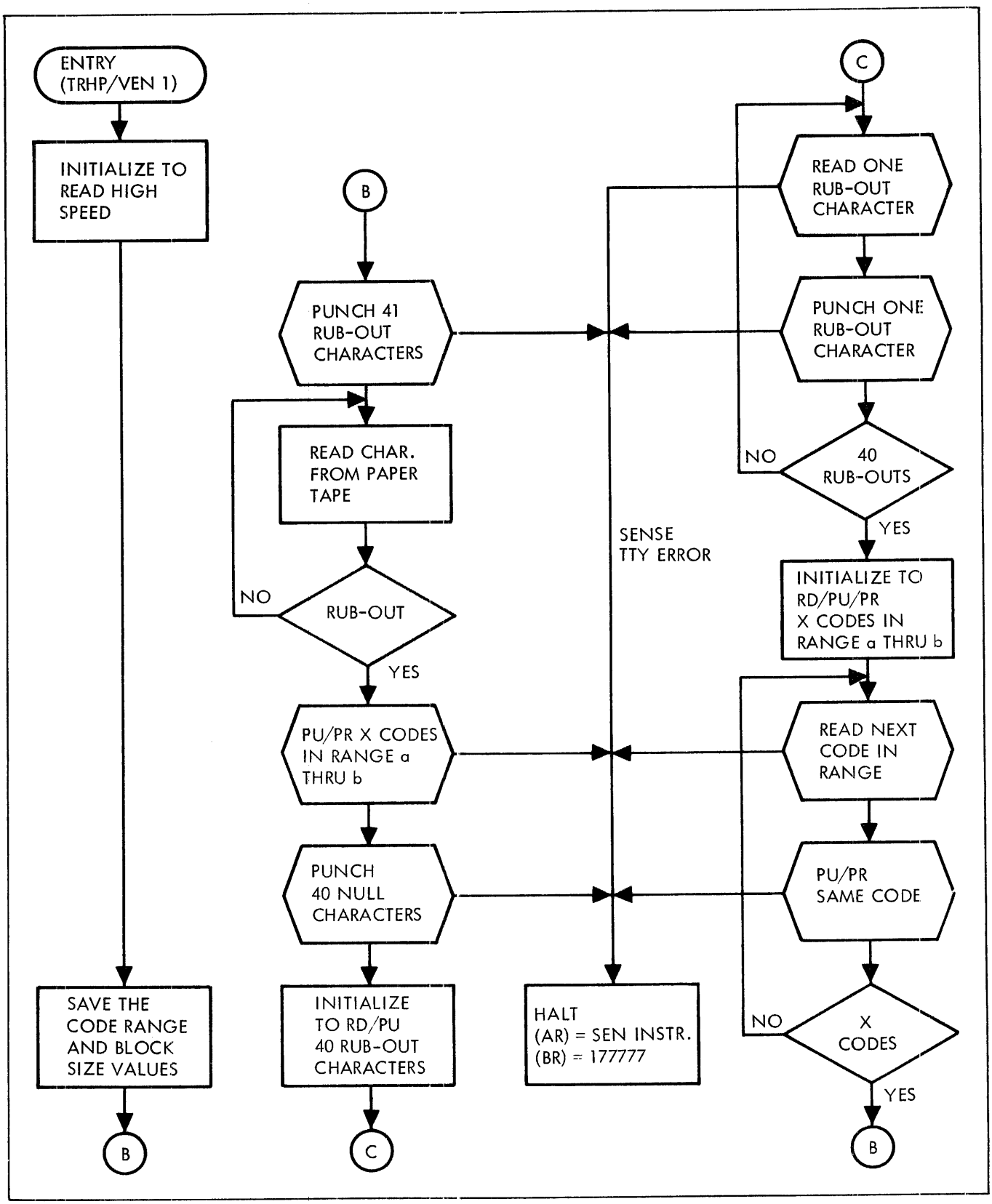
Punch/Print Test



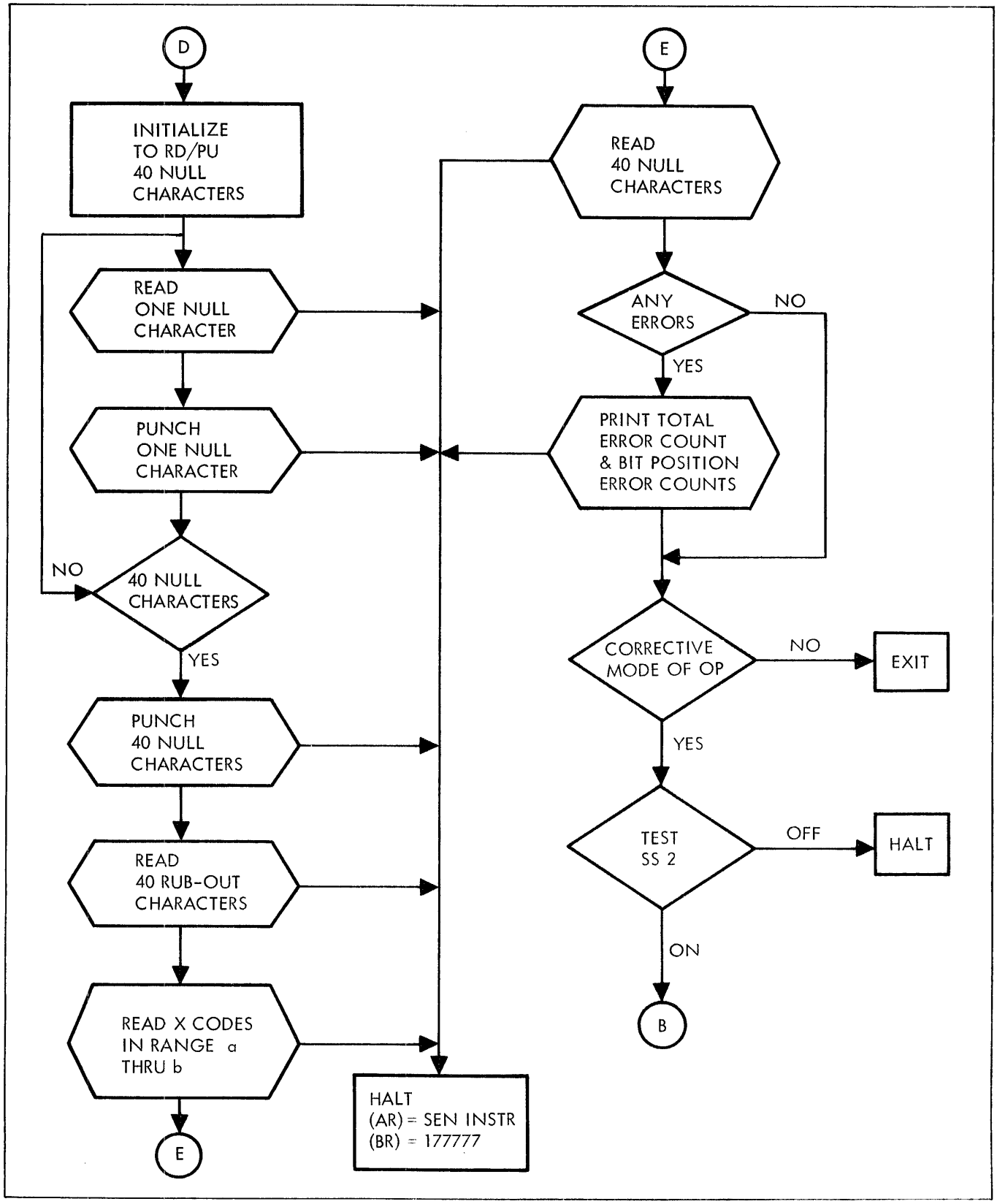
Read Paper Tape And Read Keyboard Tests



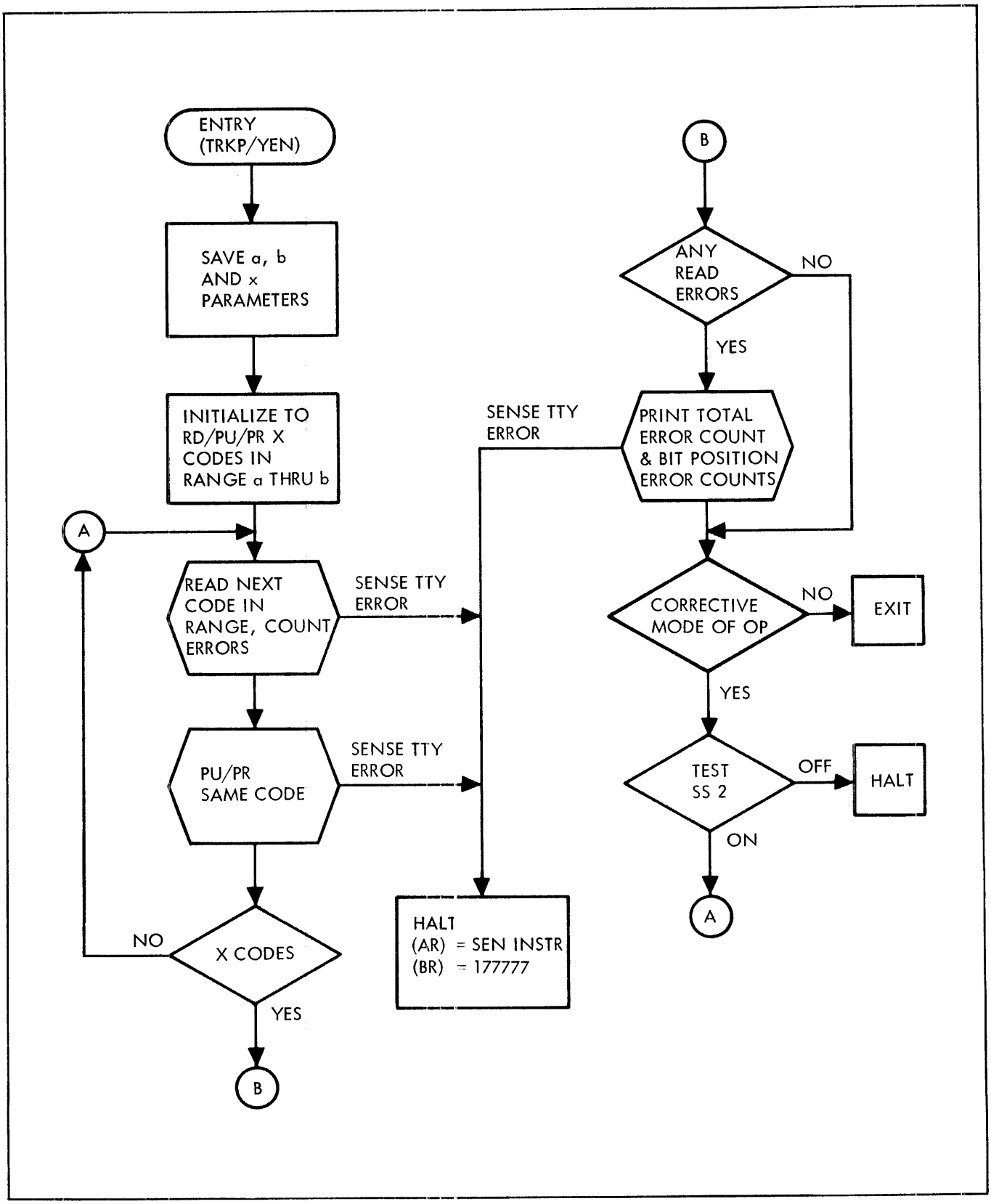
Read Paper Tape And Read Keyboard Tests



Read Paper Tape/Punch/Print Test



Read Paper Tape/Punch/Print Test



Read Keyboard/Punch/Print Test

APPENDICES

Appendix A
DATA 620/i Number System

DATA 620/i Number System

Binary numbers in the DATA 620/i are represented in 2's-complement form. Single-precision numbers are 15 bits plus sign (16-bit configuration) or 17 bits plus sign (18-bit configuration). The sign bit occupies the most-significant bit position (15 or 17). A "0" in the sign position denotes a positive number; a "1" in the sign position denotes a negative number. The negative of a positive number is represented in 2's-complement form.

The 2's-complement of a number may be found in either of two ways:

a. Take the 1's-complement of the number (i.e., complement each bit); add "1" in the least-significant bit position. Example:

+9	0000000000001001
1's-complement	1111111111110110
	+0000000000000001
2's-complement (-9)	1111111111110111

b. For an n-bit number (including sign) subtract it from 2^{n+1}. Example:

2^{n+1}	10000000000000000
-(+9)	-0000000000001001
-9	1111111111110111

It is generally convenient to express binary numbers by their octal equivalent. This conversion is easily performed by grouping the binary bits by threes, starting with the least-significant bit. Thus, in the 18-bit configuration, numbers may be expressed by six full octal digits ($000000\text{-}777777_8$).

In the 16-bit configuration, the range of octal numbers is less than six full digits ($000000\text{-}177777_8$). The octal equivalents for the above examples are:

Decimal	Octal
+9	000011_8
-9	177767_8

The range of numbers in the DATA 620/i is from -2^{15} to $+2^{15}-1$ for the 16-bit configuration and -2^{17} to $+2^{17}-1$ for the 18-bit configuration. The zero minus 1 and plus/minus full-scale numbers for the 16-bit configuration are:

Binary	Octal	Decimal	
0111111111111111	077777_8	+32,767	+Full Scale
0000000000000000	000000	0	0
1111111111111111	177777_8	-1	-1
1000000000000000	100000_8	-32,768	-Full Scale

The negative of the octal equivalent number is found by subtracting the number from 177777_8 and adding 1 in the least-significant digit (subtract from 777777_8 for the 18-bit configuration). Example:

$$\begin{array}{ll} & 177777_8 \\ -(9) & -000011_8 \\ \hline & +1 \\ \hline (-9) & 177767_8 \end{array}$$

In performing addition or subtraction, it is possible for the results to exceed the ± full scale range of the machine. For example:

Decimal	Octal	
+21,980	052734_8	
+11,843	$+027103_8$	
33,823	102037_8	-31,713

The negative result is in error. The same type of error occurs if the sum of the two negative numbers exceeds the minus full-scale range:

Decimal	Octal	
-21,980	125044_8	
(+)-11,843	150675_8	
-33,823	$(1)075741_8$	31,803

Note that the carry out of the most-significant octal digit position is generally lost. However, to inform the programmer that the true result of an addition/subtraction falls outside the range of the machine, an overflow indicator is provided. The overflow indicator is set if the sign bit changes when two numbers of the same sign are added together (where the sign of the subtrahend is changed in subtraction).

In multiplication, a double-length product is formed in the arithmetic registers (A or B). Since the product cannot exceed 32-bits (36-bits in the 18-bit configuration), overflow will never occur as the result of a multiply. The sign of the product is automatically determined.

Example:

Decimal	Octal
21,980	052734
X 11,843	027103
65,940	200624
87,920	52734
175,840	454404
21,980	125670
21,980	
260,299,140	001741000224
	A B

The double-length result is accumulated in the A and B registers.

In division, an overflow (underflow) can occur if the divisor is less than or equal to the dividend.

Appendix B
Standard DATA 620/i Subroutines

Standard DATA 620/i Subroutines

Subroutines	Locations	Time
Elementary Functions*		
Log^{e} (1 + X), (0 ≤ X < 1)	20	8470 usec
Exponential (e^{-X}) (0 ≤ X < 1)	20	4958 usec
Exponential (e^{+x}) (0 ≤ X < 1)	18	5104 usec
Square Root (0 ≤ X < 1)	67	1443 usec
Sine X ($-\pi < X < \pi$)	30	5689 usec
Cosine X ($-\pi < X < \pi$)	18	5835 usec
Arctan (-1 to 1)	14	8323 usec
Single Precision (fixed point)		
Multiply (optional)	hardware	18 usec
Divide (optional)	hardware	27 usec
Divide (programmed)	77	424 usec
Double Precision (fixed point)		
Closed		
Addition	23	56 usec
Subtraction	25	59 usec
Multiply	36	3030 usec
Divide	35	2326 usec
Conversion		
Binary-to-BCD (4 characters)	32	249 usec
BCD-to-Binary	28	205 usec

*All elementary functions exept square root require a subroutine called POLY, which takes 42 locations.

Appendix C
Table of Powers of Two

Table of Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

APPENDIX D
OCTAL-DECIMAL INTEGER CONVERSION TABLE

OCTAL-DECIMAL INTEGER CONVERSION TABLE

0000	0000
to	to
0777	0511
(Octal)	(Decimal

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000	0512
to	to
1777	1023
(Octal)	(Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

OCTAL-DECIMAL INTEGER CONVERSION TABLE

4000 to 4777 (Octal)	2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 Octal)	2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000	3072
to	to
6777	3583
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	**4067**	4068	4069	4070	4071
7750	4072	4073	**4074**	**4075**	4076	4077	4078	4079
7760	4080	4081	**4082**	**4083**	4084	4085	4086	4087
7770	4088	4089	**4090**	**4091**	4092	4093	4094	4095

7000	3584
to	to
7777	4095
(Octal)	(Decimal)

APPENDIX E
OCTAL-DECIMAL FRACTION CONVERSION TABLE

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

Appendix F
DATA 620/i Instructions (Alphabetical Order)

Appendix F
DATA 620/i Instructions (Alphabetical Order)

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
ADD	120000	Add to A Register	1	2	Yes
ADDE*	00612z	Add to A Register Extended	2	3	Yes
ADDI	006120	Add to A Register Immediate	2	2	No
ANA	150000	AND to A Register	1	2	Yes
ANAE*	00615z	AND to A Register Extended	2	3	Yes
ANAI	006150	AND to A Register Immediate	2	2	No
AØFA	005511	Add OF to A Register	1	1	No
AØFB	005522	Add OF to B Register	1	1	No
AØFX	005544	Add OF to X Register	1	1	No
ASLA	00420x+n	Arithmetic Shift Left A n Places	1	1+0.25n	No
ASLB	00400x+n	Arithmetic Shift Left B n Places	1	1+0.25n	No
ASRA	00430x+n	Arithmetic Shift Right A n Places	1	1+0.25n	No
ASRB	00410x+n	Arithmetic Shift Right B n Places	1	1+0.25n	No
CIA	1025xx	Clear and Input to A Register	1	2	No
CIAB	1027xx	Clear and Input to A and B Registers	1	2	No
CIB	1026xx	Clear and Input to B Register	1	2	No
CPA	005211	Complement A Register	1	1	No
CPB	005222	Complement B Register	1	1	No
CPX	005244	Complement X Register	1	1	No
DAR	005311	Decrement A Register	1	1	No
DBR	005322	Decrement B Register	1	1	No

x = 0 through 7; z = 4 through 7

*Optional Instructions. See table 10, appendix G

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
DIV*	170000	Divide AB Register 16-Bit 18-Bit	1 1	10-14 11-15	Yes
DIVE*	00617z	Divide AB Register Extended 16-Bit 18-Bit	2	11-15 12-16	Yes
DIVI*	006170	Divide AB Register Immediate 16-Bit 18-Bit	2	10-14 11-15	No
DXR	005344	Decrement X Register	1	1	No
ERA	130000	Exclusive OR to A Register	1	2	Yes
ERAE*	00613z	Exclusive OR to A Register Extended	2	3	Yes
ERAI	006130	Exclusive OR to A Register Immediate	2	2	No
EXC	100xxx	External Control Function	1	1	No
HLT	000000	Halt	1	1	No
IAR	005111	Increment A Register	1	1	No
IBR	005122	Increment B Register	1	1	No
IME	1020xx	Input to Memory	2	3	No
INA	1021xx	Input to A Register	1	2	No
INAB	1023xx	Input to A and B Registers	1	2	No
INB	1022xx	Input to B Register	1	2	No
INR	040000	Increment and Replace	1	3	Yes
INRE*	00604z	Increment and Replace Extended	2	4	Yes
INRI	006040	Increment and Replace Immediate	2	3	No
IXR	005144	Increment X Register	1	1	No
JAN	001004	Jump if A Register Negative	2	2	Yes
JANM	002004	Jump and Mark if A Register Negative	2	2-3	Yes

x = 0 through 7; z = 4 through 7

*Optional Instructions. See table 10, appendix G

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
JAP	001002	Jump if A Register Positive	2	2	Yes
JAPM	002002	Jump and Mark if A Register Positive	2	2-3	Yes
JAZ	001010	Jump if A Register Zero	2	2	Yes
JAZM	002010	Jump and Mark if A Register zero	2	2-3	Yes
JBZ	001020	Jump if B Register Zero	2	2	Yes
JBZM	002020	Jump and Mark if B Register Zero	2	2-3	Yes
JMP	001000	Jump Unconditionally	2	2	Yes
JMPM	002000	Jump and Mark Unconditionally	2	3	Yes
JØF	001001	Jump if Overflow On	2	2	Yes
JØFM	002001	Jump and Mark if Overflow On	2	2-3	Yes
JS1M	002100	Jump and Mark if Sense Switch 1 On	2	2-3	Yes
JS2M	002200	Jump and Mark if Sense Switch 2 On	2	2-3	Yes
JS3M	002400	Jump and Mark if Sense Switch 3 On	2	2-3	Yes
JSS1	001100	Jump if Sense Switch 1 On	2	2	Yes
JSS2	001200	Jump if Sense Switch 2 On	2	2	Yes
JSS3	001400	Jump if Sense Switch 3 On	2	2	Yes
JXZ	001040	Jump if X Register Zero	2	2	Yes
JXZM	002040	Jump and Mark if X Register Zero	2	2-3	Yes
LASL	00440x+n	Long Arithmetic Shift Left n Places	1	1+0.50n	No
LASR	00450x+n	Long Arithmetic Shift Right n Places	1	1+0.50n	No

x = 0 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
LDA	010000	Load A Register	1	2	Yes
LDAE*	0060Iz	Load A Register Extended	2	3	Yes
LDAI	006010	Load A Register Immediate	2	2	No
LDB	020000	Load B Register	1	2	Yes
LDBE*	00602z	Load B Register Extended	2	3	Yes
LDBI	006020	Load B Register Immediate	2	2	No
LDX	030000	Load X Register	1	2	Yes
LDXE*	00603z	Load X Register Extended	2	3	Yes
LDXI	006030	Load X Register Immediate	2	2	No
LLRL	00444x+n	Long Logical Rotate Left n Places	1	1+0.50n	No
LLSR	00454x+n	Long Logical Shift Right n Places	1	1+0.50n	No
LRLA	00424x+n	Logical Rotate Left A n Places	1	1+0.25n	No
LRLB	00404x+n	Logical Rotate Left B n Places	1	1+0.25n	No
LSRA	00434x+n	Logical Shift Right A n Places	1	1+0.25n	No
LSRB	00414x+n	Logical Shift Right B n Places	1	1+0.25n	No
MUL*	160000	Multiply B Register 16-Bit 18-Bit	1	10 11	Yes
MULE*	00616z	Multiply B Register Extended 16-Bit 18-Bit	2	11 12	Yes
MULI*	006160	Multiply B Register Immediate 16-Bit 18-Bit	2	10 11	No
NØP	005000	No Operation	1	1	No
ØAB	1033xx	Output from A and B Registers	1	2	No
ØAR	1031xx	Output from A Register	1	2	No
ØBR	1032xx	Output from B Register	1	2	No

x = 0 through 7; z = 4 through 7

*Optional Instructions. See table 10, appendix G

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
ØME	1030xx	Output from Memory	2	3	No
ØRA	110000	Inclusive OR to A Register	1	2	Yes
ØRAE*	006llz	Inclusive OR to A Register Extended	2	3	Yes
ØRAI	006110	Inclusive OR to A Register Immediate	2	2	No
RØF	007400	Reset Overflow	1	1	No
SEN	101xxx	Sense Input/Output Lines	2	2	Yes
SØF	007401	Set Overflow	1	1	No
SØFA	005711	Subtract OFLO from A Register	1	1	No
SØFB	005722	Subtract OFLO from B Register	1	1	No
SØFX	005744	Subtract OFLO from X Register	1	1	No
STA	050000	Store A Register	1	2	Yes
STAE*	00605z	Store A Register Extended	2	3	Yes
STAI	006050	Store A Register Immediate	2	2	No
STB	060000	Store B Register	1	2	Yes
STBE*	00606z	Store B Register Extended	2	3	Yes
STBI	006060	Store B Register Immediate	2	2	No
STX	070000	Store X Register	1	2	Yes
STXE*	00607z	Store X Register Extended	2	3	Yes
STXI	006070	Store X Register Immediate	2	2	No
SUB	140000	Subtract from A Register	1	2	Yes
SUBE*	00614z	Subtract from A Register Extended	2	3	Yes

x = 0 through 7; z = 4 through 7

*Optional Instructions. See table 10, appendix G

Mnemonic	Octal	Description	Words/ Inst	Time Cycles	Indirect Address
XS1	003100	Execute SENSE switch 1 set	2	2	Yes
XS2	003200	Execute SENSE switch 2 set	2	2	Yes
XS3	003400	Execute SENSE switch 3 set	2	2	Yes
XXZ	003040	Execute X register zero	2	2	Yes

Appendix G
DATA 620/i Instructions (By Type)

Table G-1
Single-Word Addressed Instructions

Table G-1(a)
Load/Store Instruction Group

Op Code		Instruction	Timing (Cycles)
Octal	Mnemonic		
01	LDA	Load A Register	2
02	LDB	Load B Register	2
03	LDX	Load X Register	2
05	STA	Store A Register	2
06	STB	Store B Register	2
07	STX	Store X Register	2

Table G-1(b)
Arithmetic Instruction Group

Op Code		Instruction	Timing (Cycles)
Octal	Mnemonic		
04	INR	Increment and Replace	3
12	ADD	Add Memory to A	2
14	SUB	Subtract Memory from A	2
16	MUL(*)	Multiply 16-bit	10
		18-bit	11
17	DIV(*)	Divide 16-bit	10-14
		18-bit	11-15

*Optional Instructions

Table G-1(c)
Logical Instruction Group

Op Code		Instruction	Timing (Cycles)
Octal	Mnemonic		
11	ØRA	Inclusive OR, Memory and A	2
13	ERA	Exclusive OR, Memory and A	2
15	ANA	AND Memory and A	2

Table G-1(d)
Addressing Modes for Single Word Addressed Instructions

M Field			Addressing Mode	Operation
11	10	9		
0	X	X	Direct	Combine bits 9, 10 with A field (0-8) to form effective address (0000 - 2047).
1	0	0	Relative	Add A field (bits 0-8) to contents of P to form effective address (Mod 2^{15}).
1	0	1	Index (X Register)	Add A field (bits 0-8) to contents of X to form effective address (Mod 2^{15}).
1	1	0	Index (B Register)	Add A field (bits 0-8) to contents of B to form effective address (Mod 2^{15}).
1	1	1	Indirect	A field (bits 0-8) specifies location of an address word.

Table G-2
Control Instruction Group Codes
(Single-Word, Non-Addressable)

Op Code		M Field	A Field	Instruction	Timing (Cycles)
Octal	Mnemonic				
00	HLT	0	XXX	Halt	1
00	NØP	5	000	No Operation	1
00	RØF	7	400	Reset Overflow	1
00	SØF	7	401	Set Overflow	1

Table G-3
Shift Instruction Group

Table G-3(a)
Instruction Format

Octal	Octal	A Field								
OP Code	M Field	U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
00	4	0 = A or B 1 = A & B	0 = B 1 = A	0 = Left 1 = Right	0 = Arith. 1 = Logical rotate	Shift Count (0 - 31)				

Table G-3(b)
Instruction Format

U_8	U_7	U_6	U_5	Mnemonic	Shift Instruction	Timing (Cycles)
0	0	0	0	ASLB	Arithmetic Shift B Left	1 + 0.25n
0	0	0	1	LRLB	Logical Rotate B Left	1 + 0.25n
0	0	1	0	ASRB	Arithmetic Shift B Right	1 + 0.25n
0	0	1	1	LSRB	Logical Shift B Right	1 + 0.25n
0	1	0	0	ASLA	Arithmetic Shift A Left	1 + 0.25n
0	1	0	1	LRLA	Logical Rotate A Left	1 + 0.25n
0	1	1	0	ASRA	Arithmetic Shift A Right	1 + 0.25n
0	1	1	1	LSRA	Logical Shift A Right	1 + 0.25n
1	0	0	0	LASL	Long Arithmetic Shift A, B Left	1 + 0.50n
1	0	0	1	LLRL	Long Logical Rotate A, B Registers Left	1 + 0.50n
1	0	1	0	LASR	Long Arithmetic Shift A, B Right	1 + 0.50n
1	0	1	1	LLSR	Long Logical Shift, A, B Registers	1 + 0.50n
1	1	0	0		Invalid	
1	1	0	1		Invalid	
1	1	1	0		Invalid	
1	1	1	1		Invalid	

Table G-4
Register Change Instruction Group

Table G-4(a)
Instruction Format

Octal		A Field						
		Source				Dest.		
Class Code	M Field	U_8	U_7	U_6	U_5 U_4 U_3	U_2	U_1	U_0	Type of Transfer
00	5	See Note (2)	0	0	X B A	X	B	A	Transfer Unchanged
			0	1					Transfer Incremented
			1	0					Transfer Complemented
			1	1					Transfer Decremented

NOTES:
1. Multiple source transfer results in inclusive-OR; multiple source complemented results in complement inclusive-OR.
2. Bit-8 is the conditional indicator. If Bit-8 is zero, the instruction is executed unconditionally. If Bit-8 is one, the instruction is executed only if the overflow is on.

Table G-4(b)
Register Change Instruction Codes

Class Code Field Octal	Mnemonic	Register Change Instruction	Timing
0 0 1	TZA	Transfer Zero to A Register	1
0 0 2	TZB	Transfer Zero to B Register	1
0 0 4	TZX	Transfer Zero to X Register	1
0 1 2	TAB	Transfer A Register to B Register	1
0 1 4	TAX	Transfer A Register to X Register	1
0 2 1	TBA	Transfer B Register to A Register	1
0 2 4	TBX	Transfer B Register to X Register	1
0 4 1	TXA	Transfer X Register to A Register	1
0 4 2	TXB	Transfer X Register to B Register	1
1 1 1	IAR	Increment A Register	1
1 2 2	IBR	Increment B Register	1
1 4 4	IXR	Increment X Register	1
2 1 1	CPA	Complement A Register	1
2 2 2	CPB	Complement B Register	1
2 4 4	CPX	Complement X Register	1
3 1 1	DAR	Decrement A Register	1
3 2 2	DBR	Decrement B Register	1
3 4 4	DXR	Decrement X Register	1
5 1 1	AØFA	Add Overflow to A Register	1
5 2 2	AØFB	Add Overflow to B Register	1
5 4 4	AØFX	Add Overflow to X Register	1
7 1 1	SØFA	Subtract Overflow from A Register	
7 2 2	SØFB	Subtract Overflow from B Register	
7 4 4	SØFX	Subtract Overflow from X Register	

Table G-5
Jump Instruction Group

Table G-5(a)
Instruction Format

Octal		A Field								
OP Code	M Field	U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
00	1	SS3 ON	SS2 ON	SS1 ON	X = 0	B = 0	A = 0	A < 0	A ≥ 0	OF = 1

Note: Jump condition is logical AND of all A field bits.

Table G-5(b)
Jump Instruction Codes

A Field Octal	Mnemonic	Jump Instruction	Timing (Cycles)
0 0 0	JMP	Jump Unconditionally	2
0 0 1	JØF	Jump If Overflow Set	2
0 0 2	JAP	Jump If A Register Positive	2
0 0 4	JAN	Jump If A Register Negative	2
0 1 0	JAZ	Jump If A Register Zero	2
0 2 0	JBZ	Jump If B Register Zero	2
0 4 0	JXZ	Jump If X Register Zero	2
1 0 0	JSS1	Jump If Sense Switch 1 Set	2
2 0 0	JSS2	Jump If Sense Switch 2 Set	2
4 0 0	JSS3	Jump If Sense Switch 3 Set	2

Table G-6
Jump-and-Mark Instruction Group

Table G-6(a)
Instruction Format

Octal		A Field								
OP Code	M Field	U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
00	2	SS3	SS2	SS1	X = 0	B = 0	A = 0	A < 0	A ≥ 0	OF = 1

Note: Jump and Mark condition is logical-AND of all A field bits.

Table G-6(b)
Jump-and-Mark Instruction Codes

A Field Octal	Mnemonic	Jump-and-Mark Instructions	Timing (Cycles)
000	JMPM	Jump and Mark Unconditionally	3
001	JØFM	Jump and Mark if Overflow Set	2 (3 if Jump)
002	JAPM	Jump and Mark if A Register Positive	2 (3 if Jump)
004	JANM	Jump and Mark if A Register Negative	2 (3 if Jump)
010	JAZM	Jump and Mark if A Register Zero	2 (3 if Jump)
020	JBZM	Jump and Mark if B Register Zero	2 (3 if Jump)
040	JXZM	Jump and Mark if X Register Zero	2 (3 if Jump)
100	JS1M	Jump and Mark if Sense Switch 1 On	2 (3 if Jump)
200	JS2M	Jump and Mark if Sense Switch 2 On	2 (3 if Jump)
400	JS3M	Jump and Mark if Sense Switch 3 On	2 (3 if Jump)

Table G-7
Execute Instruction Group

Table G-7(a)
Instruction Format

Octal		A Field								
OP Code	M Field	U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
0 0	3	SS3 ON	SS2 ON	SS1 ON	X = 0	B = 0	A = 0	A 0	A 0	OF = 1

Note: Execute condition is logical-AND of all A field bits. Executed instruction must be single word.

Table G-7(a)
Instruction Format

A Field Octal	Mnemonic	Execute Instruction	Timing (Cycles)
000	XEC	Execute Unconditionally	2
001	XØF	Execute if Overflow Set	2
002	XAP	Execute if A Register Positive	2
004	XAN	Execute if A Register Negative	2
010	XAZ	Execute if A Register Zero	2
020	XBZ	Execute if B Register Zero	2
040	XXZ	Execute if X Register Zero	2
100	XS1	Execute if Sense Switch 1 set	2
200	XS2	Execute if Sense Switch 2 set	2
400	XS3	Execute if Sense Switch 3 set	2

Table G-8
Immediate Instruction Group

OP Code		Octal		Instruction	Timing (Cycles)
Octal	Mnemonic	M Field	a FIELD		
00	LDAI	6	010	Load A Immediate	2
00	LDBI	6	020	Load B Immediate	2
00	LDXI	6	030	Load X Immediate	2
00	INRI	6	040	Increment and Replace Immediate	2
00	STAI	6	050	Store A Immediate	2
00	STBI	6	060	Store B Immediate	2
00	STXI	6	070	Store X Immediate	2
00	ØRAI	6	110	Inclusive OR Immediate	2
00	ADDI	6	120	Add Immediate	2
00	ERAI	6	130	Exclusive OR Immediate	2
00	SUBI	6	140	Subtract Immediate	2
00	ANAI	6	150	AND Immediate	2
00	MULI*	6	160	Multiply Immediate 16 bits 18 bits	10 11
00	DIVI*	6	170	Divide Immediate 16 bits 18 bits	10-14 11-15

*Optional Instructions

Table G-9
Input/Output Instruction Group

OP Code		Octal		Instruction	Timing (Cycles)
Octal	Mnemonic	M Field	A Field		
10	EXC	0	XZZ	External Control	1
10	SEN	1	XZZ	Program Sense	2
10	IME	2	0ZZ	Input to Memory	3
10	INA	2	1ZZ	Input to A	2
10	INB	2	2ZZ	Input to B	2
10	CIA	2	5ZZ	Clear and Input to A	2
10	CIB	2	6ZZ	Clear and Input to B	2
10	ØME	3	0ZZ	Output from Memory	3
10	ØAR	3	1ZZ	Output from A	2
10	ØBR	3	2ZZ	Output from B	2

X - Mode or logical unit number

Z - Device number

Table G-10
Extended Address Instruction Group (Optional)

OP Code		Octal		Instruction	Timing (Cycles)
Octal	Mnemonic	M Field	A Field		
00	LDAE	6	01X	Load A Register Extended	3
00	LDBE	6	02X	Load B Register Extended	3
00	LDXE	6	03X	Load X Register Extended	3
00	STAE	6	05X	Store A Register Extended	3
00	STBE	6	06X	Store B Register Extended	3
00	STXE	6	07X	Store X Register Extended	3
00	INRE	6	04X	Increment and Replace Extended	4
00	ADDE	6	12X	Add Memory to A Register Extended	3
00	SUBE	6	14X	Subtract Memory from A Register Extended	3
00	MULE	6	16X	Multiply 16-Bit Extended Multiply 18-Bit Extended	11 12
00	DIVE	6	17X	Divide 16-Bit Extended Divide 18-Bit Extended	11 - 15 12 - 16
00	ØRAE	6	11X	Inclusive OR Extended	3
00	ERAE	6	13X	Exclusive OR Extended	3
00	ANAE	6	15X	AND Extended	3

X in the A field may equal 4 through 7

Appendix H
DATA 620/i Reserved Instruction Codes

Table H-1. 620/i-06-A Teletype Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0101	100101	Connect Write Register to BIC
EXC 0201	100201	Connect Read Register to BIC
EXC 0401	100401	Initialize
B. Transfer		
OAR 01	103101	Transfer A Register to Write Register
OBR 01	103201	Transfer B Register to Write Register
OME 01	103001	Transfer Memory Register to Write Register
INA 01	102101	Transfer Read Register to A Register
INB 01	102201	Transfer Read Register to B Register
IME 01	102001	Transfer Read Register to Memory Register
CIA 01	102501	Transfer Read Register to Cleared A Register
CIB 01	102601	Transfer Read Register to Cleared B Register
C. Sense		
SEN 0101	101101	Write Register Ready
SEN 0201	101201	Read Register Ready

D. Teletype Command Codes

Function	Symbol	Code	Typed As
Print Enable	SOM	201	Control and A
Print Suppress	EOT	204	Control and D
Reader On	XON	221	Control and Q
Punch On	TAPE	222	Control and R
Reader Off	XOFF	223	Control and S
Punch Off	TAPE OFF	224	Control and T

Teletype models are listed as follows:

620-60B	(ASR-33 TM)
620-61B	(ASR-35 TM)
620-62B	(KSR-35 TM)

Note: External control instructions are for use only with the BIC.

Table H-2. 620/i-10 Multiply/Divide and Extended Addressing Instructions

	Mnemonic	Octal Code	Functional Description	Time/Cycles
A.	Divide (one-word instruction)			
	DIV	170000	Divide AB register 16-bit 18-bit	10-14 11-15
B.	Multiply (one-word instruction)			
	MUL	160000	Multiply B register 16-bit 18-bit	10 11
C.	Extended Address (two-word instruction)			
	LDAE	00601X	Load A register extended	3
	LDBE	00602X	Load B register extended	3
	LDXE	00603X	Load X register extended	3
	STAE	00605X	Store A register extended	3
	STBE	00606X	Store B register extended	3
	STXE	00607X	Store X register extended	3
	INRE	00604X	Increment and Replace Extended	4
	ADDE	00612X	Add memory to A register extended	3
	SUBE	00614X	Subtract memory from A register extended	3
	MULE	00616X	Multiply B register extended 16-bit 18-bit	11 12
	DIVE	00617X	Divide AB register extended 16-bit 18-bit	11-15 12-16
	ORAE	00611X	Inclusive OR extended	3
	ERAE	00613X	Exclusive OR extended	3
	ANAE	00615X	AND extended	3

Table H-3
620/i-13 Real Time Clock Instructions

Mnemonic	Octal Code	Functional Description
EXC 0147	100147	Enable RTC. Enables both increment and overflow interrupts.
EXC 0447	100447	Disable RTC (initialize). Disables both increment and overflow interrupts, resets interrupt register and "divide-by-eight" counter.
EXC 0247	100247	Disable Overflow. Inhibits overflow interrupt requests.
EXC 0347	100347	Enable Increment/disable overflow. Enables increment interrupt; inhibits overflow interrupts.

Table H-4
620/i-16 Priority Interrupt Module Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 014X*	10014X*	Clear interrupt registers
EXC 024X	10024X	Enable PIM
EXC 034X	10034X	Clear interrupt registers and enable PIM
EXC 044X	10044X	Disable PIM
EXC 054X	10054X	Clear interrupt registers and disable PIM
B. Data Transfer		
ØME 04X	10304X	Transfer memory to mask register
ØAR 04X	10314X	Transfer A register content to mask register
ØBR 04X	10324X	Transfer B register content to mask register

*X represents the last character of device address. Its value ranges from 0 through 7 and is determined by jumper connections on the PIM backplane.

Table H-5
620/i-20 Buffer Interlace Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 020	100020	Active Enable
EXC 021	100021	Initialize
B. Transfer		
OAR 020	103120	Load Initial Register from A
ØBR 020	103220	Load Initial Register from B
ØME 020	103020	Load Initial Register from Memory
ØAR 021	103121	Load Final Register from A
ØBR 021	103221	Load Final Register from B
ØME 021	103021	Load Final Register from Memory
INA 020	102120	Read Initial Register into A
INB 020	102220	Read Initial Register into B
IME 020	102020	Read Initial Register into Memory
CIA 020	102520	Read Initial Register into Cleared A
CIB 020	102620	Read Initial Register into Cleared B
C. Sense		
SEN 020	101020	Sense BIC Not Busy
SEN 021	101021	Sense Abnormal Device Stop

Table H-6
620/i-22/23 Card Reader Controllers Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0230	100230	Read One Card
B. Transfer		
IME 030	102030	Transfer Character to Memory
INA 030	102130	Transfer Character to A Reg.
INB 030	102230	Transfer Character to B Reg.
CIA 030	102530	Transfer Character to A Reg., Cleared
CIB 030	102630	Transfer Character to B Reg., Cleared
C. Sense		
SEN 0130	101130	Sense Character Ready
SEN 0230	101230	Sense Reader Error
SEN 0330	101330	Sense Hopper Empty
SEN 0630	101630	Sense Reader Ready

Table H-7
620/i-30 9-track Magnetic Tape System Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 010	100010	Read One Record
EXC 0210	100210	Write One Record
EXC 0410	100410	Write File Mark
EXC 0510	100510	Forward One Record
EXC 0610	100610	Backspace One Record
EXC 0710	100710	Rewind
B. Transfer		
OME 010	103010	Output Memory to Magnetic Tape Buffer
OAR 0110	103110	Output A Reg to Magnetic Tape Buffer
OBR 0210	103210	Output B Reg to Magnetic Tape Buffer
IME 010	102010	Input Magnetic Tape Buffer to Memory
INA 0110	102110	Input Magnetic Tape Buffer to A Register
INB 0210	102210	Input Magnetic Tape Buffer to B Register
CIA 0510	102510	Input Magnetic Tape Buffer to A Register Cleared
CIB 0610	102610	Input Magnetic Tape Buffer to B Register Cleared
C. Sense		
SEN 010	101010	Sense Tape Error
SEN 0110	101110	Sense Buffer Ready
SEN 0210	101210	Sense Tape Unit Ready
SEN 0310	101310	Sense File Mark
SEN 0410	101410	Sense Odd Length Record
SEN 0510	101510	Sense End of Tape
SEN 0610	101610	Sense Beginning of Tape
SEN 0710	101710	Sense Rewinding
D. Transport Select		
EXCB 0110	104110	Select Tape Drive No. 1
EXCB 0210	104210	Select Tape Drive No. 2
EXCB 0310	104310	Select Tape Drive No. 3
EXCB 0410	104410	Select Tape Drive No. 4

Table H-8
620/i-31 7-track Magnetic Tape System Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 010	100010	Read One Record Binary
EXC 0110	100110	Read One Record BCD
EXC 0210	100210	Write One Record Binary
EXC 0310	100310	Write One Record BCD
EXC 0410	100410	Write File Mark
EXC 0510	100510	Forward One Record
EXC 0610	100610	Backspace One Record
EXC 0710	100710	Rewind
B. Transfer		
OME 010	103010	Output Memory to Magnetic Tape Buffer
OAR 0110	103110	Output A Reg to Magnetic Tape Buffer
OBR 0210	103210	Output B Reg to Magnetic Tape Buffer
IME 010	102010	Input Magnetic Tape Buffer to Memory
INA 0110	102110	Input Magnetic Tape Buffer to A Register
INB 0210	102210	Input Magnetic Tape Buffer to B Register
CIA 0510	102510	Input Magnetic Tape Buffer to A Register Cleared
CIB 0610	102610	Input Magnetic Tape Buffer to B Register Cleared
C. Sense		
SEN 010	101010	Sense Tape Error
SEN 0110	101110	Sense Buffer Ready
SEN 0210	101210	Sense Tape Unit Ready
SEN 0310	101310	Sense File Mark
SEN 0410	101410	Sense Odd Length Record/Sense High Density
SEN 0510	101510	Sense End of Tape
SEN 0610	101610	Sense Beginning of Tape
SEN 0710	101710	Sense Rewinding
D. Transport Select		
EXCB 0110	104110	Select Tape Drive No. 1
EXCB 0210	104210	Select Tape Drive No. 2
EXCB 0310	104310	Select Tape Drive No. 3
EXCB 0410	104410	Select Tape Drive No. 4

Table H-9
620/i-40/41/42/43 Disc Memory System Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 014	100014	Initialize and select interlace mode
EXCB 014	104014	Initialize and select non-interlace mode
EXC 0114	100114	Select read mode
EXC 0214	100214	Select write mode
EXC 0414	100414	Select address mode zone 0 (first 65K)
EXC 0514	100514	Select address mode zone 1 (second 65K)
EXC 0614	100614	Select address mode zone 2 (third 65K)
EXC 0714	100714	Select address mode zone 3 (fourth 65K)
B. Transfer		
CIA 014	102514	Clear and input to A-register
CIB 014	102614	Clear and input to B-register
INA 014	102114	Input to A-register
INB 014	102214	Input to B-register
IME 014	102014	Input to memory
OME 014	103014	Output from memory
OAR 014	103114	Output from A-register
OBR 014	103214	Output from B-register
C. Sense		
SEN 014	101014	Sense parity error
SEN 0114	101114	Sense buffer ready
SEN 0214	101214	Sense disc ready
SEN 0414	101414	Sense disc register ready

Table H-10
620/i-52 Paper Tape System Controller Instructions

Mnemonic	Octal Code	E-Bus Signal	Functional Description
A. External Control			
EXC 037	100037	004037	Connect Punch to BIC
EXC 0437	100437	004437	Stop Reader
EXC 0537	100537	004537	Start Reader
EXC 0637	100637	004637	Punch Buffer
EXC 0737	100737	004737	Read One Character
B. Transfer			
OAR 037	103137	040137	Load buffer from A register
OBR 037	103237	040237	Load buffer from B register
OME 037	103037	040037	Load buffer from Memory
INA 037	102137	020137	Read buffer into A register
INB 037	102237	020237	Read buffer into B register
IME 037	102037	020037	Read buffer into memory
CIA 037	102537	020537	Read buffer into cleared A register
CIB 037	102637	020637	Read buffer into cleared B register
C. Sense			
SEN 0537	101537	010537	Sense buffer ready

Table H-11
620/i-65 Data Set Coupler (synchronous) Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 071	100071	Go to Search
EXC 0171	100171	Connect Write Buffer to BIC
EXC 0271	100271	Connect Read Buffer to BIC
EXC 0471	100471	Turn on Request to Send
EXC 0571	100571	Turn off Request to Send
EXC 0671	100671	Go to Character Format
B. Transfers		
IME 071	102071	Transfer Read Buffer to 8 LSB of Memory
INA 071	102171	Transfer Read Buffer to 8 LSB of A Reg.
INB 071	102271	Transfer Read Buffer to 8 LSB of B Reg.
CIA 071	102571	Transfer Read Buffer to 8 LSB of A Reg. cleared
CIB 071	102671	Transfer Read Buffer to 8 LSB of B Reg. cleared
OME 071	103071	Transfer Memory 8 LSB to Write Buffer
OAR 071	103171	Transfer A Register 8 LSB to Write Buffer
OBR 071	103271	Transfer B Register 8 LSB to Write Buffer
C. Sense		
SEN 0171	101171	Write Buffer Empty
SEN 0271	101271	Read Buffer Full
SEN 0371	101371	Carrier On
SEN 0471	101471	Clear to Send

Notes:

1. All commands listed are used for 201A3 Dataset operation.

2. EXC 571 is not necessary for 201B1 (true) full-duplex operation.

3. SEN 371 and SEN 471 will always be ON if Request to Send is left on at both ends when using 201B1. Carrier On also comes ON when outputting using a 201A3 dataset.

4. 201A3 = Half-Duplex - 2 wire. 201B1 = Full-Duplex - 4 wire.

Table H-12
620/i-66 Data Set Coupler Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0471	100471	Initialize
EXC 0271	100271	Select Load MCR
B. Transfers		
IME 071	102071	Transfer Read Buffer to Memory
INA 071	102171	Transfer Read Buffer to A Register
INB 071	102271	Transfer Read Buffer to B Register
CIA 071	102571	Transfer Read Buffer to A Register Cleared
CIB 071	102671	Transfer Read Buffer to B Register Cleared
OME 071	103071	Transfer Memory to Write or MCR Buffer
OAR 071	103171	Transfer A Register to Write or MCR Buffer
OBR 071	103271	Transfer B Register to Write or MCR Buffer Write or MCR
C. Sense		
SEN 0171	101171	Output Buffer Ready
SEN 0271	101271	Input Buffer Ready
SEN 0371	101371	Call Connect
SEN 0471	101471	Call Disconnect
SEN 0571	101571	Carrier On

Notes:

1. All commands listed are used for 103A2 Dataset operation.
2. Request to Send and Clear to Send could be substituted for SEN 371 and SEN 471 commands if desired.
3. 103A = Dialup; 103F = Private Line.
4. Device address listed is 71; any other device address may be used according to system requirements.

Table H-13
620/i-72 Digital Plotter Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 032	100032	BIC to DPC Enable
B. Transfer		
OME 032	103032	Transfer Memory to Buffer
OAR 032	103132	Transfer A Register to Buffer
OBR 032	103232	Transfer B Register to Buffer
C. Sense		
SEN 0132	101132	Sense Buffer Ready

Table H-14
620/i-80 Buffered I/O Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0X6Z*	100X6Z	Output control pulse on line selected by X from controller addressed by Z.
B. Sense		
SEN 0X6Z	101X6Z	Test state of line selected by X from controller addressed by Z.
C. Input Data		
IME 06Z	10206Z	Read input buffer of controller addressed by Z into memory.
INA 016Z	10216Z	Read input buffer of controller addressed by Z into B register.
INB 026Z	10226Z	Read input buffer of controller addressed by Z into B register.
CIA 056Z	10256Z	Clear A register and read controller input buffer addressed by Z.
CIB 066Z	10266Z	Clear B register and read controller input buffer addressed by Z.
D. Output Data		
ØME 06Z	10306Z	Load output buffer of controller addressed by Z from memory.
ØAR 016Z	10316Z	Load output buffer of controller addressed by Z from A register.
ØBR 026Z	10326Z	Load output buffer of controller addressed by Z from B register.

*6Z = Device address (60-67). Determined on individual system basis by wiring on backplane of peripheral expansion chassis.

*X = Discrete control/sense line (0-7).

Table H-15
620/i-81 Digital I/O Controller Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC	100XZZ*	Select device address of ZZ and initiate a control pulse on line X.
B. Sense		
SEN	101XZZ	Select device address of ZZ and test logical state of sense response line X.

*ZZ = Device address 60_8 to 67_8

* X = Control or sense line 0 through 7

Table H-16
620/i-83 Relay Contact I/O Module Instructions

Mnemonic	Octal Code	Functional Description
A. External Control		
EXC 0DA	1000DA	Clear All Outputs. Causes all 16 output contacts to open.
EXC 1DA	1001DA	Clear All Inputs. Returns all input bits that are not being set by contact closure to zero.
B. Sense		
SEN 0DA	1010DA	Sense Contact Closed. This command is available as an option. A specified contact closure will cause a jump to the jump address to occur.

620/i-83 Relay Contact I/O Module Instructions (Contd)

Mnemonic	Octal Code	Functional Description
C. Transfer In		
INA 0DA	1020DA	Input to A register. Input relay buffered input data on module to A register.
CIA 0DA	1020DA	Clear and Input to A register. Input relay buffered input data on module to A register cleared.
INB 0DA	1020DA	Input to B register. Input relay buffered input data on module to B register.
CIB 0DA	1020DA	Clear and Input to B register. Input relay buffered input data on module to B register cleared.
IME 0DA, ADDR	1020DA	Input to Memory. Input relay buffered input data on module to memory.
D. Transfer Out		
OAR 0DA	1030DA	Output from A Register. Output A register to the buffered relay output contacts.
OBR 0DA	1030DA	Output from B Register. Output B register to buffered relay contact outputs.
OME 0DA, ADDR	1030DA	Output from Memory. Output memory to buffered relay contact outputs.

Table H-17
620/i-85 Analog Input System Instructions

Mnemonic	Octal Code	Description
EXC 054 EXC 0154	100 054 100 154	Initializes the AIS system. The Program Control Mode.
EXC 0254	100 254	Places the AIS in the Scan Mode.
EXC 0354	100 354	Start conversion command for the first conversions in the SCAN mode.
SEN 054	101054	This SEN indicates the conversion data is ready. The data must be taken within 40 microseconds of the start of the SEN or the data will be replaced by new conversion data if operating at maximum throughput.
SEN 0154	101 154	This SEN indicates the AIS is requesting a new multiplexer address.
SEN 0254	101 254	This SEN indicates the AIS has completed the multiplexer address SCAN.
DTO INSTRUCTION OAR, OBR, OME		Data Transfer Out - In the program mode the DTO occurs for each multiplexing address given to the AIS. In the SCAN Mode, a DTO occurs for the first (preset) address.
DTI INSTRUCTIONS CIA 054 CIB 054 INA 054 INB 054 IME 054		Data Transfers "In" - After each conversion the data for that conversion is ready and a DTI Transfers it into the 620 i. If the throughput rate is 20,000. The DTI must occur within 40 microseconds of the data ready signal.

Appendix I
Standard Character Codes

Appendix I
DATA 620/i Standard BCD Codes

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
@	300	00	32	0-2-8	77
A	301	01	61	12-1	13
B	302	02	62	12-2	14
C	303	03	63	12-3	15
D	304	04	64	12-4	16
E	305	05	65	12-5	17
F	306	06	66	12-6	20
G	307	07	67	12-7	21
H	310	10	70	12-8	22
I	311	11	71	12-9	23
J	312	12	41	11-1	24
K	313	13	42	11-2	25
L	314	14	43	11-3	26
M	315	15	44	11-4	27
N	316	16	45	11-5	30
O	317	17	46	11-6	31
P	320	20	47	11-7	32
Q	321	21	50	11-8	33
R	322	22	51	11-9	34
S	323	23	22	0-2	35
T	324	24	23	0-3	36
U	325	25	24	0-4	37
V	326	26	25	0-5	40
W	327	27	26	0-6	41

DATA 620/i Standard BCD Codes (continued)

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
X	330	30	27	0-7	42
Y	331	31	30	0-8	43
Z	332	32	31	0-9	44
[	333	33	75	12-5-8	76*
\	334	34	36	0-6-8	76*
]	335	35	55	11-5-8	76*
↑	336	36	17 (Note)	7-8	76*
←	337	37	20	2-8	76[1]
blank	240	40	20	No Punch	00
!	241	41	52	11-2-8	51
"	242	42	35	0-5-8	62
#	243	43	37	0-7-8	63
$	244	44	53	11-3-8	60
%	245	45	57	11-7-8	64
&	246	46	77	12-7-8	65
'	247	47	14	4-8	66
(	250	50	34	0-4-8	52
)	251	51	74	12-4-8	53
*	252	52	54	11-4-8	47
+	253	53	60	12	45
,	254	54	33	0-3-8	54
-	255	55	40	11	46
.	256	56	73	12-3-8	51
/	257	57	21	0-1	50

DATA 620/i Standard BCD Codes (continued)

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
0	260	60	12	0	01
1	261	61	01	1	02
2	262	62	02	2	03
3	263	63	03	3	04
4	264	64	04	4	05
5	265	65	05	5	06
6	266	66	06	6	07
7	267	67	07	7	10
8	270	70	10	8	11
9	271	71	11	9	12
:	272	72	15	5-8	67
;	273	73	56	11-6-8	70
<	274	74	76	12-6-8	76*
=	275	75	13	3-8	55
>	276	76	16	6-8	76[2]
?	277	77	72	12-2-8	76

Note: End-of-file for mag tape.
*: Undefined character.
1: Form control: Return to col 1.
2: Tab control: Skip to col 7.

} FORTRAN System only

Teletype Character Codes

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
0	260	Y	331
1	261	Z	332
2	262	blank	240
3	263	!	241
4	264	'	242
5	265	#	243
6	266	$	244
7	267	%	245
8	270	&	246
9	271	'	247
A	301	(	250
B	302	)	251
C	303	*	252
D	304	+	253
E	305	,	254
F	306	–	255
G	307	.	256
H	310	/	257
I	311	:	272
J	312	;	273
K	313		274
L	314	=	275
M	315		276
N	316	?	277
O	317	@	300
P	320		333
Q	321		334
R	322		335
S	323		336
T	324		337
U	325	Rub Out	377
V	326	NUL	200
W	327	SOM	201
X	330	EOA	202

Teletype Character Codes (continued)

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
EOM	203	X-OFF	223
EOT	204	TAPE OFF	
WRU	205	AUX	224
RU	206	ERROR	225
BEL	207	SYNC	226
FE	210	LEM	227
H TAB	211	SO	230
LINE FEED	212	S1	231
V TAB	213	S2	232
FORM	214	S3	233
RETURN	215	S4	234
SO	216	S5	235
SI	217	S6	236
DCO	220	S7	237
X-ON	221		
TAPE AUX ON	222		

Appendix J

Summary of Test Identifiers and Parameters

APPENDIX J

Summary of Test Identifiers and Parameters

Diagnostic Test	Test Identifier	Param 1	Param 2	Param 3
A. Driver				
1. Terminate preventative mode	HALT			
2. Load another test	RUN	X7600		
B. Memory Test				
1. Memory address verification	MADR	Block addr		
2. Memory pattern	MPAT	Block addr	Select bits	
3. Sequence of above for all of core memory	MEMO			
C. Instructions Test				
1. Register change	IREG			
2. Load/store	ILOD			
3. Logical	ILOG			
4. Overflow	IOVF			
5. Jump/execute	IJMX			
6. Logical and arithmetic shifts	ISHF			
7. Standard arithmetic	IARS			
8. Optional arithmetic	IARO			
9. Extended addressing	IEXA			
10. Byte	IBYT			
11. Auto indexing	IAUT			
12. Sequence of the above	INST			
D. Model 33/35B Teletype Test ASR and KSR Models				
1. Page printer accuracy	PPAC			
2. Keyboard accuracy	KBAC			
ASR Models				
3. Print suppress	PTSP			
4. Reader control	RDCT			
5. Punch control	PCTL			
6. Reader/punch accuracy	RPCA			
E. Model 33A Teletype Tests				
1. Read paper tape (high speed read)	TRH	Min code	Max code	No. codes
(low speed read)	TRL	Min code	Max code	No. codes
2. Read keyboard	TRK	Min code	Max code	No. codes
3. Punch/print	TP	Min code	Max code	No. codes
4. Read PT/punch/print (high speed read)	TRHP	Min code	Max code	No. codes

Diagnostic	Test Identifier	Param 1	Param 2	Param 3
E. Model 33A Teletype Tests (Continued)				
5. Read kyb/punch/print	TRKP	Min code	Max code	No. codes
6. Print read error counts	TPRN			
7. Teletype transfer instruc. (keyboard input)	TIRK			
8. Teletype transfer instruc. (paper tape input)	TIRL			
F. Paper Tape System Test Routine				
1. Read paper tape test				
(high speed)	PRH	Min code	Max code	No. codes
(step)	PRS	Min code	Max code	No. codes
2. Punch paper tape test	PP	Min code	Max code	No. codes
G. Line Printer Test Routine				
1. Diagonal format test	LPRD			
2. Line/slew test	LPRL			
3. Diagonal and line/slew	LPRB			
4. Character test	LPRS	Char code		
H. Card Reader Test Routine				
1. Read a card	RDAC			
I. disc Memory Test Routine				
1. disc pattern test	DPAT	Init addr	Final addr	Pattern & sector
2. Full disc test	DISC	disc size		

Appendix K
Maintain Memory Map

APPENDIX K

Maintain Memory Map

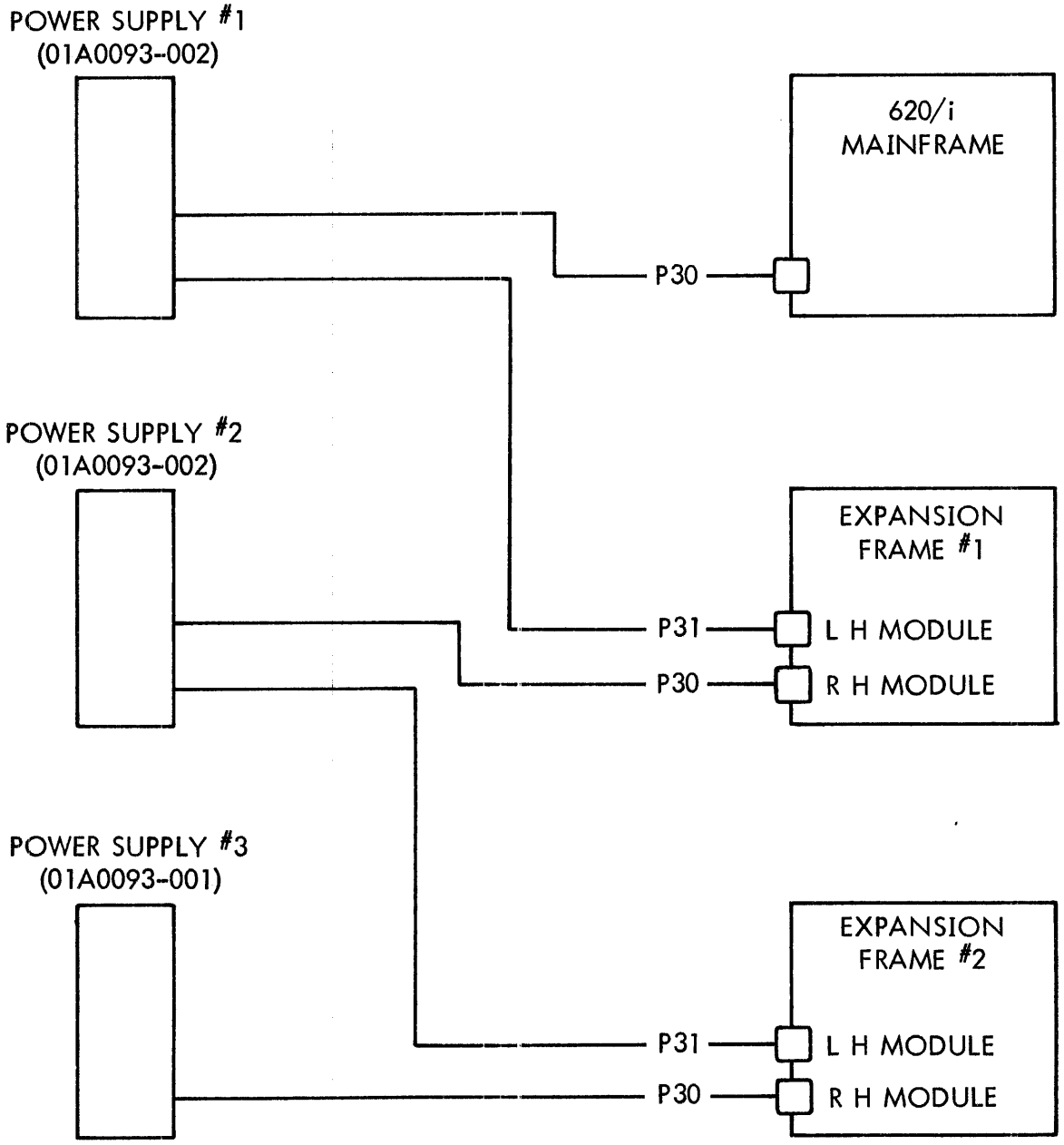
Test	Octal Addresses		
	First	Last	Execution
Driver	6000	6700	6000
Memory	4000	4657	6000
Instruction	1500	4457	6000
Model 33A Teletype	2000	3140	6000
Model 33/35B Teletype	2000	3554	6000
Paper Tape	2000	2470	6000
Line Printer	2000	2425	6000
Card Reader	2000	2212	6000
Disc Memory	2000	3360	6000

Appendix L

620/i Power Supply Information and Schematics

The contents of this appendix are listed as follows:

The following diagram illustrates dc power connections for a 620/i mainframe plus two expansion frames. The power supplies are shown with assembly numbers in parenthesis. The -001 and -002 digits designate units with one and two power cables, respectively. The first power supply provides power to the 620/i mainframe and the left-hand module of expansion frame #1. The second power supply provides power to the right-hand module of expansion frame #1 and the left-hand module of expansion frame #2. The third power supply provides power to the right-hand module of expansion frame #2.



DC Power Connections Diagram

The following wiring diagrams show how dc power is applied to the 620/i mainframe and expansion frames.

Wiring diagram A illustrates a power supply connected to a 620/i mainframe with no expansion frames. The AC control relay K1 is used to apply 115 VAC to the ±5 volt and ±12 volts power supply circuits only when both power ON-OFF switches, S12 and S1, are turned on. The high side (black) of the 115 VAC input is applied to one side of the coil of K1 via S12, J30-11, S1, and J30-4. The low side (white) of the 115 VAC input is applied to the other side of the coil of K1 via S12, J30-3, and J30-7. With 115 VAC across the coil of relay K1, the relay is energized which routes the 115 VAC input to the ±5 volt and ±12 volt power supply circuits.

Wiring diagram B illustrates three power supplies connected to provide dc power for a 620/i mainframe plus two expansion frames. The first two power supplies each contain two identical power cables (P30 and P31) while the third power supply contains one power cable (P30). The AC control relay K1 in the first power supply is energized in the same manner as in diagram A. However, the relay is connected in parallel with the control relays in the remaining power supplies; thus the dc power applied to the expansion frames is controlled by the power ON-OFF switch S1 located on the mainframe power console.

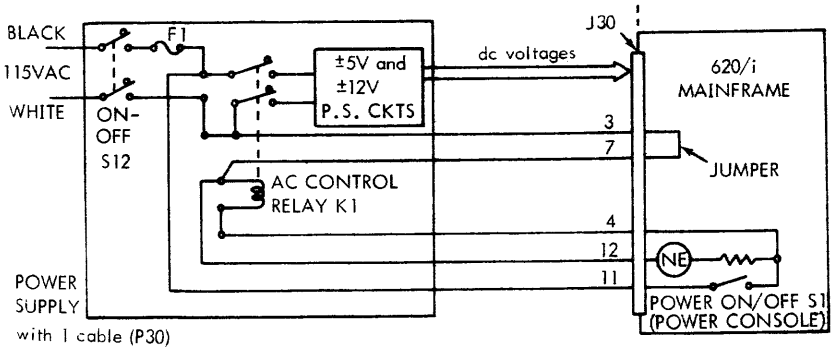


Diagram A. Mainframe Connections.

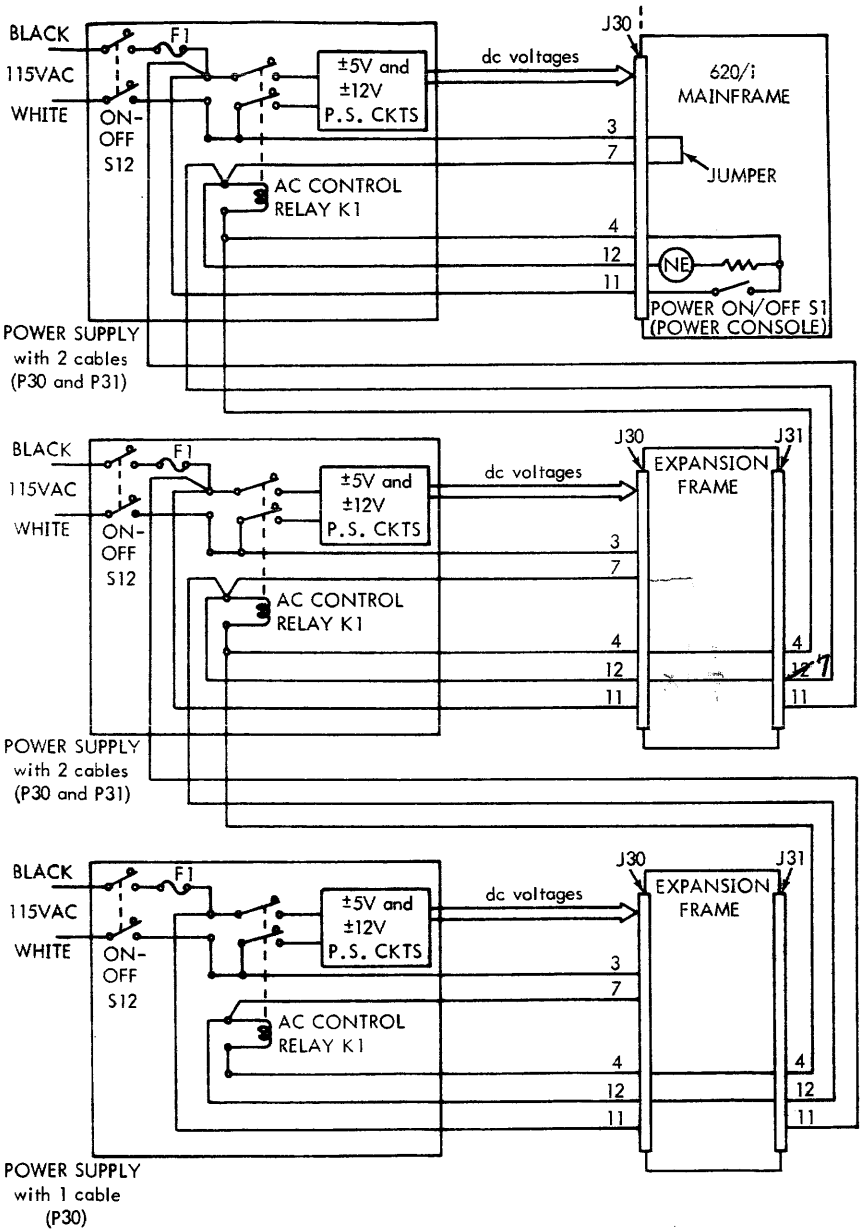


Diagram B. Mainframe Plus Two Expansion Frames Connections.

620/i POWER SUPPLY WIRING DIAGRAMS

Ambient Temperature Range (free air, no forced air cooling)	0° C to 55° C
Adjustable Voltage Range	-0%, +10%
DC Isolation	100 megohms minimum from primary to all other windings and chassis.
Ripple	0.05% maximum P-P
Transient Response	50 μsec maximum for 50% change in load
Input Line Frequency	47 to 440 cps single phase
Input Line Voltage	105 to 123 VAC or 210 to 250 VAC
Line Regulation +12 VDC and -12 VDC	10 mv maximum for 105 to 125 VAC line change at one-half of full load
Line Regulation +5 VDC and -5 VDC	10 mv maximum for 105 to 125 VAC line change at one-half of full load
Load Regulation +5 and -5 VDC	35 mv maximum for full load change at 115 VAC input
Load Regulation +12 and -12 VDC	40 mv maximum for full load change at 115 VAC input
Relay Turn On/Off Transient at Output Terminals	250 V peak maximum

The relay coil shall be isolated and brought out to terminals on the I/O terminal strip.

Total Regulation	Regulation includes the combined effects of ripple, transient loads, DC loading from 0 to 100%, line voltage and frequency change, temperature, long term stability over 8 hours and all other sources.
+5 and -5 VDC	±4% maximum
+12 and -12 VDC	±2% maximum
Package Dissipation	330 watts maximum
Overload Protection	Electronic current limit with automatic recovery.
Over-voltage Limit (including overshoot) (+5 supply only)	6 VDC minimum, 6.5 VDC maximum

Foldback Current

Supply	Current Range
+5	9 to 12A
-5	2.5 to 3.5A
+12	7 to 9A
-12	5 to 7A

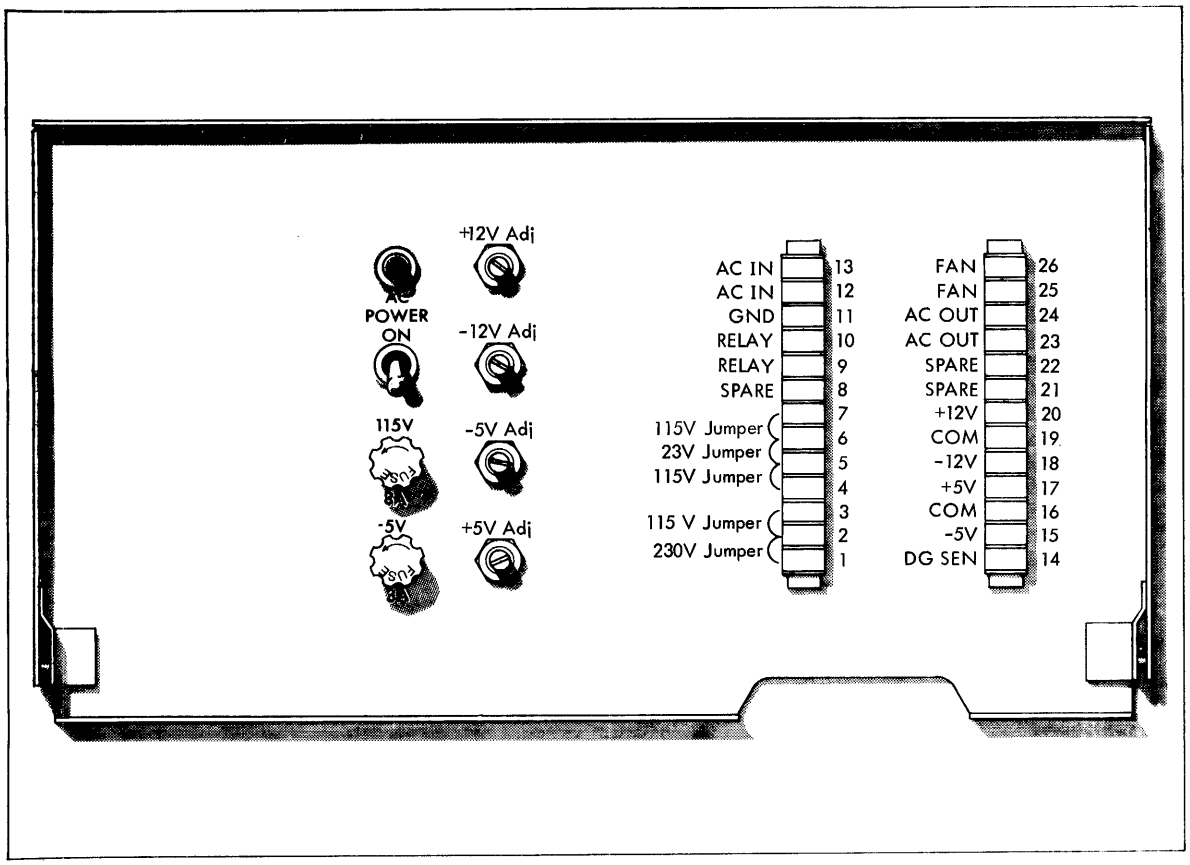
Short Circuit Current

Supply	Short Circuit Current
+5	Greater than 2.5A
-5	Greater than 0.5A
+12	Greater than 1.5A
-12	Greater than 1.0A

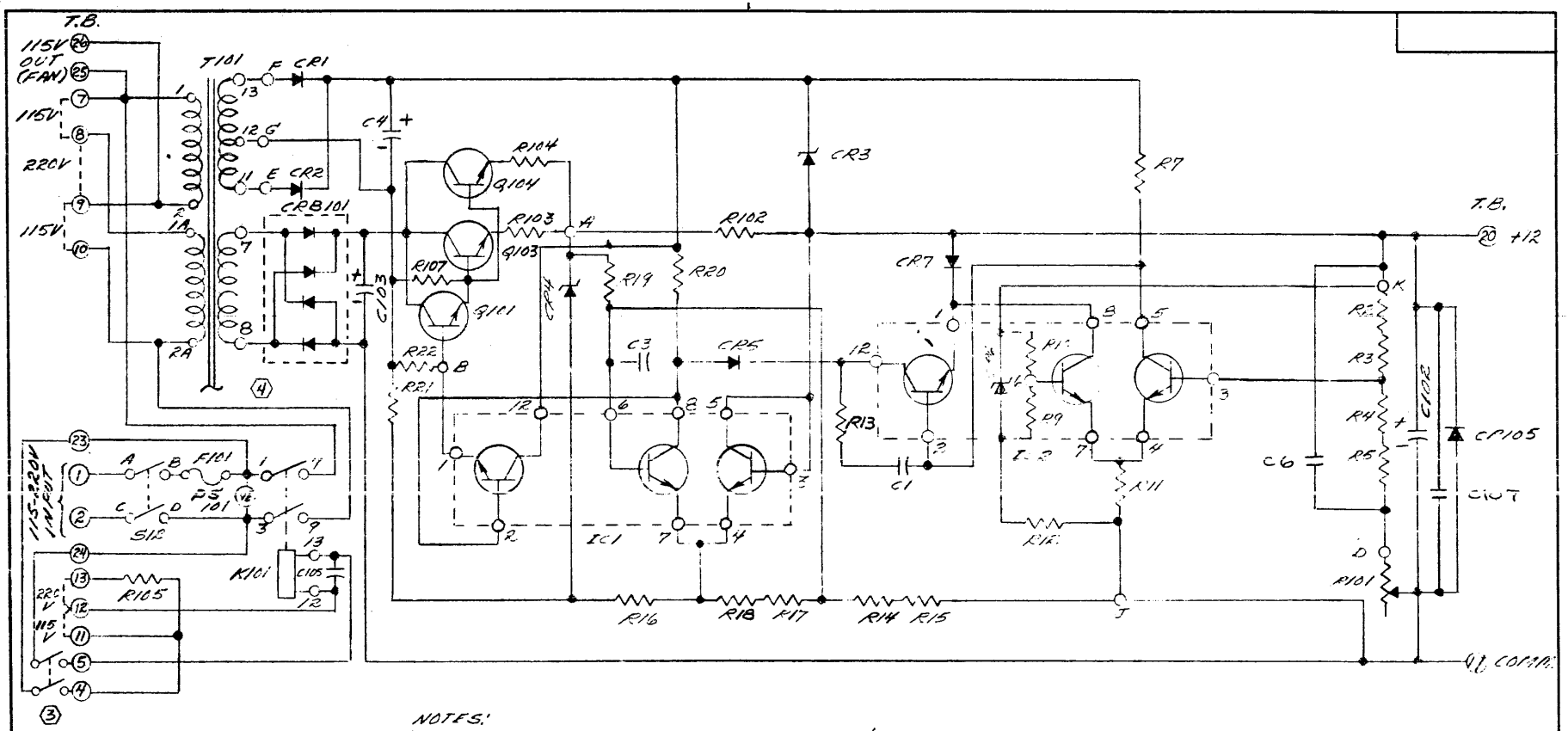
The short circuit current shall in all cases be less than the full load current.

Data Gurad Sense Voltage

15.5V ± 5%; measured open circuit at 105 VAC input line voltage. The source will have a 1500 OHM series resistor and shall be capable of driving a minimum external load of 1800 OHMS.



620/i Integrated Power Supply (Front View)



NOTES:

1. FOR 115 V INPUT, JUMPER 7-8, 9-10 & 11-12 ----
2. FOR 220 V INPUT, JUMPER 8-9 & 12-13 - - -
   REMOVE 115 V JUMPERS
3. SWITCH SHOWN TO BE SUPPLIED BY VENDOR
4. FOR ADDIONAL WINDING SEE SHT 2, 3, 4
5. INTEGRATED POWER SUPPLY IS INSTALLED ON ALL 620/i COMPUTERS HAVING SERIAL NUMBERS LATER THAN 5757

NO.	REASON	DATE	APPV
	REVISIONS		

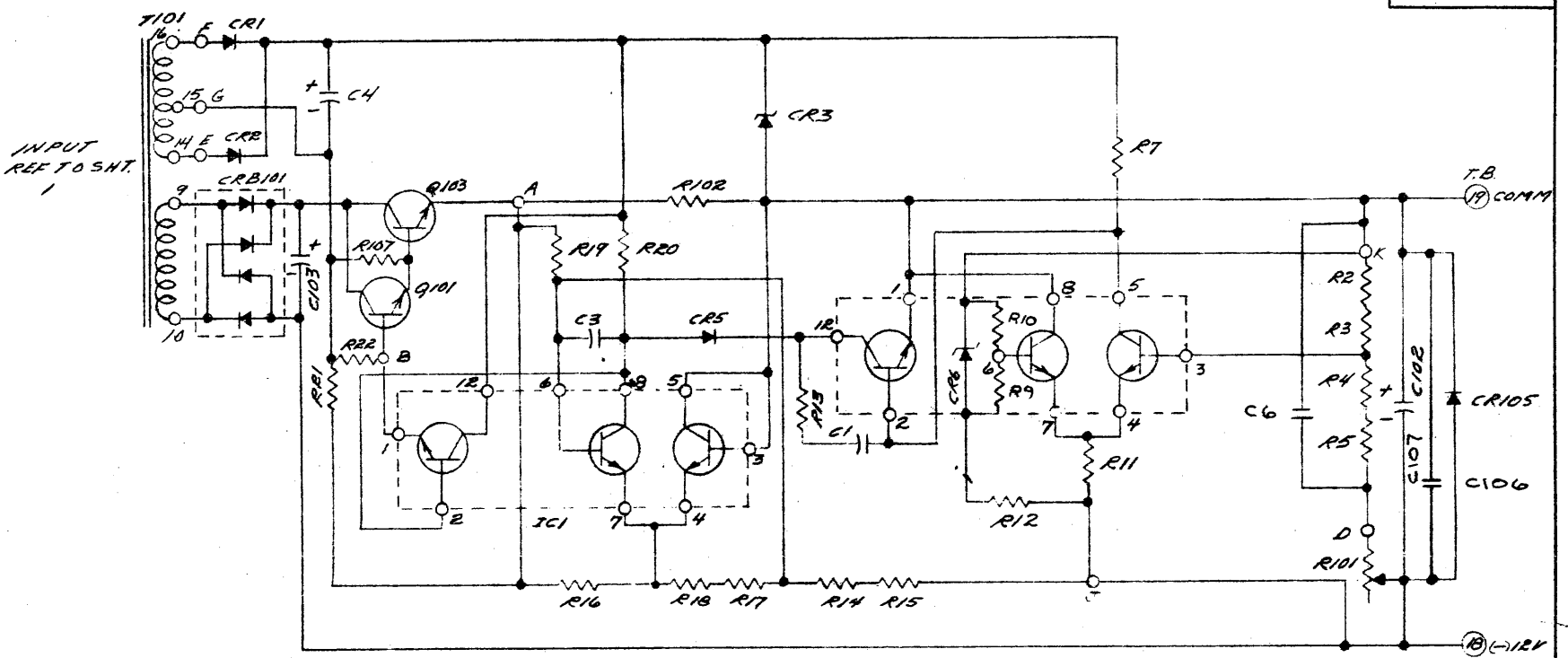
ENGR.	DRAWN BY	APPR.		SCALE
McGREW	DOUGHAR	[redacted]	SHT 1 OF 4	N.A.

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

[redacted]

TITLE: INTEGRATED 620/i POWER SUPPLY (+12V DC) SCHEMATIC

DWG. NO. 1094-7



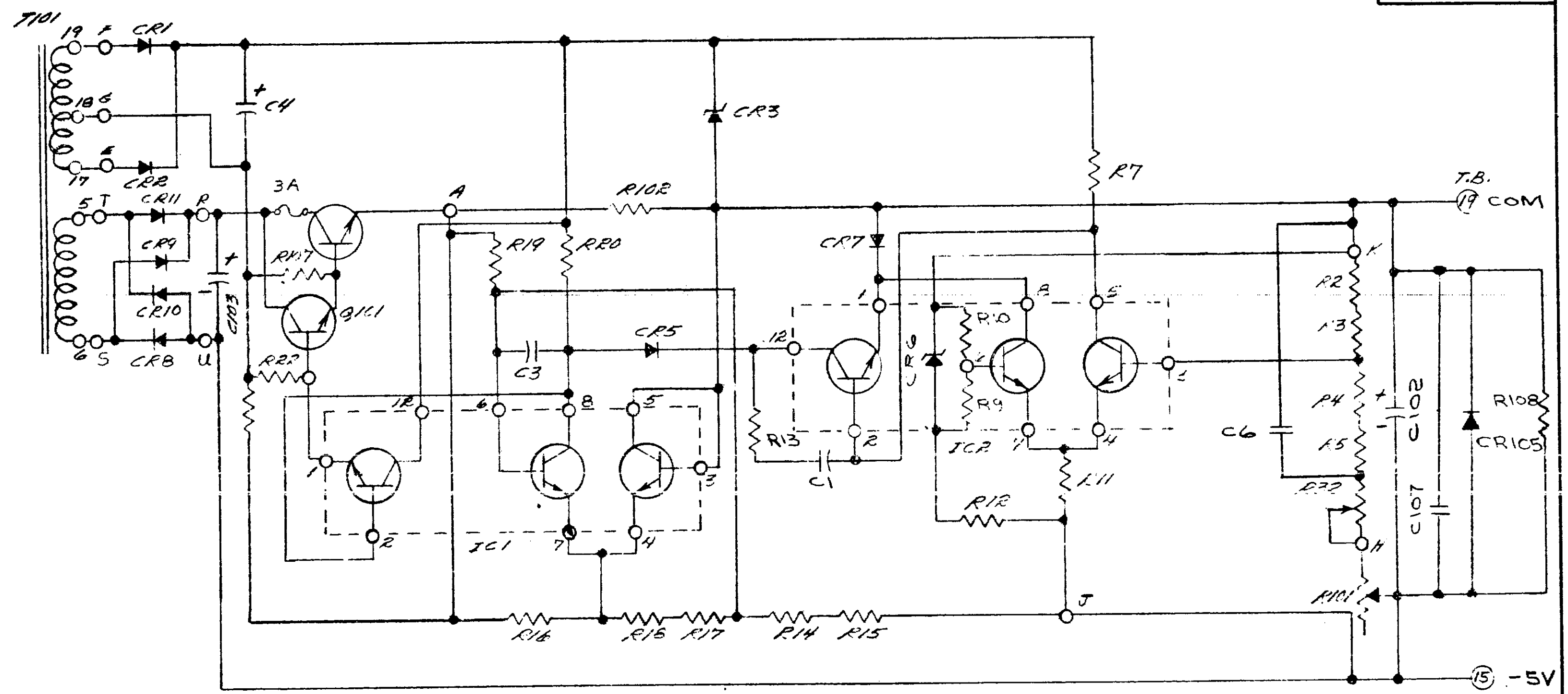
NO.	REASON	DATE	APPV
	REVISIONS		

ENGR.	DRAWN BY	APPR.	SHT.	SCALE
MGIFFEN	DOUGLAS		SHT. 2 OF 4	N/A

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

TITLE
INTEGRATED 620/i
POWER SUPPLY
(-12VDC) SCHEMATIC

DWG. NO.
1094-8



ENGR.	DRAWN BY	APPR.		SCALE
			SHT 3 OF 4	

NO.	REASON	DATE	APPV.

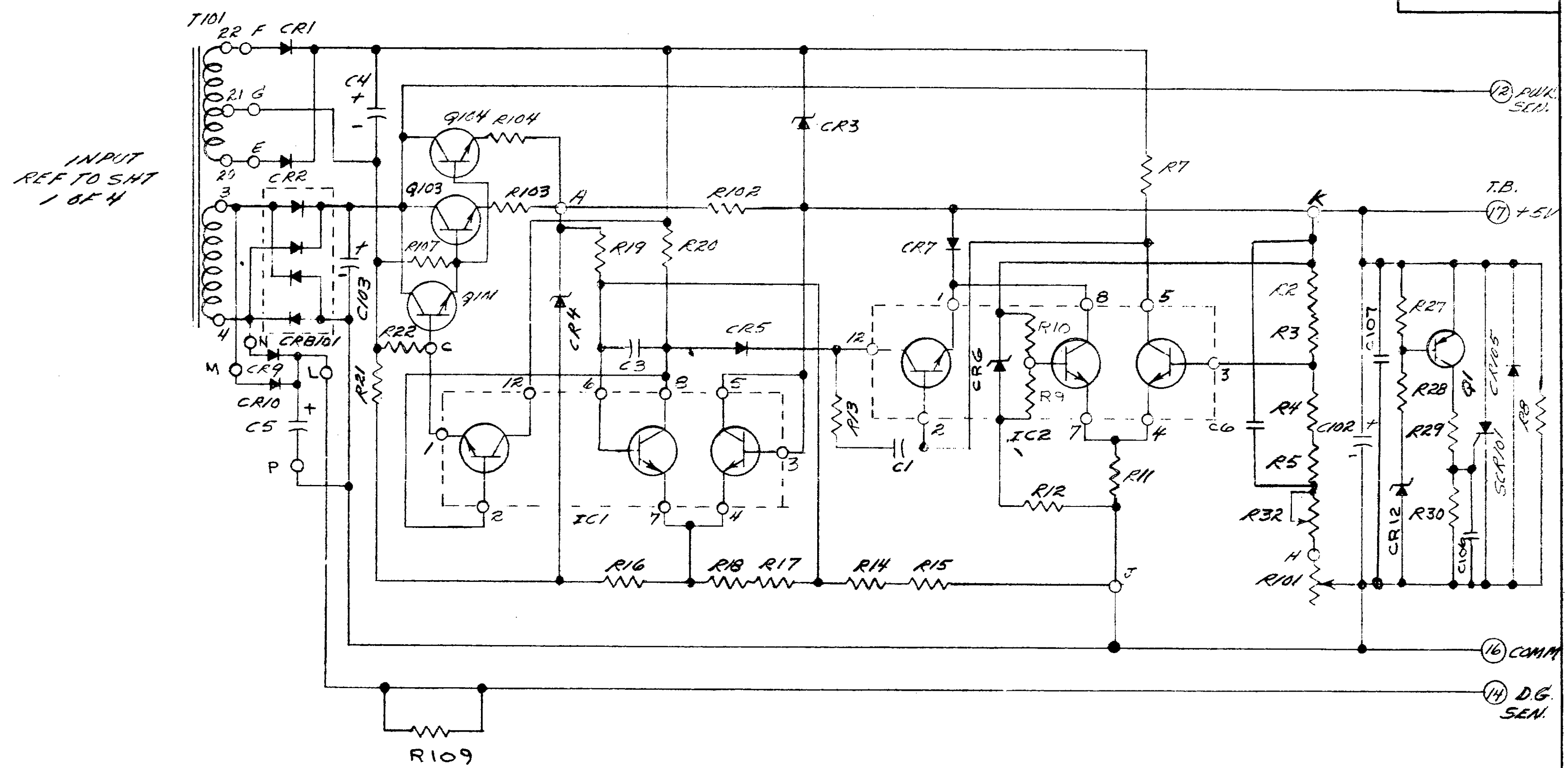
REVISIONS

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
1165 W. 135 STREET
GARDENA, CALIF. 90247

TITLE
INTEGRATED 620/i POWER SUPPLY (-5V DC) SCHEMATIC

DWG. NO. 1094-8



NO.	REASON	DATE	APPV.

REVISIONS

ENGR.	DRAWN BY	APPR.		SCALE
McGREW	[signature]	[signature]	SHT 4 OF 4	N.A.

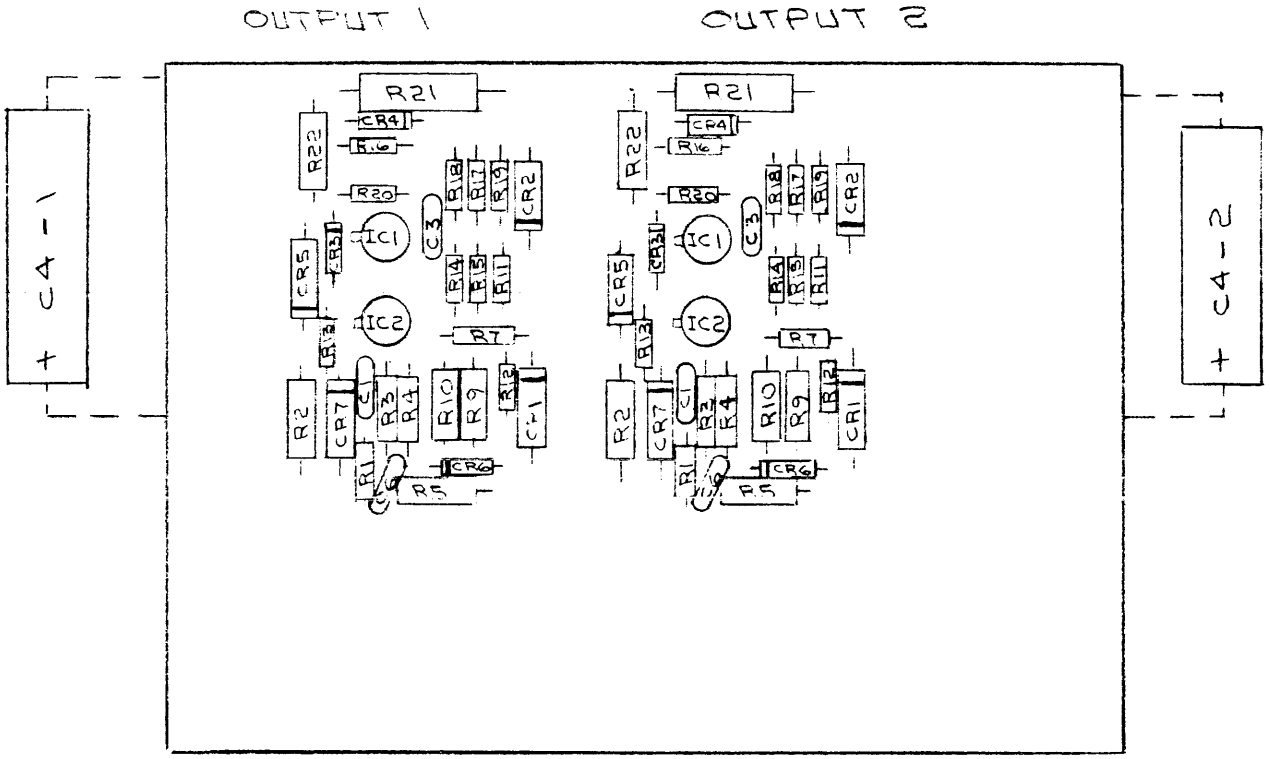
TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
1265 W. 135 STREET
GARDENA, CALIF. 90247

TITLE
INTEGRATED 620/i POWER SUPPLY (+5VDC) SCHEMATIC

DWG. NO. 1094-8

1096-7



NO.	REASON	DATE	APPV.
	REVISIONS		

ENGR.	DRAWN BY	APPR.	NEXT ASSY.	SCALE
Mc GREW	HYATT	RLD	SHT 1 OF 2	

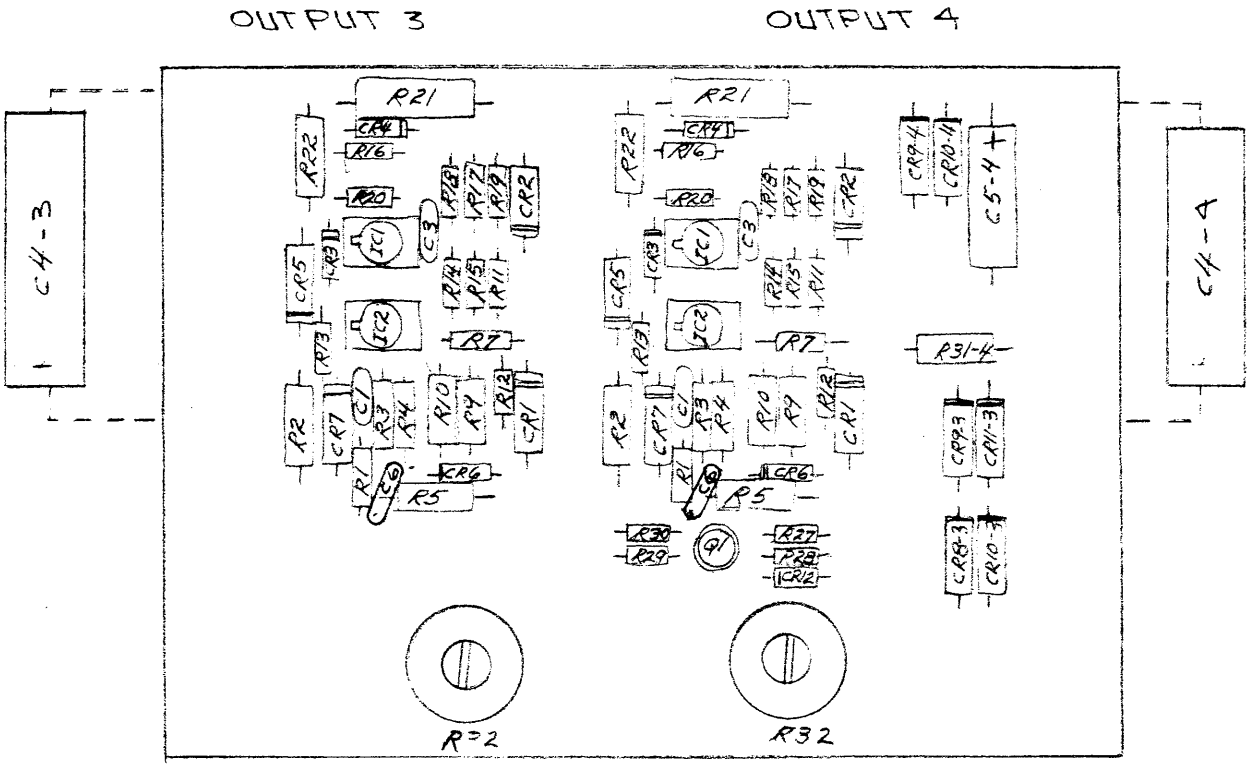
TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
1265 W. 135 STREET
GARDENA, CALIF. 90247

TITLE
P.C. BOARD
PARTS LAYOUT
INTEGRATED P.S.

DWG. NO.
1096-7

1096-7



NO.	REASON	DATE	APPV.
	REVISIONS		

ENGR.	DRAWN BY	APPR.	NEXT ASSY.	SCALE
			SHT 2 OF 2	1:1

TOLERANCES
EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

TITLE
PC BOARD
PARTS LAYOUT
INTEGRATED P.S.

DWG. NO.
1096-7

MASTER BILL OF MATERIAL FOR 85S1003-000

MODULAR DEVICES INC. OUTPUT 1

+12V 6A

SHEET 1 OF 4 REV

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	Not Used		
R2	470 ohms 2W WW	IRC	BWH
R3	100 ohms ½W 10%		
R4	100 ohms ½W 10%		
R5	Not Used		
R6	Not Used		
R7	10K ½W 10%		
R8	Not Used		
R9	330 ohms ½W 10%		
R10	Not Used		
R11	4.7K ½W 10%		
R12	2.2K ½W 10%		
R14 *	8.2K " "		
R15	100 ohms " "		
R16	4.7K " "		
R17 *	330 ohms " "		
R18*	1K " "		
R19	470 ohms " "		
R20	10K " "		
R21	1.5K 2W "		
R22	15K ½W "		
R23	220 ohms 2W WW	IRC	BWH
R24	Not Used		
R25	Not Used		
R26	Not Used		
R101	500 ohms POT WW	Clarostat	43C2
R102	0.1 ohms 7W "	IRC	PW7
R103	0.1 ohms 5W WW	IRC	PW5
R104	" " " "	"	"
R105	5K 8W WW	Ohmite	1545
R107	6.8K 1W 10%		
C1	.001 MFD 20V	Cen.Lab.	DD102
C2	Not Used		
C3	.01 MFD 50VDC	Cen.Lab.	CK103
C4	100 MFD 50VDC	C-D	BR100-50
C6*	.01 MFD 50 VDC	Cen.Lab.	CK103

Notes & Part No	Part Name & Description	MFG	MFG Part No
C102	1000 MFD 15VDC	C-D	BR1000-15
C103	14000 MFD 30VDC	STM	
C105	0.22 MFD 200VDC	Sprague	192P
C107	.05 MFD 20VDC	Cen.Lab.	UK20-50
CR1,CR2	D9906		
CR3,CR4	IN752A Zener		
CR5	D9906		
CR6	IN752A Zener		
CR7	D9906		
CR8	Rect. Bridge	Sem-Tech	SCBA-05
CR105	368	Weatha	
IC1	CA3018		
IC2	CA3018		
Q101	2N3055		
Q103	2N3055		
Q104	2N3055		
*	Selected Value		
S12	Power Switch		
DS1	Dialight		249-784[illegible] -1431-57[illegible]
F1	Fuse holder+	Little Fuse	342004
F2	Fuse holder+	"	342004
K1	Relay	Guardian	IR-1220
			2C-115A
T101	Power Transformer	Mod.Dev.	PT270

MASTER BILL OF MATERIAL FOR 83S1003-000

MODULAR DEVICES, INC. OUTPUT 2

-12V 4A

SHEET 2 OF 4 REV

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	Not Used		
R2	470 ohms 2W WW	IRC	BWH
R3	100 ohms ½W 10%		
R4	" " " "		
R5	Not Used		
R6	Not Used		
R7	10K ¼W 10%		
R8			
R9	330 ohms ¼W 10%		
R10	Not Used		
R11	4.7K ¼W 10%		
R12	2.2K ½W 10%		
R13	10K ¼W 10%		
R14 *	8.2K ¼W 10%		
R15 *	2.2K " "		
R16	4.7K " "		
R17 *	1K " "		
R18 *	680 ohms " "		
R19	470 ohms " "		
R20	10K " "		
R21	1.5L 2W WW		
R22	15K ½W 10%		
R23	220 ohms 2W WW	IRC	BWH
R101	500 ohms POT WW	Clarostat	43C2
R102	0.1 ohms 5W WW	IRC	PW5
R107	6.8K 1W 10%		
C1	.001 MFD 1000VDC	Cen. Lab	DD102
C2	Not Used		
C3	.01 MFD	Cen. Lab	CK103
C4	100 MFD 50 VDC	C-D	BR100-50
C6 *	.01 MFD 50 VDC	Cen.Lab.	CK103
C102	1000 MFD 15 VDC	C-D	BR1000-15
C103	7900 MFD 25 VDC	STM	

Notes & Part No	Part Name & Description	MFG	MFG Part No
CR1	D9906		
CR2	D9906		
CR3	IN752A Zener		
CR4	IN752A		
CR5	D9906		
CR6	IN752A Zener		
CR7	D9906		
CRB	RECT. BRIDGE	Sem-Tech	SCBA-05
C105	568A		
C107	.05 MFD 20 VDC	Cen.Lab.	UK20-503
Q101	2N3055		
Q103	2N3055		
IC1	CA3018		
IC2	CA3018		
*	Selected Value		

MASTER BILL OF MATERIAL FOR 83S1003-000
MODULAR DEVICES, INC. OUTPUT 3
-5VDC 2A

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	Not Used		
R2	680 ohms 2W WW	IRC	IRC
R3	10 ohms ½W 10%		
R4	" " " "		
R5	Not Used		
R6	Not Used		
R7	10K ½W 10%		
R8	Not Used		
R9	2.2K ½W MF	Corning	RL20S-C5
R10	" " "	"	"
R11	1K ½W 10%		
R12	100 ohms ½W 10%		
R13	2.2K " "		
R14 *	4.7K " "		
R15 *	8.2K " "		
R16	4.7K " "		
R17 *	1.2K " "		
R18 *	1.5K " "		
R19	680 ohms " "		
R20	10K " "		
R21	1.5K 2W "		
R22	15K ½W "		
R23	470 ohms 2W WW	IRC	BWH
R24	Not Used		
R25	Not Used		
R26	Not Used		
R32	200 ohms POT	Clarostat	U-39
R101-1	500 ohms WW POT	Clarostat	43C2
R102	0.2 ohms 5W WW	IRC	PW-5
R107	6.8K 1W 10%		
R108	33 ohms 2W 10%		
C1	.001 MFD 1000 VDC	Central	ab DD102
C2 *	Not Used		
C3	.01 MFD 50VDC	Central	ab CK103
C4	100 MFD 50VDC	C-D	BR100-50
C6 *	.01 MFD 50 VDC	Cen.Lab.	CK103

Notes & Part No	Part Name & Description	MFG	MFG Part No
C102	1000MFD 15VDC	C-D	BR1000-15
C103	13000MFD 15VDC	STM	
CR1,CR2	D9906		
CR3,CR4	IN752A ZENER		
CR5	D9906		
CR6	IN749A ZENER		
CR7	D9906		
CR8-CR9	D9906		
CR10	D9906		
CR11	D9906		
CR105	368A		
IC1	CA3018	RCA	
IC2	CA3018		
Q101	2N3055		
Q103	2N3055		
F2	Fuse 2A	Little	3AG
		Fuse	
*	Selected Value		
C107	.05 MFD 20VDC	Can.Lab.	UK20-503

MASTER BILL OF MATERIAL FOR 83S1003-000

MODULAR DEVICES, INC. OUTPUT 4

+5VDC 8A

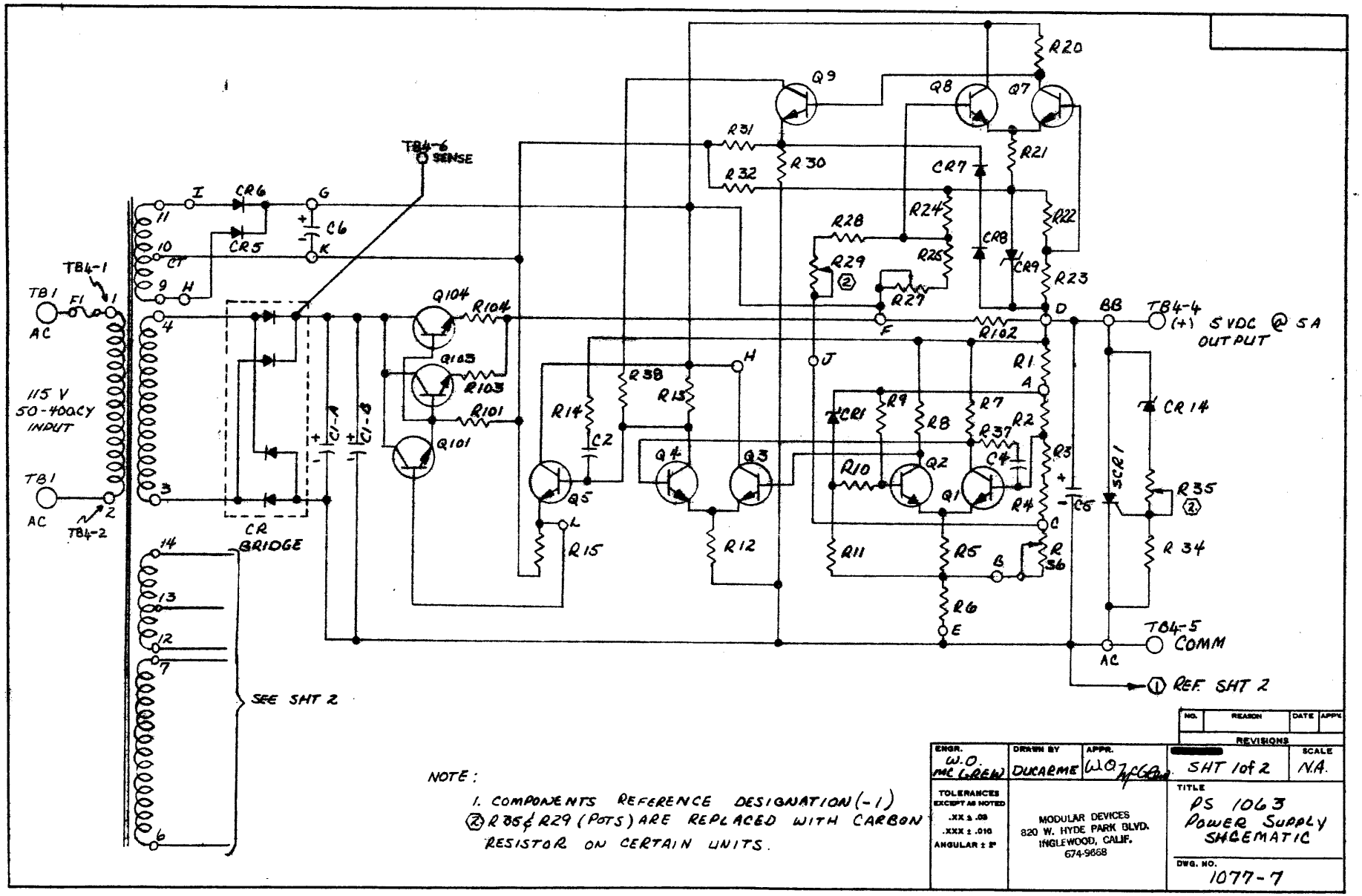
SHEET 4 OF 4 REV

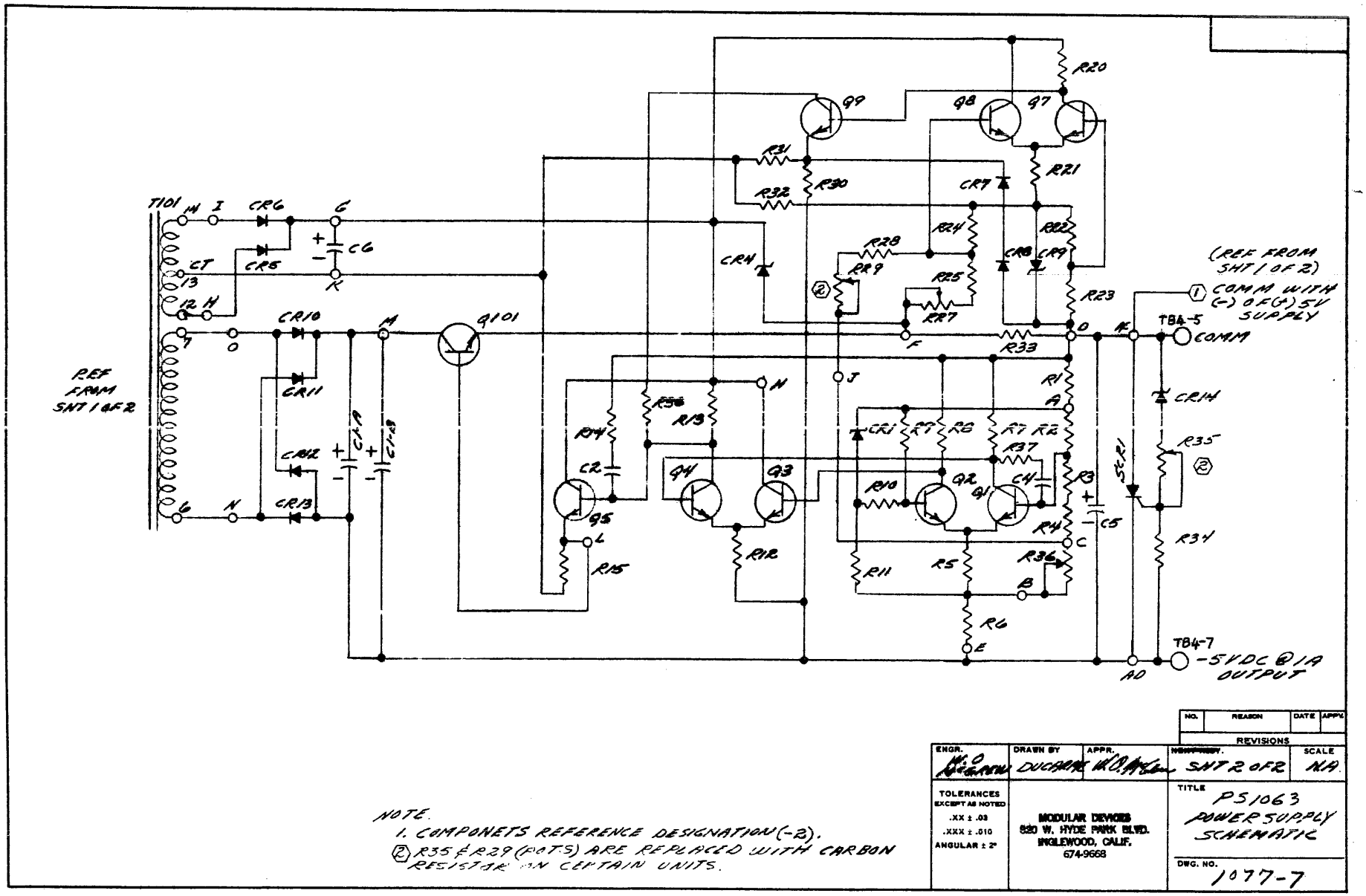
Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	Not Used		
R2	680 ohms 2W WW	IRC	BWA
R3	10 ohms ½W 10%		
R4	10 ohms ½W 10%	IRC	
R5	Not Used		
R6	Not Used		
R7	10K ½W 10%		
R8	Not Used		
R9	2.2K 2W WW	Corning	RL205-C5
R10	" " "	"	"
R11	1K ½W 10%		
R12	100 ohms " "		
R13	2.2K " "		
R14 *	2.2K " "		
R15 *	3.3K " "		
R16	4.7K " "		
R17 *	2.2K " "		
R18 *	1.5K " "		
R19	680 ohms " "		
R20	10K " "		
R21	1.5K 2W "		
R22	15K ½W "		
R23	470 ohms 2W	IRC	BWH
R24	Not Used		
R25	Not Used		1C1
R26	Not Used		
R27	100 ohms ½W 10%		
R28	120 ohms " "		
R29	100 ohms ½W 10%		
R30	" " "		
R31	330 ohms ½W 10%		
R32	200 ohms WW POT	Clarostat U-39	
R101-1	500 ohms WW POT	Clarostat 43C2	
R102A,B	0.1 ohms 5W WW	IRC	PW-5
R103	0.1 ohms " "	"	"
R104	" " " "	"	"
R107	6.8K 1W 10%		
R108 *	33 ohms 2W 10%		

Notes & Part No	Part Name & Description	MFG	MFG Part No
C1	.001 MFD 1000VDC	Cen.Lab.	DD102
C2	Not Used		
C3	.01 MFD 50 VDC	Cen.Lab.	CK103
C4	100 MFD 50 VDC	G-D	BR100-50
C5	50 MFD 25VDC		
C6 *	.01 MFD 50 VDC	Cen.Lab.	CK103
C102	1000 MFD 15 VDC	C-D	BR1000-15
C103	14000 MFD 30 VDC	STM	
C106	0.1 MFD 10V	Cen.Lab.	
C107	.05 MFD 20 VDC	Cen.Lab.	UK20-503
CR1,CR2	D9906		
CR3,CR4	IN752A ZENER		
CR5	D9906		
CR6	IN749A ZENER		
CR7	D9906		
CR9	D9906		
CR10	D9906		
CR11	D9906		
CR12	IN751A ZENER		
CRB	Rectifier Bridge	Sem.Tech	SCBA-05
CR105	368A		
SCR101	2N4167		
1C1	CA3018	RCA	
1C2	CA3018	RCA	
Q1	2N3638=	Fairchild	
Q101	2N3055		
Q103	2N3055		
Q104	2N3055		
*	Selected Value		
*R109	1.5K ½W 10%		

S 1063 POWER SUPPLY SPECIFICATIONS

INPUT:	105-125 VAC 47-440 cps single phase
OUTPUT:	+5 VDC @ 8.0 amps. -5 VDC @ 1.0 amps.
ADJUSTMENT RANGE:	± 5 % minimum.
LINE REGULATION:	3 mv maximum for 105-125v line change.
LOAD REGULATION:	5 mv maximum for full load change.
RIPPLE:	.05% maximum peak to peak.
TRANSIENT RESPONSE:	Recovery with 50 microseconds maximum for 50% change in load.
TOTAL REGULATION:	± 4% max. for all effects including ripple, transient loads, dc loading from 0 to 100%, line voltage & frequency, temperature, 8 hour stability and all other sources.
AMBIENT TEMPERATURE:	-20 to +70°C with load of 5 amperes at +5V and 1 ampere at -5V with natural convection cooling. At maximum load conditions, the supply shall operate satisfactorily in a -20 to +70°C ambient with a maximum air movement over the unit of 100 lfm.
PACKAGE DISSIPATION:	85 watts maximum.
ISOLATION:	100 megohms minimum from primary winding to all other windings and chasis, at 220 volts.
OVERLOAD PROTECTION:	Electronic current limit with automatic recovery.
I/O TERMINALS:	Barrier strip.
SIZE:	See drawing.


TB4-6 SENSE
TB4-1
TB1 AC
F1
115 V 50-400CY INPUT
TB1 AC
TB4-2
CR BRIDGE
SEE SHT 2
CR6
CR5
C6
CT
Q104
R104
Q103
R103
R101
Q101
C1-A
C1-B
R14
R38
R13
C2
Q5
Q4
Q3
R15
R12
H
J
L
Q9
R31
R32
R30
R20
Q8
Q7
R21
CR7
R28
R29
R24
R26
R27
CR8
CR9
R22
R23
R102
D
F
BB
TB4-4 (+) 5 VDC @ 5A OUTPUT
R1
A
CR1
R9
R8
R7
R37
R2
C4
Q2
Q1
R10
R4
R3
C5
C
R11
R5
B
R36
R6
E
SCR1
CR14
R35
R34
TB4-5 COMM
AC
REF SHT 2
NOTE:
1. COMPONENTS REFERENCE DESIGNATION (-1)
2 R35 & R29 (POTS) ARE REPLACED WITH CARBON RESISTOR ON CERTAIN UNITS.
NO. REASON DATE APPR.
REVISIONS
ENGR. W.O. MC (GREW)
DRAWN BY DUCARME
APPR. WOTTGEB
SHT 1 of 2
SCALE N.A.
TOLERANCES EXCEPT AS NOTED .XX ± .03 .XXX ± .010 ANGULAR ± 2°
MODULAR DEVICES 820 W. HYDE PARK BLVD. INGLEWOOD, CALIF. 674-9668
TITLE PS 1063 POWER SUPPLY SHCEMATIC
DWG. NO. 1077-7



NOTE.
1. COMPONETS REFERENCE DESIGNATION (-2).
2. R35 & R29 (POTS) ARE REPLACED WITH CARBON RESISTOR ON CERTAIN UNITS.

NO.	REASON	DATE	APPV.
	REVISIONS		

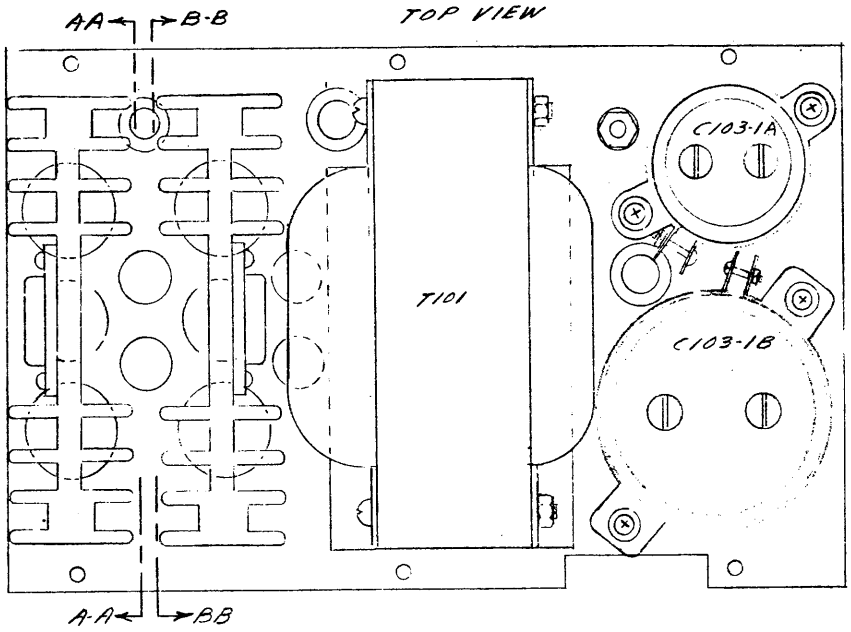
ENGR.	DRAWN BY	APPR.	SHEET	SCALE
M.O.	DUCHARME	M.O.	SHT 2 OF 2	N/A

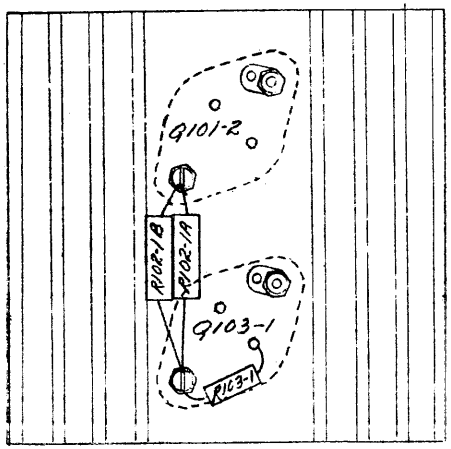
TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
930 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

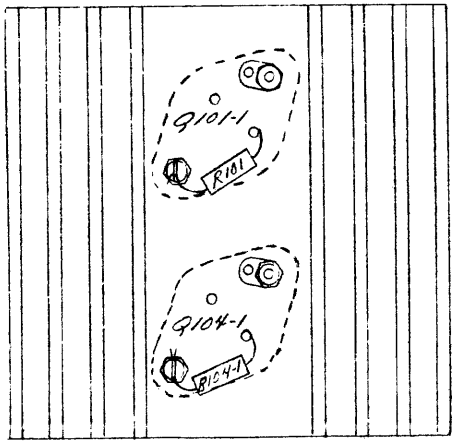
TITLE: PS1063 POWER SUPPLY SCHEMATIC

DWG. NO. 1077-7





VIEW A-A



VIEW BB

NOTE:
1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY.

NO.	REASON	DATE	APPV.
	REVISIONS		

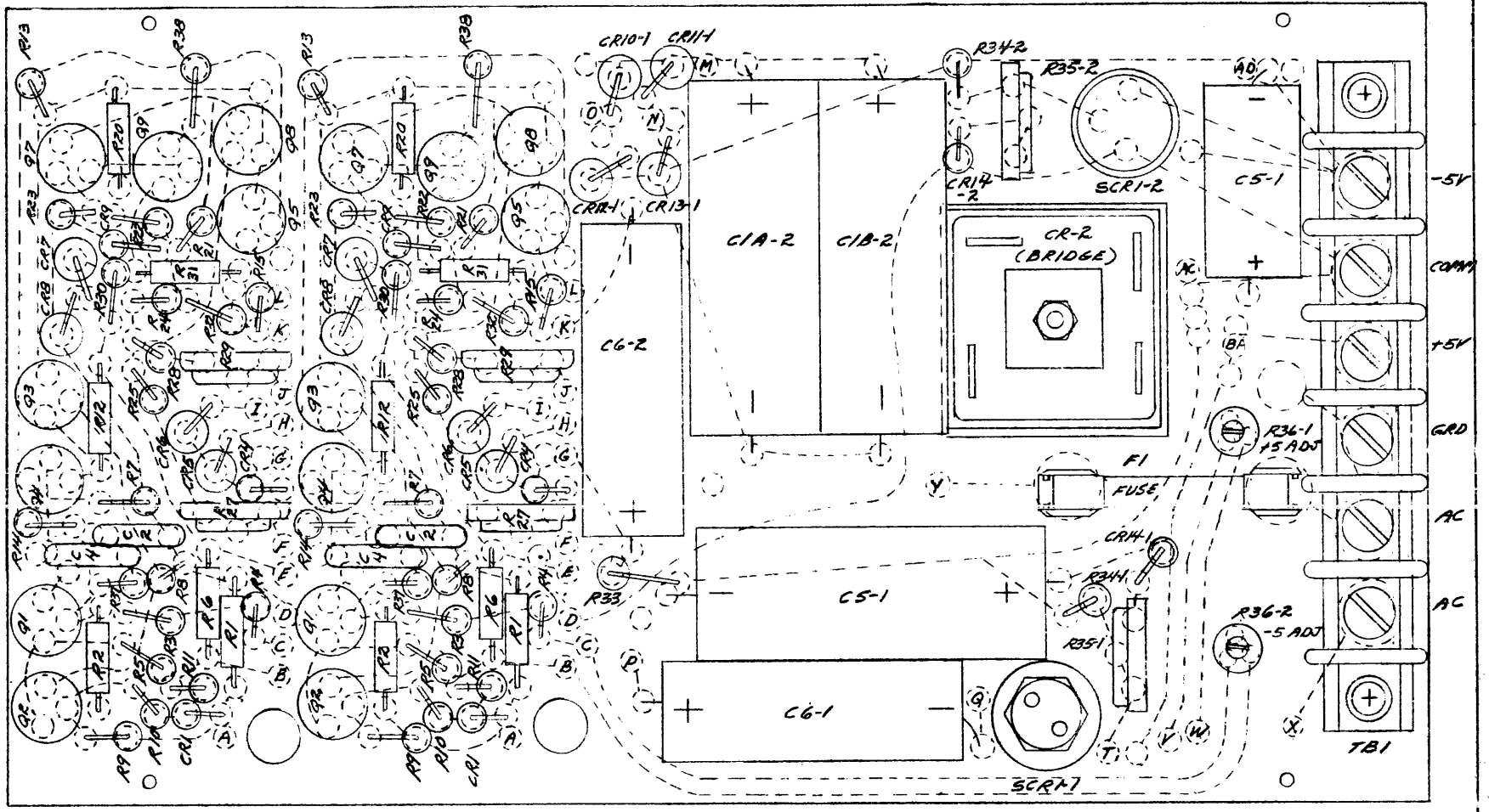
ENGR.	DRAWN BY	APPR.	[illegible]	SCALE
McGREW	DUCHARME	McGREW	N.A.	1X1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
820 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

TITLE
PS1063
COMPONENT
LAYOUT

DWG. NO.
1077-8



NOTE
1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY

ENGR.	DRAWN BY	APPR.	NEXT ASSY.	SCALE
MCGREW	R.L.D.	W/M	N.A.	2X1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
820 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

TITLE
PS 1063
COMPONENT
LAYOUT

DWG. NO.
1077-6

MASTER BILL OF MATERIAL FOR S1063 Decision Control

MODULAR DEVICES Output 1 +5V 5A

SHEET 1 OF 2 REV

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	330 ohms 2W WW		
R3	400 ohms " "	Sprague	
R4	150 ohms " "		
R5	1.5K ½W 10%		
R6	10 ohms " "		
R7	1K " "		
R8	" " "		
R9	2.2K " "		
R10	" " "		
R11	100 ohms " "		
R12	1.5K " "		
R13	4.7K " "		
R14	68 ohms " "		
R15	15K " "		
R16	Not used		
R17	Not used		
R18	Not used		
R19	Not used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not used		
R27	250 POT Carbon	Mallory	
R28	3.3K ½W 10%		
R29	10K POT Carbon	Mallory	
R30	1K ½W 10%		
R31	6.8K " "		
R32	1.5K 2W WW		
R33	Not used		
R34	100 ohms ½W 10%		
R35	250 ohms POT Carbon	Mallory	
R36	200 ohms POT Cermet	Beckman	
R37	1K ½W 10%		
SCR1	MCR 2305-3		

Notes & Part No	Part Name & Description	MFG	MFG Part No
R101	6.8K 1W 10%		
R102A,B	0.1 ohms 5W WW		PW-5
R103	" " "	IRC	PW-5
R104	" " "	IRC	PW-5
C101A	21000 MFD 15V	Sprague	
C101B	9200 MFD 15 VDC	Sprague	
C2	0.02 MFD 20 VDC		
C4	.001 MFD 20 VDC		
C5	1000 MFD 15 VDC	C-D	
C6	100 MFD 50 VDC	C-D	
CR1	IN 748		
CR2	Not used		
CR3	Not used		
CR4	IN 752		
CR5	IN 3253		
CR6	IN 3253		
CR7	IN 3253		
CR8	IN 3253		
CR9	IN 752		
CR10	Not used		
CR11	Not used		
CR12	Not used		
CR13	Not used		
CR14	IN4733		
CR Bridge	Rectifier Bridge	Sem-Tech	SCBA-1
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not used		
Q7	2N697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
Q103	2N3055		
Q104	2N3055		

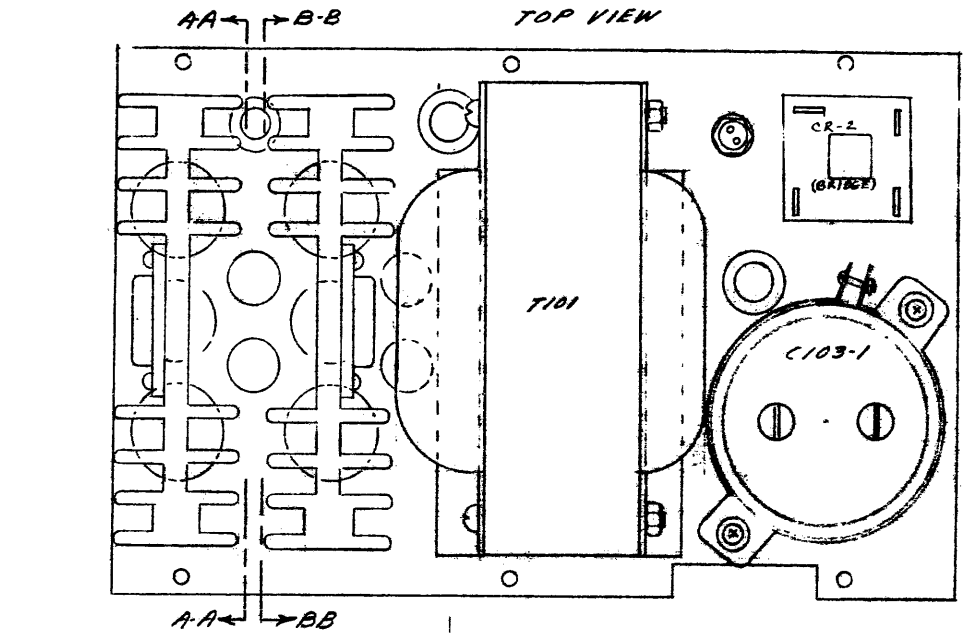
MASTER BILL OF MATERIAL FOR S1063 Decision Control

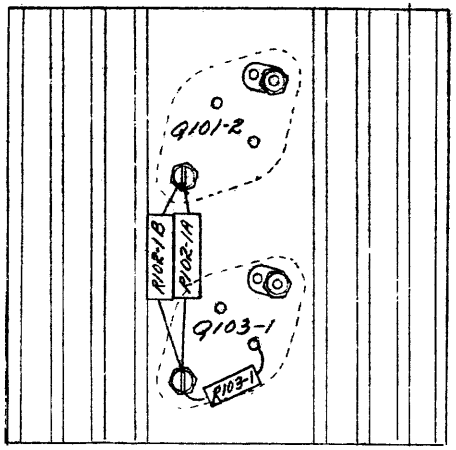
MODULAR DEVICES Output 2 -5V 1A

SHEET 2 OF 2 REV

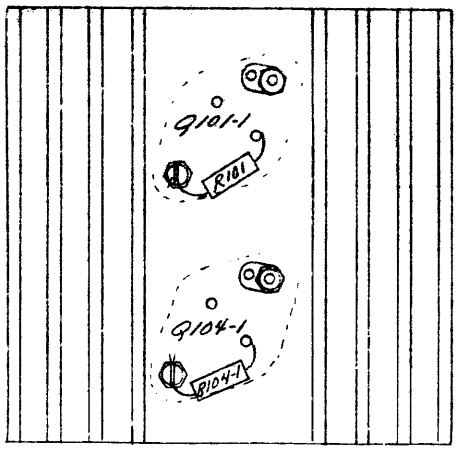
Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	330 ohms 2W WW		
R3	400 ohms " "	Sprague	
R4	150 ohms " "		
R5	1.5K ½W 10%		
R6	10 ohms " "		
R7	1K " "		
R8	" " "		
R9	2.2K " "		
R10	" " "		
R11	100 ohms " "		
R12	1.5K " "		
R13	4.7K " "		
R14	68 ohms " "		
R15	15K " "		
R16	Not used		
R17	Not used		
R18	Not used		
R19	Not used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not used		
R27	250 POT Carbon	Mallory	
R28	3.3K ½W 10%		
R29	10K POT Carbon	Mallory	
R30	1K ½W 10%		
R31	6.8K " "		
R32	680 ohms 2W WW		
R33	0.47 ohms " "	BWH	
R34	100 ohms ½W 10%		
R35	" POT Carbon	Mallory	
R36	200 ohms " Cermet	Beckman	
R37	1K ½W 10%		

Notes & Part No	Part Name & Description	MFG	MFG Part No
C1A,B	1000 MFD 15 VDC	Sprague	390
C2	0.02 MFD 20 VDC		
C4	.001 MFD 20 VDC		
C5	250 MFD 15 VDC	C-D	
C6	100 MFD 50 VDC	C-D	
CR1	IN 748		
CR2	Not used		
CR3	Not used		
CR4	IN 752		
CR5	IN 3253		
CR6	IN 3253		
CR7	IN 3253		
CR8	IN 3253		
CR9	IN 752		
CR10	IN 3253		
CR11	IN 3253		
CR12	IN 3253		
CR13	IN 3253		
CR14	IN4732		
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not used		
Q7	2N697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
SCR1	2N3528		
F1	Fuse 2A 3AG		
PT101	Transformer	Mod.Dev.	PT251C





VIEW A-A



VIEW BB

NOTE:

1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY.

NO.	REASON	DATE	APPR.
	REVISIONS		

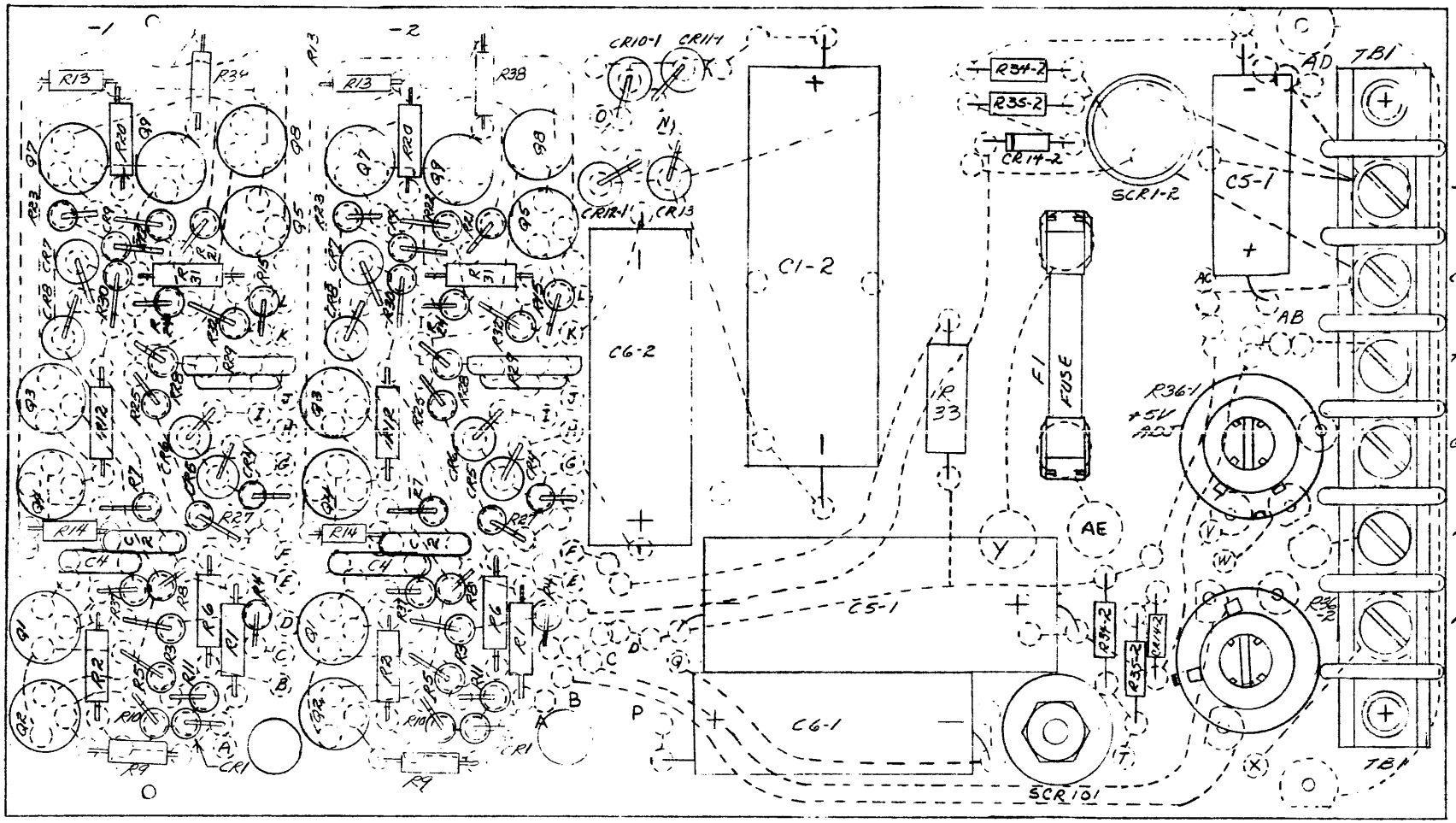
ENGR.	DRAWN BY	APPR.	MFG. APPR.	SCALE
McGREW	DUCHARME	McGREW	N.A.	1X1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
820 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

TITLE
PS1063-A
COMPONENT
LAYOUT

DWG. NO.
1077-8A



NOTE
1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY

ENGR.	DRAWN BY	APPR.	NEXT ASSY.	SCALE
MCGREW	R.L.D.		N.H.	2X1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR [illegible]
[illegible] PARK BLVD.
[illegible]
714-9664

TITLE
PS1063-A
COMPONENT
LAYOUT

DWG. NO.
1077-6-A

MASTER BILL OF MATERIAL FOR S1063 Rev.A Decision Control

Modular Devices Output 1 +5V 5A

SHEET 1 OF 2 REV A

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	330 ohms 2W WW		
R3	400 ohms " "	Sprague	
R4*	150 ohms " "		
R5	1.5K ½W 10%		
R6	10 ohms " "		
R7	1K " "		
R8	" " "		
R9	2.2K " "		
R10	" " "		
R11	100 ohms " "		
R12	1.5K " "		
R13	4.7K " "		
R14	68 ohms " "		
R15	15K " "		
R16	Not Used		
R17	Not Used		
R18	Not Used		
R19	Not Used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not Used		
R27*	68 ohms " "		
R28	3.3K ½W 10%		
R29	10K POT Carbon	Mallory	
R30	1K ½W 10%		
R31	6.8K " "		
R32	1.5K 2W WW		
R33	Not Used		
R34	100 ohms ½W 10%		
R35*	100 ohms " "		
R36	200 ohms POT WW	Clarostat	U39-200
R37	1K ½W 10%		
SCR1	MCR 2305-3		

Notes & Part No	Part Name & Description	MFG	MFG Part No
R101	6.8K 1W 10%		
R102A,B	0.1 ohms 5W WW		PW-5
R103	" " "	IRC	PW-5
R104	" " "	IRC	PW-5
C101	21000 MFD 15V	Sprague	36D
C2	0.02 MFD 20VDC		
C4	.001 MFD 20VDC		
C5	1000 MFD 15VDC	C-D	BR1000-15
C6	100 MFD 50VDC	C-D	BR100-50
CR1	IN 748		
CR2	Not Used		
CR3	Not Used		
CR4	IN 752		
CR5	IN 3253 or Equiv.		
CR6	IN 3253 "		
CR7	IN 3253 "		
CR8	IN 3253 "		
CR9	IN 752		
CR10	Not Used		
CR11	Not Used		
CR12	Not Used		
CR13	Not Used		
CR14	IN4733		
CR Bridge	Rectifier Bridge	Semtech	SCBA-1
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not Used		
Q7	2N697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
Q103	2N3055		
Q104	2N3055		

* Selected Value

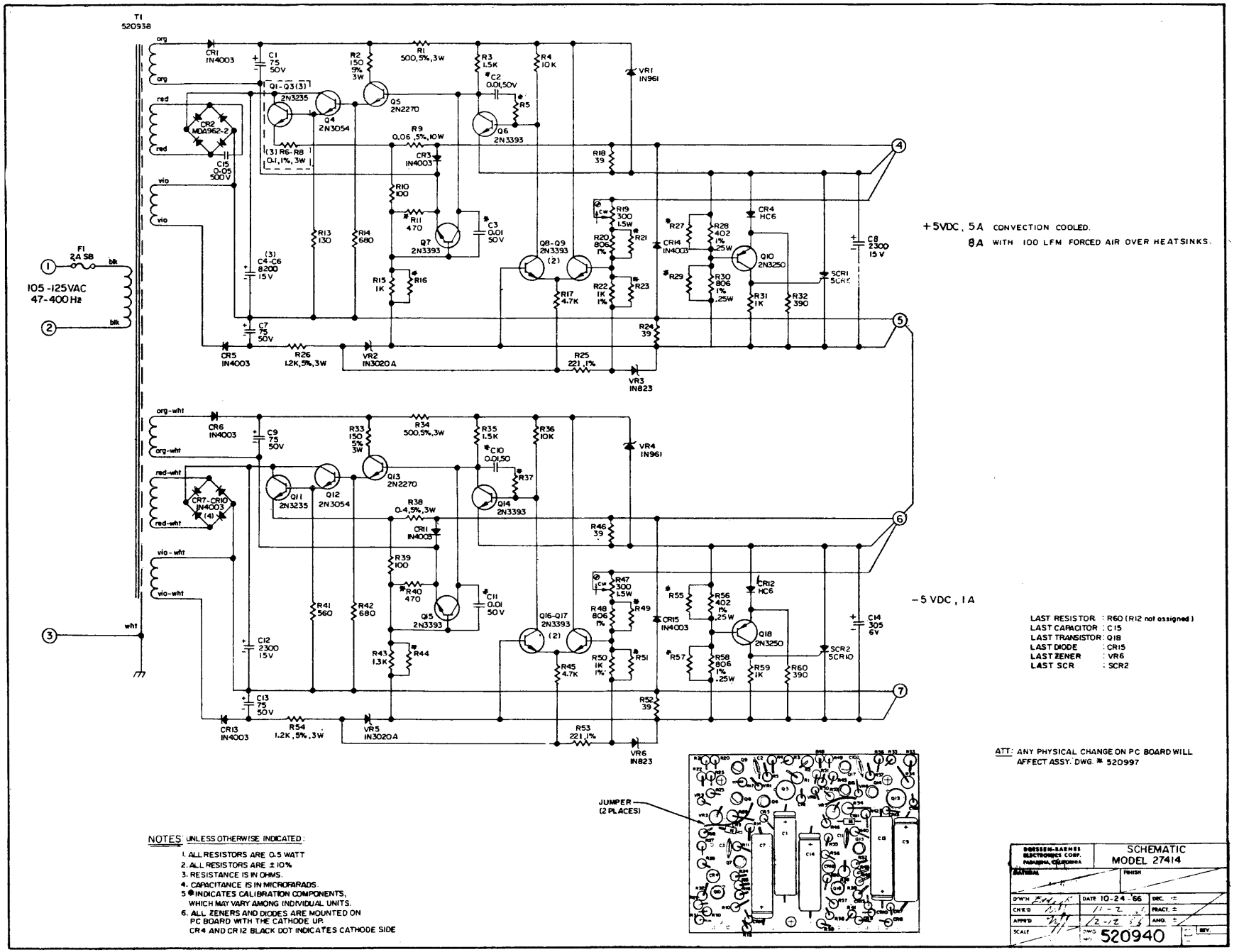
MASTER BILL OF MATERIAL FOR S1063 Rev. A Decision Control

Modular Devices Inc. Output 2 -5V 1A

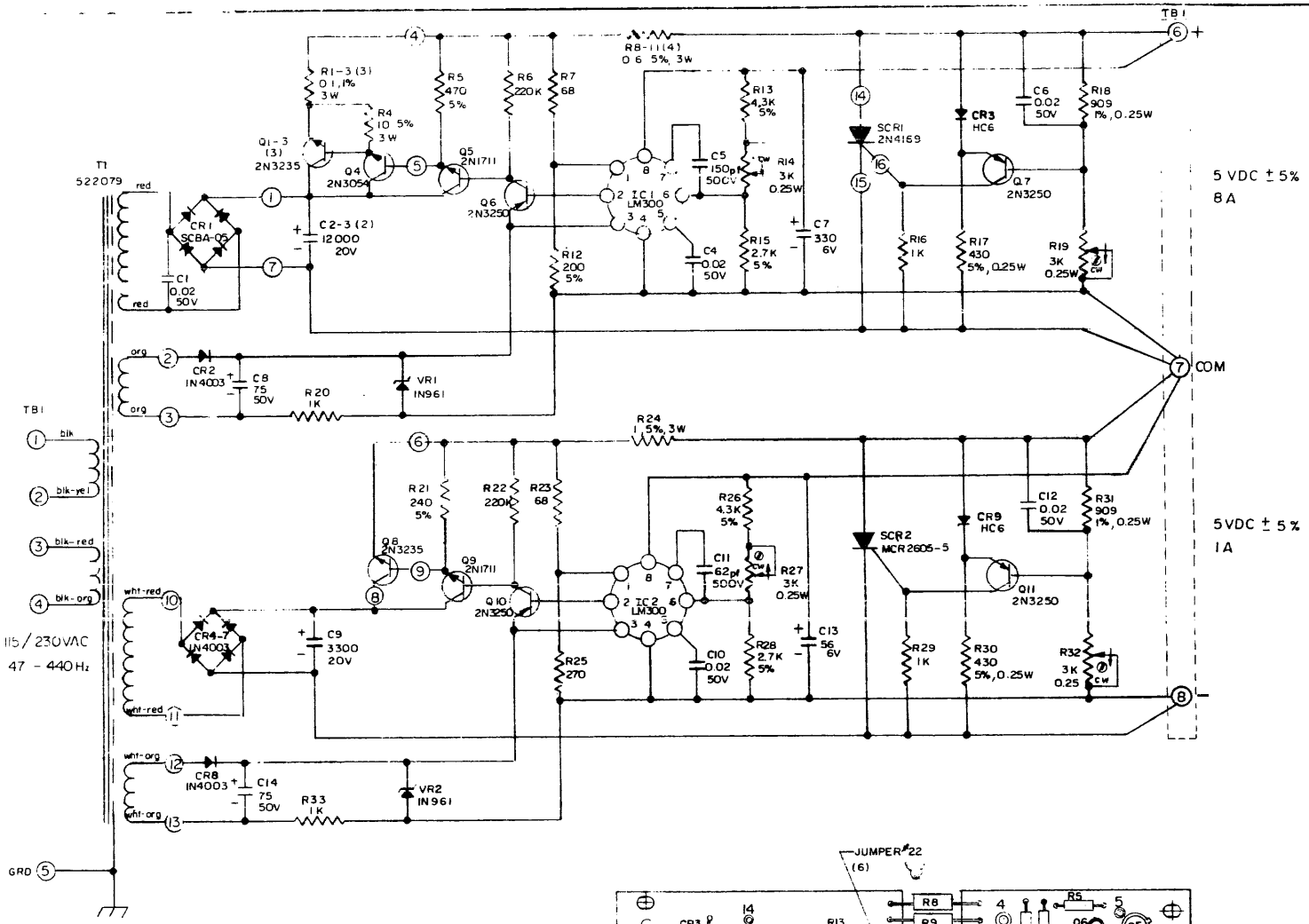
SHEET 2 OF 2 REV A

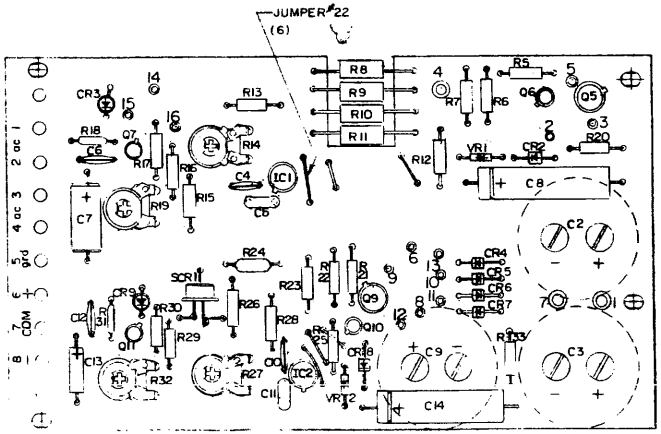
Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	330 ohms 2W WW		
R3	400 ohms " "	Sprague	
R4*	150 ohms " "		
R5	1.5K ½W 10%		
R6	10 ohms " "		
R7	1K " "		
R8	" " "		
R9	2.2K " "		
R10	" " "		
R11	100 ohms " "		
R12	1.5K " "		
R13	4.7K " "		
R14	68 ohms " "		
R15	15K " "		
R16	Not Used		
R17	Not Used		
R18	Not Used		
R19	Not Used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not Used		
R27*	68 ohms " "		
R28	3.3K ½W 10%		
R29	10K POT Carbon	Mallory	
R30	1K ½W 10%		
R31	6.8K " "		
R32	680 ohms 2W WW		
R33	0.47 ohms " "	BWH	
R34	100 ohms ½W 10%		
R35*	100 ohms " "		
R36	200 ohms POT WW	Clarostat	U39-200
R37	1K ½W 10%		

Notes & Part No	Part Name & Description	MFG	MFG Part No
C1	1900 MFD 15VDC	Sprague	39D
C2	0.02 MFD 20VDC		
C4	.001 MFD 20VDC		
C5	250 MFD 15VDC	C-D	BR250-15
C6	100 MFD 50VDC	C-D	BR100-50
CR1	IN 748		
CR2	Not Used		
CR3	Not Used		
CR4	IN 752		
CR5	IN 3253 or Equiv.		
CR6	IN 3253 or Equiv.		
CR7	IN 3253 " "		
CR8	IN 3253 " "		
CR9	IN 752		
CR10	IN 3253 or Equiv.		
CR11	IN 3253 " "		
CR12	1N3253 " "		
CR13	IN 3253 " "		
C14	IN 4732		
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not Used		
Q7	2N697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
SCR1	2N3528		
F1	Fuse 2A 3AG		
PT101	Transformer	Mod.Dev.	PT251C
*	Selected Value		


T1
520938
105 -125VAC
47-400Hz
F1
2A SB
+5VDC, 5A CONVECTION COOLED.
8A WITH 100 LFM FORCED AIR OVER HEATSINKS.
-5 VDC, 1A
LAST RESISTOR : R60 (R12 not assigned)
LAST CAPACITOR : C15
LAST TRANSISTOR : Q18
LAST DIODE : CR15
LAST ZENER : VR6
LAST SCR : SCR2
JUMPER (2 PLACES)
ATT: ANY PHYSICAL CHANGE ON PC BOARD WILL AFFECT ASSY. DWG. # 520997
NOTES: UNLESS OTHERWISE INDICATED:
1. ALL RESISTORS ARE 0.5 WATT
2. ALL RESISTORS ARE ± 10%
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS IN MICROFARADS.
5. * INDICATES CALIBRATION COMPONENTS, WHICH MAY VARY AMONG INDIVIDUAL UNITS.
6. ALL ZENERS AND DIODES ARE MOUNTED ON PC BOARD WITH THE CATHODE UP. CR4 AND CR12 BLACK DOT INDICATES CATHODE SIDE
DORSETT-BARNES ELECTRONICS CORP. PALOSPRING, CALIFORNIA
SCHEMATIC
MODEL 27414
DRWN
CHK'D
APP'D
SCALE
DATE 10-24-66
520940

REV	DESCRIPTION	DATE	APPR'D





PC BOARD ASS'Y #52225i

NOTES unless otherwise indicated

1. ALL RESISTORS ARE 0.5 WATT
2. ALL RESISTORS ARE ± 10%
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS IN MICROFARADS
5. INDICATES CALIBRATION COMPONENT, WHICH MAY VARY AMONG INDIVIDUAL UNITS
6. INPUT CONNECTIONS
   A. 115VAC TIE 1 AND 3, 2 AND 4 — USE 1 AND 2.
   B. 230VAC TIE 2 AND 3, —— — USE 1 AND 4.

LAST RESISTOR R33
" CAPACITOR C14
" TRANSISTOR Q11
" DIODE CR7
" ZENER VR4

DRESSER-RAND ELECTRONICS CORP. PASADENA, CALIFORNIA	SCHEMATIC MODEL 27929	
MATERIAL	FINISH	
DWN SJC	DATE 12-22-67	DEC. ±
CHK'D W Kew	1-14-68	FRACT. ±
APP'D		ANGL. ±
SCALE	DWG. NO. 522249	REV.

PARTS LIST WITH MANUFACTURER CROSS REFERENCE
MODEL 27929

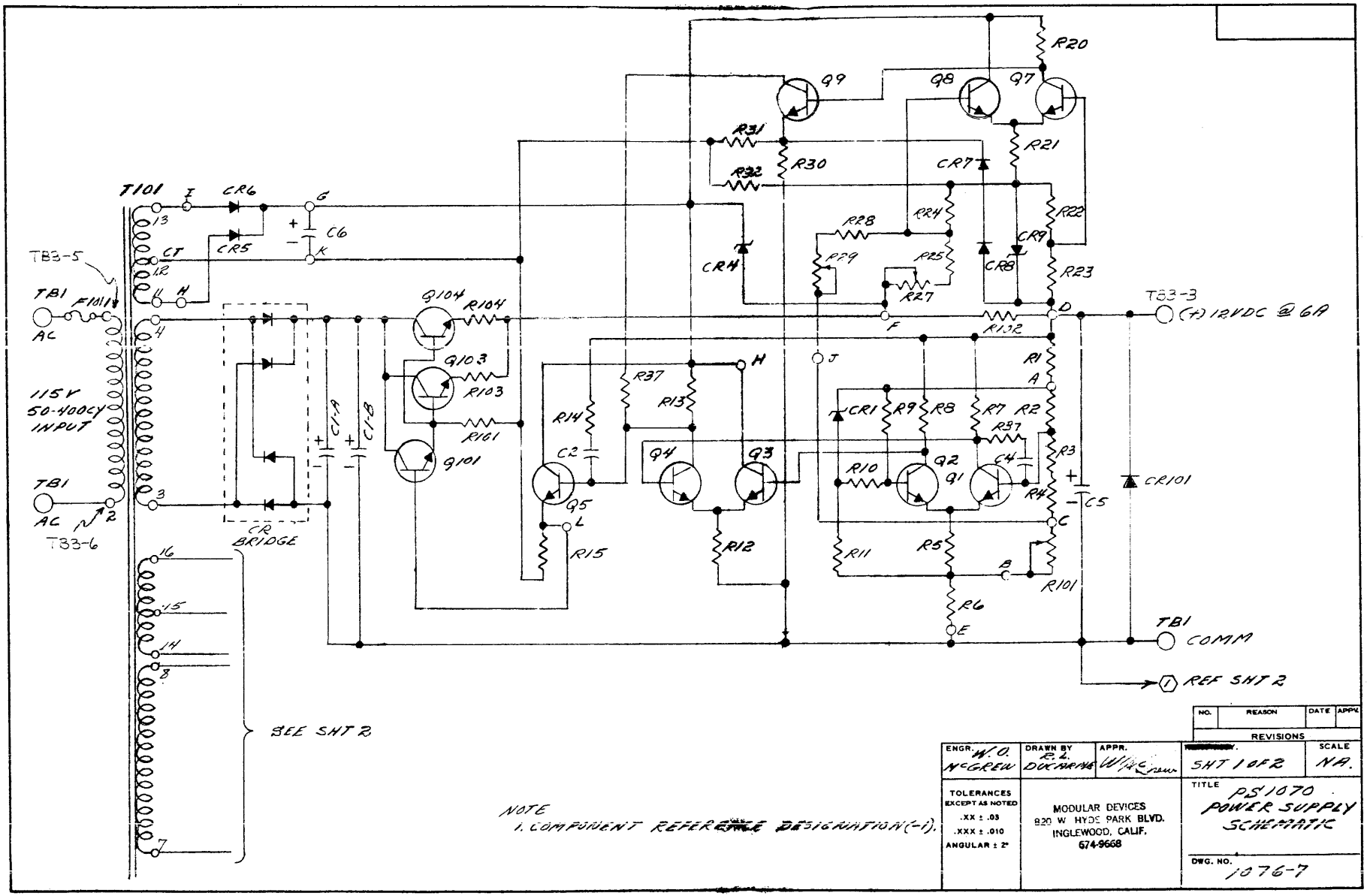
ITEM	SCHEMATIC SYMBOL	DESCRIPTION	D/B PART NO.	MFR. PART NO.	MANUFACTURER FED. CODE
1	--	Cover	522200	--	94412
2	C1	Capacitor, .02 mfd, 50 VDC	332502-2	CK203	25244
3	CR1	Rectifier, SCBA-05	432601-113	SCBA-05	14099
4	SCR1	SCR 2N4169	432602-15	2N4169	04713
5	R4	Resistor, 10 ohm, 3w, 5%	438075-191	4361	44655
6	R1-3	Resistor, 0.1 ohm, 3w, 1%	513052-2	884-3	44655
7	T1	Transformer	522079	522079	21645
8	Q4	Transistor, 2N3054	478801-68	2N3054	86684
9	Q1,2,3,8	Transistor, 2N3235	478801-69	2N3235	04713
10	--	Printed Circuit Board Assem. Dwg.	522250	522250	94412
11	--	Printed Citcuit Board (Dwg. 522246)	522245	522245	94412
12	TB1	Barrier Strip Kulka	315205-77	599-2021-8	--
13	C2, 3	Capacitor, 12,000 mfd, 20v	519651-19	71FZ20HC123	99392
14	C9	Capacitor, 3300 mfd, 20v	519653-3	71FZ20HA3321	99392
15	C7	Capacitor, 330 mfd, 6v	333104-207	CS13BB337K	83125
16	C8, 14	Capacitor, 75 mfd, 50v	333104-119	NLW75-50	14655
17	C12	Capacitor, 56 mfd, 6v	333104-208	CS13BB556K	83125
18	C4,6,10,13	Capacitor, 0.02 mfd, 50v	332502-2	CK203	25244
19	C5	Capacitor, 150 pf, 500v	334505-59	DM-15-151	84171
20	C11	Capacitor, 62 pf. 500v	334505-58	DM-15-620	84171
21	R14,19,27,32	Potentiometer, 3K	427504-23	MTC33L4	37942
22	CR2,4-8	Rectifier, 1N4003	517655-1	1N4003	04713
23	SCR2	Rectifier, SCR2605-5	432602-11	MCR2605-5	04713

PARTS LIST WITH MANUFACTURER CROSS REFERENCE
MODEL 27929

ITEM	SCHEMATIC SYMBOL	DESCRIPTION	D/B PART NO.	MFR. PART NO.	MANUFACTURER FED. CODE
24	R24	Resistor, 1 ohm, 3w, 5%	438075-67	4430	44655
25	R8-11	Resistor, 0.6 ohm, 3w, 5%	513019-15	882-3	44655
26	R18, 31	Resistor, 909 ohms, .25w, 1%	437306-5	MF5C	19701
27	R6, 22	Resistor, 220K, .5w, 10%	MS35043-27K	MS35043-27K	01121
28	R13, 26	Resistor, 4300 ohm, .5w, 5%	MS35043-102J	MS35043-102J	01121
29	R15, 28	Resistor, 2700 ohm, .5w, 5%	MS35043-97J	MS35043-97J	01121
30	R16,20,29,33	Resistor, 1000 ohm, .5w, 10%	MS35043-13K	MS35043-13K	01121
31	R17, 30	Resistor, 430 ohm, .5w, 5%	MS35043-78J	MS35043-78J	01121
32	R25	Resistor, 270 ohm, .5w, 10%	MS35043-200K	MS35043-200K	01121
33	R12	Resistor, 200 ohm, .5w, 5%	MS35043-70J	MS35043-70J	01121
34	R5	Resistor, 470 ohm, .5w, 5%	MS35043-79J	MS35043-79J	01121
35	R7, 23	Resistor, 68 ohm, .5w, 10%	MS35043-6K	MS35043-6K	01121
36	R21	Resistor, 240 ohm, .5w, 5%	MS35043-72J	MS35043-72J	01121
37	IC 1,2	I. C. LM300	478801-100	LM300	12040
38	Q5, 9	Transistor 2N1711	478801-80	2N1711	04713
39	Q6,7,10,11	Transistor 2N3250	478801-75	2N3250	04713
40	VR1, 4	Zener, 1N961	490001-23	1N961	07263
41	CR3, 9	Diode HC6	432601-91	HC6	99942
42		Schematic	522249		

S 1070 POWER SUPPLY SPECIFICATIONS

INPUT:	105-125 VAC 47-440 cps single phase
OUTPUT:	+12 VDC @ 6.0 amps -12 VDC @ 4.0 amps
ADJUSTMENT RANGE:	±10% min.
LINE REGULATION:	3 mv maximum for 105-125v line change.
LOAD REGULATION:	5 mv maximum for full load change.
RIPPLE:	.05% maximum peak to peak.
TRANSIENT RESPONSE:	Recovery within 50 microseconds maximum for 50% change in load.
TOTAL REGULATION:	±2% max. for all effects including ripple, transient loads, dc loading from 0 to 100%, line voltage & frequency, temperature, 8 hour stability and all other sources.
AMBIENT TEMPERATURE:	-20°C to + 50°C operating, convection cooling. -30°C to + 85°C non-operating.
ISOLATION:	100 megohms minimum from primary winding to all other windings and chasis, at 220 volts.
OVERLOAD PROTECTION:	Electronic current limit with automatic recovery.
I/O TERMINALS:	Barrier strip.
SIZE:	See drawing.



NOTE
1. COMPONENT REFERENCE DESIGNATION (-1).

NO.	REASON	DATE	APPR.
	REVISIONS		

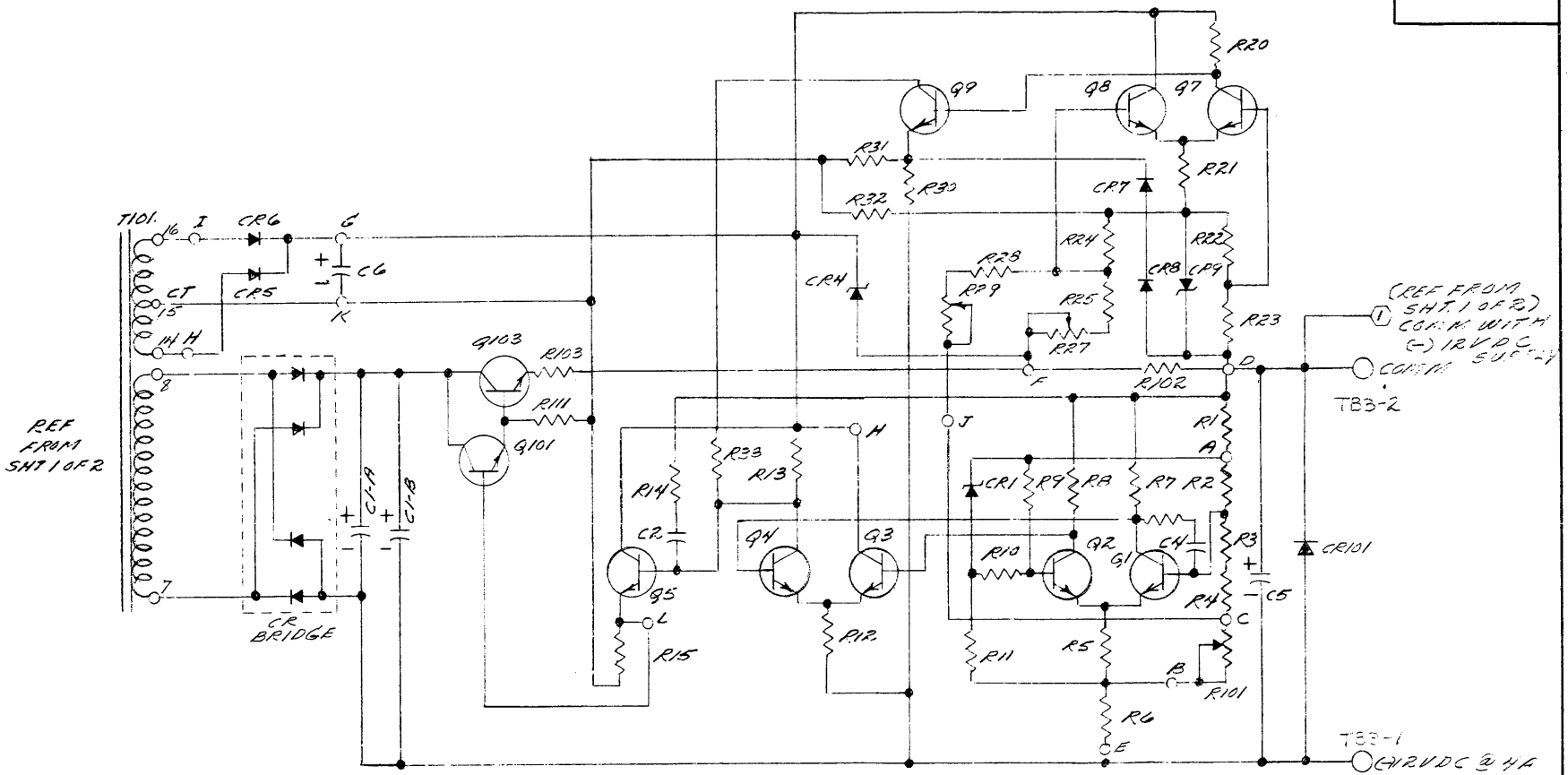
ENGR. W.O. McGREW	DRAWN BY R.L. DICKMANN	APPR. W.W.C.	SHT 1 OF 2	SCALE N.A.

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
820 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

TITLE PS1070 POWER SUPPLY SCHEMATIC

DWG. NO. 1076-7



NOTE
1. COMPONETS REFERENCE DESIGNATION (-2).

NO.	REASON	DATE	APPR.
	REVISIONS		

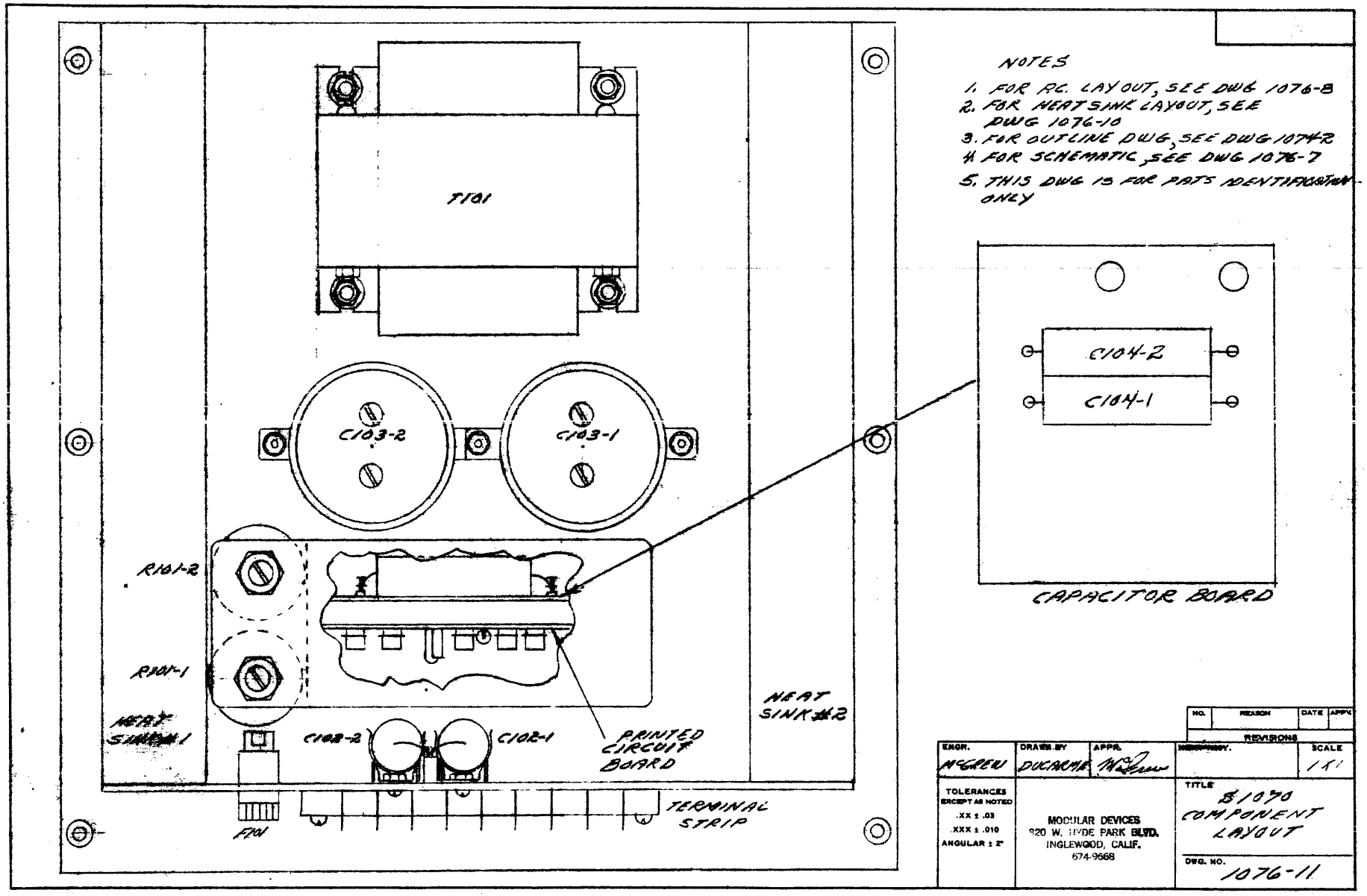
ENGR.	DRAWN BY	APPR.	~~NEXT ASSY.~~ SHT 2 OF 2	SCALE
W. O. McGREW	DUCHARME	W.O.M.		N.A

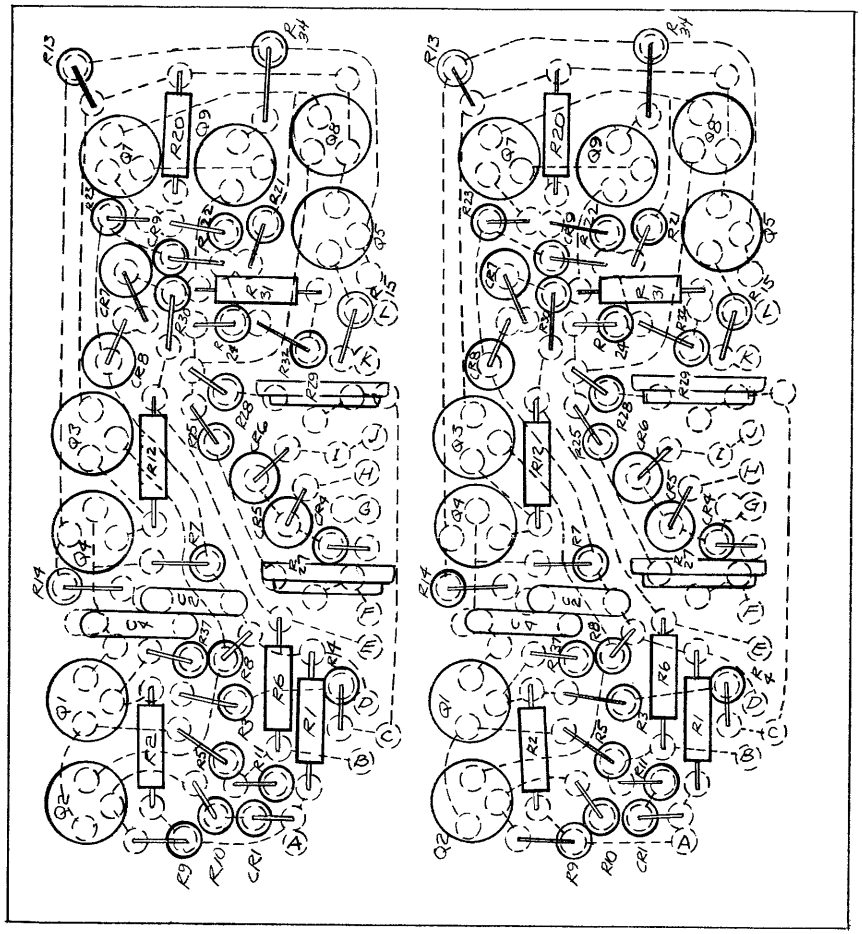
TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
320 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9568

TITLE
PS1070
POWER SUPPLY
SCHEMATIC

DWG. NO.
1076-7


T101
C103-2
C103-1
R101-2
R101-1
HEAT SINK #1
C102-2
C102-1
PRINTED CIRCUIT BOARD
HEAT SINK #2
TERMINAL STRIP
FDI
NOTES
1. FOR P.C. LAYOUT, SEE DWG 1076-8
2. FOR HEAT SINK LAYOUT, SEE DWG 1076-10
3. FOR OUTLINE DWG, SEE DWG 1074-2
4. FOR SCHEMATIC, SEE DWG 1076-7
5. THIS DWG IS FOR PARTS IDENTIFICATION ONLY
C104-2
C104-1
CAPACITOR BOARD
NO. REASON DATE APPV
REVISIONS
ENGR. NGREEN
DRAWN BY DUCKMAN
APPR. NGreen
SCALE 1/1
TOLERANCES EXCEPT AS NOTED .XX ± .03 .XXX ± .010 ANGULAR ± 2°
MODULAR DEVICES 920 W. HYDE PARK BLVD. INGLEWOOD, CALIF. 674-9668
TITLE B1070 COMPONENT LAYOUT
DWG. NO. 1076-11



NOTE:
1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY

NO.	REASON	DATE	APPV.
	REVISIONS		

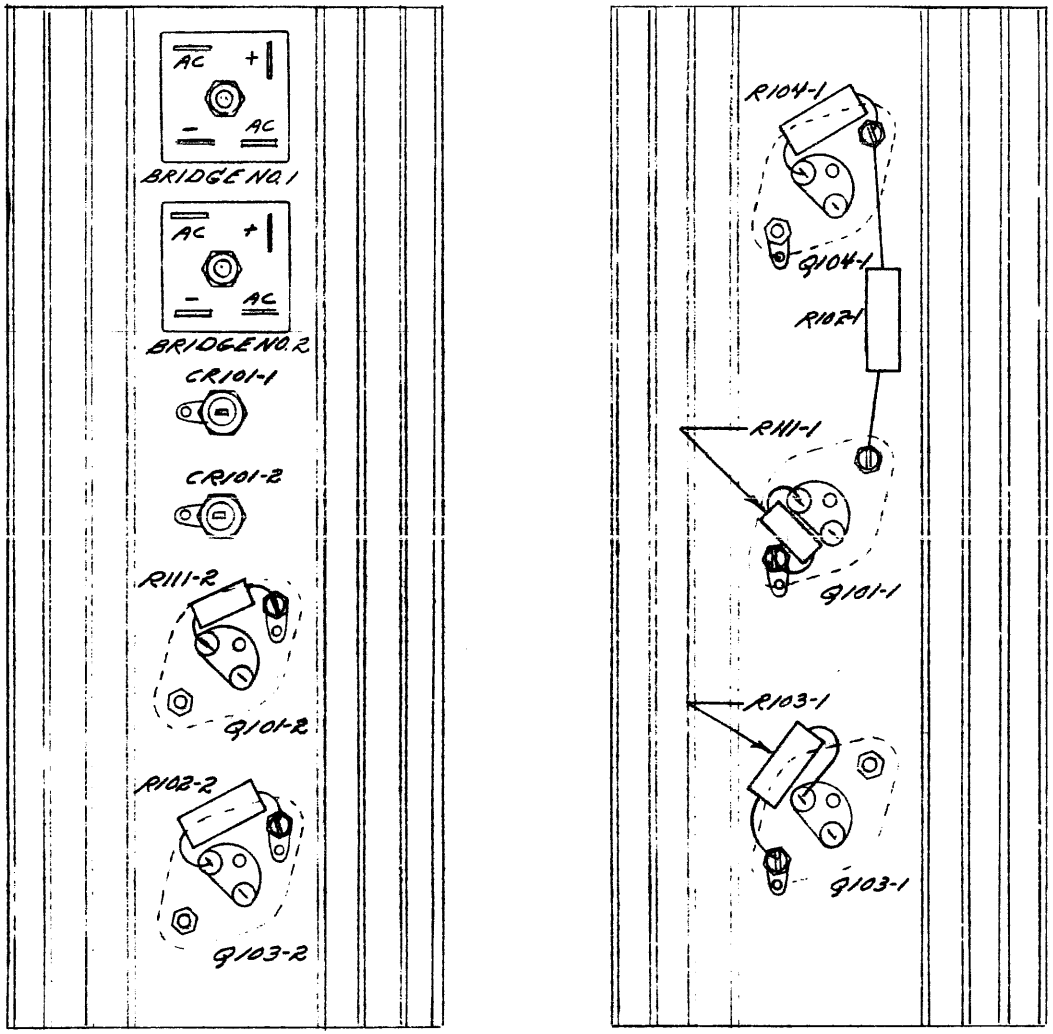
ENGR.	DRAWN BY	APPR.	NEXT ASSY.	SCALE
McGREW	Dulmage	VJ	NA	2X1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

...CES
...LVD.

TITLE
PS1070 P.C. COMPONENT LAYOUT

DWG. NO.
1676-9



NOTE

1. THIS DWG IS FOR PARTS IDENTIFICATION ONLY.

NO.	REASON	DATE	APPV.
	REVISIONS		

ENGR.	DRAWN BY	APPR.	[illegible]RY.	SCALE
N.GREN	DUCARME	W.S.		1/1

TOLERANCES EXCEPT AS NOTED
.XX ± .03
.XXX ± .010
ANGULAR ± 2°

MODULAR DEVICES
820 W. HYDE PARK BLVD.
INGLEWOOD, CALIF.
674-9668

TITLE
S1070
COMPONENT
LAYOUT

DWG. NO.
1076-10

MASTER BILL OF MATERIAL FOR S1070

MODULAR DEVICES Output 1 +12V 6A

SHEET 1 OF 1 REV

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	1.2K 2W WW		
R3	470 ohms 2W WW		
R4	470 ohms " "		
R5	3.3K ½W 10%		
R6	10 ohms " "		
R7	2.2K " "		
R8	" " "		
R9	Not used		
R10	330 ohms ½W 10%		
R11	680 ohms " "		
R12	680 ohms " "		
R13	330 ohms " "		
R14	10 ohms " "		
R15	15K " "		
R16	Not used		
R17	Not used		
R18	Not used		
R19	Not used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not used		
R27	250 ohms POT carbon	Mallory	
R28	10K ½W 10%	"	
R29	10K POT carbon		
R30	2.2K ½W 10%		
R31	" " "		
R32	1.5K 2W WW		
R33	Not used		
R34	100 ohms ½W 10%		
R37 R101	1K ½W 10% 500 ohms POT WW	Clarostat	
R102	0.1 ohms 5W WW	IRC	PW5
R103	" " "	"	"
R104	" " "	"	"
R111	6.8K 1W 10%		

Notes & Part No	Part Name & Description	MFG	MFG Part No
CR1	IN 752		
CR2	Not used		
CR3	Not used		
CR4	IN 752		
CR5	IN 3253		
CR6	IN 3253		
CR7	IN 3253		
CR8	IN 3253		
CR9	IN 752		
CR101-1	368D		
GR101-2	368D		
CR Bridge	Rectifier Bridge	Sem Tech	SCBA-1
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not used		
Q7	2N697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
Q103	2N3055		
Q104	2N3055		
T101	Transformer	PT252A	
C2	.02 MFD 20 VDC		
C4	0.001 MFD 20 VDC		
C102	1000 MFD 15 VDC	C-D	
C103	18,000 MFD 25 VDC	Sprague	
C104	100 MFD 50 VDC	C-D	
F101	Fuse	5A	

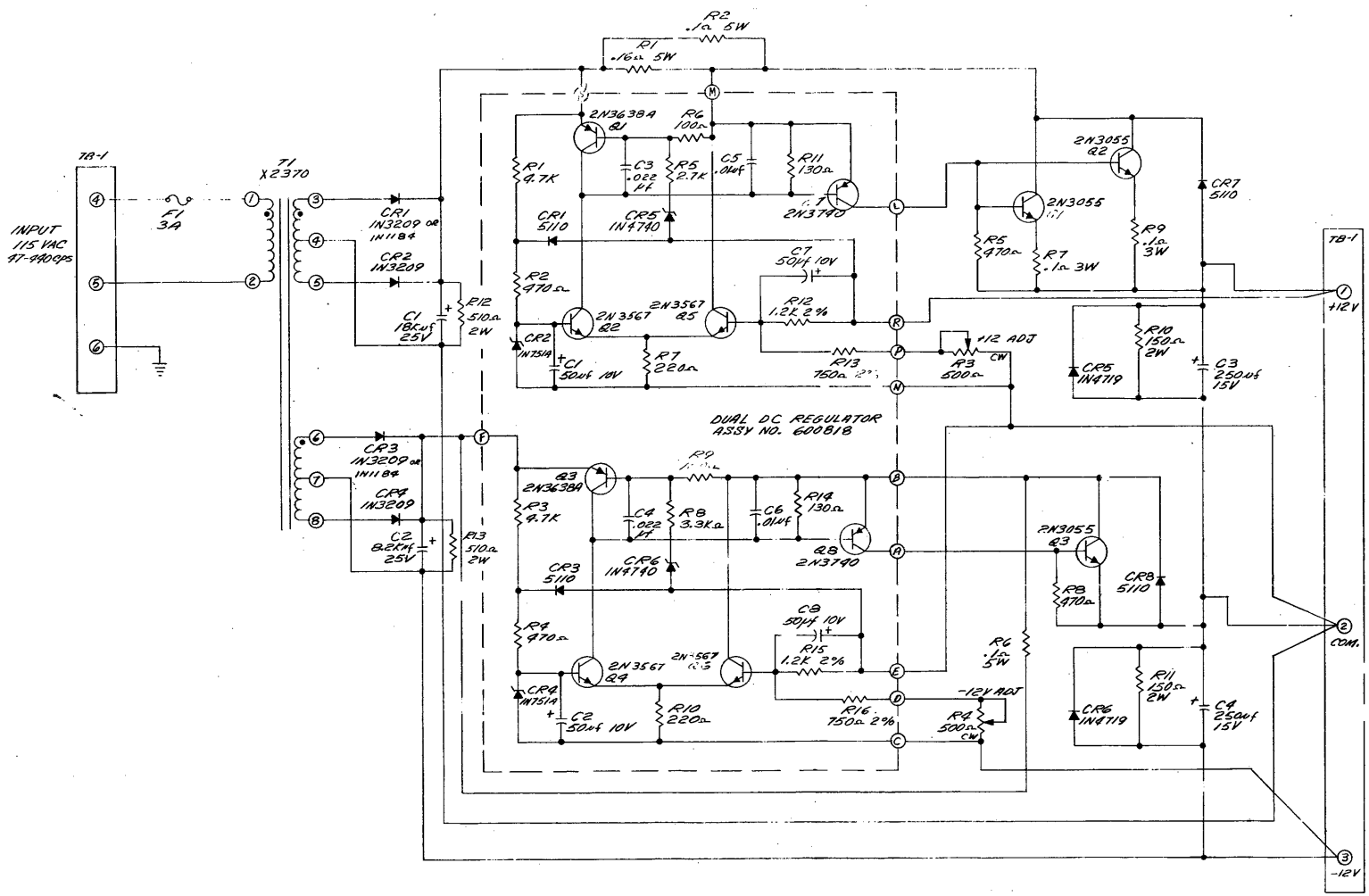
MASTER BILL OF MATERIAL FOR S1070

Modular Devices — Output 2 -12V 4A

SHEET 1 OF 1 REV

Notes & Part No	Part Name & Description	MFG	MFG Part No
R1	10 ohms ½W 10%		
R2	1.2K 2W WW		
R3	470 ohms " "		
R4	" " "		
R5	3.3K ½W 10%		
R6	10 ohms ½W 10%		
R7	2.2K " "		
R8	" " "		
R9	Not used		
R10	330 ohms ½W 10%		
R11	680 ohms " "		
R12	" " "		
R13	330 ohms " "		
R14	10 ohms " "		
R15	15K " "		
R16	Not used		
R17	Not used		
R18	Not used		
R19	Not used		
R20	10K ½W 10%		
R21	2.2K " "		
R22	680 ohms " "		
R23	" " "		
R24	" " "		
R25	" " "		
R26	Not used		
R27	250 ohms POT Carbon	Mallory	
R28	10K ½W 10%		
R29	" POT Carbon	Mallory	
R30	2.2K ½W 10%		
R31	" " "		
R32	1.5K 2W WW		
R33	Not used		
R34	100 ohms ½W 10%		
R35	Not used		
R36	Not used		
R37	1K ½W 10%		

Notes & Part No	Part Name & Description	MFG	MFG Part No
R101	500 ohms POT WW		
R102	0.1 ohms 5W WW	PW-5	
R103	6.8K 1W 10%		
CR1	IN 752		
CR2	Not used		
CR3	Not used		
CR4	IN 752		
CR5	IN 3253		
CR6	IN 3253		
CR7	IN 3253		
CR8	IN 3253		
CR9	IN 752		
CR Bridge	Rectifier Bridge	Sem Tech	SCBA-1
Q1	2N697		
Q2	2N697		
Q3	2N697		
Q4	2N697		
Q5	2N697		
Q6	Not used		
Q7	2N 697		
Q8	2N697		
Q9	2N697		
Q101	2N3055		
Q103	2N3055		
T101	Transformer	PT 252A	
C2	.02 MFD 20 VDC		
C4	.001 MFD 20 VDC		
C102	1000 MFD 15 VDC	C-D	
C103	9000 MFD 50 VDC	Sprague	
C104	100 MFD 50 VDC	C-D	
C106	0.02 MFD 20 VDC		



CALIBRATION NOTE

1. CHECK SHORT CIRCUIT CURRENT FOR LIMITS OF 2 TO 3 AMPS AT THE +12VDC OUTPUT. ADJUST R5 IF LIMITS ARE NOT MET.
2. CHECK SHORT CIRCUIT CURRENT FOR LIMITS OF 2 TO 3 AMPS AT THE -12VDC OUTPUT. ADJUST R8 IF LIMITS ARE NOT MET.

SCHEMATIC POWER SUPPLY +12V-12V AMC-M-205

ASTRO METRIX CORP

D 100523

23096

ASTRO-METRIX CORP PARTS LIST

ITEM	QUAN.	PART NO.	REF DESIG	DESCRIPTION	VENDOR OR SPEC.
1	1	600821		Chassis Assy	AMC
2	1	600818	A1	Circuit Board Assy	AMC
3	1	100523	Ref	Schematic	
4	1			Bracket - Capacitor 2 1/16 2 Leg	
5	1			Bracket-Capacitor 1 7/16 2 Leg	
6	1	600822		Terminal Cover	AMC
7	3	NC421A		Heat Sink	Wakefield
8	6	113		Heat Sink - Bracket	Wakefield
9	12	103		Teflon Insulator	Wakefield
10	1	36D183G025BC	C1	Capacitor 18K uf 25V	Sprague
11	1	36D822G025AC	C2	Capacitor 8.2Kuf 25V	Sprague
12	2	TE1165	C3	Capacitor 250uf 15V	CDE
13	X	TE1165	C4	Capacitor 250uf 15V	CDE
14	4	IN1184 OR IN3209	CR1	Diode	
15	X	IN1184 OR IN3209	CR2	Diode	
16	X	IN1184 OR IN3209	CR3	Diode	
17	X	IN1184 OR IN3209	CR4	Diode	
18	2	IN4719	CR5	Diode	Mot
19	X	IN4719	CR6	Diode	Mot
20	2	5110	CR7	Diode	AMC
21	X	5110	CR8	Diode	AMC
22					
23	1	3AG-3 Amp	F1	Fuse - 3A	
24	1	4405	XF1	Fuse Holder	Little Fuse
25					

TITLE: POWER SUPPLY ASSY +12V-12V AMC-M-245	COMPILED BY: 4/6/67 R. Zega	DATE RELEASED:
	CHECKED BY:	PAGE 1 OF 2
	APPROVED BY: 4/7/67	DWG NO: 100525 A

ASTRO-METRIX CORP PARTS LIST

ITEM	QUAN.	PART NO.	REF DESIG	DESCRIPTION	VENDOR OR SPEC.
26	3	2N3055	Q1	Transistor	
27	X	2N3055	Q2	Transistor	
28	X	2N3055	Q3	Transistor	
29					
30	3	2TS-3		Transistor Socket	C-J
31					
32	1		R1	Resistor .16Ohm 5W Axial	
33	2		R2	Resistor .1 Ohm 5W Axial	
34	2	TT-4	R3	Resistor Pot 500 Ohm	Cent
35	X	TT-4	R4	Resistor Pot 500 Ohm	Cent
36	2	RC20GF471J	R5	Resistor 470 Ohm 1/2W	Mil-R-11
37	X		R6	Resistor .1 Ohm 5W Axial	
38	2		R7	Resistor .1 Ohm 3W Axial	
39	X		R8	Resistor .1 Ohm 3W Axial	
40	X	RC20GF471J	R9	Resistor 470 Ohm 1/2W Axial	Mil-R-11
41	2	RC42GF151J	R10	Resistor 150 Ohm 2W	Mil-R-11
42	X	RC42GF151J	R11	Resistor 150 Ohm 2W	Mil-R-11
43	2	RC42GF511J	R12	Resistor 510 Ohm 2 W	Mil-R-11
44	X	RC42Gf511J	R13	Resistor 510 Ohm 2 W	Mil-R-11
45	1	X2370	T1	Transformer	AMC
46					
47	1	6-141-Y	TB1	Terminal Strip	C-J
48	1	MS6-141		Terminal Strip Marker	C-J
49	1	15 PIN SINGLE ROW	J1	CONNECTOR, PRINTED CIRCUIT	C-J EQUIV.
50					

TITLE: POWER SUPPLY ASSY
+12V -12V
AMC-M-245

COMPILED BY: 4/6/67 R. Zega
CHECKED BY:
APPROVED BY: 4/12/67

DATE RELEASED:
PAGE 2 OF 2
DWG NO 100525 A

The following table provides fuse information for the Modular Devices power supplies used in the 620/i computer.

Power Supply Model	Fuse Application	Fuse Value and Type
S1063	AC Input	2 amp, 3AG Quick Acting[1]
S1070	AC Input	3 amp, 3AG Quick Acting
S1003 (Integrated)	AC Input	5 amp, 3AG Quick Acting[2]
S1003 (Integrated)	-5 Volt Output	3 amp, 3AG Quick Acting

NOTES:

1. Use of a 10 amp, 3AG quick acting is approved when a 3 amp 3AG quick acting is used in series externally.

2. Was 8 amp. Manufacturer now recommends the use of 5 amp. The fuse holder markings on all supplies to date (March 1969) still indicate 8 amp.