WinSystems®

STD BUS

Numeric Index

Ordering Information

Placing an Order

Orders should be placed with WinSystems, Inc. at the following location:

WinSystems, Inc.
715 Stadium Drive
Suite 100
Arlington, Texas 76011
Phone: 817-274-7553
FAX: 817-548-1358

All orders should have the complete model number, quantity, purchase order number, a bill-to address, ship-to address, method of shipment, desired ship date, Federal Tax ID #, and for Texas customers include the sales tax exempt ID number. Orders are subject to acceptance in writing by WinSystems, Inc.

Outside the USA

In countries without a WinSystems' sales representative, orders may be placed by guarantee of payment in US dollars such as letters of credit, sight draft or advance payment.

Terms

Terms with prior credit approval are net 30 days from the date of invoice. Credit must be established prior to shipment. WinSystems, Inc. maintains the right to require partial or full payment in advance if the financial condition of the Buyer does not warrant net terms. A MasterCard, VISA, money order, certified check, or company check is accepted for prepaid orders.

Prices

All prices are in U.S. dollars and F.O.B. Arlington, Texas. Applicable federal, state, and local taxes are extra and paid by the buyer. Prices are subject to change without notification.

Discounts

Quantity and OEM discounts are available on an order or contract basis. Consult the WinSystems' Sales Department for details.

Product Availability

WinSystems' normal delivery for most products in quantities of less than ten is stock to two weeks after receipt of order. Shipping dates are approximate and are based upon prompt receipt by WinSystems of all necessary information. Partial shipments may be made unless instructed otherwise.

Shipping

All products are shipped in rugged containers suitable for ensuring safe delivery under normal shipping conditions. Unless otherwise directed, all products are shipped via UPS or Federal Express. Depending upon the shipping method, charges are collect or prepaid and added to the invoice.

Product Demonstration

The STD-AT and other WinSystems' products are best evaluated through demonstrations. If you would like a demonstration or a 30-day evaluation unit, call WinSystems' Sales Department.

Technical Support

WinSystems' has an Applications Engineering staff to answer your technical questions concerning hardware, software, and systems products and configurations both before and after purchase. Please call 817-274-7553, FAX 817-548-1358, or write your questions to the Applications Engineering Department.

24-Hour Bulletin Board

A WinSystems' Electronic Bulletin Board System is accessible 24 hours a day. It offers on-line technical support, application articles, and example code. Modem transmissions speeds supported are 300, 1200 or 2400 baud. The communication settings are: 8-bits, no parity, and one-stop bit. The phone number is 817-861-8739. If you have trouble gaining access to the bulletin board, call 817-274-7553 and ask for the Applications Engineering Department.

Federal Supply Code

WinSystems' CAGE/FSCM number is 1AU87.

Facsimile Transmission

WinSystems' FAX machine is capable of supporting CCITT G3, G2, and North American FM compatibility. The direct telephone number is 817-548-1358.

STD BUS
DATA BOOK

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WinSystems, Inc.

WinSystems, Inc.

A Message from the President

To Our Customers:

In response to the challenge of the 90's, we are proud to furnish our latest catalog of STD Bus products representing over a decade of growth and development for the ever changing STD Bus marketplace.

We thank you, our customers, for your role as "partners" in development, and for your input and response to our commitment to customer oriented, superior innovation and highest quality products at a competitive price.

We pledge to continue this commitment to you.

Sincerely,
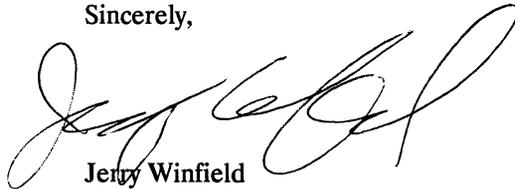
Jerry Winfield
President

STD BUS Data Book

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General Information

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WinSystems

Since its founding in 1982, WinSystems has designed and manufactured a wide range of STD and CMOS STD Bus products. The company has gained an excellent reputation for innovative design and engineering skills and has become recognized as a leading supplier of STD Bus products.

WinSystems' products and customer support are superior in many areas:

- Full range of product solutions. WinSystems offers solutions from high-end 80486 fully compatible PC-AT systems to low cost single board computers running the ROM-DOS embedded operating system.

- Software Solutions. WinSystems supports PC-compatible operating systems, networks, and development tools to allow the customer to quickly and easily design, develop and debug applications. WinSystems also offers drivers for selected I/O cards, and example start-up code and application examples to facilitate the programmers' job.

- Ruggedized Design. WinSystems' products are designed and manufactured to lead performance and reliability standards. Our LPM series of CMOS product will operate from battery power and at temperature extremes from -40° to +85° Centigrade.

- Total Engineering Support. Every customer's application is unique requiring special solutions. WinSystems' Applications Engineers standby their customers with assistance before, during, and after the installation is complete.

The STD Bus

In the late 1970s, Mostek and Pro-Log Corporation developed the STD Bus in a joint effort to produce a reliable, electronic data bus for industrial applications. Jerry Winfield, President of WinSystems, was the system architect for Mostek of the STD Bus who defined and developed the first products ever introduced to this industry standard.

The STD Bus is the approved, IEEE-961 standard microcomputer bus which is popular worldwide with over 150 manufacturers. The STD Bus has a number of advantages over other bus architectures used in industrial applications such as the PCBus and Multibus. Its simple interface, smaller card size (4.5" x 6.5"); solid, nearly square peripheral cards, and strong card mounts tolerate shock and vibrations, making the STD Bus ideal for rugged industrial environments.

The STD system is also more modular than existing busses because its smaller cards contain fewer functions. This allows systems designers and integrators to select precisely the functions they need. In addition, the card is less expensive -- an important consideration in industrial and OEM markets.

The STD Bus has evolved from 8-bit 8085/Z80 performance to 16/32-bit PC/AT minicomputer performance levels while retaining compatibility with the earliest product designs. This migration path philosophy protects the user's time and hardware investment. This continuity is important in applications where a long product life cycle and assured source of supply is required.

The STD Bus has an active manufacturers' group, STDMG, (which WinSystems supports and is an active member) to monitor standards, specifications, and new technical developments which assures an orderly, evolutionary growth. This evolution has occurred by adapting to newer technologies for higher performance and more cost-effective solutions. The net result is a lasting standard for industrial applications that will work with bus products today and in the future.

Quality

WinSystems' manufacturing expertise and aggressive quality control have produced a respected line of STD Bus products known for their reliability and their tolerance of the rigors of industrial, military and scientific applications. WinSystems demands the highest quality workmanship standards in all of its products. All elements of the product from design, layout, fabrication, testing, and inspection are carefully checked and monitored for conformance to standards. The boards and systems are burned-in and tested before shipping.

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Drawing from our application-focused engineering expertise, we have developed an inventory of hardware "building blocks" which can be configured into products which solve industrial automation problems in response to your specific needs. We offer a wide variety of both software and hardware on the STD Bus and non-bus single board computers. The products exhibited throughout this catalog can be configured in many different ways to provide specific solutions to your needs.

We think it's important to look at our products from the customer's perspective. Feedback from our customers on their current and future requirements is integral to our product planning and development. In fact, every product in this catalog was directly influenced by our customers.

IEEE 961 STD Bus

We are a full line supplier of the industry standard IEEE 961 STD products. Our "MCM" product line includes 8-bit to 32-bit CPUs, memories, I/O, and special function cards. A wide selection of backplanes, card cages and card cages with power supplies complement the over 150 different WinSystems' STD Bus cards.
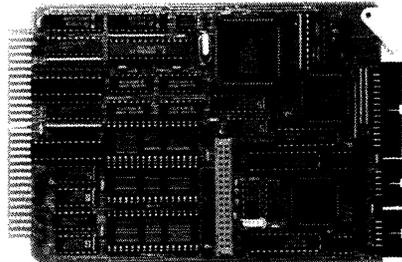
CMOS STD Bus

We are also the largest supplier of CMOS STD Bus products in the world with our "LPM" Series of boards. CMOS is needed in harsh environments where low power, wide temperature operation (-40° to +85°C), supply voltage tolerance (+10%), and high electrical noise immunity are required. Low power means low system operating temperatures, no fans, smaller power supplies, and sealed enclosures to meet the rigors of the factory floor.
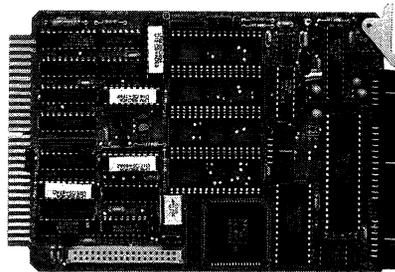
Replacement Products

We offer over 100 replacement boards for the most popular Mostek (Mizar), Analog Devices, Pro-Log, and DY-4 STD and CMOS STD Bus cards. This option provides you with a cost-effective alternative when price, delivery, and continued support is critical. Also, we offer a 30-day trial evaluation period for these plug replacement cards so that you can have a no risk comparison of these products.
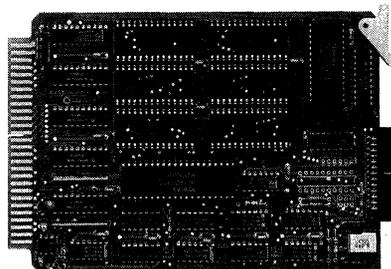
STD-AT Systems

Our STD-AT is a true PC-AT software compatible, rugged, industrial computer on the STD Bus. It combines the powerful processing capability of the 80286/386/486 and vast library of PC-DOS software with the reliability and industrial I/O interfaces of the open architecture IEEE 961 STD Bus. This PC compatibility provides you with the ability to use the extensive pool of PC applications software, utilities, networking, and development tools without modification. The result is a completely AT-compatible system with CPU operational speeds from 10 to 50 MHz.
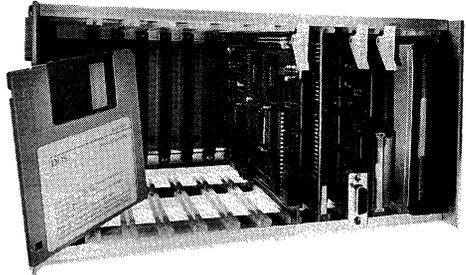
Single Board Computers

We offer a number of single board computers for special applications requirements. These are units that are optimized for low cost and high functionality. The SBC25 and SBC88 are two non-STD Bus products. We also offer a number of STD and CMOS STD Bus Single Board Computers (SBCs) that can function in a standalone mode without the need for additional I/O or memory cards for embedded systems applications. We are a manufacturer of standard products but we additionally welcome the opportunity to examine special configurations to your existing product modifications or totally new designs of SBCs.
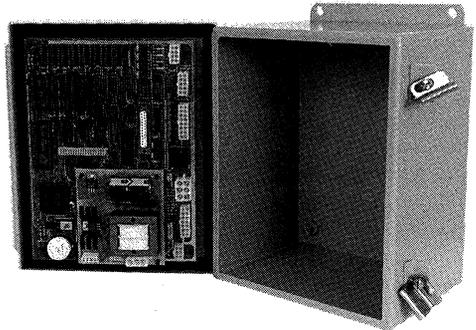
SBX Multimodules

Our SBX cards are small (3.7" x 2.85") specialized, I/O mapped boards that plug into a host via the IEEE P959 Bus. These cards enable you to economically expand or modify a system with a standard product while obtaining maximum performance. These SBX boards can be used on our STD Bus, CMOS STD Bus, SBCs, and Multibus boards as well.
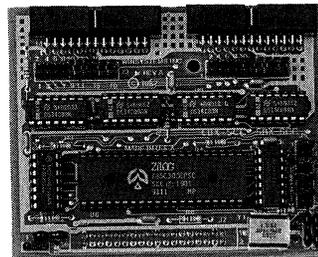
80486DX/SX SBC

The MCM-486DX offers up to a 50 MHz micro-processor which comes equipped with a maximum of 8 Mbytes of onboard parity-protected DRAM configured. With an onboard Mosel MS401 32/64-bit data-path chip, automatic interleaving creates an effective 64-bit-wide memory bus. The 64-bit data path permits one-clock burst reads and memory post-write operations to nearly double the memory accesses compared with just using 32-bit data paths. This capability offers lower cost and high performance in non-cache modes. (See page 4-5)
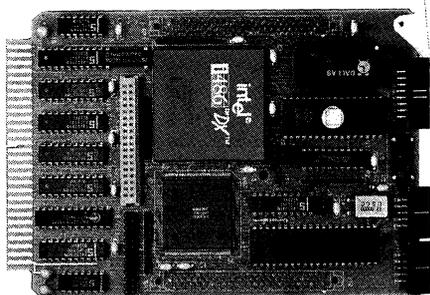
Low Cost 80386SX SBC

The LPM/MCM SX386 is an unbeatable multi-purpose board for use with either a STD Bus system or as a standalone controller with PC/104 expansion modules. It is fully functional for industrial applications and will run without disks, keyboard, or monitor. It is designed for applications where PC power and performance are needed in a small system, but offers rugged hardware suitable for operation in harsh or remote environments. (See page 4-39)
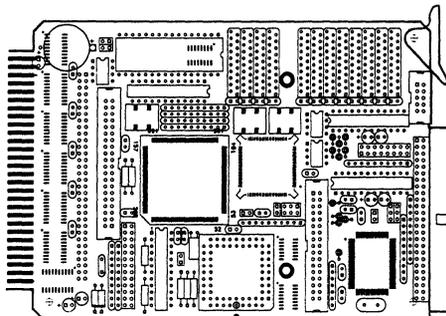
Digital Signal Processor

Our new MCM-DSP32C single board processor can handle computation-intensive embedded applications at the high speed of a DSP chip. It plugs into a STD Bus, and its 32-bit architecture operates at a clock frequency of 50 MHz. In key benchmark tests, this board can execute a 1024-point complex FFT in 3.3 msec, multiply two 4x4 matrices in 6.16 microseconds, and compute the response of a complex adaptive FIR filter in real-time at 80 nanoseconds/tap. The MCM-DSP32C offers a high performance and cost effective solution to many traditional and emerging signal-processing applications. (See page 4-35)
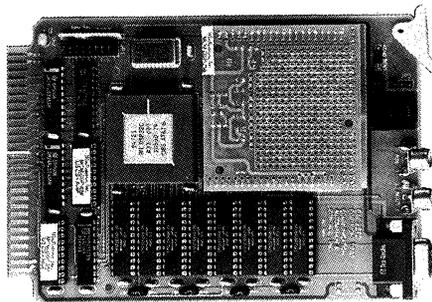
Low Cost V-53 SBC

Bringing IBM PC/AT performance to the STD Bus, the LPM/MCM-SBC53 is a high performance, 16-bit, V53 STD Bus single board computer designed for harsh embedded applications where small size, economical prices, and 80286 performance are required. It combines the most popular I/O functions used in most applications onto a single card. And it dissipates a maximum of only 1.5W. The combination of the CPU and peripheral mix makes it ideal for high performance data control applications. (See page 4-41)
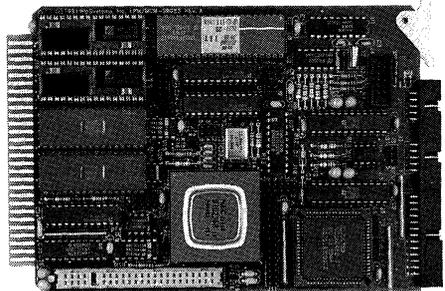
Real-Time Embedded O.S.

QNX is a distributed processing real-time multiuser and multi-tasking operating system which is now available on our industrial STD-AT systems. It can operate on a network or as a standalone unit. Configurations vary from small diskless embedded systems to complete rack mounted disk-based systems with graphics. The combination provides you with the perfect blend of software and hardware platforms designed for use in factory automation and harsh industrial environments. (See page 3-13)
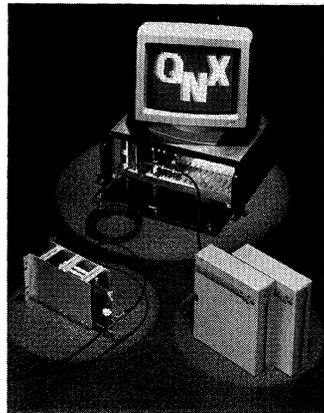
Flat Panel/CRT VGA Controller

The LPM/MCM-FPVGA is a versatile LCD VGA controller that provides support for basic VGA modes for an LCD or CRT, and extended 800 x 600 resolution graphics on the CRT. It provides excellent display quality, with up to 64 shades of gray on monochrome Super-Twist Nematic (STN) LCD panels and a direct connection capability for active matrix color LCD panels. The board can display on the flat panel and on an VGA CRT simultaneously. (See page 6-31)
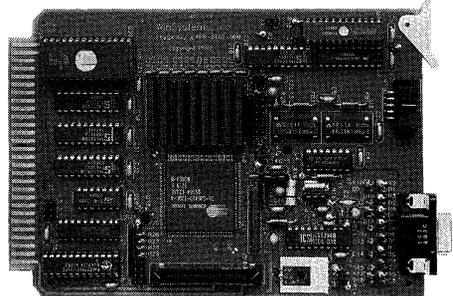
Flat Panel Controller

The LPM/MCM-FPC is a low cost universal display card that functions as a flat panel display controller. CGA, Hercules and MDA graphics modes are supported. An onboard state machine performs auto-initialization, thereby eliminating the need for special driver software. Based upon the Yamaha V6366, the LPM/MCM-FPC will support all three flat panel display technologies (EL, Plasma, and Liquid Crystal) with full text and graphics. (See page 6-29)
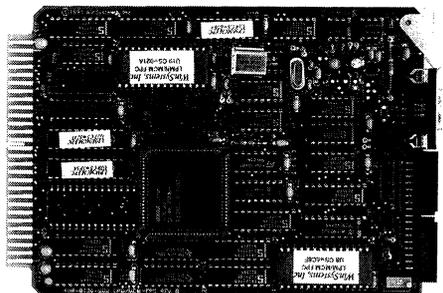
Keyboard/LCD Interface

The LPM/MCM-KYBLCD board is well suited for applications where both an inexpensive keyboard and LCD interface are needed — such as system control, data entry, status display, and operator prompting. It is also useful for system development, testing and training applications. It supports 4 x 4 or 5 x 4 matrix keyboard inputs and 1 to 4 line parallel LCD displays with up to 80 characters from companies such as Hitachi, Epson, Seiko, Densitron, Sharp and others. (See page 6-111)
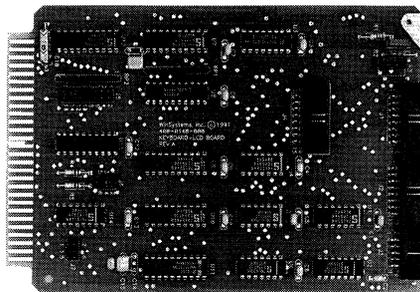
IEEE-488 Controller

Designed to meet all of the control specifications required for talker, listener and controller as specified by IEEE 488-1978, our LPM/MCM-488 is an IEEE-488 interface board for the STD Bus. This interface makes possible the transfer of data between thousands of IEEE-488 compatible devices. The board is based upon the NEC 7210 allowing its use with STD Bus DOS compatible and ROM-DOS embedded STD Bus systems. (See page 6-49)
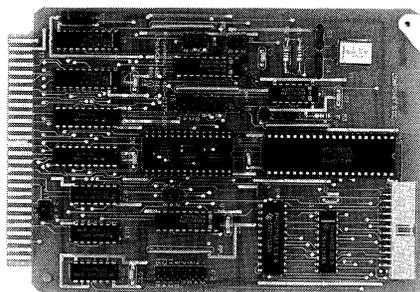
Racks and Backplanes

The CX Series is a new line of STD Bus card racks and backplanes. Based on 0.625" centers with vertical card orientation to take advantage of convection cooling, the CX card cages allow either a smaller enclosure size or provide more card slots when compare to other card cages. They are available in 3- to 26-slot versions in 3-slot increments. In addition, 50W or 100W power supplies are available to power the racks. Backplanes support high-performance STD Bus processors, including the new 16/32-bit types with full 16-bit data transfers. (See page 7-15)
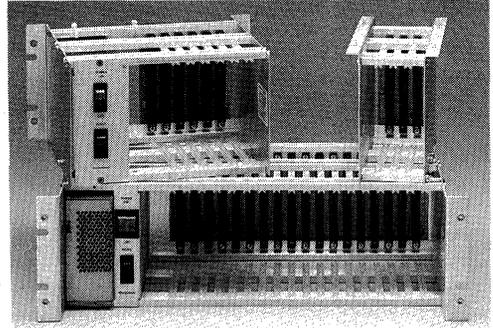
STD Bus Enclosures

Our STD Bus enclosures provide a foundation for STD DOS XT/AT and non-DOS embedded systems. They serve as a platform for industrial computer based products, enclosures for self-contained OEM systems, or as a prototyping shell for systems development. They are user configurable since the CPU, I/O and memory boards, disk drives, power supplies can all be added to the unit to customize it to the specific application. (See page 7-27)
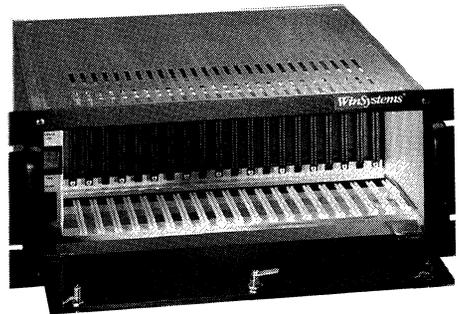
12-Bit SBX A/D card

The SBX-A/D12 card provides up to eight channels of 12-bit analog input on a single SBX module. Any channel can be configured as unipolar or bipolar for maximum flexibility. The board is designed to serve as a complete data acquisition system with a 100KHz sampling rate. (See page 9-3)
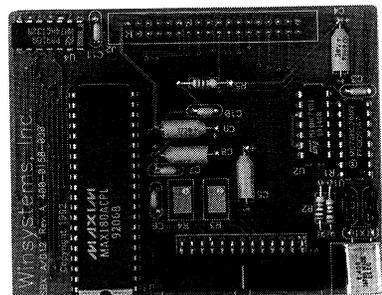
Opto-22 Rack Interface SBX Card

The SBX-OPTO is a compact, SBX multimodule, general purpose 48-line parallel I/O controller based upon two 82C55A Programmable Peripheral Interface (PPI) devices. These lines are organized as 2 groups of three 8-bit I/O ports that interface directly to 2 independent industry standard 4, 8, 16, and 24-I/O module mounting racks (Opto-22, Gordos, etc.). (See page 9-7)
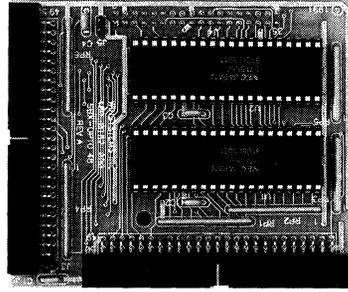
21 Megabyte Floptical Disk Drive

Providing hard disk storage capacity with the removable, low cost convenience of a floppy, the FD3-21M is a high capacity floppy designed for escalating storage demands. It combines optical and magnetic recording technologies to achieve very high capacities (21 MB), yet still reads and writes 3.5" double density (720 KB) and high-density (1.44 MB) floppy disk formats. (See page 6-23)
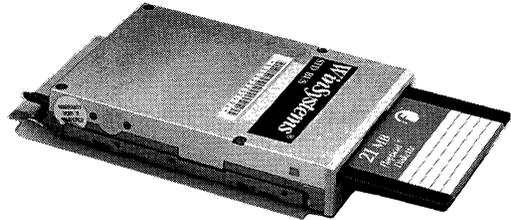
Disk I/O Support Controller

The LPM/MCM-DSKIO is a general purpose DOS system support card for use with the LPM/MCM-SBC41, LPM/MCM-SBC53 and other V40/V53 class CPUs. The card provides the peripheral interface electronics for floppy and hard disks, keyboard interface, real time clock, and BIOS ROM extension socket. It allows embedded SBCs to be configured to work with rotational media for complete PC-software compatible systems. (See page 6-11)
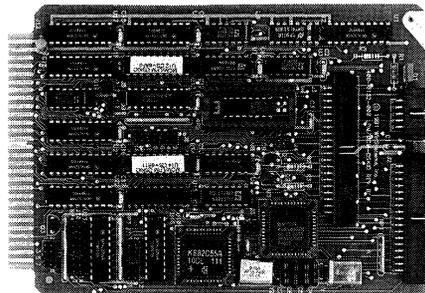
Universal Solid State Disk

Our LPM/MCM-USSD is an I/O mapped, universal STD Bus Solid State Disk (SSD). It can be populated by the user with up to 4 megabytes of RAM, EPROM, or PEROM (Flash). And four cards can be grouped for 16 MByte of SSD. The card allows you to substitute onboard semiconductor devices in applications where the environment is too harsh for mechanical hard disks or floppy disk drives, plus it has significant speed advantages. It is designed to store programs and data for applications such as data collection and logging, diagnostics, etc. (See page 6-19)
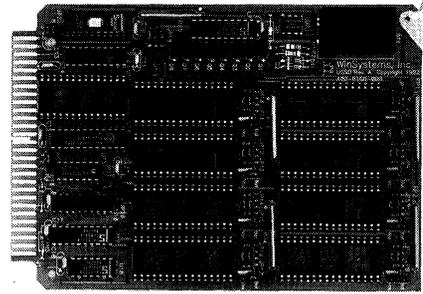
Integrating A/D Converter

The LPM/MCM-7109 is a very low cost, 12-bit (plus sign) integrating A/D converter for use in data acquisition and control applications. A dual slope integrating converter provides the benefits of high frequency noise reduction through signal averaging while offering a rate of up to 30 conversions per second. (See page 6-87)
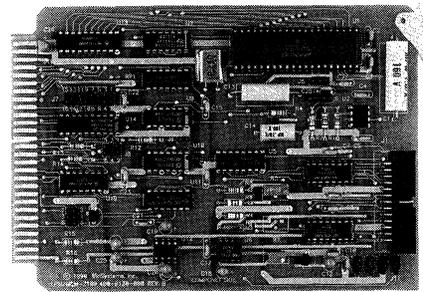
Analog and Digital Termination Boards

Our series of termination boards provide both connection and signal conditioning from field wiring to our STD Bus I/O cards and standalone single board computers such as the SBC25 and SBC88. For ease of mechanical layout and packaging, all termination boards are the same size (only 4.1" x 5.65") and mounting style, offering excellent configuration flexibility. (See page 7-47)
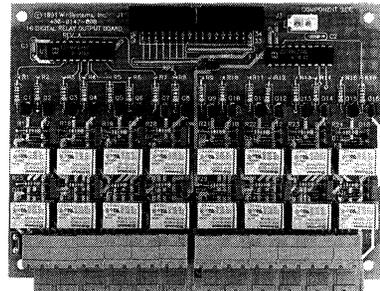
In addition to our standard products, we welcome the opportunity to examine and quote special purpose product designs, modifications, configurations and packaging. These opportunities may involve small modifications to existing cards, to complete designs of totally new STD Bus and non-STD Bus products such as CMOS STD Bus, CMOS PC Bus or other standalone single board computers.

Examples of special product configurations are as followings:

    Special card cage mounting configurations
    Power supplies in card cages
    Card cages with no motherboards
    Card cages with multiple motherboards
    Cards with all sockets
    Cards with special latching connectors
    Special memory card decode options

Contact our Marketing Department so that a quote for specialized product configurations, special packaging or additional products can be obtained.

MACHINE TOOL SOCKETS

We use production double leaf low profile dip sockets for selected NMOS and TTL devices on the PC boards. These give 100% more contact area than the regular single leaf sockets used by other STD manufacturers; however, certain applications require an even higher quality socket. We can supply machine tool sockets which have pin sockets for high reliability and high retention. This type of socket design gives the best gripping action on the integrated circuit and is used where extra protection is needed from extreme shock and vibration.

CONFORMAL COATING

Our boards can be coated with a transparent lacquer type material to protect the boards against air, dirt, oxidation, water, salt spray, acids, alkalais and fungi. This material is ideal for protection of these boards in harsh environments. It is non-conductive, nonflammable, and has a low order of toxicity.

It has a dielectric strength of 1500 volts/mil. Furthermore, it does not attack plastic, rubber, paints, or metals and facilitates compliance with environmental OSHA standards. We use a Miller-Stephenson chemical MS-470 urethane coating that meets MIL-I46058C type UR. It is applied as an aerosol. Spot recoating of areas is quick and easy. It contains an ultraviolet indicator that is visible under U.V. light for inspection purposes. The coating can be readily removed with MS-114 Stripper.

PIN-AND-SOCKET CONNECTORS

Some customers' applications require pin-and-socket connectors rather than the regular edge STD Bus card connectors for certain hardened and non-tactical military environments. We have adapted selected boards and backplanes to support a 56-pin military grade M55302/57 connector.

The combination of this connector with our industry standard CMOS STD Bus architecture provides the best performance, reliability, and cost-effective solutions if a Mil-Spec computer is not required. Compared to equivalent Mil-Spec solutions, this approach is over 20 times less expensive. We have chosen the MIL-55302 for these reasons:

- Pin-and-socket connectors
- Low insertion and extraction force
- High reliability closed entry socket
- Multiplicity of pin-to-socket contact points
- 5 amps current per pin
- Low contact resistance due to greater average contact area
- Unsurpassed shock and vibration characteristics
- Superior performance to DIN 41612-style connectors
- Optional polarization keys
- Multiple sources for connectors
- Easy modification to existing PCB designs

Pin-and-Socket Connector - The MIL-55302 type connector is a dual row, high density interconnection system on 0.100 inch centers. This differs from the STD Bus 0.156 inch standard. The interconnect system has polarizing shrouds to prevent plugging the card in backwards. The STD Bus board is lengthened by 0.25 inches and a male connector has been added.

Card Dimensions - The circuit card is now 4.5 x 6.75 inches. This length dimension is increased by 0.25 inches from the standard STD Bus 4.5 x 6.5 inch card. The additional length permits a designer to use the same basic card design artwork and choose either a card edge or pin-and-socket connector.

Polarization - The construction of the connector along with the mounting of the STD Bus card guides prevents boards from being plugged in backwards. Optional polarization pin hardware allows keying of the individual card to a specific slot on the backplane for maximum safety.

Ordering information - Contact our application engineers for more information about this XIM product family.
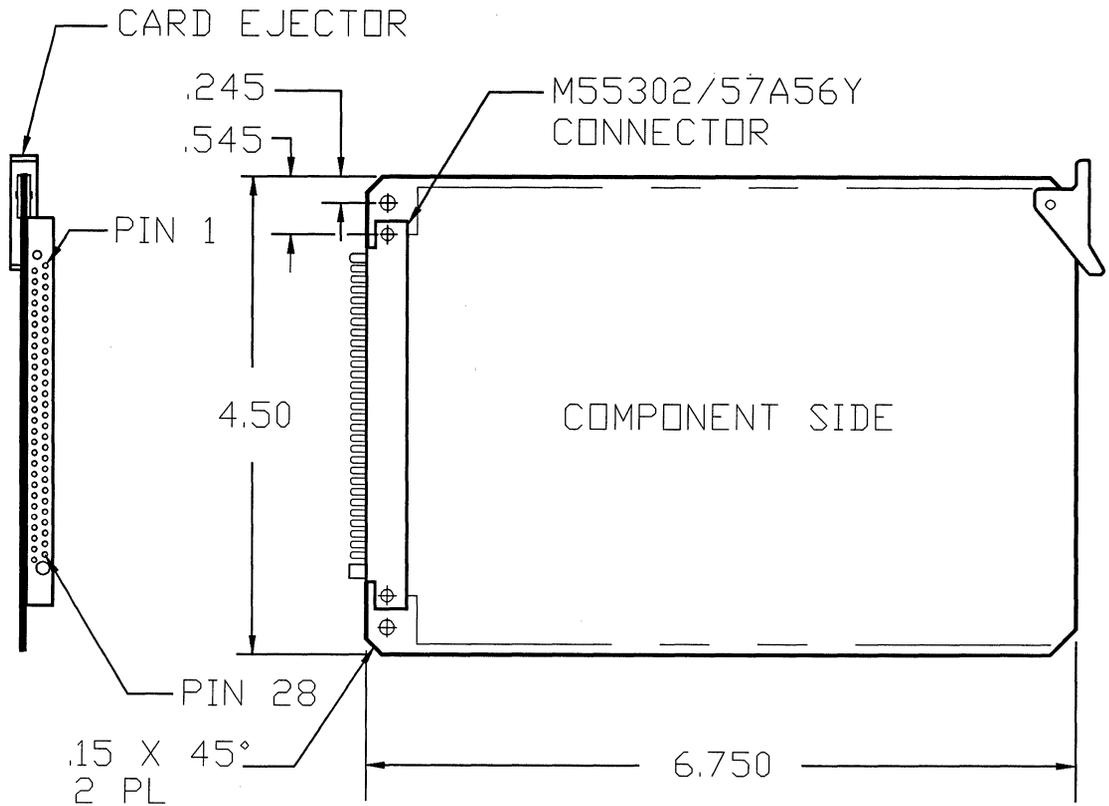
Warranty

WinSystems warrants products manufactured by WinSystems against defects in materials or workmanship for two years from the date of purchase from WinSystems. This limited warranty is subject to the following terms and conditions:

A. If the product has defects in materials or workmanship, WinSystems will repair or replace the products, at WinSystems' sole option, at no charge to you for the duration of this warranty.

1. To obtain service under this warranty, obtain a return authorization number (RMA). In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.

2. You must send the product postage prepaid and insured. You must enclose the product in an anti-static bag to protect it from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.

B. This warranty does not apply to any products which have been modified, altered or tampered with; to any products which have been subject to abuse, accident, improper installation or misuse; to any products whose serial numbers have been removed; or to any products which have been repaired or serviced by other than an authorized representative of WinSystems.

C. This warranty does not extend to and shall not apply to products or components of systems not manufactured by WinSystems. Products not manufactured by WinSystems are limited to the warranty provided by the original manufacturer.

D. For the repair or replacement of any products not covered by this warranty, WinSystems will repair or replace such products, at WinSystems' sole option, at WinSystems' current charges for labor and materials.

E. THERE ARE NO WARRANTIES BY WINSYSTEMS EXCEPT AS STATED HEREIN. THERE ARE NO OTHER WARRANTIES EXPRESSED OR IMPLIED INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND OF FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL WINSYSTEMS BE LIABLE FOR CONSEQUENTIAL, INCIDENTAL OR SPECIAL DAMAGES INCLUDING, BUT NOT LIMITED TO, DAMAGES FOR LOSS OF DATA, PROFITS OR GOODWILL. WINSYSTEMS' MAXIMUM LIABILITY FOR ANY SUCH BREACH OF THIS AGREEMENT OR OTHER CLAIM RELATED TO ANY PRODUCTS, SOFTWARE, OR THE SUBJECT MATTER HEREOF, SHALL NOT EXCEED THE PURCHASE PRICE OR LICENSE FEE PAID BY CUSTOMER TO WINSYSTEMS FOR THE PRODUCTS OF SOFTWARE OR PORTION THEREOF TO WHICH SUCH BREACH PERTAINS.

Life Support Policy

WINSYSTEMS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF WINSYSTEMS CORPORATION. As used herein.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonable expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WinSystems offers a growing line of over 90 plug replacement cards for the most popular Mostek (Mizar), Pro-Log, Analog Devices, DY-4, and Data Translation STD and CMOS STD Bus cards. Processor, memory, I/O cards and card cages are included in the list. The concept of a generic alternate source of product was begun by WinSystems to give the customer a choice of vendor.

The real benefit to the volume users of industrial standard STD Bus products is that another source of supply can be secured without costly redesign or lengthy evaluation cycles. This provides a cost effective alternative when price, delivery, and continued support are critical.

WinSystems, Inc. offers a free 30 day trial evaluation period for its plug replacement cards. This allows a no risk comparison of the product. Contact WinSystems' for further information on this program.

WinSystems has defined two categories of replacement boards: Functional and Nearest Replacement. They are defined as follows:

Functional Replacement: Suggestions are based upon the similiarity of mechanical and electrical characteristics as reported by the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications and programming considerations.

Nearest Replacement: Suggestions are based on the similarity of electrical characteristics as reported in the manufacturer's published data. Interchangeability is not guaranteed as these parts usually have slightly different I/O pin configurations and/or programming considerations. Before selecting a device as a substitute, compare the specifications. Since STD bus designs vary widely, it is possible that similar boards from two or more manufactures will satisfy an application. Therefore slight mechanical or electrical variations should not disqualify the nearest equivalent.

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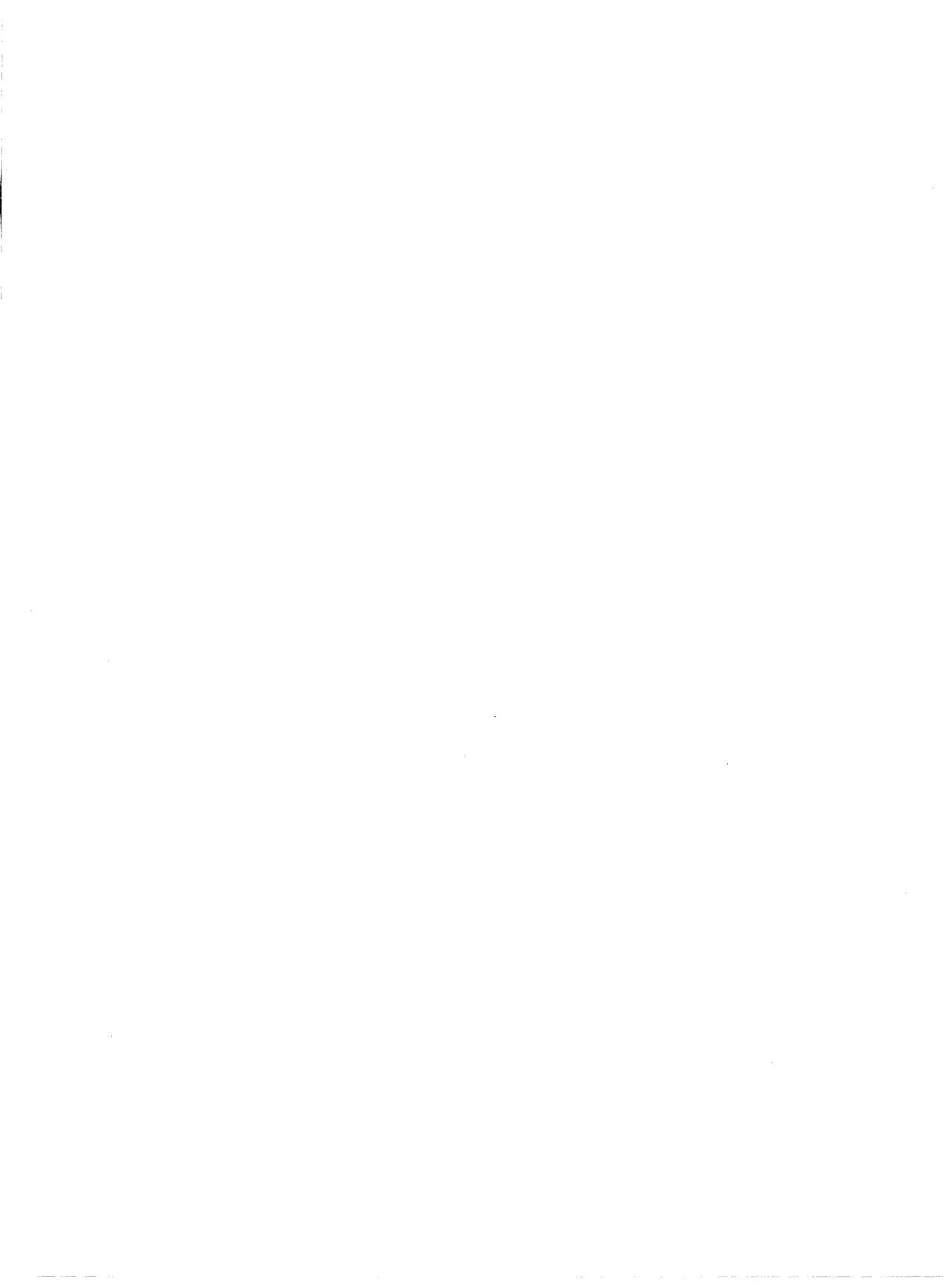
CROSS REFERENCE/INTERCHANGEABILITY GUIDE

Manufacturer's Product	Functional Replacement	Nearest Replacement	Manufacturer's Description
MOSTEK (Mizar)			
MK77650-00	MCM-PIO		MDX-PIO; 2.5 MHz
MK77650-04	MCM-PIO		MDX-PIO-4; 4 MHz
MK77651-00	MCM-SIO2		MDX-SIO; 2.5 MHz
MK77651-04	MCM-SIO2		MDX-SIO; 4.0 MHz
MK77666	MCM-D/A8		MDX-D/A2727/8; 8-bit D/A
MK77670-00	MCM-SIO2		MDX-SIO2 dual serial I/O
MK77670-04	MCM-SIO2		MDX-SIO2-4; 4 MHz
MK77674		MCM-A/D12	MDX-A/D8; 8-bit A/D
MK77676	MCM-SIO2A		MDX-422N; dual RS-422
MK77754-00	MCM-DRAM64		MDX-DRAM16; 16Kb, 2.5 MHz
MK77754-04	MCM-DRAM64		MDX-DRAM16-4; 16Kb, 4 MHz
MK77759	MCM-UMC		MDX-UMC; 8 24-pin sockets
MK77760	MCM-7706-4L		MDX-BRAM4; 4K battery RAM
MK77761-00	MCM-DRAM64		MDX-DRAM32A; 32Kb dynamic
MK77761-04	MCM-DRAM64		MDX-DRAM32A-4; 32Kb, 4 MHz
MK77762	MCM-7706-4L		MDX-BRAM2; 2K battery RAM
MK77763	MCM-UMC		MDX-UMC2; 28-pin sockets
MK77764	MCM-DRAM64		MDX-RAM64; 64Kb dynamic RAM
MK77765	MCM-DRAM128		MDX-RAM128; 128Kb dynamic
MK77767-04	MCM-7706-4L		MDX-ZRAM4; 4K battery RAM
MK77767-08	MCM-7706-8L		MDX-ZRAM8; 8K battery RAM
MK77767-16	MCM-7706-16L		MDX-ZRAM16; 16K battery RAM
MK77850-00		MCM-CPU2A-2	MDX-CPU1; 2.5 MHz Z-80
MK77850-04		MCM-CPU2A-4	MDX-CPU1; 4.0 MHz Z-80A
MK77853-00	MCM-CPU2A-2		MDX-CPU2; 2.5 MHz Z-80
MK77853-04	MCM-CPU2A-4		MDX-CPU2; 4.0 MHz Z-80A
MK77855-00		MCM-CPU2A-2	MDX-CPU1A; 2.5 MHz Z-80
MK77855-04		MCM-CPU2A-4	MDX-CPU1A; 4.0 MHz Z-80A
MK77856-00	MCM-CPU2A-2		MDX-CPU2A; Z-80, 2.5 MHz
MK77856-04	MCM-CPU2A-4		MDX-CPU2A-4; Z-80A, 4 MHz
MK77857		MCM-SBC2	MDX-CPU3; Z-80A SBC
MK77858		MCM-SBC3	MDX-CPU4; Z-80A SBC
MK77859-00	MCM-CPU2A-2		MDX-CPU2B; Z-80, 2.5 MHz
MK77859-04	MCM-CPU2A-4		MDX-CPU2B; Z-80A, 4.0 MHz
MK77952	STD-WW2		Wire Wrap card
MK77953	STD-EXT		Extender card
MK77955	CBL-101-3		RS-232 cable (DTE)
MK77970	CBL-102-3		RS-232 cable (DCE)
MK77973	CC6-SE		MD-CC6; 6 slot, 0.75" ctr
MK77976		MCM-CLK	MDX-BCLK; battery clock
MK77977	CC16-RM		MD-CC16; 16 slot, 0.75"
MK77978		CC6-WM	MD-CC6WM; 6 slot, 0.75"
MK77989		CC16-RM	MD-CC10; 10 slot, 0.75"
MK77990	CC12-RM		MD-CC12A; 12 slot, 0.75"

Manufacturer's Product	Functional Replacement	Nearest Replacement	Manufacturer's Description
PRO-LOG			
7304	MCM-7304	MCM-DSIO	Dual UART card
7507	MCM-7507		Opto-22 I/F card
7508	MCM-7508		Dual Opto-22 I/F card
7601A	MCM-7604		TTL I/O card
7602A	MCM-7604		TTL I/O card
7603A	MCM-7604		TTL I/O card
7604A	MCM-7604		TTL I/O card
7605	MCM-7605		32 line TTL I/O card
7606	MCM-PIO		32 line prog. TTL I/O
7614	MCM-7614		TTL I/O card
7702A	MCM-UMC		Universal memory card
7704	MCM-UMC		Universal memory card
7705A	MCM-UMC		Universal memory card
7706-04L	MCM-7706-4L		4Kb battery RAM
7706-08L	MCM-7706-8L		8Kb battery RAM
7706-16L	MCM-7706-16L		16Kb battery RAM
7707-64K		MCM-DRAM64	64K dynamic RAM
7707-128K		MCM-DRAM128	128K dynamic RAM
7709-00	MCM-UMC2		64K memory card
7709-08N	MCM-7709-8N		8K CMOS battery RAM
7709-16N	MCM-7709-16N		16K CMOS battery RAM
7709-32N	MCM-7709-32N		32K CMOS battery RAM
7709-64N	MCM-7709-64N		64K CMOS battery RAM
7710	MCM-UMC2		512Kb memory
7716	MCM-UMC2-256		256Kb Static RAM card
7803A	MCM-CPU2A		Z80A plus memory
7804A-0		MCM-CPU2A-4	Z80A CPU, 4.0 MHz
7804A-1		MCM-CPU2A-2	Z80A CPU, 2.5 MHz
7805	MCM-7815		8085A plus memory
7806		MCM-SBC3	Z80A multifunction SBC
7808-01		MCM-SBC3-6	Z80H, SBC
7807		MCM-SBC3	Z80A multifunction SBC
7815	MCM-7815		8085A plus memory
7842		MCM-SBC3	Z80A/RS-422 SBC
7862		MCM-SBC8-5	8088; serial I/O plus timer
7864-1		MCM-SBC8-5	8088 SBC
7880		MCM-CPU2A	Z80A plus memory plus timer
7885		MCM-7815	8085A plus memory
7901	STD-EXT		Extender card
7903	STD-WW2		Wire Wrap card
7904	MCM-7904		Decoded I/O card
7911	STD-EXT		Extender card
7914		MCM-7904	Decoded I/O card
73C04	LPM-7304	LPM-DSIO	CMOS dual UART card
75C07	LPM-7507		CMOS Opto-22 I/F card
76C04		LPM-7604	CMOS I/O card
76C14		LPM-7614	CMOS I/O card
77C02	LPM-UMC		CMOS memory card
77C08	LPM-UMC		CMOS memory card
77C09-00	LPM-UMC2		64Kb CMOS memory card
77C09-08L	LPM-7709-8L		8Kb CMOS battery RAM
77C09-16L	LPM-7709-16L		16Kb CMOS battery RAM
77C09-32L	LPM-7709-32L		32Kb CMOS battery RAM
77C09-64L	LPM-7709-64L		64Kb CMOS battery RAM

Manufacturer's Product	Functional Replacement	Nearest Replacement	Manufacturer's Description
PRO-LOG			
77C09-00	LPM-UMC2		64Kb CMOS memory card
77C09-08L	LPM-7709-8L		8Kb CMOS battery RAM
77C09-16L	LPM-7709-16L		16Kb CMOS battery RAM
77C09-32L	LPM-7709-32L		32Kb CMOS battery RAM
77C09-64L	LPM-7709-64L		64Kb CMOS battery RAM
78C05	LPM-7815		CMOS 80C85 plus memory
78C13	LPM-CPU2A-2		CMOS Z80C plus memory
78C15	LPM-7815		CMOS 80C85 plus memory
79C04	LPM-7904		Decoded I/O card
ANALOG DEVICES			
RTI-1260	MCM-1260-DC		12-bit A/D; 16 Ch, S.E.
RTI-1262	MCM-D/A12-DC	MCM-D/A8-DC	12-bit D/A; 4 Ch.
RTI-1280	LPM-1280-DC		12-bit CMOS A/D; 16 Ch.
RTI-1282	LPM-D/A12-DC		12-bit D/A; 4 or 8 Ch.
DATA TRANSLATION			
DT-2724		MCM-A/D12-DC	12-bit A/D; 16 Ch, S.E.
DT-2727	MCM-D/A8-DC		8-bit D/A; 4 Ch.
DATRICON			
ACS-2A-2	MCM-CPU2A-2		Z80 CPU + Timers, 2.5 MHz
ACS-2A-4	MCM-CPU2A-4		Z80 CPU + Timers, 4.0 MHz
ACS-2A-6	MCM-CPU2A-6		Z80 CPU + Timers, 6.0 MHz
MS-128	MCM-UMC2		Universal Memory
MS-2B	MCM-7706-4L		2K Byte CMOS memory
MS-4B	MCM-7706-4L		4K Byte CMOS memory
MS-8B	MCM-7706-8L		8K Byte CMOS memory
MS-16B	MCM-7706-16L		16K Byte CMOS memory
Z80-SIO2-4	MCM-SIO2		Z80 Dual SIO
Z80-SIO2-6	MCM-SIO2-6		Z80 Dual SIO 6.0 MHz
Z80-PIO4	MCM-PIO		32 Channel Parrallel I/O
Z80-PIO4-6	MCM-PIO-6		32 Channel PIO, 6 MHz
VIA-04		MCM-7508	Opto-22 Rack I/F
RTX		MCM-CLK	Real Time Clock
EXT-BD	STD-EXT		Extender Card
DY-4			
DSTD-102	MCM-102		Z80A CPU with serial I/O
DSTD-325		MCM-DRAM	Dynamic RAM
DSTD-401		MCM-SIO2A	Dual RS-422 I/O
DSTD-502		MCM-UMC2	EPROM/RAM board
DSTD-503		MCM-UMC2	EPROM/RAM board
DSTD-800	MB-6		6 Slot motherboard
DSTD-804	CC4-WM		4 Slot card cage
DSTD-806	CC6-WM		6 Slot card cage

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WinSystems, Inc.

DOS Systems

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FEATURES

- Fully IBM PC-AT compatible
- Fast 80286/386/486 CPUs
- AT BIOS with power on self test (POST)
- Supports MS-DOS, QNX, UNIX, and OS/2
- 16 Megabyte direct addressing
- 512KB, 1MB, 2MB, 4M or 8 MBytes of memory with parity on CPU card
- Dynamic Bus sizing for 8-or 16-bit transfers
- Variable speed bus
- Keyboard interface with lockout
- Speaker onboard
- Optional 80287/387 math coprocessor socket
- Full PC I/O complement available on STD Bus
  - Serial I/O
  - Centronics line printer port
  - Floppy and hard disk support
  - RAM/ROM disk support
  - VGA video and flat panel support
  - Ethernet and ARCNET LAN support
  - 2400/1200/300 baud modems
  - Analog and digital I/O
  - Full range of card cages and powered racks
- Supports up to two 200 MByte disks (formatted) and two 720K/1.44MByte 3.5″ drives in the cage
- Does not require keyboard, video, floppy or hard disk to boot the system
- Watchdog timer
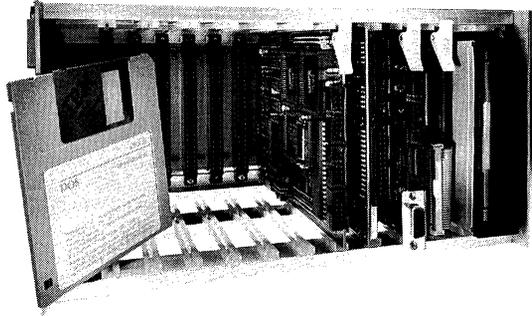
- Precision powerfail reset
- Small, rugged STD Bus card size: 4.5″ x 6.5″″
- Industry Standard IEEE 961 STD Bus interface
- WinSystems PC-XT compatible available
- Low Power

The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "software bus", for hosting operating systems utilities, real time executives, development tools, networking, and application specific programs. The combination of

CPUs

80486DX
80486SX
80386SX
80286
V53
V40

DISK I/F

FLOPPY
HARD
OPTICAL
ROM DISK
RAM DISK

DISPLAY CONTROL

LCD
VGA
FLAT PANEL
M/CGA

OTHER I/O BOARDS

S T D

B U S
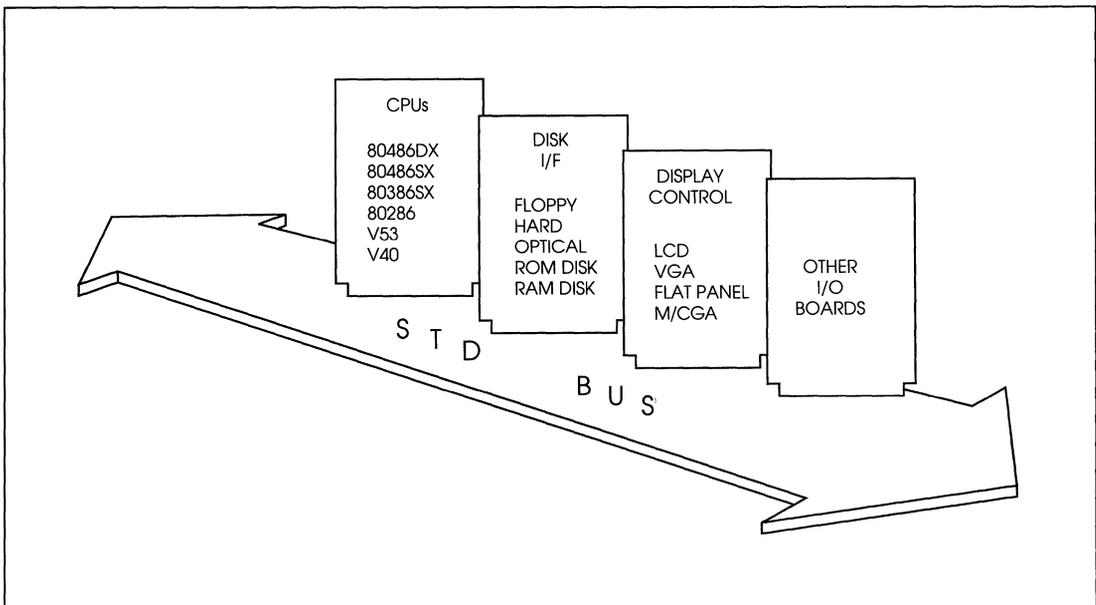
hardware and software standards assure flexibility when designing and configuring a rugged industrial computer.

SYSTEMS OVERVIEW

STD-AT - WinSystems' STD-AT is a true 80286/386/486 based PC-AT compatible industrial computer on the STD Bus. It combines the powerful processing capability of the 80286/386/486 and the vast library of PC-DOS software with the reliability and industrial I/O interfaces of the open architecture IEEE 961 STD Bus.

The STD-AT is a product family that covers a number of system components that combined together create a STD Bus PC-AT compatible system. The system components can be categorized as CPUs, memory, disk controllers, video controllers, communications/network controllers, serial I/O, parallel I/O, analog I/O, and powered card racks. WinSystems offers preconfigured systems or user configurable systems.

The basic philosophy of the STD-AT is DOS compatibility and high performance. WinSystems' designed the base set of boards for the STD-AT to be 100% MS/PC-DOS compatible. Rather than trying to force fit DOS onto an existing hardware design, WinSystems' designed two completely new CPUs, video, serial I/O, network, and disk cards that are based upon known VLSI devices which offered DOS compatibility. PC compatibility provides the ability to use the extensive pool of PC applications software without modification.

The result is a completely AT compatible system with CPU ranging from the low cost 80286 to the high performance 80486SX at operational speeds from 10 to 50 MHz.

High Performance - The STD-AT is based on three different AT class CPUs, offering a migration path to 80486 performance. Originally, the WinSystems' STD-AT was based on the 16-bit 80286 microprocessor and the optional 80287 numerical coprocessor. The 80286's pipelined architecture and operational speed, up to 20 MHz, still offers performance that is comparable to many high-end minicomputers. The 80386SX provides the performance benefits of a 32-bit programming architecture with the cost savings associated with 16-bit hardware systems.

The STD-AT can also support the powerful 80486 high performance microprocessor which has specially optimized capabilities for multiple user and multitasking systems. By incorporating the 80486 coprocessor, the system's performance is approximately twice that of a 80386-based unit running at the same frequency. Both the 80386 and the 80486 offer a 32-bit programming architecture compatible with the software base of the 80X86 microprocessor to provide backward compatibility to the large installed base of 8086 and 80286 software. The STD-AT supports both 8- and 16-bit data transfers on the STD Bus for maximum performance.

WinSystems' DOS Comparison Chart

PRODUCT	CPU	SPEED*	NORTON SYSINFO	LANDMARK V 2.0
MCM-SBC41	V40 (8088)	8, 10	2.2	4.49
MCM-SBC53	V53	10, 16	10.8	19.78
MCM-SX386	80386SX	16, 20, 33	TBD	TBD
MCM-286AT	80C286	10, 12, 16, 20	11.8	25.4
MCM-386SX	80386SX	16, 20	11.4	19.63
MCM-486DX	80486DX	25, 33, 50	71.4	110.4

*Benchmarks calculated with underlined CPU speed.

80286 vs 80386 vs 80486 - Should you choose WinSystems' 80286, 80386SX or 80486 based CPU? Each chip has its own advantages and disadvantages. You should look at three areas to make the decision: performance, capabilities, and cost.

If you are going to be running current DOS software without a coprocessor, then the 80286 is probably your best choice. If you are planning on running 32-bit software now or in the future, written specifically for the 80386/486 instruction set, running code that requires the fast number crunching of a coprocessor, or require true multitasking, then you should select the 80386/486. For more information about the performance benchmarks or system configurations, call WinSystems' applications engineering department at 817-274-7553.

PC-XT - WinSystems offers a PC-XT compatible based upon the LPM/MCM-SBC41 board. It will run MS-DOS compatible software with or without a disk. One key feature of the LPM-SBC41 is that it will operate from -40° to +85° Centigrade. In harsh environments or at extended temperatures, it will work with a RAM/ROM disk with MS-DOS and with the application program residing in ROM. Video and a standard keyboard are supported, but neither are required for operation. The existing STD Bus I/O cards will work with either the STD-AT or SBC41.

Industry Standards - The STD-AT design uses the industry standard 80286/386/486 CPUs, Chips and Technologies NEAT CHIPSet, Phoenix BIOS, Cirrus Logic VGA, EGA, CGA video controller, and IDE compatible 40, 100, or 200MByte disk drive packaged on the industry standard IEEE 961 STD Bus. It supports either PC-DOS or MS-DOS. The open architecture of the system allows for 8-or 16-bit I/O expansion modules and upgrades to meet new requirements while operating under a DOS environment. Since it is 100% DOS compatible, it can support other operating systems or real-time operating systems. It runs the thousands of software applications and utility packages developed for the PC-XT/AT. Additionally, it will run the growing selection of DOS programs targeted at industrial and commercial applications. The STD-AT provides the core hardware foundation for industrial control systems.

STD Bus - The STD-AT supports industry standard IEEE 961 STD Bus. This hardware standard is very popular because of its small size, rugged design, high quality, and support from multiple vendors worldwide. As an approved IEEE standard, it provides a well documented scheme for combining microprocessor and peripheral devices. Nine out of every 10 major

American manufacturers use the STD Bus because of its reliability, flexibility and cost effectiveness. These users include large and small OEMs who use the STD Bus to bring their products to life. Other users include chemical engineers, technicians and scientists who build custom systems with off-the-shelf convenience. Whether users are skilled computer programmers or first-time designers, they know they can rely on the STD Bus for ease-of-use and long-term support from manufacturers.

The STD Bus 16-bit bus systems architecture is quite similar in power and functionality to the AT bus, yet it is designed specifically for the rigors of industrial applications. The STD Bus is well known for the wealth of real-world interface cards that links it to most any industrial sensor. The STD Bus has an active manufacturers group (STDMG) to monitor standards, specifications, and new technical developments to assure orderly evolutionary growth. While the PC-XT/ AT Bus has been abandoned by its developer, the STD Bus has continued to evolve to meet the new challenges of customer applications. This evolution has occured by adapting to newer technologies for higher performance and more cost-effective solutions. The result is a lasting standard for industrial applications not threatened by obsolescence or abandonment every 5 years.

Unlike other bus types, the STD Bus is specifically designed for process control and industrial applications. Often it is referred to as the "Blue Collar Bus". Its simple bus interface contributes to lower overall cost and high reliability (typical MTBF of 15 to 25 years, depending on card type).

I/O interfaces are available for pressure and temperature measurement, stepper and large motor control, analog and digital interface, networking, video graphics, and so on. Users who need special I/O functions can easily design and construct their systems, since the STD Bus offers a larger variety of interface cards than any other bus. In fact, many special I/O interfaces that must be custom made for other busses are often off-the-shelf products with the STD Bus. Currently over 150 manufacturers worldwide produce more than 2000 different kinds of STD Bus boards.

CMOS STD Bus - The STD-AT is also available for the CMOS STD Bus. CMOS offers very low power, improved noise immunity, and extended temperature operation. The temperature range is wider than with an NMOS equivalent and the power requirement is much less. Lower power requirements mean low system operating temperatures, reduced internal heating, no fans, smaller power supplies, and sealed enclosures.

The MCM prefix on WinSystems' cards designates STD Bus products and the LPM prefix designates CMOS STD Bus boards. A LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS STD Bus and STD Bus versions. The difference between these products are the various power requirements and operational temperature ranges. For example, the LPM-286AT CMOS STD Bus single board computer has the Harris 80C286 installed rather than the Intel 80286. The operational temperature range (excluding rotational media and the video terminal) is 0 to +70 degrees Centigrade. Normally -40° to +85° Centigrade is the operational temperature range of CMOS digital devices; however, the CHIPSet, keyboard controller and dynamic RAMs are unavailable at extended temperature ratings at this time. The LPM-SBC41 will work at the full extended industrial temperature range.

STD vs PC Bus - Should you choose a commercial PC-AT or clone or should you install a industrial grade STD Bus system at the same cost? The choice should be made on a number of considerations: functionality, reliability, speed, cost, form factor, temperature range, I/O modules, software support, factory support, and familiarity with the hardware.

The PC Bus and STD Bus are similar enough that they may be thought of as cousins. The former was designed for the office. The latter was intended at the start for the factory and industrial settings. STD Bus cards are much more compact than PC Bus cards; therefore, the overall volume of the system is greatly reduced. These units can be easily mounted in sealed NEMA type enclosures or in RETMA racks. The WinSystems' STD-AT is designed to replace commercial PC-AT's with a more conservative design to ensure better quality and greater reliability.

The small size of the STD Bus cards, 4.5" x 6.5", make it ideal for use in disguised and embedded industrial controller applications. The small format is designed for industrial environments since the cards don't bend or flex and are engineered to stand shock and vibration. An STD Bus card is held in place by the STD Bus card cage on 3 sides and with an optional additional hold down bar across the card ejector on the top of the cards. This secure placement permits the STD Bus card to sustain violent vibrations without coming loose. The small format and the low cost of the STD Bus cards render their maintenance simple, quick, and economical.

PC bus cards by comparison are relatively long and cumbersome, and are supported at only one other
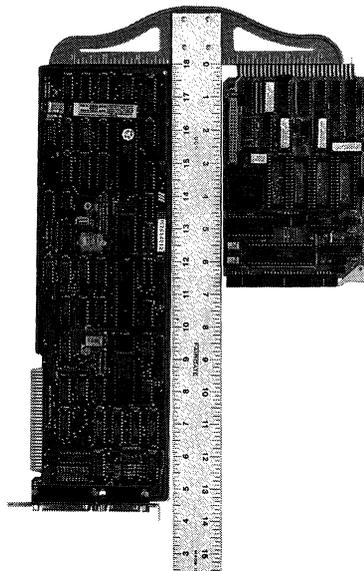
Size Comparison of STD vs PC Bus Card

point on the card in addition to the card edge connector. Traditional PC bus cards won't fit into the space allotted or provide as many mounting configurations in embedded applications as compared to the STD Bus.

The Mean Time to Repair (MTTR) is very low for STD Bus cards. Replacement is as simple as sliding a card out and the new card back in the rack. PC's require much more disassembly and reassembly.

STD Bus cards are not subject to rapid obsolescence. A PC Bus card may only be in production for only a few months before either major changes or becoming unavailable. This creates problems with customer's engineering and production documentation control systems, as well as a purchasing problem.

The STD Bus card does not look like a PC card so that it carries added value in the eyes of the end user. Customers typically associate PC based product with very low cost hardware. Even though the ultimate product may have a high dollar price, an embedded PC Bus system tends to lower the price the integrator can charge their customer.

STD Bus I/O Cards - WinSystems offers a full line of both CMOS STD Bus (LPM) and STD Bus (MCM) memory and I/O cards covering A/D, D/A, digital I/O, Opto-22 interface, serial I/O, counter/timers, and other functions. For a detailed description of these

products, please refer to the WinSystems' STD Bus Databook. Call the factory and ask for a free copy of the latest issue. This Databook also includes a complete copy of the STD Bus specification and application notes.

Applications - The WinSystems' STD-AT is ideal for a broad range of embedded and dedicated applications in which a microcomputer is used as an intelligent component, or other device. This allows the OEM or system integrator to maximize return on investment by utilizing the STD-AT and supporting I/O cards as the basis for system design. Some typical applications include:

- Machine Control
- Medical Instruments
- Specialized Test Fixtures
- Process Control
- Communications Controllers
- Data Acquisition
- Weighing/Inventory
- Inspection/Quality

- Robotics
- Semiconductor Manufacturing
- Military
- Printing
- Telecommunications
- Test/Measurement Equipment
- Factory Automation
- Energy Management

SOFTWARE SUPPORT

The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "Software Bus" for hosting operating systems, utilities, real time executives, development tools, networking, and application of specific programs.

The STD-AT contains an AT BIOS and authorized copy of Microsoft's MS-DOS, Version 5.0. Together, these two components assure you of the highest possible degree of IBM-compatibility. Compatibility means that your system, which is made up of hardware and system software, runs all application software programs that normally run on the IBM PC.

DOS can operate in a disk based or diskless hardware environment. Industrial disk based systems are well defined and understood. Alternatively diskless configurations are fully supported by WinSystems for embedded systems applications.

For embedded systems, the STD-AT will boot without a keyboard, a video card, and without floppy disk or hard disk installed. The video can be redirected to the COM channels and the RAM/ROM disk can serve as storage. This is required in applications where rotational media and video displays cannot survive due to temperature, vibration, shock, dust, or other severe environmental conditions.

Disk Based DOS Systems

DOS - The STD-AT is designed to be architecturally compatible with the PC-AT. As such, it will run either MS-DOS or IBM PC-DOS and will support calls either through the BIOS or directly to the hardware. WinSystems can supply the STD-AT with the BIOS only or with the BIOS and MS-DOS. Microsoft GW-BASIC product is also provided with MS-DOS. The card will also support other operating systems such as UNIX or XENIX and real time executives that require a "PC-AT" hardware environment.

BIOS - The Basic Input/Output System (BIOS) provides maximum performance and full IBM-AT compatibility. It is designed for high speed 80286/80386/80486 systems. It supports both 720KB and 1.44MB 3.5 inch and 360KB and 1.2MB 5.25 inch floppy disk drives, 101, 102, and 84-key AT-compatible keyboards, the 80287/80387SX math coprocessor, offers enhanced protected mode to real mode switching for faster VDISK, INT 15H multitasking extensions for extended memory and block moves, IBM defined extensions to BIOS calls, and is fully compatible with Novell NetWare. The BIOS also provides complete power-on self test and boot diagnostics.
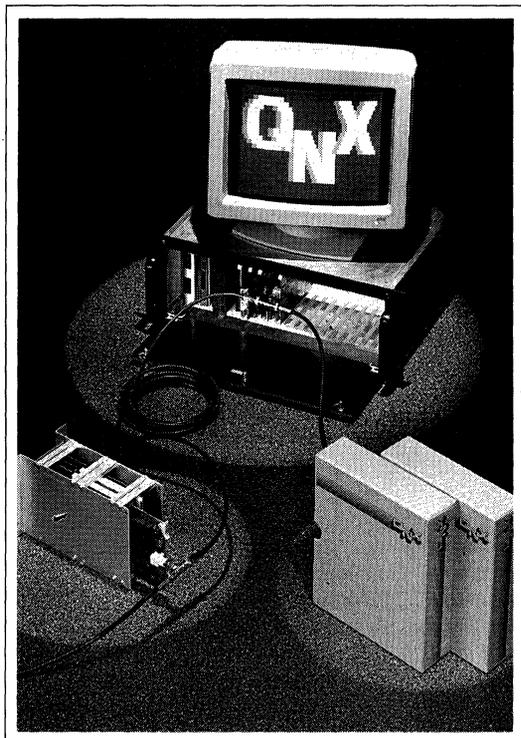
QNX - QNX is a powerful, real-time, networked, distributed processing operating system. It permits up to 57 users per computer and up to 250 concurrent tasks. Its preemptive, priority driven scheduling, coupled with a fast task-switch time, allow QNX to provide the response needed for process control and other real-time applications.

Both QNX 2..15 and 4.x are supported by WinSystems' STD-AT compatible computers. It will run on small diskless embedded controllers without requiring video ("blind nodes") up through large systems with multiple disk drives. Whether you are running a network of four or 400 machines, QNX makes it all feel like a single computer. Interprocess communication is network wide, so every process can transparently access every resource — programs, files, devices, even CPUs — anywhere on the network. It supports both the ARCNET and Ethernet local area networking schemes.

Embedded Systems Support

Diskless MS-DOS - The WinSystems' STD-AT can run MS-DOS with or without a disk. In harsh environments where disk operation is not practical, either the LPM/MCM-SSD or LPM/MCM-RSSD solid state disks will permit the application to bootup and run. It allows DOS to reside in EPROM along with applications programs and be copied into system RAM. With it, standard .EXE and .COM files execute on a diskless system even using DOS calls for I/O. Up to 4 megabytes can be stored in each RAM/ROM disk. Also, that ROM disk will support a non-volatile, battery-backed RAM disk for data and program storage up to 12 megabytes. These RAM/ROM disks will support either EPROMs for Read only and battery-backed RAMs for Read/Write file access.

ROM-DOS - ROM-DOS is a MS-DOS 3.X compatible ROM based embedded operating system. ROM-DOS provides 3 major functions: hardware initialization, file support and standard drivers. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied.

ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS has been ported to WinSystems' STD Bus, CMOS STD Bus and non-bus based single board computers. Each different board has its own mini-BIOS to support ROM-DOS. This allows easy development, debugging, loading and execution of programs written in C, Quick BASIC, Turbo Pascal, etc. that are loaded as .EXE or .COM files.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that greatly simplifies data storage and retrieval. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

C-Thru-ROM Development Software - C-THRU-ROM (CTR) is a complete, comprehensive, full featured integrated debugging package for generating stand-alone ROMable programs with Microsoft or Borland Turbo C for use with WinSystems' STD Bus or stand alone single board computers (SBCs). This program does not require MS-DOS or ROM-DOS to operate. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC/XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

SYSTEMS SUPPORT

Technical Support - WinSystems has an applications engineering staff to answer technical questions concerning hardware, software and system products and configurations both before and after purchase. You can call 817-274-7553, write, or FAX your questions to the Applications Engineering Department. The FAX number is 817-548-1358.

Product Demonstration - The STD-AT is best evaluated through demonstrations. If you would like a demonstration, please call our sales department at 817-274-7553.

FCC Compliance - The STD-AT is exempt from FCC requirements for computing devices based on Part 15, Subpart J, Paragraph 15.801(c)(3) for industrial test equipment. The customer is responsible for compliance for finished systems.

Quality - WinSystems demands the highest quality workmanship standards in all of its products. All elements of the product from design, layout, fabrication, testing, and inspection are carefully checked and monitored for conformance to standards. Painstaking attention to detail is demanded to assure a constant supply of quality products. All of the boards are burned-in for 48 hours and 100% of them are tested before shipping.

Systems Components   CPU's

MCM-486DX/SX
80486DX and SX, STD-AT Compatible
Single Board Computer

The MCM-486DX/SX board includes the Intel 80486DX or SX CPU operating at either 25, 33 or 50 MHz for the DX version or with 20 or 25MHz for the 486SX, both are available with up to 8MB of DRAM, two RS-232 serial ports, DMA, interrupt controller, printer port, real time clock, keyboard controller, watchdog timer, and speaker.
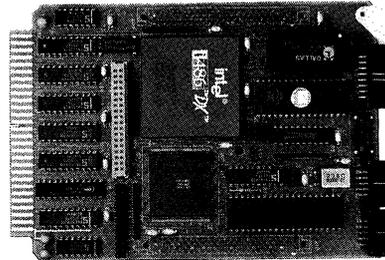
LPM/MCM-SX386
Low Cost 80386SX
Single Board Computer

The LPM/MCM-SX386 is a low cost complete single board computer including 80386SX CPU. It includes up to 4MB of memory, keyboard controller, RTC, 2 serial ports, 1 printer port, floppy and IDE hard disk interface, and BIOS on a single card. It is available in 16, 20, or 33 MHz.
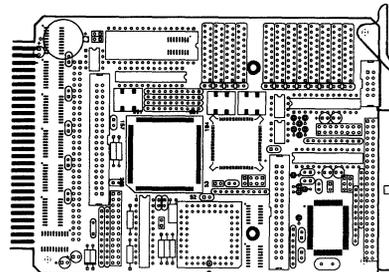
LPM/MCM-386SX
80386SX STD-AT Compatible
Single Board Computer

The LPM/MCM-386SX board includes the Intel 80386SX CPU operating at either 16 or 20 MHz with either 512KB, 1MB, 2MB, or 4MB of parity DRAM, two EPROM sockets, an 80387SX coprocessor socket, two RS-232 serial ports, interrupt controller, DMA, Centronics parallel I/O port, real time clock, keyboard controller, watchdog timer, and speaker.
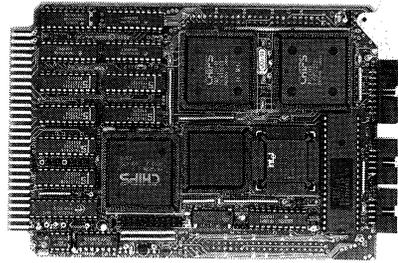
LPM/MCM-286AT
80286 STD-AT Compatible
Single Board Computer

The LPM/MCM-286AT board includes the 80286 CPU operating at either 10, 12, 16 or 20 MHz with either 512KB, 1MB, 2MB, or 4MB of parity DRAM, two EPROM sockets, an 80287 coprocessor socket, two RS-232 serial ports, interrupt controller, DMA, Centronics parallel I/O port, real time clock, keyboard controller, watchdog timer, and speaker.
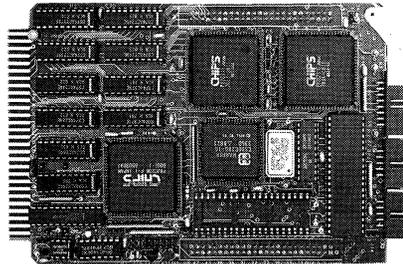
LPM/MCM-SBC53
Low Cost V-53
Single Board Computer

The LPM/MCM-SBC53 is a high performance AT Class, 16-bit, V53 SBC operating at 10 or 16 MHz. Four memory sockets support up to 2MB of SRAM, psuedo-static RAM, EPROM, and PEROMs (Flash). It also supports 3 serial ports, SBX connector, optional 80C287 coprocessor, printer port, 3 counter/timers, and watchdog timer.
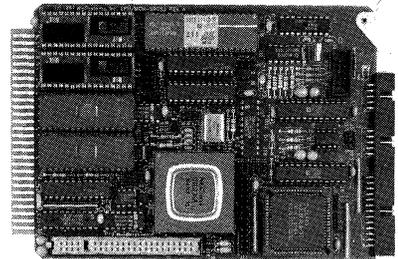
LPM/MCM-SBC41
Low Cost V-40
Single Board Computer

The LPM/MCM-SBC41 board is a V40 based (highly integrated 80C88 equivalent) PC-XT compatible. It contains the CPU, 3 memory sockets supporting up to 768KB of RAM, EPROM, and EEPROM, 2 serial I/O channels, 3 counter/timers, interrupt controller, clock calendar, keyboard controller and watchdog timer.
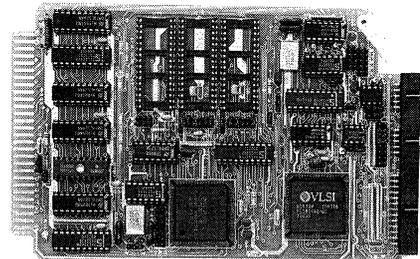
Disk Controllers

LPM/MCM-DISK-AT
IDE/Floppy
Interface Board

The LPM/MCM-DISK-AT controls both 3.5 inch IDE compatible hard disk drives and 3.5 inch and 5.25 inch floppy disk drives. The total storage capacity is over 400 MB with a single controller card. It is compatible with WinSystems' 80286/386/486 STD-AT and supports 16-bit data transfers.
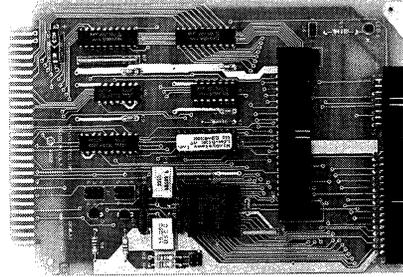
LPM/MCM-DSKIO
Disk I/O
Support Card

The LPM/MCM-DSKIO is a general purpose DOS system support card for use with the SBC41, SBC53 and other WinSystems' V40/V53 class CPUs. It provides the peripheral interface electronics for floppy and hard disks, keyboard, real time clock, and BIOS ROM extension socket. This card allows embedded SBCs to be configured to work with rotational media for complete PC-type systems.
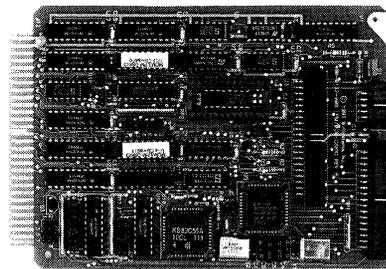
LPM/MCM-SSD
RAM/ROM
Solid State Disk

The LPM/MCM-SSD is a STD Bus RAM/ROM solid state disk designed for applications where the environment is too harsh for mechanical hard disks or floppy disk drives. Software drivers are available for STD Bus XT/AT applications for use in DOS and embedded ROM-DOS systems.
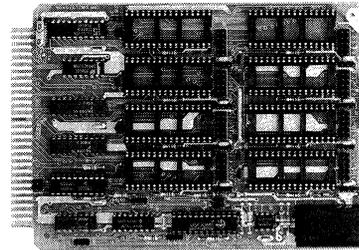
LPM/MCM-RSSD
Removable Solid State
Disk Drive

The LPM/MCM-RSSD is a Removable Solid State Disk Drive that supports credit card size RAM data cartridges for storage up to 2 megabytes. It is ideal for embedded control applications requiring portable data and program storage. It will survive in harsh environments where floppy disks will fail.
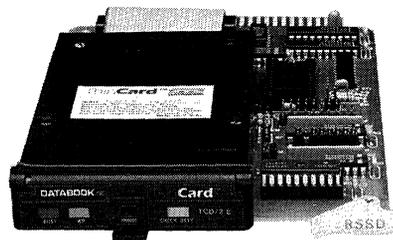
LPM/MCM-EGA
High-Resolution EGA
Display Adapter Card

The LPM/MCM-EGA board is a high-resolution display adapter card that provides PC-compatible EGA, CGA, MDA, and Hercules graphics capability on a single card. It is compatible with both the STD-AT and XT compatible from WinSystems and also supports a light pen input.
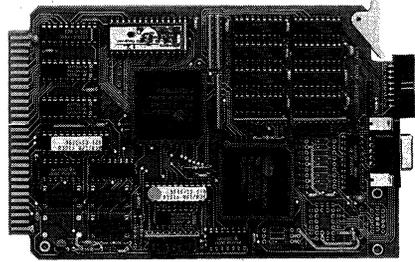
LPM/MCM-VGA
High-Resolution VGA
Display Adapter Card

The LPM/MCM-VGA board is a high-resolution display adapter card that provides PC-compatible VGA, EGA, CGA, MDA, and Hercules graphics capability on a single card. It is compatible with both the STD-AT and XT compatible from WinSystems and also supports a light pen input.
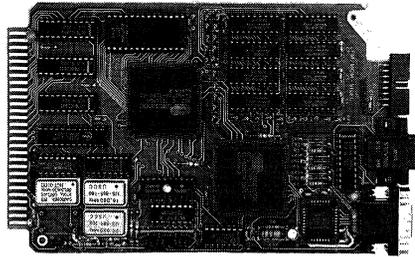
LPM/MCM-M/CGA
MGA/CGA Low Cost
Video Adapter Card

The LPM-M/CGA and MCM-M/CGA are low cost CMOS STD and STD Bus boards that provide color graphics and monochrome CGA, MDA, and HGC compatibility. Both digital and composite video output is available. This card supports a light pen and also permits 2 video boards in a system.
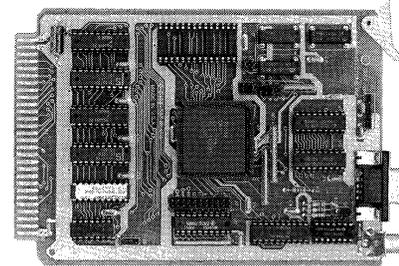
LPM/MCM-FPVGA
Flat Panel/CRT
VGA Card

The LPM/MCM-FPVGA is a versatile LCD VGA controller that provides support for basic VGA modes for an LCD or CRT, and extended 800 x 600 resolution graphics on the CRT. It provides excellent display quality, with up to 64 shades of gray on monochrome STN LCD panels and a direct connection capability for active matrix color LCD panels.
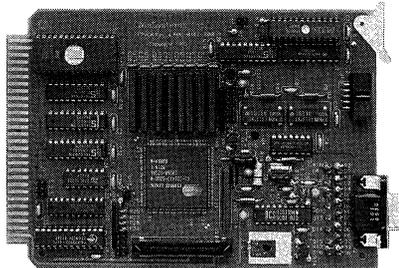
Communications/Network Controllers

LPM/MCM-ANET
ARCNET
Local Area Network Card

The LPM/MCM-ANET is a complete ARCNET interface board designed to operate with coaxial systems in either a star or bus topology or with fiber optic cables in a star topology. It is software compatible with NetWare and ViaNet. It can support 255 nodes at 2.5 Mbps for distances up to four miles.
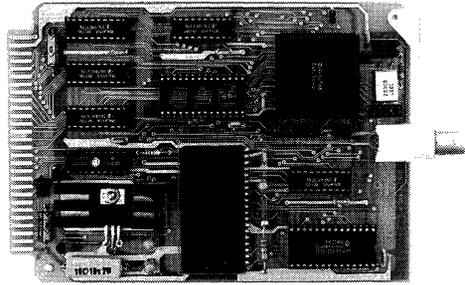
LPM/MCM-ENET
Ethernet
Local Area Network Card

The MCM-ENET board is a local area network adapter board which is compatible with the IEEE 802.3 10BASE5 ETHERNET and 10BASE2 Thin Wire ETHERNET standards. It is software compatible with NetWare, ViaNet, and other software that requires WD8003EB compatibility.
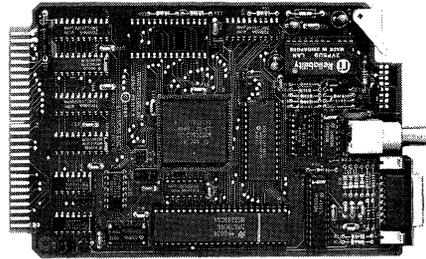
MCM-2400/2400MNP
2400/1200/300 Bps
Smart Modem

The MCM-2400 is a 2400/1200/300 Bps Smart modem card. It supports synchronous and asynchronous modes plus the industry standard Hayes "AT" command set used by all popular communications software. The MCM-2400MNP board supports MNP, Microcom Networking Protocol, up to Class 5.
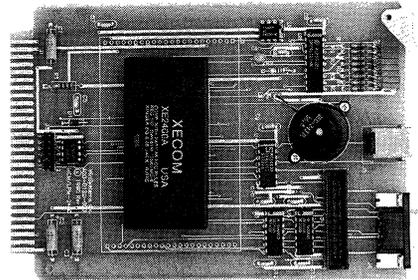
LPM/MCM-MODEM
Bell 212A/103
1200/300 Bps Smart Modem

The LPM/MCM-MODEM is a self contained 1200/300 bps Bell 212A/103 or CCITT V.22/V.21 compatible modem. It includes a 8250B type UART for the bus connection, modem and FCC registered DAA for direct connections to a telephone line. It supports the industry standard "AT" command set.
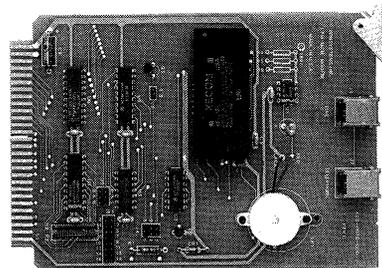
LPM/MCM-7507
24-Line Bidirectional
Digital I/O Card

The LPM/MCM-7507 is a 24-line TTL Input/Output card that can be used as a general-purpose I/O card or can provide an interface to the industry standard 4-, 8-, 16-, or 24-I/O module mounting racks from Opto-22 or equivalent manufacturers. It controls AC or DC opto-isolated input or output modules.
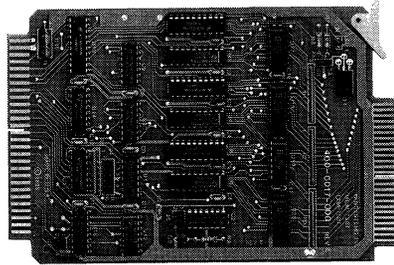
LPM/MCM-7508
48-Line Bidirectional
Digital I/O Card

The LPM/MCM-7508 is a 48-line TTL Input/Output card that can be used as a general-purpose I/O card or can provide an interface to two industry standard 4-, 8-, 16-, or 24-I/O module mounting racks from Opto-22 or equivalent manufacturers. The 7508 card is the equivalent of two LPM/MCM-7507 cards.
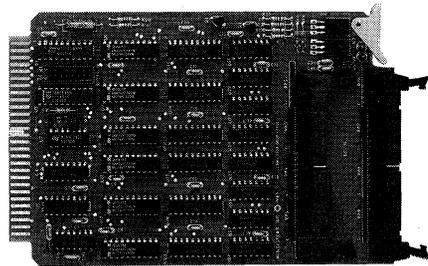
LPM/MCM-7605
32-Bit I/O Card

The LPM/MCM-7605 is a general purpose, 32-line parallel input/output TTL interface cards. Each of the 32 lines can be individually configured as input, output, or output with readback. This is particularly useful when an external device requires more or less than eight lines or a mixture of inputs and outputs.
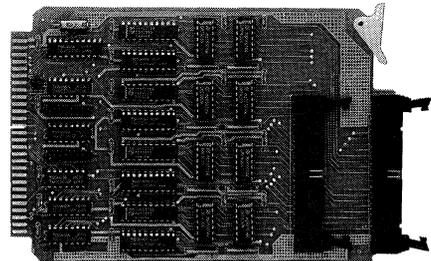
LPM/MCM-7614
64 Line TTL I/O Card

The LPM/MCM-7614 is a general purpose 64 line TTL input/output interface card. It is grouped as 8 ports of 8 lines, each port can be configured as 8 inputs or 8 outputs with readback. It is ideal for applications for reading and controlling devices such as keyboards, encoders, displays, and switches.
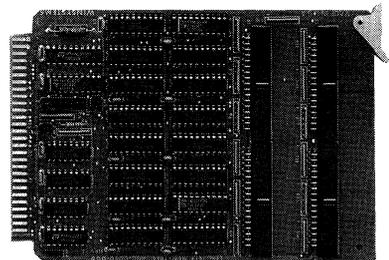
Parallel I/O

LPM/MCM-DLPT
Dual Printer and
Joystick Port

The LPM/MCM-DLPT is a low cost, 2 channel parallel line printer and joystick card for STD Bus DOS and ROM-DOS applications. Either or both of the printer ports can be used as a general purpose parallel I/O port if printer support is not required. Two standard joysticks are supported by the board.
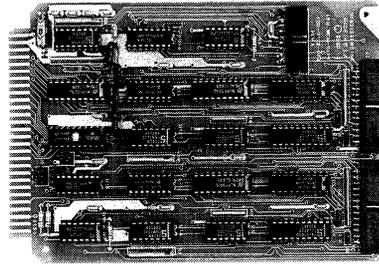
LPM/MCM-STATUS
Switch Input and
LED Display Card

The LPM/MCM-STATUS is a general purpose status and diagnostic cards that provide 32 switch inputs and 32 LEDs on a single card. Both are suitable for applications where a low cost interface is needed for manual switch inputs and visual status for system testing, diagnostics or on-site configuration.
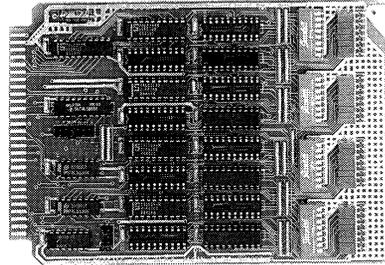
Serial I/O

LPM/MCM-DSPIO
Dual Serial and
Parallel I/O Card

The LPM/MCM-DSPIO is a dual serial 8250 UART and Centronics parallel I/O card. Both serial channels are RS-232/485 compatible. It is ideally suited for applications running DOS programs or languages that require exact register compatible hardware for program execution.
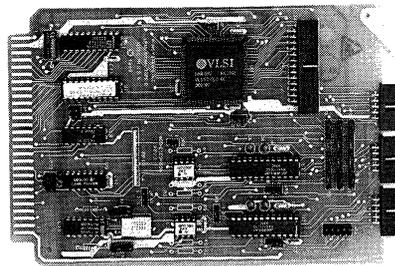
LPM/MCM-7314
Quad Multiprotocol
Serial I/O Card

The LPM/MCM-7314 is a four channel, full-duplex, RS-232 serial input/output boards that can support multiprotocol asynchronous or synchronous communications. A driver program is available from WinSystems that supports asynchronous operation for both DOS and ROM-DOS applications.
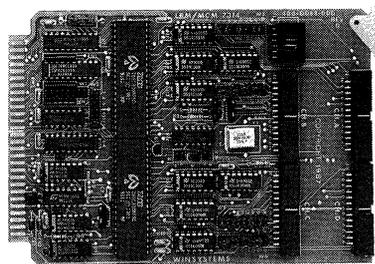
LPM/MCM-AIO
12-bit Analog
Input/Output Card

The LPM/MCM-AIO is a low cost, 12-bit analog input and output board. It has 32 single ended 0 to + 5V voltage input channels with a software programmable gain amplifier of 1, 10, and 100. The conversion time is 125 uS per channel. The two D/A output channels are 0 to +5V.
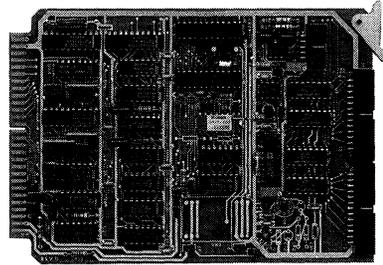
LPM/MCM-A/D12
12-Bit Analog
Input Card

The LPM/MCM-A/D12 is a 12-bit analog to digital converter card with 8 differential or 16 single ended analog input channels. Conversion time is 75 microseconds. The voltage input ranges are 0 to + 5V, 0 to +10V, + 2.5V, + 5V or +10V. A user selectable gain from 1 to 1000 is resistor programmable.
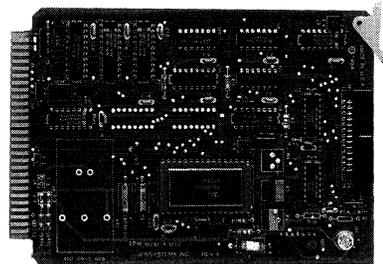
LPM/MCM-D/A12
12-Bit Analog
Output Card

The LPM/MCM-D/A12 is a 12-bit D/A converter offered configured with either four or eight output channels. Each channel is independent of the other and can be selected for one of four output voltages: 0 to +5V, 0 to +10V, +5V, or +10V. Each channel has its own gain adjustment for calibration.
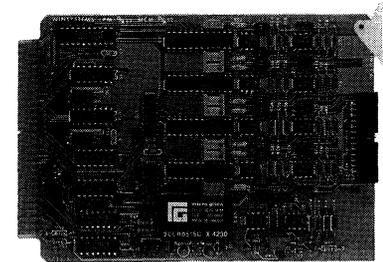
LPM/MCM-D/A8
8-Bit Analog
Output Board

The LPM/MCM-D/A8 is an eight channel, 8-bit digital to analog converter. Each channel is independent from the other and can be configured for one of four output voltages: 0 to +1V, 0 to +2.5V, 0 to +5V, or 0 to +10V. Each has its own gain adjustment for calibration.
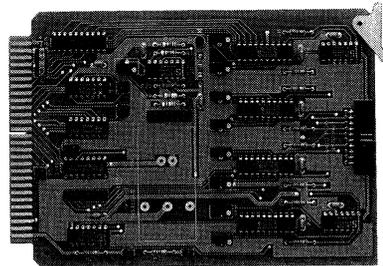
Miscellaneous Cards

LPM/MCM-488
Talker/Listener/Controller
IEEE-488 Controller

The LPM/MCM-488 is an interface designed to meet the specifications required for talker, listener and controller as specified by IEEE 488-1978. This interface makes possible the transfer of data between thousands of IEEE-488 compatible devices.
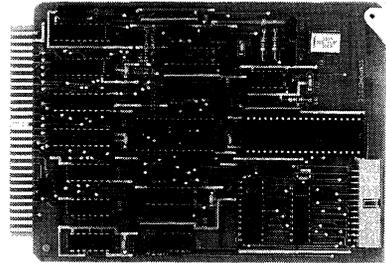
LPM/MCM-7904
Decoded I/O
Utility Card

The LPM/MCM-7904 is a card designed for prototyping I/O circuitry. The card contains the decoding circuitry, logic, and buffering so that experimental and custom interfaces can be built. The 0.100 inch grid provided in the breadboard area accepts standard DIP sockets, press-fit pins and discrete logic.
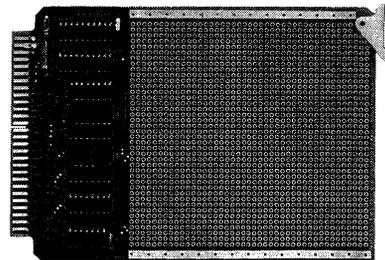
LPM/MCM-CTC
9 Channel, 16-bit
Counter/Timer Card

The LPM/MCM-CTC is a 9 channel, 16-bit counter/timer card capable of counting from DC to 8MHz. Eight channels have a buffered Clock, Gate, and Output available at the connector. The 9th channel can be used for timing, a time base generator for the other 8 channels or as a watchdog timer.
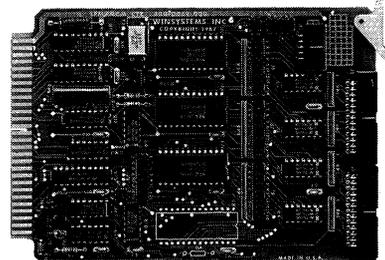
PC-STD Bus Adapter
Direct High Speed
Bus to Bus Interface

The PC-STD Bus adapter is a direct PC Bus to STD Bus link. It permits STD Bus I/O cards to be coupled into a PC-XT/AT or compatible for use as an "in-systems-emulator" for program development. The adapter also allows STD Bus I/O cards to be used as an I/O front end for standard PC-XT/AT.
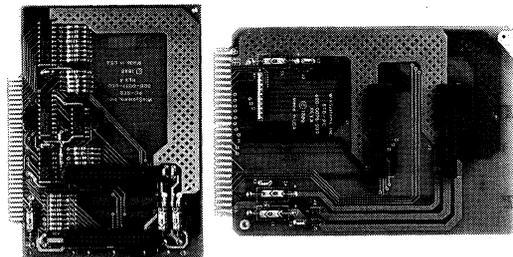
FD3-720/144
STD Bus Mounted
3.5" Floppy Disk Drive

The FD3-720 and FD3-144 are floppy disk drive modules containing 3.5 inch, double sided, micro-floppy drives mounted directly on an STD Bus card. This configuration allows a floppy drive to be easily and conveniently mounted inside a STD Bus card cage for STD-AT and XT DOS compatible systems.
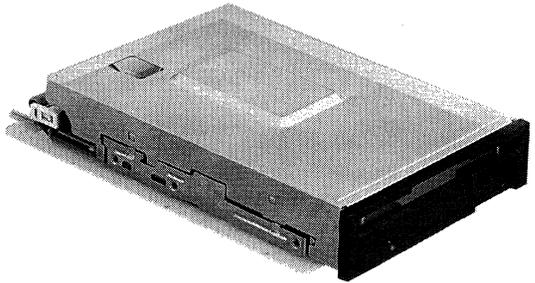
HDAT-40/100/200
STD Bus Mounted
3.5" Hard Disk Drive

The HDAT/XT-40/100/200 are hard disk drive modules containing a 3.5 inch drive and controller mounted directly on a STD Bus card. The HDAT is an IDE compatible controller/drive and the HDXT is a SCSI compatible drive, either are easily mounted inside a card cage for STD-AT and XT DOS compatible systems.
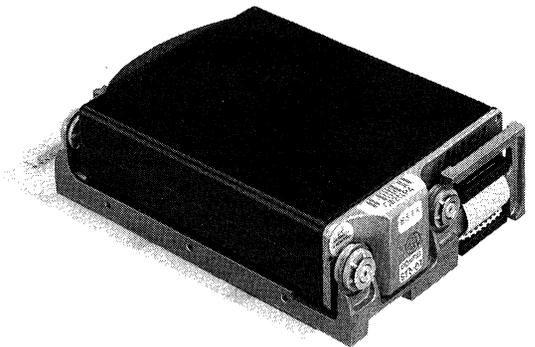
POWERED RACKS
CARD CAGES &
BACKPLANES
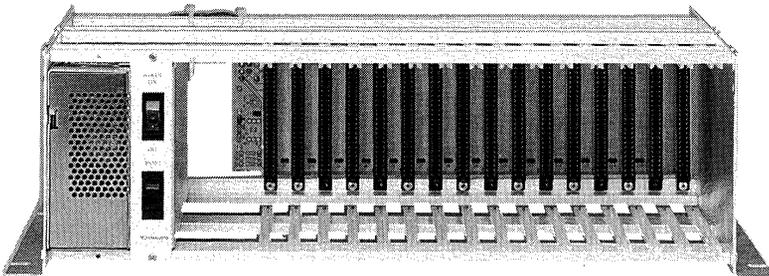
WinSystems' offers a broad line of backplanes, assembled card cages and card cages with power supplies. The card racks and backplanes are available from 2 to 26 slots and are ideal for high performance and demanding STD Bus applications.

Card Cages - WinSystems card cages are constructed of aluminum for light weight and strength. The design is optimized in order to offer the highest integrity and reliability for industrial applications. Spacing is on 3/4 or 5/8 inch centers with a vertical card orientation to take advantage of convection cooling.

Backplanes - WinSystems' STD Bus backplanes are available in eight different versions from 2 to 26 slots. Spacing is on 0.625 (5/8") or 0.75 (3/4") inch centers. The backplanes support both STD and CMOS STD Bus cards with no termination required.

Power Supplies - Two types of high efficiency switching power supplies are available for the card cages: 50W and 100W. They are available in a number of different configurations for both embedded and DOS compatible systems.

WinSystems' STD Bus enclosures provide a foundation for STD DOS XT/AT and non-DOS embedded systems. They serve as a platform for industrial computer based products, enclosures for self contained OEM systems, or as a prototype shell for systems development. They are user configurable since the CPU, I/O and memory boards, disk drives, power supplies can all be added to the unit to customize it to the specific application.

The enclosures are available in three different product styles; however, two types are appropriate for the STD-AT system. The ENC-100 series is a 19" rack mount enclosure for STD Bus cards and the ENC-200 is an instrument case with power supply for STD Bus cards. Both the ENC-100 and ENC-200 enclosures are supplied with a WinSystems' high performance backplane with voltage status LEDs. The different enclosures should be selected based upon the application and its environmental conditions. Each enclosure has a series of options based upon configuration requirements. Please refer to chapter seven of the WinSystems' databook for detailed information.

2

ENC-100
Rack Mount Chassis

The ENC-100 is a rugged and versatile enclosure complete with 100 Watt power supply, fan and 20-slot STD Bus card cage on 0.75 inch centers. This enclosure is designed specifically for rack mounted industrial applications. Typical applications include automatic test stands, machine controllers and monitoring systems. For severe environments, where no mechanical disk drives are allowed, the ENC-100 can host a system that can run with solid state disks.
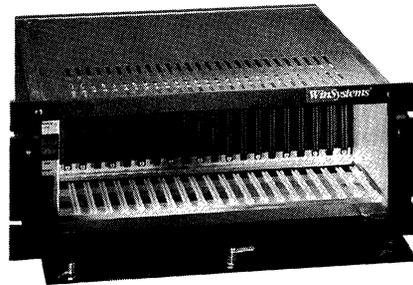
ENC-200
Instrument Case

WinSystems' ENC-200 instrument case enclosure offers a convenient packaging solution for STD Bus systems. The ENC-200 series is 21.02" wide, 6.53" high and 11.81" deep. It is a desktop enclosure with a STD Bus card rack mounted inside the unit. Many custom configurations are provided including 50 and 100 Watt power supplies; 12, 16, and 21 slot backplanes, multiple backplanes, hold down bars, locking front panel, carrying handles, and more.
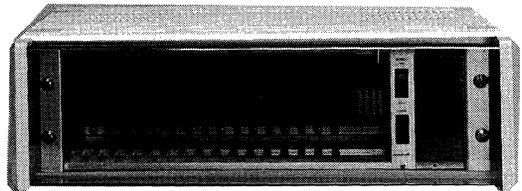
ORDERING INFORMATION

Selecting an STD-AT System - Your system can be customized by optional hardware and software to meet a range of applications. The application often dictates the amount of system memory, type of I/O interfaces and peripheral devices used in the system. The following guide is designed to help you select the appropriate features for your STD-AT system.

1. Determine your processor needs.

CPU-type	Speed (MHz)	Memory
___ 80286	10, 12, 16, 20	512Kb, 1M, 2M, 4M
___ 80386SX	16, 20	512Kb, 1M, 2M, 4M
___ 80486DX	25, 33, 50	1M, 2M, 4M, 8M
___ 80486SX	20, 25	1M, 2M, 4M, 8M
___ SX386	16, 20, 33	512Kb, 1M, 2M, 4M
___ SBC41	8, 10	512Kb, 640Kb
___ SBC53	10, 16	1MP, 1MS*
___ SBC53SX	10, 16	1MP, 1MS*

___ STD Bus or CMOS STD Bus

___ Optional math coprocessor (80287, 80387)

*P = psuedo-Static RAM, S = Static RAM

2. Software.

___ MS-DOS 5.X   ___ QNX, Version 2.x

___ ROM-DOS   ___ QNX, Version 4.x

3. Disk controller/mass storage.

___ 40M, 100M, 200M hard disk option

___ 360K, 720K, 1.2M, 1.44M floppy disk option

___ ROM/RAM solid state disks

___ IDE/SCSI hard disk

4. Video interfaces.

___ EGA/VGA   ___ Flat Panel VGA

___ LCD   ___ M/CGA

5. Communications/network controller.

___ ARCNET   ___ ETHERNET

___ RS232/485   ___ 1200/300 Bps Modem

6. Industrial Input/Output (I/O).

___ Parallel I/O   ___ Serial I/O

___ Analog I/O   ___ Intelligent I/O

7. Other miscellaneous interfaces.

___ IEEE-488   ___ Utility I/O

___ Counter/Timer   ___ Keyboard/LCD

___ PC-STD Bus Adapter ___ SBX

8. Type and size of card cage with backplane.

___ Number of slots and spacing needed:

3/4" spacing: 2, 4, 6, 8, 9, 12, 16, 21

5/8" spacing: 3, 6, 9, 12, 15, 18, 21, 24, 26

___ Type: Wall, Table, or Rack Mount

___ Power supply requirements, 50W or 100W

___ Optional hold down bar

9. Enclosure.

___ Rack Mount Chassis   ___ Instrument Case

---

10. Telephone (817/274-7553) us; or FAX (817/548-1358) this form back to us. Our applications engineers will review your system requirements and will contact you with pricing.

Name _____

Company _____

Address _____

City _____ State/Prov. _____ Zip _____

Phone   (____) _____ Ext. _____

FAX   (____) _____

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

Software

3

FEATURES

- Remote source level debugger for WinSystems V20/V25/V40/V50 and 80X86/88 family of Single Board Computers
- Supports Microsoft C version 6.x, MASM, and Borland Turbo C version 2.x
- Generates ROMable code including floating point support
- Uses standard Microsoft linker
- User friendly
- Multiple window display with pop-up menus
- CodeView style screen presentation format
- Symbolic manipulation of data variables
- Supports source only, mixed and assembly only viewing options
- Start up code source and sample program included
- Includes in-line assembler and disassembler
- Multi-feature Locator utility included
- Complete communications link between PC and target SBC
- Complete, well-written documentation
- Factory applications support

C-THRU-ROM (CTR) is a complete, comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft or Borland Turbo C for use with WinSystems' STD Bus or stand alone Single Board Computers (SBC's). It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC/XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

FUNCTIONAL CAPABILITY

Overview - C-THRU-ROM consists of several parts: The locator, local debugger, remote debugger, kernel, startup code, library, utilities, and sample program.

FREE Demo Disk
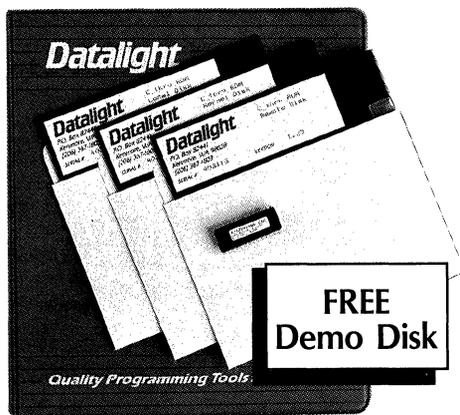
Debugger - The C-THRU-ROM windowing source level debugger provides access into the WinSystems SBC and is completely compatible with Microsoft C version 6.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote Code-View. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

The Debugger is a source level debugger. This means that the Debugger, in addition to understanding the 80X86/88 machine code, understands such symbols as function names, global variables and publics, locals, and register variables. This also means that the debugger knows about line numbers and even modules, making it possible to set break points, unassemble, and go directly to the code at any line.

With the Debugger, a listing of the program appears on the screen. One can single-step through the program lines, examine variables, execute parts of the program, and watch both program listing and the output it generates.

The lines of code are displayed as they are executed, giving one the opportunity to stop execution, examine and change variables and registers, trace a single line or instruction, or even restart the program from scratch.

Windows - The Debugger is a windowing debugger, showing the source code in one window, the typed-in commands in another, and the CPU's registers and

```
 Help—Break Point—File—Execute—Calls—Options—Display—I/O—Miscellaneous
 ┌──────────────────────────sieve.c──────┌Display───────┬─Registers─
 │ 16:     main ()                       │ Assembly  (v -)│ AX = 0004 │
 │ 17:     (                             │ Mixed     (v &)│ BX = 0FA2 │
 │ 18:         register int i,k;          │ Source    (v +)│ CX = 0019 │
 │ 19:                                   │ Next Mode (v *)│ DX = 000E │
 │ 20:         size = SIZE;               │ Registers      │ SP = 0F9E │
 │ 21:         count = 0;                 │ Window Switch  │ BP = 0FA6 │
 │ 22:                                   │ Expression     │ SI = 0001 │
 │ 23:         for( i = 0; i <= size; i++ )    /* Set │ Cls     │ DI = 0FBE │
 │ 24:            flags[i] = TRUE;         │ Up      │ CS = 5BF0 │
 │ 25:                                   │ Down    │ DS = 5D60 │
 │ 26:         for( i = 2; i <= size; i++ ) │ Output  │ SS = 5D60 │
 │ 27:         (                         └─────────┘ ES = 5D60 │
 │ 28:            if ( flags[i] )    /* Found a prime */      IP = 0032 │
 │ 29:             (                                          FL = 0202 │
 │ 30:                k = i + i;                              no carry │
 ├──────────────────────── Command Window ═══════════════════ no parity │
 │>view *                                                      no aux │
 │  source                                                     non zero │
 │>trace                                                       sign (+) │
 │>? flags[i]                                                  int (ena) │
 │   =   (char) '\x00'                                         dir (inc) │
 │>mix                                                         no ovflow │
 └─────────────────────────────────────────────────────────────────────┘
```

flags in a third window. Pop-up menus give full support for all commands.

Four windows can be open and displayed on the screen at one time. Each window has specific functions: Source (top), Command (bottom), Expression (above the Source Window), and Register (right).

The Source Window displays the source code, assembly code, or a mixture of source and assembly code. Listed at the top of the Source Window is the name of the current file that is being displayed.

The Command Window displays the commands as they are entered, and any output produced.

The Expression Window is an optional window which displays both *watch* expressions and *assert* expressions. The values in this window are updated at each trace point, break point, and continually during execution mode.

The Register Window displays the values of the target 80X88/80X86 registers. The flags register is displayed in both text and hexadecimal value.

Pop-Up Menus - The pop-up menus are a simple and easy way to access most of the commands. Pop-up menus allow the user to select the required command by a simple keystroke instead of memorization of cryptic commands. The menu selections are HELP,

Break Point, File, Execute, Calls, Options, Display, and Miscellaneous.

Locator - The multi-feature locator utility converts a normal MS-DOS formatted .EXE program into a program that can be placed within a specified location in the SBC's CPU memory address space either by segment or class name. The output program can be in Intel Hex, Intel OMF, binary, or HP64700 Emulator format.

The CTR locator, LOC.EXE, operates on the executable (.EXE) and map file (.MAP) as produced by a normal link. The .MAP file and the user created LOC file contains the segment and class names, the sizes of each segment, and the segment starting address to specify where to locate the program in ROM and/or RAM.

Kernel - The kernel is a small program (under 8K bytes) resident in the WinSystems target SBC that is being debugged and provides access to the host PC. It handles the debugging interrupts and process switching, supports a communications device, and accepts the commands from the Remote Debugger (RDEB).

The kernel monitors the UART in the target SBC for commands from the remote debugger, RDEB, performing such tasks as reading and writing target system memory, I/O ports, and executing program code on

C-THRU-ROM COMMAND SELECTION

Command	Menu Selection	Command	Menu Selection	Command	Menu Selection
ASSEMBLE	I/O	EXECUTE	Execute	REGISTER	I/O
ASSERT POINT	Break Point	FILL	I/O	RESTART	File
BIND	Miscellaneous	GO	Execute	SAVE	Miscellaneous
BREAK POINT SET	Break Point	HELP	Help	SWAP	Options
BREAK POINT CLEAR	Break Point	IN	I/O	SWITCH	Display
BREAK POINT DISABLE	Break Point	INW	I/O	SYMBOL	--
BREAK POINT ENABLE	Break Point	LOAD	File	TAB	Options
BREAK POINT LIST	Break Point	MACRO	--	TRACE	Execute
CHKSUM	--	MOVE	I/O	UNASSEMBLE	I/O
CLS	Display	OUT	I/O	UP	Display
COMPARE	I/O	OUTW	I/O	VERSION	Miscellaneous
DELAY	Options	PAUSE	Options	VIEW	File
DOWN	Display	PROGRAMSTEP	Execute	WATCH	Break Point
DUMP	I/O	QUIT	File	XAMINE	I/O
ENTER	I/O	RADIX	Options	YANK	Break Point
EVALUATE	--	REDIRECTION	--		

the target system. These simple functions allow the host PC sufficient access to the target machine to download, modify, display, and execute a program on that target machine.

The kernel supports full communication and interaction between the PC/XT/AT and the target SBC. The systems are connected via a standard RS-232 serial link on the target and COM1 or COM2 on the PC. No PROM programming is required during the development cycle. This allows C programs to be debugged while executing on the actual target hardware for real time remote debugging.

Startup Code - The C-THRU-ROM startup code provides the ability to take the application from a cold boot to calling the main C function. The startup code supports all Microsoft C memory models and is provided in MASM compatible source.

The startup code sets up the stack and heap in RAM. The initialized data is copied to RAM, and the uninitialized data RAM is zeroed. All segment registers are setup for proper C operation.

The startup code also has several features for debugging. The startup will check for stack overflow and null pointer assignments. The startup can also install an interrupt 21H (DOS call interrupt) for trapping unexpected DOS calls.

The hardware initialization code is localized into a single file.

All startup code configuration constants are placed in a special Include file. The configurable parameters determine if a power-up segment should be generated, if floating point is to be used, the stack size, and the amount of available RAM.

The startup code is the assembly code that initializes the WinSystems SBC's CPU and then calls the C function *main* (). The jobs of the startup code are to initialize the hardware (for a ROMed program), set up the stack and heap, copy the initialized data to RAM, and zero uninitialized data. WinSystems provides a diskette with C-THRU-ROM that contains the source code for the kernel that is unique to the WinSystems' SBC that you have purchased.

ST.INC contains the necessary options for configuring the startup code. There are 11 options that can be set. Some of these cause other files to be included during assembly, some affect error trapping, allow floating point or change the memory model.

ST.INC Options

memX	Which C memory model shall this startup code work with
BIOSEXT	Is the file BIOSEXT.INC included?
POWERUP	Is the file POWERUP.INC included
HARDINIT	Is the file HARDINIT.INC included in the start up code?
FLOATING_PT	Should the floating point package be included?
FP8087	Is in-line 8087 floating point used?
NULL_PTR_CHK	Should NULL pointer assignment be trapped as an error?
INT_21_CHK	Should INT21H be trapped for an error code?
USEREXIT	Does the user wish to define their own exit() function?
STACKSIZE	This defines the size of the stack, in bytes
DATASIZE	This defines the size of the near heap in Kbytes

Library - The ROMable library provides a few important C functions that can be used in a ROM environment. It is distributed in both source and library (.LIB) form. It is not intended to replace the Microsoft or Turbo libraries, but to supplement them.

The following programs are found in the library:

assert	exit	puts
chkmem	malloc	printf
cli	putch	free

Utilities - There are four utilities provided: AS, COMM, KERNTEST, and LOADGO. AS.EXE is the Add Symbols utility that will add source level information to a program what was built with a compiler other than Microsoft. COMM.EXE is a communications program to help in the process of remote debugging and to provide access to the WinSystems' Bulletin Board. It supports xmodem file transfer, autodialing, and simple terminal emulation. KERNTEST.EXE is a simple functional test to the kernel on the WinSystems' SBC to verify it is communicating with the host PC. LOADGO.EXE is used to download a program or data into RAM on the WinSystems' SBC and then begin execution of the program.

Sample Program - A sample programs is included with C-THRU-ROM on the distribution diskette. The program is compiled and ready to be downloaded into the WinSystems' target SBC and executed. Its purpose is to provide a simple C source code example so that the user can become quickly familiarized with the overall operation of C-THRU-ROM with a debugged, working program.

Run Time ROM Generation - Once a program has been debugged, only a few final steps are needed to produce a run time ROM. The LOC file is modified to specify code location in the ROM. It requires the .EXE, the .MAP, and the .LOC files. This program then creates an Intel HEX, Intel OMF, or binary file that is accepted by the EPROM programmer. The EPROMs are programmed and inserted into the target WinSystems' SBC.

Technical Assistance

Support - WinSystems has a staff of trained applications engineers to answer questions about C-THRU-ROM and WinSystems' Single Board Computers. You can call 817-274-7553, write, or FAX your questions to the Applications Engineering Department. The FAX number is 817-548-1358.

WinSystems also has a 24 hour a day Bulletin Board Service (BBS). It offers application articles, example code, and technical support information. To call, you need a 300, 1200, or 2400 bps modem connected to your PC. The communications settings are 8-data bits, no parity, and one-stop bit. The BBS phone number is 817-861-8739.

ORDERING INFORMATION

C-THRU-ROM does not include Microsoft C, MASM or Borland Turbo-C since it is assumed these PC based development tools are owned by the user. The C-THRU-ROM development package includes the diskettes, RAM, target system kernel EPROM, serial I/O cable and documentation. If C-THRU-ROM is ordered at the same time as the WinSystems' Single Board Computer, the factory will integrate 804 test the system at no extra charge.

C-THRU-ROM must be specified with the CPU clock speed for the WinSystems' LPM/MCM-SBC40A and LPM/MCM-SBC53 STD Bus SBCs. This specifies a unique kernel for the card since the communications data rate is a function of the CPU frequency and not an independent baud rate clock oscillator.

CTR-M-286AT	Microsoft C Development Kit
CTR-T-286AT	Turbo C & C ++ Development Kit
CTR-M-386SX	Microsoft C Development Kit
CTR-T-386SX	Turbo C & C ++ Development Kit
CTR-M-486DX/SX	Microsoft C Development Kit
CTR-T-486DX/SX	Turbo C & C ++ Development Kit
CTR-M-CDU25	Microsoft C Development Kit
CTR-M-SBC25	Microsoft C Development Kit
CTR-M-SBC40A-5	Microsoft C Development Kit
CTR-T-SBC40A-5	Turbo C & C ++ Development Kit
CTR-M-SBC40A-8	Microsoft C Development Kit
CTR-T-SBC40A-8	Turbo C & C ++ Development Kit
CTR-M-SBC40A-10	Microsoft C Development Kit
CTR-T-SBC40A-10	Turbo C & C ++ Development Kit
CTR-M-SBC41-8	Microsoft C Development Kit
CTR-T-SBC41-8	Turbo C & C ++ Development Kit
CTR-M-SBC41-10	Microsoft C Development Kit
CTR-T-SBC41-10	Turbo C & C ++ Development Kit
CTR-M-SBC42-8	Microsoft C Development Kit
CTR-T-SBC42-8	Turbo C & C ++ Development Kit
CTR-M-SBC42-10	Microsoft C Development Kit
CTR-T-SBC42-10	Turbo C & C ++ Development Kit
CTR-M-SBC53-10	Microsoft C Development Kit
CTR-T-SBC53-10	Turbo C & C ++ Development Kit
CTR-M-SBC53-16	Microsoft C Development Kit
CTR-T-SBC53-16	Turbo C & C ++ Development Kit
CTR-M-SBC8	Microsoft C Development Kit
CTR-M-SBC88	Microsoft C Development Kit

WinSystems, Inc.

FEATURES

- MS-DOS 3.3 equivalent operating system for diskless embedded systems
- Runs entirely out of ROM
- Uses 29K bytes of ROM and as little as 5K bytes of RAM
- ROMDISK utility provided
- Supports all INT 21H DOS calls
- Supports installable device drivers
- Support for MS-DOS file system for applications that require file I/O
- Mini-BIOS used for reduced system size
- Command interpreter not required in final systems
- Executes standard .EXE and .COM files
- Does not require keyboard, video or rotational media

ROM-DOS is a MS-DOS 3.3 compatible ROM based operating system for embedded WinSystems single board computers using the 8088, V20, V40, V53, 80186, 80286, 80386SX or 80486DX series microprocessors. ROM-DOS greatly reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS has been ported to WinSystems' STD Bus, CMOS STD Bus and non-bus based single board computers. Each different board has its own mini-BIOS to support ROM-DOS. This allows easy development, debugging, loading and execution of programs written in C, Quick BASIC, Turbo Pascal, etc. that are loaded as .EXE or .COM files.

FUNCTIONAL CAPABILITY

The ROM-DOS operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied. ROM-DOS supports all documented INT 21 hex DOS Services (except networking). It will not accept unsupported BIOS calls or direct manipulation of nonexistent PC hardware. A standard ROM-DOS setup has the code for ROM-DOS and Mini-BIOS in the top 32K bytes of ROM, and the user's application program (.EXE file) and associated disk files in ROM on a ROM-disk. The ROM's containing the actual ROM-disk files are placed above the system RAM. The ROMDISK is configured as the "A" drive so ROM-DOS will search it for the initial program upon booting.

FREE Demo Disk
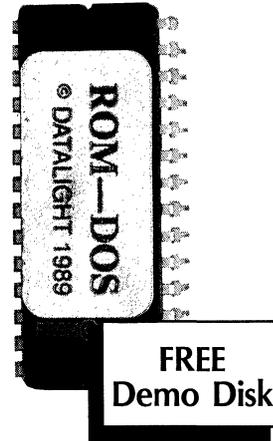
The booting process is started when power is applied to the system. The BIOS initializes the hardware and transfers control to ROM-DOS. ROM-DOS then performs its own initialization and loads the user's application program for execution. The user's program is then given control and typically remains running until the power is turned off.

Why Use ROM-DOS?

ROM-DOS is designed especially for programmers designing embedded systems software. It provides two major functions: MS-DOS compatible file support and standard device drivers.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the application code. Programs can be written in assembly, C, or high level languages such as Pascal or compiled BASIC. It supports standard MS-DOS file structures that greatly simplify data storage and retrieval. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

All development can be done on a PC and the code debugged on either a PC or the target system which completes the project in the shortest time.

ROM-DOS has been optimized to run on WinSystems' Single Board Computers (SBCs) and requires a minimum of hardware which lowers system costs. ROM-DOS uses a minimum amount of memory which

3 - 7

also reduce costs. It does not require a keyboard, video or rotational media to function which is ideal for embedded control applications.

All above the benefits add up to easy software and hardware development on WinSystems' products for embedded system applications.

Applications - ROM-DOS is suitable for a number of rugged applications such as embedded controllers, portable instruments, industrial data acquisition and control, vehicle data logging, security systems, medical instrumentation, and diskless systems.

What is ROM-DOS?

ROM-DOS is an embedded operating system. The task of an operating system is basically to supervise and direct the work of the computer and its associated peripheral devices. ROM-DOS is best described by comparisons with MS-DOS.

MS-DOS appears to be a single program but is actually a multitude of programs that can be classified into three major parts: managing of devices, control of programs, and Command processing. ROM-DOS likewise handles these same tasks. Also ROM-DOS, like MS-DOS, is made adaptable through the configuration file.

Management of devices involves interaction with the mini-BIOS as well as organizing the disk space, efficient storage of data, and retrieval. Control of programs involves the loading of programs, setting up the system for program execution, and provision for DOS services. Finally Command processing provides direct user interaction with DOS.

Command Processing

The Command processor, provided with ROM-DOS, looks and feels like the MS-DOS counterpart. The Command processor takes text commands and performs the corresponding systems calls. This program is a standard MS-DOS executable (.EXE) program. The command processor supports simple batch files, the PATH environment variable, file redirection and most MS-DOS COMMAND.COM commands.

Command processing is ROM-DOS' ability to accept and act upon operator requests through a command interpreter called COMMAND.EXE. The Command processor can carry out 4 categories of Command Interpretation which can be divided into one internal and three external.

Internal Commands - The list of internal commands varies with DOS versions. ROM-DOS is functionally equivalent to DOS version 3.3. The COMMAND.EXE shell recognizes the standard MS-DOS wildcard characters "*" and "?". It recognizes the redirection ">", ">>", and "<" characters as well.

ROM-DOS SYSTEM INTERNAL COMMAND SUMMARY	
BREAK	turns control break setting On or Off
CD	change directory
CHDIR	change directory
COPY	to and from, device or file
CTTY	change console I/O to a device
DATE	display date and prompt for new date
DEL	deletes one or more files
DIR	displays directory listing
ECHO	turns the Batch Echo on and off
ERASE	deletes one or more files
EXIT	terminate current COMMAND.EXE interpreter if not the primary
HELP	lists currently supported internal commands
MD	create a subdirectory
MKDIR	create a subdirectory
RD	remove a subdirectory
RMDIR	remove a subdirectory
REN	change a file name
SET	show system environment
TIME	set and show time
TYPE	display contents of ASCII file to console
VER	returns ROM-DOS version number

External Commands - Two of the three external commands, .COM and .EXE files, are variations on the same principle for loading of executable binary code. The .BAT file is the third external command and is an ASCII text file that the Command interpreter will attempt to execute. .BAT job control files are in a much simpler form than standard MS-DOS. Only internal commands and actual programs may be executed from within a .BAT file.

.COM and .EXE files are program files the command processor will load and execute. The difference is that .COM files are a simple, quick-loading format, while .EXE files are more complex requiring relocation fixups at load time. A .COM file is often called an image file and always uses less than 64KB of memory. .EXE programs are typically larger and require last minute processing before execution. This processing involves resolving memory addressing for loading and setting the stack.

ROM-DOS Services

ROM-DOS Kernel Interrupts - ROM-DOS is called by using the 80X88 and 80X86 software interrupt system. Interrupts 20H through 27H are reserved for these vectors.

ROM-DOS is configured to keep DOS as hardware independent as possible. This is achieved in part by the mini-BIOS and the ROM-DOS services. ROM-DOS requires "well behaved code" which does not attempt to directly manipulate nonexistent hardware to operate properly. This is obtained if the user makes Interrupt 21H ROM-DOS function calls.

The ROM-DOS service routines are all invoked by a common interrupt instruction, Interrupt 21 hex. The specific services are requested by placing the function code in register (AH) and issuing a software interrupt 21H; subfunctions are accessed in the same manner and use register (AL). Each function has individual entry and exit specifications.

ROM-DOS does not support file locking or sharing for networking support.

Configuring ROM-DOS:CONFIG.SYS

The configuration file, CONFIG.SYS, is key to ROM-DOS' flexibility and adaptability. When ROM-DOS begins operation, it looks for the CONFIG.SYS file and if it exists, reads it and follows the commands. Three ways ROM-DOS can be customized is by directing tunable parameters that ROM-DOS is already familiar with such as BUFFERS, FILES, and BREAK. The second way is with

installable device drivers and the last is with changing the initial program loading.

FILES, BUFFERS, BREAK - The number of files open at one time may be modified by using the FILES command. From 8 to 20 may be opened which include the preopened files stdin, stdout, stdprn, and stdaux.

ROM-DOS uses buffers to hold data read from disk. The number defined by BUFFERS is from 1 to 20.

The BREAK command allows the setting or resetting of the system BREAK flag. The flag, when set, causes the system to check for Control-C after each system call rather than only during console I/O.

Device Drivers - Installable device drivers are programs that expand ROM-DOS' ability to work with a variety of peripherals. This facility permits WinSystems to take advantage of new or additional hardware with ROM-DOS' character and block file handling capability.

ROM-DOS supports DOS character and block device drivers. A device driver may be installed at load time (using CONFIG.SYS).

WinSystems includes two standard device drivers: RAMDISK.SYS and CLOCK.SYS. Additional DOS compatible device drivers can be installed.

3

ROM-DOS FUNCTION CALLS

Function	Summary	Function	Summary	Function	Summary
00H	Terminate Program	1DH-20H	Reserved, Unsupported	3BH	Change Current Directory
01H	Keyboard Input	21H	Random Read	3CH	Create File
02H	Display Character	22H	Random Write	3DH	Open a File
03H	Auxiliary Input	23H	Get File Size	3EH	Close a File Handle
04H	Auxiliary Output	24H	Set Random Record Field	3FH	Read From a File or Device
05H	Print Character	25H	Set Interrupt Vector	40H	Write to File or Device
06H	Direct Console I/O	26H	Create New Program Segment	41H	Delete File (unlink)
07H	Direct Console Input	27H	Random Block Read	42H	Move a File Pointer
08H	Read Keyboard	28H	Random Block Write	43H	Get/Set File Attributes
09H	Display String	29H	Parse File Name	44H	I/O Device Control (with
0AH	Buffered Keyboard Input	2AH	Get Date		Subfunctions 00,01,02,03H)
0BH	Check Keyboard Status	2BH	Set Date	45H	Duplicate File Handle
0CH	Flush Buffer, Read Input	2CH	Get Time	46H	Force DUP Handle
0DH	Reset Disk	2DH	Set Time	47H	Get Current Directory
0EH	Select Disk	2EH	Set/Reset Verify Flag	48H	Allocate Memory
0FH	Open File	2FH	Get Disk Transfer Address	49H	Free Allocated Memory
10H	Close File	30H	ROM-DOS Version Number	4AH	Modify Allocated Memory
11H	Search For First Entry	31H	Keep Process	4BH	Load and Execute Program
12H	Search For Next Entry	32H	Reserved, not supported	4CH	Terminate Process
13H	Delete File	33H	Control-C Check	4DH	Retrieve Child Exit Status
14H	Sequential Read	34H	Reserved, not supported	4EH	Find First File
15H	Sequential Write	35H	Get Interrupt Vector	4FH	Find Next File
16H	Create File	36H	Get Disk Free Space	50H-52H	Reserved, Supported
17H	Rename File	37H	DOS-1 Internal, supported	52H-53H	Reserved, Unsupported
18H	DOS-1 Internal, Supported	38H	Get Country Information	54H	Get Verify State
19H	Get Current Disk	39H	Create Directory	56H	Change Directory Entry
1AH	Set Disk Transfer Address	3AH	Remove Directory	57H	Get/Set File Date & Time

RAMDISK.SYS is supplied with ROM-DOS to allow a portion of the system RAM to be used as a "Silicon Disk". This silicon disk would be located on either the main SBC board or on an external UMC4 card. This RAMDISK is volatile and the contents are lost with each boot. Non-volatile "silicon disk" drivers are also available and when coupled with battery backed RAM cards, provide a reliable data storage and retrieval media.

Most of WinSystems' SBC's and CPU's have an onboard real-time clock capable of maintaining time, date, and year. A CLOCK.SYS driver is provided for WinSystems hardware with the ROM-DOS port in order to access the clock. The TIME and DATE commands are used to set or read it. Also application programs can set or read the clock with the appropriate DOS Function calls.

Initial Program Loading - The SHELL command allows the user to specify an alternative command processor to the default COMMAND.EXE. Specifying the command:

SHELL = program arguments

will cause the program to be executed immediately at boot time without first loading a command interpreter.

Basic I/O System (BIOS)

The part of DOS that communicates with the computers hardware is called the Basic Input/Output System (BIOS). It contains the routines that provide the most basic, low-level control and supervision for the CPU and peripherals. Its task is to provide a bridge between the hardware and other software. Each WinSystems SBC has an individual mini-BIOS to customize ROM-DOS to the hardware.

The first part of the mini-BIOS is the start-up and hardware initialization routines. It creates the interrupt vectors, set the registers, stack, power-on-self-test (POST) and boot routines.

The mini-BIOS provides a minimum complement of BIOS services necessary for embedded systems to run ROM-DOS. The mini-BIOS provides the BIOS support for a remote console, timer, BIOS extensions, and hardware identification as well as power on testing for RAM and serial devices. The mini-BIOS does not support floppy disks, printers, or standard PC keyboard or monitor. The BIOS is small since many of the expand functions used in a desk-top PC are not needed for embedded applications. All keyboard and video operations are handled through the SBC's serial port for console I/O.

The supported BIOS functions are listed in the table below. Obviously programs that make unsupported calls

will not perform as desired. Most compilers use the operating system as their principal mode of I/O and only a few hardware specific routines need to be avoided.

The mini-BIOS supports only interrupts 10H, 11H, 12H, 16H, and 1AH as shown in the Interrupt Vector Table below.

INTERRUPT VECTOR TABLE		
Interrupt	Function Code	Function
0H	-	Divide by 0
1H	-	Trace
2H	-	NMI Interrupt
3H	-	Break Point
4H	-	Overflow
5H	-	Free
6H	-	Free
7H	-	Free
8H	-	IRQ0 - Clock Tick
9H	-	IRQ1 - Keyboard
AH	-	IRQ2 - Free
BH	-	IRQ3 - Free
CH	-	IRQ4 - Free
DH	-	IRQ5 - Free
EH	-	IRQ6 - Free
FH	-	IRQ7 - Free
10H	-	Video Functions
	0E	Write TTY
11H	-	Equipment Report
12H	-	Memory Size
16H	-	Keyboard
	0	Get Kybd Character
	1	Check Key Available
	2	Read Shift Status
19H	-	Force Warm Boot
1AH	-	Get/Set Time of Day
	0	Read Time of Day
	1	Set Time of Day
20H	-	Program Terminate
21H	-	DOS Function Call
22H	-	Terminate Address
23H	-	Control Break Handler
24H	-	Critical Error Handler
25H	-	Absolute Disk Read
26H	-	Absolute Disk Write
27H	-	Terminate and Stay Resident
28H-3FH	-	Reserved, unsupported

Hardware Environment

ROM-DOS is ported to many of WinSystems Single Boards Computers some of which are fully PC compatible and others that are not. ROM-DOS is designed to communicate through a serial channel rather than a standard keyboard and video display. Programs should not attempt to bypass ROM-DOS and manipulate the PC style hardware directly. Embedded systems typically do not have screens or PC style keyboards and programs that do output by writing directly to the screen memory (i.e. QuickBASIC) will not function as desired. This is not to say that the system hardware cannot be manipu-

lated by a custom application program or driver, but only that some canned programs or library routines will not be cognizant of the actual hardware present.

ROM-DOS is currently supported on the following WinSystems boards:

- LPM-SBC40
- LPM-SBC41
- LPM-286AT
- LPM-386SX
- LPM-486DX
- LPM-SBC53
- MCM-SBC40
- MCM-SBC41
- MCM-SBC53
- MCM-286AT
- MCM-386SX
- MCM-486DX
- SBC-88
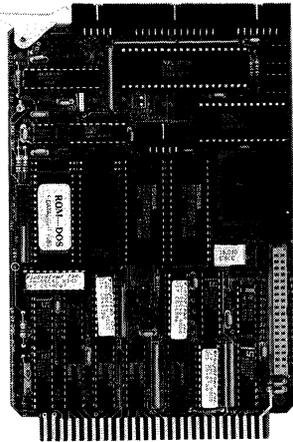
Memory Allocation - ROM-DOS is very memory efficient. A typical memory allocation will take less than 32K bytes for ROM-DOS and the mini-BIOS and 5K bytes of RAM. Additional memory is a function of the application program and any RAMDISK or ROMDISK storage requirements.

EXAMPLE MCM-SBC40 MEMORY MAP		
ADDRESS	USE	ALLOCATION
00000H-7FFFFH	System RAM	512KB
80000H-BFFFFH	Application ROMDISK area	256KB
C0000H-CFFFFH	Reserved for user	64KB
D0000H-EFFFFH	UMC4 based RAMDISK	128KB
F0000H-F7FFFH	Reserved for system	32KB
F8000H-FF3FFH	ROM-DOS	29KB
FF400H-FFFFFH	Mini-BIOS	3KB

DISK FILE Management

ROM-DOS accesses files through an organized hierarchical directory system which supports volume label

and file attributes. The I/O system handles DOS's disk filing system and communications with peripheral devices such as communications, printers, etc. The Command processor has several built in functions or subprograms that handle most of DOS's common tasks such as copying files, display, etc.

Solid State Disk Drives - The obvious difference between ROM-DOS and MS-DOS is the amount of EPROM space and rotational memory required. Embedded systems imply construction that will not allow desktop PC's to fit. Power consumption, heat dissipation, shock, vibration and cooling dictate that standard floppy or hard disks will be prone to failure in this environment. The obvious solution is to replace the rotational media with solid state disk drives.

ROM-DOS gives you the tools to reserve a portion of the available memory space and substitute the functionality of a disk through onboard semiconductor devices such as EPROMs and nonvolatile RAMs. The devices can be installed in the spare memory sockets on the boards to act like normal disk drives which can boot the system and run programs.

ROMDISK -The Read only files used for initial program loading and execution can be easily stored in EPROMs on one of the WinSystems SBC's using the ROMDISK utility. This program resides on the host PC and gathers all the necessary files together to build a ROMDISK. The ROMDISK program will keep a tally of the total space used as each file is added. It will prompt for a output file name and make a disk image. The program will then read all specified files and write the output to the file name given. This file can be burned into one or more EPROMs using a standard EPROM programmer. The EPROMs are then installed in the appropriate sockets on the SBC or auxiliary memory board. No special software tools or programming techniques are needed.

RAMDISK - A user installable silicon disk driver, RAMDISK.SYS, is provided that allows a portion of system RAM to be used as a disk drive. It is reinitialized at each boot up and is acts as a temporary storage medium for volatile data. WinSystems also has drivers for battery backed RAMDISKs which provide a READ/WRITE mass storage option for data.

Other installable device drivers are available for removable memory cards, memory cartridges, tape drives and cartridge memories from companies such as Enlode and Databook. Contact WinSystems' applications engineering department at the factory for specific details on your applications and specific hardware interface.

3

ROM-DOS Development System

ROM-DOS should be ordered initially preconfigured as a "ready-to-run" system. The selected WinSystems' single board computer will be shipped with 2 ROM-DOS EPROMs installed, a 5 1/4" utilities disk, serial communications cable, and a minimum amount of RAM. This permits a user to have a totally working system to begin development.

ROM-DOS EPROM - Two EPROMs are shipped with a system. The first contains ROM-DOS and the mini-BIOS. The second EPROM is a ROMDISK configured to operate as drive A: with a sample program installed.

Utility Diskette - A 5 1/4" diskette is supplied with the following files: COMM.EXE, COMMAND.EXE, CONFIG.SYS, CLOCK.SYS, RAMDISK.SYS, TRANSFER.EXE, AUTOEXEC.BAT and SAMPLE.EXE.

COMM.EXE is a program to allow communications with the remote ROM-DOS. It resides in the host PC and supports xmodem file transfer, autodialing, and simple terminal emulation. COMMAND.EXE is the ROM-DOS command interpreter that may be required by the application program. CONFIG.SYS permits system configuration at start up. CLOCK.SYS and RAMDISK.SYS are installable device drivers. TRANSFER.EXE is a utility program that allows files to be down loaded via serial port console to the ROM-DOS system during debugging. TRANSFER.EXE resides in the silicon disk in the ROM-DOS system and communicates with COMM.EXE in the host PC. AUTOEXEC.BAT is the auto executing batch file. SAMPLE.EXE is the sample program provided by WinSystems.

Cable - A serial cable is provided to link the WinSystems' SBC to the host PC for communications during debug.

ORDERING INFORMATION

RDOS-286AT	ROM-DOS for the LPM/MCM-286AT
RDOS-386SX	ROM-DOS for the LPM/MCM-386SX
RDOS-SBC40R-8	ROM-DOS for the LPM/MCM-SBC40-8
RDOS-SBC40R-10	ROM-DOS for the LPM/MCM-SBC40-10
RDOS-SBC41R-8	ROM-DOS for the LPM/MCM-SBC41-8
RDOS-SBC41R-10	ROM-DOS for the LPM/MCM-SBC41-10
RDOS-SBC53R-10	ROM-DOS for the LPM/MCM-SBC53R-10
RDOS-SBC53R-16	ROM-DOS for the LPM/MCM-SBC53R-16
RDOS-SBC53RX-10	ROM-DOS for the LPM/MCM-SBC53RX-10
RDOS-SBC53RX-16	ROM-DOS for the LPM/MCM-SBC53RX-16
RDOS-SBC88R	ROM-DOS for the LPM/MCM-SBC88

WinSystems, Inc.

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FEATURES

- QNX 2.15 and 4.x supported
- Supported on WinSystems' industrial STD Bus 286/386/486 CPU's
- High-performance, real-time, multi-tasking
- Low overhead, small OS kernel
- Preemptive priority based task scheduler
- Fast task switch time
- "Seamless networking" with transparent access of resources attached to any node
- POSIX compliant Real Time OS (QNX 4.x)
- Applications can be written in C, assembler and FORTRAN and other languages
- QNX Windows supports OPEN LOOK user interface standard
- Supports remote Netboot
- RAM/ROM DISK support
- Complete operating system, not just an executive
- Does not require hard disk or video to operate
- Standalone or network configurations supported
- Distributed processing over flexible peer-to-peer ARCNET (2.15 & 4.x) or Ethernet (4.x) networks
- Extensive 3rd party support with application software, software tools, training, and consultants
- Bulletin Board with over 1800 files of free software including games, graphics, demos and powerful applications

For industrial applications that require small, modular, networked, reliable, and cost effective solutions, WinSystems offers the QNX operating system. It is a real-time, multi-tasking operating system, with the proven, industrial strength STD Bus. The combination provides users with the perfect blend of software and hardware platforms for use in factory automation an harsh environments.

Both QNX 2.15 and 4.x are supported by WinSystems' STD-AT compatible computers. It will run on small diskless embedded controllers without requiring video ("blind nodes") up through large systems with multiple disk drives.

Whether you are running a network of four or 400 machines, QNX makes it all feel like a single computer. Interprocess communication is network wide, so every process can transparently access every resource — programs, files, devices, even CPUs — anywhere on the network. It supports both the ARCNET and Ethernet local area networking schemes.

QNX 4.x extends the capabilities of QNX 2.15 while maintaining the fundamental design. QNX 4.x is still a
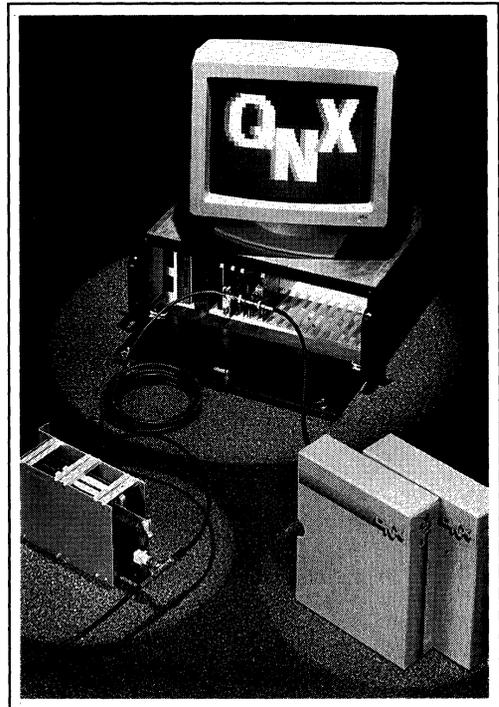
multi-user, multi-tasking, distributed, modular, message-passing, operating system. QNX 4.x also provides many functions and features not found in 2.15.

FUNCTIONAL CAPABILITY

Overview - Todays computer users are demanding open systems to solve their computing problems. In the past, real-time applications — process control, communications, automation and high-speed data acquisition — were handled with proprietary computer solutions because of performance demands. With current hardware and software technology, it is possible to use an open systems concept to demanding real-time environments. QNX combines real-time performance now with WinSystems' industry standard hardware STD Bus platforms. Over 170,000 QNX nodes have been installed in over 47 countries.

QNX is designed to provide real-time performance that is not possible with conventional operating systems. It allow users to prioritize multiple time dependent asynchronous tasks and guarantees quick responses to external events. QNX provides the

connectivity and user-friendly interface essential in todays computer world but rare in real-time systems.

QNX is designed from the ground up as a network-wide operating system. In some ways, a QNX network feels more like a mainframe computer than a set of micros. Users are simply aware of a large set of resources available for use by an application. But unlike a mainframe, QNX provides a highly responsive environment, since the appropriate amount of computing power can be made available at each node to meet the needs of each user.

QNX's exceptional ability to facilitate distributed processing and intertask communication make it an excellent candidate for process control and other industrial applications. In a process control environment, for example, PLCs and other real-time I/O devices may require more resources than other, less critical applications, such as a word processor. The QNX network is responsive enough to support both types of applications at the same time. QNX lets you focus computing power on the plant floor where and when it is needed, without sacrificing concurrent connectivity to the clean room.

QNX offers a migration path since it is available for many different computers and Intel-based micros including the 8088, 286, 386, or 80486 for large computers with multiple disk drives through small diskless embedded systems on the factory floor.
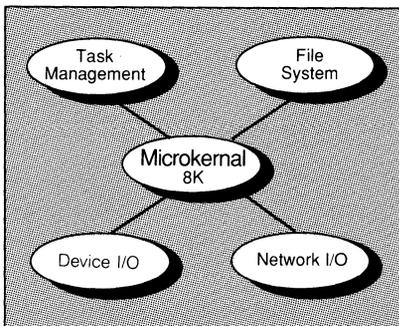
QNX's 8KB microkernal coordinates cooperating tasks.

QNX, A Modular OS - Unlike monolithic systems, QNX consists of a microkernel (10Kbytes) in charge of a team of cooperating tasks. The microkernel's main job is to schedule tasks and to coordinate message passing activity. All other functions of the OS such as file handling, network management, device I/O, etc. are handled by accessible modules known as Server

Tasks. QNX's modular design lets you customize the OS by using only those Server Tasks needed for a specific application. You can run a standalone or networked system, add and test device drivers, or even load a guest file system without having to take apart and rebuild the entire OS.

Program Development Environment - Complete multi-tasking/multi-user support in QNX simplifies and speeds development of software projects. The target computer can be used as the software development system. QNX is supported by a complete set of software development tools including Compilers (ANSI, K & R, C++, FORTRAN, to name just a few), Assemblers, full-screen editor, symbolic debugger with core dump analysis, a host of utilities and libraries, and multiple full screen windows.

Most real-time systems force you to develop your application on one machine and then run it on another. With QNX you are working in an integral environment, where your development system and your target system can be one and the same.

Distributed Processing - QNX is grounded on the principle that effective communication is the key to effective operation. The key to QNX's efficient modular design and distributed computing capabilities is a simple yet powerful technique known as message passing. Message passing thus forms the cornerstone of QNX's architecture and enhances the efficiency of all transaction among all processed throughout the entire system, whether across a STD Bus backplane or across a mile of coax.
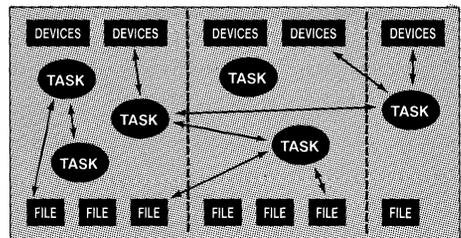
A QNX network appears to be a single computer consisting of tasks, files, and devices.

Tasks communicate with each other via messages, whether they reside on the same machines or on distant nodes. The reason they communicate so effectively is that QNX was designed with interprocess communication (IPC) as its very foundation, not as an after thought as in most other systems.

Thanks to its uniform, network-wide IPC, QNX creates an environment in which an application can harness the processing power of all the CPUs on the entire network. To each user, a QNX network feels like one homogeneous computer, regardless of the physical distribution of the machines.

Networking - QNX's ability to network a group of PC's in a UNIX-like environment is its most powerful asset. QNX doesn't require any additional software, only a WinSystems' MCM-ANET ARCNET card in each node. The MCM-ANET is ported to the QNX OS and will work only with WinSystems' AT compatible CPU boards. Nevertheless, machines running this version of QNX can coexist on a QNX ARCNET network with machines running PC, AT, or STD QNX on Qnet ARCNET cards. The MCM-ENET is the Ethernet card that is supported by QNX 4.x.

Peer-to-Peer Operation - QNX allows every machine to be both a file server and a workstation. Every machine can have one or more hard disks, or it can be without any disk drives, booting from the network. Any node on the network can start tasks on any other node of the network, read any file on any disk on any node, or make use of any device on any node.

Multi-tasking - QNX supports up to 64 tasks on a XT and 250 tasks on an AT class machine. DOS can be supported as a task. Real mode execution is supported on PC's. Protected mode execution is supported on 80286 and above equipped machines, providing up to 16M bytes of memory for executing tasks.

Embedded Systems and ROMability - The compact size of the microkernel with its real-time responsiveness, makes it attractive for intelligent embedded systems operating standalone or in a network.

QNX will support embedded applications where a hard disk is not available. WinSystems offers a solid state disk which is designed to replace conventional rotational disk memories in harsh applications which will permit the application to boot up and run.

Netboot Support - For embedded systems, the STD-AT will boot without a keyboard, video card, and floppy disk or hard disk installed by accessing the network servers for its OS files and application. The MCM-ANET boot ROM will generate the request to the server.

The NETBOOT server utility is shipped standard with WinSystems' version of QNX 2.15 and will accept boot requests from machines that wish to boot over the network. Upon receiving boot request, NETBOOT downloads the operating system to the requesting machine.

QNX 4.x

QNX 4.x is a POSIX-compliant OS based on micro-kernel technology. POSIX (Portable Operating System Interface, X as in Unix), an IEEE operating system interface standard, will serve as the common denominator among all the various UNIX and UNIX-like systems on the market. The advantages of POSIX compliance are many. Existing QNX developers can participate in the standards trend and can enter larger markets for their products without sacrificing performance. It is a simple matter for anyone who has written POSIX-conforming code to port their application to the QNX 4.x environment. QNX 4.x offers the realtime performance that no conventional UNIX system could ever deliver.

With a task switch speed of 27 uS per task switch on a 33 MHz 386 (18 uS on a 486), QNX is comparable in performance to dedicated realtime executives.

QNX 4.x follows the IEEE POSIX group of standards, so that it provides all the benefits of a real UNIX system. POSIX QNX gives users a much broader base of networking capabilities, but more importantly, the microkernel architecture continues to give engineers the flexibility they want without sacrificing the real-time performance that they need.

Who Should Move To 4.x? - The answer to question is based upon R&D costs and technical issues. If you have developed an application that works fine under existing QNX 2.15 and don't plan to make any significant changes or upgrades, then you should probably stay with it.

If you are about to start a major new project or re-work an existing one, then you should consider 4.x. This new QNX brings an operating system with enormous performance, flexibility, and feature enhancements. It represents over 10 years of operating system design focused on a single new product for todays embedded hardware environment. It also embraces the trend towards open system by adhering to the POSIX standard for the operating system interface.

HARDWARE ENVIRONMENT

Industrial Strength QNX - In harsh industrial environments, most conventional PC platforms, including so-called "ruggedized" PCs, simply are not tough enough to drive process-critical applications. Moreover, they are usually too unwieldy to be embedded in machinery or instrumentation. WinSystems' STD-AT is an alternative platform to deliver QNX-based solutions for a variety of demanding industrial conditions.
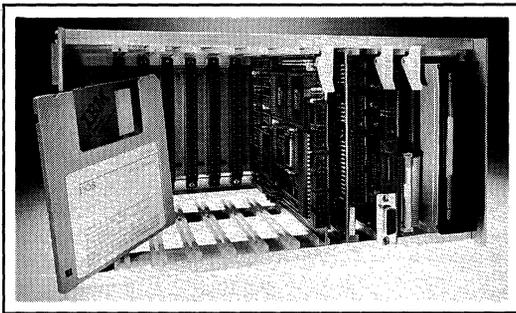
3

STD-AT - The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the de facto "software bus", for hosting operating systems utilities, real-time executives, development tools, networking, and application specific programs. The combination of hardware and software standards assure flexibility when designing and configuring a rugged industrial computer.

Our STD-AT is a true software compatible PC-AT compatible industrial computer. It combines the powerful processing capability of the 80286/386/486 and vast library of PC-DOS software with the reliability and industrial I/O interfaces of the open architecture IEEE 961 STD Bus.

The STD-AT is a product family that covers a number of system components that combined together create a STD Bus PC-AT compatible system. The system components can be categorized as CPUs, memory, disk controllers, video controllers, communications/network controllers, various I/O cards, and powered card racks. The result is an industrial grade, small form factor, completely software AT-compatible system with CPU operational speeds from 10 to 50 MHz.

WinSystems' CPUs

Product	CPU-type	Speed (MHz)
MCM-486DX	80486DX	25, 33, 50
MCM-486SX	80486SX	20, 25
MCM-386SX	80386SX	16, 20
MCM-286AT	80286	10, 12, 16, 20

Packaging Flexibility - The small size of the STD Bus cards, 4.5" x 6.5" , make them ideal for use in disguised and embedded industrial controller applications. The small format is designed for industrial environments since the cards don't bend or flex and are engineered to stand shock and vibration. The format and low cost of STD Bus cards make their maintenance simple, quick, and economical.

The open architecture of the system allows for 8- or 16-bit I/O expansion modules. And the STD-AT upgrades to meet new requirements while operating under a DOS environment.

I/O Flexibility - I/O interfaces are available for pressure and temperature measurement, stepper and large motor control, analog and digital interface, networking, video graphics, and so on. Users can easily design and construct their systems, since the STD Bus offers a larger variety of interface cards than any other bus. In fact, many special I/O interfaces that must be custom-made for other buses are often off-the-shelf products with the STD Bus.

Extended Operating Temperature Range - The 80C286 based STD-AT is also available for the CMOS STD Bus. CMOS offers very low power, improved noise immunity, and extended temperature (40°C to +85°C) operation. CMOS STD Bus boards typically draw 90% less power than their NMOS/TTL equivalent. Some of the advantages of lower power requirements are low system operating temperatures, reduced internal heating, no fans, smaller power supplies, and sealed enclosures.

Net Boot Support - For networked embedded systems, the STD-AT will boot without a keyboard, video card, and floppy disk or hard disk installed by accessing the network servers for its OS files and application.

Solid State Disk Drives - Embedded systems imply construction that will not allow desktop PC's to fit. Power consumption, heat dissipation, shock, vibration and cooling dictate that standard floppy or hard disks will be prone to failure in this environment. The obvious solution is to replace the rotational media with solid state disk drives. WinSystems' STD-AT can run QNX without a disk by using a solid state disk drive.

Solid state disks (SSD) have a number of advantages over magnetic media drives. They have a low power consumption and do not have the start-up surge currents characteristics of rotational media. They are resistant to environmental factors and can operate over a wide temperature range. SSD drives have high reliability because they dissipate very little heat an there are no moving parts.

The MCM-SSD-QNX is a WinSystems' solid state disk subsystem. The board will support both a bootable RAM and ROM disk. The board acts like a very fast rotational disk drive which can both boot the system and provide program/data storage.

Other QNX Tools

QNX Windows - QNX Windows provides developers the benefits of graphical user interfaces (GUIs). It offers both the look and feel of AT&T's OPEN LOOK interface. It is a fast, responsive, user-friendly package designed for real-time applications and equipped with integrated networking and distributed processing already built in.

C Compiler - This is a full Kernighan and Ritchie C with shared memory support. It supports floating point operations via software or 80X87 coprocessors. Other features include:

• Assembler
• Symbolic debugger with core-dump analysis
• Make utility, network-distributed parallel Make also available
• Nearly 450 library routines
• Terminal support

QRCS: QNX Revision Control System - This program stores and retrieves multiple revisions of a file. It logs a complete history of changes made to a file. It also supports version locking to eliminate access conflicts.

Ditto - This is a remote access screen sharing program that allows any computer or terminal to transparently access the screen of any other computer via LAN or modem. It supports remote keyboard control, including remote rebooting. It also allows access to video data of unattended console-less embedded systems. This product is ideal for remote on-line technical support, remote debugging, class room training, etc.

RUNDOS - This program is a DOS emulator that runs many popular DOS applications under QNX. Users do not need to supply DOS itself. It includes a DOS file system which provides live access to DOS files from QNX programs. An application runs as a single task within the QNX multi-tasking, multi-user environment. It supports one DOS session at each network node or standalone computer.

QNX Support

QNX 3rd Party Support - QNX is supported by a network of vendors, VARs, OEMs, and consultants that offer a number of products and services. A 3rd-Party Products Guide and Consultants Registry is published regularly to help users find information on QNX related hardware, application software, development tools, training, integration, and services throughout the world.

Bulletin Board - There is an on-line, 24-hour QNX bulletin board available for licensed users where one can download free software updates and utilities, upload sample code for analysis, as well as joining other QNX users in discussions on a variety of topics.

The free software area of the BBS contains over 1,800 archived files (25Mbytes). The files range from code fragments that describe the use of the more exotic selections available, all the way to games, graphics, commercial demos and powerful application programs. Much of the software has been donated by QNX users.

QNXnews - Registered QNX users also receive a subscription to QNXnews. It is a quarterly newsletter featuring application stories, the latest third-party products, technical tips, a registry of QNX consultants, and other news that affects the QNX world.

Annual User's Group Conference - Each year, hundreds of QNX users from around the world gather together for three days of presentations, product exhibits, and Q&A sessions hosted by Quantum Software Systems Limited. This world-class conference has become one of the most exciting product centered user groups meetings in the industry.

3

ORDERING INFORMATION

QNX 2.x from WinSystems includes the ARCNET interface and remote boot capability. It also includes the solid state disk RAM/ROM driver utilities for use in diskless remote embedded applications.

QNX is available as a single node or as additional expansion nodes in a system. The expansion nodes do not include detailed documentation and are less expensive. If you run QNX as a network, you will need our ARCNET card with BIOS extension. The ARCNET boot ROM is the same for both versions 2.x and 4.x.

Other QNX Tools:

QNX QTERM	Communication/terminal emulation program
QNX DITTO	Interactive screen sharing program
QNX RUNDOS	DOS emulator and DOS file system administrator
QNX MAIL	Electronic mail
QNX QRCS	Source Code management system

QNX Configuration Guide

PART NUMBER: QNX - X - X X - X X X

— Number of Nodes

SC = Single Computer (with documentation)

2 = Version 2.x (latest release) —   RT = Run Time (no documentation)

4 = Version 4.x (latest release) —   NE = Network Expansion
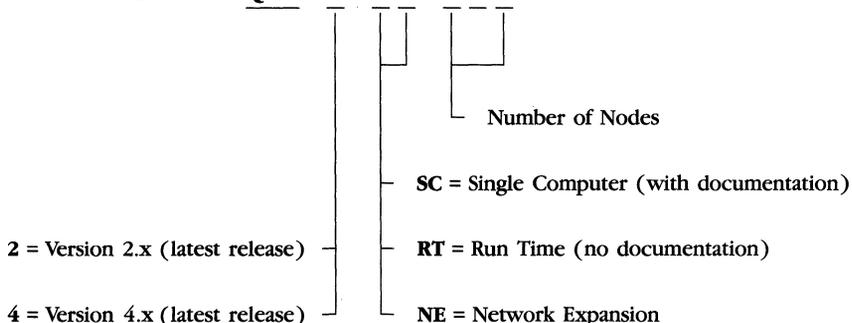
Examples:

QNX-2-SC-001
Description: QNX OS version 2.x single user Development system with documentation

QNX-4-NE-003
Description: QNX OS version 4.x three user network expansion

NOTE: If you operate an QNX OS network, you will need our ARCNET card with a BIOS extension.

LPM-ANET-AB-QNX   CMOS ARCNET card for coaxial bus or star topology

MCM-ANET-AB-QNX   ARCNET card for coaxial bus or star topology

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WinSystems, Inc.

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Processors

16- and 32-bit Processors

8-Bit Processors

MCM prefix on a product name designates a STD Bus card and a LPM prefix designates a CMOS STD Card. The LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS STD Bus and STD Bus logic. The differences between these products are the various power requirements and operational temperature ranges.

PRODUCT	TECHNOLOGY	CPU	SPEED (MHz)	COPROCESSOR SOCKET	(EP) ROM KBytes (MAX)	RAM KBytes (MAX)	MEMORY ADDRESSING MBytes	SERIAL	PARALLEL	TIMERS	RTC
LPM-286AT	CMOS	80C286	10, 12, 16 20	X	128	4096	16	2	1 LPT	3	X
MCM-286AT	NMOS/TTL	80286									
LPM-386SX	CMOS	80386SX	16, 20	X	128	4096	16	2	1 LPT	3	X
MCM-386SX	NMOS/TTL										
MCM-486DX	NMOS/TTL	80486DX	25, 33, 50	—	128	8192	16	2	LPT	3	X
MCM-486SX	NMOS/TTL	80486SX	20, 25	—							
MCM-DSP32C	NMOS/TTL	DSP-32	50	—	—	512	1024	1	1	—	—
LPM-SBC8	CMOS	80C88 8088	5, 8	X	128	64	1	1	24	3	OPT.
MCM-SBC8	NMOS/TTL										
LPM-SBC40A	CMOS	V40	5, 8, 10	—	1024	1024	1	2	24	3	X
MCM-SBC40A	NMOS/TTL										
LPM-SBC41	CMOS	V40	8, 10	—	1024	1024	1	3	24	3	OPT.
MCM-SBC41	NMOS/TTL										
LPM-SBC42	CMOS	V40	8, 10	—	512	512	1	3	24	3	OPT.
MCM-SBC42	NMOS/TTL										
LPM-SBC53	CMOS	V53	10, 16	X	1024	1024	16 (WITH PAGE MODE)	3	LPT	3	X
MCM-SBC53	NMOS/TTL										
LPM-SX386	CMOS	80386SX	16, 20, 25 33	X	512	8192	16	2	LPT	3	X
MCM-SX386	NMOS/TTL										

4

FEATURES

- 80486DX CPU with 25, 33 and 50 MHz clock
- 80486SX CPU with 20 and 25 MHz clock
- 100% object code compatibility with the 80386, 80286, and 8086/88 CPUs
- Full PC-AT software compatibility
- Supports MS/DOS, OS/2, UNIX, Windows/386, QNX and other popular PC-AT operating systems, real time executives, and application software
- 1MB, 2MB, 4MB or 8MB of parity checked DRAM
- 128K bytes of EPROM storage capacity
- On-chip IEEE 754 coprocessor for MCM-486DX
- AT standard BIOS with self test (POST)
- Shadow BIOS for improved performance
- Dynamic Bus sizing for 8/16/32-bits transfers
- 2 Serial RS-232/485 COM ports
- Asynchronous I/O bus controller assures Compatibility with slower I/O cards
- Centronics compatible parallel I/O port
- Keyboard controller
- Battery backed calendar clock
- Onboard speaker
- Three 16-bit timer/counters
- DMA and interrupt controller
- 8/16-bit STD Bus interface
- Watchdog timer
- Supports ROM-DOS embedded operating system
- +5 volt only operation
- Precision power fail reset circuit
- Small size: 4.5" X 6.5"
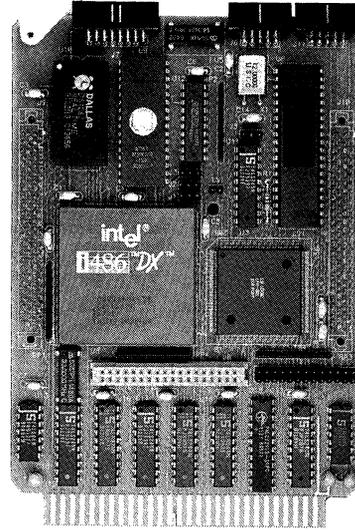
The MCM-486 is a high performance 80486 based STD Bus single board computer that can operate as a PC-AT DOS compatible or a standalone board for embedded systems applications. Configured with a 25, 33 or 50 MHz system clock and up to 8 Megabytes

*SHADING INDICATES SOCKET ONLY
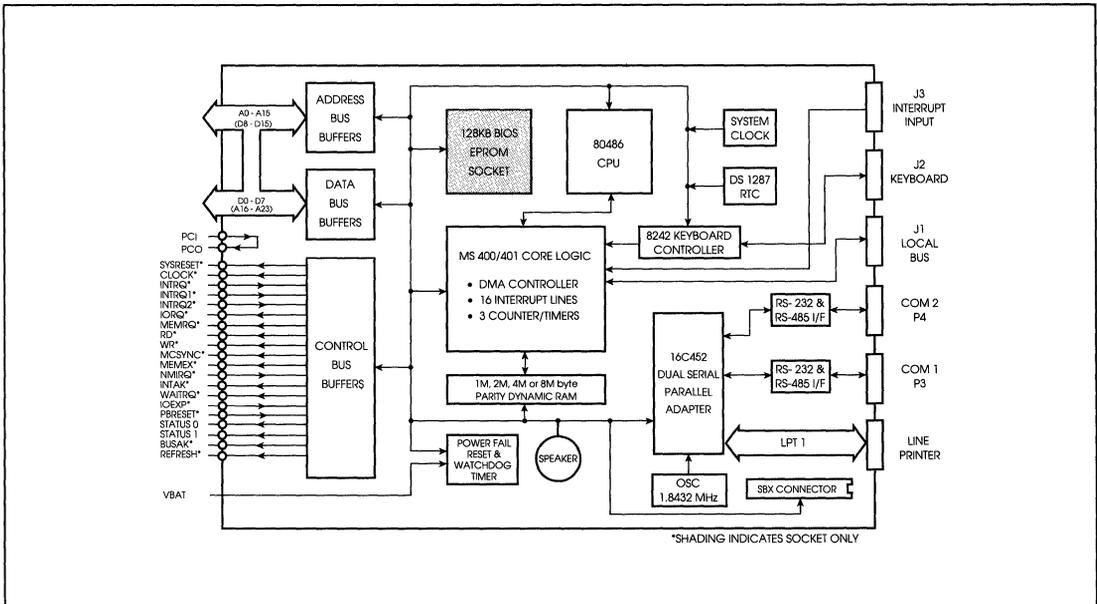
of onboard system memory, the MCM-486DX is designed to meet demanding processor intensive requirements in applications such as industrial, factory floor, automatic test, instrumentation, 40 robotics, machine control, aerospace, and other difficult environments.

By incorporating the 80486 CPU, the board's performance is approximately twice that of a 80386 based system at the same frequency. The improvement is a result of its 32-bit integer core which is optimized to executed the most frequently used instructions in only one clock cycle. Also 8Kbytes of on-chip cache, improved on-chip coprocessor, and a memory management unit add to its performance while remaining 8086 compatible. Existing WinSystems' 80286 and 80386SX systems' speed and performance are upgraded by simply changing the CPU.

The MCM-486 board is offered with either the 80486SX or DX version CPU. The differences between the SX and DX is that with the 80486SX installed, it costs less, runs at slower speeds and has no internal coprocessor. This option allows a user to save money for applications that do not require intensive numeric calculations. Intel claims that "(depending upon the application) . . . the 25 MHz Intel486SX provides up to 70% more performance than the 33 MHz Intel386DX microprocessor."

The MCM-486DX board includes the 80486DX CPU with 1MB, 2MB, 4MB or 8MB of parity RAM, BIOS in EPROM, internal coprocessor, two RS-232/485 serial ports, 15 channel interrupt controller, DMA controller, Centronics parallel I/O port, SBX connector, real time clock, keyboard controller, watchdog timer, speaker and 8/16-bit STD Bus interface. The MCM-486DX requires only a single +5 volt supply.

The MCM-486 can work without DOS and BIOS software, or video, a keyboard or rotational memory for applications requiring a standalone single board computer.

FUNCTIONAL CAPABILITY

Processor - The MCM-486 board uses either the 80486DX or 80486SX CPU. It offers a 32-bit programming architecture compatible with the software base of the 80386 microprocessor. The integer unit uses RISC design techniques to provide 1 clock execution for core instructions. The 486 CPU provides backward compatibility to the large base of installed base of 8086/88, 80286 and 80386 software. Moreover, the MCM-486DX CPU brings the new generation of high-performance 32-bit software to the STD Bus. All

applications software and operating systems developed for 80386 microprocessor based systems run unmodified on similarly configured 80486 microprocessor based systems.

The MCM-486DX is available in a 25, 33 or 50 MHz configuration. The lower cost MCM-486SX is available with a system clock of 20 or 25 MHz.

Coprocessor Support - The MCM-486DX card has a on-chip floating point unit (FPU) which implements the full IEEE 754 floating-point standard and is binary compatible with the 80387 Math Coprocessor. By building in the math coprocessor, using the wider internal data buses, sharing on-chip caching, and eliminating I/O cycles for passing data between the processor and an external device, the performance is more than double as compared to a separate coprocessor.

The MCM-486SX board does not have the internal FPU. To upgrade the board, the 80486SX CPU chip must be replaced with a 80486DX chip. Contact the factory for the details.

MOSEL Chip Set - The MCM-486DX uses the MS400/401 from MOSEL to provide the core logic for high performance PC-AT hardware compatibility. The MS400, optimized specifically for 80486 CPU's, integrates the DRAM controller, DMA controllers, interrupt controllers, memory mapper, timer and all other logic basic to an AT system. The MS401 supports 32 and 64-bit data paths to DRAM. This offers higher integration and better performance in non-cache modes.

The MS400 supports shadowing of BIOS and Video ROM so that system performance will not be degraded by the slow access speed of EPROM. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution.

Memory - The MCM-486 has 4 memory sources onboard: on-chip 8K cache, parity checked DRAM, battery backed static RAM and BIOS EPROM.

The 8KB code and data cache on the 80486 allow one clock per instruction execution rate at 50 MHz to be sustained even with slower external DRAMs for mass storage.

The MCM-486 is configured with up to 8MB of onboard parity checked DRAM installed in two banks of 4MB each. The MS401 32/64-bit data path chip

uses interleaving automatically with both banks to create an effective 64-bit wide memory bus for the 40 8 MB configuration. The 64-bit data path permits one clock burst reads and memory post write operations to nearly double the memory accesses compared to using 32-bit data paths which offers lower cost and higher performance in non-cache modes.

System configuration information and the register values are stored in the 50 bytes of battery powered CMOS static RAM inside the DS1287. The values from the CMOS memory or the default ones from the BIOS EPROM will be loaded into the configuration registers when the system is initialized.

The MCM-486DX will work with either 8- or 16-bit external memory cards such as the MCM-UMC4 or solid state disks such as the MCM-SSD. The MCM-486DX automatically determines the transfer status and will access it as either 8- or 16-bits.

Serial I/O - A 16C452 serves as the serial communication controller mapped as a standard COM1 and COM2 port. It has two independent double buffered serial asynchronous channels that are 82C50A hardware compatible. The unit contains on-chip software programmable baud rate generators selectable through 56K bits per second. Each has independent control of transmit, receive, line status and data set interrupts. Individual modem handshake control signals are available for each line.

COM1 and COM2 Serial Channels

Pin	FLOW	Signal
1	IN	Data Carrier Detect (DCD)
2	IN	Receive Data (RxD)
3	OUT	Transmit Data (TxD)
4	OUT	Data Terminal Ready (DTR)
5	--	Signal Ground (GND)
6	IN	Data Set Ready (DSR)
7	OUT	Request To Send (RTS)
8	IN	Clear To Send (CTS)
9	IN	Ring Indicator (RI)

Each channel will support 5, 6, 7, or 8 bit characters with even, odd or no parity generation/checking. It will handle 1, 1 ½ or 2 stop bits.

Both serial channels support RS-232 and 2 wire RS-485 electrical interface levels. RS-422 is configurable for COM 2 only by strapping both the RS-485 interface chips for COM2 and leaving COM1 configured as RS-232 only. Only +5 volts is required by the MCM-486 since the +12 volts are generated by the RS-232 interface chip. Both serial channels are configured as a DTE and wired to an individual 10-pin right angle connector that permits easy connections to

a standard 9-pin male D-sub connector with the WinSystems' CBL-123-1.

Keyboard Controller - An 8242 keyboard controller is installed to provide a serial interface to a PC-AT type keyboard. Also the keyboard can be locked out by grounding pin 9 to prevent unauthorized access to the system.

The keyboard controller is buffered and wired to 10 pin connector. WinSystems offers the CBL-124-1 which is an adapter for the 10-pin ribbon to 5-pin DIN keyboard cable. The pin out is as follows:

Keyboard Interface

Pin	Signal
1 - 4	Ground
5 - 6	+5 volts
7	Keyboard Clock
8	+5 volts
9	Keyboard Lockout
10	Keyboard Data

Parallel I/O - The 16C452 also provides a direct 26-pin Centronics parallel I/O interface from the board. It is fully bidirectional with the associated handshake lines. The standard default I/O Map is LPT1.

The printer signal lines are wired to a 26-pin right angle connector. The optional WinSystems' CBL-101-3 provides a 3 foot long adapter cable designed to convert a 26-pin ribbon cable to a 25-pin male "D" type connector with strain relief.

P2 Pin out - Printer Channel

Pin	FLOW	Signal
1	IN	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper End
13	IN	Select
14	IN	Auto Error
15	I/O	Error
16	IN	Init. Printer
17	IN	Select Input
18-25	--	Ground

Counter/Timer - There are three independent software programmable 16-bit counter/timers available through a 82C54 type device on the MS400.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Real Time Clock - A battery backed Dallas Semiconductor DS1287 type clock calendar is onboard. It is totally compatible with the MC146818A with over 10 years of operation in absence of power. It counts seconds, minutes, hours, days, months, and year with leap year compensation. It also contains 50 bytes of non-volatile static CMOS RAM for setup information.

Interrupts - The MCM-486 will accept 4 interrupt signals from the STD Bus backplane (NMIRQ*, INTRQ*, INTRQ1* and INTRQ2*) and 4 additional interrupts from the front plane connector. Two onboard 82C59A type Programmable Interrupt Controllers (PICs) provide 15 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real-time systems. Since the system is PC-AT compatible, the cascade address scheme is not supported over the STD Bus backplane during interrupt acknowledge cycles.

Hardware Interrupt Channels

NMI	Parity
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	INT 8-15 expansion
IRQ3	COM2
IRQ4	COM1
IRQ5	Fixed Disk/STD INTRQ*
IRQ6	Floppy Disk
IRQ7	Parallel Printer
IRQ8	Real Time Clock
IRQ9	Video
IRQ10	Interrupt Header J3/STD INTRQ1*
IRQ11	Interrupt Header
IRQ12	Interrupt Header
IRQ13	Coprocessor
IRQ14	Hard Disk
IRQ15	Interrupt Header

In addition to these interrupts, 2 additional independent interrupt lines are provided across the front plane for the disk and video interrupts. These are mapped into the correct, dedicated interrupt input lines to maintain PC-AT compatibility.

SBX Multimodule Connector - A single 8-bit SBX multimodule connector is provided to accommodate

single-wide, 36-pin (8-bit) I/O expansion modules. This provides an alternative method for I/O expansion to the STD Bus offering the possibility of using just the MCM-486DX as a single board solution. SBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, solid state disk, networking, graphics controllers, and other special purpose peripheral functions.

The MCM-486 decodes I/O addresses and generates the chip selects for the SBX boards. DMA and interrupt operations are supported.

I/O - The MCM-486 conforms to the PC-AT I/O map and STD Bus standard 10-bit addressing. It will support older STD Bus I/O cards that decode only 8 address bits, 8 bits with IOEXP*, and the newer 10-bit I/O cards.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the CPU's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

Dynamic Bus Sizing - The MCM-486 automatically supports 8-, 16-, or 32-bit transfers between the CPU/cache and 8- or 16-bit memory and I/O peripherals which exist on the STD Bus. Misaligned transfers are supported by the MS400. Byte swapping will be performed if the transfer requests data from a peripheral device which is not physically connected to the requested bytes.

STD-AT Bus - The MCM-486 originates a 16-pin interrupt and DMA Controller Bus at the top of the card. This is required to provide 100% PC-AT hardware compatibility for video, disk and network controller cards while it frees the backplane interrupts for additional sources. However for small systems with video or hard disks, the interrupts can be routed over the backplane STD Bus interrupt lines.

STD Bus Interface - The MCM-486 does not require termination to work properly in STD Bus card cages. WinSystems has correctly designed our backplanes to minimize noise and crosstalk while maintaining good power distribution, massive ground planes and a good characteristic impedance for the signal lines. The common STD Bus recommended termination simply adds unwanted capacitance and

loads the bus drivers which results in slower data transitions and skewed signals.

CMOS STD Bus - The 80486 CPU has a narrower temperature range and higher power consumption than less powerful processors used for most industrial applications. These facts eliminate the advantage of using the CMOS STD Bus. WinSystems will install the CMOS interface bus transceivers on the MCM-486DX and MCM-486SX boards. Contact the factory for specific part numbers and pricing.

Speaker - A speaker interface and speaker are included on the board. The speaker is mounted between the two PC boards that comprise the MCM-486 board set.

Printed Circuit Board - The MCM-486 is a 2 board set of cards tightly coupled through a local bus to form a complete single board computer in the standard 4.5 x 6.5 inch STD Bus form factor. This packaging concept offers superior reliability and rugged mounting while maintaining the small STD Bus size. The onboard mass storage can function at very high CPU clock speeds through the local bus while automatically switching to a slower speed for STD Bus data transfers.

SOFTWARE SUPPORT

The MCM-486DX is designed to support both full PC-AT DOS compatible and embedded systems applications. The key to configuration is in the firmware and software.

DOS Systems Support

STD-AT - The MCM-486 is offered with a combination of STD Bus boards, enclosure and power supply configured together to make a base PC-AT compatible system called the STD-AT. The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "software bus", for hosting operating systems utilities, real time executives, development tools, networking, and application specific programs. The basic philosophy of the STD-AT is to offer full DOS compatibility with high performance processors.

BIOS - The Basic Input/Output System (BIOS) is written by AMI to provide maximum performance and full IBM-AT compatibility. It is designed for high speed 80486DX systems operating up to 33MHz. It supports both 720KB and 1.44MB 3.5 inch and 360KB and 1.2MB 5.25 inch floppy disk drives, 101, 102, and 84-key AT-compatible keyboards, the on-chip math coprocessor, offers enhanced protected mode to real

mode switching for faster VDISK, INT 15H multitasking extensions for extended memory and block moves, IBM defined extensions to BIOS calls, and is fully compatible with Novell NetWare. The BIOS also provides complete power-on self test and boot diagnostics.

DOS - The MCM-486 is designed to be architecturally compatible with the PC-AT. As such it will run either MS-DOS or IBM PC-DOS and will support calls either through the BIOS or directly to the hardware. The card will also support other operating systems such as UNIX or XENIX and real-time executives that require a "PC-AT" hardware environment.

QNX - QNX is a powerful, real-time, networked, distributed processing operating system. It permits up to 57 users per computer and up to 250 concurrent tasks. Its preemptive, priority driven scheduling, coupled with a fast task-switch time, allow QNX to provide the response needed for process control and other real-time applications.

The MCM-486 provides a powerful platform to build low cost, high performance, industrial real-time solutions.

Embedded Systems Support

C-THRU-ROM-486 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the MCM-486DX/SX. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code.

ROM-DOS - ROM-DOS is a MS-DOS 3.3 compatible ROM-based operating system for embedded MCM-486 applications. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied. ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications.

4

SPECIFICATIONS

Electrical
Bus Interface: STD Bus
CPU Clock: 20 or 25 MHz; MCM-486SX
CPU Clock: 25, 33 or 50 MHz; MCM-486DX
Serial Interface: 2 channels RS-232 and 2 wire RS-485
Parallel Interface: Centronics line interface
Interrupts: TTL input with 10K ohm pull-up resistors
Vcc = +5V ±5% at TBD mA typ.

Memory
Addressing: 16 Megabytes (direct)
Capacity: Supports up to 128K EPROM (1 socket)
          1MB, 2MB, 4MB or 8MB DRAM (supplied)

Mechanical
Dimensions: 4.5″ x 6.5″, requires 2 card slots.
Jumpers: 0.025" square posts

Connectors
Serial I/O: 10-pin 0.100″ grid
Parallel I/O: 26-pin 0.100″ grid
Interrupts: 10-pin 0.100″ grid
Keyboard: 10-pin 0.100″ grid
STD-AT Bus: 16-pin 0.100" grid

Environmental
Operating Temperature: 0° to +45°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-486DX-25-1M	Single board 25MHz 80486DX computer with 1MB of DRAM
MCM-486DX-25-2M	Single board 25MHz 80486DX computer with 2MB of DRAM
MCM-486DX-25-4M	Single board 25MHz 80486DX computer with 4MB of DRAM
MCM-486DX-25-8M	Single board 25MHz 80486DX computer with 8MB of DRAM
MCM-486DX-33-1M	Single board 33MHz 80486DX computer with 1MB of DRAM
MCM-486DX-33-2M	Single board 33MHz 80486DX computer with 2MB of DRAM
MCM-486DX-33-4M	Single board 33MHz 80486DX computer with 4MB of DRAM
MCM-486DX-33-8M	Single board 33MHz 80486DX computer with 8MB of DRAM
MCM-486DX-50-1M	Single board 50MHz 80486DX computer with 1MB of DRAM
MCM-486DX-50-2M	Single board 50MHz 80486DX computer with 2MB of DRAM
MCM-486DX-50-4M	Single board 50MHz 80486DX computer with 4MB of DRAM
MCM-486DX-50-8M	Single board 50MHz 80486DX computer with 8MB of DRAM
MCM-486SX-20-1M	Single board 20MHz 80486SX computer with 1MB of DRAM
MCM-486SX-20-2M	Single board 20MHz 80486SX computer with 2MB of DRAM
MCM-486SX-20-4M	Single board 20MHz 80486SX computer with 4MB of DRAM
MCM-486SX-20-8M	Single board 20MHz 80486SX computer with 8MB of DRAM
MCM-486SX-25-1M	Single board 25MHz 80486SX computer with 1MB of DRAM
MCM-486SX-25-2M	Single board 25MHz 80486SX computer with 2MB of DRAM
MCM-486SX-25-4M	Single board 25 MHz 80486SX computer with 4MB of DRAM
MCM-486SX-25-8M	Single board 25 MHz 80486SX computer with 8MB of DRAM

WinSystems, Inc.

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FEATURES

- 80386SX CPU with 16 or 20 MHz clock
- 100% object code compatibility with the 386, 286, and 8086 CPUs
- Full IBM PC-AT compatibility
- Uses the Chips and Technologies NEATsx
- Supports MS/DOS, OS/2, UNIX, Windows/386 and other popular PC-AT operating systems, real time executives, and application software
- 512K, 1MB, 2MB or 4MB of parity DRAM
- 128KBytes of EPROM storage capacity
- 16 Megabyte direct addressing
- 80387SX numeric coprocessor socket
- Industry standard Phoenix PC-AT BIOS PLUS
- Set Up program stored in BIOS ROM
- Shadow BIOS for improved performance
- Asynchronous I/O bus controller assures compatibility with slower I/O cards
- 2 Serial RS-232 ports: COM1 and COM2
- Centronics compatible parallel I/O port
- Keyboard controller
- Battery backed calendar clock
- On board speaker
- Three 16-bit timer/counters
- 4 channel DMA controller
- 15 channel interrupt controller
- Full 8-bit or 16-bit STD Bus interface
- Watchdog timer
- Supports ROM-DOS embedded operating system

- Low power
- +5 volt only operation
- Precision power fail reset circuit
- 4.5" X 6.5" IEEE 961 STD Bus form factor
- Wide temperature range: 0° to 65°C

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*SHADING INDICATES SOCKET ONLY

The LPM-386SX is a high performance CMOS STD Bus single board computer that can operate as a PC-AT DOS compatible or a standalone board for embedded systems applications. The LPM-386SX is designed to meet demanding requirements in applications such as industrial, factory floor, automatic test, instrumentation, robotics, machine control, aerospace, and other difficult environments.

The LPM-386SX board includes the Intel 80386SX CPU with either 512KB, 1MB, 2MB, or 4 MB of parity DRAM, two EPROM sockets, an 80387SX coprocessor socket, two RS-232 serial ports, interrupt controller, DMA, Centronics parallel I/O port, real time clock, keyboard controller, watchdog timer, speaker and 8/16-bit STD Bus interface. The LPM-386SX requires only a single +5 volt supply.

The LPM-386SX is a 2 board set of cards tightly coupled through a local bus to form a complete single board computer in the standard 4.5 x 6.5 inch STD Bus form factor. The onboard mass storage can function at very high CPU clock speeds while the STD Bus automatically operates for existing slower memory and I/O cards.

Its DOS compatibility and performance is obtained through the use of the 80386SX CPU, NEATsx CHIPSet, and industry standard Phoenix BIOS. This yields both 100% hardware and software PC-AT compatibility.

The LPM-386SX can work without DOS and BIOS software, video, keyboard, or rotational memory for applications requiring a standalone single board computer. WinSystems offers ROM-DOS, an optional embedded operating system, and C-THRU-ROM, a full featured C source level debugger. The LPM-386SX's wealth of hardware functions also makes it an ideal candidate for disguised and embedded applications.

FUNCTIONAL CAPABILITY

Processor - The LPM-386SX incorporates the powerful 32-bit 80386SX high performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. It offers a 32-bit programming architecture compatible with the software base of the 80386 microprocessor. The LPM-386SX features a 16-bit external STD Bus data bus and a 24-bit address bus. Thus it provides the performance benefits of a 32-bit programming architecture with the cost savings associated with 16-bit hardware systems. The 80386SX includes memory management capabilities of 16 megabytes of physical and 64 Terabytes of virtual address space. The 386SX provides backward compatibility to the large base of installed base of

8086 and 80286 software. Moreover, the 386SX CPU brings the new generation of high-performance 32-bit software to the STD Bus. All applications software and operating systems developed for 386 microprocessor based systems run unmodified on similarly configured 386SX microprocessor based systems.

The 80386SX provides advanced functions such as hardware supported multitasking and virtual memory support. On-chip memory management unit and a hardware enforced memory protection mechanism are also provided. Instruction pipelining, high bus bandwidth, and a very high performance ALU ensure short average execution times.

The 386SX CPU has 2 modes of operation: Real Address Mode (Real Mode), and Protected Virtual Address Mode (Protected Mode). In Real Mode the 386SX CPU operates as a very fast 8086, but with 32-bit extensions if desired. Real Mode is required primarily to set up the processor for Protected Mode operation and for PC and DOS compatibility.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 characteristics, thus allowing 8086 software (an application program or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 386SX CPU's operating system by use of paging.

The processor is fully buffered to the STD Bus and operates at 16 or 20 MHz. It can perform either 8 or 16-bit memory and I/O transfers to the STD Bus and is compatible with existing peripheral cards.

80387 Coprocessor - The LPM-386SX card has a socket to accept an 80387SX coprocessor. The 80387SX fully implements the IEEE 754 floating point standard, with a high-precision 80-bit architecture and full support for single, double, and extended precision operations. It is object code compatible with the 8087, 80287 and 80387 allowing previous software developed for 80X86/88 numerics applications to be migrated to the LPM-386SX. Substantial performance improvement over numeric floating point software can be expected in any application using this coprocessor. Performance is 3 to 5 times faster than an 286/287 in numerics applications.

The 80387 Numeric Coprocessor directly extends the 386SX CPU instruction set to include trigonometric, logarithmic, exponential, and arithmetic instructions for all data types. Data types include 32-bit single real, 64-bit double real, 80-bit extended real, 16-bit word

integer, 32-bit short integer, 64-bit long integer, and 18-bit BCD integer.

NEAT Chip Set - The LPM-386SX uses the CS8281 NEATsx (New Enhanced AT) CHIPSet from Chips and Technologies to provide the core logic for high performance PC-AT hardware compatibility. It is the latest generation of fully AT compatible Chips which operates at 16 or 20 MHz.

NEATsx maintains full compatibility with the PC-AT. Additionally it supports the Expanded Memory Specification 3.2 (EMS), memory extended memory, and advanced memory paging schemes for on-board memory. NEATsx is all CMOS for very low power consumption.

Due to shadowing of BIOS and Video ROM, system performance will not be degraded by the slow access speed of EPROM.

Unlike the PC-AT, the clocks used for the CPU and CMOS STD Bus may be asynchronous or synchronous. This design allows for a greater flexibility in the system and yields higher performance and yet, maintains compatibility. In either mode, the CPU can operate at high clock speeds (16 MHz or 20 MHz); however, the clock source for the STD Bus (ATCLK) is different. This means that the LPM-386SX can work with CMOS STD Bus cards or backplanes that can only operate at 5 or 8 MHz while the CPU runs at full speed. The clock source is configurable in the NEATsx set up registers.

The CS8281 NEATsx CHIPSet provides a complete PC-AT compatible system with just 5 VLSI devices: the 82C811 CPU/Bus controller, the 82C812 Page/ Interleave and EMS Memory Controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEATsx CHIPSet supports the local CPU bus, a 16-bit onboard system memory bus, and the 8/16 bit CMOS STD Bus. The 82C811 provides synchronization and control signals of all busses. The 82C811 also provides an independent CMOS STD Bus clock and allows for dynamic selection between the processor clock and the user selectable CMOS STD Bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards on the CMOS STD Bus.

The 82C812 Page/Interleave and EMS Memory controller provides an interleaved memory subsystem designed with page mode operation. It supports up to 4 MB of on-board DRAM. The processor can operate at 16 MHz with 0.7 wait state memory accesses, using 100 nS DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 IPC incorporates two 8237 DMA controllers, two 82C59A interrupt controllers, one 82C54 Timer/Counter, one MC146818 Real Time Clock (RTC), 74LS612 memory mapper and other SSI interface logic chips. While offering complete compatibility to the PC-AT architecture, the chip offers enhanced features and improved speed performance. These include 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 82C59, and 82C54. A variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip.

Memory - The LPM-386SX has 3 memory sources onboard: EPROM, DRAM, and battery-backed static RAM. Two memory sockets are provided to support the BIOS and any applications program. Either 32K or 64K byte EPROMs are supported in each socket. Two banks of dynamic RAM offer population options from 512Kbytes to 4Mbytes accessed via 16-bit data transfers. Parity is included on each byte. System configuration information and the register values for the NEATsx chip set is stored in the battery powered CMOS static RAM inside the 82C206. The values from the CMOS memory or the default ones from the BIOS EPROM will be loaded into the configuration registers when the system is turned on.

The LPM-386SX will work with either 8 or 16-bit external memory cards such as the LPM-UMC3 or LPM-UMC4 or general memory storage or for use as RAM/ROM Disks. The LPM-386SX automatically tests the status of the card and will access it in either 8 or 16-bit transfers. The card will directly address 16 Megabytes of memory which is required for large applications programs or memory intensive operating systems such as OS/2.

DRAM Refresh - The NEATsx CHIPSet generates the REFRESH* signal and refresh addresses up to 512 rows. The interval can be programmed to accommodate the requirements of various types of memories.

The REFRESH* signal is buffered and can be jumpered onto the CMOS STD Bus.

A page mode feature allows the use of slower DRAM while maintaining fast memory accesses. In the page mode, the access time becomes the column address access time (CAS), which is typically less than half of row address access time. During the page mode operation, the row address (RAS) is latched into the DRAM and is maintained logic low through all successive memory cycles if a page hit (row address of the current memory access is within the same row address page) occurs. This way of operation eliminates the time normally needed to strobe a new row address. The DRAM access time is then determined by the CAS access time which is typically equal or less than half of the RAS access time. Using a page mode scheme, a system can use slower inexpensive DRAMs and still maintain a high performance memory system.

WAIT State Generation - The NEATsx CHIPSet generates Wait States for up to 3 clock cycles during a bus cycle for either I/O or Memory transfers to compensate for the access speeds of slower memory or I/O devices.

Serial I/O - A VLSI technology VL16C452 serves as the serial communication controller mapped as a standard COM1 and COM2 port. It has two independent double buffered serial asynchronous channels that are 82C50A hardware compatible. The unit contains on-chip software programmable baud rate generators selectable through 56K bits per second. Each has independent control of transmit, receive, line status and data set interrupts. Individual modem handshake control signals are available for each line.

Each channel will support 5, 6, 7 or 8 bit characters with even, odd or no parity generation/checking. It will handle 1, 1½ or 2 stop bits.

The standard I/O map is for COM1 and COM2 (3F8-3FF hex and 2F8-2FF hex respectively). Three alternative maps are available through a jumper header.

P3 and P4 Pinout
COM1 and COM2 Serial Channel

Pin	FLOW	Signal
1	IN	Data Carrier Detect (DCD)
2	IN	Receive Data (RxD)
3	OUT	Transmit Data (TxD)
4	OUT	Data Terminal Ready (DTR)
5	--	Signal Ground (GND)
6	IN	Data Set Ready (DSR)
7	OUT	Request To Send (RTS)
8	IN	Clear To Send (CTS)
9	IN	Ring Indicator (RI)

Both channels support RS-232 electrical interface levels. Only +5 volts is required for the system since a Maxim MAX235 chip is used which generates the plus and minus voltages required.

Both serial channels are configured as a DTE and wired to an individual 10-pin right angle connector that permits easy connections to a standard 9-pin male D-sub connector with the WinSystems CBL-123-1.

Keyboard Controller - An 8242 keyboard controller is installed to provide a serial interface to a PC-AT type keyboard. Also the keyboard can be locked out by grounding pin 9 to prevent unauthorized access to the system.

The keyboard controller is buffered and wired to a 10-pin connector, J2. WinSystems offers the CBL-124-1 which is an adapter for the 10-pin ribbon to 5-pin DIN keyboard cable. The pinout of the 10-pin cable, J2, is as follows:

J2- Keyboard Interface

Pin	Signal
1 - 4	Ground
5 - 6	+5 volts
7	Keyboard Clock
8	+5 volts
9	Keyboard Lockout
10	Keyboard Data

Parallel I/O - The VL16C452 also provides a direct 26-pin Centronics parallel I/O interface from the LPM-386SX. It is fully bidirectional with the associated handshake lines. The standard default I/O Map is LPT1 (378-37F hex). J8 provides jumper selectable options for other locations such as LPT2.

P2 Pinout - Printer Channel

Pin	FLOW	Signal
1	OUT	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper End
13	IN	Select
14	OUT	Auto Feed
15	IN	Error
16	OUT	Init. Printer
17	OUT	Select Input
18-25	- -	Ground

The printer signal lines are wired to P2, a 26-pin right angle connector. The optional WinSystems' CBL-101-3 provides a 3-foot long adapter cable designed to convert a 26-pin ribbon cable to a 25-pin male "D" type connector with strain relief.

Counter/Timer - There are three independent software programmable 16-bit counter/timers available through a 82C54 type device. Counter 0 is dedicated to a real time clock tick output to IRQ0 of 55 mS (18.2 ticks per second). Counter 1 is available for DRAM refresh. Since the NEATsx CHIPSet generates DRAM refresh independently, then this timer could be freed for other timing purposes. Counter 2 is dedicated to the speaker oscillator. If required, it could be tied to the interrupt controller to provided another timer input.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Real Time Clock - A battery backed onboard MC146818 type clock calendar is provided by the NEATsx CHIPSet. It can be programmed for binary or BCD. It counts seconds, minutes, hours, days, months, and year. It has automatic end of month recognition and leap year compensation.

Interrupts - The LPM-386SX will accept 3 interrupt signals from the CMOS STD Bus backplane (INTRQ*,

INTRQ1* and INTRQ2*) and 4 additional interrupts from the front plane connector. Two onboard 82C59A type Programmable Interrupt Controllers (PICs) provide 15 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Since the system is PC-AT compatible, the cascade address scheme is not supported over the CMOS STD Bus backplane during interrupt acknowledge cycles.

In addition to these interrupts, 2 additional independent interrupt lines are provided across the front plane for the disk and video interrupts. These are mapped into the correct, dedicated interrupt input lines to maintain PC-AT compatibility.

Dynamic Bus Sizing - The LPM-386SX has two new signals, MEM16 and I/O16, defined which automatically looks at the STD Bus memory and I/O board status to determine whether a 8 or 16-bit transfer should occur. If these signals are active low, then a 16-bit transfer will occur. If the peripheral board does not respond, then it is assumed a 8-bit transfer is

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Hardware Interrupt Channels

Interrupt	Description
NMI	Parity
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	INT 8-15 expansion
IRQ3	COM2
IRQ4	COM1
IRQ5	Fixed Disk/STD INTRQ*
IRQ6	Floppy Disk
IRQ7	Parallel Printer
IRQ8	Real Time Clock
IRQ9	Video
IRQ10	Interrupt Header J3/STD INTRQ1*
IRQ11	Interrupt Header J3
IRQ12	Interrupt Header J3
IRQ13	80387 Co-processor
IRQ14	Hard Disk
IRQ15	Interrupt Header J3

PC-AT I/O Map

Hex Range	Usage
000-00F	8237A-5DMA Controller 1
020-021	8259A Interrupt Controller 1
040-043	8253/8254 Timer
060-063	8255A-5 PPI (XT)
060-064	8042 Kbd. Controller (AT)
070-071	CMOS RAM & NMI Mask Reg(AT)
080-083	DMA Page Registers (XT)
080-09F	DMA Page Registers (XT)
0A0-0BF	8259A Interrupt Controller 2
0A0-0AF	NMI Mask Register (XT)
0C0-0CF	Reserved
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
0C0-0DF	8237 #2 (AT) (See Note)
0E0-0EF	Reserved
200-20F	Game I/O Adapter
210-217	Expansion Unit (XT only)
220-24F	Reserved
278-27F	Parallel Printer 2
2F0-2F7	Reserved
2F8-2FF	Serial Port 2
300-31F	Prototype Card
320-32F	Fixed Disk
360-36F	Reserved
378-37F	Parallel Printer 1
380-38F	SDLC, Bisynchronous 1
3A0-3AF	Bisynchronous 2
3B0-3BF	Monochrome Display/Printer (Printer 3BC-3BF)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Adaptor
3E0-3EF	Reserved
3F0-3F7	Floppy Disk
3F8-3FF	Serial Port 1

required making the system upward compatible with previously designed CMOS STD Bus cards.

I/O - The LPM-386SX conforms to the PC-AT I/O map and CMOS STD Bus standard 10-bit addressing. It will support older CMOS STD Bus I/O cards that decode only 8 address bits, 8 bits with IOEXP*, and the newer 10-bit I/O cards. The LPM-386SX provides this flexibility by decoding I/O addresses 100 - 1FF and driving IOEXP* active low via a jumper option onboard. To understand both the LPM-386SX I/O map and a typical PC-AT I/O port assignment, an I/O map is listed below showing the I/O addresses, usage and where the LPM-386SX is mapped.

STD-AT Bus - The LPM-386SX originates a 16-pin interrupt and DMA controller Bus at the top of the card. This is required to provide 100% PC-AT hardware compatibility for video, disk and network controller cards while it frees the backplane interrupts for additional sources. However for small systems with video or hard disks, the interrupts can be routed over the backplane CMOS STD Bus interrupt lines.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the CPU's write line, preventing invalid data from being written to battery backed RAM's or EEPROMs during power fluctuations.

Battery - A 750 mA hour battery is provided to supply current for both the real time clock and CMOS configuration RAM.

Speaker - A speaker interface and speaker are included on the board. The speaker is mounted between the two PC boards that comprise the LPM-386SX board.

STD Bus Interface - The LPM-386SX does not require termination to work properly in STD Bus card cages. WinSystems' has correctly designed our backplanes to minimize noise and crosstalk while maintaining good power distribution, massive ground planes and a good characteristic impedance for the signal lines. The common CMOS STD Bus recommended termination simply adds unwanted capacitance and loads the bus drivers which results in slower data transitions and skewed signals.

Printed Circuit Board - The LPM-386SX is a 2 board "sandwich" that comprises the system. The first board contains the 80386SX CPU, 80387SX coprocessor socket, keyboard controller, reset circuit, and STD Bus interface logic. It is connected through two 50-pin, gas tight, pin-and-socket connectors to a second board. This board contains the 2 EPROM sockets, DRAMs, 2 serial channels, Centronics I/O port, and real time clock. The speaker and battery are mounted in between the 2 boards. This packaging concept offers superior reliability and rugged mounting while maintaining the STD Bus 4.5" X 6.5" format.

SOFTWARE SUPPORT

The LPM-386SX is designed to support both full PC-AT DOS compatible and embedded systems applications. The key to configuration is in the firmware and software.

DOS Systems Support

STD-AT - The LPM-386SX is offered with a combination of CMOS STD Bus boards, card cage and power supply configured together to make a base PC-AT compatible system called the STD-AT. The STD-AT blends the industry proven CMOS STD Bus hardware with MS/PC-DOS, the defacto "software bus", for hosting operating systems utilities, real time executives, development tools, networking, and application specific programs. The basic philosophy of the STD-AT is to offer full DOS compatibility with high performance processors.

BIOS - The Basic Input/Output System (BIOS) is written by Phoenix Technologies to provide maximum performance and full IBM-AT compatibility. It is designed for high speed 80386SX systems operating a 16 MHz with no Wait States. It supports both 720KB and 1.44MB 3.5 inch and 360KB and 1.2MB 5.25 inch floppy disk drives, 101, 102, and 84-key AT-compatible keyboards, the 80387SX math coprocessor, offers enhanced protected mode to real mode switching for faster VDISK, INT 15H multitasking extensions for extended memory and block moves, IBM defined extensions to BIOS calls, and is fully compatible with Novell NetWare. The BIOS also provides complete power-on self test and boot diagnostics.

DOS - The LPM-386SX is designed to be architecturally compatible with the PC-AT. As such it will run either MS-DOS or IBM PC-DOS and will support calls either through the BIOS or directly to the hardware. The card will also support other operating systems such as UNIX or XENIX and real time executives that require a "PC-AT" hardware environment.

Embedded Systems Support

C-THRU-ROM-386SX - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated

debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the LPM-386SX. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM consists of a source level debugging user interface with target communication facility that resides on the LPM-386SX. The target system kernel includes an execution control program and host communication facility. During a debug session, the symbolic information is maintained on a PC-AT host and the program code is downloaded to the LPM-386SX for execution over a 9600 bps serial port. The application program is debugged directly on the LPM-386SX.

CTR Debugger - The C-THRU-ROM windowing debugger provides access into the LPM-386SX and is completely compatible with Microsoft C version 5.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote CodeView. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

The Debugger is a source level debugger. This means that the Debugger, in addition to understanding the 80X86/88 machine code, understands such symbols as function names, global variables, and publics, locals, and register variables. This also means that the debugger knows about line numbers, and even modules, making it possible to set break points, unassemble, and go directly to the code at any line.

With the Debugger a listing of the program appears on the screen. One can single-step through the program lines, examine variables, execute parts of the program, and watch both program listing and the output it generates. The lines of code are displayed as they are executed, giving one the opportunity to stop

execution, examine and change variables and registers, trace a single line or instruction, or even restart the program from scratch.

ROM-DOS - ROM-DOS is a MS-DOS 3.2 compatible ROM based operating system for embedded LPM-386SX applications. ROM-DOS provides 3 major functions: hardware initialization, file support and standard drivers. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied.

ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that greatly simplifies data storage and retrieval. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

A standard ROM-DOS setup has the code for ROM-DOS and Mini-BIOS in the top 64K bytes of ROM, and the user application program (.EXE file) and associated disk files in ROM on a ROM-disk. The ROM's containing the actual ROM-disk files are placed in any convenient location above the system RAM. The ROMDISK is configured as the "A" drive so ROM-DOS will search it for the initial program upon booting.

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SPECIFICATIONS

Electrical

Bus Interface: 8/16-bit STD Bus
CPU Clock: 16 or 20 MHz
STD Bus System Clock: 8 MHz
Serial Interface: 2 channels RS-232
Parallel Interface: Centronics line interface
Interrupts: TTL input with 10K ohm pull-up resistors
Vcc = +5V $\pm$ 5% at 1500 mA typ. (with no 80387SX
    installed)

Memory

Addressing: 16 Megabytes
Capacity: Supports up to 128K EPROMs (2 sockets)
    and 512KB, 1MB, 2MB or 4MB supplied

Mechanical

Dimensions: Meets all STD Bus mechanical
    specifications: 4.5 x 5 x 6.5 inches, requires
    2 card slots.

Jumpers: 0.025" square posts

Connectors

Serial I/O: 10-pin 0.100" grid
Parallel I/O: 26-pin 0.100" grid
Interrupts: 10-pin 0.100" grid
Keyboard: 10-pin 0.100" grid
STD-AT Bus: 16-pin 0.100" grid

Environmental

Operating Temperature: 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-386SX-16-512	Single board 16MHz computer with 512KB of DRAM
LPM-386SX-16-1M	Single board 16MHz 80386SX computer with 1MB of DRAM
LPM-386SX-16-2M	Single board 16MHz 80386SX computer with 2MB of DRAM
LPM-386SX-16-4M	Single board 16MHz 80386SX computer with 4MB of DRAM
LPM-386SX-20-512	Single board 20MHz 80386SX computer with 512KB of DRAM
LPM-386SX-20-1M	Single board 20MHz 80386SX computer with 1MB of DRAM
LPM-386SX-20-2M	Single board 20 MHz 80386SX computer with 2MB of DRAM
LPM-386SX-20-4M	Single board 20 MHz 80386SX computer with 4MB of DRAM

WinSystems, Inc.

FEATURES

- 80386SX CPU with 16 or 20 MHz clock
- 100% object code compatibility with the 386, 286, and 8086 CPUs
- Full IBM PC-AT compatibility
- Uses the Chips and Technologies NEATsx
- Supports MS/DOS, OS/2, UNIX, Windows/386 and other popular PC-AT operating systems, real time executives, and application software
- 512K, 1MB, 2MB or 4MB of parity DRAM
- 128K bytes of EPROM storage capacity
- 16 Megabyte direct addressing
- 80387SX numeric coprocessor socket
- Industry standard Phoenix PC-AT BIOS PLUS
- Set Up program stored in BIOS ROM
- Shadow BIOS for improved performance
- Asynchronous I/O bus controller assures compatibility with slower I/O cards
- 2 Serial RS-232 ports: COM1 and COM2
- Centronics compatible parallel I/O port
- Keyboard controller
- Battery backed calendar clock
- On board speaker
- Three 16-bit timer/counters
- 4 channel DMA controller
- 15 channel interrupt controller
- Full 8-bit or 16-bit STD Bus interface
- Watchdog timer
- Supports ROM-DOS embedded operating system

- Low power
- +5 volt only operation
- Precision power fail reset circuit
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- Wide temperature range: 0° to 65°C

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FUNCTIONAL CAPABILITY

Processor - The MCM-386SX incorporates the powerful 32-bit 80386SX high performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. It offers a 32-bit programming architecture compatible with the software base of the 80386 microprocessor. The MCM-386SX features a 16-bit external STD Bus data bus and a 24-bit address bus. Thus it provides the performance benefits of a 32-bit programming architecture with the cost savings associated with 16-bit hardware systems. The 80386SX includes memory management capabilities of 16 megabytes of physical and 64 Terabytes of virtual address space. The 386SX provides backward compatibility to the large base of installed base of

8086 and 80286 software. Moreover, the 386SX CPU brings the new generation of high-performance 32-bit software to the STD Bus. All applications software and operating systems developed for 386 microprocessor based systems run unmodified on similarly configured 386SX microprocessor based systems.

The 80386SX provides advanced functions such as hardware supported multitasking and virtual memory support. On-chip memory management unit and a hardware enforced memory protection mechanism are also provided. Instruction pipelining, high bus bandwidth, and a very high performance ALU ensure short average execution times.

The 386SX CPU has 2 modes of operation: Real Address Mode (Real Mode), and Protected Virtual Address Mode (Protected Mode). In Real Mode the 386SX CPU operates as a very fast 8086, but with 32-bit extensions if desired. Real Mode is required primarily to set up the processor for Protected Mode operation and for PC and DOS compatibility.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 characteristics, thus allowing 8086 software (an application program or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 386SX CPU's operating system by use of paging.

The processor is fully buffered to the STD Bus and operates at 16 or 20 MHz. It can perform either 8 or 16-bit memory and I/O transfers to the STD Bus and is compatible with existing peripheral cards.

80387 Coprocessor - The MCM-386SX card has a socket to accept an 80387SX coprocessor. The 80387SX fully implements the IEEE 754 floating point standard, with a high-precision 80-bit architecture and full support for single, double, and extended precision operations. It is object code compatible with the 8087, 80287 and 80387 allowing previous software developed for 80X86/88 numerics applications to be migrated to the MCM-386SX. Substantial performance improvement over numeric floating point software can be expected in any application using this coprocessor. Performance is 3 to 5 times faster than an 286/287 in numerics applications.

The 80387 Numeric Coprocessor directly extends the 386SX CPU instruction set to include trigonometric, logarithmic, exponential, and arithmetic instructions for all data types. Data types include 32-bit single real, 64-bit double real, 80-bit extended real, 16-bit word

integer, 32-bit short integer, 64-bit long integer, and 18-bit BCD integer.

NEAT Chip Set - The MCM-386SX uses the CS8281 NEATsx (New Enhanced AT) CHIPSet from Chips and Technologies to provide the core logic for high performance PC-AT hardware compatibility. It is the latest generation of fully AT compatible Chips which operates at 16 or 20 MHz.

NEATsx maintains full compatibility with the PC-AT. Additionally it supports the Expanded Memory Specification 3.2 (EMS), memory extended memory, and advanced memory paging schemes for on-board memory. NEATsx is all CMOS for very low power consumption.

Due to shadowing of BIOS and Video ROM, system performance will not be degraded by the slow access speed of EPROM.

Unlike the PC-AT, the clocks used for the CPU and STD Bus may be asynchronous or synchronous. This design allows for a greater flexibility in the system and yields higher performance and yet, maintains compatibility. In either mode, the CPU can operate at high clock speeds (16 MHz or 20 MHz); however, the clock source for the STD Bus (ATCLK) is different. This means that the MCM-386SX can work with STD Bus cards or backplanes that can only operate at 5 or 8 MHz while the CPU runs at full speed. The clock source is configurable in the NEATsx set up registers.

The CS8281 NEATsx CHIPSet provides a complete PC-AT compatible system with just 5 VLSI devices: the 82C811 CPU/Bus controller, the 82C812 Page/Interleave and EMS Memory Controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEATsx CHIPSet supports the local CPU bus, a 16-bit onboard system memory bus, and the 8/16 bit STD Bus. The 82C811 provides synchronization and control signals of all busses. The 82C811 also provides an independent STD Bus clock and allows for dynamic selection between the processor clock and the user selectable STD Bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards on the STD Bus.

The 82C812 Page/Interleave and EMS Memory controller provides an interleaved memory subsystem designed with page mode operation. It supports up to 4 MB of on-board DRAM. The processor can operate at 16 MHz with 0.7 wait state memory accesses, using 100 nS DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature

allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 IPC incorporates two 8237 DMA controllers, two 82C59A interrupt controllers, one 82C54 Timer/Counter, one MC146818 Real Time Clock (RTC), 74LS612 memory mapper and other SSI interface logic chips. While offering complete compatibility to the PC-AT architecture, the chip offers enhanced features and improved speed performance. These include 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 82C59, and 82C54. A variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip.

Memory - The MCM-386SX has 3 memory sources onboard: EPROM, DRAM, and battery-backed static RAM. Two memory sockets are provided to support the BIOS and any applications program. Either 32K or 64K byte EPROMs are supported in each socket. Two banks of dynamic RAM offer population options from 512Kbytes to 4Mbytes accessed via 16-bit data transfers. Parity is included on each byte. System configuration information and the register values for the NEATsx chip set is stored in the battery powered CMOS static RAM inside the 82C206. The values from the CMOS memory or the default ones from the BIOS EPROM will be loaded into the configuration registers when the system is turned on.

The MCM-386SX will work with either 8 or 16-bit external memory cards such as the MCM-UMC3 or MCM-UMC4 or general memory storage or for use as RAM/ROM Disks. The MCM-386SX automatically tests the status of the card and will access it in either 8 or 16-bit transfers. The card will directly address 16 Megabytes of memory which is required for large applications programs or memory intensive operating systems such as OS/2.

DRAM Refresh - The NEATsx CHIPSet generates the REFRESH* signal and refresh addresses up to 512 rows. The interval can be programmed to accommodate the requirements of various types of memories. The REFRESH* signal is buffered and can be jumpered onto the STD Bus.

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A page mode feature allows the use of slower DRAM while maintaining fast memory accesses. In the page mode, the access time becomes the column address access time (CAS), which is typically less than half of row address access time. During the page mode operation, the row address (RAS) is latched into the DRAM and is maintained logic low through all successive memory cycles if a page hit (row address of the current memory access is within the same row address page) occurs. This way of operation eliminates the time normally needed to strobe a new row address. The DRAM access time is then determined by the CAS access time which is typically equal or less than half of the RAS access time. Using a page mode scheme, a system can use slower inexpensive DRAMs and still maintain a high performance memory system.

WAIT State Generation - The NEATsx CHIPSet generates Wait States for up to 3 clock cycles during a bus cycle for either I/O or Memory transfers to compensate for the access speeds of slower memory or I/O devices.

Serial I/O - A VLSI technology VL16C452 serves as the serial communication controller mapped as a standard COM1 and COM2 port. It has two independent double buffered serial asynchronous channels that are 82C50A hardware compatible. The unit contains on-chip software programmable baud rate generators selectable through 56K bits per second. Each has independent control of transmit, receive, line status and data set interrupts. Individual modem handshake control signals are available for each line.

Each channel will support 5, 6, 7 or 8 bit characters with even, odd or no parity generation/checking. It will handle 1, 1½ or 2 stop bits.

The standard I/O map is for COM1 and COM2 (3F8-3FF hex and 2F8-2FF hex respectively). Three alternative maps are available through a jumper header.

Both channels support RS-232 electrical interface levels. Only +5 volts is required for the system since

P3 and P4 Pinout
COM1 and COM2 Serial Channel

Pin	FLOW	Signal
1	IN	Data Carrier Detect (DCD)
2	IN	Receive Data (RxD)
3	OUT	Transmit Data (TxD)
4	OUT	Data Terminal Ready (DTR)
5	--	Signal Ground (GND)
6	IN	Data Set Ready (DSR)
7	OUT	Request To Send (RTS)
8	IN	Clear To Send (CTS)
9	IN	Ring Indicator (RI)

a Maxim MAX235 chip is used which generates the $\pm$ voltages required.

Both serial channels are configured as a DTE and wired to an individual 10-pin right angle connector that permits easy connections to a standard 9-pin male D-sub connector with the WinSystems CBL-123-1.

Keyboard Controller - An 8242 keyboard controller is installed to provide a serial interface to a PC-AT type keyboard. Also the keyboard can be locked out by grounding pin 9 to prevent unauthorized access to the system.

The keyboard controller is buffered and wired to a 10-pin connector, J2. WinSystems offers the CBL-124-1 which is an adapter for the 10-pin ribbon to 5-pin DIN keyboard cable. The pinout of the 10-pin cable, J2, is as follows:

J2- Keyboard Interface

Pin	Signal
1 - 4	Ground
5 - 6	+5 volts
7	Keyboard Clock
8	+5 volts
9	Keyboard Lockout
10	Keyboard Data

Parallel I/O - The VL16C452 also provides a direct 26-pin Centronics parallel I/O interface from the MCM-386SX. It is fully bidirectional with the associated handshake lines. The standard default I/O Map is LPT1 (378-37F hex). J8 provides jumper selectable options for other locations such as LPT2.

The printer signal lines are wired to P2, a 26-pin right angle connector. The optional WinSystems' CBL-101-3

P2 Pinout - Printer Channel

Pin	FLOW	Signal
1	OUT	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper End
13	IN	Select
14	OUT	Auto Feed
15	IN	Error
16	OUT	Init. Printer
17	OUT	Select Input
18-25	— —	Ground

provides a 3-foot long adapter cable designed to convert a 26-pin ribbon cable to a 25-pin male "D" type connector with strain relief.

Counter/Timer - There are three independent software programmable 16-bit counter/timers available through a 82C54 type device. Counter 0 is dedicated to a real time clock tick output to IRQ0 of 55 mS (18.2 ticks per second). Counter 1 is available for DRAM refresh. Since the NEATsx CHIPSet generates DRAM refresh independently, then this timer could be freed for other timing purposes. Counter 2 is dedicated to the speaker oscillator. If required, it could be tied to the interrupt controller to provide another timer input.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Real Time Clock - A battery backed onboard MC146818 type clock calendar is provided by the NEATsx CHIPSet. It can be programmed for binary or BCD. It counts seconds, minutes, hours, days months, and year. It has automatic end of month recognition and leap year compensation.

Interrupts - The MCM-386SX will accept 3 interrupt signals from the STD Bus backplane (INTRQ*, INTRQ1* and INTRQ2*) and 4 additional interrupts from the front plane connector. Two onboard 82C59A

type Programmable Interrupt Controllers (PICs) provide 15 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Since the system is PC-AT compatible, the cascade address scheme is not supported over the STD Bus backplane during interrupt acknowledge cycles.

In addition to these interrupts, 2 additional independent interrupt lines are provided across the front plane for the disk and video interrupts. These are mapped into the correct, dedicated interrupt input lines to maintain PC-AT compatibility.

Dynamic Bus Sizing - The MCM-386SX has two new signals, MEM16 and I/O16, defined which automatically looks at the STD Bus memory and I/O board status to determine whether a 8 or 16-bit transfer should occur. If these signals are active low, then a 16-bit transfer will occur. If the peripheral board does not respond, then it is assumed a 8-bit transfer is required making the system upward compatible with previously designed STD Bus cards.

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Hardware Interrupt Channels

Interrupt	Description
NMI	Parity
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	INT 8-15 expansion
IRQ3	COM2
IRQ4	COM1
IRQ5	Fixed Disk/STD INTRQ*
IRQ6	Floppy Disk
IRQ7	Parallel Printer
IRQ8	Real Time Clock
IRQ9	Video
IRQ10	Interrupt Header J3/STD INTRQ1*
IRQ11	Interrupt Header J3
IRQ12	Interrupt Header J3
IRQ13	80387 Co-processor
IRQ14	Hard Disk
IRQ15	Interrupt Header J3

PC-AT I/O Map

Hex Range	Usage
000-00F	8237A-5DMA Controller 1
020-021	8259A Interrupt Controller 1
040-043	8253/8254 Timer
060-063	8255A-5 PPI (XT)
060-064	8042 Kbd. Controller (AT)
070-071	CMOS RAM & NMI Mask Reg(AT)
080-083	DMA Page Registers (XT)
080-09F	DMA Page Registers (AT)
0A0-0BF	8259A Interrupt Controller 2
0A0-0AF	NMI Mask Register (XT)
0C0-0CF	Reserved
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
0C0-0DF	8237 #2 (AT) (See Note)
0E0-0EF	Reserved
200-20F	Game I/O Adapter
210-217	Expansion Unit (XT only)
220-24F	Reserved
278-27F	Parallel Printer 2
2F0-2F7	Reserved
2F8-2FF	Serial Port 2
300-31F	Prototype Card
320-32F	Fixed Disk
360-36F	Reserved
378-37F	Parallel Printer 1
380-38F	SDLC, Bisynchronous 1
3A0-3AF	Bisynchronous 2
3B0-3BF	Monochrome Display/Printer (Printer 3BC-3BF)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Adaptor
3E0-3EF	Reserved
3F0-3F7	Floppy Disk
3F8-3FF	Serial Port 1

I/O - The MCM-386SX conforms to the PC-AT I/O map and STD Bus standard 10-bit addressing. It will support older STD Bus I/O cards that decode only 8 address bits, 8 bits with IOEXP*, and the newer 10-bit I/O cards. The MCM-386SX provides this flexibility by decoding I/O addresses 100 - 1FF and driving IOEXP* active low via a jumper option onboard. To understand both the MCM-386SX I/O map and a typical PC-AT I/O port assignment, an I/O map is listed below showing the I/O addresses, usage and where the MCM-386SX is mapped.

STD-AT Bus - The MCM-386SX originates a 16-pin interrupt and DMA controller Bus at the top of the card. This is required to provide 100% PC-AT hardware compatibility for video, disk and network controller cards while it frees the backplane interrupts for additional sources. However for small systems with video or hard disks, the interrupts can be routed over the backplane STD Bus interrupt lines.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the CPU's write line, preventing invalid data from being written to battery backed RAM's or EEPROMs during power fluctuations.

Battery - A 750 mA hour battery is provided to supply current for both the real time clock and CMOS configuration RAM.

Speaker - A speaker interface and speaker are included on the board. The speaker is mounted between the two PC boards that comprise the MCM-386SX board.

STD Bus Interface - The MCM-386SX does not require termination to work properly in STD Bus card cages. WinSystems' has correctly designed our backplanes to minimize noise and crosstalk while maintaining good power distribution, massive ground planes and a good characteristic impedance for the signal lines. The common STD Bus recommended termination simply adds unwanted capacitance and loads the bus drivers which results in slower data transitions and skewed signals.

Printed Circuit Board - The MCM-386SX is a 2 board "sandwich" that comprises the system. The first board contains the 80386SX CPU, 80387SX coprocessor socket, keyboard controller, reset circuit, and

STD Bus interface logic. It is connected through two 50-pin, gas tight, pin-and-socket connectors to a second board. This board contains the 2 EPROM sockets, DRAMs, 2 serial channels, Centronics I/O port, and real time clock. The speaker and battery are mounted in between the 2 boards. This packaging concept offers superior reliability and rugged mounting while maintaining the STD Bus 4.5" X 6.5" format.

SOFTWARE SUPPORT

The MCM-386SX is designed to support both full PC-AT DOS compatible and embedded systems applications. The key to configuration is in the firmware and software.

DOS Systems Support

STD-AT - The MCM-386SX is offered with a combination of STD Bus boards, card cage and power supply configured together to make a base PC-AT compatible system called the STD-AT. The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "software bus", for hosting operating systems utilities, real time executives, development tools, networking, and application specific programs. The basic philosophy of the STD-AT is to offer full DOS compatibility with high performance processors.

BIOS - The Basic Input/Output System (BIOS) is written by Phoenix Technologies to provide maximum performance and full IBM-AT compatibility. It is designed for high speed 80386SX systems operating a 16 MHz with no Wait States. It supports both 720KB and 1.44MB 3.5 inch and 360KB and 1.2MB 5.25 inch floppy disk drives, 101, 102, and 84-key AT-compatible keyboards, the 80387SX math coprocessor, offers enhanced protected mode to real mode switching for faster VDISK, INT 15H multitasking extensions for extended memory and block moves, IBM defined extensions to BIOS calls, and is fully compatible with Novell NetWare. The BIOS also provides complete power-on self test and boot diagnostics.

DOS - The MCM-386SX is designed to be architecturally compatible with the PC-AT. As such it will run either MS-DOS or IBM PC-DOS and will support calls either through the BIOS or directly to the hardware. The card will also support other operating systems such as UNIX or XENIX and real time executives that require a "PC-AT" hardware environment.

Embedded Systems Support

C-THRU-ROM-386SX - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable

programs with Microsoft C or Borland Turbo-C for use with the MCM-386SX. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM consists of a source level debugging user interface with target communication facility that resides on the MCM-386SX. The target system kernel includes an execution control program and host communication facility. During a debug session, the symbolic information is maintained on a PC-AT host and the program code is downloaded to the MCM-386SX for execution over a 9600 bps serial port. The application program is debugged directly on the MCM-386SX.

CTR Debugger - The C-THRU-ROM windowing debugger provides access into the MCM-386SX and is completely compatible with Microsoft C version 5.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote CodeView. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

The Debugger is a source level debugger. This means that the Debugger, in addition to understanding the 80X86/88 machine code, understands such symbols as function names, global variables, and publics, locals, and register variables. This also means that the debugger knows about line numbers, and even modules, making it possible to set break points, unassemble, and go directly to the code at any line.

With the Debugger a listing of the program appears on the screen. One can single-step through the program lines, examine variables, execute parts of the program, and watch both program listing and the output it generates. The lines of code are displayed as they are executed, giving one the opportunity to stop execution, examine and change variables and registers,

trace a single line or instruction, or even restart the program from scratch.

ROM-DOS - ROM-DOS is a MS-DOS 3.2 compatible ROM based operating system for embedded MCM-386SX applications. ROM-DOS provides 3 major functions: hardware initialization, file support and standard drivers. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied.

ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that greatly simplifies data storage and retrieval. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

A standard ROM-DOS setup has the code for ROM-DOS and Mini-BIOS in the top 64K bytes of ROM, and the user application program (.EXE file) and associated disk files in ROM on a ROM-disk. The ROM's containing the actual ROM-disk files are placed in any convenient location above the system RAM. The ROMDISK is configured as the "A" drive so ROM-DOS will search it for the initial program upon booting.

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SPECIFICATIONS

Electrical

Bus Interface: 8/16-bit STD Bus
CPU Clock: 16 or 20 MHz
STD Bus System Clock: 8 MHz
Serial Interface: 2 channels RS-232
Parallel Interface: Centronics line interface
Interrupts: TTL input with 10K ohm pull-up resistors
Vcc = +5V ± 5% at 1500 mA typ. (with no 80387SX installed)

Memory

Addressing: 16 Megabytes
Capacity: Supports up to 128K EPROM (2 sockets) and 512KB, 1MB, 2MB or 4MB supplied

Mechanical

Dimensions: Meets all STD Bus mechanical specifications: 4.5 x 5 x 6.5 inches, requires 2 card slots.

Jumpers: 0.025" square posts

Connectors

Serial I/O: 10-pin 0.100" grid
Parallel I/O: 26-pin 0.100" grid
Interrupts: 10-pin 0.100" grid
Keyboard: 10-pin 0.100" grid
STD-AT Bus: 16-pin 0.100" grid

Environmental

Operating Temperature: 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-386SX-16-512	Single board 16MHz computer with 512KB of DRAM
MCM-386SX-16-1M	Single board 16MHz 80386SX computer with 1MB of DRAM
MCM-386SX-16-2M	Single board 16MHz 80386SX computer with 2MB of DRAM
MCM-386SX-16-4M	Single board 16MHz 80386SX computer with 4MB of DRAM
MCM-386SX-20-512	Single board 20MHz computer with 512KB of DRAM
MCM-386SX-20-1M	Single board 20MHz 80386SX computer with 1MB of DRAM
MCM-386SX-20-2M	Single board 20 MHz 80386SX computer with 2MB of DRAM
MCM-386SX-20-4M	Single board 20 MHz 80386SX computer with 4MB of DRAM

WinSystems, Inc.

WinSystems®

STD BUS, CMOS STD Bus

LPM-286AT
MCM-286AT
PC-AT Compatible SBC

FEATURES

- 80C286 CPU with up to a 20 MHz clock
- Full IBM PC-AT compatibility
- Uses the Chips and Technologies NEAT (New Enhanced AT) chip set
- Supports MS/DOS, OS/2, UNIX, CP/M-86, ADA and other popular PC-AT operating systems, real time executives, and application software
- 512KB, 1MB, 2MB or 4MB of parity DRAM
- 128Kbytes of EPROM storage capacity
- 16 Megabyte direct addressing
- 80287 coprocessor socket
- Industry standard Phoenix PC-AT BIOS with power on self test (POST)
- Set Up program stored in BIOS ROM
- Shadow BIOS for improved performance
- Asynchronous I/O bus controller assures compatibility with slower I/O cards
- Dynamic Bus sizing
- 2 Serial RS-232 ports: COM1 and COM2
- Centronics compatible parallel I/O port
- Keyboard controller
- Battery backed calendar clock
- On board speaker
- Three 16-bit timer/counters
- 4 channel DMA controller
- 15 channel interrupt controller
- Full 8-bit or 16-bit STD Bus interface

- Low power
- +5 volt only operation
- Precision powerfail reset circuit
- 4.5" X 6.5" IEEE 961 STD Bus

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*SHADING INDICATES SOCKET ONLY
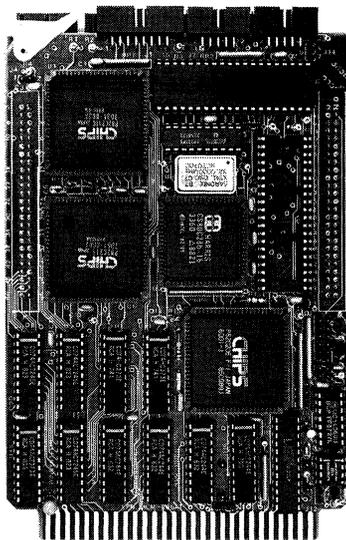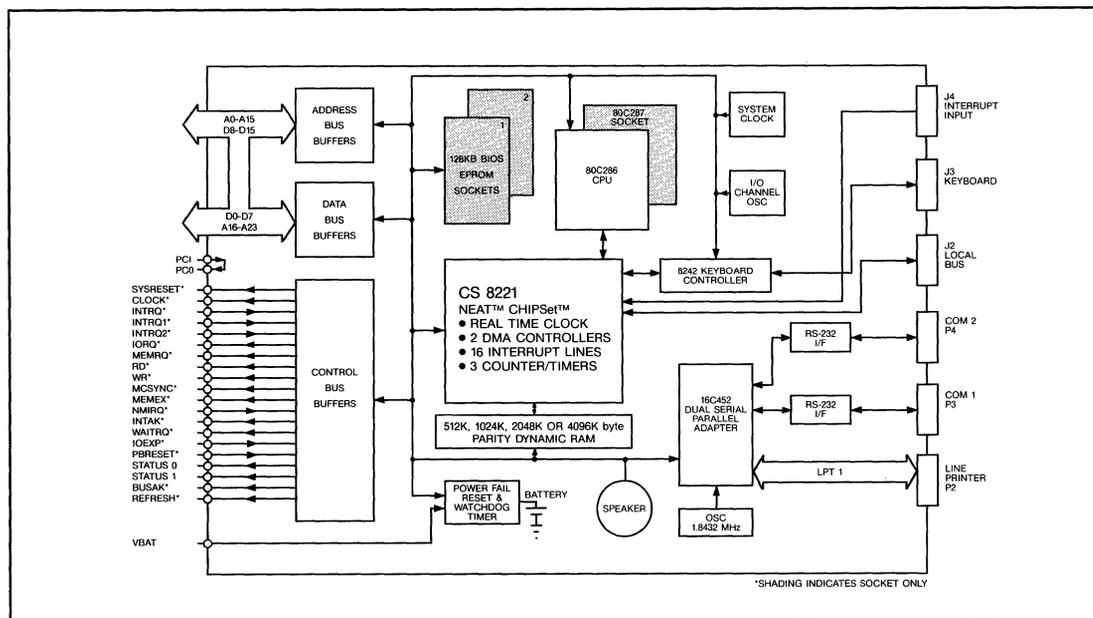
The LPM/MCM-286AT is the first truly compatible IBM PC-AT single board computer. At 16 MHz, it offers over an 18 fold performance improvement over a standard PC-XT. Its compatibility and performance is obtained through the use of the 80C286 CPU, NEAT chip set, and industry standard BIOS. This yields both 100% hardware and software PC/XT/AT compatibility. The LPM/MCM-286AT includes the Intel 80C286 CPU with either 512K, 1M, 2M or 4M bytes of RAM, an 80C287 co-processor socket, two RS-232 serial ports, a Centronics parallel port, a real time clock, keyboard controller, and speaker. The LPM/MCM-286AT requires only a single +5 volt supply.

The LPM/MCM-286AT will automatically switch speeds during accesses to the STD Bus to insure compatibility with slower memory or I/O cards. This is controlled during set up in the configuration RAM. Also, it will permit maximum speed and performance with the CPU's on card memory and I/O while working with other external memory and I/O cards. The LPM/MCM-286AT card is compatible with either 8 or 16-bit external memory or I/O cards offering upward compatibility with previously designed Win-Systems' or customer-designed STD Bus I/O cards.

The LPM/MCM-286AT is a 2 board set of cards tightly coupled through a local bus to form a complete single board computer in the standard 4.5 x 6.5 inch STD Bus form factor. The onboard mass storage can function at very high clock speeds while the I/O bus operates at a slower speed. If video and rotational mass storage are not required, then the LPM/MCM-286AT can function stand alone even with DOS by booting from ROM disk and redirecting the console through one of the COM channels.

The LPM/MCM-286AT can work without DOS and BIOS software as a stand alone single board computer. Its wealth of hardware functions make it an ideal candidate for disguised and embedded applications.

The LPM/MCM-286AT is designed to meet demanding requirements in applications such as industrial, factory floor, automatic test, instrumentation, robotics, machine control, aerospace, and other difficult environments. A 2 year limited warranty is standard. The unit has the advantage of a passive backplane with over 1200 industrial I/O cards from over 150 different STD Bus vendors.

FUNCTIONAL CAPABILITY

Processor - The LPM/MCM-286AT incorporates the powerful 16-bit 80C286 high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. The 80C286's pipelined architecture and operational speed up to 20 MHz offer performance that is comparable to many high-end minicomputers. Its large virtual address space and 80C286 hardware enforced data protection make it especially well suited for multitasking applications. Unlike the V30 (8086) and V50 CPU's, the 80C286 has built in memory protection that supports operating systems and task isolation as well as program and data privacy within tasks. A 16 MHz 80C286 provides up to 18 times greater performance than a standard PC-XT. The 80C286 includes memory management capabilities with a physical memory space of 16 megabytes. The 80C286 is upward compatible with the 8086 and 8088 software.

The 80C286 provides special operations to support the efficient implementation and execution of operation systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing segment-not-present exception and restartable instructions.

The processor is fully buffered to the STD Bus and can operate at either 10, 12, 16 or 20 MHz. According to the the Norton benchmark speed test, the LPM/MCM-286AT at 16MHz has a Performance Index (PI) of 18.7 relative to the 4.77 MHz PC-XT. The 16 MHz LPM/MCM-286AT with 0 Wait State DRAM will run faster than a Compaq 386 running at 16MHz as measured by PC Magazine's Benchmark Program release 4.02.

80287 Coprocessor - The LPM/MCM-286AT card has a socket to accept an optional 80287 coprocessor providing up to 100 times the performance of the CPU alone. The 80287 Numeric Processor Extension (NPX) provides arithmetic instructions for a variety of numeric types in 80286 systems. It provides arithmetic, logarithmic, exponential, trigonometric, and floating point arithmetic with up to 80-bit results.

NEAT Chip Set - The LPM/MCM-286AT uses the NEAT (New Enhanced AT) CHIPSet from Chips and Technologies. It is the latest generation of fully AT compatible Chips which works from 12 MHz and 16 MHz up to a fast speed of 20 MHz while still using low cost slower memories. No PCB modifications are required to allow the system to operate at different speeds.

NEAT maintains full compatibility with the IBM PC-AT. Additionally it supports the Expanded Memory Specification (EMS 4.0), expanded memory, and

advanced memory paging schemes for on-board memory. NEAT is all CMOS for very low power consumption.

NEAT supports both the MS/DOS and OS/2 operating systems. It supports the built-in FAST GATEA20 and FAST CPU RESET which allow the fast switching between the real addressing mode and protected mode. This feature will improve the OS/2 performance up to 20% over conventional chipsets which will run OS/2.

Due to shadowing of BIOS and Video ROM, system performance will not be degraded by the slow access speed of EPROM.

Unlike the IBM PC-AT, the clocks used for the CPU and STD Bus may be asynchronous or synchronous. This design allows for a greater flexibility in the system, yields higher performance and yet, maintains compatibility. In either mode, the CPU can operate at high clock speeds (up to 20 MHz); however, the clock source for the STD Bus (ATCLK) is different. This means that the LPM/MCM-286AT can work with STD Bus cards or backplanes that can only operate at 5 or 8 MHz while the CPU runs at full speed. The clock source is configurable in the NEAT set up registers.

Due to the availability of higher density memory, the extended/expanded memory can now be moved on the LPM/MCM-286AT and run at the same speed of the CPU. The performance improvement of a local memory cycle can be 300% over a STD Bus memory cycle.

The CS8221 NEAT CHIPSet provides a complete PC-AT compatible system with just 5 VLSI devices: the 82C11 CPU/Bus controller, the 82C212 Page/Interleave and EMS Memory Controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet supports the local CPU bus, a 16-bit onboard system memory bus, and the 8/16 bit STD Bus. The 82C211 provides synchronization and control signals of all buses. The 82C211 also provides an independent STD Bus clock and allows for dynamic selection between the processor clock and the user selectable STD Bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards on the STD Bus.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system designed with page mode operation. It supports up to 2 MB of on-board DRAM. The processor can operate

at 16 MHz with 0 wait state memory accesses, using 70 nS DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 IPC incorporates two 8237 DMA controllers, two 8259A interrupt controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock (RTC), 74LS612 memory mapper and other SSI interface logic chips. While offering complete compatibility to the PC-AT architecture, the chip offers enhanced features and improved speed performance. These include 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 8259, and 8254. A variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip. The chip also provides an option to select an 5 or 8 MHz system clock.

Memory - The LPM/MCM-286AT has 3 memory sources onboard: EPROM, DRAM, and Battery backed static RAM. Two memory sockets are provided to support the BIOS and any applications program. Either 32K or 64K byte EPROMs are supported in each socket. Up to 4M bytes are supplied by dynamic RAMs accessed via 16-bit data transfers. Parity is included on each byte. System configuration information and the register values for the NEAT chip set is stored in the battery powered CMOS static RAM inside the 82C206. The values from the CMOS memory or the default

Memory Map

Address Range		Usage
00000-001DF	(480)	Interrupt Vectors
001E0-002FF	(288)	User Vectors
00300-003FF	(256)	BIOS Stack
00400-004FF	(256)	BIOS Data
00500-005FF	(256)	For DOS & BASIC
00600-09FFF	(638K)	User RAM
0A000-AFFFF	(64K)	EGA Video Buffer
B0000-B7FFF	(32K)	Mono. Video Buffer
B8000-B8FFF	(32K)	CGA Video Buffer
C0000-C7FFF	(32K)	EGA Video BIOS
C8000-CFFFF	(32K)	XT Hard Disk Controller BIOS
D0000-DFFFF	(64K)	User Space
E0000-EFFFF	(64K)	User Space (PC/XT) System ROM (AT)
F0000-FFFFF	(64K)	BIOS & BASIC

ones from the BIOS EPROM will be loaded into the configuration registers when the system is turned on.

The LPM/MCM-286AT will work with either 8 or 16-bit external memory cards such as the LPM/MCM-UMC3 or LPM/MCM-UMC4. The card automatically tests the status of the card and will access it in either 8 or 16-bit transfers. The card will directly address 16 Megabytes of memory which is required for memory intensive application programs or operating systems such   as OS/2.

DRAM Refresh - The NEAT chipset generates the REFRESH* signal and refresh addresses up to 512 rows. The interval can be programmed to accommodate the requirements of various types of memories. The REFRESH* signal is buffered and can be jumpered onto the STD Bus.

A page mode feature allows the use of slower DRAM while maintaining fast memory accesses. In the page mode, the access time becomes the column address access time (CAS), which is typically less than half of row address access time. During the page mode operation, the row address (RAS) is latched into the DRAM and is maintained logic low through all successive memory cycles if a page hit (row address of the current memory access is within the same row address page) occurs. This way of operation eliminates the time normally needed to strobe a new row address. The DRAM access time is then determined by the CAS access time which is typically equal or less than half of the RAS access time. Using a page mode scheme, a system can use slower inexpensive DRAMs and still maintain a high performance memory system.

WAIT State Generation - The NEAT chipset generates Wait States for up to 3 clock cycles during a bus cycle for either I/O or Memory transfers to compensate for the access speeds of slower memory or I/O devices.

Serial I/O - A VLSI technology VL16C452 serves as the serial communication controller mapped as a standard COM1 and COM2 port. It has two independent double buffered serial asynchronous channels that are 82C50A hardware compatible. The unit contains on-chip software programmable baud rate generators selectable through 56K bits per second. Each has independent control of transmit, receive, line status and data set interrupts. Individual modem control signals are available for each line.

Each channel will support 5, 6, 7 or 8 bit characters with even, odd or no parity generation/checking. It will handle 1, 1½ or 2 stop bits.

The standard I/O map is for COM1 and COM2 (3F8-3FF and 2F8-2FF respectively). Three alternative maps are available through a jumper option.

Both channels support RS-232 electrical interface levels. Only +5 volts is required for the system since a Maxim MAX235 chip is used to generate the ± voltages required.

Both serial channels are configured as a DTE and wired to an individual 10-pin right angle connector. Easy connections to a standard 9-pin male D-sub connector is provided by the CBL-123-1 cable. The pinout is as follows:

P3 and P4 Pinout - COM1 and COM2 Serial Channel

Pin	FLOW	Signal
1	IN	Data Carrier Detect (DCD)
2	IN	Receive Data (RxD)
3	OUT	Transmit Data (TxD)
4	OUT	Data Terminal Ready (DTR)
5	--	Signal Ground (GND)
6	IN	Data Set Ready (DSR)
7	OUT	Request To Send (RTS)
8	IN	Clear To Send (CTS)
9	IN	Ring Indicator (RI)

Keyboard Controller - An 8242 keyboard controller is installed to provide a serial interface to a PC-AT type keyboard. A jumper, J5, is provided on the card to disable the unit if no keyboard is used in the application. Also the keyboard can be locked out by grounding pin 9 to prevent unauthorized access to the system.

The keyboard controller is buffered and wired to 10 pin connector. WinSystems offers the CBL-124-1 which is an adapter for the 10-pin ribbon to 5-pin female DIN keyboard cable. The pinout of the 10-pin cable, J2, is as follows:

J2 - Keyboard Interface

Pin	Signal
1 - 4	Ground
5 - 6	+5 volts
7	Keyboard Clock
8	+5 volts
9	Keyboard Lockout
10	Keyboard Data

Parallel I/O - The VL16C452 also provides a direct 26-pin Centronics parallel I/O interface from the LPM/MCM-286AT. It is fully bi-directional with the associated handshake lines. The standard default I/O Map is LPT1 (378-37F hex). J8 provides jumper selectable options for other locations such as LPT2.

The printer signal lines are wired to P2, a 26-pin right angle connector. The optional WinSystems' CBL-101-3

provides a 3 foot long adapter cable designed to convert a 26-pin ribbon cable to a 25-pin male "D" type connector with strain relief.

P2 Pinout - Printer Channel

Pin	FLOW	Signal
1	OUT	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper End
13	IN	Select
14	OUT	Auto Feed
15	IN	Error
16	OUT	Init. Printer
17	OUT	Select Input
18-25	— —	Ground

Counter/Timer - There are three independent software programmable 16-bit counter/timers available through a 8254 type device. Counter 0 is dedicated to a real time clock tick output to IRQ0 of 55 mS (18.2 ticks per second). Counter 1 is available for DRAM refresh. Since the NEAT CHIPSet generates DRAM refresh independently, this timer can be freed for other timing purposes. Counter 2 is dedicated to the speaker oscillator. If required, it could be tied to the interrupt controller to provided another timer input.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Real Time Clock - A battery backed onboard MC146818 type clock calendar is provided by the NEAT chipset. It can be programmed for binary or BCD. It counts seconds, minutes, hours, days, months, and year. It has automatic end of month recognition and leap year compensation.

Interrupts - The LPM/MCM-286AT will accept 3 interrupt signals from the STD Bus backplane (INTRQ*, INTRQ1* and INTRQ2*) and 5 additional

interrupts from the front plane connector. Two onboard 8259A type Programmable Interrupt Controllers (PICs) provide 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Since the system is PC/XT/AT compatible, the cascade address scheme is not supported over the backplane during interrupt acknowledge cycles.

In addition to these interrupts, 2 additional independent interrupt lines are provided across the front plane for the disk and video interrupts. These are mapped into the correct, dedicated interrupt input lines to maintain PC-AT compatibility.

Hardware Interrupt Channels

Pin	FLOW
NMI	Parity
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	INT 8-15 expansion
IRQ3	COM2
IRQ4	COM1
IRQ5	Fixed Disk/STD INTRQ*
IRQ6	Floppy Disk
IRQ7	Parallel Printer
IRQ8	Real Time Clock
IRQ9	Video
IRQ10	Interrupt Header J3/STD INTRQ1*
IRQ11	Interrupt Header J3
IRQ12	Interrupt Header J3
IRQ13	80287 Co-processor
IRQ14	Hard Disk
IRQ15	Interrupt Header J3

Dynamic Bus Sizing - The LPM/MCM-286AT has two new signals, MEM16 and I/O16, defined which automatically looks at the STD Bus memory and I/O board status to determine whether a 8 or 16-bit transfer should occur. If these signals are active low, then a 16-bit transfer will occure. If the peripheral board does not respond, it is assumed that a 8-bit transfer is required making the systems upward compatible with previously designed STD Bus cards.

STD-AT Bus - The LPM/MCM-286AT originates a 16-pin interrupt and DMA controller Bus at the top of the card. This is required to provide 100% PC-AT hardware compatibility for video, disk and network controller cards while it frees the backplane interrupts for additional sources. However for small systems with video or hard disks, the interrupts can be routed over the backplane STD Bus interrupt lines.

Reset - A precision voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically

important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the CPU's write line, preventing invalid data from being written to battery backed RAM's or EEPROMs during power fluctuations.

Battery - A 750 mA hour battery is provided to supply current for both the real time clock and CMOS configuration RAM.

Speaker - A speaker interface and speaker are included on the board. The speaker is mounted between the two PC boards that comprise the LPM/MCM-286AT.

I/O - The LPM/MCM-286AT conforms to the PC-AT I/O map and standard 10-bit addressing. It is recommended that general purpose I/O boards operate in

PC-AT I/O Map

Hex Range	Usage
000-00F	8237A-5DMA Controller 1
020-021	8259A Interrupt Controller 1
040-043	8253/8254 Timer
060-063	8255A-5 PPI (XT)
060-064	8042 Kbd. Controller (AT)
070-071	CMOS RAM & NMI Mask Reg(AT)
080-083	DMA Page Registers (XT)
080-09F	DMA Page Registers (AT)
0A0-0BF	8259A Interrupt Controller 2
0A0-0AF	NMI Mask Register (XT)
0C0-0CF	Reserved
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
0C0-0DF	8237 #2 (AT)
0E0-0EF	Reserved
200-20F	Game I/O Adapter
210-217	Expansion Unit (XT only)
220-24F	Reserved
278-27F	Parallel Printer 2
2F0-2F7	Reserved
2F8-2FF	Serial Port 2
300-31F	Prototype Card
320-32F	Fixed Disk
360-36F	Reserved
378-37F	Parallel Printer 1
380-38F	SDLC, Bisynchronous 1
3A0-3AF	Bisynchronous 2
3B0-3BF	Monochrome Display/Printer (Printer 3BC-3BF)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Adaptor
3E0-3EF	Reserved
3F0-3F7	Floppy Disk
3F8-3FF	Serial Port 1

the 100-1FF hex address space. The LPM/MCM-286AT additionally decodes I/O addresses 100 - 1FF and drives IOEXP* active low via a jumper option onboard. The reason for this circuit is to support 8-bit only STD Bus I/O boards within the 10-bit PC/XT/AT address space.

STD Bus Interface - The LPM/MCM-286AT does not require termination to work properly in STD Bus card cages. WinSystems has correctly designed our backplanes to minimize noise and crosstalk while maintaining good power distribution, massive ground planes and a good characteristic impedance for the signal lines. The common STD Bus recommended termination simply adds unwanted capacitance and loads the bus drivers which results in slower data transitions and skewed signals.

CMOS STD Bus - The MCM prefix on the 286AT card designates a standard STD Bus board. The LPM prefix designates a CMOS STD Bus board. A LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS and regular NMOS/TTL logic. The difference between these two products are the power requirements and operational temperature ranges.

SOFTWARE SUPPORT

The LPM/MCM-286AT is designed to support both full PC-AT DOS compatible and embedded systems applications. The key to configuration is in the firmware and software.

DOS Systems Support

STD-AT - The LPM/MCM-286AT is offered with a combination of STD Bus boards, card cage and power supply configured together to make a base PC-AT compatible system called the STD-AT. The STD-AT blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "software bus", for hosting operating systems utilities, real time executives, development tools, networking, and application specific programs. The basic philosophy of the STD-AT is to offer full DOS compatibility with high performance processors.

BIOS - The Basic Input/Output System (BIOS) is written by Phoenix Technologies to provide maximum performance and full IBM-AT compatibility. It supports both 720KB and 1.44MB 3.5 inch and 360KB and 1.2MB 5.25 inch floppy disk drives, 101, 102, and 84-key AT-compatible keyboards, the 80287 math coprocessor, offers enhanced protected mode to real mode

switching for faster VDISK, INT 15H multitasking extensions for extended memory and block moves, IBM defined extensions to BIOS calls, and is fully compatible with Novell NetWare. The BIOS also provides complete power-on self test and boot diagnostics.

DOS - The LPM/MCM-286AT is designed to be architecturally compatible with the PC-AT. As such it will run either MS-DOS or IBM-DOS and will support calls either through the BIOS or directly to the hardware. The card will also support other operating systems such as UNIX or XENIX and real time executives that require a "PC-AT" hardware environment.

Embedded Systems Support

C-THRU-ROM-286AT - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the LPM/MCM-286AT. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

The C-THRU-ROM windowing debugger provides access into the LPM/MCM-286AT and is completely compatible with Microsoft C version 5.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote CodeView. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

ROM-DOS - ROM-DOS is a MS-DOS 3.3 compatible ROM based operating system for embedded LPM/MCM-286AT applications. ROM-DOS provides 3 major functions: hardware initialization, file support and standard drivers. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied.

ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that greatly simplifies data storage and retrieval. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

SPECIFICATIONS

4

Electrical

Bus Interface: 8/16 STD Bus and CMOS STD Bus
System Clock: 10, 12, 16 or 20 MHz
Serial Interface: 2 channels RS-232
Parallel Interface: Centronics line interface
Interrupts: TTL input with 10K ohm pull-up resistors
Vcc +5V $\pm$ 5% at 1000 mA typ. (with no 80287 installed)

Memory

Addressing: 16 Megabytes
Capacity: Supports up to 128K EPROM (2 sockets) and either 512KB, 1MB, 2MB or 4MB supplied

Mechanical

Dimensions: Meets all STD Bus mechanical specifications: 4.5 x 6.5 inches, requires 2 card slots.

Jumpers: 0.025" square posts

Connectors

Serial I/O: 10-pin 0.100" grid
Parallel I/O: 26-pin 0.100" grid
Interrupts: 10-pin 0.100" grid
Keyboard: 10-pin 0.100" grid
STD-AT Bus: 16-pin 0.100" grid

Environmental

Operating Temperature:
                0° to +70° Centigrade (LPM-286AT)
                0° to +65° Centigrade (MCM-286AT)
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-286AT-10-512	Single board 10MHz computer with 512KB of DRAM
MCM-286AT-10-1M	Single board 10MHz 80286 computer with 1MB of DRAM
MCM-286AT-10-2M	Single board 10MHz 80286 computer with 2MB of DRAM
MCM-286AT-10-4M	Single board 10MHz 80286 computer with 4MB of DRAM
MCM-286AT-12-512	Single board 12MHz computer with 512KB of DRAM
MCM-286AT-12-1M	Single board 12MHz 80286 computer with 1MB of DRAM
MCM-286AT-12-2M	Single board 12MHz 80286 computer with 2MB of DRAM
MCM-286AT-12-4M	Single board 12MHz 80286 computer with 4MB of DRAM
MCM-286AT-16-512	Single board 16MHz computer with 512KB of DRAM
MCM-286AT-16-1M	Single board 16MHz 80286 computer with 1MB of DRAM
MCM-286AT-16-2M	Single board 16MHz 80286 computer with 2MB of DRAM
MCM-286AT-16-4M	Single board 16MHz 80286 computer with 4MB of DRAM
MCM-286AT-20-512	Single board 20MHZ computer with 512KB of DRAM
MCM-286AT-20-1M	Single board 20MHz 80286 computer with 1MB of DRAM
MCM-286AT-20-2M	Single board 20MHz 80286 computer with 2MB of DRAM
MCM-286AT-20-4M	Single board 20MHz 80286 computer with 4MB of DRAM
LPM-285AT-10-512	Single board 10MHz 80C286 computer with 512KB of DRAM
LPM-286AT-10-1M	Single board 10MHz 80C286 computer with 1MB of DRAM
LPM-286AT-10-2M	Single board 10MHz 80C286 computer with 2MB of DRAM
LPM-286AT-10-4M	Single board 10MHz 80C286 computer with 4MB of DRAM
LPM-286AT-12-512	Single board 12MHz 80C286 computer with 512KB of DRAM
LPM-286AT-12-1M	Single board 12MHz 80C286 computer with 1MB of DRAM
LPM-286AT-12-2M	Single board 12MHz 80C286 computer with 2MB of DRAM
LPM-286AT-12-4M	Single board 12MHz 80C286 computer with 4MB of DRAM
LPM-286AT-16-512	Single board 16MHz 80C286 computer with 512KB of DRAM
LPM-286AT-16-1M	Single board 16MHz 80C286 computer with 1MB of DRAM
LPM-286AT-16-2M	Single board 16MHz 80C286 computer with 2MB of DRAM
LPM-286AT-16-4M	Single board 16MHz 80C286 computer with 4MB of DRAM
LPM-286AT-20-512	Single board 20MHz 80C286 computer with 512KB of DRAM
LPM-286AT-20-1M	Single board 20MHz 80C286 computer with 1MB of DRAM
LPM-286AT-20-2M	Single board 20MHz 80C286 computer with 2MB of DRAM
LPM-286AT-20-4M	Single board 20MHz 80C286 computer with 4MB of DRAM

WinSystems, Inc.

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FEATURES

- STD Bus 50 MHz AT&T DSP32C board
- 25 MFLOPS Operation
- 32-Bit architecture onboard including floating point arithmetic
- 64KB or 256KB of onboard memory
- Easy to program, C-like assembly language
- Plug-in daughter boards for I/O
  - 16-bit A/D converter
  - 16-bit 8KHz CODEC
  - 16-bit A/D and D/A
  - High speed Serial I/O
  - Prototype cards
- Window based debugger for Microsoft or Borland C
- Optional AT&T software libraries include C compiler, assembler/linker/ and applications library
- Third party application software

The MCM-DSP32C is a 50 MHz AT&T DSP32C based STD Bus Digital Signal Processor board designed for a wide range of computation-intensive applications such as waveform analysis, process control digital audio and speech processing.

A daughter board adapter is located on the MCM-DSP32C that accepts serial I/O, CODEC, 16-bit A/D and D/A or a prototype card. These options allow a user to select or design an interface card to match the specific application requirement.
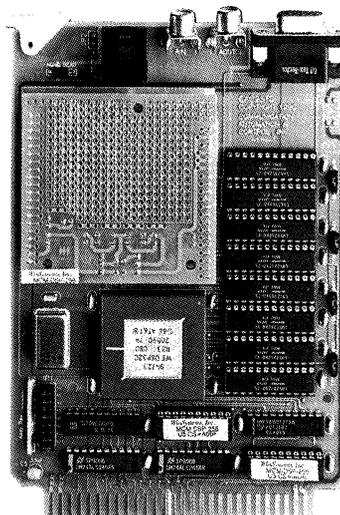
DSP OVERVIEW

Why Use a DSP? - The field of signal processing has exploded in the last few years. A new class of

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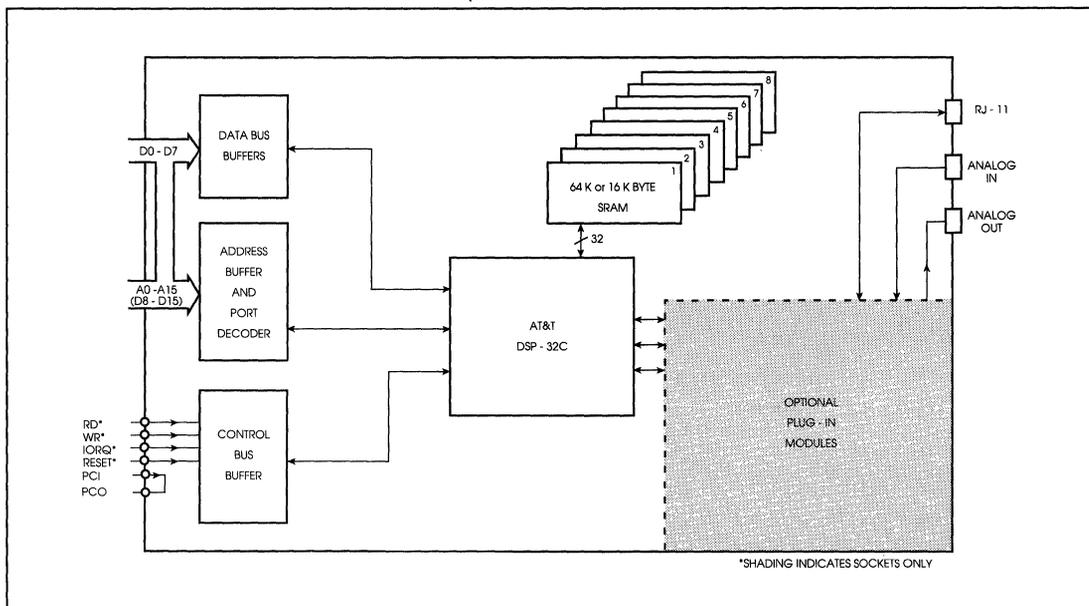
microprocessor called the DSP has appeared with register architectures, features, and performance characteristics useful in many types of embedded systems, including telecommunications, Instrumentation, Industrial, and Government/Military. Since a DSP is a digital design, it replaces resistors, capacitors, diodes, transistors, and Op Amps. Digital parts will not drift, are more stable, and can easily be retuned or modified in software rather than with a different component selection. Any complex operation in the analog world can be done with a fewer parts, less cost, better stability, and more flexibility using a DSP.

Digital signal processors (DSPs) offer a high performance, cost-effective and easy-to-use solution in many traditional and emerging signal processing applications. Digital signal processing involves the representation, transmission, and manipulation of signals using numerical techniques and digital processors. A DSP chip is designed to perform arithmetic calculations rapidly and efficiently, usually on sequences of digital numbers that represent and actual signal found in nature, such as speech.

The arithmetic calculation is multiply and accumulated for modulation, transforms, implementing filters and other digital signal processing functions. Optimization of the DSP architecture to perform processing algorithms efficiently sets DSPs apart from other general purpose microprocessors, whether CISC or RISC. A typical DSP executes its algorithms 10 times faster than a general purpose microprocessor of comparable technology.

Application Categories

Telecommunications	Industrial
Data Transmission	Robotics
Data Compression	Image Processing
Transient Analysis	Process Control
Filtering	Spectral Analysis
Test Equipment	Vibration Analysis
Channel Analysis	Biomedical Signal
Speech Recognition	Evaluation

Government/Military	
Sonar	ECM
Precision FFT	Math Accelerators
Simulation	Encryption

FUNCTIONAL CAPABILITY

DSP-32C - AT&T's DSP32C digital signal processor is one of the fastest and most versatile, low cost floating point coprocessors available. It is a high-speed, programmable integrated circuit comprised of a 32-bit

floating-point unit, a 16/24 bit fixed point unit, on-chip memory, and flexible serial I/O port.

The AT&T DSP32C chip is a 32-bit CMOS floating point processor rated at 25 MFLOPS (Million Floating point Operations Per Second). It has four 40-bit accumulators, twenty-two general purpose registers, and 6K bytes of internal RAM and supports IEEE Std. 754 floating point format conversion with only a single instruction.

The DSP32C has 2 general types of instructions that correspond to the two execution units: data arithmetic (DA) instructions and control arithmetic (CA) instructions. Primarily, DA instructions perform 32-bit floating-point multiply/accumulate operations for signal processing algorithms. Other DA instructions convert the DSP32C internal floating-point data to and from each of the following types: 8-, 16-, or 24-bit single precision IEEE 754 standard floating-point. The CA instructions perform microprocessor operation such as 16- and 24-bit integer arithmetic and logic functions, conditional branching, and moving data.

Performance - The MCM-DSP32C, operating at a clock frequency of 50 MHz, is available with either 64KB or 256KB of high speed, 32-bit wide, zero wait state RAMs. In key benchmarks, it can execute a 1024 point complex FFT (Fast Fourier Transform) in 3.3 milliseconds, a 4x4 matrix multiply in 6.16 microseconds, and a complex adaptive FIR filter in 80 nanoseconds/tap.

On-board memory - Zero wait-state, 25nS SRAM is used to augment the internal 6Kbytes of internal memory for maximum throughput. The MCM-DSP32C-A0 is normally shipped with 64KBytes but can be upgraded to 256KB by the user or by returning the board for factory upgrade. The conversion amounts to replacing the eight memory chips and moving four jumpers. Alternatively, the board can be ordered as an MCM-DSP32C-C0 which comes with 256KB of memory.

STD Bus Interface - The MCM-DSP32C's execution is independent of a STD Bus host CPU. The high speed data transfer (up to 3.5Mbytes/sec) between the DSP and the host is achieved through programmed I/O which does not interfere with the MCM-DSP32C's operation. The MCM-DSP32C supports either 8 or 16-bit data transfers to the STD Bus.

The board is I/O mapped, requires 16 consecutive I/O addresses, and is jumper configurable from 000 to FF0 hex. All software support requires the MS-DOS operating system operating in the host STD Bus CPU.

I/O EXPANSION BOARDS

A daughter board adapter is located on the MCM-DSP32C that accepts a Serial I/O, CODEC, 16-bit A/D or prototype board. An RJ11 telephone handset connector, phono connector, and subminiature female 15-pin D connector provides easy and convenient interconnection from the daughter boards to external signals. No daughter boards are required to use the MCM-DSP32C as a general purpose math accelerator.

DBCS5339

The DBCS5339 provides dual channel audio analog input between the external connectors of the DSP32C board and the DSP's serial port. The DBCS5339 daughter board provides a 16-bit, dual channel 48KHz delta-sigma A/D and anti-aliasing filters for spectral analysis and filtering applications. It features the Crystal Semiconductor, Inc. CS5339 delta-sigma A/D converter and input amplifiers/attenuators. The trimpots adjust the input signal from 0.1 to 10 times. Highlights of the board include:

- 16-bit dual channel ADC
- 20/24/32/44.1/48 KHz alternative sampling rate options (oscillator determines rate)
- Simultaneous sampling of both channels
- Anti-aliasing filters
- Delta-sigma modulation
- 64x oversampling
- 3-stage digital FIR filter
- 90db Signal to Noise ratio

DBT7525

The DBT7525 board provides a single channel, high precision, PCM, 16-bit CODEC at a standard rate of 8 KHz for use with telecommunications applications. It provides a single-channel voice band interface. It features the AT&T T7525 CODEC with 15-bit resolution, 10-bit linearity, anti-aliasing and reconstruction filters, and a precision voltage reference. The encoder uses a double-loop, sigma-delta modulator at a 1.024 MHz sampling frequency. Signals are interfaced via the RJ11 telephone handset or phono-plugs on the MCM-DSP32C board's edge.

DBDADA

The DBDADA-50 is both a 16-bit A/D and D/A board that provides exceptional quality analog interfacing for speech, pro-audio and industrial control applications. Both input and output converters are sigma-delta devices with a standard oscillator frequency of 50KHz.

Other frequencies available include 8, 16, 20, 24, 32, 44.1 48, and 51.2 KHz. The analog input range is ± 3.5 volts and the analog output range is ± 2.0 volts.

DBSERIAL

The DBSERIAL daughter board buffers the DSP32C on-chip serial port with the subminiature 15-pin D-type female connector. Jumpers are used to select the direction of the timing signals which can be generated by the DSP32C chip or external circuitry.

DBPROTO

The DBPROTO board is designed to be a general purpose prototype card for use by customers that need to design special purpose interface electronics to the MCM-DSP32C board. Custom circuits can first be wire-wrapped with the prototype board DBPROTO. If an analog board is being designed, use the DBPROTO-V which has voltage regulators that supply a noise-reduced $\pm 5V$ power source.

SOFTWARE SUPPORT

D3EMU, Window Based Debugger - To facilitate debugging, WinSystems offers a screen-oriented, user friendly package called D3EMU. Highlights include:

- Three windows to display/modify memory contents with scrolling and paging. Data formats can be hex, decimal, floating point, or disassembled code.
- Separate windows for accumulators and registers
- Twenty-one breakpoints
- Single stepping with automatic window update
- Full speed execution
- Automatic Help windows
- Values that change between breakpoints are highlighted by a flashing colon
- D3EMU windows can be called up by your host's Microsoft C or Turbo-C program

The contents of accumulators, registers, and memory are automatically updated on the screen as you single-step through the DSP code. Break points, source code labels and multiple board applications are supported. A run-time library, either Microsoft-C or Borland Turbo-C linkable, provides upload and download of data, and location of source code labels. All of the debugging features of D3EMU can be accessed by the user's host program with only two function calls. The source code of several demo programs are included as examples on how to implement the MCM-DSP32C, ranging from a simple inverse routine to a commonly used matrix multiplication and a complete FFT function.

AT&T Software - Extensive software support from AT&T's includes a C-compiler, assembler, link editor and simulator. A collection of trigonometric, matrix, FFT, and filter functions are available with the AT&T applications support software library.

DSP32C-SL - Application programs for the WE DSP32C digital signal processors are developed using the WE DSP32C-SL Support Software Library, which includes tools used to assemble, link, and debug DSP32C code at the assembly language level. The support software is provided on 5¼" floppy diskettes that are compatible with MS-DOS.

The assembler translates the DSP32C source files into machine-coded instructions placed in a object file. The linker combines object files, performs relocation, resolves external references, and generates symbol table information for symbolic testing. Other utilities include an archiver, symbolic table lister, etc.

DSP32C-CC C Language Compiler - The optimizing C Language compiler for the DSP32C family allows application programs to be written in a general, high-level language. In applications where preliminary program development is performed using the C language, the source code can be ported to the DSP32C with a minimal amount of time and effort. The AT&T compiler provides a full implementation of the standard Kernighan and Ritchie C language for directly converting C source into object code for the DSP32C. The complete limb library is provided along with an appropriate libc library. Included is the WE DSP32C-AL (application library) software package whose functions are C-callable. If the assembly programs will be developed without the compiler, then order the DSP32C-AL software as well.

DSP32C-AL Application Software Library - This package contains the source code on floppy diskettes for a set of over 65 commonly used routines written in optimized assembly language for the DSP32C chip. The library is divided into sections covering arithmetic, matrix, graphics/imaging, filter, adaptive filter and FFT routines.

DEVELOPMENT SYSTEM

WinSystems offers a complete development system package so that a user can successfully implement the DSP32C in a WinSystems' STD-AT system. The

MCM-DSP32C-A0-DS includes the MCM-DSP32C-A0 card with 64K bytes of fast SRAM, DSP-32C-SL support library, DSP-32C-AL applications library, D3EMU debugger, and DSP32C information manual and data sheet. The MCM-DSP32C-A0-CDS includes everything above plus adds the DSP32C-CC C language compiler. The MCM-DSP32C-C0-DS and MCM-DSP32C-C0-CDS are similar except the latter contains 256Kbytes of memory on board.

SPECIFICATIONS

Electrical
STD Bus Compatible
MCM-DSP32C-A0: 64K Bytes 0-WS SRAM
MCM-DSP32C-C0: 256K Bytes 0-WS SRAM
Power: +5V @ 400 mA. (typ.)

Mechanical
Size: 4.5" X 6.5"
Environmental
Operating Temperature: 0°C to 55°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-DSP32C-A0	STD Bus DSP w/64Kb SRAM
MCM-DSP32C-A0-CDS	C Development system
MCM-DSP32C-A0-DS	64KB Development system
MCM-DSP32C-C0	STD Bus DSP w/256Kb SRAM
MCM-DSP32C-C0-CDS	C Development system
MCM-DSP32C-C0-DS	256KB development system
DBPROTO	Wirewrap proto card
DBPROTO-V	Proto card with ± 5V
DBSERIAL	Serial RS-232 driver/receiver
DBT7525	16-bit, 8 KHz CODEC
DBCS5339-50	Dual 16-bit, 50 KHz A/D
DBDADA-50	Dual 16-bit, 50 KHz A/D & D/A
D3EMU	Window-based debugger
DSP32C-CC	AT&T C compiler (includes DSP32C-SL)
DSP32C-SL	AT&T assembler/linker
DSP32C-AL	AT&T applications library

WinSystems, Inc.

WinSystems®

STD BUS, CMOS STD BUS

LPM-SX386
MCM-SX386
Low Cost 80386SX SBC

FEATURES

- 80386SX CPU with 16, 20, 25 and 33MHz clock
- STD Bus or standalone operation
- Up to 4Mbytes of parity onboard system DRAM
- Shadow RAM BIOS support
- Optional onboard bootable ROM Disk
- Supports MS-DOS, QNX, other operating systems and user applications
- Real-time clock with battery backup
- One parallel port (LPT1)
- Two serial ports (COM1 & COM2) with RS-232/485/422 levels
- Watchdog Timer and Power Fail Reset
- Onboard 16-bit IDE hard disk interface
- Onboard floppy disk controller
- Two interrupt controllers
- Three 16-bit Counter/timers
- Keyboard and speaker port
- Optional 80387SX co processor support
- PC/104 Expansion Bus for VGA, Solid State Disk, and other stackable I/O cards
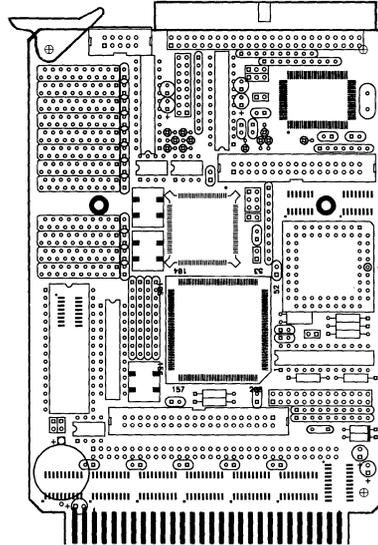
The LPM/MCM-SX386 is a fast, low cost, embeddable unit designed to provide users with a complete high performance system on just one board. It is designed for applications where PC power and performance are needed in a small system, but offers rugged hardware suitable for operation in harsh or remote environments.

Embedded Applications - The LPM/MCM-SX386 is an unbeatable multi-purpose board for use with either a STD Bus system or as a standalone controller with PC/104 expansion modules. It is fully functional for industrial applications and will run without disks, keyboard, or monitor. The LPM-SX386 can operate from -40°C to +85°C.

4 - 39
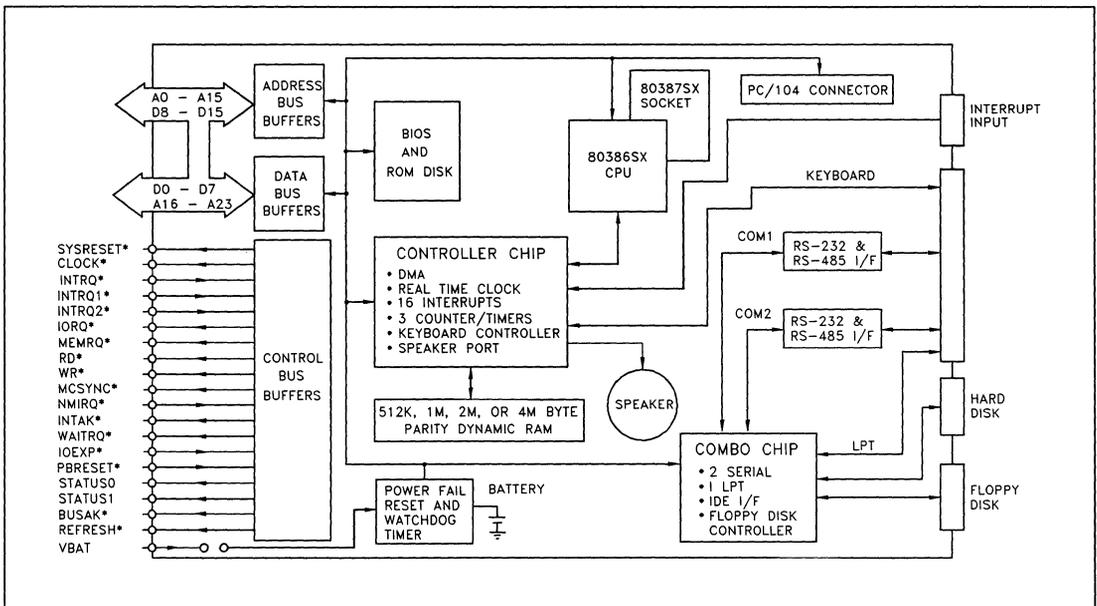
Processor - The LPM/MCM-SX386 is based upon the powerful 32-bit 80386SX high performance CPU running at clock speeds up to 33 MHz. A 80387SX socket is provided to support a user installable coprocessor for math intensive applications.

Memory - Up to 4Mbytes of parity checked dynamic RAM may be installed on the board. Built-in page mode operation and two way interleaving maximizes system performance using low cost DRAMs. A 32-pin EPROM socket can support up to a 512Kbyte device. The EPROM can be mapped to include the AT BIOS, BIOS extensions and up to a 440Kbyte bootable ROM Disk. Additional solid state disk support is available via expansion cards on the STD Bus or PC/104 Bus.

Core Logic Chip Set - The board uses a VLSI chip set to provide the basic AT peripheral logic map to allow the board to adhere to PC hardware standards. The 8042 keyboard controller, dual 8259A interrupt controllers, 146818A compatible real time clock, dual 8237 DMA controllers, DRAM refresh controller, parity generation and checking logic, speaker interface, and Bus steering logic are on a single chip.

The real time clock is battery backed by an onboard cell. It also includes 128 extra battery-backed RAM locations for system configuration information.

Serial I/O - Two equivalent 82C50 UARTs are implemented that are fully compatible with the 16450 ACE registers. Both serial channels are configured as Data Terminal Equipment (DTE) with modem control lines. Both channels support RS-232 and two wire RS-485. COM2 can support RS-422 if COM1 is configured as RS-232 only.

Keyboard - This board supports a PC/AT type keyboard including keylock.

Printer Port - A full Centronics compatible parallel printer interface is provided on the board with 24 mA drivers on the output buffers.

3.5″ and 5.25″ Floppy Disk Support - Up to 2 floppy disk drives are supported by the board. The output buffers are capable of sinking 48mA and are accessed via a standard 34-pin connector.

IDE Hard Disk Interface - A 40-pin header connector handles all command, data, and status I/O lines to an industry standard IDE interface.

Interrupts - The LPM/MCM-SX386 board will accept 4 interrupt signals from the STD Bus backplane (NMIRQ*, INTRQ*, INTRQ1*, and INTRQ2*) and 4 additional interrupts from the front plane. The front plane connector is compatible with the interrupt connector of WinSystems' LPM/MCM-286AT, LPM/MCM-386SX, and MCM-486SX/DX single board computers.

PC/104 Expansion Bus -This board has a PC/104 interface that supports the ultra-compact (3.6 x 3.8 inch), stackable modules that are offered by a number of third party companies. These modules support video, LANs, analog, digital and other special purpose I/O functions at a low cost.

Standalone Operation - The LPM/MCM-SX386 is designed to operate without a STD Bus backplane. A separate power connector is located on the board to provide power. The board is only 4.5 x 6.5 inches which is ideal for use as a low power AT computer for embedded or portable industrial applications. It also contains a watchdog timer and powerfail reset circuit for use in remote and unattended applications.

CMOS STD Bus - The MCM prefix on the SX386 card designates a standard STD Bus board. The LPM prefix designates a CMOS STD Bus board. A LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS and regular NMOS/TTL logic. The difference between these two products are the power requirements and operational temperature ranges.

This board is designed to replace WinSystems' LPM/MCM-286AT and LPM/MCM-386SX boards with higher functionality at a lower cost.

Software Support - The LPM/MCM-SX386 is designed to support both full PC-AT DOS compatible and embedded systems applications. It can operate with or without a full complement of video, keyboard, and rotational media depending upon the application. The board supports DOS, ROM-DOS, QNX and other application specific software, utilities that require a "DOS compatible" hardware platform.

ORDERING INFORMATION

This product brief outlines the basic features of the low cost LPM/MCM-SX386 at the time of the printing of the WinSystems' STD Bus databook. Please contact us for detailed specifications, configuration options, price and delivery information.

WinSystems, Inc.

FEATURES

- 10 or 16 MHz NEC V53 16-bit CPU
  - Fast 80286 class performance
  - High integration at low cost
- Four, 32-pin bytewide memory sockets support up to 2 MB of onboard SRAM, psuedo-Static RAM, EPROM, and PEROMs (Flash)
- Support optional battery backed RAM operation
- 80C287 coprocessor socket
- Memory and I/O WAIT State generator
- Three serial ports:
  - Channel 1, 8250 type, RS-232/485
  - Channel 2, 8250 type, RS-232/485/422
  - Channel 3, 8251 type, TTL level RS-232
- 8 Channel Interrupt Controller (82C59 type)
- Centronics parallel printer port
- Three 16-bit Counter/Timer channels (82C54)
- SBX expansion connector
- Dynamic 8/16-bit bus sizing
- Calendar clock with optional battery
- Watchdog timer
- Activity status LED
- Precision power-on/brown-out detect circuit
- Optional ROM-DOS for embedded applications
- Borland Turbo C and Microsoft C remote
- symbolic debuggers supported
- +5 Vdc only required
- Small, 4.5" x 6.5" STD Bus Interface
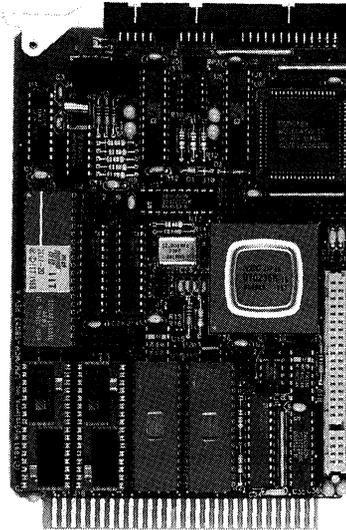
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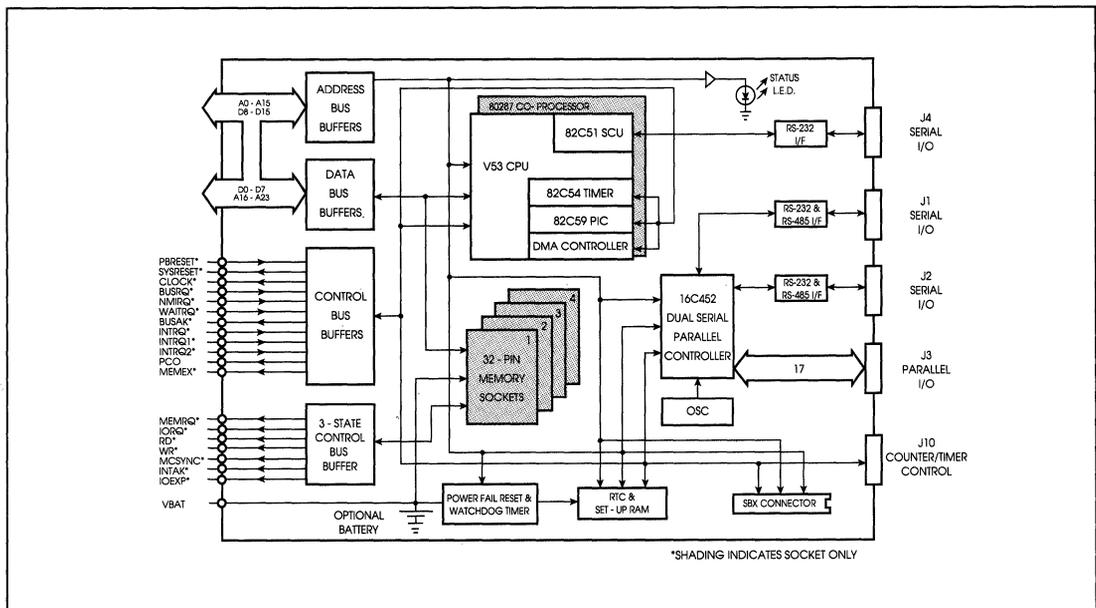
OVERVIEW

The LPM/MCM-SBC53 is a high performance, 16-bit, V53 STD Bus single board computer designed for harsh embedded applications where small size, low cost, and 80286 PC-AT performance are required. It combines the most popular I/O functions used in most applications onto a single card.

A wide range of software support is available including remote symbolic debuggers that support both Borland Turbo C and MicroSoft C as well as the macro assembler. DOS operating from ROM is an option to provide access to a wide range of applications programs, utilities and tools.

The LPM/MCM-SBC53 is available in 3 different configurations depending upon software support requirements. The board is available as a single board computer for embedded applications written in C or assembly language with no operating system supplied by WinSystems. This configuration is designated the LPM/MCM-SBC53.

For applications with high level language support, file management, or other operating systems environment structures, WinSystems offers two additional versions that support DOS. Full MS-DOS 3.3 is supported on the LPM/MCM-SBC53PC for industrial PC-AT type applications. Coupled with the MCM-DSKIO board, hard disk, floppy disk, and keyboard support is added for systems requiring rotational media. WinSystems offers display boards for MDA through VGA video and EL, LCD, and plasma flat panel displays.

ROM-DOS is available for the lowest cost, optimized embedded system designs that need to boot from ROM and run DOS executable (.EXE and .COM) files. ROM-DOS requires only very minimum hardware and does not require keyboards, displays or disks to work. ROM-DOS eliminates many portions of DOS that are "excess baggage" but still supports memory management, MS-DOS compatible file support, time functions, and installable device drivers. This board is designated LPM/MCM-SBC53R.

The RAM/ROM population, firmware supplied and decoder PALs determine the ultimate configuration of the SBC53. These options are designed to make application software development as quick and easy as possible while offering the lowest hardware cost.

CMOS STD Bus - The MCM prefix on the SBC53 card designates a standard STD Bus board. The LPM prefix designates a CMOS STD Bus board. A LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS and regular NMOS/TTL logic. The difference between these two products are the power requirements and operational temperature ranges.

The all CMOS LPM version is ideal for high performance applications requiring low cost, low power, small size, extended temperature operation and high reliability.

SBC53 Configuration - This board is offered both as the LPM/MCM-SBC53 and LPM/MCM-SBC53SX. The LPM/MCM-SBC53SX differs since the onboard memory and SBX data path is 8-bits. This permits 4 different device types (RAM, EPROM, PEROM "Flash", PSRAM, and EEPROMs) to be installed in each socket rather than in pairs for maximum flexibility and lowest cost for a memory intensive system.

FUNCTIONAL CAPABILITY

NEC V53 Processor - The LPM/MCM-SBC53 uses the high-performance 16-bit V53 processor. The 16 MHz V53 surpasses the 80286 and 80386SX CPUs with the Landmark, Norton SI, and Dhrystone Benchmarks. The combination of the CPU and peripheral mix makes it ideal for high-bandwidth data control applications. It will execute standard 80X86/V20/V30 source code and will support DOS and ROM-DOS for PC compatible applications.

Performance Comparison of NEC V53 CPU

CPU/speed	Norton SI	Landmark	Dhrystone/sec
V53-16	21	21	5800
80286-16	19	20	4800
80386-16	17	15	4100

The V53 contains hardwired data path control and no microcode which greatly increases the instruction execution speed. Bus cycles are nominally 2 clock cycles long. The V53 is four times faster than the 10 MHz V30 (8086) and up to 20% faster than the 80286. The main difference between the 80286 and the V53 is that the V53 does not support protected address mode. The V53 can support LIM 4.0 for direct memory addressing to 16 megabytes (MB).

The instruction set is upward compatible with the native modes of the 8088, 8086, V40 and V50. It includes added enhanced and unique instructions for bit processing, bit field insertion and extraction, and BCD string arithmetic to increase software performance. The processor is available at 10 or 16 MHz.

80287 Coprocessor - The LPM/MCM-SBC53 card has a socket to accept an optional 80C287 coprocessor providing greatly improved performance over the CPU alone. It provides arithmetic, logarithmic, exponential, trigonometric, and floating point arithmetic with up to 80-bit results.

Addressing - The I/O address space is 64K bytes. The full 16-bit address is used to map on-chip peripherals and the 10 least significant bits (A0-A9) are available for decoding by the on-board peripherals, SBX connector, and on the STD Bus backplane for I/O cards. IOEXP* is driven active low in a certain address range to prevent redundant decoding from older STD Bus I/O cards.

The normal memory address space is 1 Mbyte (20-bit address). The expanded address space is 16 Mbytes (24-bit address) by using an on-chip address translation table.

I/O ports are specified by a 16-bit address by the V53 for a total system capacity of 64K ports. The V53 CPU permits the internal peripheral addresses to be re-located within the memory map by writing to the internal peripheral relocation register. The other off-chip peripherals (16C452, Watchdog Timer, and Status LED) are mapped by a PLA to fixed locations.

Memory - Four standard 32-pin bytewide sockets are provided to allow the use of RAM, ROM, EPROM or EEPROMs. Both 32- and 28-pin devices are supported. On board data transfer uses a 16-bit data path for the LPM/MCM-SBC53.

The sockets on the LPM/MCM-SBC53 are configured in pairs. The first pair support EPROMs and PEROM (Flash) devices from 32K to 512K bytes. The second pair are organized to support Static or Pseudo Static RAMs of 32K, 128K or 512 Kbytes. The LPM/MCM-SBC53SX sockets are configured individually and support 8-bit data transfers.

The board supports the 5 volt only ATMEL style PEROMs (Flash) which may be programmed on board under software control to eliminate the need for external EPROM programmers.

Two of the sockets are configured to support battery backed static RAMs. The standby voltage source can be the optional onboard battery or VBAT, pin 5, from the STD Bus.

Direct Memory Access - Four DMA channels are available on the V53 chip to perform high speed data transfers between memory and I/O devices in bytes or

words. It can be programmed in either the single, block, or demand mode.

DRAM Refresh - The MCM-SBC53 generates the REFRESH* signal and refresh addresses up to 512 rows. The REFRESH* signal is wired to the onboard RAM memory sockets to permit the use of low cost pseudo-static RAMs for cost sensitive designs.

WAIT State Generation - A Wait Control Unit can be programmed to insert wait states of up to seven clocks during a bus cycle to compensate for the access speeds of slower memory or I/O devices.

Serial I/O - A double buffered, full-duplex, asynchronous, serial channel is implemented using the 16C452 Dual Asynchronous Communications Element. This device is a dual 8250A that offers software compatibility with PC type driver programs. Independent control of transmit, receive, line status and data set interrupts are on both channels. The unit contains two independent on-chip software programmable baud rate generator selectable through 38.4K bits per second.

Both channels have RS-232 and RS-485 interface levels and channel 2 also supports RS-422. Only +5Vdc is required since the plus and minus RS-232 voltage is generated by the MAX239 interface chip.

Channels 1 and 2 are wired to a 10-pin header which support the AT type DB9 connector when the CBL-123-1 adapter cable is used.

Channel 1 and 2 Pin-Out

Pin	FLOW	Signal
1	IN	Data Carrier Detect (DCD)
2	IN	Receive Data (RxD)
3	OUT	Transmit Data (TxD)
4	OUT	Data Terminal Ready (DTR)
5	--	Signal Ground (GND)
6	IN	Data Set Ready (DSR)
7	OUT	Request To Send (RTS)
8	IN	Clear To Send (CTS)
9	IN	Ring Indicator (RI)

An 8251A type serial port (V53-SCU) is also provided that can be used as either a debugging port or third serial channel. TxD, RxD, and ground are wired to a 10-pin header. The data rate will run up to 38.4Kbaud. The electrical interface levels are 0 to +5V (TTL compatible) with input clamping so that it will work directly with equipment using RS-232 signals separated by short cable distances.

The MCM-SBC53 serial ports will work with 5-, 6-, 7- or 8-bit character lengths. They will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Automatic error detection is provided for parity, overrun, and framing. Even, odd, or no parity bit generation and detection is provided. Each serial channel is fully interrupt driven.

Parallel I/O - The 16C452 also contains a parallel I/O port. It is wired and has the drive capability of a Centronics parallel I/O port mapped at LPT1 (378-37F hex). It can also be used as two general purpose I/O ports if a printer is not required. The first port is configured as 8 input or output only lines. The other port is configured as 5 input and 4 output lines.

P2 Pin out - Printer Channel

Pin	FLOW	Signal
1	IN	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper End
13	IN	Select
14	IN	Auto Error
15	I/O	Error
16	IN	Init. Printer
17	IN	Select Input
18-25		Ground

Counter/Timers - There are three independent, software programmable, 16-bit counter/timers available through an 8254A type device internal to the V53 CPU.

Interrupts - The MCM-SBC53 supports non-maskable interrupts (NMIRQ*), 8 maskable interrupts, and software exceptions (traps). Interrupt vectors are determined automatically for exceptions and the NMIRQ* or supplied by hardware for maskable interrupts.

An on-board master 8259A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems.

Vectored interrupts can be generated from the 3 serial channels, LPT, real time clock, counter/timer output, SBX connector, or four inputs from the STD Bus backplane. The interrupt sources are jumper selectable by the user.

For systems with multiple slave 8259A PIC's, additional logic is included to provide the cascade STD-8088 interrupt priority scheme. It is implemented by supplying the slave cascade address on the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. This permits a single peripheral card to generate an interrupt and receive its cascade response totally on the STD Bus backplane.

SBX Multimodule Connector - A single 8/16-bit SBX multimodule connector is provided to accommodate single-wide, 36-pin (8-bit) or 44-pin (16-bit) I/O expansion modules. This provides an alternative method for I/O expansion to the STD Bus offering the possibility of using just the LPM/MCM-SBC53 as a single board solution. SBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, networking, graphics controllers, and other special purpose peripheral functions.

The LPM/MCM-SBC53 decodes I/O addresses and generates the chip selects for the SBX boards. DMA and interrupt operations are supported by the V53. The LPM/MCM-SBC53SX only supports the 8-bit SBX connector.

Real Time Clock - A National DP8572A clock calendar is included that keeps track of seconds, minutes, hours, days of week, date, month, and years. It can operate in either a 12/24 hour format and Leap Year timing is automatic. It can generate a software selectable periodic, alarm/compare, or power fail interrupts. It can be battery powered by either the VBAT line of the STD Bus or by an optional battery attached to the board.

Up to 44 bytes of CMOS RAM are available for data storage in the DP8572A. These bytes are used for set-up tables by the LPM/MCM-SBC53PC board.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Status LED - A status LED is available on the board to monitor system activity. Under program control, it can indicate error conditions or blink different patterns to provide a visual indication of program status.

Battery Back-up - An optional 125 mAH battery can be supplied with the MCM-SBC53 board to provide power for the RAM memory sockets. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the RAM's selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and back OFF again when Vcc returns to normal.

Reset - A precision voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

Power Conservation - The V53 has three modes of power reduction for use in portable or other low power applications: Scalable system clock, HALT, and STOP. By reducing the system clock frequency, power use can be significantly decreased in direct proportion. The V53 system clock frequency can be dynamically adjusted by software to lower power consumption. The HALT mode further reduces power by putting the CPU in a standby mode. The STOP mode provides the maximum power reduction by turning the oscillator off. NMIRQ*, PBRESET*, an unmasked interrupt, or SYSRESET* will wake up the processor.

STD Bus - The STD Bus 16-bit bus systems architecture is quite similar in power and functionality to the AT bus, yet designed specifically for the rigors of industrial applications. Unlike other bus types, the STD Bus is specifically designed for process control and industrial applications.

The small size of the STD Bus cards, 4.5″ x 6.5″, make it ideal for use in disguised and embedded industrial controller applications. The small format is designed for industrial environments since the cards don't bend or flex and are engineered to stand shock and vibration. An STD Bus card is held in place by the STD Bus card cage on 3 sides and with an optional additional hold down bar across the card ejector on the top of the cards. This secure placement permits the STD Bus card to sustain violent vibrations without coming loose. The small format and the low cost of the STD Bus cards render their maintenance simple, quick, and economical.

SOFTWARE SUPPORT

C-THRU-ROM - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the MCM-SBC53. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM consists of a source level debugging user interface with target communication facility that resides on the LPM/MCM-SBC53. The target system kernel includes an execution control program and host communication facility. The user can debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a a non-DOS embedded system, and locate code and data anywhere in the 80X86/88 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM does not include Microsoft C, MASM, or Borland Turbo-C since it is assumed these PC based development tools are owned by the user. CTR-M-SBC53 is the Microsoft version and CTR-T-SBC53 is the Turbo C version of the C-THRU-ROM development package which includes the diskettes, RAM, target system kernel EPROM, serial I/O cable and documentation. If C-THRU-ROM is ordered at the same time as the LPM/MCM-SBC53A, the factory will integrate and test the system at no extra charge.

ROM-DOS - ROM-DOS is a MS-DOS 3.3 compatible ROM-based operating system for embedded MCM-SBC53 applications. ROM-DOS provides 3 major functions: hardware initialization, file support and standard software drivers. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services.

ROM-DOS reduces the ROM, RAM and hardware requirements while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational

media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS provides a DOS-level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that greatly simplifies data storage and retrieval. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur. All development can be done on a PC and debugged on the target system which completes the project in the shortest time.

MS-DOS - The LPM/MCM-SBC53PC is MS-DOS compatible with or without a disk. In harsh environments or at extended temperatures, it will work with a RAM/ROM disk with MS-DOS and the application program residing in ROM. Video and a standard keyboard are not required for operation either.

For program/application development, the LPM/MCM-SBC53PC coupled with the MCM/LPM-DSKIO supports floppy and hard disk drives and a keyboard. Video or flat panel display controllers are also available to form a complete STD Bus DOS system with AT class performance. The system can serve as a platform for initial development and debugging or be used as an rugged, industrial PC. Or later the extra components can be removed during run time if they are not needed or if they are not rugged enough for the application environment. The benefit is that all the familiar development tools on the IBM PC are available for use to expedite software development.

SPECIFICATIONS

Electrical
System Clock: 10MHz or 16MHz
Serial Interface: 3 Serial channels
Parallel: TTL compatible, Centronics compatible
MCM-SBC53-10: Vcc = +5V $\pm$ 5% @600 mA typ.
LPM-SBC53-10: Vcc = +5V $\pm$ 10% @300 mA typ.

Mechanical
Dimensions: 4.5″ x 6.5″

Environmental
Operating Temperature:
   LPM-SBC53:   -40° to +85°C
   MCM-SBC53:   0° to +65°C
Non-condensing relative humidity: 5% to 95%

WinSystems, Inc.

Connectors
Ch 1. Serial I/O: 10-pin, 0.100″ grid
Ch 2. Serial I/O: 10-pin, 0.100″ grid
Ch 3. Serial I/O: 10-pin, 0.100″ grid
Parallel I/O: 26-pin, 0.100″ grid
SBX I/O: 36/44-pin, 0.100″ dual row female

ORDERING INFORMATION

LPM-SBC53-10	10MHz CMOS V53 SBC
LPM-SBC53-16	16MHz CMOS V53 SBC
LPM-SBC53R-10	10MHz SBC53 with ROM-DOS
LPM-SBC53R-16	16MHz SBC53 with ROM-DOS
LPM-SBC53PC-10	10MHz SBC53 with PC-BIOS
LPM-SBC53PC-16	16MHz SBC53 with PC-BIOS
MCM-SBC53A-10	10MHz V53 SBC
MCM-SBC53A-16	16MHz V53 SBC
MCM-SBC53R-10	10MHz SBC53 with ROM-DOS
MCM-SBC53R-16	16MHz SBC53 with ROM-DOS
MCM-SBC53PC-10	10MHz SBC53 with PC-BIOS
MCM-SBC53PC-16	16MHz SBC53 with PC-BIOS
CTR-M-SBC53	Remote C Symbolic Debugger development kit for Microsoft C
CTR-T-SBC53	Remote C symbolic debugger development kit for Turbo C & C++

The LPM/MCM-SBC53SX differs from the LPM/MCM-SBC53 since both the onboard memory and SBX data path are 8-bits. This configuration offers maximum flexibility by permitting four different memory device types to be installed in each socket, rather than in pairs.

LPM-SBC53SX-10	10MHz CMOS V53SX SBC
LPM-SBC53SX-16	16MHz CMOS V53SX SBC
LPM-SBC53PX-10	10MHz SBC53SX with PC-BIOS
LPM-SBC53PX-16	16MHz SBC53SX with PC-BIOS
LPM-SBC53RX-10	10MHz SBC53SX with ROM-DOS
LPM-SBC53RX-16	16MHz SBC53SX with ROM-DOS
MCM-SBC53SX-10	10MHz V53SX SBC
MCM-SBC53SX-16	16MHz V53SX SBC
MCM-SBC53PX-10	10MHz SBC53SX with PC-BIOS
MCM-SBC53PX-16	16MHz SBC53SX with PC-BIOS
MCM-SBC53RX-10	10MHz SBC53SX with ROM-DOS
MCM-SBC53RX-16	16MHz SBC53SX with ROM-DOS
CTR-M-SBC53SX	Remote C Symbolic Debugger development kit for Microsoft C
CTR-T-SBC53SX	Remote C symbolic debugger development kit for Turbo C & C++

FEATURES

- 8 or 10 MHz V40 CMOS 16-bit processor
- Intelligent standalone I/O controller
- Memory mapped to the STD Bus
- Three 32-pin bytewide memory sockets support up to 1024KB of RAM, EPROM, and EEPROM
- 1 socket supports battery backed RAM operation
- Memory and I/O WAIT State generator on board
- Two 85C30 SCC serial sync/async I/O ports which support RS-232/485 interface levels
- One 82C51 RS-232 serial port (V40 SCU)
- 8 Channel Interrupt Controller (82C59A type)
- 24 I/O lines (82C55A parallel port)
- Three 16-bit Counter/Timers (V40)
- DMA to SCC and SBX supported
- Watchdog timer
- Precision power-on/brown out detect circuit
- Optional C-Thru-ROM C Source Debugger
- Operational temperature range: -40°C to +85°C
- +5 volt only operation
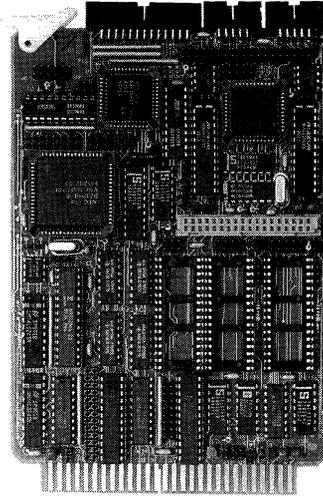
The LPM/MCM-SBC42 is an intelligent V40 based single board computer that operates as a memory mapped slave I/O processor on the STD Bus. It is designed to operate independently of the master STD Bus CPU to provide high speed independent parallel processing for processor intensive I/O. It can boot up and automatically load an application program from the master CPU. The LPM/MCM-SBC42 board is ideal for high speed communications, data manipulation, analog data acquisition, or other time critical functions. Coupled with the SBX-SCC dual serial I/O board, it can function as a 4-channel intelligent serial I/O board. A broad base of software tools support the card including a remote C source debugger and an

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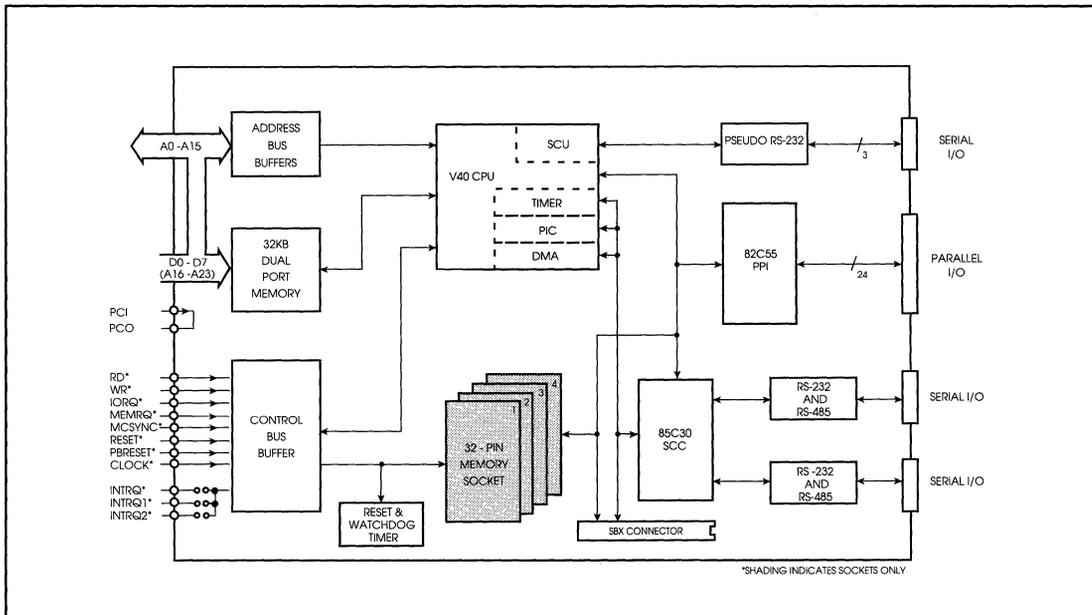
embedded operating system. It is ideal for high performance applications requiring low power, small size, extended temperature operation and high reliability.

FUNCTIONAL CAPABILITY

CMOS STD Bus - The LPM/MCM-SBC42 is designed with high speed, low power CMOS devices which offer a high degree of noise immunity, low power consumption, and a wide operational temperature range. The LPM-SBC42 is the CMOS STD Bus version and the MCM-SBC42 is the regular STD Bus version.

STD Bus Interface - The LPM/MCM-SBC42 can operate as an independent, stand-alone single board computer, or as a slave I/O control processor. It appears as a 32KByte dual ported RAM on the STD Bus to provide the maximum interface flexibility and data transfer speed. The memory is located on the LPM/MCM-SBC42 and is mapped into the main master systems address space. Multiple LPM/MCM-SBC42 boards can be supported by the master system and mapped into the same location to conserve system memory.
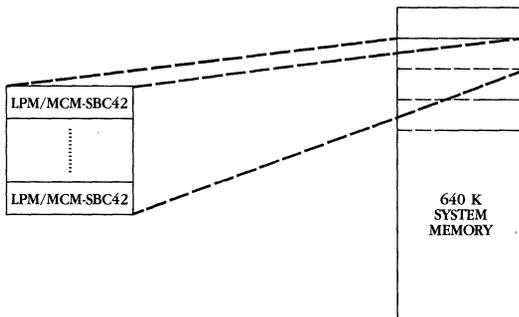
LPM/MCM-SBC42 Memory Mapping

Processor - The LPM/MCM-SBC42 incorporates the powerful 16-bit CMOS V40 processor which has a 20-bit direct memory address capability of 1 MByte. It is code compatible with the 8088 family of microprocessors. The V40 has 16-bit internal and 8-bit external data busses for enhanced execution speed. The processor is fully buffered and operates at either 8 or 10 MHz.

An NEC V40 processor is installed for improved performance over the 80188 plus it has the power/economy of CMOS. The V40 executes faster than the 80188 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high-speed multiplication/division instructions.

Direct Memory Access - A DMA controller is on the V40 CPU to transfer data from the SBX multi-module and both onboard SCC serial channels to the LPM/MCM-SBC42's memory for maximum performance.

Memory - Three JEDEC standard 32-pin bytewide sockets are provided to allow the use of RAM, ROM, EPROM or EEPROMs. The sockets are configurable for 32K, 64K, 128K and 512KByte devices for a total of 1024KB onboard. Either 28 or 32-pin memory devices can be plugged into the sockets.

DRAM Refresh - The V40 CPU generates a refresh signal which is wired to the onboard memory sockets to permit the use of low cost 128KB and 512KB psuedo-static RAMs for cost sensitive designs.

WAIT State Generation - A Wait Control Unit can be programmed to insert wait states of up to three clocks during a bus cycle to compensate for the access speeds of slower memory or I/O devices.

Serial Communications - A total of 3 serial channels are provided. Two double buffered, full-duplex, asynchronous or synchronous serial channels are implemented using the 85C30 SCC. Independent control of transmit, receive, line status and data set interrupts, and modem control signals are on each channel. The unit contains two independent on-chip software programmable baud rate generator selectable for data rates up to 56 Kbps. Each serial channel is fully interrupt driven.

Jumpers options permit configuration of the serial I/O as either DCE or DTE. Both RS-232 and two wire RS-485 interface levels are supported. The RS-232 devices require only +5 volts since the plus and minus voltages are generated on-chip by the interface buffer.

SCU Channel 3 - A double buffered, full-duplex, serial asynchronous channel is implemented inside the V40 CPU with a 82C51 type programmable communication interface to provide the third serial channel. The V40 contains an independent on-chip software programmable baud rate generator selectable through 38.4K bits per second. This port can be used as a debugging tool with C-Thru-ROM and ROM-DOS or as a general purpose asynchronous serial I/O channel.

Counter/Timers - There are three independent, software programmable, 16-bit counter/timers available through an 82C54A type device internal to the V40.

Parallel I/O - The LPM/MCM-SBC42 also contains 24 parallel I/O lines provided through a 82C55A PPI. It supports 24 I/O pins which may be individually programmed in 2 groups of 12 in three major modes of operation. In the first mode, Mode 0, each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking, and interrupt control signals. The third mode, (Mode 2), is a bidirectional bus mode which used 8 lines for a bidirectional bus, borrowing one from the other group for handshaking.

There is also a direct bit set/reset capability for control application interface requirements. The 82C55A has sufficient drive capability to interface directly with Opto-22 type modules and panels. Also one port can be configured for a Centronics type interface.

The signal levels are TTL compatible. The 24 lines are connected to a 26-pin connector. Pins 25 and 26 are wired to +5 volts and ground respectively in order to provide easy and convenient connection to display interfaces, keypads, or other devices that require power.

Interrupts - The LPM/MCM-SBC42 supports non-maskable interrupts (NMIRQ*), 8 maskable interrupts, and software exceptions. Interrupt vectors are determined automatically for software exceptions and for the NMIRQ*.

An onboard master 82C59A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the 3 serial channels, 3 counter/timer outputs, and the SBX connector. The interrupt sources are jumper selectable by the user and assigned unique vectors by the PIC.

Multimodule Interface - A single iSBX Multimodule connector is provided to accommodate a single wide, 36-pin (8-bit) I/O expansion module. Both interrupts and DMA are supported.

SBX modules are available for implementing counter/timer functions, serial I/O, parallel I/O, disk controllers, A/D, D/A and other special purpose controllers. This connector permits the customizing of the LPM/MCM-SBC42 to meet special applications such as an intelligent serial controller, intelligent analog controller, special purpose SCSI adapter, etc.

Status LED - A status LED is available on the board to monitor system activity. Under program control, it can indicate error conditions or blink different patterns to provide a visual indication of program status.

Real Time Clock - The LPM/MCM-SBC42 can be optionally populated with a Dallas Semiconductor SmartWatch.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a 50 mS PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Battery Back-up - An optional 160 mAH battery can be supplied with the LPM/MCM-SBC42 board to provide power for one of the RAM memory sockets. The LPM/MCM-SBC42 has special circuitry to support both the low power 32K and 128K byte RAM's. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the RAM socket selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and back OFF again when Vcc returns to normal.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important because it detects brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

SOFTWARE SUPPORT

Firmware Support Package (FSP) - The LPM/MCM-SBC42 can contain an optional boot EPROM that provides start up and program loading from the master CPU. This means that the LPM/MCM-SBC42's application program can be stored and/or changed by the master system without removing the LPM/MCM-SBC42 and changing EPROMs.

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C-THRU-ROM-SBC42 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the LPM/MCM-SBC42. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems' target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X86/88 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM requires Microsoft C version 5.0 and above and Borland Turbo C. Microsoft MASM is supported.

SBC42 Firmware Support Package (FSP) - The board can be ordered with an optional firmware support package called the LPM/MCM-SBC42F. The firmware includes functions to access the board through the dual port RAM by another master STD Bus CPU. The functions include reading and writing, memory and I/O, loading and starting programs and manipulation of the serial channels on the board. This firmware has been written to allow the LPM/MCM-SBC42F with a SBX-SCC to act as a smart serial controller by supporting up to 4 SCC serial channels under interrupt control.

Also, the FSP-SBC42 package is recommended for initial program development. It includes a 128KB static RAM, two SCC serial cables, and a diskette. The disk includes sample program in both executable (for WinSystems' STD-AT DOS systems) and C source code for use as both a utility program and as an example of interaction with the firm support ROM.

SPECIFICATIONS

Electrical
System Clock: 8.0 or 10 MHz
Serial Interface: RS-232/485 on channels 1 and 2
            pseudo RS-232 on channel 3
Parallel: 5 74LS TTL loads
Vcc = +5V $\pm$ 10% at TBD mA typ. (LPM-SBC42)
        +5V $\pm$ 5% at TBD mA typ. (MCM-SBC42)
    Without RS-422/485 Drivers
Vcc = +5V $\pm$ 10% at TBD mA typ. (LPM-SBC42)
        +5V $\pm$ 5% at TBD mA typ. (MCM-SBC42)

Memory
Addressing: 1 Megabyte onboard
Capacity: Supports 32K, 64K, 128K and 512KByte
32-pin RAM, ROM, EPROM, and EEPROMs.

Mechanical
Dimensions: Meets STD Bus mechanical specifications:
        4.5" x 6.5"

Connectors
Serial I/O:	10-pin 0.100" grid
Serial I/O:	10-pin 0.100" grid
Parallel I/O:	26-pin 0.100" grid
SCU I/O:	10-pin 0.100" grid
SBX Multimodule:	36-pin, 0.100" dual row

Environmental
Operating Temperature: -40° to +85°C (LPM-SBC42)
                0°C to +65°C (MCM-SBC42)
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC42-8	8 MHz CMOS STD Bus Slave I/O Board
LPM-SBC42-8-BAT	LPM-SBC42-8 with battery
LPM-SBC42F-8	LPM-SBC42-8 with firmware
LPM-SBC42-10	10 MHz CMOS STD Bus Slave I/O Board
LPM-SBC42-10-BAT	LPM-SBC42-10 with battery
MCM-SBC42-8	8 MHz STD Bus Slave I/O Board
MCM-SBC42-8-BAT	MCM-SBC42-8 with battery
MCM-SBC42F-8	MCM-SBC42-8 with firmware
MCM-SBC42-10	10 MHz STD Bus Slave I/O Board
MCM-SBC42-10-BAT	MCM-SBC42-10 with battery
CTR-M-SBC42	CTR for MicroSoft C on the LPM/MCM-SBC42
CTR-T-SBC42	CTR for Turbo C on the LPM/MCM-SBC42
FSP-SBC42-8	Firmware Support package for the 8MHz LPM/MCM-SBC42F

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FEATURES

- Low Cost V40 16-bit (8088) SBC
- Three 32-pin bytewide memory sockets support up to 1024KB of RAM, EPROM, and EEPROM
- 2 of the 3 memory sockets support optional battery backed RAM operation
- Memory and I/O WAIT State generator
- Two 8250A serial I/O ports both with RS-232 and one with RS-485 levels
- One 8251 serial port (V40 SCU)
- 8 Channel Interrupt Controller (8259A type)
- 16 I/O lines configured as Centronics parallel port with 6 additional input and 2 output lines
- Three 16-bit Counter/Timer channels (8254A)
- Watchdog timer
- Activity status LED
- Precision power-on/brown out detect circuit
- 8080 Software emulation mode
- ROM-DOS and C-THRU-ROM software support
- Available for CMOS STD Bus: LPM-SBC41
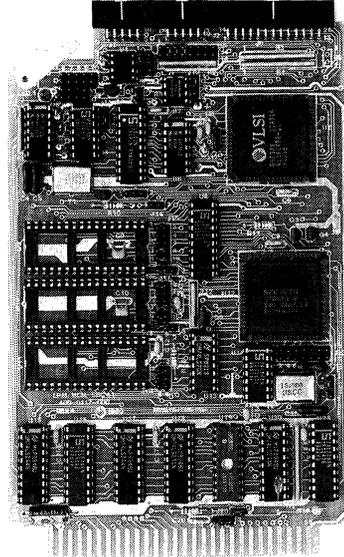
The LPM/MCM-SBC41 is a low cost V40 based single board computer on the STD Bus combining the CPU, 3 memory sockets, 3 serial I/O channels, 3 counter/timers, 8 channel interrupt controller, and parallel I/O on a single card. Furthermore a precision power-fail reset circuit, activity LED, and watchdog timer are incorporated on this card making it ideal for high-performance applications requiring low cost, low power, small size and high reliability.

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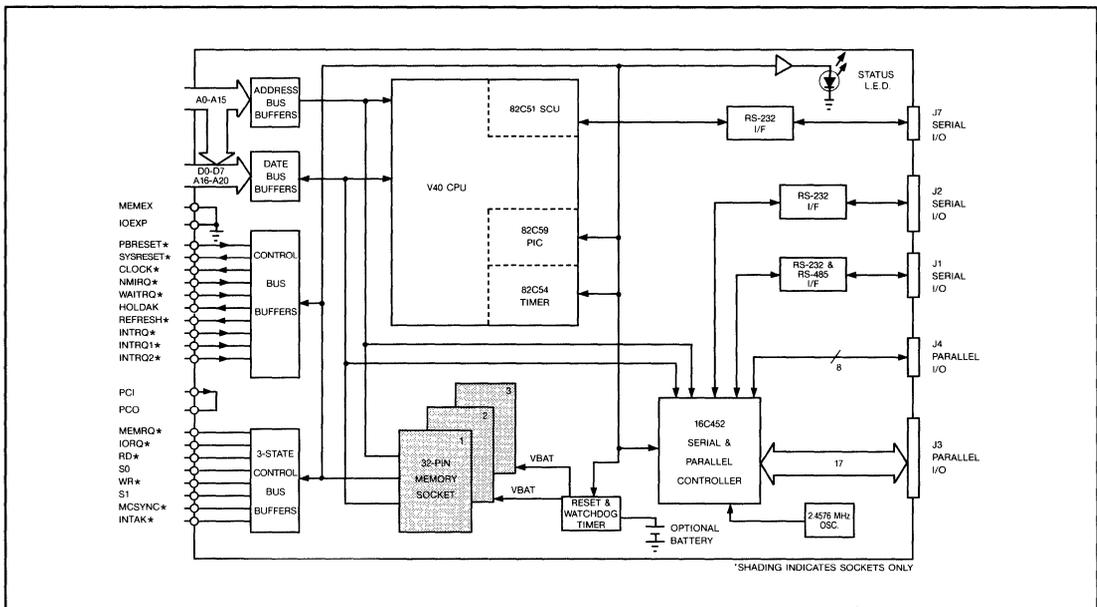
FUNCTIONAL CAPABILITY

Processor - The LPM/MCM-SBC41 incorporates the powerful 16-bit V40 processor which has a 20-bit direct memory address capability of 1 MByte. It is code compatible with the 8088 CPU. The V40 has 16-bit internal and 8-bit external data busses for enhanced execution speed. It runs all the 8088 instructions plus enhanced and unique instructions for bit manipulation, high speed block transfers, and engineering control applications. The processor is fully buffered and operates at 8 or 10MHz.

A NEC V40 processor is installed for improved performance over the 80188 plus it has the power/economy of CMOS. The reason the V40 executes faster than the 80188 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8- and 16-bit signed and un-signed arithmetic in binary and BCD including high-speed multiplication/division instructions.

The V40 chip will also operate in the 8080 emulation mode. In this mode, the 8080 instruction set is emulated by the V40 allowing migration of previously developed 8-bit software to this board.

SLEEP Mode - The NEC V40 has a low power standby mode to reduce power consumption. The standby mode is available in both the native V40 and 8080 emulation mode and is entered automatically when a HALT condition is detected. The processor stops in a known condition with only the internal oscillator and standby release circuits operational. The mode is released by detection of a SYSRESET*, INTRQ* or NMIRQ*.

Addressing - The V40 processor supports direct addressing of 1 MByte using 20-bit memory address-ing. MEMEX* is wired to ground.

I/O ports are specified by a 16-bit address by the V40 for a total system capacity of 64K ports. The V40 CPU permits the internal peripheral addresses to be relocated within the memory map by writing to the internal peripheral relocation register. The other off-chip peripherals (16C452, Watchdog Timer, and Status LED) are mapped by a PLA to fixed locations. IOEXP* is wired to ground.

Memory - Three JEDEC standard 32-pin bytewide sockets are provided to allow the use of RAM, ROM, EPROM or EEPROMs. For a total of 1024KB onboard. Either 28- or 32-pin memory devices can be plugged into the sockets.

Socket 1 accepts up to a 512K EPROM. Socket 2 is configured for 32K, 64K and 128K static and pseudo-

static RAMs, EPROMs or EEPROMs. Socket 3 accepts up to a 512K static or pseudo-static RAM.

Two of the sockets are configured to support the REFRESH* signal required for psuedo-static RAM devices. These sockets also support 32KB or 128KB battery backed static RAMs. The standby voltage source can be the optional onboard battery.

DRAM Refresh - The V40 generates the REFRESH* signal and refresh addresses up to 512 rows. The REFRESH* signal is wired to two of the onboard memory sockets to permit the use of low cost pseudo-static RAMs for cost sensitive designs. REFRESH* can be optionally jumpered to the STD Bus. The interval can be programmed to accommodate the require-ments of various types of memories.

WAIT State Generation - A Wait Control Unit can be programmed to insert wait states of up to three clocks during a bus cycle to compensate for the access speeds of slower memory or I/O devices.

Serial Communications - A double buffered, full-duplex, serial asynchronous channel is implemented using the 16C452 Dual Asynchronous Communica-tions Element. This device is a dual 8250A that offers software compatibility with PC-type driver programs. They are mapped at COM1 and COM2 (3F8-3FF and 2F8-2FF hex) respectively. Independent control of transmit, receive, line status and data set interrupts are on both channels. The unit contains two independent on-chip software programmable baud rate generator selectable through 38.4K bits per second.

The V40 CPU also contains a 8251A type serial port (SCU) that is useful as either a debugging port or third serial channel.

The LPM/MCM-SBC41 will work with 5-, 6-, 7- or 8-bit character lengths. It will handle 1, or 2 stop bits; false start bit detection, and automatic break detection and handling. Automatic error detection is provided for parity, overrun, and framing. Even, odd, or no parity bit generation and detection is provided. Each serial channel is fully interrupt driven.

RS-232 interface levels are supported on all channels and RS-485 is jumper selectable on channel 1 only. A 100 ohm termination resistor is installed across the RS-485 data lines.

Counter/Timers - There are three independent, software programmable, 16-bit counter/timers availa-ble through an 8254A type device internal to the V40 CPU to solve most of the timing problems in micro-computer systems design. The individual counter channels can be cascaded for longer count sequences. Counting can be done in either BCD or binary.

Channel 0 is reserved for internal timing. Channel 1 is selectable as a general timer or baud rate generator for the SCU. Channel 2 is a general purpose timer. The TCLK, TOUT2, and TCTL2 control lines are available at connector J7 for customer use.

Parallel I/O - The 16C452 contains a parallel I/O port. It is wired and has the drive capability of a Centronics parallel I/O port mapped at LPT1 (378-37F hex). It can also be used as a two general purpose I/O ports if a printer is not required. The first port is configured as 8 input or output only lines. The other port is configured as 5 input and 4 output lines.

For additional parallel I/O capability, the DTR, DSR, RLSD, and RI status lines from both serial channels are available for use as general purpose TTL level, parallel I/O lines through connector J4. This provides 6 input and 2 output lines.

Interrupts - The LPM/MCM-SBC41 supports non-maskable interrupts (NMIRQ*), maskable interrupts, and software exceptions. The six software exceptions supported are: Divide error, Array bound overflow, Break on overflow, Break, Single Step, and Mode Switch (for 8080 emulation). Interrupt vectors are determined automatically for exceptions and the NMIRQ* or supplied by hardware for maskable interrupts.

An onboard master 8259A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the 3 serial channels, parallel I/O channel, 3 counter/timer outputs, or the STD Bus backplane signals INTRQ*, INTRQ*1, and INTRQ*2. The interrupt sources are jumpered selectable by the user and assigned unique vectors by the PIC.

For systems with multiple slave 8259A PIC's, additional logic is included to provide the cascade STD-8088 interrupt priority scheme. It is implemented by supplying the slave cascade address on the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. This permits a single peripheral card to generate an interrupt and receive its cascade response totally on the STD Bus backplane.

Status LED - A status LED is available on the board to monitor system activity. Under program control, it can indicate error conditions or blink different patterns to provide a visual indication of program status.

Real Time Clock - The LPM/MCM-SBC41 can be optionally populated with a Dallas Semiconductor Smart Watch. It is a 32-pin DIP socket with a built-in CMOS watch, power sequencer, and an embedded lithium energy source. Since the battery is internal to the socket, there is no danger of shorting out or accidental discharge due to mishandling.

The SmartWatch plugs into one of the onboard memory sockets. It permits either 28- or 32-pin bytewide memory devices to be plugged into its socket. This permits full utilization of all the LPM/MCM-SBC41's memory sockets while having a transparent battery backed timekeeping function.

The SmartWatch provides time keeping information including hundredths, tenths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. It operates in either 24-hour or 12 hour format with an AM/PM indicator.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a RESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Battery Back-up - An optional 170 mAH battery can be supplied with the LPM/MCM-SBC41 board to provide power for up to 2 RAM memory sockets. The LPM/MCM-SBC41 has special circuitry to support both the low power 32K and 128KByte RAMs. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the RAM's selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and back OFF again when Vcc returns to normal.

Reset - A precision voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a RESET* is generated. This action is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

4

SOFTWARE SUPPORT

C-THRU-ROM-SBC41 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the LPM/MCM-SBC41. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X86/88 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

ROM-DOS - ROM-DOS is a MS-DOS 3.3 compatible ROM based operating system for embedded applications. ROM-DOS reduces the ROM, RAM and hardware requirements while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function. This operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied.

CMOS STD Bus - The LPM-SBC41 is the CMOS STD Bus version and the MCM-SBC41 is the standard STD Bus version of the low cost V40 SBC.

SPECIFICATIONS

Electrical
Bus Interface: STD Bus compatible.
System Clock: 8.0 or 10 MHz
Serial Interface: 3 Serial channels with RS-232 on channels 1 and 2 and RS-485 on channel 1 only. Channel 3 is inverted TTL configured to work directly with RS-232.

Vcc = +5V $\pm$5% @125 mA typ. (LPM-SBC41)
$\pm$12V $\pm$10% @5 mA typ. (LPM-SBC41)
+5V $\pm$5% @525 mA typ. (MCM-SBC41)
$\pm$12V $\pm$10% @30 mA typ. (MCM-SBC41)

Memory
Addressing: 1 Megabyte

Mechanical
Dimensions: 4.5 x 7.0

Connectors
J1, Serial I/O: 10-pin, 0.100" grid
J2, Serial I/O: 14-pin, 0.100" grid
J3, Parallel I/O: 26-pin, 0.100" grid
J4, Parallel I/O: 16-pin, 0.100" grid

Environmental
Operating Temperature: -40°C to +85°C (LPM-SBC41)
0°C to +65°C (MCM-SBC41)
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC41-8	CMOS Low Cost 8MHz V40 SBC
LPM-SBC41-8-BAT	SBC41-8 with battery
LPM-SBC41R-8	SBC41-8 with ROM-DOS installed
LPM-SBC41R-8-BAT	SBC41R-8 with battery
LPM-SBC41-10	CMOS Low Cost 10MHz V40 SBC
LPM-SBC41-10-BAT	SBC41-10 with battery
LPM-SBC41R-10	SBC41-10 with ROM-DOS installed
LPM-SBC41R-10-BAT	SBC41R-10 with battery
LPM-SBC41XT-10-512	SBC41XT with 512KB of memory
LPM-SBC41XT-10-640	SBC41XT with 640KB of memory
MCM-SBC41-8	Low Cost 8MHz V40 SBC.
MCM-SBC41-8-BAT	SBC41-8 with battery
MCM-SBC41R-8	SBC41-8 with ROM-DOS installed
MCM-SBC41R-8-BAT	SBC41R-8 with battery
MCM-SBC41-10	Low Cost 10MHz V40 SBC.
MCM-SBC41-10-BAT	SBC41-10 with battery
MCM-SBC41R-10	SBC41-10 with ROM-DOS installed
MCM-SBC41R-10-BAT	SBC41R-10 with battery
MCM-SBC41XT-10-512	SBC41XT with 512KB of memory
MCM-SBC41XT-10-640	SBC41XT with 640KB of memory
CTR-M-SBC41-8	Remote C Symbolic Debugger development kit for Microsoft C
CTR-T-SBC41-8	Remote C Symbolic Debugger development kit for Turbo C & C + +
CTR-M-SBC41-10	Remote C Symbolic Debugger development kit for Microsoft C
CTR-T-SBC41-10	Remote C Symbolic Debugger development kit for Turbo C & C + +

WinSystems, Inc.

WinSystems®

CMOS STD BUS

LPM-SBC40A
LPM-SBC40R
LPM-SBC40XT

FEATURES

- V40 (integrated 80C88) CMOS 16-bit processor
- Standalone or DOS compatible Single Board Computer
- PC-XT compatible (LPM-SBC40XT)
- Direct Addressing to 1 Mbyte
- Onboard DMA
- Four 32-pin bytewide memory sockets supports RAM, EPROM, psuedo-static RAM and EEPROM
- 3 memory sockets support battery backed RAM
- Memory and I/O WAIT State generator
- Two 82C51 type Serial I/O ports both with RS-232 and one with RS-422/485 levels
- Programmable Interrupt Controller (82C59A type)
- 24 parallel I/O lines (82C55)
- Three 16-bit Counter/Timer channels (82C54 type)
- 24 hour battery backed Calendar clock
- Flexible I/O mapping
- iSBX Multimodule connector
- Watchdog timer
- Precision power-on/brown out detect circuit
- LED Status monitor
- SLEEP mode for very low power operation
- 8080 Software emulation mode
- Optional symbolic firmware debugger
- Optional ROM-DOS Embedded Operating System
- +5V only operation
- Extended temperature operation: -40° to +85°C
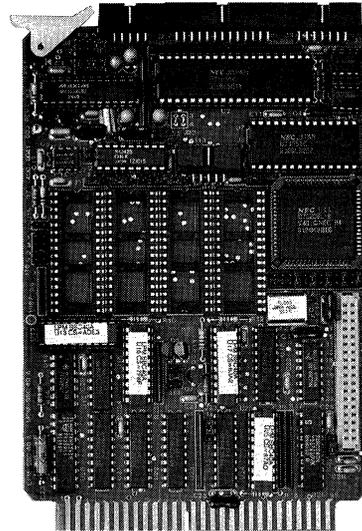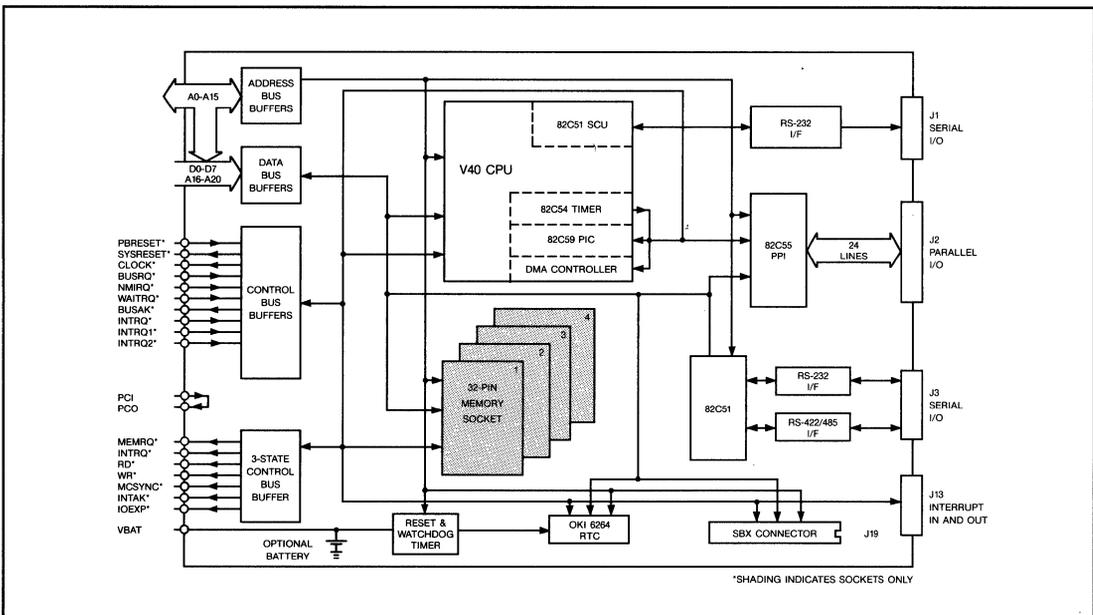
The LPM-SBC40A is a very versatile, V40 based (highly integrated 80C88 equivalent) CMOS Single Board Computer (SBC) on the CMOS STD Bus. The LPM-SBC40A contains the CPU, 4 memory sockets, 2 serial I/O channels, counter/timers, interrupt controller, DMA controller, clock calendar, parallel I/O and STD Bus interface on a single card. Furthermore a precision powerfail reset circuit, watchdog timer, and SBX multimodule connector are incorporated on the all CMOS card making it ideal for high performance embedded applications requiring low power, small size, extended temperature operation. It is designed for users requiring a standalone SBC with no operating system onboard.

For other applications with file management or other operating system environment structures, WinSystems offers two additional versions of this board. The LPM-SBC40R is the SBC40A with the ROM-DOS Embedded Operating System installed. The LPM-SBC40XT is the SBC40A configured as a PC-XT running MS-DOS version 3.3 including memory and a keyboard interface. The RAM/EPROM population option, firmware supplied and decoder PALs determine the ultimate configuration of the SBC40A. These options are designed to make application software development as quick and easy as possible.

FUNCTIONAL CAPABILITY

Processor - The LPM-SBC40A incorporates the powerful 16-bit V40 processor which has a 20-bit direct memory address capability of 1 Mbyte. It is code compatible with the 8088 CPU. The V40 has 16-bit internal and 8-bit external data busses for enhanced execution speed. It runs all the 80C88 instructions plus enhanced and unique instructions for bit manipulation, high speed block transfers, and engineering control applications. The processor is fully buffered and operates at either 5, 8 or 10 MHz.

An NEC V40 processor is installed for improved performance over the 80188 plus the power/economy of CMOS. The V40 executes faster than the 80188 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high-speed multiplication/division instructions.

The V40 will also operate in the 8080 emulation mode. In this mode, the 8080 instruction set is emulated by the V40, allowing migration of previously developed 8-bit software to this board.

SLEEP Mode - The NEC V40 has a low power standby mode to reduce power consumption. The standby mode is available in both the native V40 and 8080 emulation mode and is entered automatically when a HALT condition is detected. The processor stops in a known condition with only the internal oscillator and standby release circuits operational. The mode is released by detection of a SYSRESET*, INTRQ* or NMIRQ*.

Addressing - The V40 processor supports direct addressing of 1 Mbyte on 20 address lines. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data lines D0 through D3 at the beginning of each memory operation. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. The multiplexing of the extra address lines on the data bus requires no additional CPU overhead and is transparent and compatible to other I/O mapped cards. MEMEX* is wired to ground.

Memory - Four JEDEC standard 32-pin bytewide sockets are provided to allow the use of static RAM, pseudo-static RAM, ROM, EPROM or EEPROMs. The sockets are configurable for 8K, 16K, 32K, 64K, and 128Kbyte devices for a total of 512KB onboard. Either 28 or 32-pin memory devices can be plugged into the sockets. Eight standard memory maps are jumper selectable. Five maps are preprogrammed and 3 are user programmable for custom decoding by the user. The LPM-SBC40A is supplied with no memory installed.

The LPM-SBC40XT board is configured with a PC-XT compatible BIOS in EPROM and up to 384KB of pseudo-static RAM installed in the other 3 sockets. This board will attempt to boot DOS from a floppy disk, hard disk or RAM/ROM disk upon power up. The LPM-SBC40R has the ROM-DOS EPROM installed in the first socket and no other memory.

Direct Memory Access - A DMA channel is available from the V40 CPU to the SBX socket to perform high speed data transfers between memory and I/O devices in bytes or words. It can be programmed in either the single, block, or demand mode.

DRAM Refresh - The V40 generates the REFRESH* signal and refresh addresses up to 512 rows. The interval can programmed to accommodate the requirements of dynamic and pseudo-static memories.

A pseudo-static RAM incorporates features and benefits from both DRAMs and SRAMs. It is similar to

a DRAM since it needs a 4 mS refresh; however, it will fit into a standard 28 or 32-pin bytewide memory socket and access just like a SRAM. This means that a standard bytewide socket accepts a lower cost, high density, high speed RAM offering more memory flexibility to the board.

WAIT State Generation - A Wait Control Unit can be programmed to insert wait states of up to three clocks during a bus cycle to compensate for the access speeds of slower memory or I/O devices.

Serial Communications - A double buffered, full-duplex, serial asynchronous channel is implemented inside the V40 CPU with a 82C51 type programmable communication interface. The V40 contains an independent on-chip software programmable baud rate generator selectable through 38.4K bits per second. A second 82C51 device is onboard to provide the other serial channel.

The card will work with 7 or 8-bit character lengths. It will handle 1 or 2 stop bits; false start bit detection, and automatic break detection and handling. Automatic error detection is provided for parity, overrun, and framing. Each serial channel is fully interrupt driven.

Jumpers options permit configuration of the serial I/O as either DCE or DTE. Both RS-232 and RS-422/485 interface levels are supported on channel 1. Channel 2 supports RS-232 only. The RS232 devices require only +5 volts since the $\pm$ voltages are generated on-chip by a Maxim MAX238.

Channel 1 is configurable for RS-422/485 electrical interface levels. The RS-422 configuration provides separate transmit and receive signal pairs. For RS-485 multidrop lines, only one signal pair is used for "party line" network structures. The LPM-SBC40A is designed to properly disable the transmitter upon reset to prevent potential lock-up problems cause from a transmitter being stuck in the ON mode. Both the RS-422/485 transmitter and receiver have 100 ohm termination resistors installed onboard.

J1 Pinout - V40 SCU Serial Channel

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J3 Pinout - 82C51A Serial Channel

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	No connection
7	Ground
14	RS-422/485 Transmit Data +
15	RS-422/485 Transmit Data -
16	RS-422/485 Receive Data +
17	RS-422/485 Receive Data -

Counter/Timers - There are three independent, software programmable, 16-bit counter/timers available through an 82C54 type device internal to the V40 to solve most of the timing problems in microcomputer systems design. The individual counter channels can be cascaded for longer count sequences. Counting can be done in either BCD or binary. Two of the counters are typically dedicated to generate the independent baud rates for both serial channels.

An external clock input, TCLK, is accessible to each of the 3 counter/timers as a software selectable source. Its input is through J13 pin 10.

Parallel I/O - Three 8-bit parallel I/O ports are provided through a 82C55A PPI. It supports 24 I/O pins which may be individually programmed in 2 groups of 12 in three major modes of operation. In the first mode, Mode 0, each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines for control, borrowing one from the other group for handshaking.

There is direct bit set/reset capability for control application interface requirements. The 82C55A has sufficient drive capability to interface directly with Opto-22 type modules. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. Each I/O line has a pull-up resistor to keep the input from flotation. The 24 lines are connected through J2, a 26-pin connector. Pins 25 and 26 are wired to +5 volts and ground respectively in order to allow easy and convenient connection to display interfaces, keypads or other devices that require power.

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J2 - Parallel I/O Connector

Pin	Signal	Pin	Signal
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	+5 VDC	26	Ground

Interrupts - The LPM-SBC40A supports nonmaskable interrupts (NMIRQ*), maskable interrupts, and software exceptions. The six software exceptions supported are: Divide error, Array bound overflow, Break on overflow, Break, Single Step, and Mode Switch (for 8080 emulation). Interrupt vectors are determined automatically for exceptions and the NMIRQ* or supplied by hardware for maskable interrupts.

Jumper J17 on the LPM-SBC40A permits the user to select a variety of interrupt input sources. An onboard master 82C59A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the four interrupt lines from the front plane interrupt connector (J13), the 2 serial channels, 3 counter/timer outputs, iSBX connector, real time clock, or the STD Bus backplane signals INTRQ*, INTRQ*1, and INTRQ*2. The interrupt sources are jumpered selectable by the user and assigned unique vectors by the PIC.

The LPM-SBC40XT has the 82C59A hardware interrupt inputs jumpered by WinSystems at the factory for PC-XT compatibility. Additionally, the BIOS configures the interrupt controller at power up. The interrupt input vectors and input sources can still be changed by the user; however, it may alter PC compatibility.

PC-XT Compatible Vector Table

PIC Input	Vector	Function
IRQ0	8H	Clock Tick
IRQ1	9H	Keyboard
IRQ2	AH	STD Bus pin 50 (INTRQ*)
IRQ3	BH	STD Bus pin 37 (INTRQ1*)
IRQ4	CH	STD Bus pin 44 (INTRQ2*)
IRQ5	DH	Open
IRQ6	EH	Floppy disk
IRQ7	FH	Open

Four interrupt request lines are available over the front plane and are accessed through connector J13. The V40 parallel interrupt priority scheme is implemented over the front plane of the card for multiple interrupting cards. For systems with multiple slave 82C59A PIC's, additional logic is included to provide the cascade STD-8088 interrupt priority scheme. It is implemented by supplying the slave cascade address over the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. This permits a single peripheral card to generate an interrupt and receive its cascade response totally on the STD Bus backplane.

J13 Pinout - Interrupts

Pin	Signal
2	Int Req 3
4	Int Req 4
6	Int Req 5
8	Int Req 6
10	TCLK input
Odd pins	Ground

Real Time Clock - An OKI MSM6264 clock calendar is on board. The chip keeps track of seconds, minutes, hours, days of week, date, month, and years. It can operate in either a 12/24 hour format and Leap Year timing is automatic. An onboard 32.768 KHz crystal oscillator determines the time base. The RTC can generate a software selectable interrupt of 1/64 second, 1 second, 1 minute, or 1 hour. Input to the PIC is via the J17 interrupt selection header.

It can be battery powered by either the VBAT line of the STD Bus (pin 5) or by an optional external battery attached to the board.

A device driver called CLOCK.SYS is provided for the LPM-SBC40R and LPM-SBC40XT that will allow the reading and setting of the real time clock using the MS-DOS TIME/DATE commands.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a 50 mS PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

The LPM-SBC40XT's ROM BIOS will support the watchdog timer. The BIOS senses if it is enabled and will load the interrupt routine that will retrigger the

watchdog timer. It is the user's responsibility to call the routine at least every 1.5 seconds or a hardware reset will occur.

Battery Back-up - An optional 170 mAH battery can be supplied with the LPM-SBC40A board to provide power for the real time clock and up to 3 RAM memory sockets. The LPM-SBC40A has special circuitry to support both the low power 32K and 128K byte static RAMs. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the calendar clock and the RAM's selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and back OFF again when Vcc returns to normal.

Multimodule Connector - A single 8-bit iSBX Multimodule connector is provided to accommodate single-wide, 36-pin I/O expansion modules. SBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, networking, graphics controllers, and other special purpose peripheral functions.

The LPM-SBC40A decodes I/O addresses and generates the chip selects for the SBX boards. DMA operations are supported through channel 0 on the V40 chip.
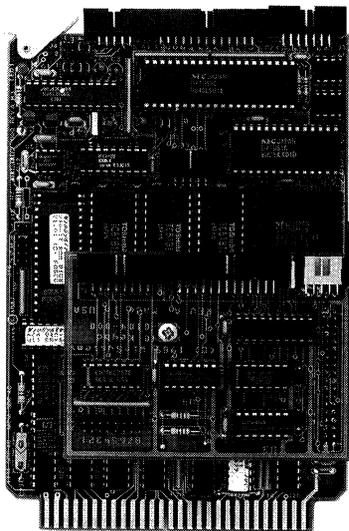
The LPM-SBC40XT is shipped with a special multimodule attached that serves as the status, keyboard and floppy disk/DMA interface. A PC-XT compatible keyboard will plug into the board for console input

operations. A connector and interface electronics is provided to link the DMA, Interrupt, and I/O signals necessary to communicate with the WinSystems LPM-SCSI floppy disk/SCSI STD Bus controller card.

Status LED - A status LED is available on the board to monitor system activity. Under program control it can indicate error conditions or blink different patterns to provide visual indication of program status.

I/O - I/O ports are specified by a 16-bit address by the V40 for a total system capacity of 64K ports. IOEXP* is supported and is active high whenever an I/O address above 4096 is generated by ORing A13 through A15. This allows I/O mapped boards which only decode 8 address bits to be mixed with boards that decode 16-bits.

The V40 CPU permits the internal peripheral addresses to be relocated within the memory map by writing to the internal peripheral relocation register. This gives the LPM-SBC40A the ability to be DOS compatible and be easily reconfigured to run either ROM-DOS or MS-DOS. The other off-chip peripherals (82C55A, 82C51A, OKI MSM6242 RTC, SBX connector, Watchdog Timer, and Status LED) are mapped by a PAL to a fixed location. This is different for the LPM-SBC40A, LPM-SBC40R and LPM-SBC40XT board configurations.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important because it detects brown-outs or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, which prevents invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

SOFTWARE SUPPORT

WINMON88-SBC40 is an optional monitor program for the LPM-SBC40A that is used for program development and debugging. It is resident in an 8Kbyte EPROM and allows the user to develop, load, execute, debug, and modify a program. This firmware allows the development of application programs on IBM PC compatible products for subsequent loading directly into the LPM-SBC40A through the serial I/O channel. Furthermore it has user selectable program functions including memory, register and port read and write, load data, execute, and multiple breakpoint detection.

It has the same instruction mnemonics and display format as the IBM DEBUG program.

C-THRU-ROM-SBC40 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the LPM-SBC40A. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC/XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM consists of a source level debugging user interface with target communication facility that resides on the LPM-SBC40A. The target system kernel includes an execution control program and host communication facility. During a debug session, symbolic information is maintained on a PC/XT/AT host and the program code is downloaded to the LPM-SBC40A for execution over a 9600 bps serial port. The application program is debugged directly on the LPM-SBC40A.

CTR Debugger - The C-THRU-ROM windowing debugger provides access into the LPM-SBC40A and is completely compatible with Microsoft C version 5.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote CodeView. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

The Debugger is a source level debugger. This means that the Debugger, in addition to understanding the 80X86/88 machine code, understands such symbols as function names, global variables, and publics, locals, and register variables. This also means that the debugger knows about line numbers, and even

modules, making it possible to set break points, unassemble, and go directly to the code at any line.

With the Debugger a listing of the program appears on the screen. One can single-step through the program lines, examine variables, execute parts of the program, and watch both program listing and the output it generates.

The lines of code are displayed as they are executed, giving one the opportunity to stop execution, examine and change variables and registers, trace a single line or instruction, or even restart the program from scratch.

C-THRU-ROM does not include Microsoft C, MASM, or Borland Turbo-C since it is assumed these PC based development tools are owned by the user. The C-THRU-ROM development package includes the diskettes, RAM, target system kernel EPROM, serial I/O cable and documentation. If C-THRU-ROM is ordered at the same time as the LPM-SBC40A, the factory will integrate and test the system at no extra charge.

C-THRU-ROM must be specified with the CPU clock speed for the WinSystems' LPM/MCM-SBC40 and LPM/MCM-SBC50 STD Bus SBCs. This specifies a unique kernel for the card since the communications data rate is a function of the CPU frequency and not an independent baud rate clock oscillator.

ROM-DOS - ROM-DOS is a MS-DOS 3.2 compatible ROM based operating system for embedded the LPM-SBC40R. ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS is designed especially for programmers with embedded systems designs. It provides 3 major functions: start-up code, file support and standard drivers.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that

greatly simplifies data storage and retrieval. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

All development can be done on a PC and debugged on the target system which completes the project in the shortest time.

The ROM-DOS operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. It will not accept unsupported BIOS calls or direct hardware manipulation.

A standard ROM-DOS setup has the code for ROM-DOS and Mini-BIOS in the top 32K bytes of ROM, and the user application program (.EXE file) and associated disk files in ROM on a ROM-disk. The ROM's containing the actual ROM-disk files are placed in any convenient location above the system RAM. The ROMDISK is configured as the "A" drive so ROM-DOS will search it for the initial program upon booting.

The booting process is started when power is applied to the system. The BIOS initializes the hardware and transfers control to ROM-DOS. ROM-DOS then performs its own initialization and loads the user's application program for execution. The user's program is then given control and typically remains running until the power is turned off.

MS-DOS - The LPM-SBC40XT is MS-DOS 3.3 compatible with or without a disk. In harsh environments or at extended temperatures, it will work with a RAM/ROM disk with MS-DOS and the application program residing in ROM. Video and a standard keyboard are not required for operation either.

For program/application development, the LPM-SBC40XT is offered configured with disk drives and video in a card cage to make a complete STD Bus DOS system. This can serve as a platform for initial development and debugging. Later the extra components can be removed during run time if they are not needed or if they are not rugged enough for the application environment. The benefit is that all the familiar development tools on the IBM PC are available for use to expedite software development.

WinSystems offers a wide selection of additional CMOS STD Bus I/O cards including Ethernet, Arcnet, serial I/O, parallel I/O, A/D, D/A and other special purpose I/O cards.

Technical Assistance

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4

SPECIFICATIONS

Electrical

Bus Interface: CMOS STD-8088 compatible.
System Clock: 5, 8, or 10 MHz
Serial Interface: RS-232 both channels,
                RS-422/485 channel 1 only
Interrupts: TTL input level with 10K ohm pull-up resistors

Parallel: 5 74LS TTL loads

Vcc = +5V ± 10% at 125 mA typ. (No memory installed)

Without RS-422/485 Drivers

Vcc = +5V ± 10% at 75 mA typ. (No memory installed)

Memory

Addressing: 1 Megabyte

Capacity: Supports 8K, 16K, 32K, 64K, and 128K byte 32-pin RAM, RQM, EPROM, and EEPROMs.

Mechanical

Dimensions: Meets all STD Bus mechanical specifications except I/O connectors extend beyond card edge: 4.5 x 7.0 x 0.6 inches
Jumpers: 0.025" square posts

Connectors

J1, Serial I/O: 10-pin 0.100" grid
J3, Serial I/O: 14-pin 0.100" grid
J2, Parallel I/O: 26-pin 0.100" grid
J13, Interrupts: 10-pin 0.100" grid
J19, SBX Multimodule: 44-pin 0.100" dual row female

Environmental

Operating Temperature: -40° to +85°C
        (with no memory installed)
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC40A-5	5MHz V40 SBC
LPM-SBC40A-5-BAT	5MHz V40 SBC with battery installed
LPM-SBC40A-8	8 MHz V40 SBC
LPM-SBC40A-8-BAT	8 MHz V40 SBC with battery installed
LPM-SBC40A-10	10 MHz V40 SBC
LPM-SBC40A-10-BAT	10 MHz V40 SBC with battery installed
LPM-SBC40R-8	LPM-SBC40A-8 setup to run ROM-DOS
LPM-SBC40R-8-BAT	LPM-SBC40R with battery installed
LPM-SBC40XT-128	8MHz LPM-SBC40A with 128K of RAM, PC-XT BIOS, and keyboard interface
LPM-SBC40XT-256	LPM-SBC40XT with 256KB of memory
LPM-SBC40XT-384	LPM-SBC40XT with 384KB of memory
WINMON88-SBC40	Monitor program for the LPM-SBC40A with WINTERM terminal emulator for a PC/XT/AT
RDOS-SBC40-8	ROM-DOS development package for LPM-SBC40R-8
CTR-SBC40-5	Symbolic Debugger for the LPM-SBC40A-5 including monitorEPROMs, communications facility and host program.
CTR-SBC40-8	8 MHz version of CTR-SBC40
CTR-SBC40-10	10MHz version of CTR-SBC40

WinSystems, Inc.

WinSystems®

STD BUS

MCM-SBC40A
MCM-SBC40R
MCM-SBC40XT

FEATURES

- V40 (integrated 8088) CMOS 16-bit processor
- Standalone or DOS compatible Single Board Computer
- PC-XT compatible (MCM-SBC40XT)
- Direct Addressing to 1 Mbyte
- Onboard DMA
- Four 32-pin bytewide memory sockets supports RAM, EPROM, psuedo-static RAM and EEPROM
- 3 memory sockets support battery backed RAM
- Memory and I/O WAIT State generator
- Two 8251 type Serial I/O ports both with RS-232 and one with RS-422/485 levels
- Programmable Interrupt Controller (8259A type)
- 24 parallel I/O lines (8255A)
- Three 16-bit Counter/Timer channels (8254 type)
- 24 hour battery backed Calendar clock
- Flexible I/O mapping
- iSBX Multimodule connector
- Watchdog timer
- Precision power-on/brown out detect circuit
- LED Status monitor
- Optional 8087 coprocessor support
- 8080 Software emulation mode
- Optional symbolic firmware debugger
- Optional ROM-DOS Embedded Operating System
- +5V only operation
- Temperature range: 0° to +65°C
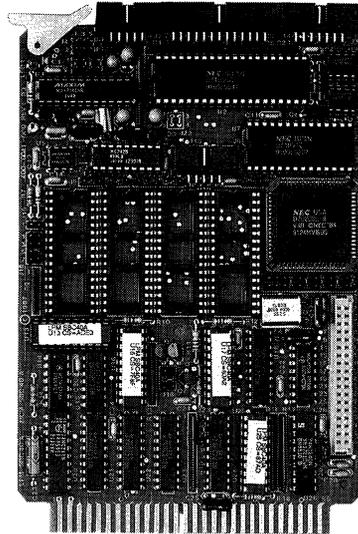
4

*SHADING INDICATES SOCKETS ONLY
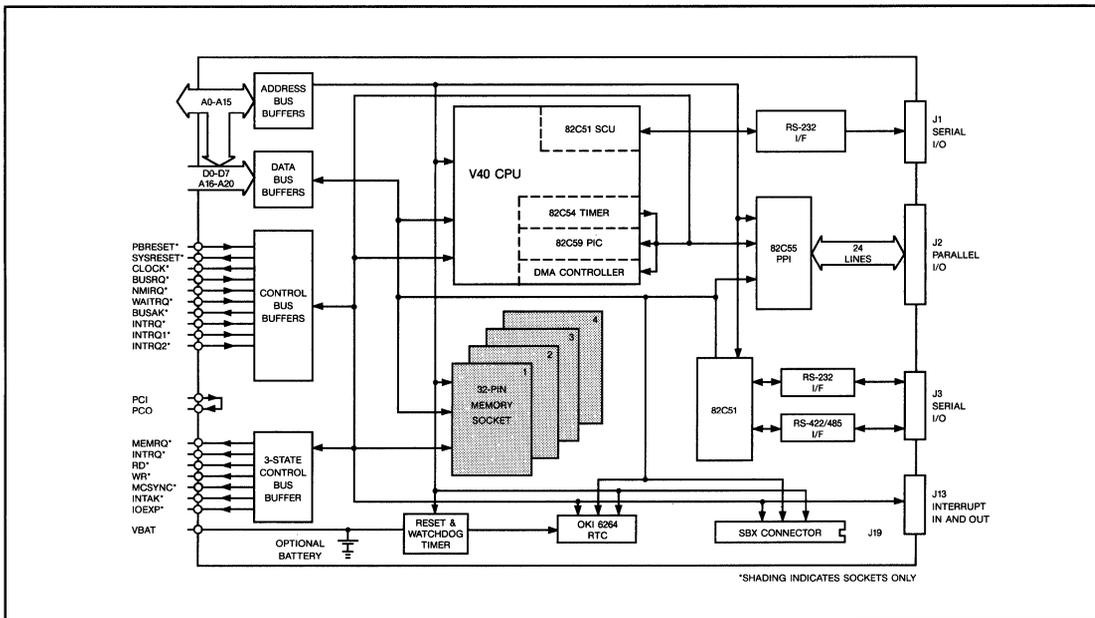
The MCM-SBC40A is a very versatile, V40 based (highly integrated 8088 equivalent) Single Board Computer (SBC) on the STD Bus. The MCM-SBC40A contains the CPU, 4 memory sockets, 2 serial I/O channels, counter/timers, interrupt controller, DMA controller, clock calendar, parallel I/O and STD Bus interface on a single card. Furthermore a precision powerfail reset circuit, watchdog timer, and SBX multimodule connector are incorporated on the all card making it ideal for high performance embedded applications requiring low power, small size, extended temperature operation. It is designed for users requiring a standalone SBC with no operating system onboard.

For other applications with file management or other operating system environment structures, WinSystems offers two additional versions of this board. The MCM-SBC40R is the SBC40A with the ROM-DOS Embedded Operating System installed. The MCM-SBC40XT is the SBC40A configured as a PC-XT running MS-DOS version 3.3 including memory and a keyboard interface. The RAM/EPROM population option, firmware supplied and decoder PALs determine the ultimate configuration of the SBC40A. These options are designed to make application software development as quick and easy as possible.

FUNCTIONAL CAPABILITY

Processor - The MCM-SBC40A incorporates the powerful 16-bit V40 processor which has a 20-bit direct memory address capability of 1 Mbyte. It is code compatible with the 8088 CPU. The V40 has 16-bit internal and 8-bit external data busses for enhanced execution speed. It runs all the 8088 instructions plus enhanced and unique instructions for bit manipulation, high speed block transfers, and engineering control applications. The processor is fully buffered and operates at either 5, 8 or 10 MHz.

An NEC V40 processor is installed for improved performance over the 80188 plus the power/economy of CMOS. The V40 executes faster than the 80188 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high-speed multiplication/division instructions.

The V40 will also operate in the 8080 emulation mode. In this mode, the 8080 instruction set is emulated by the V40, allowing migration of previously developed 8-bit software to this board.

Co-Processor - The SBC40 card can accept the optional NDP-8087, 8087 numeric data processor module, for a hundredfold increase in arithmetic operations over the CPU alone. It contains the V40 CPU, interface electronics, and 8087 socket. A special version of the SBC40 is supplied with a only a PGA socket for the CPU so that the NDP-8087 then will plug into the location normally occupied by the V40. The coprocessor is not normally supplied by WinSystems.

Addressing - The V40 processor supports direct addressing of 1 Mbyte on 20 address lines. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data lines D0 through D3 at the beginning of each memory operation. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. The multiplexing of the extra address lines on the data bus requires no additional CPU overhead and is transparent and compatible to other I/O mapped cards. MEMEX* is wired to ground.

Memory - Four JEDEC standard 32-pin bytewide sockets are provided to allow the use of static RAM, pseudo-static RAM, ROM, EPROM or EEPROMs. The sockets are configurable for 8K, 16K, 32K, 64K, and 128Kbyte devices for a total of 512KB onboard. Either 28 or 32-pin memory devices can be plugged into the sockets. Eight standard memory maps are jumper selectable. Five maps are preprogrammed and 3 are user programmable for custom decoding by the user. The MCM-SBC40A is supplied with no memory installed.

The MCM-SBC40XT board is configured with a PC-XT compatible BIOS in EPROM and up to 384KB of pseudo-static RAM installed in the other 3 sockets. This board will attempt to boot DOS from a floppy disk, hard disk or RAM/ROM disk upon power up. The MCM-SBC40R has the ROM-DOS EPROM installed in the first socket and no other memory.

Direct Memory Access - A DMA channel is available from the V40 CPU to the SBX socket to perform high speed data transfers between memory and I/O devices in bytes or words. It can be programmed in either the single, block, or demand mode.

DRAM Refresh - The V40 generates the REFRESH* signal and refresh addresses up to 512 rows. The interval can programmed to accommodate the requirements of dynamic and pseudo-static memories.

A pseudo-static RAM incorporates features and benefits from both DRAMs and SRAMs. It is similar to

a DRAM since it needs a 4 mS refresh; however, it will fit into a standard 28 or 32-pin bytewide memory socket and access just like a SRAM. This means that a standard bytewide socket accepts a lower cost, high density, high speed RAM offering more memory flexibility to the board.

WAIT State Generation - A Wait Control Unit can be programmed to insert wait states of up to three clocks during a bus cycle to compensate for the access speeds of slower memory or I/O devices.

Serial Communications - A double buffered, full-duplex, serial asynchronous channel is implemented inside the V40 CPU with a 8251 type programmable communication interface. The V40 contains an independent on-chip software programmable baud rate generator selectable through 38.4K bits per second. A second 8251 device is onboard to provide the other serial channel.

The card will work with 7 or 8-bit character lengths. It will handle 1 or 2 stop bits; false start bit detection, and automatic break detection and handling. Automatic error detection is provided for parity, overrun, and framing. Each serial channel is fully interrupt driven.

Jumpers options permit configuration of the serial I/O as either DCE or DTE. Both RS-232 and RS-422/485 interface levels are supported on channel 1. Channel 2 supports RS-232 only. The RS232 devices require only +5 volts since the $\pm$ voltages are generated on-chip by a Maxim MAX238.

Channel 1 is configurable for RS-422/485 electrical interface levels. The RS-422 configuration provides separate transmit and receive signal pairs. For RS-485 multidrop lines, only one signal pair is used for "party line" network structures. The MCM-SBC40A is designed to properly disable the transmitter upon reset to prevent potential lock-up problems cause from a transmitter being stuck in the ON mode. Both the RS-422/485 transmitter and receiver have 100 ohm termination resistors installed onboard.

J1 Pinout - V40 SCU Serial Channel

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J3 Pinout - 82C51A Serial Channel

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	No connection
7	Ground
14	RS-422/485 Transmit Data +
15	RS-422/485 Transmit Data -
16	RS-422/485 Receive Data +
17	RS-422/485 Receive Data -

Counter/Timers - There are three independent, software programmable, 16-bit counter/timers available through an 8254 type device internal to the V40 to solve most of the timing problems in microcomputer systems design. The individual counter channels can be cascaded for longer count sequences. Counting can be done in either BCD or binary. Two of the counters are typically dedicated to generate the independent baud rates for both serial channels.

An external clock input, TCLK, is accessible to each of the 3 counter/timers as a software selectable source. Its input is through J13 pin 10.

Parallel I/O - Three 8-bit parallel I/O ports are provided through a 8255A PPI. It supports 24 I/O pins which may be individually programmed in 2 groups of 12 in three major modes of operation. In the first mode, Mode 0, each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines for control, borrowing one from the other group for handshaking.

There is direct bit set/reset capability for control application interface requirements. The 8255A has sufficient drive capability to interface with Opto-22 type modules. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. Each I/O line has a pull-up resistor to keep the input from flotation. The 24 lines are connected through J2, a 26-pin connector. Pins 25 and 26 are wired to +5 volts and ground respectively in order to allow easy and convenient connection to display interfaces, keypads or other devices that require power.

4

J2 - Parallel I/O Connector

Pin	Signal	Pin	Signal
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	+5 VDC	26	Ground

Interrupts - The MCM-SBC40A supports nonmaskable interrupts (NMIRQ*), maskable interrupts, and software exceptions. The six software exceptions supported are: Divide error, Array bound overflow, Break on overflow, Break, Single Step, and Mode Switch (for 8080 emulation). Interrupt vectors are determined automatically for exceptions and the NMIRQ* or supplied by hardware for maskable interrupts.

Jumper J17 on the MCM-SBC40A permits the user to select a variety of interrupt input sources. An onboard master 8259A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the four interrupt lines from the front plane interrupt connector (J13), the 2 serial channels, 3 counter/timer outputs, iSBX connector, real time clock, or the STD Bus backplane signals INTRQ*, INTRQ*1, and INTRQ*2. The interrupt sources are jumpered selectable by the user and assigned unique vectors by the PIC.

The MCM-SBC40XT has the 8259A hardware interrupt inputs jumpered by WinSystems at the factory for PC-XT compatibility. Additionally, the BIOS configures the interrupt controller at power up. The interrupt input vectors and input sources can still be changed by the user; however, it may alter PC compatibility.

PC-XT Compatible Vector Table

PIC Input	Vector	Function
IRQ0	8H	Clock Tick
IRQ1	9H	Keyboard
IRQ2	AH	STD Bus pin 50 (INTRQ*)
IRQ3	BH	STD Bus pin 37 (INTRQ1*)
IRQ4	CH	STD Bus pin 44 (INTRQ2*)
IRQ5	DH	Open
IRQ6	EH	Floppy disk
IRQ7	FH	Open

Four interrupt request lines are available over the front plane and are accessed through connector J13. The V40 parallel interrupt priority scheme is implemented over the front plane of the card for multiple interrupting cards. For systems with multiple slave 8259A PIC's, additional logic is included to provide the cascade STD-8088 interrupt priority scheme. It is implemented by supplying the slave cascade address over the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. This permits a single peripheral card to generate an interrupt and receive its cascade response totally on the STD Bus backplane.

J13 Pinout - Interrupts

Pin	Signal
2	Int Req 3
4	Int Req 4
6	Int Req 5
8	Int Req 6
10	TCLK input
Odd pins	Ground

Real Time Clock - An OKI MSM6264 clock calendar is onboard. The chip keeps track of seconds, minutes, hours, days of week, date, month, and years. It can operate in either a 12/24 hour format and Leap Year timing is automatic. An onboard 32.768 KHz crystal oscillator determines the time base. The RTC can generate a software selectable interrupt of 1/64 second, 1 second, 1 minute, or 1 hour. Input to the PIC is via the J17 interrupt selection header.

It can be battery powered by either the VBAT line of the STD Bus (pin 5) or by an optional external battery attached to the board.

A device driver called CLOCK.SYS is provided for the MCM-SBC40R and MCM-SBC40XT that will allow the reading and setting of the real time clock using the MS-DOS TIME/DATE commands.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a 50 mS PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

The MCM-SBC40XT's ROM BIOS will support the watchdog timer. The BIOS senses if it is enabled and will load the interrupt routine that will retrigger the

watchdog timer. It is the user's responsibility to call the routine at least every 1.5 seconds or a hardware reset will occur.

Battery Back-up - An optional 170 mAH battery can be supplied with the MCM-SBC40A board to provide power for the real time clock and up to 3 RAM memory sockets. The MCM-SBC40A has special circuitry to support both the low power 32K and 128KByte static RAMs. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the calendar clock and the RAM's selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and back OFF again when Vcc returns to normal.

Multimodule Connector - A single 8-bit iSBX Multimodule connector is provided to accommodate single-wide, 36-pin I/O expansion modules. SBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, networking, graphics controllers, and other special purpose peripheral functions.

The MCM-SBC40A decodes I/O addresses and generates the chip selects for the SBX boards. DMA operations are supported through channel 0 on the V40 chip.
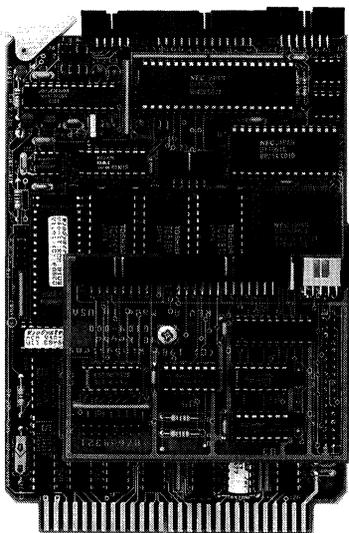
MCM-SBC40XT

The MCM-SBC40XT is shipped with a special multimodule attached that serves as the status, keyboard and floppy disk/DMA interface. A PC-XT compatible keyboard will plug into the board for console input

operations. A connector and interface electronics is provided to link the DMA, Interrupt, and I/O signals necessary to communicate with the WinSystems MCM-DISK-XT floppy disk/SCSI STD Bus controller card.

Status LED - A status LED is available on the board to monitor system activity. Under program control it can indicate error conditions or blink different patterns to provide visual indication of program status.

I/O - I/O ports are specified by a 16-bit address by the V40 for a total system capacity of 64K ports. IOEXP* is supported and is active high whenever an I/O address above 4096 is generated by ORing A13 through A15. This allows I/O mapped boards which only decode 8 address bits to be mixed with boards that decode 16-bits.

The V40 CPU permits the internal peripheral addresses to be relocated within the memory map by writing to the internal peripheral relocation register. This gives the MCM-SBC40A the ability to be DOS compatible and be easily reconfigured to run either ROM-DOS or MS-DOS. The other off-chip peripherals (82C55A, 82C51A, OKI MSM6242 RTC, SBX connector, Watchdog Timer, and Status LED) are mapped by a PLA to a fixed location. This PAL is different for the MCM-SBC40A, MCM-SBC40R and MCM-SBC40XT board configurations.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This action is critically important because it detects brown-outs or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.65 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, which prevents invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

SOFTWARE SUPPORT

WINMON88-SBC40 is an optional monitor program for the MCM-SBC40A that is used for program development and debugging. It is resident in an 8Kbyte EPROM and allows the user to develop, load, execute, debug, and modify a program. This firmware allows the development of application programs on IBM PC compatible products for subsequent loading directly into the MCM-SBC40A through the serial I/O channel. Furthermore it has user selectable program functions including memory, register and port read and write, load data, execute, and multiple breakpoint

detection. It has the same instruction mnemonics and display format as the IBM DEBUG program.

C-THRU-ROM-SBC40 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C or Borland Turbo-C for use with the MCM-SBC40A. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC/XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X88/80X86 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs.

C-THRU-ROM consists of a source level debugging user interface with target communication facility that resides on the MCM-SBC40A. The target system kernel includes an execution control program and host communication facility. During a debug session, the symbolic information is maintained on a PC/XT/AT host and the program code is downloaded to the MCM-SBC40A for execution over a 9600 bps serial port. The application program is debugged directly on the MCM-SBC40A.

The C-THRU-ROM windowing debugger provides access into the MCM-SBC40A and is completely compatible with Microsoft C version 5.x and Turbo-C version 2.x or higher. The Debugger can best be described as a remote CodeView. The window placement and usage are very similar to CodeView. A user familiar with CodeView will be able to step in and use C-THRU-ROM Debugger in a few minutes.

The Debugger is a source level debugger. This means that the Debugger, in addition to understanding the 80X86/88 machine code, understands such symbols as function names, global variables, and publics, locals, and register variables. This also means that the debugger knows about line numbers, and even

modules, making it possible to set break points, unassemble, and go directly to the code at any line.

With the Debugger a listing of the program appears on the screen. One can single-step through the program lines, examine variables, execute parts of the program, and watch both program listing and the output it generates.

The lines of code are displayed as they are executed, giving one the opportunity to stop execution, examine and change variables and registers, trace a single line or instruction, or even restart the program from scratch.

C-THRU-ROM does not include Microsoft C, MASM, or Borland Turbo-C since it is assumed these PC based development tools are owned by the user. The C-THRU-ROM development package includes the diskettes, RAM, target system kernel EPROM, serial I/O cable and documentation. If C-THRU-ROM is ordered at the same time as the MCM-SBC40A, the factory will integrate and test the system at no extra charge.

C-THRU-ROM must be specified with the CPU clock speed for the WinSystems' LPM/MCM-SBC40 and LPM/MCM-SBC50 STD Bus SBCs. This specifies a unique kernel for the card since the communications data rate is a function of the CPU frequency and not an independent baud rate clock oscillator.

ROM-DOS - ROM-DOS is a MS-DOS 3.2 compatible ROM based operating system for embedded the MCM-SBC40R. ROM-DOS reduces the ROM, RAM and hardware requirements to a minimum while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications. This results in a low cost system with access to PC based tools and DOS functionality.

ROM-DOS is designed especially for programmers with embedded systems designs. It provides 3 major functions: start-up code, file support and standard drivers.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the applications code. Programs can be written in assembly or C, or high level languages such as Pascal, compiled BASIC. It supports standard MS-DOS file structures that

greatly simplifies data storage and retrieval. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur.

All development can be done on a PC and debugged on the target system which completes the project in the shortest time.

The ROM-DOS operating system enables a user to place the MS-DOS application in a diskless embedded system and have it start running immediately after power is applied. ROM-DOS supports all documented MS-DOS calls (except networking) and all INT21 hex DOS Services. It will not accept unsupported BIOS calls or direct hardware manipulation.

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SPECIFICATIONS

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Bus Interface: STD Bus compatible.
System Clock: 5, 8, or 10 MHz
Serial Interface: RS-232 both channels,
RS-422/485 channel 1 only
Interrupts: TTL input level with 10K ohm pull-up resistors

Parallel: 5 74LS TTL loads

Vcc = +5V ± 10% at 475 mA typ. (No memory installed)

Without RS-422/485 Drivers

Vcc = +5V ± 10% at 275 mA typ. (No memory installed)

Memory

Addressing: 1 Megabyte

Capacity: Supports 8K, 16K, 32K, 64K, and 128K byte 32-pin RAM, ROM, EPROM, and EEPROMs.

Mechanical

Dimensions: Meets all STD Bus mechanical specifica-
tions except I/O connectors extend
beyond card edge: 4.5 x 6.5
Jumpers: 0.025" square posts

Connectors

J1, Serial I/O: 10-pin 0.100" grid
J3, Serial I/O: 14-pin 0.100" grid
J2, Parallel I/O: 26-pin 0.100" grid
J13, Interrupts: 10-pin 0.100" grid
J19, SBX Multimodule: 44-pin 0.100" dual row female

Environmental

Operating Temperature: 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-SBC40A-5	5MHz V40 SBC
MCM-SBC40A-5-BAT	5MHz V40 SBC with battery installed
MCM-SBC40A-8	8 MHz V40 SBC
MCM-SBC40A-8-BAT	8 MHz V40 SBC with battery installed
MCM-SBC40A-10	10 MHz V40 SBC
MCM-SBC40A-10-BAT	10 MHz V40 SBC with battery installed
MCM-SBC40R-8	MCM-SBC40A-8 setup to run ROM-DOS
MCM-SBC40R-8-BAT	MCM-SBC40R with battery installed
MCM-SBC40XT-128	8MHz MCM-SBC40A with 128K of RAM, PC-XT BIOS, and keyboard interface
MCM-SBC40XT-256	MCM-SBC40XT with 256KB of memory
MCM-SBC40XT-384	MCM-SBC40XT with 384KB of memory
WINMON88-SBC40	Monitor program for the MCM-SBC40A with WINTERM terminal emulator for a PC/XT/AT
RDOS-SBC40-8	ROM-DOS development package for MCM-SBC40R-8
CTR-SBC40-5	Symbolic Debugger for the MCM-SBC40A-5 including monitor EPROMs, communications facility and host program.
CTR-SBC40-8	8 MHz version of CTR-SBC40
CTR-SBC40-10	10MHz version of CTR-SBC40

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- 80C88 CMOS Multifunction Single Board Computer
- High-speed CMOS technology: low power consumption, high noise immunity, wide temperature range
- Direct addressing to 1 Mbyte
- 8087 Numeric Coprocessor socket
- Choice of CPU speeds (5 & 8 MHz)
- Optional debug monitor PROM
- Two 28-pin bytewide memory sockets supporting RAM, ROM, EPROM, and EEPROMs
- Serial RS-232 or RS-422/485 serial interface with diagnostic loopback capability
- Programmable baud rate from 50 to 38.4 Kbaud
- 82C59A Programmable interrupt controller with 8 interrupt sources
- Supports cascadeable or front plane interrupts
- iSBX Multimodule expansion connector
- Three 16-bit Counter/Timer channels (82C54)
- Optional 8080 software emulation mode
- Precision power-on/brown out detect circuit
- Optional SLEEP mode for very low power operation
- Operational temperature range: -40 to +85°C
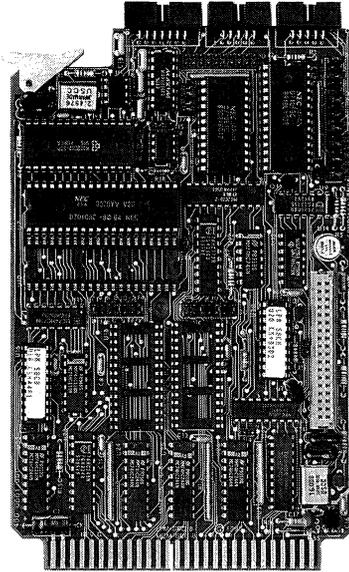
The LPM-SBC8 is a powerful, multifunction 8088 CMOS STD Bus single board computer combining the CPU, 2 28-pin memory sockets, 8087 socket, 3 counter/timers, serial I/O, interrupt controller, precision powerfail/brown out reset circuit, watchdog timer and full STD Bus interface onto a single card. Furthermore, an iSBX multimodule connector is incorporated on the card to support expansion modules mounted on the board. The LPM-SBC8 is ideal for applications requiring low power, small size, extended temperature operation and high reliability.
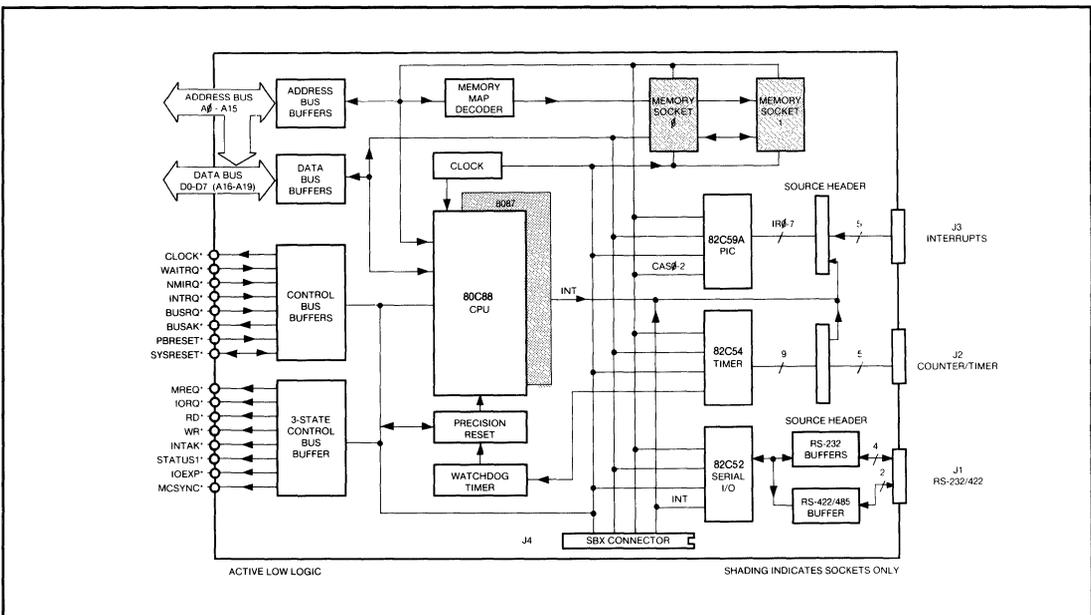
FUNCTIONAL CAPABILITY

Processor - The LPM-SBC8 incorporates the popular 16-bit 80C88 processor which has a 20-bit direct address capability of 1 Mbyte. The processor is fully buffered and operates at either 5 or 8 MHz.

A NEC V20 processor can optionally be installed for improved performance. The V20 executes faster than the 80C88 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high-speed multiplication/division instructions.

The V20 will also operate in the 8080 emulation mode. In this mode, the 8080 instruction set is emulated by the V20 allowing migration of previously developed 8-bit software to this board.

SLEEP Mode - The LPM-SBC8 with the NEC V20 has a low power standby mode to reduce power consumption. The standby mode is available in both the native 8088 and 8080 emulation mode. The processor stops in a known condition with only the internal oscillator and standby release circuits operational. The mode is released by detection of a SYSRESET*, INTRQ* or NMIRQ* external interrupt.

8087 Coprocessor - The SBC8 card is configured for the maximum mode in order to support an optional 8087 Coprocessor providing up to 100 times the performance of the CPU alone. It provides arithmetic, logarithmic, exponential, trigonometric, and floating point arithmetic with up to 80-bit results.

Addressing - The 8088 processor supports direct addressing of 1 Mbyte on 20 address lines. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data lines D0 through D3 at the beginning of each memory operation. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. The multiplexing of the extra address lines on the data bus requires no additional CPU overhead and is transparent and compatible to other I/O mapped cards. The SBC8 conforms to the STDMG STD-8088 specifications.

Memory - Two JEDEC standard 28-pin bytewide sockets are provided to allow the use of RAM, ROM, EPROM or EEPROMs. The sockets are configurable for 8K, 16K, or 32K byte RAMs and up to 64K byte EPROM devices. The first socket is configured to accept an EPROM mapped at FFFF0h for the 8088's power on restart address. The second socket is mapped to begin at 00000h to support the 8088 inter-

rupt vector table structure and user application code. The sockets can be remapped if different options are required.

MEMEX is not used and is open.

Serial Communications - A fully buffered serial asynchronous channel is implemented with the 82C52 full duplex, programmable communication interface device. The 82C52 contains an independent on-chip software programmable baud rate generator. It has 18 different frequencies that are jumper selectable from 50 through 38.4K bits per second.

In asynchronous mode, the card will work with 5 to 8 bit characters. It will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing. The serial channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream. Also the bidirectional control for the RS-422/485 signals is done by the 82C52. The serial channel status signals can be jumpered to the 82C59A to generate vectored interrupts.

Both RTS and CTS modem handshake lines are provided in addition to the transmit and receive lines. Jumpers options permit configuration of the serial I/O as either DCE or DTE. Both the RS-232 and RS-422/485 interface levels are brought out to a 14-pin connector. This allows easy connections to flat cables with 25 pin RS-232 "D" type connectors.

J1 Pinout SIO Channel

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
14	RS422/485 Data +
15	RS422/485 Data -

Counter/Timers - There are three independent software programmable 16-bit counter/timers available through the 82C54 to solve most of the timing problems in microcomputer systems design. Six flexible timer modes allow the 82C54 to be used as an event counter, time delay, multitasking executive time base, programmable one-shot, clock, motor controller, square wave generator, baud rate generator, and other applications. The individual counter channels can be cascaded for longer count sequences.

The outputs of each counter/timer can be jumpered to the 82C59A PIC to generate vectored interrupts. The Clock, Gate and Output of all 3 counter/timers are accessable through jumper options and available for external use through J2, a 10 pin connector. The standard connector configuration is as follows:

J2 Pinout - Counter/Timer

Pin	Signal
2	CLK 0 Input
4	Gate 0
6	CLK 1 Input
8	Gate 1
10	CLK 2 Input
1, 3, 5	Ground
7, 9	Ground

Watchdog Timer - Counter 2 of the 82C54 has a special configuration option to allow its output to serve as a retriggerable watchdog timer. The counter output can be jumpered to PBRESET* to automatically reset the processor after a programmable period of time. This is important for use in remote and unattended applications.

Real Time Clock - An optional Dallas Semiconductor Smart Watch can be added to one of the memory sockets. This device contains a calendar clock, oscillator, battery and powerfail detect logic in a single 28-pin socket. The chip keeps track of hundreths of seconds, seconds, minutes, hours, days, date of month, and years. Additionally the device allows a 2K or 8K byte CMOS RAM to plug "piggy back" into the Smart Watch and operate transparantly in the same memory space providing both a calendar clock and battery backed memory. For a detailed data sheet and application note call Dallas Semiconductor at 214-450-0400.

Multimodule - A single iSBX Multimodule connector is provided to accomodate a single-wide, 36-pin (8-bit) I/O expansion module. iSBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, graphics controllers, and other special purpose peripheral functions.

Interrupts - An on-board master 82C59A Programmable Interrupt Controller (PIC) provides 8 vectored priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the front plane interrupt connector, the serial channel, 3 counter/timer outputs, 8087 coprocessor, iSBX multimodules, or the STD-8088 backplane signal INTRQ*. All interrupt sources

are jumpered selectable by the user and assigned unique vectors by the PIC.

Five interrupt request lines are available over the front plane and are accessed through the connector. The 8088 parallel interrupt priority scheme is implemented over the front plane of the card for multiple interrupting cards. Alternatively the cascade STD-8088 interrupt priority scheme is implemented by supplying the slave cascade address over the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. The pinout of the external interrupt source connector J3 is as follows.

J3 Pinout - Interrupts

Pin	Signal
2	Int Req 0
4	Int Req 1
6	Int Req 2
8	Int Req 3
10	Int Req 4
1, 3, 5	Ground
7, 9	Ground

I/O - I/O ports are specified by a 16-bit address by the 80C88 for a total system capacity of 64K ports. IOEXP is supported and driven by A8. For the lower 256 port addresses, IOEXP will be active low when ports 00-FF hex are accessed. This allows I/O mapped boards which only decode 8-bits to be mixed with boards that decode 16-bits.

The LPM-SBC8 onboard I/O mapped devices start at 80 and go through A7 hexadecimal.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

CMOS STD Bus - The LPM-SBC8 is available for the CMOS STD Bus and is designed with high speed, low power CMOS logic devices. CMOS offers a high degree of noise immunity, low power consumption, and a wide temperature range (-40 to +85°C) for use in harsh industrial environments.

4

CMOS STD Bus cards should not be used in terminated backplane systems. The extra capacitive loading of the termination networks degrade system performance. It is recommended that WinSystems' high performance shielded motherboards and card racks be used.

C-THRU-ROM - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C for use with the LPM-SBC8. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

LPM-SBC8 I/O MAP

I/O Port Address (nexadecimal)	Device Register
80	82C54 Counter 0
81	82C54 Counter 1
82	82C64 Counter 2
83	82C54 Mode Control
84	Reserved
85	Reserved
86	Reserved
87	Reserved
88	82C59 ICW/OCW 0
89	82C59 ICW/OCW 1
8A - 8F	Reserved
90	82C52 Data
91	82C52 UCR/USR
92	82C52 MCR
93	82C52 BRSR/MSR
94 - 97	Reserved
98 - 9F	iSBX Module MCS0
A0 - A7	iSBX Module MCS1

SPECIFICATIONS

Electrical

Bus Interface: CMOS STD-8088 compatible.

System Clock: 5.0 or 8.0 MHz

Serial Interface: RS-232 and RS-422/485

Interrupts: TTL input level with 10K ohm pull-up resistors

Timers: 5 74LS TTL loads

$Vcc = +5V \pm 10\%$ at 105 mA typ.

Without RS-422 Drivers:
$Vcc = +5V \pm 10\%$ at 45 mA typ.

Memory

Addressing: 1 Megabyte

Capacity: Supports 8K, 16K, and 32K, and 64K byte 28-pin RAM, ROM, EPROM, and EEPROMs.

Mechanical

Dimensions: Meets all STD Bus mechanical specifications except I/O connectors extend beyond card edge: 4.5 x 7.0 x 0.6 inches

Connectors

Serial I/O: 14-pin 0.100" grid

Interrupts: 10-pin 0.100" grid

Counter/timer: 10-pin 0.100" grid

iSBX Multimodule: 36-pin 0.100" dual row female

Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40° to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC8-5 CMOS STD-8088 Single Board Multifunction Computer and manual; 5 MHz.

LPM-SBC8-8 CMOS STD-8088 Single Board Multifunc tion Computer and manual; 8 MHz.

CTR-M-SBC8 Remote C Symbolic Debugger development kit for Microsoft C

WinSystems, Inc.

FEATURES

- 8088 Multifunction Single Board Computer
- Direct addressing to 1 Mbyte
- 8087 Numeric Coprocessor socket
- Choice of CPU speeds (5 & 8 MHz)
- Optional debug monitor PROM
- Two 28 pin bytewide memory sockets supporting RAM, ROM, EPROM, and EEPROMs
- Serial RS-232 or RS-422/485 serial interface with diagnostic loopback capability
- Programmable baud rate from 50 to 38.4 Kbaud
- 8259A Programmable interrupt controller with 8 interrupt sources
- Supports cascadeable or front plane interrupts
- iSBX Multimodule expansion connector
- Three 16-bit Counter/Timer channels (8254A)
- Optional 8080 software emulation
- Precision power-on/brown out detect circuit
- CMOS STD Bus version available: LPM-SBC8
- Operational temperature range: 0 to +60°C
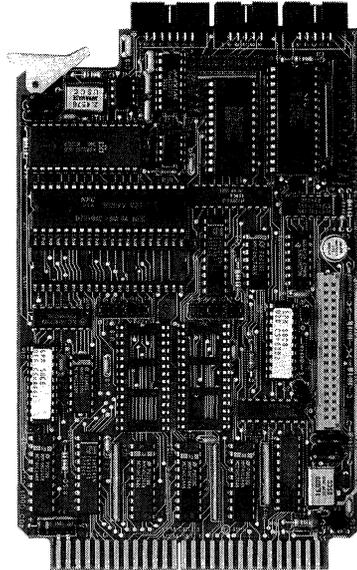
The MCM-SBC8 is a powerful, multifunction 8088 STD Bus single board computer combining the CPU, 2 28-pin memory sockets, 8087 socket, 3 counter/timers, serial I/O, interrupt controller, precision powerfail/brown out reset circuit, watchdog timer and full STD Bus interface onto a single card. Furthermore, an iSBX multimodule connector is incorporated on the card to support expansion modules mounted on the board.

* ACTIVE LOW LOGIC   SHADING INDICATES SOCKETS ONLY
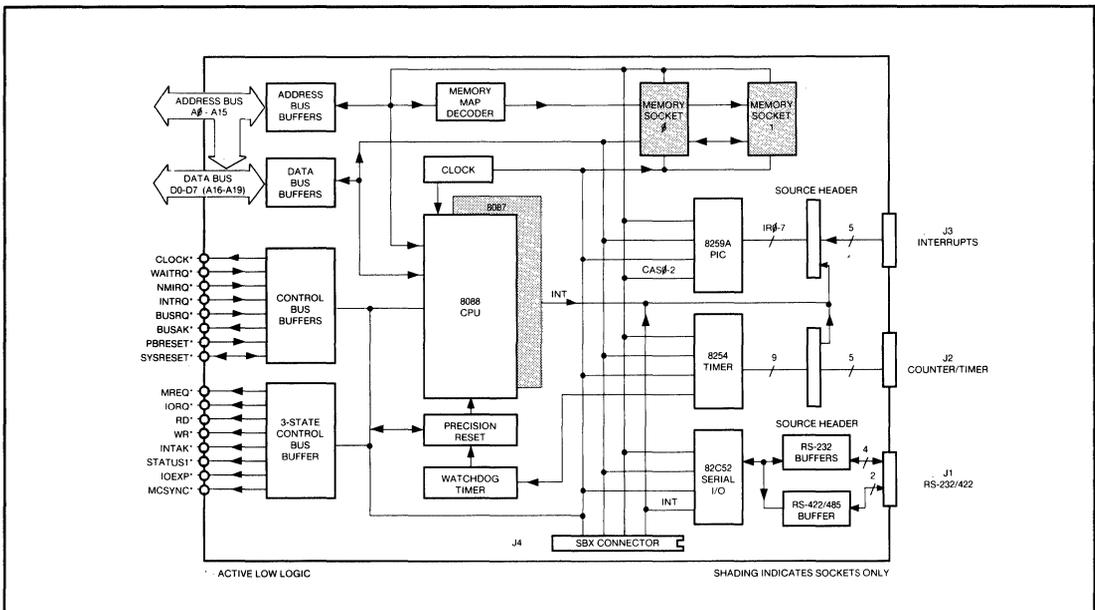
FUNCTIONAL CAPABILITY

Processor - The MCM-SBC8 incorporates the popular 16-bit 8088 processor which has a 20-bit direct address capability of 1 Mbyte. The processor is fully buffered and operates at either 5 or 8 MHz.

A NEC V20 processor can optionally be installed for improved performance. The V20 executes faster than the 8088 because of its pipelined architecture. Also the processor has a powerful instruction superset including bit processing, packed BCD operations, and 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high-speed multiplication/division instructions.

The V20 will also operate in the 8080 emulation mode. In this mode, the 8080 instruction set is emulated by the V20 allowing migration of previously developed 8-bit software to this board.

SLEEP Mode - The MCM-SBC8 with the NEC V20 has a low power standby mode to reduce power consumption. The standby mode is available in both the native 8088 and 8080 emulation mode. The processor stops in a known condition with only the internal oscillator and standby release circuits operational. The mode is released by detection of a SYSRESET*, INTRQ* or NMIRQ* external interrupt.

8087 Coprocessor - The SBC8 card is configured for the maximum mode in order to support an optional 8087 Coprocessor providing up to 100 times the performance of the CPU alone. It provides arithmetic, logarithmic, exponential, trigonometric, and floating point arithmetic with up to 80-bit results.

Addressing - The 8088 processor supports direct addressing of 1 Mbyte on 20 address lines. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data lines D0 through D3 at the beginning of each memory operation. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. The multiplexing of the extra address lines on the data bus requires no additional CPU overhead and is transparant and compatible to other I/O mapped cards. The SBC8 conforms to the STDMG STD-8088 specifications.

Memory - Two JEDEC standard 28-pin bytewide sockets are provided to allow the use of RAM, ROM, EPROM or EEPROMs. The sockets are configurable for 8K, 16K, or 32K byte RAMs and up to 64 Kbyte EPROM devices. The first socket is configured to accept an EPROM mapped at FFFF0h for the 8088's power on restart address. The second socket is mapped to begin at 00000h to support the 8088 interrupt vector table structure and user application code. The sockets can be remapped if different options are required.

MEMEX is not used and is open.

Communications - A fully buffered serial asynchronous channel is implemented with the 82C52 full duplex, programmable communication interface device. The 82C52 contains an independent on-chip software programmable baud rate generator. It has 18 different frequencies that are jumper selectable from 50 through 38.4K bits per second.

In asynchronous mode, the card will work with 5 to 8 bit characters. It will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing. The serial channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream. Also the bidirectional control for the RS-422/485 signals is done by the 82C52. The serial channel status signals can be jumpered to the 8259A to generate vectored interrupts.

Both RTS and CTS modem handshake lines are provided in addition to the transmit and receive lines. Jumper options permit configuration of the serial I/O as either DCE or DTE. Both the RS-232 and RS-422/485 interface levels are brought out to a 14-pin connector. This allows easy connections to flat cables with 25 pin RS-232 "D" type connectors.

J1 Pinout - SIO Channel

Pin	Signal
1, 7	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
14	RS422/485 Data +
15	RS422/485 Data -

Counter/Timers - There are three independent software programmable 16-bit counter/timers available through the 8254 to solve most of the timing problems in microcomputer systems design. Six flexible timer modes allow the 8254 to be used as an event counter, time delay, multitasking executive time base, programmable one-shot, clock, motor controller, square wave generator, baud rate generator, and other applications. The individual counter channels can be cascaded for longer count sequences.

The outputs of each counter/timer can be jumpered to the 8259A PIC to generate vectored interrupts. The Clock, Gate and Output of all 3 counter/timers are accessable through jumper options and available for external use through J2, a 10 pin connector. The standard connector configuration is as follows:

J2 Pinout - Counter/Timers

Pin	Signal
2	CLK 0 Input
4	Gate 0
6	CLK 1 Input
8	Gate 1
10	CLK 2 Input
1,3,5	Ground
7,9	Ground

Watchdog Timer - Counter 2 of the 8254A has a special configuration option to allow its output to serve as a retriggerable watchdog timer. The counter output can be jumpered to PBRESET* to automatically reset the processor after a programmable period of time. This is important for use in remote and unattended applications.

Real-Time Clock - An optional Dallas Semiconductor Smart Watch can be added to one of the memory sockets. This device contains a calendar clock, oscillator, battery and powerfail detect logic in a single 28-pin socket. The chip keeps track of hundreths of seconds, seconds, minutes, hours, days, date of month, and years. Additionally the device allows a 2K or 8K byte CMOS RAM to plug "piggy back" into the Smart Watch and operate transparantly in the same memory space providing both a calendar clock and battery backed memory. For a detailed data sheet and application note call Dallas Semiconductor at 214-450-0400.

Multimodule- A single iSBX Multimodule connector is provided to accomodate a single-wide, 36-pin (8-bit) I/O expansion module. iSBX modules are available for implementing serial or parallel I/O, A/D and D/A converters, disk controllers, graphics controllers, and other special purpose peripheral functions.

Interrupts - An on-board master 8259A Programmable Interrupt Controller (PIC) provides 8 vectored priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the front plane interrupt connector, the serial channel, 3 counter/timer outputs, 8087 coprocessor, iSBX multimodules, or the STD-8088 backplane signal INTRQ*. All interrupt sources are jumper selectable by the user and assigned unique vectors by the PIC.

Five interrupt request lines are available over the front plane and are accessed through the connector. The 8088 parallel interrupt priority scheme is implemented over the front plane of the card for multiple interrupting cards. Alternatively the cascade STD-8088 interrupt priority scheme is implemented by supplying the slave cascade address over the STD Bus address lines A8 - A10 during interrupt acknowledge cycles. The pinout of the external interrupt source connector J3 is as follows.

J3 Pinout - Interrupts

Pin	Signal
2	Int Req 0
4	Int Req 1
6	Int Req 2
8	Int Req 3
10	Int Req 4
1, 3, 5	Ground
7, 9	Ground

I/O - I/O ports are specified by a 16-bit address by the 8088 for a total system capacity of 64K ports. IOEXP is supported and driven by A8. For the lower 256 port addresses, IOEXP will be active low when ports 00-FF hex are accessed. This allows I/O mapped boards which only decode 8-bits to be mixed with boards that decode 16-bits.

The MCM-SBC8 onboard I/O mapped devices start at 80 and go through A7 hexadecimal.

MCM-SBC8 I/O Map

I/O Port Address (hexadecimal)	Device
80	8254 Counter O
81	8254 Counter 1
82	8254 Counter 2
83	8254 Mode Control
84	Reserved
85	Reserved
86	Reserved
87	Reserved
88	8259 ICW/OCW 0
89	8259 ICW/OCW 1
8A-8F	Reserved
90	8252 Data
91	8252 UCR/USR
92	8252 MCR
93	8252 BRSR/MSR
94-97	Reserved
98-9F	iSBX Module MCS0
A0-A7	iSBX Module MCS1

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

C-THRU-ROM - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C for use with the MCM-SBC8. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

SPECIFICATIONS

Electrical

Bus Interface: CMOS STD-8088 compatible.

System Clock: 5.0 or 8.0 MHz

Serial Interface: RS-232 and RS-422/485

Interrupts: TTL input level with 10K ohm pull-up resistors

Timers: 5 74LS TTL loads

Vcc = +5V $\pm$ 5% at 850 mA typ.

Memory

Addressing: 1 Megabyte

Capacity: Supports 8K, 16K, and 32K, and 64K byte 28-pin RAM, ROM, EPROM, and EEPROMs.

Mechanical

Dimensions: Meets all STD Bus mechanical specifications except I/O connectors extend beyond card edge: 4.5 x 7.0 x 0.6 inches

Jumpers: 0.025″ square posts

Connectors

Serial I/O: 14-pin 0.100″ grid

Interrupts: 10-pin 0.100″ grid

Counter/timer: 10-pin 0.100″ grid

iSBX Multimodule: 36-pin 0.100″ dual row female

Environmental

Operating Temperature: 0° to +60°C
Non-condensing relative humidity: 0% to 95%

ORDERING INFORMATION

MCM-SBC8-5 STD-8088 Single Board Multifunction Computer and manual; 5 MHz.

MCM-SBC8-8 STD-8088 Single Board Multifunction Computer and manual; 8 MHz.

CTR-M-SBC8 Remote C Symbolic Debugger development kit for Microsoft C

WinSystems, Inc.

8-Bit Processor Selector Guide

PRODUCT	TECHNOLOGY	CPU	SPEED (MHz)	(EP) ROM KBytes (MAX)	RAM KBytes (MAX)	SERIAL	PARALLEL
LPM-102	CMOS	Z80	2,4,6	64	64	2	—
MCM-102	NMOS/TTL						
LPM-7815	CMOS	80C85	4,6	32	32	—	—
MCM-7815	NMOS/TTL	8085					
LPM-CPU2A	CMOS	Z80A	2,4,6	64	64	—	—
MCM-CPU2A	NMOS/TTL	Z80					
LPM-SBC3	CMOS	Z80	4,6	64	64	2	16
MCM-SBC3	NMOS/TTL						
LPM-SBC5	CMOS	64180	3,6	128	64	4	16
MCM-SBC5	NMOS/TTL						
LPM-SBC6	CMOS	64180	3,6	128	64	2	24
MCM-SBC6	NMOS/TTL						

4

WinSystems®

CMOS STD BUS

LPM-7815
80C85A
CPU Card

FEATURES

- Industry standard 80C85A processor
- Four 28-pin Bytewide sockets supporting RAM's, ROM, and EPROMs
- DMA to onboard memory
- MEMEX memory expansion control
- Compatible memory map options to the Pro-Log 78C05 and 78C15 processor cards
- Access to serial data lines and 5.5, 6.5, and 7.5 interrupts
- Two connectors to support 78C15 and 78C05 pin-outs
- IOEXP jumper option
- Precision power-on/ brown-out reset circuit
- Plug compatible with Pro-Log 78C15
- Temperature range: -40° to +85°C
- Single .+5 volt supply

The LPM-7815 is a powerful, compact STD Bus 80C85A single board computer with four versatile 28-pin JEDEC memory sockets for RAMs, ROMs and/or EPROMs. WinSystems has implemented the mapping that allows the board to be configured to emulate the same system memory map as the Pro-Log 78C05 and 78C15 processor cards. This flexibility permits the LPM-7815 to be an upward compatible replacement to these cards using the latest in high density memory technology. Any combination of RAM or EPROM
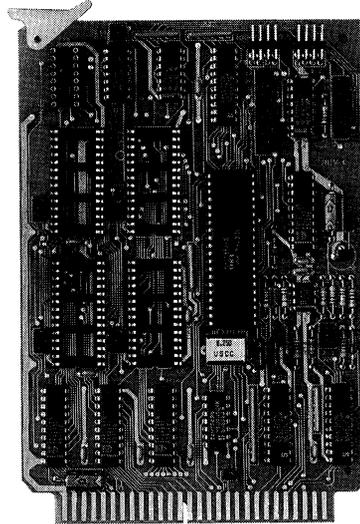
devices can be supported within the memory sockets. Also two external connectors are on the board to provide I/O for either 78C05 or 78C15 applications. The board is available in both NMOS and CMOS versions.

SHADING INDICATES SOCKETS ONLY
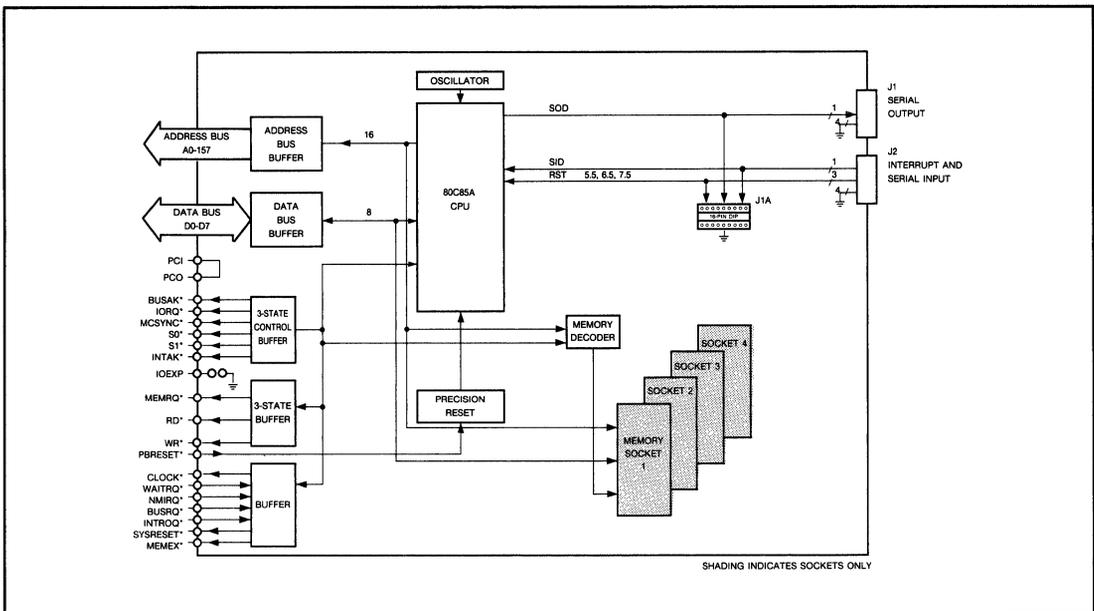
FUNCTIONAL CAPABILITY

Processor - The 78C15 is a fully buffered and fully expandable 80C85A processor card operating at either 6.144 or 4.0 MHz. Address, data, and control busses have been made bidirectional to allow external masters to have direct access to the onboard memory devices.

It implements the serial data lines SID and SOD from the processor, buffers and outputs them to two connectors on the top of the board.

Interrupts - Interrupts are supported with the RST 5.5, 6.5, and 7.5 priority interrupt inputs. These three inputs are buffered from the external connector and can be used to cause general purpose maskable interrupts in the 80C85A processor.

The LPM-7815 has two connectors for the serial I/O and interrupt lines. Since the WinSystems LPM-7815 combines both the features of the 78C05 and 78C15 processor cards, two different connector types are installed on the card. Connectors J1 and J2 are identical to the corresponding 78C15 right angle male header connectors. J1A is identical to the 78C05 machine tool DIP socket connector J1.

Memory - The memory consists of four 28-pin sockets capable of supporting RAM, ROM, or EPROMs. In 78C15 applications, they can support up to 32K bytes consisting of any combination of four 8K x 8 devices and it duplicates the memory map exactly. Each socket can be individually jumpered to address 8K bytes in the upper or lower 32K address space.

This board can also accomodate the 78C05 memory map as well. The 78C05 memory map is divided into four 16K byte quadrants. Only EPROMs can be placed in the lower 8K bytes of any quadrant and only 4K of RAM can be placed in the remaining upper 8K on the Pro-Log 78C05. WinSystems does not impose this limitation on the system memory map and allows any combination of RAM/ROM devices to be placed in the sockets. WinSystems decodes the quadrant into 4K byte segments for each socket which allows higher density memory devices to be used. Since it is becoming more difficult to obtain 2K x 8 EPROM memory devices, this memory map allows the 78C05 to use 2732 type devices.

Unused sockets can be disabled, releasing space for use by other memory devices not on this card.

The polarity of the MEMEX signal is jumper selectable and can be active high, active low or not connected to the Bus. MEMEX is active when on board memory is being accessed.

Reset - A precision power fail detect sequencer is used to detect both power up and power fail conditions. In the event of a voltage out of tolerance condition, the system will automatically generate a PBRESET*.

SPECIFICATIONS

Electrical

Systems Clock: 6.250 MHz or 6.144 MHz or 4.0 MHz
Serial Interface: TTL levels
Interrupts: TTL levels

Vcc = +5V $\pm$ 10% at 15 mA typ.

Memory

Capacity: Supports 2K, 4K, or 8K byte RAM, ROM, and
       EPROMs

Mechanical

Dimensions: Meets all STD Bus mechanical dimensions
Jumpers: 0.025" square posts

Connectors

System: 56-pin dual 0.125 inch centers
I/O: Two 8-pin right angle on 0.100 grid
     16-pin DIP socket

Environmental

Operating Temperature: $-40°$ to $+85°C$
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7815-0	6.25 MHz 80C85A based single board computer with manual
LPM-7815-1	6.144 MHz 80C85A based single board computer with manual
LPM-7815-2	4.0 MHz 80C85A based single board computer with manual

WinSystems, Inc.

FEATURES

- Industry standard 8085A processor
- Four 28-pin Bytewide sockets supporting RAM's, ROM, and EPROMs
- DMA to onboard memory
- MEMEX memory expansion control
- Compatible memory map options to the Pro-Log 7801, 7805, and 7815 processor cards
- Access to serial data lines and 5.5, 6.5, and 7.5 interrupts
- Two connectors to support 7815, 7805 and 7801 pin-outs
- IOEXP jumper option
- Precision power-on/ brown-out reset circuit
- Plug compatible with Pro-Log 7815
- Single +5 volt supply
- CMOS STD Bus version available (LPM-7815)

The MCM-7815 is a powerful, compact STD Bus 8085A single board computer with four versatile 28-pin JEDEC memory sockets for RAMs, ROMs and/or EPROMs. WinSystems has implemented the mapping that allows the board to be configured to emulate the same system memory map as the Pro-Log 7801, 7805, and 7815 processor cards. This flexibility permits the MCM-7815 to be an upward compatible replacement to these cards using the latest in high density memory technology. Any combination of RAM or EPROM de-

vices can be supported within the memory sockets. Also two external connectors are on the board to provide I/O for either 7805 or 7815 applications. The board is available in both NMOS and CMOS versions.
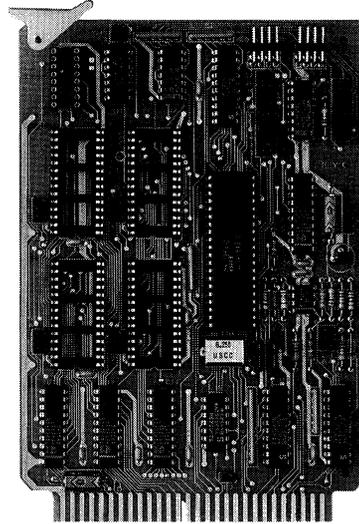
SHADING INDICATES SOCKETS ONLY
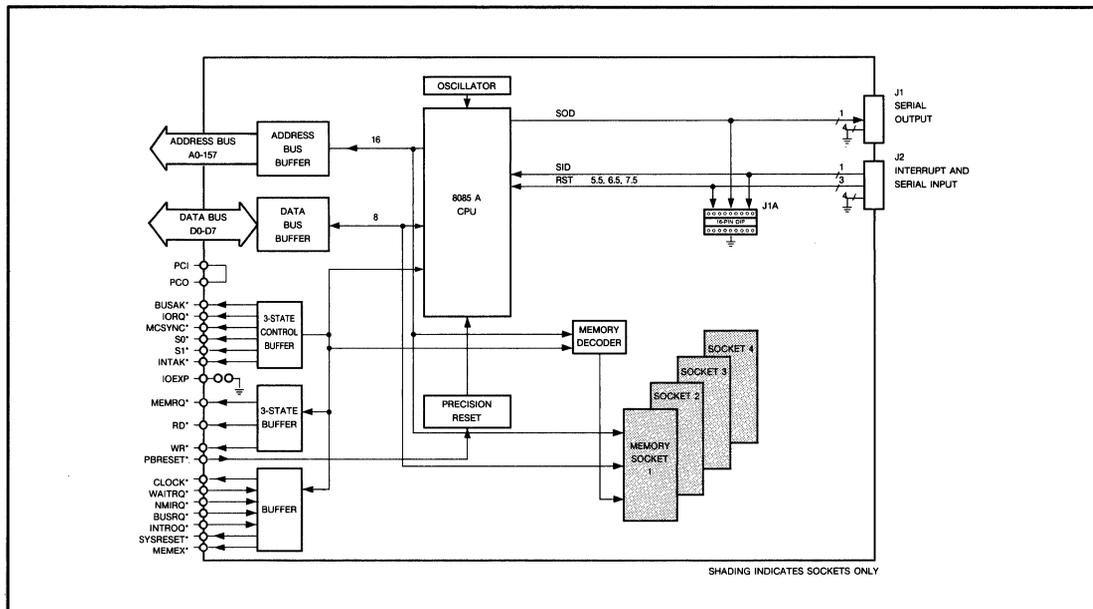
FUNCTIONAL CAPABILITY

Processor - The 7815 is a fully buffered and fully expandable 8085A processor card operating at either 6.144 or 6.250 MHz. Address, data, and control busses have been made bidirectional to allow external masters to have direct access to the onboard memory devices.

It implements the serial data lines SID and SOD from the processor, buffers and outputs them to two connectors on the top of the board.

Interrupts - Interrupts are supported with the RST 5.5, 6.5, and 7.5 priority interrupt inputs. These three inputs are buffered from the external connector and can be used to cause general purpose maskable interrupts in the 8085A processor.

The 7815 has two connectors for the serial I/O and interrupt lines. Since the WinSystems MCM-7815 combines both the features of the 7805 and 7815 processor cards, two different connector types are installed on the card. Connectors J1 and J2 are identical to the respective 7815 right angle male connectors. J1A is identical to the 7805 machine tool DIP socket connector J1.

Memory - The memory consists of four 28-pin sockets capable of supporting RAM, ROM, or EPROMs. In 7815 applications, they can support up to 32K bytes consisting of any combination of four 8K x 8 devices and it duplicates the memory map exactly. Each socket can be individually jumpered to address 8K bytes in the upper or lower 32K address space.

This board can also accomodate the 7805 memory map as well. The 7805 memory map is divided into four 16K byte quadrants. Only EPROMs can be placed in the lower 8K bytes of any quadrant and only 4K of RAM can be placed in the remaining upper 8K on the Pro-Log 7805. WinSystems does not impose this limitation on the system memory map and allows any combination of RAM/ROM devices to be placed in the sockets. WinSystems decodes the quadrant into 4K byte segments for each socket which allows higher density memory devices to be used. Since it is becoming more difficult to obtain 2K x 8 EPROM memory devices, this memory map allows the 7805 to use 2732 type devices.

Unused sockets can be disabled, releasing space for use by other memory devices not on this card.

The polarity of the MEMEX signal is jumper selectable and can be active high, active low or not connected to the Bus. MEMEX is active when on board memory is being accessed.

Reset - A precision power fail detect sequencer is used to detect both power up and power fail conditions. In the event of a voltage out of tolerance condition, the system will automatically generate a PBRESET*.

SPECIFICATIONS

Electrical

Systems Clock: 6.144 MHz or 6.250 MHz
Serial Interface: TTL levels
Interrupts: TTL levels

Vcc = +5V ± 5% at 525 mA typ.

Memory

Capacity: Supports 2K, 4K, or 8K byte RAM, ROM, and EPROMs

Mechanical

Dimensions: Meets all STD Bus mechanical dimensions
Jumpers: 0.025" square posts

Connectors

System: 56-pin dual 0.125 inch centers
I/O: Two 8-pin right angle on 0.100 grid 16-pin DIP socket

Environmental

Operating Temperature: 0° to +65°C

Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-7815-0	6.25 MHz 8085A based single board computer with manual
MCM 7815-1	6.144 MHz 8085A based single board computer with manual

WinSystems, Inc.

WinSystems®

STD BUS

LPM-102
CMOS Z80
Single Board Computer

FEATURES

- Complete CMOS STD Bus Z80A Single Board Computer
- 4 MHz operation
- Three 28-pin Bytewide sockets for up to 64Kbytes of RAM, ROM, EPROM, EEPROM, or Dallas Semi-conductor BRAMs
- 8 individual selectable memory maps
- DMA to on board memory
- Two independent serial I/O Channels (Z80-SIO) with handshake
- Async baud rate software selectable to 9600 bps
- Each channel capable of synchronous or asynchronous operation
- LED indicators on data lines
- Four independent counter/timers on board (Z80-CTC)
- Precision power-on/brown out reset circuit
- Operational Temperature: -40° to +85°C
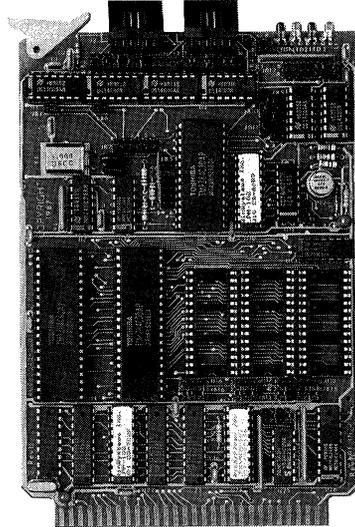
The LPM-102 from WinSystems is an integrated, CMOS Z80A STD BUS single board computer designed for rugged industrial microcomputer applications. The LPM-102 combines a Z80 processor with 2 in-dependent synchronous/asynchronous RS-232 chan-nels, a four channel counter/timer, three 28-pin byte-wide sockets and a precision powerfail reset circuit on a single CMOS STD Bus card.

FUNCTIONAL CAPABILITY

Processor - The LPM-102 uses the industry standard CMOS Z80 operating at 2.4576 MHz. The CPU will run at 6 MHz. Contact the factory for further informa-

SHADING INDICATES SOCKETS ONLY
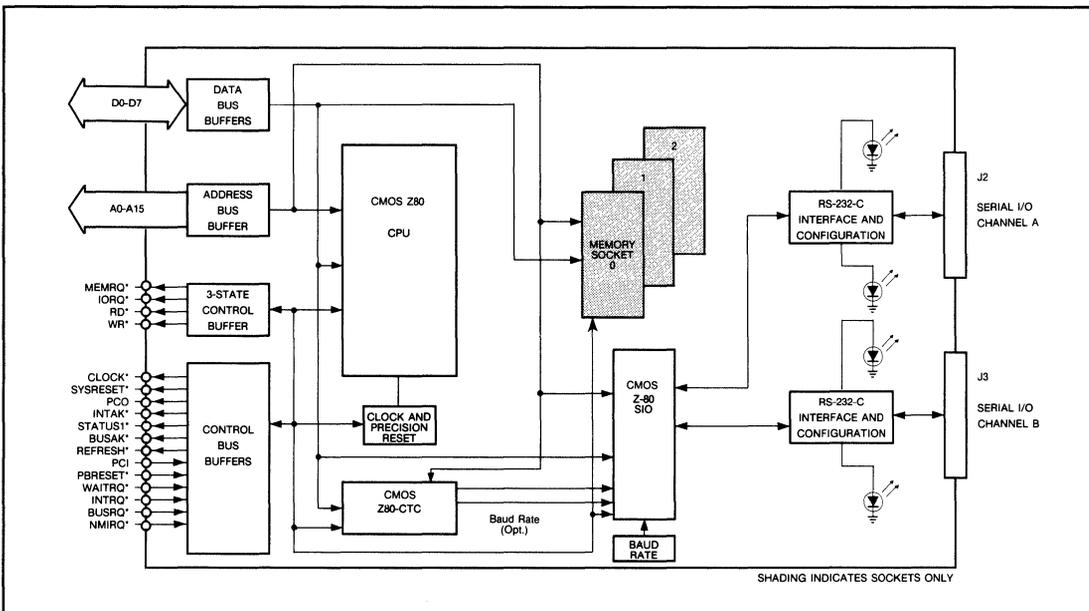
tion. It supports all 3 interrupt modes plus non maskable interrupt (NMI) for maximum system performance.

Memory - Three JEDEC 28-pin bytewide memory sockets are provided with 8 hardware selectable memory maps. The memory sockets will support 2K, 4K, 8K, 16K, or 32K byte RAM, EPROM, and EEPROM devices. It will support the Dallas Semiconductor battery backed RAMs. Also one socket will support a 64Kbyte EPROM. A control register allows the on board memory to be disabled for memory overlay applications. The LPM-102 supports DMA to on board memory.

Serial I/O - Two full duplex RS-232-C serial channels are provided with the Z80-SIO. This device supports all common asynchronous and synchronous protocols, byte or bit oriented such as SDLC, BiSync, etc.

Individual software selectable baud rates from 50-9600 bits per second are available for each asynchronous channel. The Z80-CTC generates individual programmable baud rates for each channel for both asynchronous and synchronous protocols.

Each channel is capable of full duplex asynchronous or synchronous operation jumper configurable as either Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) with modem handshake lines (RTS, CTS, DTR, and DSR). Both channels have jumper selectable LED's on the transmit and receive data lines for visual status.

Counter/Timers - A Z80-CTC provides 4 independent channels for counting, timing and baud rate generation for the serial channels. It can be used to generate real time clocks or other counting functions. The counters are cascadeable for longer count sequences.

Real Time Clock - The LPM-102 can optionally be populated with a Dallas Semiconductor DS-1216 SmartWatch. The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The SmartWatch accepts either 24 or 28-pin JEDEC Bytewide memory devices to be plugged into its socket. Then the DS-1216 plugs directly into one of the memory sockets on board the LPM-102. This permits full utilization of all the memory sockets while having a transparent battery backed timekeeping function.

WinSystems, Inc.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit also inhibits the processor's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations. A reset address of either 0000h or E000h may be selected.

SPECIFICATIONS

Electrical

System Clock: 2.4576 MHz, 4 MHz, 6 MHz

$Vcc = +5VDC \pm 10\%$ at 50 mA typ., 75 mA max.
$= +12\ VDC \pm 10\%$ at 1.6 mA typ., 5 mA max.
$= -12\ VDC \pm 10\%$ at 1.6 mA typ., 5 mA max.

Memory

Capacity: Three 28-pin JEDEC sockets. Supports 8K, 16K, 32K and 64K (socket 1 only) bytes of RAM, ROM, EPROM, EEPROM or battery backed RAM.

Memory map: 6 standard memory decoding configurations plus 2 user programmable options

I/O

Ports: Z80-CTC and -SIO reserved
7Ah to 7Fh and BCh to BFh

Counter/Timer: Four 8-bit timers with prescalers

Serial I/O: RS-232-C on both channels
Baud rate from 110 to 9600 bps

Mechanical

Dimensions: Meets all STD Bus general mechanical specifications; 4.5 x 6.5 inches

Connectors

System: 56-pin dual on 0.125" centers
Serial I/O: Two 12-pin on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-102-2   2.4576 MHz CMOS SBC
LPM-102-4   4 MHz LPM-102
LPM-102-6   6 MHz LPM-102

WinSystems®
## STD BUS

FEATURES

- Complete STD BUS Z80 Single Board Computer
- 4 MHz operation, 6 MHz optional
- Three 28-pin Bytewide sockets for up to 64K bytes of RAM, ROM, EPROM, EEPROM, or Dallas Semiconductor BRAMs
- 8 individual selectable memory maps
- DMA to on board memory
- Two independent serial I/O Channels (Z80-SIO) with handshake
- Async baud rate software selectable to 19.2Kb
- Each channel capable of synchronous or asynchronous operation
- LED indicators on data lines
- Four independent counter/timers on board (Z80-CTC)
- Precision power-on/brown out reset circuit
- Replaces DY-4 DSTD-102
- Optional CMOS version: LPM-102

The MCM-102 from WinSystems is an integrated, Z80 STD. Bus single board computer designed for rugged industrial microcomputer applications. The MCM-102 combines a Z80 processor with 2 independent synchronous/asynchronous RS-232 channels, a four channel counter/timer, three 28-pin bytewide sockets and a precision powerfail reset circuit on a single STD Bus card.
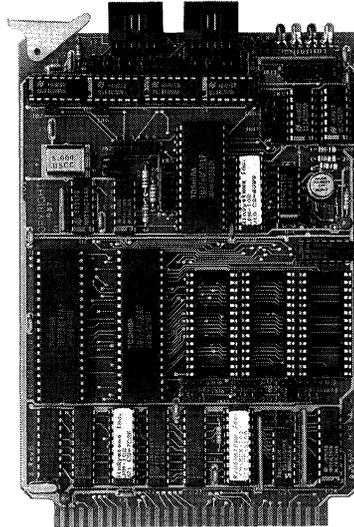
FUNCTIONAL CAPABILITY

Processor - The MCM-102 uses the industry standard Z80 operating at 4 MHz with 6 MHz optional. It sup-
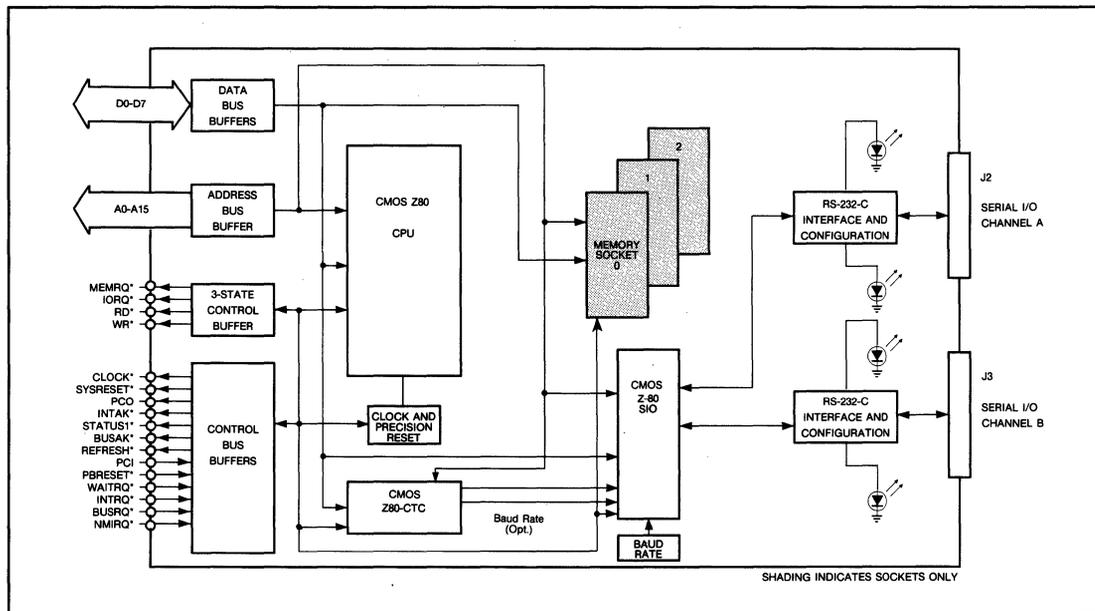
SHADING INDICATES SOCKETS ONLY

ports all 3 interrupt modes plus nonmaskable interrupt (NMI) for maximum system performance. It also generates the DRAM Refresh signal automatically. This card replaces the DY-4 DSTD-102.

Memory - Three JEDEC 28 pin bytewide memory sockets are provided with 8 hardware selectable memory maps. The memory sockets will support 2K, 4K, 8K, 16K, or 32K byte RAM, ROM, EPROM, and EEPROM devices. It will support the Dallas Semiconductor battery backed RAMs. Also one socket will support a 64K byte EPROM. A control register allows the on board memory to be disabled for memory overlay applications. The MCM-102 supports DMA to on board memory.

Serial I/O - Two full duplex RS-232-C serial channels are provided with the Z80-SIO. This device supports all common asynchronous and synchronous protocols, byte or bit oriented such as SDLC, Bisync, etc.

Individual software selectable baud rates from 50-19200 bits per second are available for each asynchronous channel. Either a separate baud rate generator or the Z80-CTC can provide the input clock.

Each channel is capable of full duplex asynchronous or synchronous operation, jumper configurable as either Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) with modem handshake lines (RTS, CTS, DTR, and DSR). Both channels have jumper selectable LED's on the transmit and receive data lines for visual status.

Counter/Timers - A Z80-CTC provides 4 independent channels for counting, timing and baud rate generation for the serial channels. It can be used to generate real time clocks or other counting functions. The counters are cascadeable for longer count sequences.

Real Time Clock - The MCM-102 can optionally be populated with a Dallas Semiconductor DS-1216 Smart-Watch. The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The SmartWatch accepts either 24 or 28-pin JEDEC Bytewide memory devices plugged into its socket. Then the DS-1216 plugs directly into one of the memory sockets onboard the MCM-102. This permits full utilization of all the memory sockets while having a transparent battery backed timekeeping function.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc status.

Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit also inhibits the processor's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations. A reset address of either 0000h or E000h may be selected.

SPECIFICATIONS

Electrical

System Clock: 4.0 MHz or 6 MHz.

Memory

Capacity: Three 28-pin JEDEC sockets. Supports 8K, 16K, 32K and 64K (socket 1 only) bytes of RAM, ROM, EPROM, EEPROM or battery backed RAM.

Memory map: 6 standard memory decoding configurations plus 2 user programmable options

I/O

Ports: Z80-CTC and -SIO reserved 7Ah to 7Fh and BCh to BFh

Counter/Timer: 4 cascadeable 8-bit timers with prescalers

Serial I/O: RS-232-C on both channels Baud rate from 110 to 19200 bps

Vcc = +5VDC $\pm$ 5% at 750 mA typ., 975 mA max.
= +12 VDC $\pm$ 10% at 50 mA typ., 75 mA max.
= -12 VDC $\pm$ 10% at 50 mA typ., 75 mA max.

Mechanical

Dimensions: 4.5 x 6.5 inches
Connectors

System: 56-pin dual on 0.125" centers
Serial I/O: Two 12-pin on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-102-4   4.0 MHz SBC with operations manual

MCM-102-6   6.0 MHz with operations manual

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

WinSystems®

CMOS STD BUS

FEATURES

- Z80 CPU at 2.5 and 4.0 MHz
- Six 28-pin Bytewide sockets support up to 64K bytes of memory in various combinations of RAM, EPROM, EEPROM and BRAM
- No external memory boards required
- 8 individual selectable memory maps
- 4 independent cascadeable counter/timers (Z80-CTC)
- Jumper selectable wait state generator
- Jumper selectable reset address
- Precision power on reset/brown out detect circuit
- Extended temperature operation: -40°C to +85°C
- Single +5 volt supply

The LPM-CPU2A is a CMOS STD Bus Z80 CPU featuring six 28-pin memory sockets that hold up to 64K bytes of memory in various combinations of RAM, ROM, EPROM, EEPROM, and battery backed RAM. This eliminates the need for external memory boards. A programmable, four channel, cascadeable Counter/Timer is also included on board.

FUNCTIONAL CAPABILITY

Processor - The LPM-CPU2A uses the industry standard Z80 operating at 2.5 or 4.0 MHz. It supports all 3 interrupt modes plus nonmaskable interrupt (NMI). It generates the Dynamic RAM Refresh signal automati-

cally. Refresh occurs during each OP code fetch cycle and is transparent to system throughput.

Memory - Six 28-pin bytewide memory sockets are
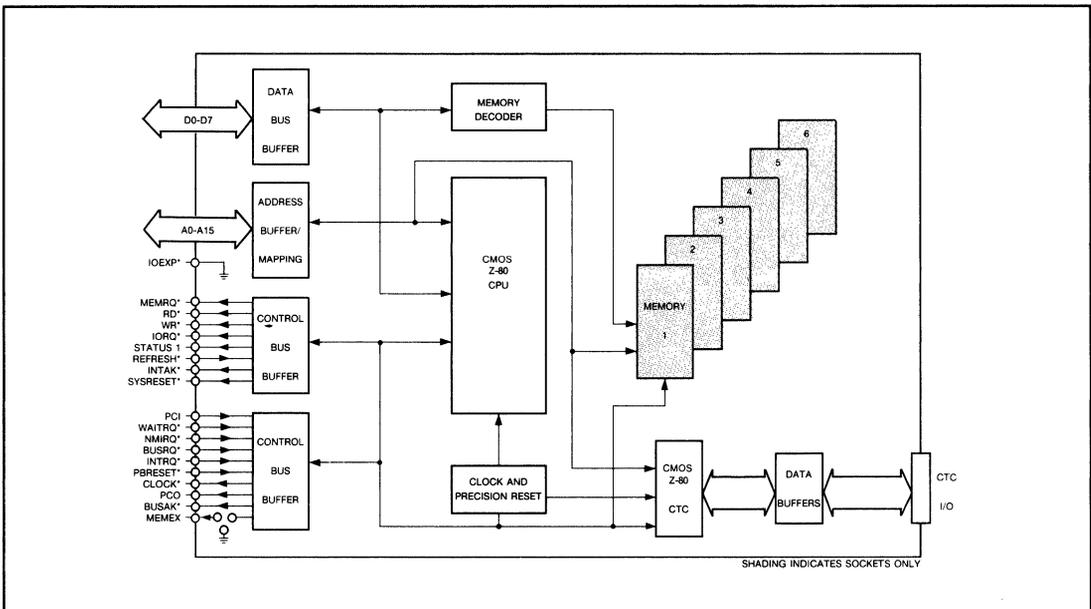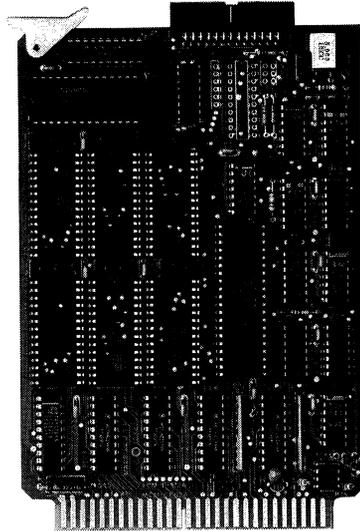
SHADING INDICATES SOCKETS ONLY

provided that hold up to 64K bytes of memory eliminating the need for external memory boards. The memory sockets support any combination of JEDEC standard 24- or 28-pin 2K, 4K, 8K, and 16K RAM, ROM, EPROM, EEPROM, and Dallas Semiconductor nonvolatile memory modules. Each memory socket can be individually jumper configured for any type of memory device. Also one socket can accept a 32K byte memory device. Eight jumper selectable memory maps are provided standard. WinSystems or the user can optionally custom reprogram the map on any 2K byte boundary.

EEPROMs, the Dallas Semiconductor SmartWatch, and 64K and 256K Nonvolatile Memory Modules can be inserted in the memory sockets. The CPU's write line is inhibited by the powerfail reset circuit to prevent bad data from being written to the devices during Vcc out of tolerance conditions.

A jumper selectable wait state generator circuit is available to ensure sufficient memory access times for slower memory devices.

Counter/Timers - The Z80-CTC provides 4 independent channels for software programmable counting and timing functions. The trigger inputs and zero count outputs are buffered and wired to a 26-pin connector at the top of the board. A strapping option permits cascading of the four CTC channels for longer count sequences.

Real Time Clock - An optional Dallas Semiconductor DS-1216 SmartWatch can be plugged into one of the memory sockets. The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month and year. It permits either 24- or 28-pin memory devices to be plugged into its socket and then the DS-1216 plugs directly into one of the LPM-CPU2A's memory sockets. This permits full utilization of all the memory sockets while having a transparent battery backed timekeeping function.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit inhibits the CPU's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations. A jumper selectable reset address of either 0000h or E000h is provided.

CMOS STD Bus - The LPM-CPU2A is designed with high speed, low power CMOS logic devices which offer a high degree of noise immunity, low power consumption, and a wide operational temperature range.

SPECIFICATIONS

Electrical

System Clock: 2.5 or 4.0 MHz.

Vcc = +5VDC $\pm$ 10% at 35 mA typ., 55 mA max.

Memory

Capacity: Six 28-pin JEDEC sockets. Supports 2K, 4K, 8K, 16K and 32K (socket 1 only) bytes of RAM, ROM, EPROM, EEPROM or battery backed RAM.

Memory map: 6 standard memory decoding configurations plus 2 user programmable options

I/O

Ports: Z80-CTC reserved
7Ah to 7Fh or FCh to FFh

Counter/Timer: 4 cascadeable 8-bit timers with prescalers

Mechanical

Dimensions: Meets all STD Bus general mechanical specifications, 4.5 x 6.5 inches

Connectors

System: 56-pin dual on 0.125" centers
CTC: 26-pin on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-CPU2A-2   2.5 MHz CMOS Z80 CPU

LPM-CPU2A-4   4.0 MHz CMOS Z80 CPU

WINMON80-CPU2 Monitor firmware for the CPU2

WinSystems, Inc.

FEATURES

- Replaces the Mostek MDX-CPU2A and MDX-CPU2B
- Z80 CPU at 2.5, 4.0 and 6.0 MHz
- Six 28-pin Bytewide sockets support up to 64K bytes of memory in various combinations of RAM, EPROM, EEPROM and BRAM
- No external memory boards required
- 8 individual selectable memory maps
- 4 independent cascadeable Counter/Timers (Z80-CTC)
- Jumper selectable wait state generator
- Jumper selectable reset address
- Precision power on reset/brown out detect circuit
- Single +5 volt supply
- Optional CMOS version: LPM-CPU2A

The MCM-CPU2A is a STD Bus Z80 CPU featuring six 28-pin memory sockets that hold up to 64K bytes of memory in various combinations of RAM, ROM, EPROM, EEPROM, and battery backed RAM. This eliminates the need for external memory boards. A programmable, four channel, cascadeable counter/timer is also included on board. The MCM-CPU2A is a functional replacement for the Mostek MDX-CPU2A and MDX-CPU2B.
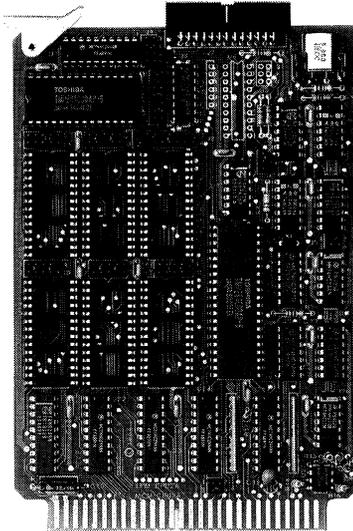
FUNCTIONAL CAPABILITY

Processor - The MCM-CPU2A uses the industry standard Z80 operating at 2.5, 4.0 or 6.0 MHz. It supports all 3 interrupt modes plus nonmaskable interrupt (NMI). It generates the Dynamic RAM Refresh signal automatically. Refresh occurs during each OP code fetch cycle and is transparent to system throughput.

4

SHADING INDICATES SOCKETS ONLY
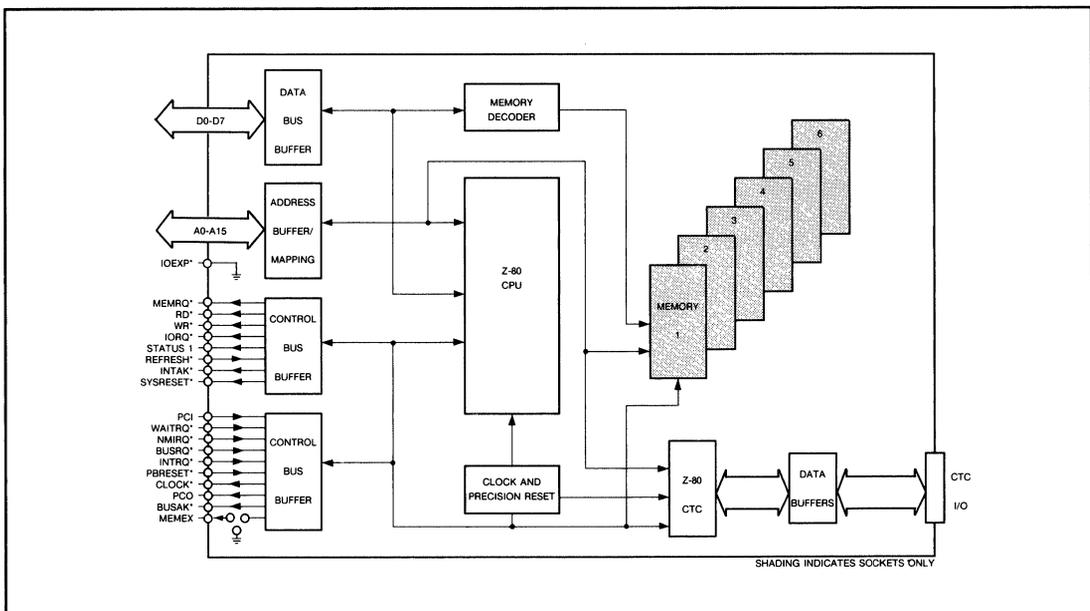
The MCM-CPU2A replaces the Mostek MDX-CPU2A and -CPU2B.

Memory - Six 28-pin bytewide memory sockets are provided that hold up to 64K bytes of memory eliminating the need for external memory boards. The memory sockets support any combination of JEDEC standard 24- or 28-pin 2K, 4K, 8K, and 16K RAM, ROM, EPROM, EPROM, and Dallas Semiconductor nonvolatile memory modules. Each memory socket can be individually jumper configured for any type of memory device. Also one socket can accept a 32K byte memory device. Eight jumper selectable memory maps are provided standard. WinSystems or the user can optionally custom reprogram the map on any 2K byte boundary.

EEPROMs, the Dallas Semiconductor SmartWatch, and 64K and 256K Nonvolatile Memory Modules can be inserted in the memory sockets. The CPU's write line is inhibited by the powerfail reset circuit to prevent bad data from being written to the devices during Vcc out of tolerance conditions.

A jumper selectable wait state generator circuit is available to ensure sufficient memory access times for slower memory devices.

Counter/Timers - The Z80-CTC provides 4 independent channels for software programmable counting and timing functions. The trigger inputs and zero count outputs are buffered and wired to a 26-pin connector at the top of the board. A strapping option permits cascading of the four CTC channels for longer count sequences.

Real Time Clock - An optional Dallas Semiconductor DS-1216 SmartWatch can be plugged into one of the memory sockets. The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month and year. It permits either 24- or 28-pin memory devices to be plugged into its socket and then the DS-1216 plugs directly into one of the MCM-CPU2A's memory sockets. This permits full utilization of all the memory sockets while having a transparent battery backed timekeeping function.

Reset - A precision band gap voltage comparator circuit is used to determine the Vcc status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit inhibits the CPU's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations. A jumper selectable reset address of either 0000h or E000h is provided.

CMOS STD Bus - For extended temperature or low power applications, the MCM-CPU2A is available as the LPM-CPU2A for the CMOS STD Bus.

SPECIFICATIONS

Electrical

System Clock: 2.5, 4.0, or 6 MHz.
Vcc = +5VDC ± 5% at 750 mA typ., 975 mA max.

Memory

Capacity: Six 28-pin JEDEC sockets. Supports 2K, 4K, 8K, 16K and 32K (socket 1 only) bytes of RAM, ROM, EPROM, EEPROM or battery backed RAM.

Memory map: 6 standard memory decoding configurations plus 2 user programmable options

I/O

Ports: Z80-CTC reserved
7Ah to 7Fh or FCh to FFh
Counter/Timer: 4 cascadeable 8-bit timers with prescalers

Mechanical

Dimensions: 4.5 x 6.5 inches

Connectors

System: 56-pin dual on 0.125" centers
CTC: 26-pin on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-CPU2A-2   2.5 MHz Z80 CPU

MCM-CPU2A-4   4.0 MHz Z80 CPU

MCM-CPU2A-6   6.0 MHz Z80 CPU

WINMON80-CPU2 Monitor firmware for the CPU2A

WinSystems, Inc.

FEATURES

- 6.144 MHz HD64180 CMOS processor
- Fully Z80 software and interrupt compatible
- High-speed CMOS technology: low power consumption, high noise immunity, wide temperature range
- Additional processor capability: 12 additional instructions including hardware multiply
- On chip MMU for direct addressing to 512K bytes
- Two 28-pin memory sockets support any mix of RAM, ROM, EPROM, and EEPROMs
- 2 channel DMA controller
- Automatic dynamic RAM REFRESH generation
- Memory and I/O Wait state generator
- Two RS-232 serial asynchronous I/O channels (RS-422 on Channel 1) with programmable baud rate generators
- Three 8-bit parallel I/O ports
- Two 16-bit reloadable timers
- Jumper enabled watchdog timer
- Supports Z80 mode 2 vectored interrupts
- Precision power-on reset/brown out detect circuit
- SLEEP, IOSTOP and SYSTEM STOP Mode for very low power operation
- Single +5 volt operation
- Temperature Range: -40°C to +85°C

The LPM-SBC6 is a HD64180 based SBC that offers the benefits of high performance while maintaining compatibility with the large base of industry standard 8080/Z80 8-bit software. The board contains the processor, with 512K bytes of direct memory addressing, hardware multiply, 2 DMA channels, 2 28-pin JEDEC memory sockets, 2 serial I/O channels, three 8-bit parallel I/O channels, two 16-bit timers, watchdog timer, powerfail/brownout reset circuit, and full CMOS STD Bus interface.

4
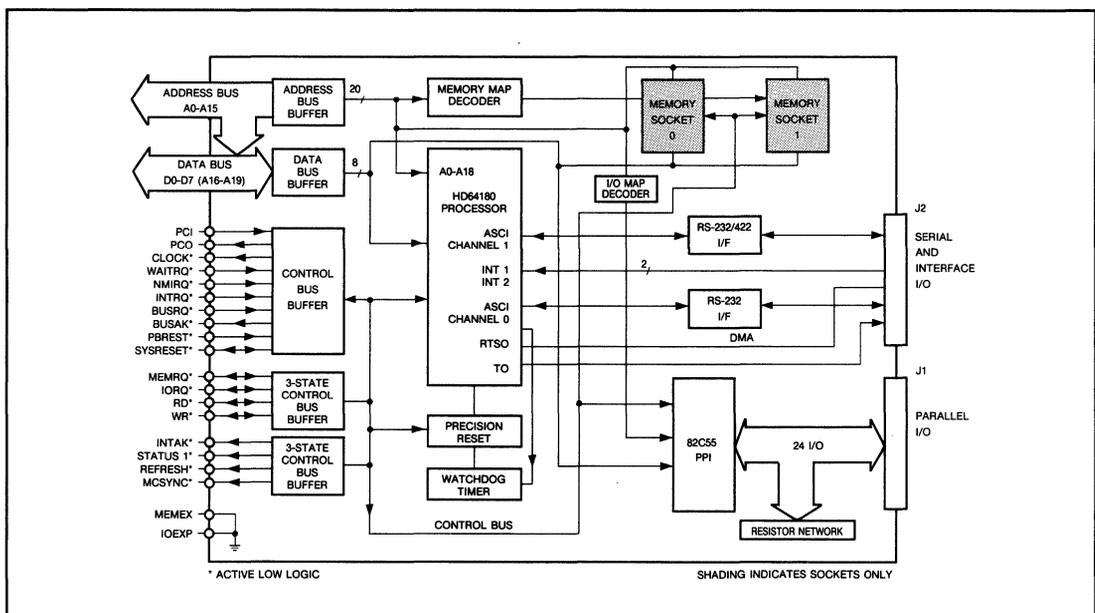
FUNCTIONAL CAPABILITY

Processor - The LPM-SBC6 is designed around the Hitachi HD64180 processor which provides high performance by virtue of its pipelining, enhanced instruction set, on-chip multiplier, and integrated Memory Management Unit (MMU). The CPU is microcoded to implement an upward compatible superset of the 8-bit 8088/Z80 standard software instruction set. Many instructions require fewer clock cycles for execution and twelve new instructions are added. A detailed HD64180 technical manual can be obtained from Hitachi America by calling 1-800-842-9000 and requesting publication U-77.

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both.

The processor, operating at 6.144 MHz, is fully buffered and interfaced to the STD Bus. It is fully mode 2 compatible for vectored interrupts and conforms to STD Z80 timing.

Addressing - The MMU maps the CPU's 64K bytes of logical memory address space into 512K bytes of physical memory space. The MMU organization preserves software object code compatibility while providing extended memory access and uses an efficient "common area - bank area" scheme. The LPM-SBC6 generates a 20-bit address conforming to the STD Bus Multiplexed Memory Addressing scheme. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data bus lines D0 through D3 respectively. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. A19 is not active and wired to ground yielding a total memory address capability of 512K bytes.

Memory - Two JEDEC standard 28-pin memory sockets are provided to allow the use of any mix of RAM's, ROM's, EPROM's, or EEPROM's. These sockets reside in the lower 64K bytes of memory and can accept 8K, 16K, or 32K byte devices per socket. The sockets can be mapped on any 8K byte boundary to cover all the popular memory configurations. The data bus buffers are bidirectional allowing DMA operations to the on-board memory sockets.

DMA - A 2 channel DMA provides high speed Memory-to-Memory and on board Memory-to-I/O transfers. The DMA features edge or level sense request inputs and is programmable for burst or cycle steal transfers. DMA control is accessed through /DREQ0 and /DREQl on pins 11 and 13 of connector J2.

A software programmable memory wait state generator inserts from 0 to 3 wait states automatically during CPU and HD64180 on-chip DMA transfer cycles.

The REFRESH* signal is automatically generated and gated on the STD Bus for dynamic RAMs. Dynamic RAM memory cells will be refreshed regardless of where they reside in the memory map. It can be disabled by a software command for faster processor operation.

MEMEX is not used is and wired to ground.

Serial Communications - Two serial channels are supported on this board. Two independent, full duplex, asynchronous channels (ASCI) are on the HD64180 chip. These are dual UARTs with independent software programmable baud rate generators up to 38.4 Kbps. They can be linked to the processor DMA channel for high speed serial data transfer and to reduce CPU overhead. Channel 1 can be configured for RS-232 or RS-422 levels and Channel 0 is configured for RS-232 levels only. Maxim MAX232 +5 volt only transceivers generate the RS-232 ±10 volt signals using a charge pump voltage converter technology. A RS-422 receiver and transmitter are on board to generate full duplex communications on Channel 1.

J2 Serial and Interface I/O Connector

Pin	Signal
1	Ground
2	Ground
3	RS-232 Transmit Data Channel 0 (TX0)
4	RS-232 Receive Data Channel 0 (RX0)
5	RS-232 Transmit Data Channel 1 (TX0)
6	RS-232 Receive Data Channel 1 (RX0)
7	RS-422/485 Transmit Data Channel 1+
8	RS-422/485 Receive Data Channel 1+
9	RS-422/485 Transmit Data Channel 1-
10	RS-422/485 Receive Data Channel 1-
11	/DREQ0-CKA0
12	T0 Timer Output
13	/DREQ1
14	/TEND0-CKA1
15	/INT1
16	/INT2

Parallel I/O - The LPM-SBC6 contains three 8-bit parallel I/O ports. A 8255A Programmable Peripheral Interface chip supports 24 I/O pins which may be individually programmed in 2 groups of 12 in 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and

interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group for handshaking.

There is direct bit set/reset capability for control application interface requirements. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. Each I/O line has a pull up resistor to keep the input from floating. The 24 lines are connected through Jl, a 26-pin connector.

J1 - Parallel I/O Connector

Pin	Description	Pin	Description
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	Ground	26	Ground

Timers - The LPM-SBC6 contains two separate 16-bit programmable, reloadable, interruptable timers (PRT). Each contains a 16-bit down timer and a 16-bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. PRT channel 1 has a TOUT output pin that is multiplexed with A18 which can be set to toggle. When TOUT is enabled, A18 becomes inoperative yielding a total memory address range of 256K bytes. This output is labeled T0 and is accessable through pin 12 of connector J2.

I/O - The LPM-SBC6's processor generates addressing for a 64K byte I/O space by using a 16-bit I/O address. Most STD I/O cards decode only an 8-bit I/O address. The HD64180 can relocate the base address of on-chip I/O and control registers on any 64 byte boundary.

A software programmable I/O wait state generator inserts from 0 to 6 wait states automatically for CPU and external I/O accesses.

IOEXP is not used and is wired to ground.

Watchdog Timer - A separate hardware retriggerable one-shot watchdog timer is implemented that is capable of automatically resetting the processor after a fixed time interval of approximately 1 second. A jump-er option is available to enable the timer. This circuit is important for use in remote or unattended applications.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a System Reset is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line preventing invalid data from being written to EEPROMs.

Interrupts - The LPM-SBC6 supports all three Z80 interrupt modes and the non maskable interrupt (NMI) as well as the 8 internal HD64180 interrupt sources. Two external interrupt lines, /INT1 and /INT2, are accessible through connector J2.

SLEEP Mode - The LPM-SBC6 has 3 different low power SLEEP modes: SLEEP, IOSTOP, and SYSTEM STOP. The SLEEP mode is entered by the execution of the 2 byte instruction. The processor stops in a known condition with only the internal oscillator running. IOSTOP stops only the internal I/O functions while the CPU continues to function. SYSTEM STOP is the combination of SLEEP and IOSTOP modes. Recovery to normal operation is from detection of an external or internal interrupt or SYSRESET*.

CMOS STD Bus - The LPM-SBC6 card is available for the CMOS STD Bus and is designed with high speed, low power CMOS logic devices. CMOS offers a high degree of noise immunity, very low power consumption, and a wide temperature range (-40°C to +85°C) for use in harsh industrial environments.

CMOS STD Bus cards should not be used in terminated backplane systems. The extra capacitive loading of the termination networks degrade the system performance. It is recommended that WinSystems shielded motherboards and card racks be used.

WINMON 80 is an optional monitor program for the LPM-SBC6 that is used for program development and debugging. It is resident in a 2K byte EPROM and allows the user to develop, load, execute, debug and modify a program. It also allows programs to be developed on CP/M 80 or IBM-PC or equivalent workstations and downloaded to the LPM-SBC6 through a serial port.

4

SPECIFICATIONS

Electrical

System Clock: 6.144 or 3.072 MHz

Bus Interface: STD Z80 compatible.

Serial Interface: RS-232 and RS-422

Vcc = +5V $\pm$ 10% at 90 mA typ.
Without RS-422/485 drivers:
Vcc = +5V $\pm$ 10% at 30 mA typ.

Memory

Addressing: 512K bytes direct addressing

Capacity: Supports 8K, 16K, and 32K byte 28-pin RAM,
ROM, EPROM, and EEPROMs.

I/O Ports

HD64180: DMA channel 0, DMA channel 1, Timer 0,
Timer 1, Interrupt vector, ASCI Channel 0,
ASCI Channel 1, and MMU
00h to 3Fh (Relocateable)
Parallel: FCh to FFh

Mechanical

Dimensions: Meets all STD Bus general mechanical
specifications except I/O connectors
extend beyond card edge; 4.5 x 6.75
inches

Connectors:

Serial I/O: 20-pin 0.100″ grid
Parallel: 26-pin 0.100″ grid
Jumpers: 0.025″ square posts

Environmental

Operating Temperature: -40°C to +85°C
Noncondensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC6-6   6.144 MHz STD Bus Single
Board Multifunction HD64180
Computer with manual

LPM-SBC6-3   3.072 MHz STD Bus Single
Board Multifunction HD64180
Computer with manual

WINMON80-SBC6   Monitor program for the
LPM-SBC6

WinSystems, Inc.

FEATURES

- 6.144 MHz HD64180 processor
- Fully Z80 software and interrupt compatible
- Additional processor capability: 12 additional instructions including hardware multiply
- On chip MMU for direct addressing to 512K bytes
- Two 28-pin memory sockets support any mix of RAM, ROM, EPROM, and EEPROMs
- 2 channel DMA controller
- Automatic dynamic RAM REFRESH generation
- Memory and I/O Wait state generator
- Two RS-232 serial asynchronous I/O channels (RS-422 on Channel 1) with programmable baud rate generators
- Three 8-bit parallel I/O ports
- Two 16-bit reloadable timers
- Jumper enabled watchdog timer
- Supports Z80 mode 2 vectored interrupts
- Precision power-on reset/brown out detect circuit
- SLEEP, IOSTOP and SYSTEM STOP Mode for very low power operation
- Single +5 volt operation
- Optional CMOS version: LPM-SBC6

The MCM-SBC6 is a HD64180 based SBC that offers the benefits of high performance while maintaining compatibility with the large base of industry standard 8080/Z80 8-bit software. The board contains the processor, with 512K bytes of direct memory addressing, hardware multiply, 2 DMA channels, 2 28-pin JEDEC memory sockets, 2 serial I/O channels, three 8-bit parallel I/O channels, two 16-bit timers, watchdog timer, powerfail/brownout reset circuit, and full STD Bus interface.
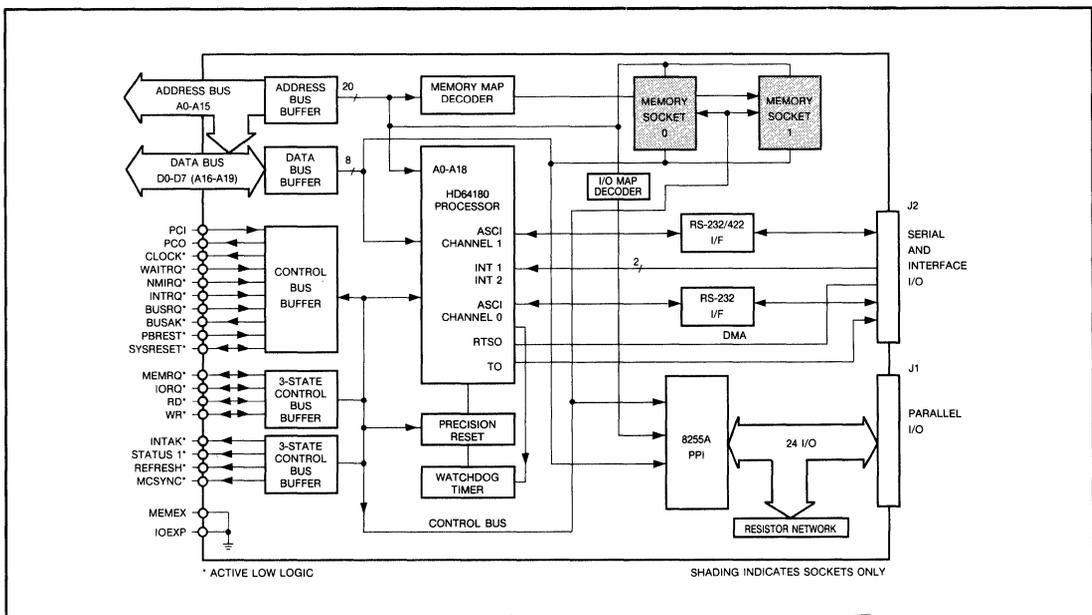
FUNCTIONAL CAPABILITY

Processor - The MCM-SBC6 is designed around the Hitachi HD64180 processor which provides high performance by virtue of its pipelining, enhanced instruction set, on-chip multiplier, and integrated Memory Management Unit (MMU). The CPU is microcoded to implement an upward compatible superset of the 8-bit 8088/Z80 standard software instruction set. Many instructions require fewer clock cycles for execution and twelve new instructions are added. A detailed HD64180 technical manual can be obtained from Hitachi America by calling 1-800-842-9000 and requesting publication U-77.

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both.

The processor, operating at 6.144 MHz, is fully buffered and interfaced to the STD Bus. It is fully mode 2 compatible for vectored interrupts and conforms to STD Z80 timing.

Addressing - The MMU maps the CPU's 64K bytes of logical memory address space into 512K bytes of physical memory space. The MMU organization preserves software object code compatibility while providing extended memory access and uses an efficient "common area - bank area" scheme. The MCM-SBC6 generates a 20-bit address conforming to the STD Bus Multiplexed Memory Addressing scheme. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data bus lines D0 through D3 respectively. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. A19 is not active and wired to ground yielding a total memory address capability of 512K bytes.

Memory - Two JEDEC standard 28-pin memory sockets are provided to allow the use of any mix of RAM's, ROM's, EPROM's, or EEPROM's. These sockets reside in the lower 64K bytes of memory and can accept 8K, 16K, or 32K byte devices per socket. The sockets can be mapped on any 8K byte boundary to cover all the popular memory configurations. The data bus buffers are bidirectional allowing DMA operations to the on-board memory sockets.

DMA - A 2 channel DMA provides high speed Memory-to-Memory and on board Memory-to-I/O transfers. The DMA features edge or level sense request inputs and is programmable for burst or cycle steal transfers. DMA

control is accessed through /DREQ0 and /DREQ1 on pins 11 and 13 of connector J2.

A software programmable memory wait state generator inserts from 0 to 3 wait states automatically during CPU and HD64180 on-chip DMA transfer cycles.

The REFRESH* signal is automatically generated and gated on the STD Bus for dynamic RAMs. Dynamic RAM memory cells will be refreshed regardless of where they reside in the memory map. It can be disabled by a software command for faster processor operation.

MEMEX is not used is and wired to ground.

Serial Communications - Two serial channels are supported on this board. Two independent, full duplex, asynchronous channels (ASCI) are on the HD64180 chip. These are dual UARTs with independent software programmable baud rate generators up to 38.4 Kbps. They can be linked to the processor DMA channel for high speed serial data transfer and to reduce CPU overhead. Channel 1 can be configured for RS-232 or RS-422 levels and Channel 0 is configured for RS-232 levels only. Maxim MAX232 +5 volt only transceivers generate the RS-232 ±10 volt signals using a charge pump voltage converter technology. A RS-422 receiver and transmitter are on board to generate full duplex communications on Channel 1.

J2 Serial and Interface I/O Connector

Pin	Signal
1	Ground
2	Ground
3	RS-232 Transmit Data Channel 0 (TX0)
4	RS-232 Receive Data Channel 0 (RX0)
5	RS-232 Transmit Data Channel 1 (TX0)
6	RS-232 Receive Data Channel 1 (RX0)
7	RS-422/485 Transmit Data Channel 1+
8	RS-422/485 Receive Data Channel 1+
9	RS-422/485 Transmit Data Channel 1-
10	RS-422/485 Receive Data Channel 1-
11	/DREQ0-CKA0
12	T0 Timer Output
13	/DREQ1
14	/TEND0-CKA1
15	/INT1
16	/INT2

Parrallel I/O - The MCM-SBC6 contains three 8-bit parallel I/O ports. A 8255A Programmable Peripheral Interface chip supports 24 I/O pins which may be individually programmed in 2 groups of 12 in 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4

to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group for handshaking.

There is direct bit set/reset capability for control application interface requirements. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. Each I/O line has a pull up resistor to keep the input from floating. The 24 lines are connected through Jl, a, 26 pin connector.

J2 - Parallel I/O Connector

Pin	Description	Pin	Description
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	Ground	26	Ground

Timers - The MCM-SBC6 contains two separate 16-bit programmable, reloadable, interruptable timers (PRT). Each contains a 16-bit down timer and a 16-bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. PRT channel 0 has a TOUT output pin that is multiplexed with A18 which can be set to toggle. When TOUT is enabled, A18 becomes inoperative yielding a total memory address range of 256K bytes. This output is labeled T0 and is accessable through pin 12 of connector J2.

I/O - The MCM-SBC6's processor generates addressing for a 64K byte I/O space by using a 16-bit I/O address. Most STD I/O cards decode only an 8-bit I/O address. The HD64180 can relocate the base address of on-chip I/O and control registers on any 64 byte boundary.

A software programmable I/O wait state generator inserts from 0 to 6 wait states automatically for CPU and external I/O accesses.

IOEXP is not used and is wired to ground.

Watchdog Timer - A separate hardware retriggerable one-shot watchdog timer is implemented that is capable of automatically resetting the processor after a fixed time interval of approximately 1 second. A jumper option is available to enable the timer. This circuit is important for use in remote or unattended applications.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a System Reset is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line preventing invalid data from being written to EEPROMs.

Interrupts - The MCM-SBC6 supports all three Z80 interrupt modes and the non maskable interrupt (NMI) as well as the 8 internal HD64180 interrupt sources. Two external interrupt lines, /INT1 and /INT2, are accessable through connector J2.

SLEEP Mode - The MCM-SBC6 has 3 different low power SLEEP modes: SLEEP, IOSTOP, and SYSTEM STOP. The SLEEP mode is entered by the execution of the 2 byte instruction. The processor stops in a known condition with only the internal oscillator running. IOSTOP stops only the internal I/O functions while the CPU continues to function. SYSTEM STOP is the combination of SLEEP and IOSTOP modes. Recovery to normal operation is from detection of an external or internal interrupt or SYSRESET*.

WINMON 80 is an optional monitor program for the MCM-SBC6 that is used for program development and debugging. It is resident in a 2K byte EPROM and allows the user to develop, load, execute, debug and modify a program. It also allows programs to be developed on CP/M 80 or IBM-PC or equivalent workstations and downloaded to the MCM-SBC6 through a serial port.

CMOS STD Bus - For high temperature or low power applications, the MCM-SBC6 is available as the LPM-SBC6 for CMOS STD Bus use.

4

SPECIFICATIONS

Electrical

System Clock: 6.144 or 3.072 MHz

Bus Interface: STD Z80 compatible.

Serial Interface: RS-232 and RS-422

MCM-SBC6: Vcc = +5V $\pm$ 5% at 750 mA typ., 900 mA max.

Memory

Addressing: 512K bytes direct addressing

Capacity: Supports 8K, 16K, and 32K byte 28-pin RAM, ROM, EPROM, and EEPROMs.

I/O Ports

HD64180: DMA channel 0, DMA channel 1, Timer 0, Timer 1, Interrupt vector, ASCI Channel 0, ASCI Channel 1, and MMU 00h to 3Fh (Relocateable)
Parallel: FCh to FFh

Mechanical

Dimensions: Meets all STD Bus general mechanical specifications except I/O connectors extend beyond card edge; 4.5 x 6.75 inches

Connectors:

Serial I/O: 20-pin 0.100″ grid
Parallel: 26-pin 0.100″ grid

Jumpers: 0.025″ square posts

Environmental

Operating Temperature: 0°C to +70°C

Noncondensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-SBC6-6   6.144 MHz STD Bus Single Board Multifunction HD64180 Computer with manual

MCM-SBC6-3   3.072 MHz STD Bus Single Board Multifunction HD64180 Computer with manual

WINMON80-SBC6   Monitor program for the MCM-SBC6

WinSystems, Inc.

WinSystems®

LPM-SBC5
HD 64180

STD BUS

Single Board Computer

FEATURES

- HD64180 CMOS processor
- Fully Z80 software and interrupt compatible
- High-speed CMOS technology: low power consumption, high noise immunity, wide temperature range
- Additional processor capability: 12 additional instructions including hardware multiply
- On chip MMU for direct addressing to 512 Kbytes
- Two 28-pin memory sockets supporting any mix of RAM, ROM, EPROM, and EEPROMs
- 2 channel DMA controller
- Automatic dynamic RAM REFRESH generation
- Memory and I/O Wait state generator
- Two RS-232 serial asynchronous I/O channels with programmable baud rate generators
- Two Z80 SIO multiprotocol DMA serial channels with one RS-232 or RS-422/485 and one RS-232 interface and modem interface signals
- Two 16-bit reloadable counter/timers
- Jumper enabled watch dog timer
- Supports Z80 mode 2 vectored interrupts
- Power-on reset/brown out detect circuit
- SLEEP, IOSTOP and SYSTEM STOP Mode for very low power operation
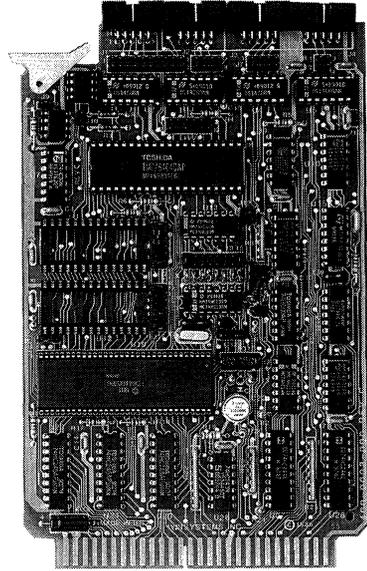
The LPM-SBC5 is a very powerful, compact, multifunction single board computer using the advanced Hitachi 64180 CMOS microcomputer. This processor offers the benefits of high performance, reduced systems cost and very low power operation while maintaining compatibility with the large base of industry standard 8080/Z80 8-bit software. The board

contains the processor, with 512K bytes of direct memory addressing, hardware multiply, 2 DMA channels, 2 28-pin JEDEC memory sockets, 4 serial I/O channels, two 16-bit timers, watchdog timer, powerfail/brownout reset circuit, and full CMOS STD Bus interface.

* = ACTIVE LOW LOGIC   SHADING INDICATES SOCKETS ONLY
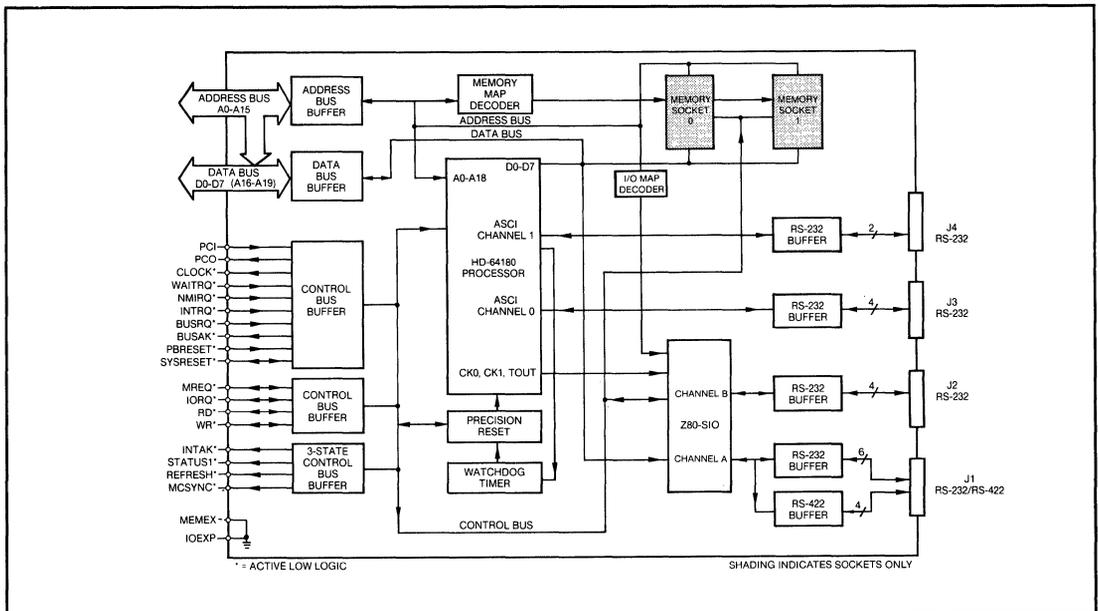
FUNCTIONAL CAPABILITY

Processor - The LPM-SBC5 is designed around the Hitachi HD64180 processor which provides high performance by virtue of its pipelining, enhanced instruction set, on-chip multiplier, and integrated Memory Management Unit (MMU). The CPU is microcoded to implement an upward compatible superset of the 8-bit 8088/Z80 standard software instruction set. Many instructions require fewer clock cycles for execution and twelve new instructions are added. A detailed HD64180 technical manual can be obtained from Hitachi America by calling 1-800-842-9000 and requesting publication U-77.

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both.

The processor, operating at 3.072 MHz, is fully buffered and interfaced to the CMOS STD Bus. It is fully mode 2 compatible for vectored interrupts and conforms to STD Z80 timing.

Addressing - The MMU maps the CPU's 64K bytes of logical memory address space into 512K bytes of physical memory space. The MMU organization preserves software object code compatibility while providing extended memory access and uses an efficient "common area - bank area" scheme. The LPM-SBC5 generates a 20-bit address conforming to the STD Bus Multiplexed Memory Addressing scheme. Address lines A0 through A15 are driven directly onto the CMOS STD Bus. Address lines A16 through A19 are time multiplexed onto data bus lines D0 through D3 respectively. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. A19 is not active and wired to ground yielding a total memory address capability of 512K bytes.

Memory - Two JEDEC standard 28-pin memory sockets are provided to allow the use of any mix of RAM's, ROM's, EPROM's, or EEPROM's. These sockets reside in the lower 64K bytes of memory and can accept 8K, 16K, or 32K byte devices per socket. The sockets can be mapped on any 8K byte boundary to cover all the popular memory configurations. The data bus buffers are bidirectional allowing DMA operations to the onboard memory sockets.

A 2 channel DMA provides high speed memory-to-memory and onboard memory-to-I/O transfers. The DMA features edge or level sense request inputs and is programmable for burst or cycle steal transfers.

A software programmable memory wait state generator inserts from 0 to 3 wait states automatically during CPU and HD64180 on-chip DMA transfer cycles. Use of 300nS components are the fastest memory devices required without needing wait states.

The REFRESH* signal is automatically generated and gated on the CMOS STD Bus for dynamic RAM's. Dynamic RAM memory cells will be refreshed regardless of where they reside in the memory map. It can be disabled by a software command for faster processor operation.

MEMEX is not used and is wired to ground.

Serial Communications - Four serial channels are supported on this board. Two independent, full duplex, asynchronous channels (ASCI) are on the HD64180 chip. These are dual UART's with independent software programmable baud rate generators up to 19.2 Kbps. They can be linked to the processor DMA channel for high speed serial data transfer and to reduce CPU overhead. Both channels are configured for RS-232 levels.

A Z80-SIO provides two additional independent, full duplex, multifunction serial channels. The device supports all common asynchronous and synchronous protocols, byte- or bit oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Both SIO channel's baud rates are software programmable and can operate up to 800 Kbps. Four different baud rate sources are available to the SIO. The CKA0, CKA1, and A18/TOUT outputs from the HD64180 and the synchronous clock inputs from the RS-232 connector serve as jumper selectable clock sources.

The SIO's transmitter registers are doubly buffered and the receiver registers are quadruply buffered. Each channel is capable of independent synchronous or asynchronous operation and is jumper configurable as either data communications equipment (DCE) or data terminal equipment (DTE). Channel A is selectable for either RS-232 or full duplex RS-422/485 operation. It can also be configured as half duplex RS-422/485 with a separate synchronous clock channel. Channel B is dedicated to RS-232. Modem handshaking is available with RTS and CTS. The SIO is wired directly to the DMA channels on the HD64180 to provide very high speed data transfers.

Counter/Timer - The LPM-SBC5 contains two separate 16-bit programmable, reloadable, interruptable timers (PRT). Each contains a 16-bit down timer and a 16-bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. PRT channel 1 has a TOUT output pin that is multiplexed with A18 which can be set to toggle. This output is jumper selectable as a baud rate source for the SIO. When TOUT is enabled, A18 becomes inoperative yielding a total memory address range of 256K bytes.

I/O - The LPM-SBC5's processor generates addressing for a 64K byte I/O space by using a 16-bit I/O address. Most CMOS STD I/O cards decode only an 8-bit I/O address. The HD64180 can relocate the base address of on-chip I/O and control registers on any 64 byte boundary.

A software programmable I/O wait state generator inserts from 0 to 6 wait states automatically for CPU and external I/O accesses.

IOEXP is not used and is wired to ground.

LPM-SBC5 I/O MAP

I/O Port Address (hexadecimal)	Register
00	ASCI Control Register A Ch 0
01	ASCI Control Register A Ch 1
02	ASCI Control Register B Ch 0
03	ASCI Control Register B Ch 1
04	ASCI Status Register Ch 0
05	ASCI Status Register Ch 1
06	ASCI Transmit Data Register Ch 0
07	ASCI Transmit Data Register Ch 1
08	ASCI Receive Data Register Ch 0
09	ASCI Receive Data Register Ch 1
0A	CSI/O Control Register
0B	CSI/O Transmit/Receive Data Register
0C	Timer Data Register Ch 0L
0D	Timer Data Register Ch 0H
0E	Reload Register Ch 0L
0F	Reload Register Ch 0H
10	Timer Control Register
11 to 13	Reserved
14	Timer Data Register Ch 1L
15	Timer Data Register Ch 1H
16	Reload Register Ch 1L
17	Reload Register Ch 1H
18 to 1F	Reserved
20	DMA Source Address Register Ch 0L
21	DMA Source Address Register Ch 0H
22	DMA Source Address Register Ch 0B
23	DMA Destination Address Register Ch 0L
24	DMA Destination Address Register Ch 0H
25	DMA Destination Address Register Ch 0B

I/O Port Address (hexadecimal)	Register
26	DMA Byte Count Register Ch 0L
27	DMA Byte Count Register Ch 0H
28	DMA Memory Address Register Ch 1L
29	DMA Memory Address Register Ch 1H
2A	DMA Memory Address Register Ch 1B
2B	DMA I/O Address Register Ch 1L
2C	DMA I/O Address Register Ch 1H
2D	Reserved
2E	DMA Byte Count Register Ch 1L
2F	DMA Byte Count Register Ch 1H
30	DMA Status Register
31	DMA Mode Register
32	DMA/WAIT Control Register
33	INT Vector Register
34	INT/TRAP Control Register
35	Reserved
36	Refresh Control Register
37	Reserved
38	MMU Common Bank Base Register
39	MMU Bank Base Register
3A	MMU Common/Bank Area Register
3B to 3E	Reserved
3F	I/O Control Register
FC	SIO Data Register Ch A
FD	SIO Control/Status Ch A
FE	SIO Data Register Ch B
FF	SIO Control/Status Ch B

4

Watchdog Timer - A separate hardware retriggerable one-shot watchdog timer is implemented that is capable of automatically resetting the processor after a fixed time interval of approximately 1 second. A jumper option is available to enable the timer. This circuit is important for use in remote or unattended applications.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a System Reset is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line preventing invalid data from being written to EEPROMs.

Interrupts - The LPM-SBC5 supports all three Z80 interrupt modes and the non maskable interrupt as well as the 8 internal HD64180 interrupt sources. The STD Bus priority daisy chain is maintained with the LPM-SBC5's Z80-SIO peripheral the highest followed by the other STD Bus cards in decreasing priority order from the beginning of the PCI/PCO chain.

SLEEP Mode - The LPM-SBC5 has 3 different low power SLEEP modes: SLEEP, IOSTOP, and SYSTEM STOP. The SLEEP mode is entered by the execution of the 2 byte instruction. The processor stops in a known condition with only the internal

oscillator running. IOSTOP stops only the internal I/O functions while the CPU continues to function. SYSTEM STOP is the combination of SLEEP and IOSTOP modes. Recovery to normal operation is from detection of an external of internal interrupt or SYSRESET*.

CMOS STD Bus - The LPM-SBC5 card is available for the CMOS STD Bus and is designed with high speed, low power CMOS logic devices. CMOS offers a high degree of noise immunity, very low power consumption, and a wide temperature range (-40° to +85°C) for use in harsh industrial environments. As an option, this card can have the RS-232/422 serial line driver/receivers depopulated and jumpered directly to the connector to offer the lowest possible current drain.

CMOS STD Bus cards should not be used in terminated backplane systems. The extra capacitive loading of the termination networks degrade the system performance. It is recommended that WinSystems shielded motherboards and card racks be used.

WINMON 80 is an optional monitor program for the LPM-SBC5 that is used for program development and debugging. It is resident in a 2K byte PROM and allows the user to develop, load, execute, debug and modify a program. It also allows programs to be developed on CP/M 80 or IBM-PC or equivalent workstations and downloaded to the LPM-SBC5 through a serial port.

J1 Pinout (RS-232 Configuration)
SIO Channel A

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
15	RCLK (DB)
17	RCLK (DD)

J1 Pinout (RS-422 Configuration)
SIO Channel A

Pin	Signal
1	Ground
14	Transmit +
15	Receive-/Sync Clock-
16	Transmit-
17	Receive+/Sync Clock+

J2 Pinout
SIO Channel B

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J3 Pinout
ASCI Channel 0

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J4 Pinout
ASCI Channel 1

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)

SPECIFICATIONS

Electrical

System Clock: 3.072 MHz or 6.144 MHz

Bus Interface: CMOS STD-Z80 compatible.

Serial Interface: RS-232 and RS-422/485

Vcc = +5V ± 10% at 85 mA typ.
         ± 12V ±10% at 1.2 mA typ.

Without RS-422 Drivers:
Vcc = +5V ± 10% at 35 mA typ.
         ± 12V ± 10% at 1.2 mA typ.

Memory

Addressing: 512K bytes direct addressing

Capacity: Supports 8K, 16K, and 32K byte 28-pin RAM,
          ROM, EPROM, and EEPROMS.
          64K bytes maximum per card

I/O Ports

HD64180: DMA channel 0, DMA channel 1, Timer 0, Timer 1,
         Interrupt vector, ASCI Channel 0, ASCI Channel 1,
         and MMU
         00h to 3Fh (Relocateable)
Z80-SIO: FCh to FFh

Mechanical

Dimensions: Meets all STD Bus general mechanical specifi-
            cations except I/O connectors extend beyond
            card edge; 4.5 x 7.0 x 0.6 inches

Connectors: Four 10-pin 0.100" grid right angle connectors
            for Serial I/O that mate with Ansley 609-1041
            or equivalent.

Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Noncondensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBC5-3   CMOS STD Bus Single Board Multifunction
             3.072 MHz CMOS HD64180 Computer

LPM-SBC5-6   6.144 MHz HD64180 Single Board Multi-
             function Computer

WINMON 80   Monitor program for the LPM-SBC5

WinSystems, Inc.

FEATURES

- HD64180 high integration processor
- Fully Z80 software and interrupt compatible
- Additional processor capability: 12 additional instructions including high speed hardware multiply
- On chip MMU for direct addressing to 512K bytes
- Two 28-pin memory sockets supporting any mix of RAM, ROM, EPROM, and EEPROMs
- 2 channel DMA controller
- Automatic dynamic RAM REFRESH generation
- Memory and I/O Wait state generator
- Two RS-232 serial asynchronous I/O channels with programmable baud rate generators
- Two Z80-SIO multiprotocol DMA serial channels with one RS-232 or RS-422/485 and one RS-232 interface with modem interface signals
- Two 16-bit reloadable timers
- Jumper enabled watchdog timer
- Supports Z80 mode 2 vectored interrupts
- Power-on reset/brown out detect circuit
- SLEEP, IOSTOP and SYSTEM STOP Mode for very low power operation

The MCM-SBC5 is a powerful, multifunction single board computer using the Hitachi HD64180 microcomputer. This processor offers the benefits of high performance while maintaining compatibility with the large base of industry standard 8080/Z80 8-bit software. The board contains the processor, with 512K bytes of direct memory addressing, hardware multiply, 2 DMA channels, 2 28-pin JEDEC memory sockets, 4 serial I/O channels, two 16-bit timers, watchdog timer, powerfail/brownout reset circuit, and full STD Bus interface.
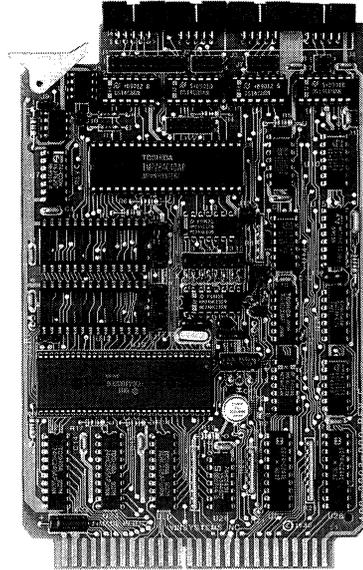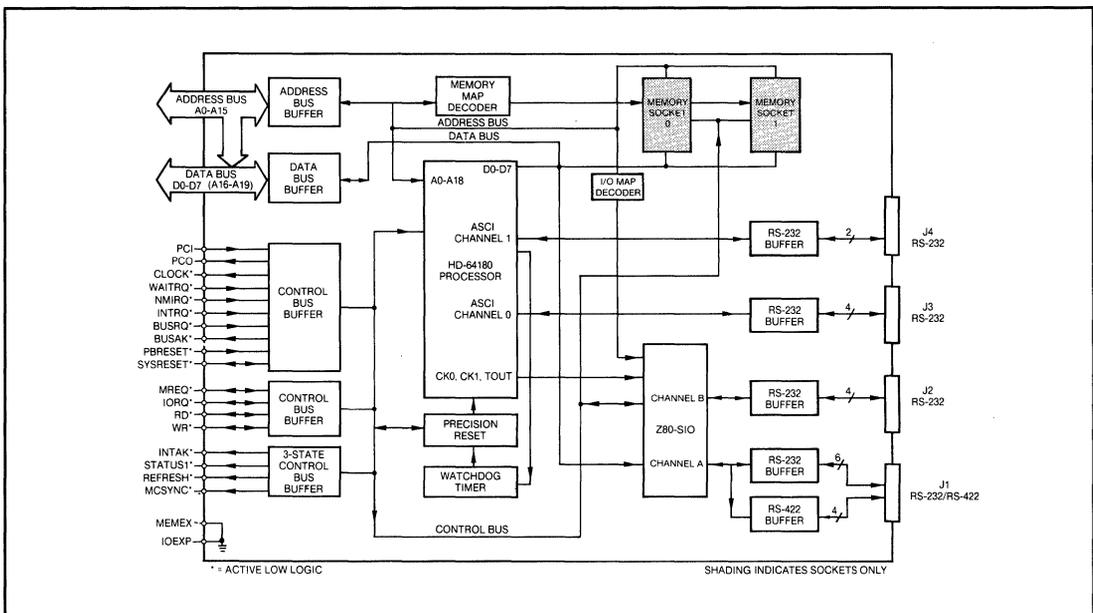
FUNCTIONAL CAPABILITY

Processor - The MCM-SBC5 is designed with the Hitachi HD64180 processor which provides high performance by virtue of its pipelining, enhanced instruction set, on-chip multiplier, and integrated Memory Management Unit (MMU). The CPU is microcoded to implement an upward compatible superset of the 8-bit 8088/Z80 standard software instruction set. Many instructions require fewer clock cycles for execution and twelve new instructions are added. A detailed HD64180 technical manual can be obtained from Hitachi America by calling 1-800-842-9000 and requesting publication U-77.

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both.

The processor, offered in either 6.144 or 3.072 MHz, is fully buffered and interfaced to the STD Bus. It is fully mode 2 compatible for vectored interrupts and conforms to STD Z80 timing.

Addressing - The MMU maps the CPU's 64K bytes of logical memory address space into 512K bytes of physical memory space. The MMU organization preserves software object code compatibility while providing extended memory access and uses an efficient "common area - bank area" scheme. The MCM-SBC5 generates a 20-bit address conforming to the STD Bus Multiplexed Memory Addressing scheme. Address lines A0 through A15 are driven directly onto the STD Bus. Address lines A16 through A19 are time multiplexed onto data bus lines D0 through D3 respectively. Memory cards latch A16 through A19 on the rising edge of MCSYNC*. A19 is not active and wired to ground yielding a total memory address capability of 512K bytes. The multiplexing of the extra address lines on the data bus requires no additional CPU overhead and is transparent to other I/O mapped cards in a system.

Memory - Two JEDEC standard 28-pin memory sockets are provided to allow the use of any mix of RAM's, ROM's, EPROM's, or EEPROM's. These sockets reside in the lower 64K bytes of memory and can accept 8K, 16K, or 32K byte devices per socket. The sockets can be mapped on any 8K byte boundary to cover all the popular memory configurations. The data bus buffers are bidirectional allowing DMA operations to the on-board memory sockets.

A 2 channel DMA provides high speed memory-to-memory and on board memory-to-I/O transfers. The DMA features edge or level sense request inputs and is programmable for burst or cycle steal transfers.

A software programmable memory wait state generator inserts from 0 to 3 wait states automatically during CPU and HD64180 on-chip DMA transfer cycles.

The REFRESH* signal is automatically generated and gated on the STD Bus for dynamic RAMs. Dynamic RAM memory cells will be refreshed regardless of where they reside in the memory map. It can be disabled by a software command for faster processor operation.

MEMEX is not used and is wired to ground.

Serial Communication - Four serial channels are supported on this board. Two Independent, full duplex, asynchronous channels (ASCI) are on the HD64180 chip. These are dual UART's with independent software programmable baud rate generators up to 38.4 Kbps. They can be linked to the processor DMA channel for high speed serial data transfer and to reduce CPU overhead. Both channels are configured for RS-232 levels.

A Z80-SIO provides two additional independent, full duplex, multifunction serial channels. The device supports all common asynchronous and synchronous protocols, byte- or bit oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Both SIO channel's baud rates are software programmable and can operate up to 307.2 Kbps asynchronous and 800 Kbps synchronous. Four different baud rate sources are available to the SIO. The CKA0, CKAl, and A18/TOUT outputs from the HD64180 and the synchronous clock inputs from the RS-232 connector serve as jumper selectable clock sources.

The SIO's transmitter registers are doubly buffered and the receiver registers are quadruply buffered. Each channel is capable of independent synchronous or asynchronous operation and is jumper configurable as either data communications equipment (DCE) or data terminal equipment (DTE). Channel A is selectable for either RS-232 or full duplex RS-422/485 operation. It can also be configured as half duplex RS-422/485 with a separate synchronous clock channel. Channel B is dedicated to RS-232. Modem handshaking is available with RTS and CTS. The SIO is wired directly to the DMA channels on the HD64180 to provide very high speed data transfers.

J1 Pinout (RS-232 Configuration)
SIO Channel A

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
15	RCLK (DB)
17	RCLK (DD)

J1 Pinout (RS-422/485 Configuration)
SIO Channel A

Pin	Signal
1	Ground
14	Transmit+
15	Receive-/Sync Clock-
16	Transmit-
17	Receive+/Sync Clock+

J2 Pinout
SIO Channel B

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J3 Pinout
ASCI Channel 0

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)

J3 Pinout
ASCI Channel 1

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)

Timers - The MCM-SBC5 contains two separate 16-bit programmable, reloadable, interruptable timers (PRT). Each contains a 16-bit down timer and a 16-bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. PRT channel 0 has a TOUT output pin that is multiplexed with A18 which can be set to toggle. This output is jumper selectable as a baud rate source for the SIO. When TOUT is enabled, A18 becomes inoperative yielding a total memory address range of 256K bytes.

I/O - The MCM-SBC5's processor generates addressing for a 64K byte I/O space by using a 16-bit I/O address. Most STD I/O cards decode only an 8-bit I/O address. The HD64180 can relocate the base address of on chip I/O and control registers on any 64 byte boundary.

A software programmable I/O wait state generator inserts from 0 to 6 wait states automatically for CPU and external I/O accesses.

IOEXP is not used and is wired to ground.

Watchdog Timer - A separate hardware retriggerable one-shot timer is implemented that is capable of automatically resetting the processor with PBRESET* after a fixed time interval of approximately 1 second. A jumper option is available to enable the timer. This circuit is important for use in remote or unattended applications.

Real Time Clock - An optional Dallas Semiconductor SmartWatch can be added to one of the memory sockets. This device contains a calendar clock, oscillator, battery and powerfail detect logic in a single 28-pin socket. The chip keeps track of hundreths of seconds, seconds, minutes, hours, days, date of month, and years. Additionally the device allows a RAM or EPROM to plug "piggy back" into the SmartWatch and operate transparently in the same memory space. For a detailed Data Sheet and Application Note, call Dallas Semiconductor at 214-450-0400.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line preventing invalid data from being written to EEPROMs.

Interrupts - MCM-SBC5 supports all three Z80 interrupt modes and the non maskable interrupt (NMI) as well as the 8 internal HD64180 interrupt sources. The STD Bus priority daisy chain is maintained with the MCM-SBC5's Z80-SIO peripheral as the highest followed by the other STD Bus cards in decreasing priority order from the beginning of the PCI/PCO chain.

4

SLEEP Mode - The MCM-SBC5 has 3 different low power SLEEP modes: SLEEP, IOSTOP, and SYSTEM STOP. The SLEEP mode is entered by the execution of the 2 byte instruction. The processor stops in a known condition with only the internal oscillator running. IOSTOP stops only the internal I/O functions while the CPU continues to function. SYSTEM STOP is the combination of SLEEP and IOSTOP modes. Recovery to normal operation is from detection of an external or internal interrupt or SYSRESET*.

WINMON 80 - is an optional monitor program for the MCM-SBC5 for program development and debugging. It is resident in an 8K byte EPROM and allows the user to develop, load, execute, debug and modify a program. It also allows programs to be developed on CP/M 80 or IBM-PC or equivalent workstations and downloaded to the MCM-SBC5 through a serial port.

SPECIFICATIONS

Electrical

System Clock: 6.144 or 3.072 MHz

Bus Interface: STD-Z80 compatible.

Serial Interface: RS-232 and RS-422/485

Vcc = +5V ± 5% at 750 mA typ.
      ± 12V ± 10% at 50 mA typ.

Memory

Addressing: 512K bytes direct addressing

Capacity: Supports 8K, 16K, and 32K byte 28-pin RAM, ROM, EPROM, and EEPROMS. 64K bytes maximum per card

I/O Ports

HD64180: DMA channel 0, DMA channel 1, Timer 0, Timer 1, Interrupt vector, ASCI Channel 0, ASCI Channel 1 and MMU 00h to 3Fh (Relocateable)
Z80-SIO: FCh to FFh

Mechanical

Dimensions: Meets all STD Bus general mechanical specifications except I/O connectors extend beyond card edge; 4.5 x 7.0 inches

Connectors: Four 10-pin 0.100″ grid right angle connectors for Serial I/O that mate with Ansley 609-1030-1, Berg 65847-004-A or equivalent

Jumpers: 0.025″ square posts

Environmental

Operating Temperature: 0° to 65°C
Noncondensing relative humidity: 5% to 95%

ORDERING INFORMATION

WinSystems, Inc.

## FEATURES

- 4.0MHz CMOS Z80A processor, 3.6864 MHz and 6 MHz optional
- Three 28-pin memory sockets for up to 64K bytes of RAM, ROM, EPROM, EEPROM, or Dallas Semiconductor BRAMs.
- 8 individual selectable memory maps
- Bootstrap shadow PROM capability
- Two independent serial I/O channels with hand shake (Z80-SIO)
- Async baud rate to 38.4Kb on both channels
- RS-232-C interface on both channels
- Channel B supports RS-422/485 levels and synchro nous data
- Independent baud rate generation per channel
- Two 8-bit Parallel I/O ports with handshake
- Watchdog Timer
- 4 independent counter/timers (Z80-CTC)
- Supports Mode 2 vectored interrupts
- Precision Powerfail/Reset Circuit
- Operational Temperature range: -40° to +85°C
- CMOS STD Bus compatible
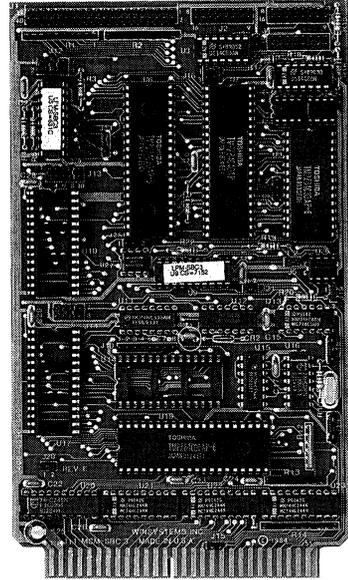
The LPM-SBC3 is a highly integrated, all CMOS STD Bus SBC featuring a Z80A CMOS processor with three 28-pin memory sockets, 16 parallel I/O lines with handshaking, 2 serial channels with modem handshaking, four counter/timer channels, and a precision powerfail reset. The LPM-SBC3 is ideal for harsh industrial solutions requiring cost critical applications with dense packaging, extended temperature and/or low power.
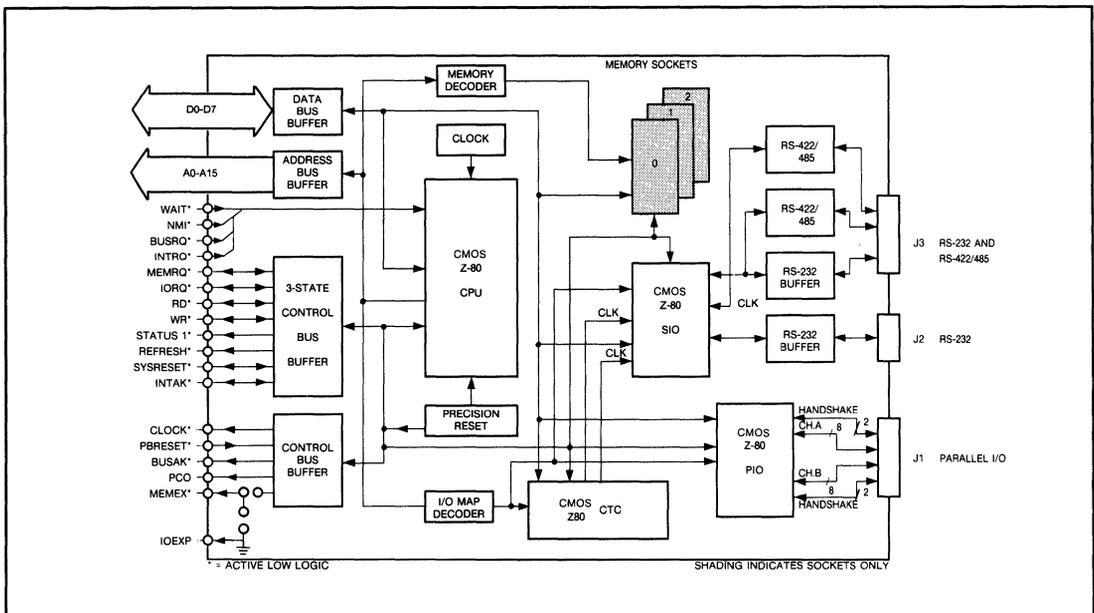
FUNCTIONAL CAPABILITY

Processor - The LPM-SBC3 uses the industry standard CMOS Z80 operating at 4 MHz with 3.6864 MHz optional. It supports all three Z80 interrupt modes plus nonmaskable interrupt (NMI). The LPM-SBC3's LSI peripherals (SIO, PIO, and CTC) are fully mode 2 interrupt driven to give maximum system performance.

Memory - Three JEDEC 28-pin bytewide memory sockets are with 8 hardware selectable memory maps. The memory sockets will support 2K, 4K, 8K, 16K, or 32K byte RAM, EPROM, and EEPROM devices in any mix. A control register allows the onboard memory to be disabled for a "phantom ROM" operation. MEMEX is not supported.

A total of 8 selectable memory maps are available. Five maps are preprogrammed and 3 are user programmable for custom decoding by the user.

EEPROMs, the Dallas Semiconductor SmartWatch and 64K and 256K Nonvolatile Memory Modules can be inserted in the memory sockets. The write line is inhibited by the powerfail reset circuit to prevent bad data from being written to the devices during Vcc out of tolerance conditions.

Serial I/O - Two independent, full duplex, serial channels are provided with the Z80-SIO. This device supports all common asynchronous and synchronous protocols, byte- or bit oriented, and performs all of the functions traditionally done by UART's and synchronous controllers combined. The SIO's transmitter registers are doubly buffered and the receiver registers are quadruply buffered.

Individual software selectable baud rates from 50-19200 bits per second are available for each asynchronous channel from the Z80-CTC. If the board uses a 3.6864 MHz system clock, then the asynchronous baud rate can be up to 38.4K bps per channel.

Channel A is asynchronous RS-232 only. Channel B is capable of full duplex RS-422/485 asynchronous or synchronous operation with a synchronous clock input or output. The RS-422/485 is used in applications requiring long cable lengths, high noise immunity, or high data rates. Channel B's RS-232 interface is capable of asynchronous operation only.

Each channel is jumper configurable as either Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) with modem handshake lines (RTS and CTS).

J1 Pinout - Serial Channel A

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
7	Ground

J3 Pinout - Serial Channel B

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
7	Ground
9	RS-422/485 Rx +
10	RS-422/485 Rx -
11	RS-422/485 Tx +
12	RS-422/485 Tx -
13	RS-422/485 Tx Clock +
14	RS-422/485 Tx Clock -

Both RS-232 and RS-422/485 interface levels are brought out to their respective 16-pin connector. This allows easy connections to flat cables with 25-pin "D" type connectors such as the WinSystems CBL-103-3 male and CBL-104-3 female ribbon cables.

Parallel I/O - A Z80 PIO is used to provide a highly versatile 16 line input/output controller. Two 8-bit ports, each with 2 handshake lines, are provided which can be configured in software for 4 operational modes under total interrupt control: Byte Input, Byte Output, Bidirectional, and Bit Input/Output. Also it can be programmed to interrupt the CPU on the occurance of specified status conditions in the peripheral device.

Each port has independent handshake signals to control the data transfer between the PIO and peripheral device. Each port automatically generates Ready and Strobe in all of the data transfer modes.

The data is brought out to a 40-pin connector. The active lines are on the even pins with the odd pins grounded for reduced noise and cross-talk.

Counter/Timers - The Z80 chip (CTC) provides 4 independent channels for counting, timing and baud rate generation for the serial channels. It can be used to generate real time clocks or other counting functions. The counters are cascadeable for longer count sequences.

J1 Pinout - Parallel I/O

Pin	Signal
2	A0
4	A1
6	A2
8	A3
10	A4
12	A5
14	A6
16	A7
18	A Ready
20	/A Strobe
22	B0
24	B1
26	B2
28	B3
30	B4
32	B5
34	B6
36	B7
38	B Ready
40	/B Strobe

Odd pins, 1 - 39, are ground

I/O - The LPM-SBC3 has 12 reserved I/O ports from locations 80h through 8B for the on-board Z-80-SIO, -CTC and -PIO peripheral devices. The I/O map is as follows:

LPM-SBC3 I/O Map

I/O Port Address (hexadecimal)	Device
80	Ch. A Data, Z80-SIO
81	Ch. A Control, Z80-SIO
82	Ch. B Data, Z80-SIO
83	Ch. B Control, Z80-SIO
84	Ch. 0, Z80-CTC (Ch. A baud rate)
85	Ch. 1, Z80-CTC (Ch. B baud rate)
86	Ch. 2, Z80-CTC
87	Ch. 3, Z80-CTC
88	Ch. A Data, Z80-SIO
89	Ch. A Control, Z80-SIO
8A	Ch. B Data, Z80-SIO
8B	Ch. B Control, Z80-SIO

IOEXP is not supported and is wired to ground.

Real Time Clock - The LPM-SBC3 can optionally be populated with a Dallas Semiconductor DS-1216 Smart-Watch. It is a 28-pin DIP socket with a built-in CMOS watch, power sequencer, and an embedded lithium energy source. Since the battery is internal to the socket, there is no danger of shorting or accidental discharge due to mishandling.

The SmartWatch accepts either 24 or 28-pin JEDEC Bytewide memory devices plugged into its socket. Then the DS-1216 plugs directly into one of the memory sockets onboard the LPM-SBC3. This permits full utilization of all the memory sockets while having a transparant battery backed timekeeping function.

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. It operates in either 24-hour or 12 hour format with an AM/PM indicator.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a 50 mS PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit also inhibits the processor's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

WINMON80 is an optional monitor program for the LPM-SBC3 for program development and debugging. It is resident in an EPROM and allows the user to develop, load, execute, and modify a program. It also allows programs to be developed on CP/M 80 or PC compatible computers and downloaded to the LPM-SBC3 through a serial port.

CMOS STD Bus - The LPM-SBC3 is designed with high speed, low power CMOS logic devices which offer a high degree of noise immunity, low power consumption, and a wide operational temperature range.

CMOS STD Bus cards should not be used in terminated backplane systems. The extra capacitive loading of the termination networks degrade the system performance. It is recommended that WinSystems shielded motherboards and card racks be used.

4

SPECIFICATIONS

Electrical

Bus Interface: CMOS STD-Z80

System Clock: 6.0 or 3.6864 MHz.

$Vcc = +5VDC \pm 10\%$ at 105 mA typ.
$= +12$ VDC $\pm 10\%$ at 1.2 mA typ.
$= -12$ VDC $\pm 10\%$ at 1.2 mA typ.

Without RS-422 Drivers
$Vcc = +5VDC \pm 10\%$ at 35 mA typ., 75 mA max.
$= +12$ VDC $\pm 10\%$ at 1.2 mA typ., 5 mA max.
$= -12$ VDC $\pm 10\%$ at 1.2 mA typ., 5 mA max.

Memory

Capacity: Three 28-pin JEDEC sockets.
Supports 2K, 4K, 8K, 16K, and 32K
bytes of RAM, ROM, EPROM, EEPROM or
battery backed RAM.

Memory map: Five standard memory decoding config-
urations plus three user programmable
options

I/O

Ports: Z80-CTC, -PIO, and -SIO reserved; 80h to 8Fh

Counter/Timer: Four 8-bit timers with prescalers

Parallel I/O: Two 8-bit TTL compatible with handshake

Serial I/O: RS-232-C on both channels
RS-422/485 on channel B only
Baud rate from 110 to 9600 bps (4.0MHz
clock) and to 38400 bps with 3.6864 MHz
system clock

Mechanical

Dimensions: Meets all STD Bus general mechanical
specifications except for length;
4.5 x 7.0 inches

PC Board: FR4 epoxy glass. Solder mask on both sides,
screened component legend and plated
through holes.

Connectors

System: 56-pin dual on 0.125" centers

Parallel I/O: 40-pin dual on 0.100" grid

Serial I/O: Two 16-pin on 0.100" grid

Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

|	
LPM-SBC3-3	3.6864 MHz CMOS Z80 SBC with operations manual.
LPM-SBC3-4	4.0 MHz CMOS Z80 SBC with operations manual
WINMON80-SBC3	Monitor firmware for the LPM-SBC3
LPM-SBC3-6	6.0 MHz CMOS Z80 SBC with operations manual

WinSystems, Inc.

FEATURES

- 3.6864, 4.0 and 6.0 MHz Z80 processor
- Three 28-pin memory sockets for up to 64K bytes of RAM, ROM, EPROM, EEPROM, or Dallas Semiconductor BRAMs.
- 8 Individual selectable memory maps
- Bootstrap shadow PROM capability
- Two independent serial I/O channels with handshake (Z80-SIO)
- Async baud rate to 38.4Kb on both channels
- RS-232-C interface on both channels
- Channel B supports RS-422/485 levels and synchronous data
- Independent baud rate generation per channel
- Two 8-bit parallel I/O ports with handshake (Z80-PIO)
- 4 independent counter/timers (Z80-CTC)
- Watchdog Timer
- Supports Mode 2 vectored interrupts
- Precision Powerfail/Reset circuit
- Optional CMOS version: LPM-SBC3
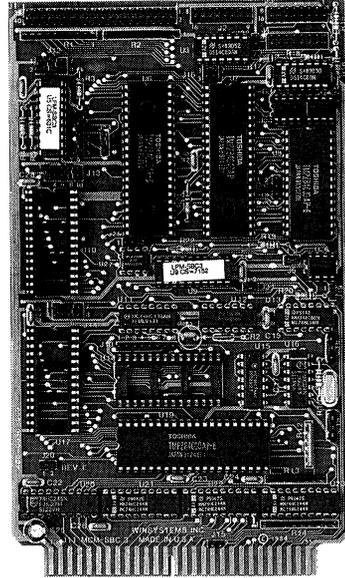
The MCM-SBC3 is a highly integrated STD Bus single board computer. It features a Z80 processor with three 28-pin memory sockets, 16 parallel I/O lines with handshaking, 2 serial channels with modem handshaking, four counter/timer channels, and a precision powerfail reset. The MCM-SBC3 is ideal for industrial solutions requiring cost critical applications with dense packaging.
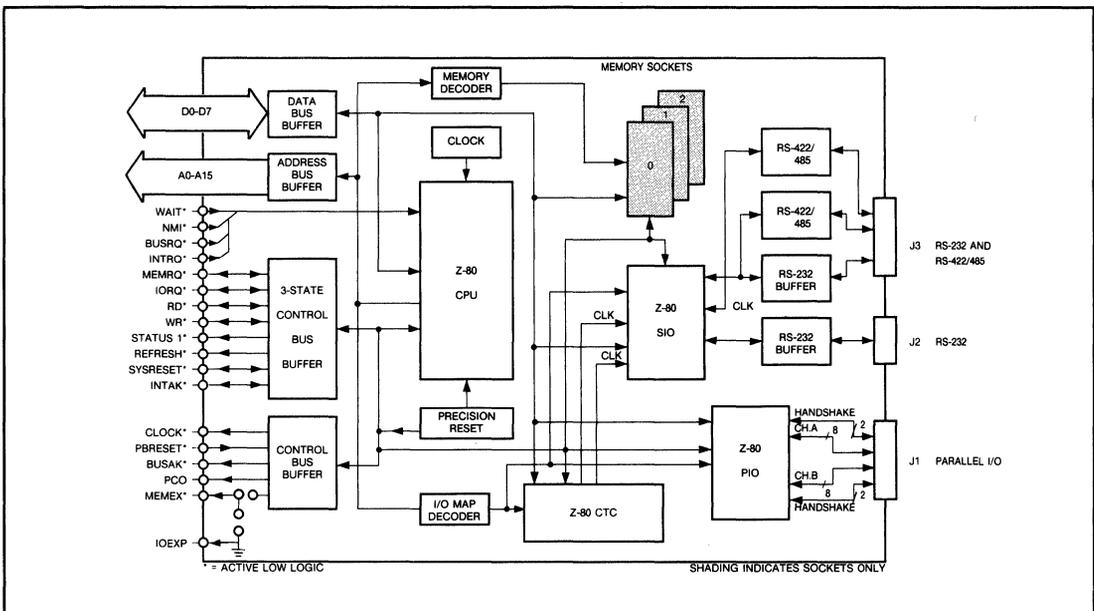
FUNCTIONAL CAPABILITY

Processor - The MCM-SBC3 uses the industry standard Z80 operating at 3.6864, 4.0 or 6.0 MHz. It supports all three Z80 interrupt modes plus non maskable interrupt (NMI). The MCM-SBC3's LSI peripherals (SIO, PIO, and CTC) are fully mode 2 interrupt driven to give maximum system performance. It also generates the DRAM Refresh signal automatically.

Memory - Three JEDEC 28-pin bytewide memory sockets are provided with 8 hardware selectable memory maps. The memory sockets will support 2K, 4K, 8K, 16K, or 32K byte RAM, EPROM, and EEPROM devices in any mix. A control register allows the onboard memory to be disabled for a "phantom ROM" operation. MEMEX is not supported.

A total of 8 selectable memory maps are available. Five maps are preprogrammed and 3 are user programmable for custom decoding by the user.

EEPROMs, the Dallas Semiconductor SmartWatch and 64K and 256K Nonvolatile Memory Modules can be inserted in the memory sockets. The write line is inhibited by the powerfail reset circuit to prevent bad data from being written to the devices during Vcc out of tolerance conditions.

Serial I/O - Two independent full duplex serial channels are provided with the Z80 SIO. The device supports all common asynchronous and synchronous protocols, byte- or bit oriented, and performs all of the functions traditionally done by UART's and synchronous controllers combined. The SIO's transmitter registers are doubly buffered and the receiver registers are quadruply buffered.

Individual software selectable baud rates from 50-19200 bits per second are available for each asynchronous channel from the Z80-CTC. If the board uses a 3.6864 MHz system clock, then the asynchronous baud rate can be up to 38.4K bps per channel.

Channel A is asynchronous RS-232 only. Channel B is capable of full duplex RS-422/485 asynchronous or synchronous operation with a synchronous clock input or output. The RS-422/485 is used in applications requiring long cable lengths, high noise immunity, or high data rates. Channel B's RS-232 interface is capable of asynchronous operation only.

Each channel is jumper configurable as either Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) with modem handshake lines (RTS and CTS).

J1 Pinout - Serial Channel A

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
7	Ground

J3 Pinout - Serial Channel B

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
7	Ground
9	RS-422/485 Rx +
10	RS-422/485 Rx -
11	RS-422/485 Tx +
12	RS-422/485 Tx -
13	RS-422/485 Tx Clock +
14	RS-422/485 Tx Clock -

Both RS-232 and RS-422/485 interface levels are brought out to their respective 16-pin connector. This allows easy connections to flat cables with with 25-pin "D" type connectors such as the WinSystems CBL-103-3 male and CBL-104-3 female ribbon cables.

Parallel I/O - A Z80-PIO is used to provide a highly versatile 16 line input/output controller. Two 8-bit ports each with 2 handshake lines are provided which can be configured in software for 4 operational modes under total interrupt control: Byte Input, Byte Output, Bidirectional, and Bit Input/Output. Also it can be programmed to interrupt the CPU on the occurance of specified status conditions in the peripheral device.

Each port has independent handshake signals to control the data transfer between the PIO and peripheral device. Each port automatically generates Ready and Strobe in all of the data transfer modes.

The data is brought out to a 40-pin connector. The active lines are on the even pins with the odd pins grounded for reduced noise and cross-talk.

Counter/Timers - The Z80 chip (CTC) provides 4 independent channels for counting, timing and baud rate generation for the serial channels. It can be used to generate real time clocks or other counting functions. The counters are cascadeable for longer count sequences.

J1 Pinout - Parallel I/O

Pin	Signal
2	A0
4	A1
6	A2
8	A3
10	A4
12	A5
14	A6
16	A7
18	A Ready
20	/A Strobe
22	B0
24	B1
26	B2
28	B3
30	B4
32	B5
34	B6
36	B7
38	B Ready
40	/B Strobe

Odd pins, 1 - 39, are ground

I/O - The MCM-SBC3 has 12 reserved I/O ports from locations 80h through 8Bh for the on-board Z80-SIO, -CTC and -PIO peripheral devices. The I/O map is as follows:

MCM-SBC3 I/O Map

I/O Port Address (hexadecimal)	Device
80	Ch. A Data, Z80-SIO
81	Ch. A Control, Z80-SIO
82	Ch. B Data, Z80-SIO
83	Ch. B Control, Z80-SIO
84	Ch. 0, Z80-CTC (Ch. A baud rate)
85	Ch. 1, Z80-CTC (Ch. B baud rate)
86	Ch. 2, Z80-CTC
87	Ch. 3, Z80-CTC
88	Ch. A Data, Z80-SIO
89	Ch. A Control, Z80-SIO
8A	Ch. B Data, Z80-SIO
8B	Ch. B Control, Z80-SIO

IOEXP is not supported and is wired to ground.

Real Time Clock - The MCM-SBC3 can optionally be populated with a Dallas Semiconductor DS-1216 Smart-Watch. It is a 28-pin DIP socket with a built-in CMOS watch, power sequencer, and an embedded lithium energy source. Since the battery is internal to the socket, there is no danger of shorting or accidental discharge due to mishandling.

The SmartWatch accepts either 24 or 28-pin JEDEC Bytewide memory devices plugged into its socket. Then the DS-1216 plugs directly into one of the memory sockets onboard the MCM-SBC3. This permits full utilization of all the memory sockets while having a transparant battery backed timekeeping function.

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. It operates in either 24-hour or 12-hour format with an AM/PM indicator.

Watchdog Timer - A Maxim 690 supervisory circuit serves as a programmable, retriggerable watchdog timer. The circuit must be toggled by writing to an I/O port at least once every 1.5 seconds. If it is not toggled in time, then the circuit assumes either a software or hardware failure and it restores the processor to a known condition by issuing a 50 mS PBRESET* pulse. The watchdog timer output is disabled with a jumper option. This circuit is important for use in remote and unattended applications.

Reset - A precision band gap voltage comparator circuit is used to accurately determine the Vcc status. Upon detection of an out of tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions. This circuit also inhibits the processor's write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

WINMON80 is an optional monitor program for the MCM-SBC3 for program development and debugging. It is resident in an EPROM and allows the user to develop, load, execute, and modify a program. It also allows program to be developed on CP/M 80 or PC compatible computers and downloaded to the MCM-SBC3 through a serial port.

CMOS STD Bus - For extended temperature or low power applications, the MCM-SBC3 is available as the LPM-SBC3 for the CMOS STD Bus.

4

SPECIFICATIONS

Electrical

Bus Interface: STD-Z80

System Clock: 3.6864, 4.0, or 6.0 MHz

Vcc = +5VDC ± 5% at 750 mA typ., 975 mA max.
    = +12 VDC ± 10% at 35 mA typ., 50 mA max.
    = -12 VDC ± 10% at 35 mA typ., 50 mA max.

Memory

Capacity: Three 28-pin JEDEC sockets.
    Supports 2K, 4K, 8K, 16K, and 32K
    bytes of RAM, ROM, EPROM, EEPROM or
    battery backed RAM.

Memory map: Five standard memory decoding config-
    urations plus three user programmable
    options

I/O

Ports: Z80-CTC, -PIO, and -SIO reserved; 80h to 8Fh

Counter/Timer: Four 8-bit timers with prescalers

Parallel I/O: Two 8-bit TTL compatible with handshake

Serial I/O: RS-232-C on both channels
    RS-422/485 on channel B only
    Baud rate from 110 to 9600 bps (4.0MHz
    clock) and to 38400 bps with 3.6864 MHz
    system clock

Mechanical

Dimensions: Meets all STD Bus general mechanical
    specifications except for length;
    4.5 x 7.0 inches

PC Board: FR4 epoxy glass. Solder mask on both sides,
    screened component legend and plated
    through holes.

Connectors

System: 56 pin dual on 0.125" centers

Parallel I/O: 40-pin dual on 0.100" grid

Serial I/O: Two 16-pin on 0.100" grid

Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-SBC3-3	3.6864 MHz Z80 SBC with operations manual.
MCM-SBC3-4	4.0 MHz Z80 SBC with operations manual
MCM-SBC3-6	6.0 MHz Z80 SBC with operations manual
WINMON80-SBC3	Monitor firmware for the MCM-SBC3

WinSystems, Inc.

Memory

MCM prefix on a product name designates a STD Bus card and a LPM prefix designates a CMOS STD Card. The LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS STD Bus and STD Bus logic. The differences between these products are the various power requirements and operational temperature ranges.

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| PRODUCT	Bus INTERFACE	DATA WIDTH (BITS)	RAM (MAX)	EPROM (MAX)	BATTERY BACKED
MCM-7706	STD Bus	8	64 KB	64 KB	YES
LPM-7709	CMOS STD Bus	8	512 KB	256 KB	YES
MCM-7709	STD Bus				
LPM-DPRAM	CMOS STD Bus	8	1 KB	—	NO
MCM-DPRAM	STD Bus				
MCM-DRAM128	STD Bus	8	128 KB	—	NO
MCM-DRAM64	STD Bus	8	64 KB		
LPM-UMC	CMOS STD Bus	8	64 KB	64 KB	NO
MCM-UMC	STD Bus				
LPM-UMC2	CMOS STD Bus	8	512 KB	256 KB	OPT.
MCM-UMC2	STD Bus				
LPM-UMC4	CMOS STD Bus	8	1024 KB	1024 KB	OPT.
MCM-UMC4	STD Bus				

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FEATURES

- Eight 28-pin Bytewide compatible memory sockets that hold up to 64K bytes of battery backed RAM
- 10 year data retention
- Unused sockets can be populated with any mix of EPROMs or RAMs up to 64K bytes
- Processor independent including 80188, 8088, 68008, HD64180, 8085A, Z80, 6502, and 6809
- Supports 16 or 20-bit direct addressing
- Compatible with STD-8088 1 Megabyte Addressing
- Page Mode Operation for up to sixteen boards per system
- Onboard flexible address decoding
- Replaces Pro-Log 7706 and Mostek MDX-ZRAM
- 8 MHz Operation
- Single +5 Volt operation

The MCM-7706 is a STD Bus bytewide memory expansion card with eight 28-pin JEDEC sockets which is populated with battery backed RAMs. Unused sockets can hold any mix of EPROMs or RAMs to 64K bytes of memory on a single board. All STD Bus processor types including the Z80, 8085A, HD64180, 6809, 6502, 8088, 80188 and 68008 are supported.
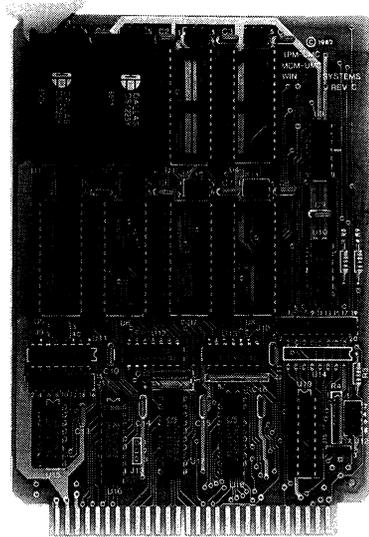
FUNCTIONAL CAPABILITY

Addressing - This card can be used with either 16-bit addressing or direct 20-bit addressing methods. Using the 20-bit address multiplexing configuration, up to 1M byte of memory may be directly addressed by 8088, 80188, 68008 or HD64180 based systems. A0 through A15 are received directly from the address bus and the MCM-7706 demultiplexes the remaining four address

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SHADING INDICATES SOCKETS ONLY
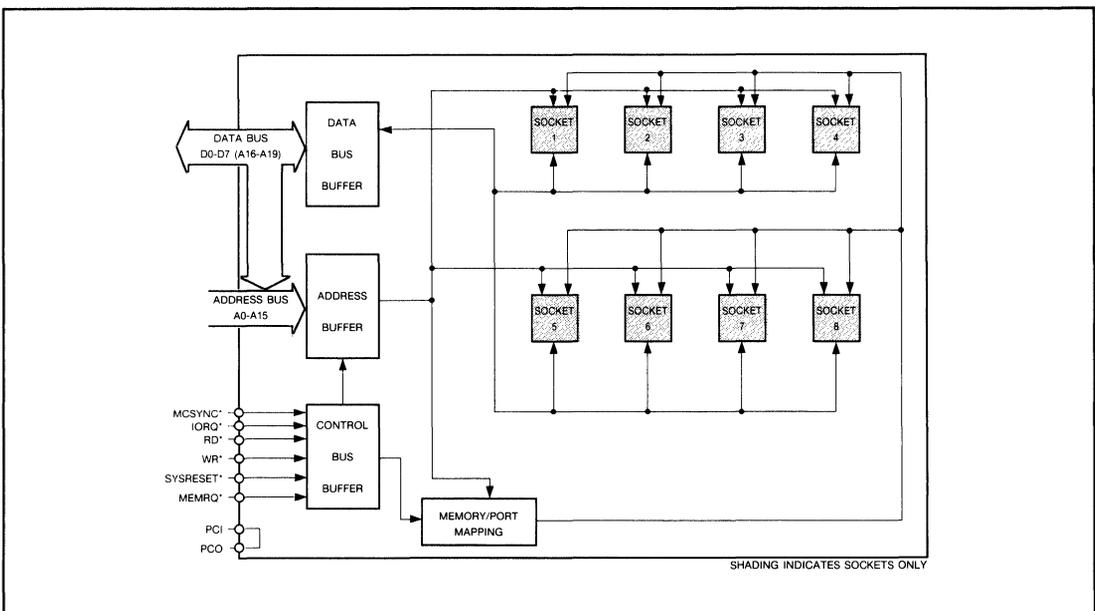
lines, A16 - A19 from the data bus. More than one MCM-7706 card can be in a STD Bus system providing up to a full 1 Megabyte of directly addressable memory.

When used with 8-bit processors that generate only a 16-bit memory address, the card supports up to 64K bytes of direct addressing.

The MCM-7706 also has a page mode operation to allow up to 16 MCM-7706 boards per STD Bus system. The page mode circuit operates from a write only I/O port located at address FFh. It writes up to 16 individual page numbers to an on-board latch which enables/disables the memory board. This circuit is used by 8-bit processors that do not support other memory management techniques for memory addressing beyond 64K bytes.

Memory - The MCM-7706 is populated with the Dallas semiconductor nonvolatile 2K x 8 and/or 8K x 8 memory modules. These units are fully static RAMs with a self contained lithium energy source and control circuitry that monitors Vcc for an out of tolerance condition. When such a condition occurs, the energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required. The devices have over 10 years of data retention. For additional information call Dallas Semiconductor at (214) 450-0400.

The board contains eight JEDEC standard 28-pin sockets that are configured to support 2K, 4K, or 8K byte, 24 or 28-pin devices for a maximum of 64K bytes of RAM or EPROMs per board. Sockets not containing a Dallas Semiconductor nonvolatile RAM can accept other bytewide memory devices.

A flexible decoder is provided that has 16 different memory maps, 12 of which are defined by WinSystems and 4 which can be custom configured by the user. For special configurations or memory maps contact the factory.

The MCM-7706 will support systems running up to 8 MHz clocks with the correct speed memory devices installed.

This board is a functional replacement to the Mostek MDX-ZRAM (MK77767) and the Pro-Log 7706.

SPECIFICATIONS

Electrical

Compatible with the STD Bus for the Z80, 8085A, 6809, 6502, HD64180, 8088, 80186 and 68008 microprocessors.
Vcc = +5 volts $\pm$ 5% at 300 mA typ. without onboard memory .

Memory

Capacity: Eight 28 pin bytewide memory sockets with 4K, 8K, 16K, 32K, 48K or 64K of battery backed memory. Each unused socket can be strapped for 2K, 4K or 8K RAM, BRAM, ROM, or EPROM devices.

Decoding: Bipolar PROM with twelve preprogrammed memory decode options and four user programmable.

Page Mode: Up to 16 boards per system controlled by I/O port FFh.

Direct Addressing: Up to 1 Megabyte using 20-bit addressing

Mechanical

Dimensions: Meets all STD Bus mechanical specifications; 4.5 x 6.5 inches

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-7706-4L   4K byte battery backed memory card

MCM-7706-8L   8K byte battery backed memory card

MCM-7706-16L 16K byte battery backed memory card

MCM-7706-32L 32K byte battery backed memory card

MCM-7706-48L 48K byte battery backed memory card

MCM-7706-64L 64K byte battery backed memory card

WinSystems, Inc.

FEATURES

- Supports 16 or 20-bit direct addressing up to 1M byte
- 256K byte CMOS static RAM capacity
- Available in 8K, 16K, 32K, and 64K byte versions
- Lithium battery backup
- Unused sockets support RAM, ROM, EPROM, and EEPROMs
- Onboard powerfail/brown-out detect circuit
- Write protection for RAMs
- Processor independent including 80188, 80C88, 68008, HD64180, 80C85A, Z80, NSC800 and 6809
- Flexible address decoding
- MEMEX supported
- Single +5 volt operation
- Operational temperature range: -40° to +85°C
- Replaces Pro-Log 77C09 card
- Available for CMOS STD Bus: LPM-7709
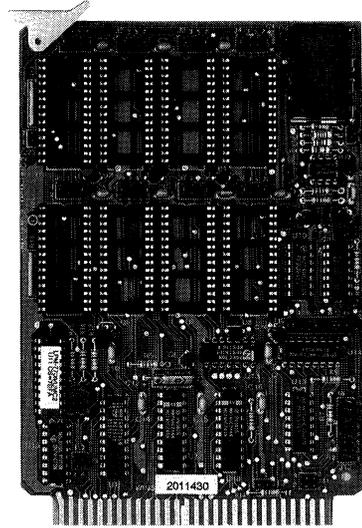
The LPM/MCM-7709 is a STD Bus and CMOS STD Bus battery backed bytewide memory expansion card with eight 28-pin JEDEC sockets that provide up to 256K bytes of non-volatile memory storage. If not all static CMOS RAM is required, ROMs, EPROMs and EEPROMs can be added in the unused sockets to provide the total memory requirements for many STD Bus and CMOS STD Bus systems. It is designed to support all the STD Bus and CMOS STD Bus processor types including the Z80, 80C85A, NSC800, HD64180, 6809, 80C88, 80188 and 68008.

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SHADING INDICATES SOCKETS ONLY
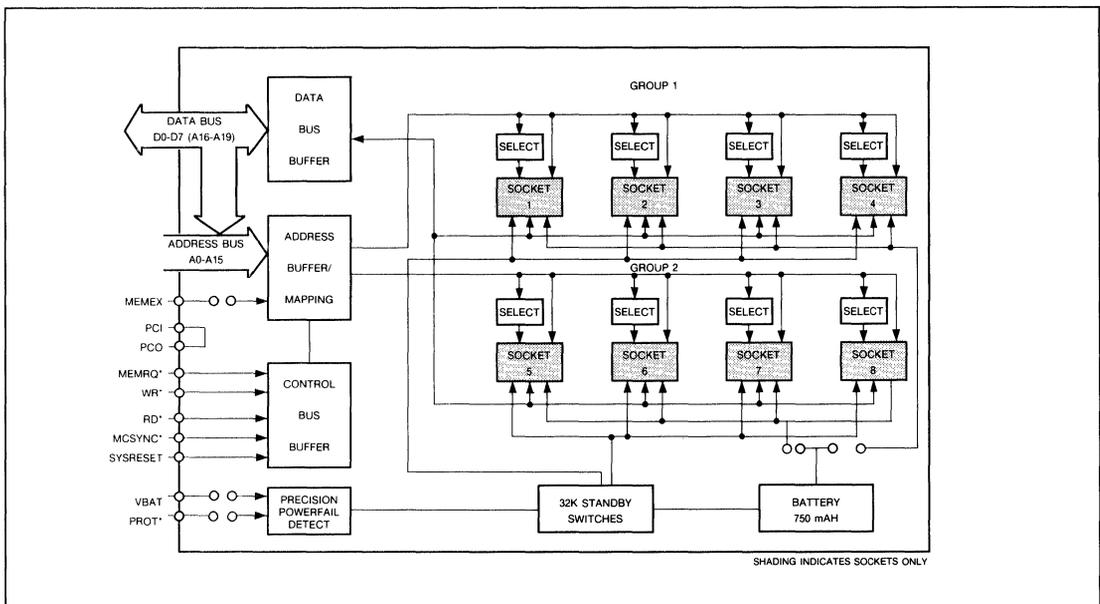
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7709 is the CMOS STD Bus version and the MCM-7709 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - This card can be used with either 16-bit addressing or direct 20-bit addressing methods. Using the 20-bit address multiplexing configuration, up to 1M byte of memory may be directly addressed by 80C88, 68008 or HD64180 based systems. A0 through A15 are received directly from the address bus and the LPM/MCM-7709 demultiplexes the remaining four address lines A16 - A19 from the data bus. More than one LPM/MCM-7709 card can be in a STD Bus and CMOS STD Bus system providing up to a full 1 Megabyte of directly addressable memory. The LPM/MCM-7709 will also respond to the MEMEX signal which allows an additional 1M byte of memory to be accessed or used for bootstrapping. When used with 8-bit processors that generate only a 16-bit memory address, the card supports up to 64K bytes of direct addressing.

Memory - The board contains eight JEDEC standard 28-pin sockets that are configured to support up to 256K bytes of CMOS RAMs. The socket size is configurable on a per group basis and 2 independent groups of 4 sockets each are available per board. Each group has its own battery backed power and user-selectable base address in the 20-bit address range. The starting address for each group is independent and does not have to be contiguous with the other group.

If one group does not require battery power, then 8K, 16K, 32K, or 64K byte devices can be added to the other group. Any combination of RAM, ROM, EPROM, or EEPROMs can be made in the group as long as the memory device is the same capacity as the configured socket. Typically one group would be used for PROM code and the other would be used for RAM data. For example, one group could be configured for 32K bytes using four 8K byte CMOS battery backed RAMs and the other group for 128K bytes using four 32K byte EPROMs.

This board is offered with a standard population of up to eight, 8K x 8 CMOS RAMs. Contact the factory for other options.

Write Inhibit - A power fail detect circuit continuously monitors the Vcc line for an out of tolerance condition. If the power drops below 4.5 volts the circuit is activated. The internal reset, SYSRESET*, or DCPD* will inhibit the write lines on the board. The reset signal can also be jumpered to drive pin 6 (VBB#2/ DCPD*) active on the STD Bus and CMOS STD Bus.

Battery Backup - A 750 mA-hour lithium battery provides backup power for the CMOS static RAMs in either or both groups of sockets. It will provide thousands of hours of backup. The exact time is a function of the standby current and number of CMOS RAMs used. Alternatively, external battery power can also be jumper selected from the CMOS STD VBAT signal.

SPECIFICATIONS

Electrical

Vcc = +5 volts $\pm$ 10% at 10mA typ.: LPM-7709-0L
+5 volts $\pm$ 5% at 350mA typ.: MCM-7709-0N

Mechanical

Meets STD Bus mechanical specifications

Environmental

Operating Temperature:
LPM-7709-0L   -40° to +85°C
MCM-7709-0N   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

|	
LPM-7709-0L	STD Bus unpopulated battery backed memory card
LPM-7709-8L	8Kbyte battery backed memory
LPM-7709-16L	16Kbyte battery backed memory
LPM-7709-32L	32Kbyte battery backed memory
LPM-7709-64L	64Kbyte battery backed memory
MCM-7709-0N	STD Bus unpopulated battery backed memory card
MCM-7709-8N	8Kbyte battery backed memory
MCM-7709-16N	16Kbyte battery backed memory
MCM-7709-32N	32Kbyte battery backed memory
MCM-7709-64N	64Kbyte battery backed memory

WinSystems, Inc.

FEATURES

- Allows two STD Bus systems to be connected via 1K x 8 Dual Port RAM
- Fully asynchronous operation from either STD Bus system
- Multiple MCM-DPRAMs can be installed in a system
- Operates in Polled Mode or with Interrupts
- Operates with 16-, 20-, or 24-bit address bus
- Can be located anywhere within the memory map
- No complicated software routines required
- Language independent
- Available for CMOS STD Bus: LPM-DPRAM
- Low Cost
- +5 volt only operation

The LPM/MCM-DPRAM is a fully asynchronous, STD Bus, 1K x 8, dual port RAM board designed to link together two independent STD Bus systems. The LPM/MCM-DPRAM can be used to implement system redundancy or to provide a means by which concurrent or parallel processing can be achieved with very high throughput between the STD Bus systems.
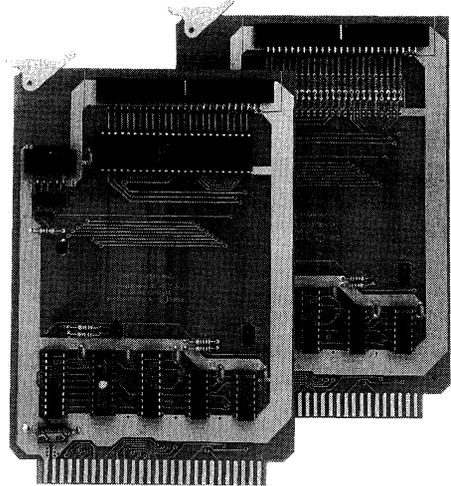
FUNCTIONAL CAPABILITY

Bus Interface - The LPM/MCM-DPRAM is a 2 board set. A separate board plugs into each STD Bus system and is connected via a 50-pin ribbon cable.

Addressing - Each board appears simply as a 1K x 8 memory device in the memory map. The dual port RAM board is not dependent upon processor type and

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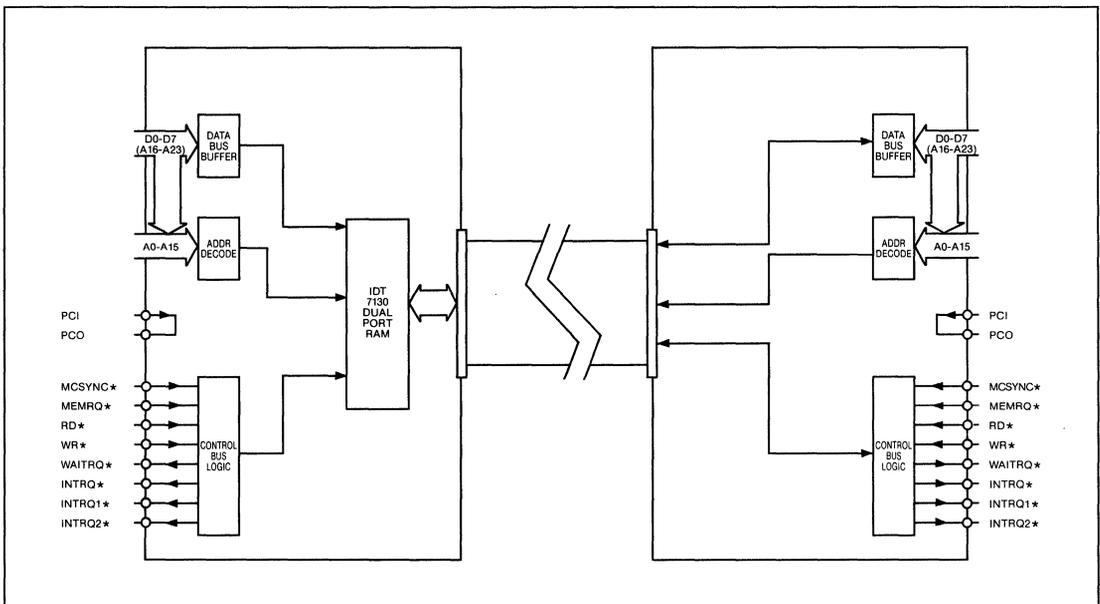
will work with non-multiplexed 16-bit or multiplexed 20- or 24-bit address busses. Either board can be jumpered to support 64KB, 1MB or 16MB direct addressing so that different processor types can be linked together through memory. For example, an existing Z80 system could be linked to an STD-AT with the MCM-DPRAM.

Dual Port Memory - The LPM/MCM-DPRAM is based upon the IDT7130 CMOS Dual-Port 1K x 8 Random Access Memory. It features very low power operation and very high speed access. The device provides two independent ports with separate control, address and I/O pins that permit independent asynchronous access for Reads or Writes to any location in its memory.

The dual port memory is 8-bits wide. It will work directly with 8085, Z80, 64180 CPUs as well as with the Intel 80X88 and V20/V40 type architectures. For use with processors having 16-bit wide data paths such as the 80186/V50, data must be transferred in an 8-bit mode only. WinSystems' 80286 and 80386SX based STD-AT systems will automatically and dynamically determine that the MCM-DPRAM is an 8-bit memory card and automatically Reads or Writes data at its memory locations with no program intervention required.

Arbitration - The IDT7130 chip has arbitration logic that will resolve the situation when both systems simultaneously access the same memory location. A Busy flag will become active which is tied to the delayed system's STD Bus WAITRQ* line. The Busy flag is set at such speeds that permit the processor to hold the operation and its respective address and data. The Busy flag will reset when the system granted access completes its operation.

Interrupts - The LPM/MCM-DPRAM can be used in either a Polled or Interrupt Mode. An interrupt flag permits communications between memory ports or systems. Each system can independently generate an interrupt message to the other by simply writing to a memory location (mail box or message center) which is assigned to each memory port. The message (8-bits located in 3FE or 3FF) is user defined. If interrupts are not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the 1K x 8 RAM.

Interrupts can be enabled or disabled with jumpers onboard the LPM/MCM-DPRAM boards. The interrupts can be either supported over the STD Bus backplane (INTRQ*, INTRQ1*, and INTRQ2*) or frontplane as defined by the STD Bus Recommended Practice.

Applications - The LPM/MCM-DPRAM is ideal for applications requiring high speed, closely linked systems in a distributed processing environment. Processor intensive tasks such as serial communications, PID calculations, intelligent machine control, real time process interfacing, etc. can be easily tied together. Multiple LPM/MCM-DPRAMs can be installed into a single chassis for larger, more complex systems.

CMOS STD Bus - The LPM-DPRAM is the CMOS STD Bus version for use in extended temperatures or very low power applications.

SPECIFICATIONS

Electrical

Data Transfer: 8-bit only, random access 1Kbyte memory with 16-, 20-, or 24-bit address decoding.

Power Requirements

Vcc = 5VDC $\pm$5% @110 mA typical: MCM-DPRAM
    = 5VDC $\pm$10% @90 mA typical: LPM-DPRAM

Mechanical

Dimensions: 4.5" x 6.5"

PC Board: FR4 Epoxy glass, 2 layer. Solder mask on both sides, screened component legend, plated through holes and gold plated edge card fingers.

Connectors

Jumpers: 0.025" square posts
Intra Board: 50-pin on 0.100" grid

Environmental

Operating Temperature: LPM-DPRAM - 40° to +85°C
                       MCM-DPRAM 0° to +65°C
Non-condensing relative humidity: 15% to 95%

ORDERING INFORMATION

MCM-DPRAM Dual port RAM board and cables.
LPM-DPRAM   CMOS STD Bus version of MCM-DPRAM

WinSystems, Inc.

FEATURES

- Z80 and HD64180 Compatible
- 2.5MHz or 4.0MHz compatible with no wait states
- 64K or 128K bytes of dynamic RAM
- Bank switch memory supported to 512K bytes
- User selectable common memory area
- DMA supported
- Mostek MDX-RAM64/128 compatible
- Single +5 volt supply

The MCM-DRAM64/128 is a STD-Z80 compatible +5 volt only dynamic RAM card providing high density memory storage for the STD Bus. The card contains either 65,536 (64K) bytes or 131,072 (128K) bytes for access of information by the computer or peripherals via DMA control.

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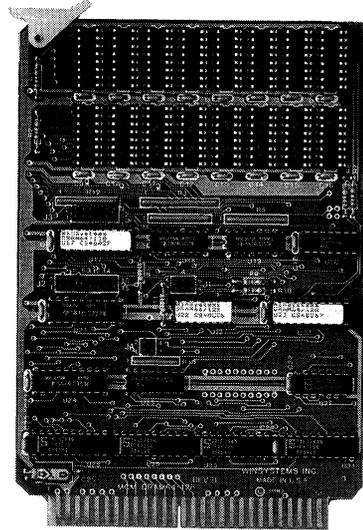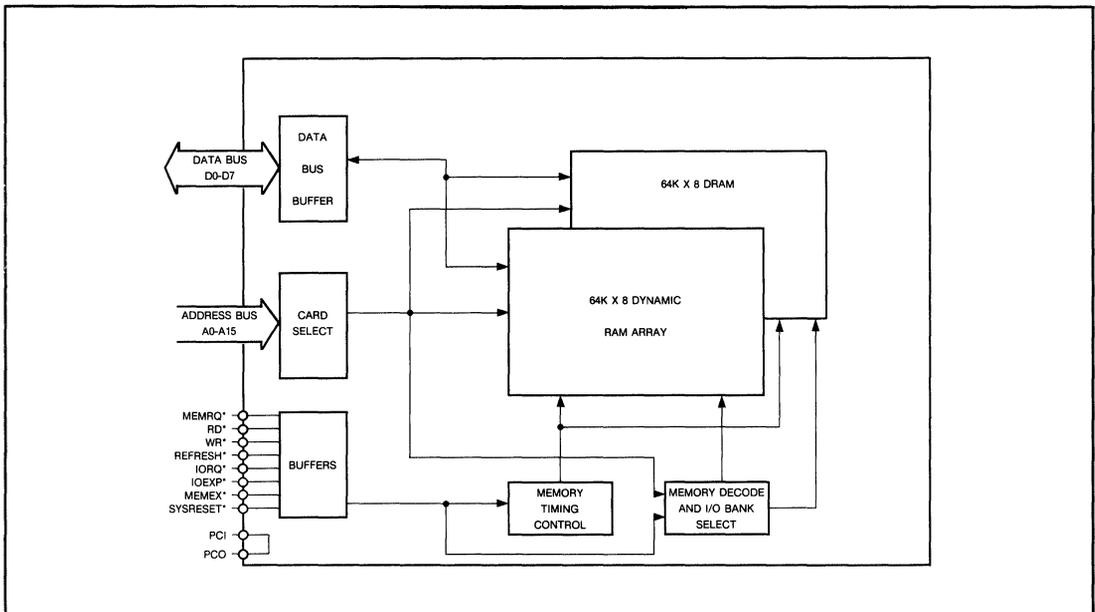
FUNCTIONAL CAPABILITY

The MCM-DRAM64/128 is a STD-Z80 dynamic RAM memory expansion board. It is available in 2 versions: MCM-DRAM64 and MCM-DRAM128. A population option provides either 64K or 128K bytes of memory.

The memory is logically oriented in two banks of 8 x 64K dynamic RAMs. The first 64Kb of memory is addressed directly and above 64K, a bank select addressing scheme is supported.

Provisions are made for user selectable common memory areas. This common area of memory remains enabled regardless of which bank has been selected providing a common memory area for the control program. The beginning and ending addresses are selectable on any 2K boundary. Up to 8 banks can be selected allowing support of 512K bytes of memory by using multiple boards. Memory cells will be refreshed regardless of whether they reside in the enabled bank.

The MCM-DRAM64/128 memory refresh circuitry utilizes the automatic transparent STD-Z80 REFRESH* signal which requires no complicated or inefficient processor intervention. This board can not be used with processors such as the 8088 that do not provide the REFRESH* signal.

The MCM-DRAM64/128 supports both jumper selectable MEMEX and IOEXP for expansion.

The MCM-DRAM64/128 is a functional replacement to the Mostek MDX-DRAM64/128 card.

SPECIFICATIONS

Electrical

System Clock: Up to 4.0 MHz

Memory Capacity: MCM-DRAM64   65,536 bytes
                 MCM-DRAM128   131,072 bytes

Page Mode Addressing: Up to 512K bytes can be supported in Z80 based systems via page mode control through I/O port FFh

Common Memory: The beginning and ending area of common memory can be selected on a 2K byte boundary with a jumper option on-board

Interfaces: System: STD-Z80 compatible

Power Requirements: +5 VDC ± 5% at 1500 mA (max)

Mechanical

Card Dimensions: 4.5 x 6.5 inches

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

System: 56-pin dual 0.125 inch centers

Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-DRAM64   64K byte dynamic RAM card operating at 4.0 MHz with operations manual

MCM-DRAM128 128K byte dyanmic RAM card operating at 4.0 MHz with manual.

WinSystems, Inc.

FEATURES

- Eight 28-pin Bytewide compatible memory sockets that will accept 2K x 8, 4K x 8 or 8K x 8 byte devices
- Processor independent including V30, 80C88, V20, NSC-800 HD64180, 80C85A, Z80, and 6502
- Supports 16 or 20-bit direct addressing
- Compatible with STD-8088 1 Megabyte Addressing
- Supports any mix of up to 64K bytes of EPROM, RAM or Dallas Semiconductor nonvolatile RAMs
- Page Mode Operation for up to sixteen boards per system
- Replaces Pro-Log 77C02 and 77C08
- Single +5 Volt operation
- Available for CMOS STD Bus: LPM-UMC

The LPM/MCM-UMC is a STD Bus and CMOS STD Bus bytewide memory expansion card with eight 28-pin JEDEC sockets which can be populated with RAMs, ROMs, EPROMs or battery backed RAMs to accomodate up to 64K bytes of memory. It is designed to support all the STD Bus processor types including the CMOS Z80, 80C85A, NSC-800, HD64180, 6502, 80C88, V20, V30, V40 and V53.

## FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-UMC is the CMOS STD Bus version and the MCM-UMC is the STD Bus version

of this card. The LPM/MCM prefix indicates the card has the same features and funtionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

5

SHADING INDICATES SOCKETS ONLY
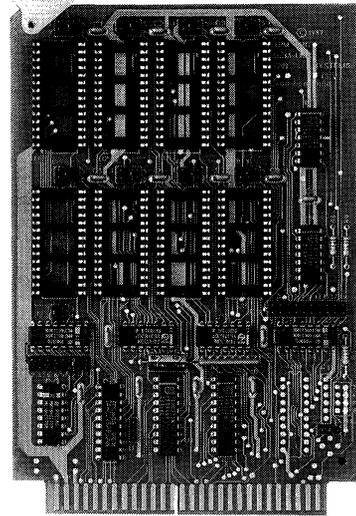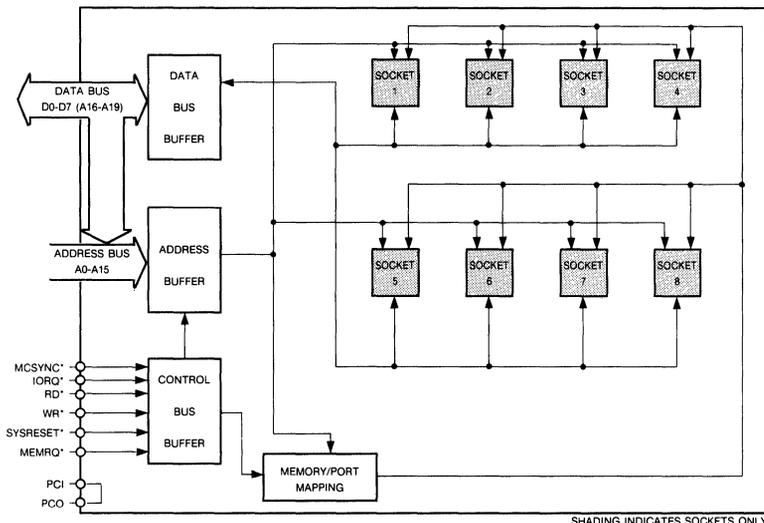
Addressing - This card can be used with either 16-bit addressing or direct 20-bit addressing methods. Using the 20-bit address multiplexing configuration, up to lM byte of memory may be directly addressed by 80C88, V20, V30 or HD64180 based systems. A0 through A15 are received directly from the address bus and the LPM/MCM-UMC demultiplexes the remaining four address lines A16 - A19 from the data bus. More than one LPM/MCM-UMC card can be in a STD Bus and CMOS STD Bus system providing up to a full 1 Megabyte of directly addressable memory.

When used with 8-bit processors that generate only a 16-bit memory address, the card supports up to 64K bytes of direct addressing.

The LPM/MCM-UMC also has a page mode operation to allow up to 16 LPM/MCM-UMC boards per STD Bus and CMOS STD Bus system. The page mode circuit operates from a write only I/O port located at address FFh. It writes up to 16 individual page numbers to an on-board latch which enables/disables the memory board. This circuit is used by 8-bit processors that do not support other memory management techniques for memory addressing beyond 64K bytes.

Memory - The board contains eight JEDEC standard 28-pin sockets that are configured to support 2K, 4K, or 8K byte, 24 or 28-pin devices for a maximum of 64K bytes of RAM or EPROMs per board.

The LPM/MCM-UMC will also support the Dallas Semiconductor nonvolatile 2K x 8 and 8K x 8 memory modules. These units are fully static RAMs with a self contained lithium energy source and control circuitry that monitors Vcc for an out of tolerance condition. When such a condition occurs, the energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. There is no limit on the number of write cycles which can be executed and no additional support circuitry required. The devices have over 10 years of data retention. For additional information call Dallas Semiconductor at (214) 450-0400.

This board is a functional replacement to the Pro-Log 77C02 and 77C08.

SPECIFICATIONS

Electrical

Vcc = +5 volts ± 10% at 3mA typ. without on board
    memory: LPM-UMC
Vcc = +5 volts ± 5% at 300mA typ. without on board
    memory: MCM-UMC

Memory

Memory Capacity: Eight 28 pin bytewide memory
                sockets. Each socket can be strap-
                ped for 2K, 4K or 8K RAM or
                EPROM devices.

Page Mode: Up to 16 boards per system controlled by
           I/O port FFh.

Mechanical

Meets STD Bus mechanical specifications;
        4.5 x 6.5 inches

PC Board: FR4 epoxy glass. Solder mask on both sides,
          screened component legend and plated
          through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers

Jumpers: 0.025" square posts

Environmental

Operating Temperature:
    LPM-UMC   -40°C to +85°C
    MCM-UMC   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-UMC   Universal 64K bytewide CMOS STD Bus
           memory card.

MCM-UMC   Universal 64K bytewide STD Bus
           memory card.

WinSystems, Inc.

FEATURES

- Eight 28-pin JEDEC standard sockets supporting RAM, ROM, EPROM, and EEPROMs
- Supports 16 or 20-bit direct addressing
- Supports up to 512K bytes of EPROM
- Processor independent 68008, HD64180, 80C85A, Z80, NSC800 and 6809
- Onboard flexible address decoding
- Optional power fail detect logic
- MEMEX supported
- Available for CMOS STD Bus: LPM-UMC2

The LPM/MCM-UMC2 is a STD Bus and CMOS STD Bus bytewide memory expansion card with eight 28-pin JEDEC sockets which can be populated with RAMs, ROMs, EPROM or EEPROMs to accomodate up to 256K bytes of memory in any combination to provide the total memory requirements for many STD Bus systems. It is ideal for mass storage of the 8/16-bit processors requiring greater than 64K of memory. It is designed to support all the STD Bus processor types including the NSC800, Z80, 80C85A, HD64180, 6809, 80C88, 80188, V40 and V53.
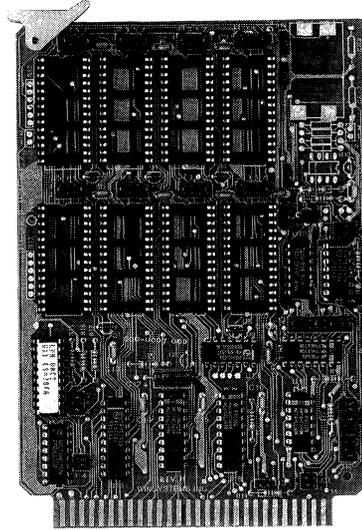
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-UMC2 is the CMOS STD Bus version and the MCM-UMC2 is the STD Bus version of this card. The LPM/MCM prefix indicates

the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

SHADING INDICATES SOCKETS ONLY
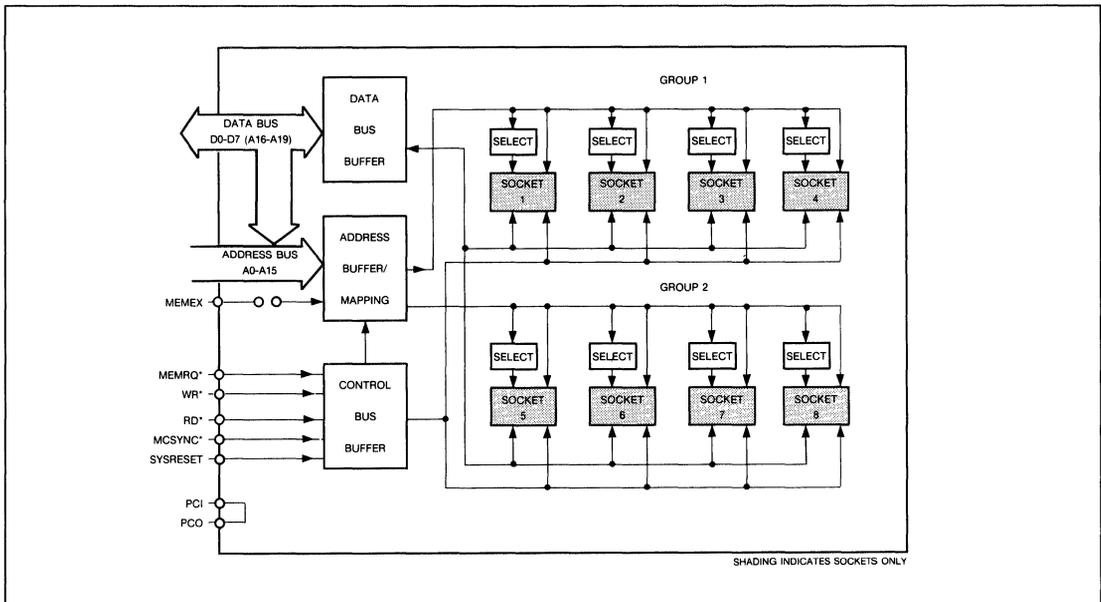
Addressing - This card can be used with either 16-bit addressing or direct 20-bit addressing methods. Using the 20-bit address multiplexing configuration, up to 1Mbyte of memory may be directly addressed by 80C88, 68008 or HD64180 based systems. A0 through A15 are received directly from the address bus and the LPM/MCM-UMC2 demultiplexes the remaining four address lines A16 - A19 from the data bus. More than one LPM/MCM-UMC2 card can be in a STD Bus system providing up to a full 1 Megabyte of directly addressable memory. The LPM/MCM-UMC2 will also respond to the MEMEX signal which allows an additional 1 Mbyte of memory to be accessed or used for bootstrapping. When used with 8-bit processors that generate only a 16-bit memory address, the card supports up to 64K bytes of direct addressing.

Memory - The board contains eight JEDEC standard 28-pin sockets that are configured to support 8K, 16K, 32K, or 64K byte devices for a maximum of 256K bytes of RAM or 512K bytes of EPROM per board. The socket size is configurable on a per group basis and 2 groups are available per board. Each group has its own user-selectable base address in the 20-bit address range. The starting address for each group is independent and does not have to be contiguous with the other group. Each group must start on a boundary that is multiple of the group's size. For example, four 8K byte RAMs (32K total) would start on a 32K byte boundary; however, four 32K byte EPROMs would start on a 128K byte boundary.

The socket size is configured on a group basis. Therefore, one group could be set for 8K byte devices and the other group could be set for 32K byte devices. Any combination of RAM, ROM, EPROM, or EEPROMs can be made in the group as long as the memory device is the same capacity as the configured socket.

Reset - An optional power fail detect circuit is available that continuously monitors the Vcc line for an out of tolerance condition. If the power drops below 4.5 volts the circuit is activated. Jumper options allow the signal to inhibit the write lines on the board which is mandatory in order to support EEPROMs. The reset signal can also be jumpered to drive pin 6 (VBB#2/ DCPD*) active on the STD Bus and CMOS STD Bus.

Battery Backup - An optional 750 mA-hour lithium battery will provide backup power for CMOS static RAMs in either or both groups of sockets. This product is designated as the LPM/MCM-7709 described in a separate Data Sheet.

SPECIFICATIONS

Electrical

Vcc = +5 volts $\pm$ 10% at 10mA typ. without onboard memory: LPM-UMC2
Vcc = +5 volts $\pm$ 5% at 350mA typ. without onboard memory: MCM-UMC2

Mechanical

Meets STD Bus mechanical specifications

Connectors

Jumpers: 0.025″ wirewrap posts on 0.1″ centers

Environmental

Operating Temperature:

LPM-UMC2	-40° to +85°C
MCM-UMC2	0° to +60°C

Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

|	
LPM-UMC2	CMOS STD Bus Universal bytewide memory card
LPM-UMC2-P	LPM-UMC2 with powerfail detect option
LPM-7709-0L	LPM-UMC2-P with lithium battery
MCM-UMC2	STD Bus Universal bytewide memory card
MCM-UMC2-P	MCM-UMC2 with powerfail detect option
MCM-7709-0N	MCM-UMC2-P with lithium battery

WinSystems, Inc.

FEATURES

- 1 Megabyte memory expansion board
- Eight Bytewide memory sockets accept 32Kx8, 64Kx8, or 128Kx8 RAMs, EPROMs, EEPROMs or psuedo-static RAMs
- Supports 16/20/24-bit addressing for use with the 80C286, 80386SX, V40, 80C88, Z80, 80C85, or 64180 CPUs for processor independent operation
- Optional battery back up for static RAMs
- RAM/EPROM disk driver software available for use with the WinSystems' STD-AT and ROM-DOS applications
- Memories can be addressed as one bank of eight or as separate devices
- Will work in "Page Mode" for extending memory space for Z80/80C85 or 80C88/188/V40 processor boards
- Available for CMOS STD Bus: LPM-UMC4

The LPM/MCM-UMC4 is a highly versatile, universal memory card designed to support all the STD Bus and CMOS STD Bus processor types that require 8-bit data transfers. It features eight, 32-pin memory sockets which can be populated with up to 1 Megabyte of RAMs, battery backed RAMs, ROMs, EPROMs, EEPROMs, or psuedo-static RAMs in any mix. This card is ideal for RAM/ROM disks for PC/XT/AT systems or embedded systems applications requiring non rotational program and data mass storage.
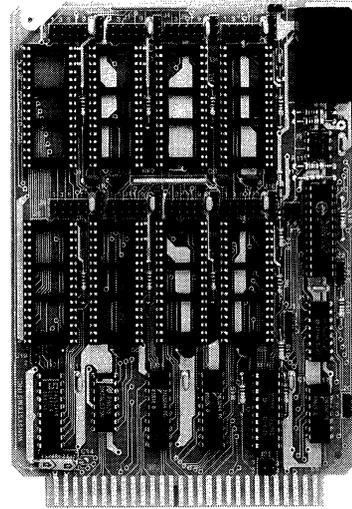
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-UMC4 is the CMOS STD Bus version and the MCM-UMC4 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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SHADING INDICATES SOCKETS ONLY
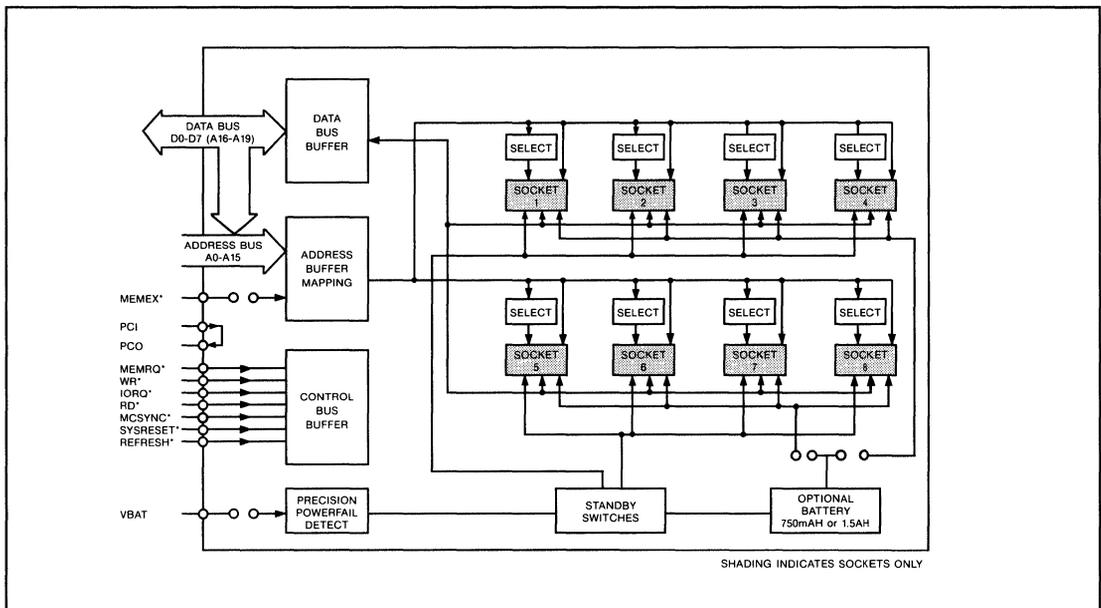
Addressing - This card can be used with 16-, 20- or 24-bit addressing methods which support Z80 through 80486DX CPUs. Using the 20- or 24-bit address multiplexing configuration, up to 1MB or 16MB respectively of memory can be directly addressed by the CPU. A0 through A15 are received directly from the address bus and the LPM/MCM-UMC4 demultiplexes the remaining address lines A16 - A23 from the data bus.

When 24-bits are decoded, direct addressing to 16 MBytes is supported for 80286-80486DX and V53 processors. Since the LPM/MCM-UMC4 is an 8-bit memory card, processors such as the 80C286/386/486 must transfer data in a byte mode. With 20-bit decoding, direct addressing of 1 MByte is supported for 80C88, V40, 80C188, and 64180 type CPU's. Finally, 16-bit memory addressing is supported for direct addressing of 64KBytes for 80C85, 6809, Z80, and NSC800 type processors.

The page mode is provided in the 16- and 20-bit address decoder to offer extended memory space. A page mode circuit operates from a Write Only I/O port located at address 200H. It writes to the individual page numbers to an onboard latch which enables/disables the memory board. The circuit is used by processors that do not support other memory management techniques for memory addressing beyond 64KB or 1MB. Sixteen pages are available for 20-bit addressing and 256 pages for 16-bit addressing.

Memory - The LPM/MCM-UMC4 has eight, 32-pin byte-wide memory sockets that will accept 32K x 8, 64K x 8, or 128K x 8 RAMs, psuedo-static RAMs, EPROMs, or EEPROMs. The board can support any mix of these memory devices to offer different population options for specific customer application.

Pseudo-static RAM support incorporates features and benefits from both DRAMs and SRAMs. The device is similar to a DRAM since it needs a 4 mS refresh; however, it will fit into a standard 28- or 32-pin bytewide memory socket and access just like a SRAM. This means that a standard bytewide socket accepts a lower cost, high density, high speed RAM offering more memory flexibility to the board.

Battery-backed operation - A 750mA-hour lithium battery provides backup power for the CMOS static RAMs in any of the memory socket. It will provide thousands of hours of backup. The exact time is a function of standby current and number of CMOS RAMs used. External battery power is also jumper selectable from the VBat pin on the STD Bus and CMOS STD Bus. The LPM/MCM-UMC4-BAT is a special version of the LPM/MCM-UMC4 that allows the user to install from 0K to 1024KBytes of battery protected low power SRAM. Each socket on the LPM/MCM-UMC4-BAT can be individually addressed, and powered by Vcc or optional battery stand-by voltage. Unused sockets can also be filled with EPROMs or EEPROMS.

SPECIFICATIONS

Electrical

Vcc = +5 volts $\pm$10% at 95mA typ. without onboard memory: LPM-UMC4
Vcc = +5 volts $\pm$5% at 300mA typ. without onboard memory: MCM-UMC4

Memory Capacity: Eight, 32-pin bytewide sockets for 32Kx8, 64Kx8, or 128Kx8 memory devices. (RAMs, EPROMs, EEPROMs, and psuedo-static RAMs.)

Optional Battery: 750 mA-Hour Lithium

Mechanical

Meets STD Bus mechanical specifications

Connectors

STD Bus: 56-pin dual 0.125 centers
Jumpers: 0.025" square posts

Environmental

Operating temperature:
    LPM-UMC4   -40°C to +85°C
    MCM-UMC4   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-UMC4	CMOS STD Bus 1 MByte (unpopulated) memory card
LPM-UMC4-BAT	LPM-UMC4 with battery and power-fail reset installed
MCM-UMC4	STD Bus 1 MByte (unpopulated) memory card
MCM-UMC4-BAT	MCM-UMC4 with battery and power-fail reset installed

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

I/O Cards

Disk Controllers/Mass Storage

Video/Graphics Controllers

Networking/Communications Controllers

6

I/O Cards

Serial and Parallel I/O

I/O Cards

Analog Input/Output

Miscellaneous

MCM prefix on a product name designates a STD Bus card and a LPM prefix designates a CMOS STD Card. The LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS STD Bus and STD Bus logic. The differences between these products are the various power requirements and operational temperature ranges.

Disk Controller Selection Guide

PRODUCT	BUS INTERFACE	FLOPPY DRIVE SUPPORTED	HARD DISK	SILICON DISK	INTEGRATED WITH MEMORY
LPM-DISK-AT	CMOS STD Bus	3½″, 5¼″	IDE	—	No
MCM-DISK-AT	STD Bus				
LPM-DISK-XT	CMOS STD Bus	3½″, 5¼″	SCSI	—	No
MCM-DISK-XT	STD Bus				
LPM-DSKIO	CMOS STD Bus	3½″, 5¼″	IDE	—	No
MCM-DSKIO	STD Bus				
LPM-SCSI	CMOS STD Bus	—	SCSI	—	No
MCM-SCSI	STD Bus				
LPM-SSD	CMOS STD Bus	—	—	RAM/ROM	Yes
MCM-SSD	STD Bus				
LPM-USSD	CMOS STD Bus	—	—	RAM/ROM PEROM (FLASH)	Yes
MCM-USSD	STD Bus				

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Mass Storage Device Selection Guide

PRODUCT	MEDIA	INTERFACE	MAXIMUM CAPACITY
FD3-720	3.5" Floppy Disk	PC-Micro Floppy	720 KBytes
FD3-144	3.5" Floppy Disk	PC-Micro Floppy	1.44 MBytes
FD3-21M	3.5" Floptical Disk	PC-Micro Floppy	21 MBytes
HDAT	3.5" Hard Disk	IDE	40/100/200 MBytes
HDXT	3.5" Hard Disk	SCSI	40 MBytes
LPM-SSD MCM-SSD	RAM/ROM Disk	CMOS STD Bus STD Bus	1 MBytes
LPM-USSD MCM-USSD	RAM/ROM PEROM (FLASH)	CMOS STD Bus STD Bus	4 MBytes

WinSystems®

STD BUS, CMOS STD BUS

LPM-DISK-AT
MCM-DISK-AT
IDE/FLP Disk Interface

FEATURES

- Hard Disk interface and Floppy Disk controller on a single card
- Supports up to two 40, 100, 200 Mbyte IDE compatible 3.5 inch hard drives
- Supports up to two 3.5 and/or 5.25-inch floppy disk drives
- 16-bit hard disk transfers for maximum data transfer rates
- Supports WinSystems' FD3-720 and FD3-144 micro-floppy disk subsystem
- Supports WinSystems' HDAT-40/100/200 3.5 inch hard drive subsystems
- Hard disk activity LED
- Interrupt driven
- Supports DMA transfers
- Direct STD-AT compatible, no BIOS extension required
- Single +5 volts only required
- Available for CMOS STD Bus: LPM-DISK-AT

The LPM/MCM-DISK-AT supports both 3.5 inch (IDE compatible) Conner's Peripheral hard disk drives and 3.5 inch or 5.25 inch floppy disk drives on the STD Bus with a storage capacity of over 400 Megabytes. It is directly compatible with WinSystems' LPM/MCM-286/386/486 and the STD-AT, the industrial PC-AT compatible 80286/386/486 based STD Bus systems.
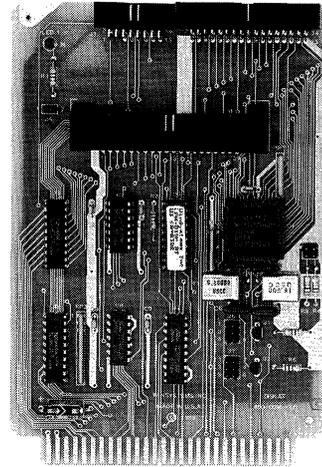
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-DISK-AT is the CMOS STD Bus version and the MCM-DISK-AT is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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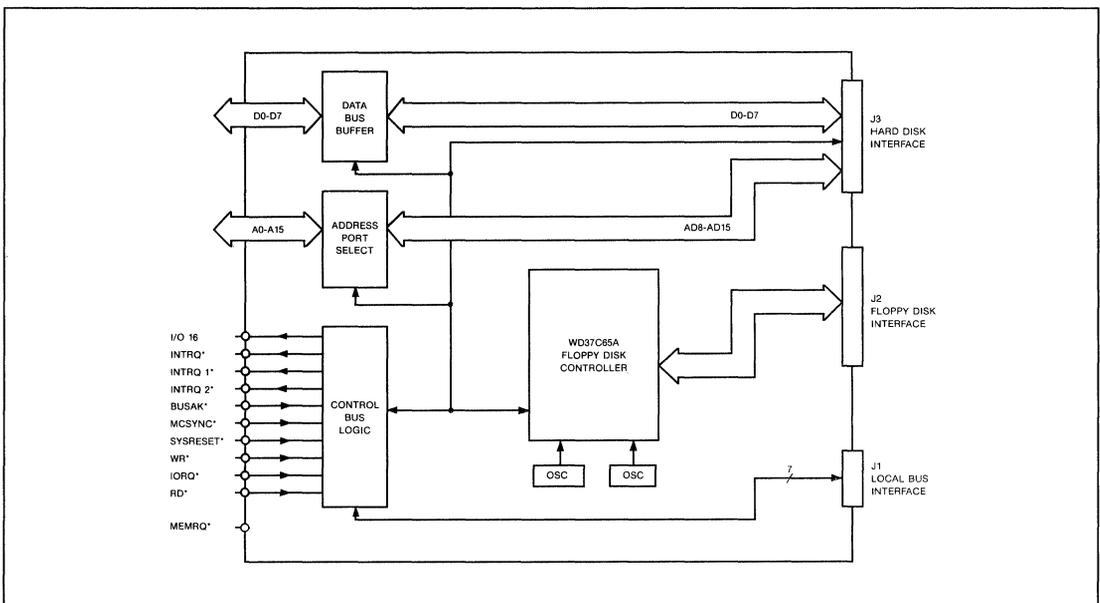
Interrupts and DMA - Both interrupts and DMA are supported on the card. The interrupts are jumper selectable as INTRQ*, INTRQ1* or INTRQ2*.

Floppy Disk Controller - The LPM/MCM-DISK-AT utilizes the Western Digital WD37C65A to handle all floppy disk operations to support two (A: and B:) 720KB or 1.44MB 3.5 inch and/or 360KB or 1.2MB 5.25 inch disks with both interrupt and DMA operations. The WD37C65A provides all the needed functionality to control a floppy disk drive on a single chip including the formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

The controller chip is fully DOS compatible and will accept DOS commands directly. The output from the chip will drive 2 floppy drives. Resistive termination should be installed only on the drive farthest from the LPM/MCM-DISK-AT.

WinSystems offers the FD3-720 which is a 3.5 inch double sided, double density, micro-floppy disk drive mounted on an STD Bus board that can be easily installed directly inside an STD Bus card cage. The FD3-144 is the 1.44Mbyte version. This configuration provides a 720Kbyte or 1.44Mbyte storage capacity and is quite popular due to its removable media, in-rack mounting, and low cost.

Hard Disk Interface - The hard disk interface is a IDE compatible interface to a Conner Peripherals micro Winchester 3.5 inch drive. The drive contains all the interface electronics to make it DOS compatible. Data is transferred in 16-bit words to the controller to maximize performance.

The HDAT-40/100/200 is the WinSystems' hard disk subsystem that mounts a 3.5 inch Conner Peripherals 40, 100 or 200 megabyte (formatted) hard disk drive on a STD Bus card. It easily fits inside a card cage. Two HDAT-200's can be supported by the LPM/MCM-DISK-AT in a STD-AT system to provide up to 400 megabytes of storage in addition to up to 2 floppy disk drives.

A totally sealed head/disk assembly and automatic head landing zone protect the head, media and data from shock up to 50G's. Microprocessor controlled diagnostic routines and automatic error correction maintain data integrity. Data is 2,7 Run Length Limited

(RLL) coded to further assure maximum data density and high transfer rates. An embedded servo assures data integrity by maintaining precise alignment of each read/write head over the data throughout the operating temperature range.

The data to and from the disk is routed through a FIFO buffer to improve the continuous data transfer rate. The interface to the STD Bus and CMOS STD Bus is 16-bits wide for higher data rates. An activity LED is onboard that blinks whenever the hard disk is being accessed.

Cabling - Disk drives can be bought separately or as individual products from WinSystems. Multiple drives can used in a system and wired to the LPM-DISK-AT with either the CBL-125-1 or CBL-126-1. The CBL-125-1, a 34-pin ribbon cable, interfaces the LPM-DISK-AT to the FD3-720 or FD3-144 micro-floppy disk subsystem. The CBL-126-1, a 40-pin ribbon cable, interfaces the LPM/MCM-DISK-AT to the HDAT-40/100/200.

SPECIFICATIONS

Electrical
Power Requirements: +5 VDC ± 5% at 100 mA typ.

Mechanical
Meets STD Bus mechanical dimensions

Connectors
Floppy interface: 34-pin on 0.100" grid
Hard disk interface: 40-pin on 0.100" grid

Environmental
Operating Temperature:
    LPM-DISK-AT   0°C to +70°C
    MCM-DISK-AT 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDER INFORMATION

LPM-DISK-AT	Winchester/Floppy disk interface card
MCM-DISK-AT	Winchester/Floppy disk interface card
CBL-125-1	34-pin ribbon cable from the LPM-DISK-AT to FD3-720 or FD3-144
CBL-126-1	40-pin ribbon cable from the LPM-DISK-AT to the HDAT-40, HDAT-100

WinSystems, Inc.

FEATURES

- SCSI interface and Floppy Disk controller on a single STD Bus and CMOS STD Bus card
- Uses an NCR 53C80 type SCSI controller
- Asynchronous transfer rate up to 4 MBytes/sec
- Multiple host adapters can be attached
- DMA, pseudo-DMA or polled I/O with interrupt on completion
- On chip SCSI Bus drivers capable of sinking 48mA
- Supports up to two 3.5 and/or 5.25 inch floppy disk drives
- EPROM socket for BIOS extensions
- Available for CMOS STD Bus: LPM-DISK-XT
- Single +5 volts only required
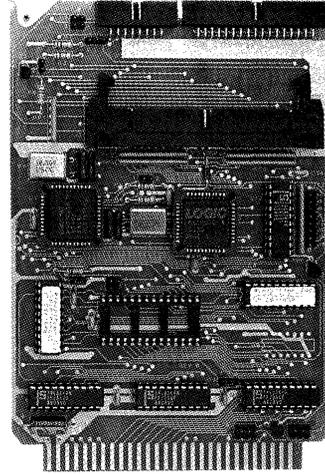
The LPM/MCM-DISK-XT supports both and 3.5 inch or 5.25 inch floppy disk drives on the STD Bus and CMOS STD Bus. It is designed to provide mass storage access for STD Bus and CMOS STD Bus XT/AT systems or non-DOS embedded systems.

The LPM/MCM-DISK-XT is also a Small Computer Systems Interface (SCSI) host adapter card. It permits multiple peripherals such as disk drives, WORM and optical drives, printers, tape streamers, computers, network gateways, etc. to be linked to the STD Bus and CMOS STD Bus in a very low cost manner.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-DISK-XT is the CMOS STD Bus version and the MCM-DISK-XT is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

*SHADING INDICATES SOCKET ONLY
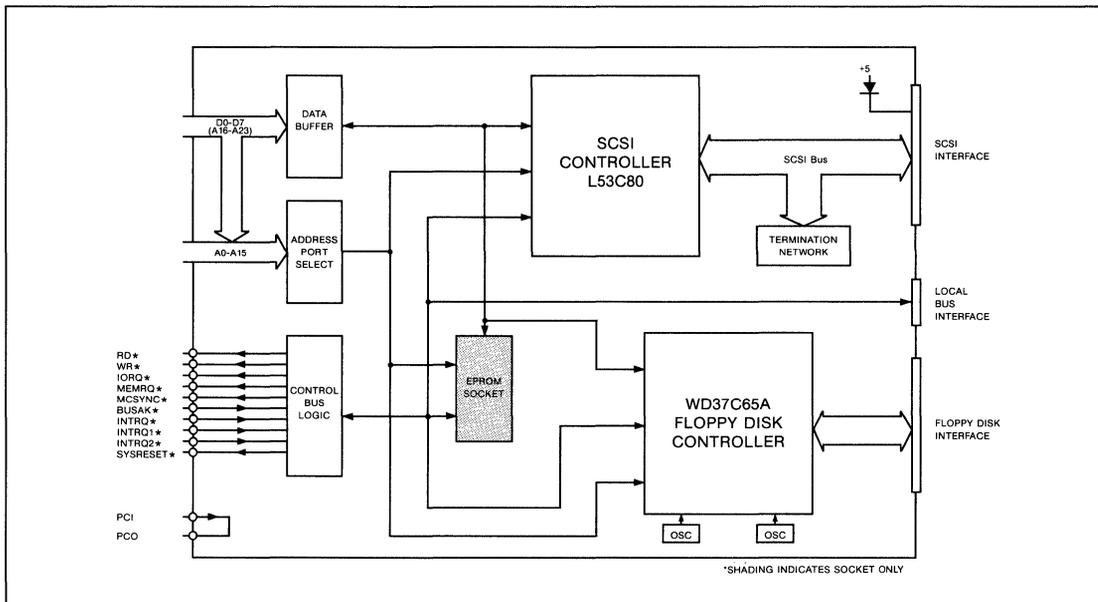
Interrupts and DMA - Both interrupts and DMA are supported on the card. The interrupts are jumper selectable as INTRQ*, INTRQ1* or INTRQ2*

Floppy Disk Controller - The LPM/MCM-DISK-XT utilizes the Western Digital WD37C65A to handle all floppy disk operations to support two (A: and B:) 720KB or 1.44MB 3.5 inch and/or 360KB or 1.2MB 5.25 inch disks with both interrupt and DMA operations. The WD37C65A provides all the needed functionality to control a floppy disk drive on a single chip.

The controller chip is fully BIOS compatible and will accept DOS commands directly. The output from the chip will drive 2 floppy drives directly.

SCSI Interface - The LPM/MCM-DISK-XT is a complete interface to the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.0 committee. The LPM/MCM-DISK-XT offers the ability to interface different peripherals to the STD Bus through an industry standard architecture. Devices including printers, streaming tapes, disk drives, network gateways, and various other storage devices can be linked with this board. This allows several devices to communicate with either a single host or multiple hosts and devices. When several unlike devices need to be joined together, the LPM/MCM-DISK-XT allows signals from one device to be translated and utilized by the other. This interface determines an entire bus system, allowing clear electrical paths and well-defined communication protocols.

SCSI Controller - The LPM/MCM-DISK-XT contains a very high performance, low cost, SCSI host adapter which supports the physical layer of the SCSI bus. It uses the Logical Devices' L53C80 CMOS controller which is pin and functionally compatible with the NMOS NCR 5380, yet it offers up to a 2.5 times performance improvement. The LPM/MCM-DISK-XT has the capability to operate in either DMA, pseudo-DMA, or programmed I/O Mode. It can be either an initiator or target which provides 8-bit wide data transfer speeds up to 4 MBytes per second.

Software - An EPROM socket is available for installation of a 8KB or 32KB integrated BIOS extension. The socket decodes both 20- and 24-bit memory maps for use with either the STD Bus and CMOS STD Bus XT or AT type systems. A standard SCSI BIOS extension is available for the LPM/MCM-DISK-XT.

Connector - The LPM/MCM-DISK-XT SCSI controller supports the standard 50-pin cable wiring convention. Each signal line is single ended and is capable of sinking 48 mA and has a 220/330 ohm termination network. The board is shipped from the factory with the termination network installed. The floppy drive connector is the standard 34-pin configuration.

Disk drives can be bought separately that can be installed directly into the STD Bus card cage. Both 720KB and 1.44MB 3.5″ floppy disk drives as well as 20 and 40MB SCSI 3.5″ hard disk drives are available. Interface cables are available for all the units.

SPECIFICATIONS

Electrical

Power Requirements: +5 VDC ±5% @ 700 mA typ.

Mechanical

Meets STD Bus mechanical dimensions

Connectors

Floppy interface: 34-pin on 0.100″ grid
SCSI interface: 50-pin on 0.100″ grid

Environmental

Operating Temperature:
    LPM-DISK-XT   0° to +70°C
    MCM-DISK-XT   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-DISK-XT   Winchester/SCSI disk controller Card
MCM-DISK-XT Winchester/SCSI disk controller Card

WinSystems, Inc.

WinSystems®

STD BUS, CMOS STD BUS

FEATURES

- Provides IDE hard disk interface for up to 2 drives
- Supports HDAT-40/100/200 drive subsystem
- Supports WinSystems' FD3-720 and FD3-144, 3.5" and/or 5.25" floppy disk subsystems
- EPROM socket for BIOS extensions
- PC-XT compatible keyboard interface
- Hard disk activity LED
- Dallas Semiconductor Real Time Clock
- Operational temperature range: 0°C to +65°C
- Requires +5 volts only

The LPM/MCM-DSKIO is a general purpose DOS system support card for use with the MCM-SBC41, MCM-SBC53 and other WinSystems' V40/V53 class CPUs. The card provides the peripheral interface electronics for floppy and hard disks, keyboard, real time clock, and BIOS ROM extension socket. This allows embedded SBCs to be configured to work with rotational media for complete PC type systems.

The MCM-DSKIO is the STD Bus version and the LPM-DSKIO is the CMOS STD Bus version of the card.
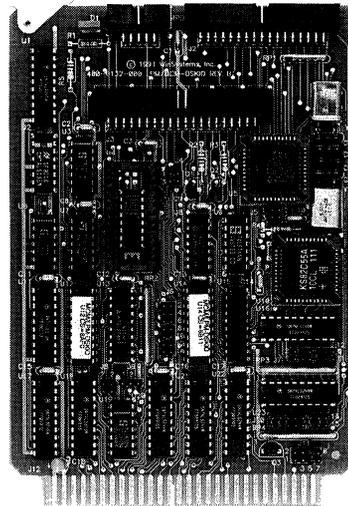
FUNCTIONAL CAPABILITY

Addressing - Full data, address, and control line buffering is provided to and from the STD Bus. The LPM/MCM-DSKIO supports 10-bit I/O addressing.

One memory socket is provided for a 8K - 64Kbyte EPROM mapped anywhere in the lower 1Mbyte memory address space. The socket decodes both

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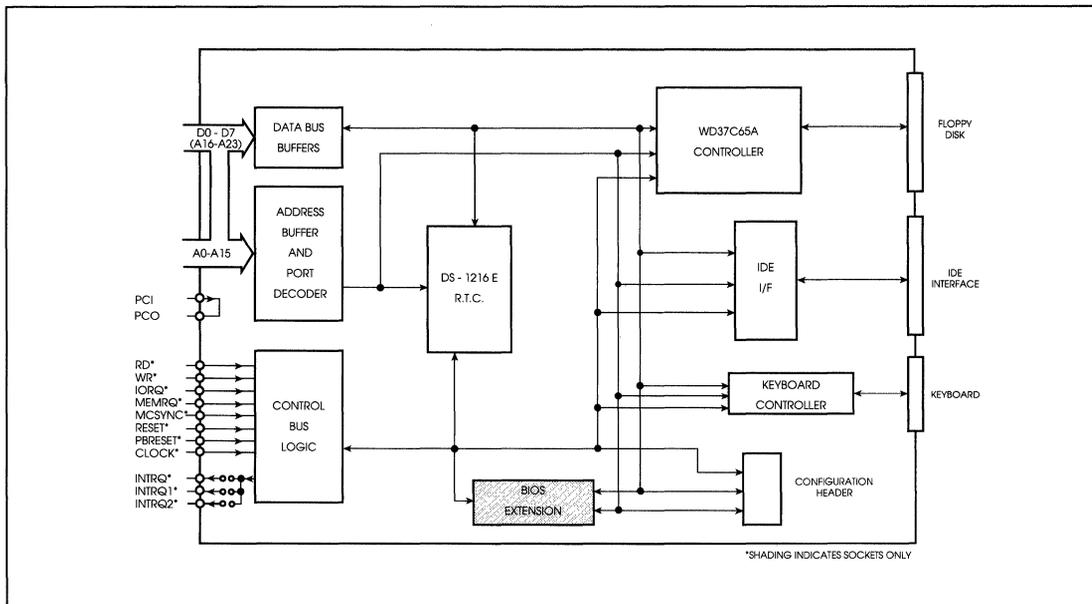
20- and 24-bit memory maps for use with either the STD Bus XT or AT type systems. It will accept BIOS extension code for use in conjunction with DOS or ROM-DOS systems. A BIOS EPROM is not required for regular WinSystems' XT systems.

Interrupts - Interrupts are generated by the keyboard and are jumper selectable as INTRQ*, INTRQ1* or INTRQ2* in any order on the STD Bus backplane.

Keyboard Interface - Any PC-XT compatible keyboard is supported by the LPM/MCM-DSKIO board. A 10-pin right angle connector is on the board with a adapter cable supplied for interface with the 5-pin "DIN" type female keyboard connector.

Floppy Disk Controller - The LPM/MCM-DSKIO utilizes the Western Digital WD37C65A to handle all floppy disk operations to support two (A: and B:) 720KB or 1.44MB 3.5 inch and/or 360KB or 1.2MB 5.25 inch disks. The WD37C65A provides all the needed functionality to control a floppy disk drive on a single chip.

A hardware jumper configuration header is provided so that software can read the type of hard and floppy disk drives that are installed with the board.

WinSystems offers the FD3-720 which is a 3.5 inch double-sided, double-density, micro-floppy disk drive mounted on an STD Bus board that can be easily installed directly inside an STD Bus card cage. The FD3-144 is the 1.4 Mbyte version. This configuration provides a 720KB or 1.44 MB storage capacity and is quite popular due to its removable media, in-rack mounting and low cost.

Hard Disk Interface - The MCM-DSKIO uses a direct IDE-compatible interface to the hard disk drive. This insures DOS compatibility and reduces the interface electronics complexity.

The HDAT-40/100/200 is the WinSystems' hard disk subsystem that mounts a 3.5 inch 40 - 200Mbyte (formatted) hard disk drive inside a card cage.

Real Time Clock - The LPM/MCM-DSKIO is populated with a Dallas Semiconductor SmartWatch. It is a 32-pin DIP socket with a built-in CMOS watch, power sequencer, and an embedded lithium energy source.

Since the battery is internal to the socket, there is no danger of shorting out or accidental discharge due to mishandling.

The SmartWatch is the lower portion of the onboard BIOS memory socket and permits either 28- or 32-pin bytewide EPROMS to be installed. This permits full utilization of all the LPM/MCM-DSKIO's BIOS memory socket while having a transparent battery-backed time keeping function.

The SmartWatch provides time keeping information including hundredths, tenths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. It operates in either 24-hour or 12-hour format with an AM/PM indicator.

Connectors - The LPM/MCM-DSKIO supports the standard 40-pin cable wiring convention for the hard disk, 34-pin connector for the floppy disk, and 10-pin DIN connector for the keyboard. The CBL-124-1 is supplied to adapt to a 5-pin DIN keyboard connector.

SPECIFICATIONS

Electrical
STD Bus compatible
LPM-DSKIO: +5VDC ± 5% @ 200 mA typ.
MCM-DSKIO: +5VDC ± 5% @ 400 mA typ.

Mechanical
Meets STD Bus mechanical dimensions: 4.5" x 6.5"

Connectors
Jumpers: 0.025" square posts
Floppy interface: 34-pin on 0.100" grid
Hard disk interface: 40-pin on 0.100" grid
Keyboard interface: 10-pin on 0.100" grid

Environmental
Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-DSKIO	CMOS STD Bus Dos support card
MCM-DSKIO	STD Bus DOS support card
CBL-126-1	HDAT interface cable
CBL-131-1	FD3-720/144 interface cable

WinSystems, Inc.

FEATURES

- ANSI X3T9.0 Small Computer Systems Interface (SCSI)
- Asynchronous transfer rate up to 4 MBytes/sec
- Multiple host adapters can be attached
- DMA, pseudo-DMA or polled I/O with interrupt on completion
- Uses an 53C80 type controller
- On chip SCSI Bus drivers capable of sinking 48mA
- Onboard termination resistors
- Supports arbitration, selection/reselection, initiator or target roles
- EPROM socket for BIOS support
- SCSI BIOS extension for STD XT/AT systems
- Single +5 volt operation
- Available for CMOS STD Bus: LPM-SCSI

The LPM/MCM-SCSI is a CMOS Small Computer Systems Interface (SCSI) host adapter card. It permits multiple peripherals such as disk drives, WORM and optical drives, printers, tape streamers, computers, network gateways, integrated systems, etc. to be linked to the STD Bus in a very low cost manner.

The card supports the 80C88, V40, 80C286/386/486 single board computers and the STD Bus and CMOS STD Bus XT/AT systems requiring a SCSI interface with DMA, pseudo-DMA and programmed I/O modes.
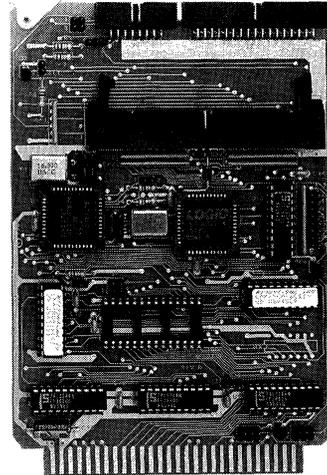
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-SCSI is the CMOS STD Bus version and the MCM-SCSI is the STD Bus version of this card. The LPM/MCM prefix indicates the card
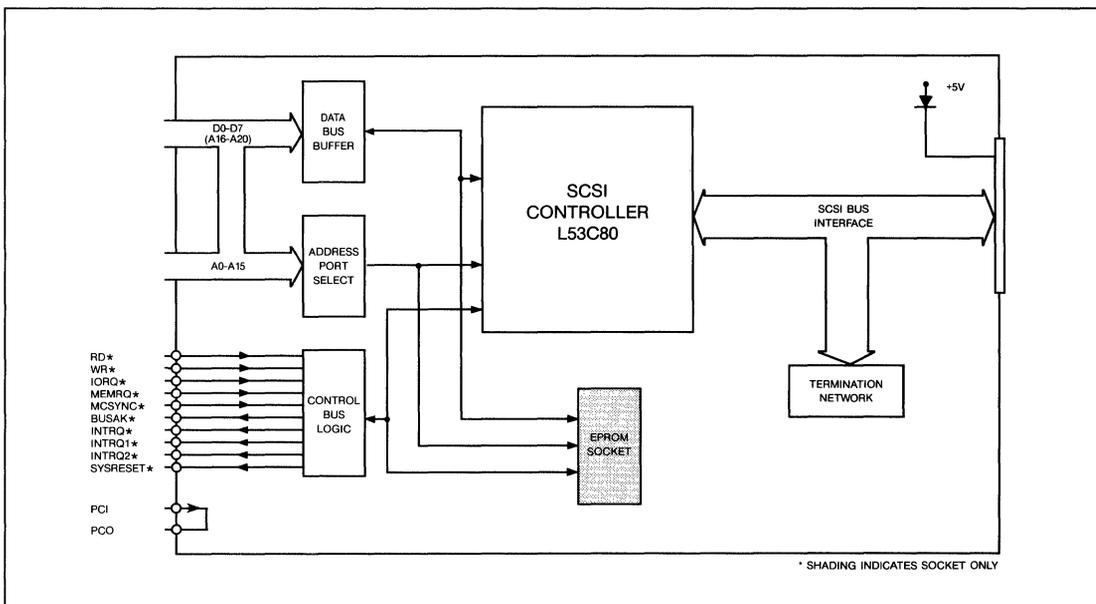
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has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

**Addressing** - Full data, address, and control line buffering is provided to and from the bus. The LPM/MCM-SCSI supports 10-bit addressing and is mapped at locations 2B0 through 2B8 hex.

Interrupts and DMA - Both interrupts and DMA are supported on the card. The interrupts are jumper selectable as INTRQ*, INTRQ1*, and INTRQ2* in any order on the STD Bus and CMOS STD Bus backplane or as IRQH on the front plane connector. DMA is controlled across the front plane connector only.

SCSI Interface - The LPM/MCM-SCSI is a complete interface to the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.0 committee. The LPM/MCM-SCSI offers the ability to interface different peripherals to the STD Bus and CMOS STD Bus through an industry standard architecture. Devices including printers, streaming tapes, disk drives, network gateways, and various other storage devices can be linked with this board. This allows several devices to communicate with either a single host or multiple hosts and devices. When several unlike devices need to be joined together, the LPM/MCM-SCSI allows signals from one device to be translated and utilized by the other. This interface determines an entire bus system, allowing clear electrical paths and well-defined communication protocols.

SCSI Controller - The LPM/MCM-SCSI is a very high performance, low cost, SCSI host adapter which supports the physical layer of the SCSI bus. It uses the Logical Devices' L53C80 CMOS controller which provides extensive bus status monitoring features and includes buffers capable of directly driving a terminated SCSI bus for an efficient STD Bus implementation. The LPM/MCM-SCSI has the capability to operate in either DMA, pseudo-DMA, or programmed I/O Mode. It can be either an initiator or target which provides 8-bit wide data transfer speeds up to 4 MBytes per second.

Software - A standard SCSI BIOS ROM is available for the LPM/MCM-SCSI to be used with WinSystems' STD Bus and CMOS STD Bus XT/AT systems.

An EPROM socket is available for installation of a 8KB or 32KB integrated BIOS extension. The socket decodes both 20- and 24-bit memory maps for use with either the CMOS STD Bus XT or AT type systems.

Connector - The LPM/MCM-SCSI supports the standard 50-pin cable wiring convention. Each signal line is single ended and is capable of sinking 48 mA and has a 220/330 ohm termination network. The board is shipped from the factory with the termination network installed. WinSystems offers various cables to interface the LPM/MCM-SCSI to external SCSI devices such as the HDXT-40 hard disk drive.

Hard Disk Drives - WinSystems offers various 3.5 inch, hard disk drives mounted on STD Bus and CMOS STD Bus cards. These units are a complete storage subsystem which plug directly into the STD Bus card cage. Cables are required to connect the drive to the LPM/MCM-SCSI host adapter card.

Floppy Disk Support - The LPM/MCM-DISK-XT is a version of the LPM/MCM-SCSI board with the floppy disk controller also on board. In addition to the SCSI support, it will support up to two, 3.5" or 5.25" standard or high density floppy disks.

SPECIFICATIONS

Electrical

Vdc = +5 volts ±10% @ 675mA typ.: LPM-SCSI

Vdc = +5 volts ±5% @ 700mA typ.: MCM-SCSI

Mechanical

Meets STD Bus mechanical dimensions

Connectors

Jumpers: 0.025" square posts
SCSI: 50-pin on 0.100 inch grid

Environmental

Operating Temperature:
    LPM-SCSI 0°C to +70°C
    MCM-SCSI 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SCSI	CMOS STD Bus SCSI host interface card
MCM-SCSI	STD Bus SCSI disk controller card
HDXT-40	40 MByte SCSI hard disk drive on an STD Bus card

WinSystems, Inc.

FEATURES

- STD Bus solid state disk for WinSystems' ROM-DOS and STD-AT/XT MS-DOS systems
- RAM/EPROM disk driver software available for use with the WinSystems' STD-AT and XT
- BIOS extension provided for STD-AT and XT
- Device driver provided for ROM-DOS and XT-80
- Supports up to 1 MByte of RAM, EPROM or battery backed SRAM per board
- Eight bytewide memory sockets that will accept 32K x 8, 64K x 8, or 128K x 8 SRAMs or EPROMs
- 20/24-bit addressing for use with the 80386SX, 80286, 8088, or V40 based systems
- High speed data access and storage
- Resistant to dirt, moisture, vibration, and temperature variations
- Optional onboard or offboard battery power
- CMOS STD Bus extended temperature range LPM-SSD = -40°C to +85°C
- Single +5 volt operation
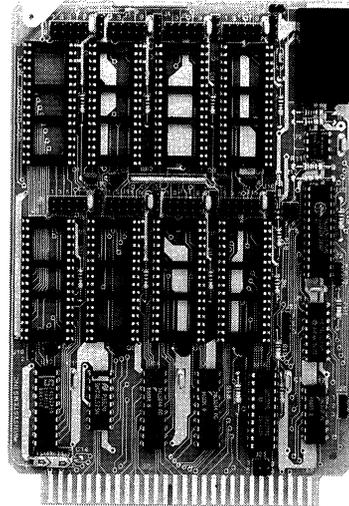
The LPM/MCM-SSD is a STD Bus RAM/ROM Solid State Disk. It is mandatory for applications where the environment is too harsh for mechanical hard disks or floppy disk drives, plus it has significant speed advantages. It is designed to store programs and data for applications such as data collection and logging, diagnostics, etc. Software drivers are available for STD Bus XT/AT applications for use in diskless DOS and embedded ROM-DOS systems.

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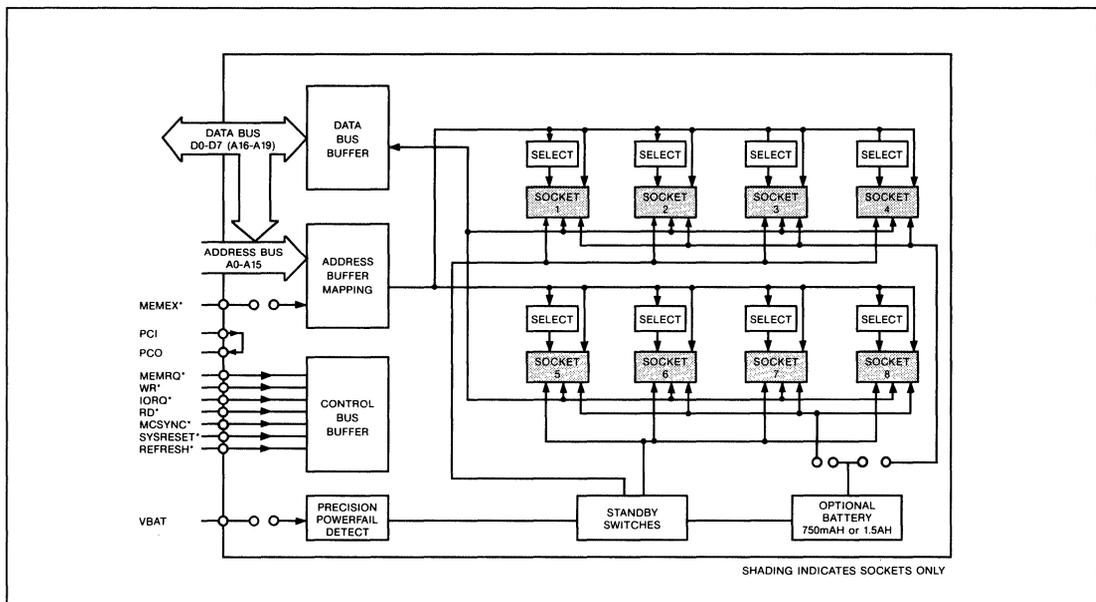
FUNCTIONAL CAPABILITY

Solid State Disk - The LPM/MCM-SSD is a very versatile solid state disk (SSD) subsystem that allows a user to substitute onboard semiconductor devices for disk drives normally required to boot and run a system or to serve as program storage. It replaces mechanical disks in embedded systems applications where power consumption, heat dissipation, shock, vibration, dirt, and cooling will cause a floppy or hard disk to fail. SSD drives have high reliability because there are no moving parts, they dissipate very little heat, and are completely digital.

The LPM/MCM-SSD offers nearly instantaneous data access since there is no track-to-track seeking. Data transfers occur at memory bus speed which is much quicker than with rotational magnetic media drives.

RAM/ROM Disk Storage Capacity - The LPM/MCM-SSD has eight, 32-pin bytewide memory sockets that will accept 32K x 8, 64K x 8, or 128K x 8 SRAMs or EPROMs for a total of 1MByte per board. This card is based upon a special configuration and population option of the WinSystems' LPM/MCM-UMC4-BAT. The standard SSD board configuration is shipped with no memory installed. Multiple boards are permitted for even larger memory storage.

System Compatibility - The LPM/MCM-SSD is designed to work with both STD Bus and CMOS STD Bus systems. A LPM/MCM prefix indicates the card has the same features and functionality and is available in both CMOS and regular NMOS/TTL logic. The basic differences between these two products are the power requirements, operational temperature range and Bus interface logic.

System Interface - The LPM/MCM-SSD is a memory mapped semiconductor disk board that supports both 20-bit (1MB) and 24-bit (16MB) addressing for use with WinSystems' XT and AT compatible CPUs. Various configuration options support the 8088/V40 CPUs in page mode through to the 80286/386SX CPUs in the protected, extended memory "AT" mode. Either a BIOS extension EPROM or installable device driver is provided to support the RAM/ROM disk operation.

AT Mode - The LPM/MCM-SSD operates in the extended memory above 1MB with WinSystems' 80286/386SX CPUs. Both RAM disk and ROM disk are supported in the protected mode. The RAM disk is expandable up to 12MBytes. The ROM Disk is a floppy disk image which will support any standard floppy disk format from 160KBytes to 1.44MBytes.

Page Mode - The LPM/MCM-SSD supports a banked-switched or "page mode" operation to allow expan-

sion of memory beyond the 640KB limit. This feature is very important for 8088/V40 based XT systems with the 1MB memory limitation. The board supports 16 pages with a page size of either 64KB or 128KB for a total capacity of 2 Megabytes.
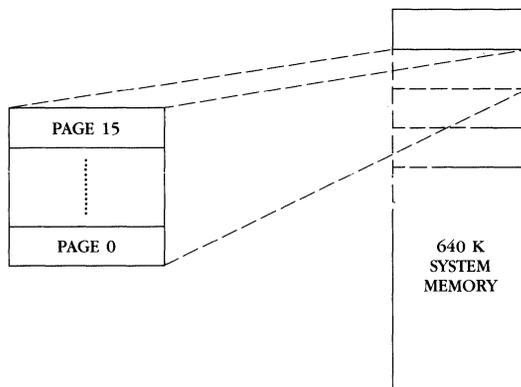
Page Mode Memory Usage

ROM DISK - A LPM/MCM-SSD populated with EPROMs and BIOS extension will create a bootable ROM DISK for either WinSystems' STD-AT or XT systems. The LPM/MCM-SSD emulates a Read Only floppy disk drive at the BIOS level. It allows users the ability to create a diskless PC capable of booting a ROM-resident copy of MS-DOS, application program and optional autoexec.bat file (for autostart).

The bootable ROM disk uses a disk imaging technique to assure complete compatibility with software utilizing BIOS level calls. The bootable ROM disk may be an image of any of the following floppy diskette formats:

A. 160KB,	5 1/4″,	Single Sided,	8 Sectors,	40 tracks
B. 180KB,	5 1/4″,	Single Sided,	9 Sectors,	40 tracks
C. 320KB,	5 1/4″,	Double Sided,	8 Sectors,	40 tracks
D. 360KB,	5 1/4″,	Double Sided,	9 Sectors,	40 tracks
E. 720KB,	5 1/4″,	Double Sided,	9 Sectors,	80 tracks
F. 1.2MB,	5 1/4″,	Double Sided,	15 Sectors,	80 tracks
G. 720KB,	3 1/2″,	Double Sided,	9 Sectors,	80 tracks
H. 1.4MB,	3 1/2″,	Double Sided,	18 Sectors,	80 tracks

Because the bootable ROM disk is an exact image of a floppy diskette, all testing and debugging can be accomplished using floppy drives. Once the application is debugged, it's a simple matter to use the MKDISK utility to create a series of EPROMs to install in the LPM/MCM-SSD. The output file format will support any number of PROM programmers and is menu selectable as a binary ROM image, Intel Hex ROM image, or Motorola S-record image file. Currently, the three supported EPROM types are:

1. 32K x 8 (27256 type)
2. 64K x 8 (27512 type)
3. 128K x 8 (27010 type)

The LPM/MCM-SSD-AT ROM disk operates in the protected area for STD-AT systems and does not require any memory in the 640K main system memory map. The LPM/MCM-SSD-XT, XT-compatible ROM Disk, is page mapped into either a 64K (E$\phi\phi\phi$:ϕ) or 128K (D$\phi\phi\phi$:ϕ) page (depending upon the size of EPROMs used) above the 640K main system memory map. For ROM-DOS systems, the ROM disk driver is supplied with the Operating System and permits the ROM Disk to reside either on the CPU or on the memory card.

Copyright Compliance - It is the users responsibility to assure that software placed in EPROMs with the LPM/MCM-SSD must comply with the original manufacturer's software licensing agreement.

RAM DISK - The RAM disk uses the LPM/MCM-SSD with the onboard 750 mA-hour battery jumper enabled to the memory sockets. It can be populated with up to eight 32KB or 128KB low power CMOS SRAMs for a total of 1 MB per board.

The storage capability of the RAM disk differs for AT and page mode operation. The AT mode RAM disk support is provided by the extended memory driver

WINDISK.SYS capable of up to 12 megabytes. This driver is similar to the standard VDISK.SYS supplied with MS-DOS 3.3 but with special differences. It is nonvolatile and will not be subject to destructive testing by the Phoenix BIOS self test routine. The current WINDISK.SYS driver does not support a bootable RAM disk in the AT mode.

The page mode RAM disk is available in bootable and non-bootable versions. The LPM/MCM-SSD-XT is the bootable version that is supplied with a BIOS extension EPROM installed in the first socket of the board. The RAM disk appears as a floppy disk image with a storage capability from 160KBytes to 1.44MBytes.

Universal RAM Disk - The LPM/MCM-SSD-RD non-bootable RAM disk is supplied with an installable device driver rather than a BIOS extension EPROM. This is the most universal version of the RAM disk and can work with WinSystems' ROM-DOS, XT and even AT compatible systems.

Removable Solid State Disk - WinSystems offers the LPM/MCM-RSSD which is a removable solid state disk. It supports credit card RAM data cartridges for storage up to 2MBytes. The IC memory card is small, light and durable, and can be installed and removed thousands of times without degradation. The drive is mounted on an STD Bus card but can be mounted externally to the card cage for application specific

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Solid State Disk Selection Guide

	WinSystems' CPU Support				Software Support		Capacity	
	80286AT	80386SX	V40XT	ROM-DOS SBC's	BIOS Extension	Device Driver	ROM	RAM
AT Mode ROM Disk LPM/MCM-SSD-AT	X	X	—	—	X	—	160KB to 1.44MB	—
AT Mode RAM Disk LPM/MCM-SSD-AT	X	X	—	—	—	X	—	Up To 12MB
Page Mode Bootable RAM Disk LPM/MCM-SSD-XT	X	X	X		X	—	160KB to 1.44MB	160KB to 1.44MB
Page Mode Non-Bootable RAM Disk LPM/MCM-SSD-RD	X	X	X	X	—	X	448KB	Up to 2MB

requirements. This product will work WinSystems STD-AT, XT and ROM-DOS systems. This product is described in detail in the LPM/MCM-RSSD data sheet.

CMOS STD Bus - The LPM-SSD is the CMOS STD Bus version which is needed for use in very low power and/or extended temperature (-40°C to +85°C) applications. The user should carefully select the memory devices that are mounted on the board to be sure that they will function across the entire temperature range. Contact WinSystems if you need help with selecting or locating the devices.

The MCM-SSD is designed with standard LS/TTL integrated circuits for use in regular STD Bus systems where the temperature range is not as extreme (0° to +65°C).

SPECIFICATIONS

Electrical
STD Bus compatible, 8-bit data transfers
Addressing: 20-bit page (1MB XT mode) or
          24-bit (16MB AT mode)
Power required with no memory installed
LPM-SSD = +5 VDC $\pm$10% @95mA
MCM-SSD = +5 VDC $\pm$5% @300mA

Memory Capacity: Eight, 32-pin bytewide sockets for 32KB, 64KB, or 128KB EPROMs or RAMs

Battery: 750 mA-Hour Lithium

Mechanical
Meets STD Bus mechanical specifications: 4.5″ x 6.5″

Environmental
Operating temperature:
        LPM-SSD   -40°C to +85°C
        MCM-SSD   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SSD-AT	CMOS STD Bus AT mode RAM/ROM DISK board with a 750 mAH battery installed and installable device driver
LPM-SSD-XT	CMOS STD Bus page mode bootable RAM/ROM disk with a 750 mAH battery installed for use with WinSystems' XT compatible. Includes BIOS extension EPROM
LPM-SSD-RD	CMOS STD Bus page mode non-bootable, universal RAM/ROM Disk board for use with ROM-DOS, XT and AT compatible systems with a 750 mAH battery and installable device driver on disk.
MCM-SSD-AT	STD Bus AT mode RAM/ROM DISK board with a 750 mAH battery installed and installable device driver.
MCM-SSD-XT	STD Bus page mode bootable RAM/ROM disk with a 750 mAH battery installed for use with WinSystems' XT compatible. Includes BIOS extension EPROM.
MCM-SSD-RD	STD Bus page mode non-bootable, universal RAM/ROM Disk board for use with ROM-DOS, XT and AT compatible systems with a 750 mAH battery and installable device driver on disk.

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Supports up to 4MBytes of RAM, PEROM (Flash) EPROM, or battery backed SRAM per board
- Eight bytewide memory sockets that will accept 128K x 8, 256K x 8, or 512K x 8 SRAMs, EPROMs or PEROMs (+5V only Flash memory)
- I/O mapped board requires no system memory
- Up to 4 boards can be mapped together to provide 16 MB of contiguous storage per solid state disk
- Multiple solid state disk are supported
- RAM/EPROM disk driver software available for WinSystems' DOS and ROM-DOS systems
- EPROM socket supports BIOS extension for bootable STD-AT and XT systems
- High speed data access and storage
- Resistant to dirt, moisture, vibration, and temperature variations
- Onboard battery power for SRAM support
- CMOS STD Bus extended temperature range LPM-USSD = -40°C to +85°C
- Single +5 volt operation
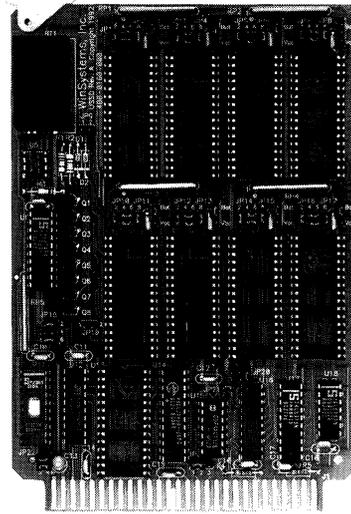
The LPM/MCM-USSD is an I/O mapped, universal STD Bus Solid State Disk (SSD). It can be populated by the user with up to 4 megabytes of RAM, EPROM, or PEROM (Flash). The card allows a user to substitute onboard semiconductor devices in applications where the environment is too harsh for mechanical hard disks or floppy disk drives, plus it has significant speed advantages. It is designed to store programs and data for applications such as data collection and logging, diagnostics, etc.

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*SHADING INDICATES SOCKETS ONLY
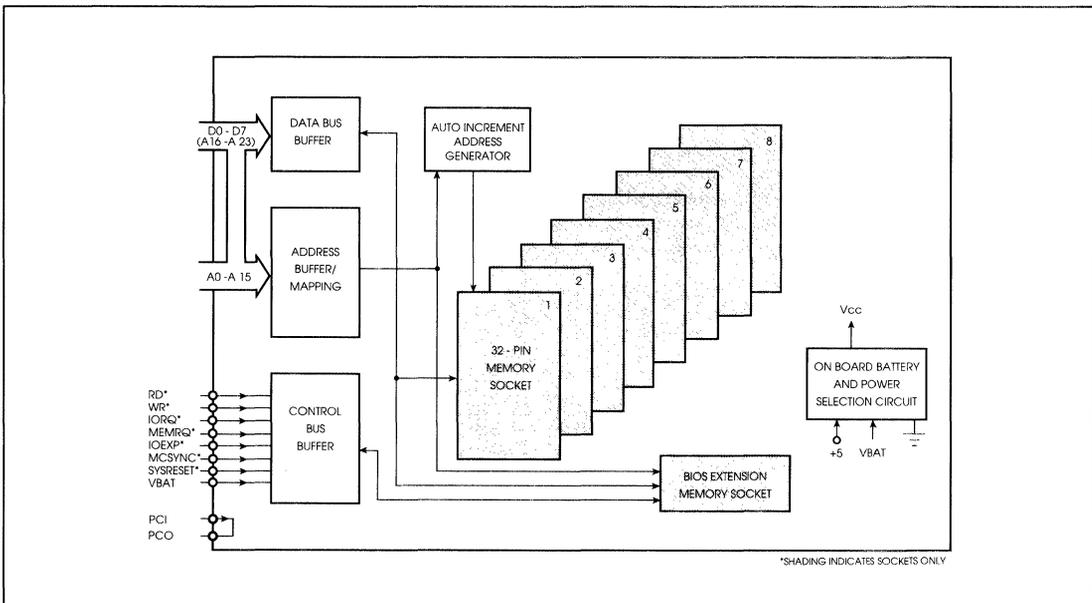
FUNCTIONAL CAPABILITY

STD Bus Interface - The MCM-USSD is the STD Bus version and the LPM-USSD is the CMOS STD Bus version of the card. Programming, bus pin assignments, and jumper configurations are identical for both. The LPM/MCM prefix indicates the card has the same features and functionality but a different bus interface logic, power requirements and operational temperature range.

The LPM/MCM-USSD is I/O mapped and does not require any memory in the 1 megabyte main system memory map for normal operation as a non-bootable solid state disk. Only 4 contiguous I/O ports are required.

Up to 4 boards can be mapped at the same port block to provide up to 16 MB of solid state storage. Additional 16 MB SSD drives can be mapped at different I/O port blocks if more storage is required.

The LPM/MCM-USSD offers nearly instantaneous data access since there is no track-to-track seeking. Data transfers are very quick since the board contains an auto-incrementing address pointer for use with 256 byte string move instructions from the CPU.

An additional socket is decoded for 20-bit (XT) or 24-bit (AT) addressing in the memory map for the installable BIOS extension required for bootable DOS systems.

RAM/ROM Disk Storage Capacity - The standard LPM/MCM-USSD is unpopulated and has eight, 32-pin bytewide memory sockets that will accept 128K x 8, 256K x 8, or 512K x 8 SRAMs, EPROMs, or PEROMs (+5 volt only Flash memory) for a total of up to 4 megabytes per board.

ROM DISK - A LPM/MCM-USSD, populated with EPROMs and BIOS extension, will create a bootable ROM DISK for either WinSystems' STD-AT or XT DOS or ROM-DOS systems.

RAM DISK - The RAM disk uses the LPM/MCM-USSD with the onboard 750 mA-hour battery jumper enabled to the memory sockets. It can be populated with up to eight 128KB, 256KB or 512KB low power CMOS SRAMs for a total of up to 4 MB per board.

An installable device driver is supplied with the RAM disk which can work with WinSystems' ROM-DOS, XT and STD-AT compatible systems.

SPECIFICATIONS

Electrical
STD Bus compatible
Addressing: 20-bit (1MB XT mode) or
24-bit (16MB AT mode) for BIOS socket
10-bit page for the eight 32-pin sockets

Power required with no memory installed
LPM-USSD = +5 VDC ±10% @ 95 mA
MCM-USSD = +5 VDC ±5% @ 300 mA

Memory Capacity: Eight, 32-pin bytewide sockets for 128KB, 256KB, 512KB EPROMs, SRAMs, or Flash PEROMs

Battery: 750 mA-Hour Lithium

Mechanical
Meets STD Bus mechanical specifications: 4.5″ x 6.5″

Environmental
Operating temperature:
    LPM-USSD   -40°C to +85°C
    MCM-USSD   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-USSD	CMOS STD Bus 4MB SSD
MCM-USSD	STD Bus 4MB SSD

WinSystems, Inc.

FEATURES

- 3.5" 720 KByte or 1.44 MByte floppy disk drive
- Double sided, standard or quad density
- Push button ejection mechanism
- Mounts directly inside a STD Bus card cage
- No extra mounting hardware required
- Supports STD-AT and XT compatible systems
- OEM version (without drive) available
- Very low power consumption
- +5 volt only operation

The FD3-720 and FD3-144 are floppy disk drives modules containing 3.5 inch, double sided, micro-floppy drives mounted directly on an STD Bus card. This configuration allows a floppy drive to be easily and conveniently mounted in a STD Bus card cage.

FUNCTIONAL CAPABILITY

Disk Drive - The FD3-720 and FD3-144 uses a 3.5" microfloppy whose features include a low profile, low power consumption, light weight, durability and high reliability. The mean time between failures (MTBF) for the drive is 30,000 POH. Standby power is 0.1 Watt max and 1.1 Watt typical during Read/Write mode.

The FD3-720 and FD3-144 are drive modules only. The WinSystems' MCM-DISK-AT or MCM-DISK-XT contain the controller and drive electronics necessary to interface the drive with a PC-XT/AT compatible STD Bus system.

Mounting Configuration - The disk drive is mounted directly on the STD Bus card and held in place by 4 screws. The STD Bus card cage provides mechanical positioning and rigidity plus power for the drive electronics. The drive will mount in any of the WinSystems' table top, rack mount or wall mount card cage configurations. The mounting also will not interfere with the optional hold down bar available for the card cages.

OEM Disk Mounting Kit - The disk drive STD Bus mounting board is available by itself for volume OEMs who wish to mount their own floppy disk drives. The kit includes the base board and power cable. The STD Bus disk drive mounting board is notched to facilitate cabling between multiple disk drives and the controller.

Warranty - The disk drives are not manufactured by WinSystems and are limited to the warranty (typically 90 days) provided by the original manufacturer.
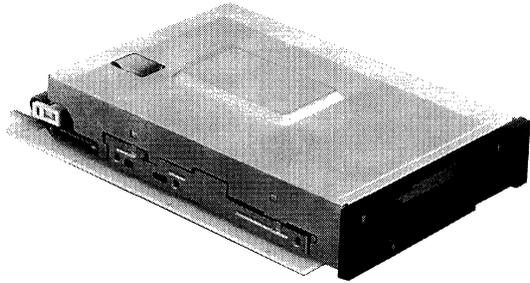
SPECIFICATIONS

Electrical
Drives: Double sided/double density
        720KBytes or 1.44MBytes formatted

Power = +5VDC @20mA (Stand-by)
              220mA typ. (Read/Write)
              890mA max. (Step during motor
                                      rotation)

Environmental
Operating Temperature: 10° to 45°C
Non-condensing relative humidity: 8 to 80%

ORDERING INFORMATION

FD3-720   3.5" Floppy Disk Drive Module,
           720K Byte
FD3-144   3.5" Floppy Disk Drive Module,
           1.44 MByte
FD3-0   OEM Mounting Kit

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WinSystems, Inc.

FEATURES

- 21 MByte storage on a 3.5" floppy drive that also reads and writes 720KB and 1.44 MB disks
- Removable high capacity media
- Push button ejection mechanism
- Mounts directly inside a STD Bus card cage
- No extra mounting hardware required
- Supports STD-AT and XT compatible systems
- OEM version (without drive) available
- Very low power consumption
- +5 volt only operation
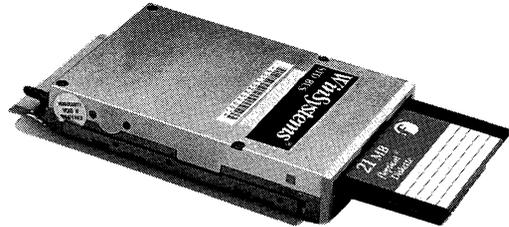
The FD3-21M is a high capacity floppy designed for escalating storage demands. It combines optical and magnetic recording technologies to achieve very high capacities (21MB) yet still reads and writes double density (720KB) and high-density (1.44MB) formats. It provides hard disk storage capacity with the removable, low cost convenience of a floppy.

A floptical disk drive is the same size as a 3.5" floppy disk drive and is mounted directly on an STD Bus card. This configuration allows the unit to be easily and conveniently mounted inside a STD Bus card cage.

FUNCTIONAL CAPABILITY

Floptical Disk Drive - The Floptical disk drive is a patented optical and magnetic recording technique from Insite Peripherals that has been able to achieve a 21 megabyte formatted capacity that is economical and doesn't obsolete older 720KB and 1.44 MB formats.

Like ordinary floppy drives, Floptical drives read and write magnetically on barium ferrite (BaFe) media encased in an industry standard 3.5" cartridge. The drive features dual gap heads which read and write standard double density and high density disks as well as 21 MB Floptical diskettes. This "downward compatibility" allows Floptical drives to access all your files stored on previous diskettes without obsoleting them.

Optical Servo - While the design of the Floptical drive is based on past formats, it is not limited by them. The difference lies in the concentric "servo" tracks embossed in the magnetic surface of a Floptical disk. Operating on a principle similar to CD-players, the drive optically senses track position by reflecting a light from an LED onto the servo pattern of the diskette. This optical tracking allows the Floptical drive to read and write data densely packed between the grooves with greater speed, accuracy and reliability than other methods. Because the optical tracking is so accurate, Floptical media has a track density of 1245 tracks per inch (tpi) which is still much lower than the 15,000 tpi densities of other optical technologies.

The optical servo is indelibly pressed into the media so it cannot be erased or damaged. It can be written over without risking errors and it does not require defect free media as is typically required with magnetic servos.

High reliability - The Floptical drive's reliability is further enhanced by a built-in error correction code (ECC) that corrects single error bursts of up to 80 bits and multiple error bursts totaling 70 bits. Also there is a built-in cyclic redundancy check (CRC) that ensures the ECC was correct.

Media - Two of the worlds largest media manufacturers, Hitachi Maxell, Ltd. and 3M's Data Storage Products Division, support this technology. These two companies assure quality production and world wide availability which adds to the acceptance as a industry standard. Second sources also keep the prices reasonable.

Floptical technology uses barium ferrite for the magnetic recording medium. This low-cost, very reliable medium is also being used on credit cards, and other flexible media disk drives. BaFe is a highly-durable, non-corrosive medium which can withstand harsher environments without loss of data or errors.

Floptical media is forecast to reach 40MB, 80MB and higher capacities in the near future for a higher density migration path.

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How Floptical Stacks Up Against Other Removable Media

Category	Floppy	Tape	Removable Winchester	Floptical
Formatted Capacity	1.44MB	80MB	43MB	21MB
Track Density (tpi)	135 tpi	112 tpi	1257 tpi	1245 tpi
Tracking Technique	Stepper	Stepper	Magnetic Servo	Optical Servo
Seek Time (milliseconds)	100ms	25 seconds	20ms	65ms
Bit Density (bpi)	17500	14700	24000	24000
Downward Compatibility with 720K & 1.44MB disks	Yes	No	No	Yes
Intelligent Interface	No/Floppy	No/Floppy	Yes/SCSI	Yes/SCSI

Product Comparison - Compared with high capacity floppies, tape, or removable Winchester drives, the Floptical has high capacity, performance, and low cost. It is also removable and compatible with earlier floppy diskettes.

Winchesters may be faster for now, but they lack compatibility with standard floppies. Compared to tape cartridges, Floptical media has the edge when it comes to speed. At 1.5 Mbps, it takes only 7 to 8 minutes to back up 40 MB hard disk onto two Floptical disks. A tape cartridge would take almost 24 to 30 minutes to backup the same hard drive — at least three times longer. Floptical drives retrieve data much faster by random access rather than the slow sequential access of tape systems.

Compared to slow, low capacity floppies which are relatively inexpensive, Floptical media makes economic sense. It takes over fourteen 1.44 MB floppies to store the same amount of data as one Floptical diskette.

Controller Interface - The FD3-21M is a drive module only. The WinSystems' MCM-SCSI or MCM-DISK-XT contain the SCSI host adapter and drive electronics necessary to interface the drive with an STD Bus XT/AT compatible system.

Mounting Configuration - The disk drive is mounted directly on the STD Bus card and held in place by 4 screws. The STD Bus card provides mechanical positioning and rigidity inside the card cage and power for the drive electronics. The drive will mount in any of the WinSystems' table top, rack mount or wall mount card cage configurations. The mounting also will not interfere with the optional hold down bar available for the card cages.

OEM Disk Mounting Kit - The disk drive STD Bus mounting board is available by itself for volume OEMs that wish to mount their own floppy disk drives. The kit includes the base board and power cable.

Warranty - The disk drives are not manufactured by WinSystems and are limited to the warranty (typically 90 days) provided by the original manufacturer.

SPECIFICATIONS

Formatted capacity: 21 MB fully read/write downward compatible with 720KB and 1.44MB disks
Average Seek time: 65 ms

ORDERING INFORMATION

FD3-21M   21MB Floptical Disk Drive Module

WinSystems, Inc.

FEATURES

- 40, 100 and 200 MByte storage capacity
- 3.5 inch disk drive mounts directly inside a STD Bus card cage
- High performance: 29 mS access time (avg.)
- Automatic head landing zone
- Internal error correction
- Microprocessor controlled diagnostics that are automatically executed at start-up
- Internal air filtration system
- Supports STD-AT and XT compatible systems
- No extra mounting hardware required
- MTBF greater than 20,000 hours (POH)
- HDAT withstands 10G's shock operating
- OEM version (without drive) available
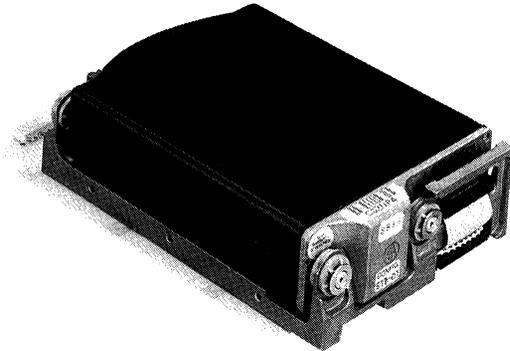
The HDAT-40/100/200 and HDXT-40/100/200 are hard disk drive modules containing a 3.5 inch drive mounted directly on an STD Bus card. Two versions are available: HDAT and HDXT. The HDAT is an IDE compatible and the HDXT is a SCSI compatible drive used with STD Bus compatible DOS systems. This configuration allows mass storage from a hard drive to be easily and conveniently mounted in a STD Bus card cage.

FUNCTIONAL CAPABILITY

STD Bus Interface - The HDAT and HDXT is a 3.5 inch 40, 100, or 200 megabyte formatted hard disk drive packaged on a STD Bus card that easily fits inside a card cage. The STD Bus is used only for the +12VDC, +5VDC and ground since the STD Bus disk controller is located on a separate board.

Disk Drive - The drive uses a brushless DC drive motor and a high performance rotary voice coil actuator with an embedded servo system to maintain precise alignment of each read/write head over the data throughout the operating temperature range. A dynamic break is used to provide a fast stop to the spindle motor when power is removed. Also at power down, the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is inside the data tracks.

A totally sealed head/disk assembly protect the head, media and data from non-operational shock of 50G's. Within the sealed enclosure, a 0.3 micron filter provides a clean environment to the heads and disk.

Data is 2, 7 Run Length Limited (RLL) coded to further assure maximum data density and high transfer rates. The drive performs internal error correction on the data. An onboard microprocessor controls diagnostic routines that are automatically executed at start-up. If an error is detected, the drive will not come ready.

The mean time between failures (MTBF) for the drive exceeds 20,000 POH.

HDAT - The HDAT interfaces to an IDE compatible host adapter card such as the WinSystems' MCM-DISK-AT. The interface to the STD Bus is 16-bits wide for use with high data rates and improved performance on STD-AT systems. The HDAT drive contains the electronics to permit it to operate with a STD-AT in either translate or native modes featuring a 1:1 interleave.

HDXT - The HDXT interfaces to a SCSI host adapter such as the WinSystems' MCM-DISK-XT or MCM-SCSI. The data path is 8-bits wide and can be used for either STD Bus XT or AT compatible systems.

Software Support - The HDAT and HDXT are designed to work with the appropriate disk controller boards. No BIOS extensions or modifications are required for the HDAT to work with WinSystems' STD-AT systems.

An EPROM socket is available for installation of an integrated BIOS extension on the MCM-DISK-XT and MCM-SCSI controller. The socket decodes both 20- and 24-bit memory maps for use with either the STD Bus XT or AT type systems. A standard SCSI BIOS extension is available for the MCM-DISK-XT to be used with WinSystems' STD Bus XT/AT systems 40 MByte hard disks (HDXT-40).

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Mounting Configuration - The disk drive is mounted directly on the STD Bus card and held in place by 4 screws. The STD Bus card cage provides mechanical positioning and rigidity plus power for the drive electronics. The drive will mount in any of the WinSystems' table top, rack mount or wall mount card cage configurations. The mounting also will not interfere with the optional hold down bar available for the card cages.

OEM Disk Mounting Kit - The disk drive STD Bus mounting board is available by itself for volume, cost conscious OEMs who wish to install their own hard disk drives and integrate it directly into the card cage. The kit includes the base board and power cable. The STD Bus disk drive PC board is notched to facilitate cabling to the controller.

Warranty - The disk drives are not manufactured by WinSystems and are limited to the warranty (typically 1 year) provided by the original manufacturer.

Cables - WinSystems offers a variety of cables to interface the drives with its respective controller. The CBL-126-1 is a 7 inch, 40-pin ribbon cable that connects the MCM-DISK-AT to the HDAT-40, HDAT-100, or HDAT-200. The cable is designed for a single hard drive in a STD Bus card cage. The CBL-129-1 is a 6 inch 50-pin ribbon cable the connects the

MCM-DISK-XT or MCM-SCSI controller to the HDXT-40, HDXT-100, or HDXT-200 disk drives. This cable also is designed for a single SCSI hard drive in a STD Bus card cage. For other cable configurations not listed, contact the factory.

SPECIFICATIONS

Electrical
Drives: 40, 100, or 200 megabyte (formatted)

Power:
HDAT = +5VDC 300mA typ.
    +12VDC @ 325mA typ. (steady state)
        @ 1.8A max. start surge during the initial 7 seconds

HDXT = +5VDC 600mA typ. (does not include SCSI termination resistors)
    +12VDC @ 325mA typ. (steady state)
        @ 2.0A max. start surge during the initial 7 seconds

Environmental
Operating temperature: 5°C to 45°C
Non-operating temperature: -40° to 60°C
Thermal gradient: 20°C per hour maximum
Non-condensing relative humidity: 8 to 80%

ORDERING INFORMATION

HDAT-40	40 MByte 3.5" IDE Hard Disk Drive
HDAT-100	100 MByte 3.5" IDE Hard Disk
HDAT-200	200 MByte 3.5" IDE Hard Disk
HDXT-40	40 MByte 3.5" SCSI Hard Disk Drive
HDXT-100	100 MByte 3.5" SCSI Hard Disk
HDXT-200	200 MByte 3.5" SCSI Hard Disk
HDAT-0	OEM Mounting Kit
CBL-126-1	HDAT to MCM-DISK-AT cable
CBL-129-1	HDXT to MCM-DISK-XT or MCM-SCSI cable

WinSystems, Inc.

Video/Graphics Controller

PRODUCT	BUS INTERFACE	GRAPHICS MODE	LIGHT PEN	FLAT PANEL SUPPORT
LPM-M/CGA	CMOS STD Bus	Hercules, MDA CGA	Yes	No
MCM-M/CGA	STD Bus			
LPM-EGA	CMOS STD Bus	Hercules, MDA CGA, EGA	Yes	No
MCM-EGA	STD Bus			
LPM-FPC	CMOS STD Bus	Hercules, MDA CGA	Yes	Yes
MCM-FPC	STD Bus			
LPM-FPVGA	CMOS STD Bus	Hercules, VGA	Yes	Yes
MCM-FPVGA	STD Bus			
LPM-VGA	CMOS STD Bus	Hercules, MDA CGA, EGA, VGA	Yes	No
MCM-VGA	STD Bus			

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FEATURES

- Low cost STD Bus flat panel controller
- Supports EL, Plasma and LCD
- Supports MDA, CGA, HGC
- Uses Yamaha PCDC V6366 controller chip
- Internally converts color information to gray scale on LCDs and hatching on EL and Plasma
- Auto-Initialization for selecting display and panel type
- Light pen supported
- Onboard EPROM socket for BIOS extensions
- 24V DC converter for LCDs included
- Supports STD Bus XT/AT compatibles
- CMOS STD Bus version: LPM-FPC
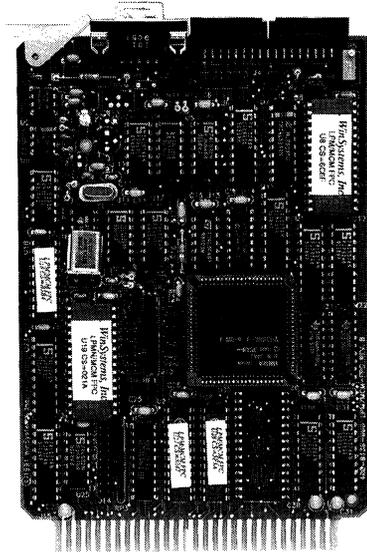
The LPM/MCM-FPC board is a universal display card that functions as a flat panel display controller. An onboard state machine performs auto-initialization, thereby eliminating the need for special driver software. Based upon the Yamaha V6366, the LPM/MCM-FPC will support all three flat panel display technologies (EL, Plasma, and Liquid Crystal) with full text and graphics. CGA, Hercules and MDA graphics modes are supported.

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*SHADING INDICATES SOCKETS ONLY
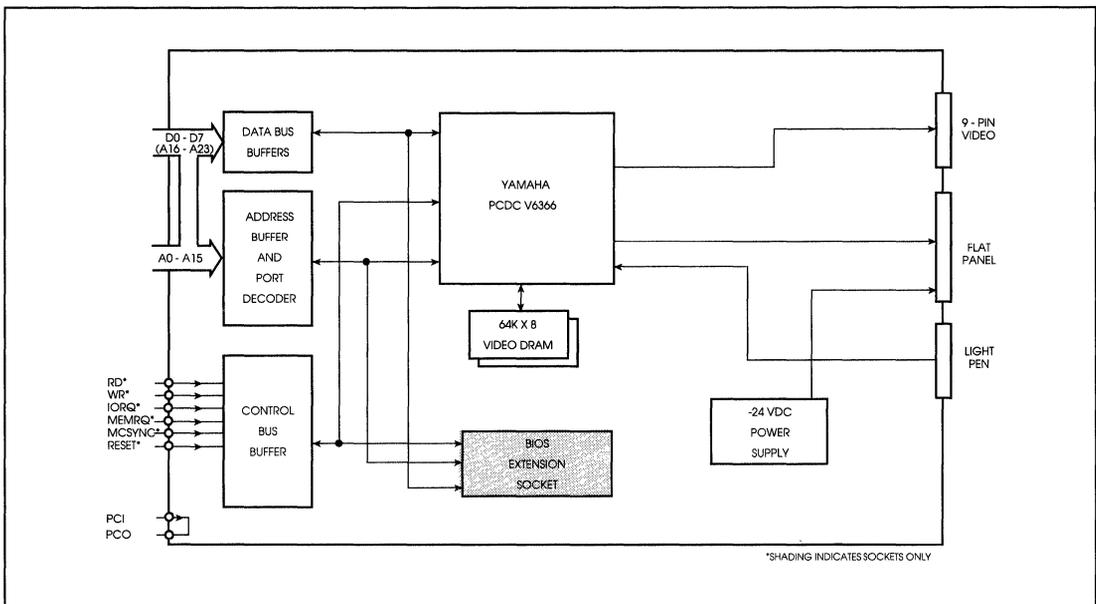
FUNCTIONAL CAPABILITY

Bus Interface - The MCM-FPC is the STD Bus and the LPM-FPC is the CMOS STD Bus version of the board. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operational temperature ranges.

Addressing - The LPM/MCM-FPC supports either 20- or 24-bit addressing for memory and 10-bit for I/O for use with XT or AT compatible STD Bus processors. Memory addressing and size of the EPROM socket is jumper selectable on the board.

The EPROM socket accepts from 8K to 64Kbyte EPROMs and can be used to store BIOS extensions, drivers or other special code.

Controller - The Yamaha PCDC V6366 will drive the flat panel technologies including LCD, Plasma, and EL. It internally converts color information to gray scale on LCD's, and hatching on EL and Plasma displays.

Operational Modes

Mode	Format	Screen Resolution
MDA	80 x 25	720 x 350
CGA	40 x 25	320 x 200
	80 x 25	640 x 200
HGC	80 x 25	720 x 348

Manufacturers currently supported are:

AND Corp.	Fuji	Optrex
Cherry	Fujitsu	Panasonic
Citizen	Hitachi	Planar
Densitron	Kyocera	Seiko
Epson	NEC	Sharp
Finlux		Toshiba

Call WinSystems for the display you have selected for specific part numbers of new and existing panels supported.

LCD Interface - A negative 24V DC power supply for LCD displays is included on the board. Software programmable internal logic sequentially applies power which prolongs the life of display. Preselection of display types is performed by setting a seven position switch during board installation.

Light Pen - The light pen circuitry consists of the light pen switch and light pen input plus power and ground for the pen. Input is via a 6-pin polarized connector at the top of the board.

SPECIFICATIONS

Electrical
Interface Bus: STD Bus
I/O Addressing: 10-bit
Memory Addressing: 20- or 24-bit decoding
Data Transfer: 8-bits wide

Power Requirements
LPM-FPC: + 5V $\pm$ 5% at 200 mA (typ.)
          + 12Vdc (Light pen only)
          - 12Vdc T.B.D.
MCM-FPC: + 5V $\pm$ 5% at 450 mA (typ.)
          + 12Vdc (Light pen only)
          - 12Vdc T.B.D.

Mechanical
Dimensions: 4.5" x 6.5"

Connectors
Flat Panel: 34-pin header, 0.100 centers
Light Pen: 6-pin keyed header, 0.100" centers
Jumpers: 0.025" square posts

Environmental
Operating Temperature:
    LPM-FPC: 0°C to 70°C
    MCM-FPC: 0°C to 65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-FPC   CMOS STD Flat panel controller
MCM-FPC   STD Bus Flat panel controller card

WinSystems, Inc.

FEATURES

- Supports plasma, EL, LCD and color LCD panels
- 64 shades of gray on monochrome LCD panels
- Simultaneous display on LCD and CRT
- VGA resolution for LCD and CRT
- Onboard DC/DC converter for contrast voltage
- High resolution digital and analog graphics modes
- 256KB x 4 video RAM on board
- Memory socket for BIOS extension
- Keyboard controller onboard
- 8 or 16-bit STD Bus interface
- CMOS STD Bus version: LPM-FPVGA

The LPM/MCM-FPVGA is a versatile LCD VGA controller that provides support for basic VGA modes for an LCD or CRT, and extended 800 x 600 resolution graphics on the CRT. It provides excellent display quality, with up to 64 shades of gray on monochrome Super-Twist Nematic (STN) LCD panels and a direct connection capability for active matrix color LCD panels.

The board can display on the flat panel and on a VGA CRT simultaneously. Direct power sequencing for panels that require sequencing is supported.

The LPM/MCM-FPVGA includes an onboard keyboard controller for use with embedded systems. This board replaces WinSystems' LPM/MCM-VGA board and is recommended for new designs.

FUNCTIONAL CAPABILITY

Bus Interface - The MCM-FPVGA is the STD Bus and the LPM-FPVGA is the CMOS STD Bus version of the board. Programming, cable pin-outs, bus pin assignments, and jumper configurations are identical for both cards. The LPM/MCM prefix indicates the card has the same features and functionality but a different bus interface logic, power requirements and operational temperature range.

Addressing - The LPM/MCM-FPVGA supports either 20 or 24-bit memory addressing for use with XT or AT compatible STD Bus systems. For I/O requirements, 10-bits are decoded.

Memory - A 32KB BIOS EPROM and 256KB x 4 of video DRAM are installed on the card. A video BIOS extension is provided in the EPROM to provide PC video compatibility for the various modes of operation.
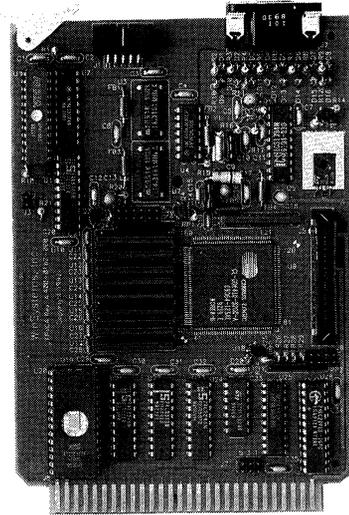
Video Controller - This board is based upon the Cirrus Logic GD6410 LCD VGA controller. The chipset allows the full spectrum of PC applications written for analog monitors and various video modes to run on standard 640 x 480 flat panels. This is accomplished through color emulation, attribute remapping, and resolution mapping.

In color text modes, foreground and background attributes can be automatically remapped to black and white for maximum contrast. Positive or negative raster may be selected under program control to match the visual qualities of the display and/or needs of the application.

CRT Display Modes - CRT displays supported are PS/2 VGA-compatible analog monitors, including the IBM 85xx families, and multi-frequency analog monitors. The board includes all registers and data paths required for VGA compatibility. VGA enhancements include 16 simultaneously-loadable text fonts (twice the capability of IBM VGA), and readable registers.

Extended graphics resolutions beyond the 640 x 480 IBM VGA standard are available. Using multi-frequency monitors, 800 x 600 Mode with 4:3 aspect ratio can be displayed.

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Modes Supported During LCD Display

Mode No.	Mono. STN Number of Shades	Color TFT Number of Colors	CRT Number of Colors	Char. x Row	Char. Cell	Number of Pixels	Display Mode
			IBM Standard VGA Modes				
0,1	16/16	16/512	16/256K	40 x 25	9 x 16	360 x 400	Text
2,3	16/16	16/512	16/256K	80 x 25	9 x 16	720 x 400	Text
4,5	4/64	4/512	4/256K	40 x 25	8 x 8	320 x 200	Graphics
6	2/16	2/512	2/256K	80 x 25	8 x 8	640 x 200	Graphics
7	2/16	2/512	Mono.	80 x 25	9 x 16	720 x 400	Text
d	16/64	16/512	16/256K	40 x 25	8 x 8	320 x 200	Graphics
e	16/16	16/512	16/256K	80 x 25	8 x 14	640 x 200	Graphics
f	2/16	2/512	Mono.	80 x 25	8 x 14	640 x 350	Graphics
10	16/16	16/512	16/256K	80 x 25	8 x 14	640 x 350	Graphics
11	2/16	2/512	2/256K	80 x 25	8 x 16	640 x 480	Graphics
12	16/16	16/512	16/256K	80 x 25	8 x 16	640 x 480	Graphics
13	64/64	256/24K	256/256K	40 x 25	8 x 8	320 x 200	Graphics
			Extended Video Modes				
64,6a	16/16	NA	NA	100 x 37	8 x 16	800 x 600	All

For CRT based applications, the interface provides register level compatibility with VGA, and BIOS-level compatibility with MDA, CGA, and EGA monitors. IBM-compatible, fixed frequency monochrome and multi-frequency analog monitors are supported.

Modes Supported During CRT Display

Mode No.	Number of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode
		IBM Standard VGA Modes			
0,1	16/256K	40 x 25	9 x 16	360 x 400	Text
2,3	16/256K	80 x 25	9 x 16	720 x 400	Text
4,5	4/256K	40 x 25	8 x 8	320 x 200	Graphics
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics
7	Mono.	80 x 25	9 x 16	720 x 400	Text
d	16/256K	40 x 25	8 x 8	320 x 200	Graphics
e	16/256K	80 x 25	8 x 16	640 x 200	Graphics
f	Mono.	80 x 25	8 x 14	640 x 350	Graphics
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics
12	16/256K	80 x 30	8 x 16	640 x 480	Graphics
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics
		Extended Video Modes			
		Modes supported during CRT only display			
51	16/256K	132 x 50	8 x 8	1056 x 400	Text
52	16/256K	132 x 60	8 x 8	1056 x 480	Text
53	16/256K	80 x 60	8 x 8	640 x 480	Text
64,6a	16/256K	100 x 37	8 x 16	800 x 600	Graphics

Flat Panel Display Modes -The board will directly drive all of the popular monochrome dual-panel/dual-scan LCD panels from manufacturers such as Sharp, Hitachi, Sanyo, Epson, Kyocera, Toshiba, Citizen, Seiko,

and Fujitsu. Techniques are used in the chipset to minimize flicker, noise and pattern motion while enhancing contrast within the gray scales being used.

Flat panel display devices supported will typically be 640 x 480 resolution monochrome Super-Twist Nematic (STN). With this type of panel it will achieve 64 shades of gray in VGA mode 13.

Five hundred twelve color Thin Film Transistor (TFT) LCD panels can be connected directly to the LPM/MCM-FPVGA board to provide 256 simultaneous colors from a palette of thousands of possible colors in VGA mode 13.

CRT Video Interface - The video interface is provided through a 15-pin "D" type front plane connector for VGA compatible monitors.

The flat panel interface is a on a separate connector. The board can display on the flat panel and on a VGA CRT simultaneously.

ORDERING INFORMATION

LPM-FPVGA CMOS STD Bus VGA CRT/Flat panel controller

MCM-FPVGA STD Bus VGA CRT/Flat panel controller

WinSystems, Inc.

FEATURES

- Low cost STD Bus and CMOS STD Bus video adapter board
- CGA, MDA, and Hercules compatible
- Hi-Definition CGA mode (640 x 400)
- 6845 CRTC compatible controller
- Permits 2 video boards in a system
- Supports 20 or 24-bit addressing
- Light pen input
- 9-pin TTL or composite video output
- Onboard EPROM socket for BIOS extensions
- Onboard 64K byte video RAM
- Supports STD Bus and CMOS STD Bus XT/AT compatibles
- Available for CMOS STD Bus: LPM-M/CGA

The LPM/MCM-M/CGA board from WinSystems is a color graphics and monochrome adapter providing CGA, MDA, and HGC compatibility. In addition, a high resolution CGA mode provides 640 x 400 display featuring high quality text and line double graphics. The board uses the NCR 72C81 which integrates a 6845 CRT controller and associated circuitry to provide a low cost STD Bus and CMOS STD Bus video adapter card. This card will work with STD Bus and CMOS STD Bus XT/AT compatibles or non-DOS systems as well.
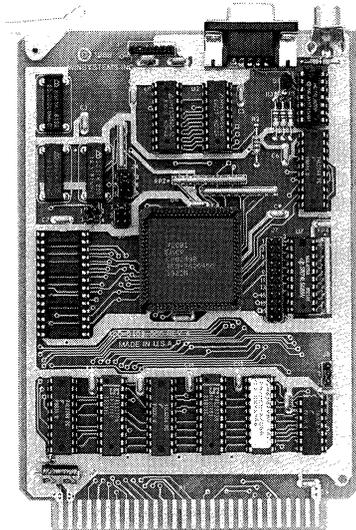
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-M/CGA is the CMOS STD Bus version and the MCM-M/CGA is the STD Bus version of this card.

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SHADING INDICATES SOCKET ONLY
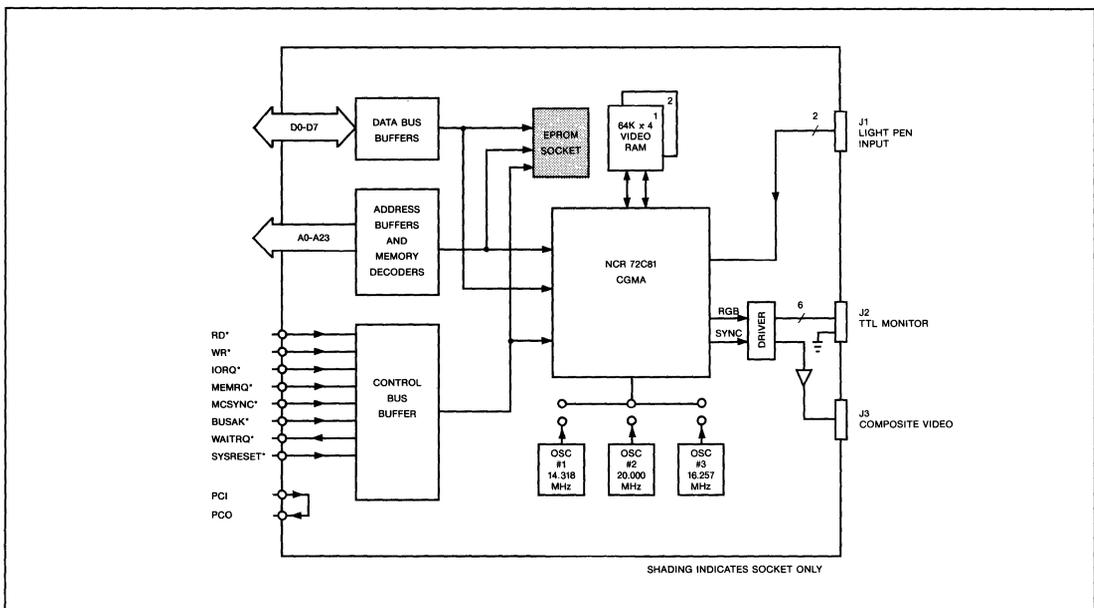
Addressing - The LPM/MCM-M/CGA supports either 20 or 24-bit addressing for memory and 10-bit for I/O for use with XT or AT compatible STD Bus and CMOS STD Bus processors. Address selection and memory address for the video RAM are software programmable inside the 72C81. Memory addressing and size for the EPROM socket is jumper selectable on the board.

The EPROM socket accepts from 8K to 64KByte EPROMs and can be used to store BIOS extensions, drivers or other special code. 64KBytes of dual port dynamic RAM provide multiple pages of video RAM. The interface to the STD Bus is synchronized through the WAIT line.

Video Controller - This board is based upon the NCR 72C81 CGMA VLSI CRT controller that supports standard IBM display modes plus a 100% CGA compatible High Definition (Hi-Def) Mode. The Hi-Def mode is a cut above the standard CGA while maintaining compatibility with the existing CGA software base. CGA compatibility is maintained because special mapper circuitry intercepts I/O access to the internal 6845 and inserts parameters that are correct for high resolution operation.

Operational Modes

Mode	Format	Screen Resolution
Color		
CGA	40 x 25	320 x 200
CGA	80 x 25	640 x 200
Hi-Def	40 x 25	320 x 400*
Hi-Def	80 x 25	640 x 400*
MDA	80 x 25	720 x 350
Alphanumeric		
CGA	40 x 25	320 x 200
CGA	80 x 25	640 x 200
Hi-Def	40 x 25	320 x 400*
Hi-Def	80 x 25	640 x 400*
MDA	80 x 25	720 x 348

* Scan Doubled Display

In color alphanumeric (A/N) modes, two bytes are used to define character images. In color graphics modes, the display memory is organized in a packed pixel format with each byte representing four or eight pixels, depending upon the mode selected.

Monochrome A/N modes operate in a similar manner to color modes. Additionally, the color encoder outputs video data on the Green output and intensity control provide the blink, underline, reverse video and intensify attributes. In the monochrome graphics

mode, data from the display memory is serialized and displayed in a 720 x 348 format.

The LPM/MCM-M/CGA board will support dual video operation. The first video board such as an LPM/MCM-M/CGA, LPM/MCM-EGA or LPM/MCM-VGA can operate in any color mode (i.e. CGA, EGA, VGA). The second video board must be the LPM/MCM-M/CGA operating in the monochrome mode only.

Monitor Interface - The LPM/MCM-M/CGA card generates two types of output. The first is a standard CGA or monochrome TTL compatible monitor interface through a 9-pin female D connector. The second is a composite video (monochrome only) through a RCA phono plug.

The TTL outputs are comprised of Red, Green, Blue, Intensity and the Horizontal and Vertical Sync pulses. These outputs are TTL/CMOS compatible with high drive capability. The Green, vertical sync and horizontal sync are mixed to generate the composite video output on J3.

Light Pen - The light pen circuitry consists of the light pen switch, light pen input and power pen.

SPECIFICATIONS

Electrical
Memory Addressing: 20 or 24-bit decoding
Data Transfer: 8-bits wide

Power Requirements
Vcc = +5V ± 5% at 250 mA (typ)
        +12V (Light pen only)

Mechanical
Dimensions: 4.5" x 6.5"

Connectors
TTL Monitor: DB-9 (female)
Composite Video: Phono jack
Light Pen: 6-pin keyed header, 0.100" centers
Jumpers: 0.025" square posts

Environmental
Operating Temperature:
        LPM-M/CGA   0° to 65°C
        MCM-M/CGA   0° to 55°C
Non-condensing relative humidity: 5% to 95%

ORDER INFORMATION

LPM-M/CGA	CMOS STD Bus M/CGA adapter
MCM-M/CGA	STD Bus M/CGA adapter

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Compatible with VGA, EGA, CGA, MDA, and Hercules
- Light pen interface
- Compatible with WinSystems' STD-AT
- Automatic Video switch mode
- Supports digital and analog graphics modes
    - 640 x 480 high-resolution graphics
    - 320 x 200 resolution, 256 colors from a palette of 262,144
    - 800 x 600 high-resolution graphics
    - 720 x 540 high-resolution graphics
    - 640 x 350, 16 color graphics
    - 640 x 200, 16 color graphics
    - 320 x 200, 16 color graphics
- 256KB video RAM on board
- Memory socket with VGA BIOS extension
- Available for CMOS STD Bus: LPM-VGA and LPM-EGA

The LPM/MCM-VGA and LPM/MCM-EGA are high-resolution display adapter cards that provide PC-compatible graphics capability on a single card. Both cards support EGA/CGA/MDA and Hercules modes. Additionally, the LPM/MCM-VGA supports analog VGA monitors.
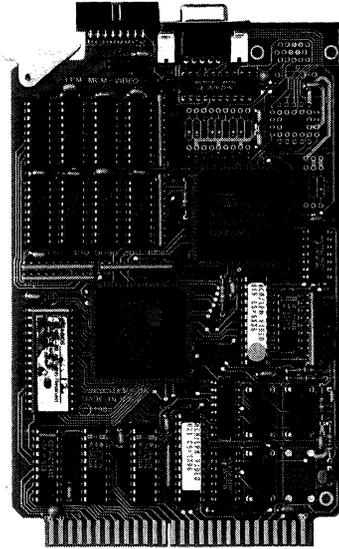
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-VGA and LPM-EGA are the CMOS STD Bus versions and the MCM-VGA and MCM-EGA are the STD Bus versions of these cards.

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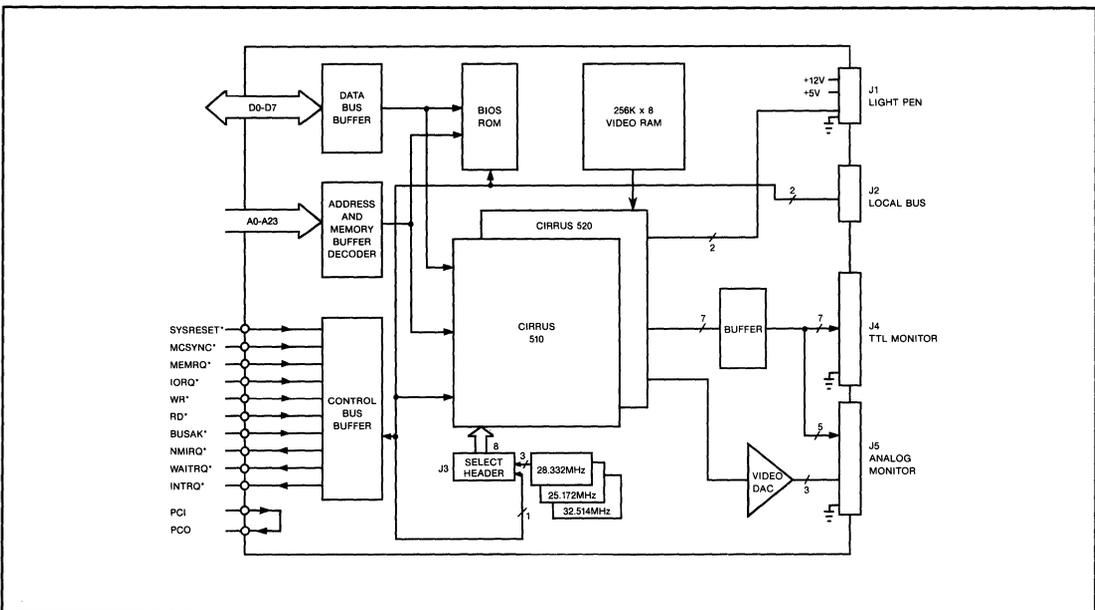
Addressing - The LPM/MCM-VGA and LPM/MCM-EGA boards support either 20- or 24-bit memory addressing for use with XT or AT compatible STD Bus and CMOS STD Bus systems. Either an "-A" or "-X" suffix is appended to the board name to designate 24- or 20-bit memory decoding respectively.

Memory - A 32KB BIOS EPROM and 256KB of DRAM are installed on the card. A video BIOS extension is provided in the EPROM to provide PC-video compatibility for the various modes of operation. The board contains 256KBytes of high speed dual port dynamic RAM for use as video memory.

Video controller - This board is based upon the Cirrus Logic 510/520 Enhanced VGA compatible graphics chip set. It is compatible with VGA, EGA, CGA, MDA standards and Hercules HGC.

Operating at dot clock rates up to 32 MHz, the 510/520 chip set supports high-resolution graphics and alphanumeric display modes for both mono-chrome and color, and for high resolution variable frequency monitors. Video outputs are provided in 4 bits per pixel (all resolutions) and 8 bits per pixel (320 x 200). Using analog video output and an external palette, selection may be made from 256K colors.

The hardware supports a mouse/graphics cursor, and a blinking insertion point text cursor. Additional text cursor controls include blink disable and replace/invert mode control. The hardware supports simultaneous and independent smooth scrolling of two separate text screens.

TTL Video Interface - The TTL outputs are comprised of Red, Green, Blue, Intensity and the Horizontal and Vertical Sync pulses. These outputs are TTL/CMOS compatible with high drive capability for PC-compatible fixed and multi-frequency mono-chrome, color, and EGA monitors. The TTL video signals are available through a 9-pin "D" type front plane connector.

Analog Video Interface - The LPM/MCM-VGA differs from the LPM/MCM-EGA since it includes the high speed video DAC to support analog monitors. The video interface is provided through a 15-pin "D" type front plane connector for VGA compatible monitors.

Co-Resident Display Adapters - The LPM/MCM-EGA and LPM/MCM-VGA boards may co-reside with another video board such as the WinSystems' LPM/MCM-M/CGA. The second video board must operate in the monochrome mode only.

Light Pen - The light pen circuitry consists of the light pen switch and light pen input plus power and ground for the pen. Input is via a 6-pin polarized connector at the top of the board.

SPECIFICATIONS

Electrical
Interface Bus: STD Bus
System clock: Up to 8 MHz
I/O Addressing: 10-bit
Memory Addressing: 20- or 24-bit decoding
Data Transfer: 8-bits wide

Power Requirements
Vcc = +5V + 5% @ 550mA typ.,
        +12V (Light pen only): LPM-VGA and LPM-EGA
Vcc = +5V + 5% @ 250mA typ.,
        +12V (Light pen only): MCM-VGA and
        MCM-EGA

Mechanical
Meets STD Bus mechanical specifications

Connectors
TTL Monitor: DB-9 (female)
Analog Monitor: 15-pin "D" shell Analog VGA video
Light Pen: 6-pin keyed header, 0.100" centers

Environmental
Operating Temperature: 0° to 65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-VGA-A CMOS STD Bus VGA, EGA, CGA, MDA
                video card for STD-AT operation
LPM-VGA-X XT version of LPM-VGA
LPM-EGA-A CMOS STD Bus EGA, CGA, MDA video
                card for STD-AT operation
LPM-EGA-X XT version of LPM-EGA
MCM-VGA-A STD Bus VGA, EGA, CGA, MDA video
                card for STD-AT operation
MCM-VGA-X XT version of MCM-VGA
MCM-EGA-A STD Bus EGA, CGA, MDA video card for
                STD-AT operation
MCM-EGA-X XT version of MCM-EGA

WinSystems, Inc.

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Networking/Communications Controllers

PRODUCT	BUS INTERFACE	NETWORK	MEDIA	SPEED
LPM-ANET	CMOS STD Bus	ARCNET Bus or Star	Coax or Fiber Optic	2.5 MBps
MCM-ANET	STD Bus			
LPM-ENET	CMOS STD Bus	Ethernet Bus	Coax	10 MBps or 1 MBps (Thin)
MCM-ENET	STD Bus			
LPM-MODEM	CMOS STD Bus	Dial Up Telephone	Telephone	1200, 300 Bps
MCM-MODEM	STD Bus			
MCM-2400	Either STD or CMOS STD Bus	Dial Up Telephone	Telephone	2400, 1200, 300 Bps
MCM-2400 MNP	Either STD or CMOS STD Bus	Dial Up Telephone	Telephone	2400, 1200, 300 Bps
LPM-488	CMOS STD Bus	IEEE-488	Cable	— —
MCM-488	STD Bus			

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FEATURES

- Complete STD Bus and CMOS STD Bus ARCNET controller board
- 2.5 Mbps data transfer rate
- Uses 90C65 single chip ARCNET controller supporting bus or star topologies
- Supports coax or optional fiber optic cable
- Onboard 8K x 8 auto-boot EPROM socket for diskless workstations
- Onboard 2K x 8 Data Packet Buffer for double-buffered transmit and receive functions
- Allows up to 255 nodes to communicate over a distance of 4 miles
- Software compatible with NetWare from Novell and QNX from Quantum Software
- Can be used with the WinSystems' STD-AT and XT compatible systems
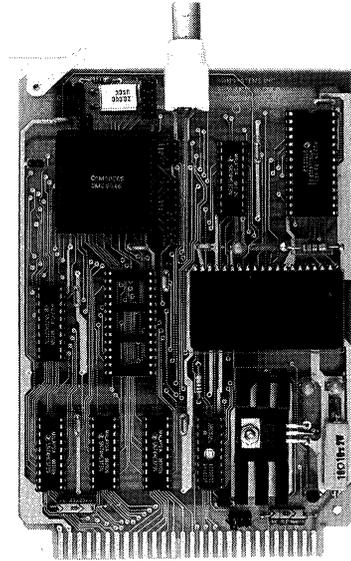
The LPM/MCM-ANET board from WinSystems is a complete ARCNET interface board designed for the STD Bus and CMOS STD Bus. It will operate with coaxial systems in either a star or bus topology or with fiber optic cables. It can support 255 nodes at 2.5 Mbps for distances up to four miles.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-ANET is the CMOS STD Bus version and the MCM-ANET is the STD Bus version of this card. The LPM/MCM prefix indicates

the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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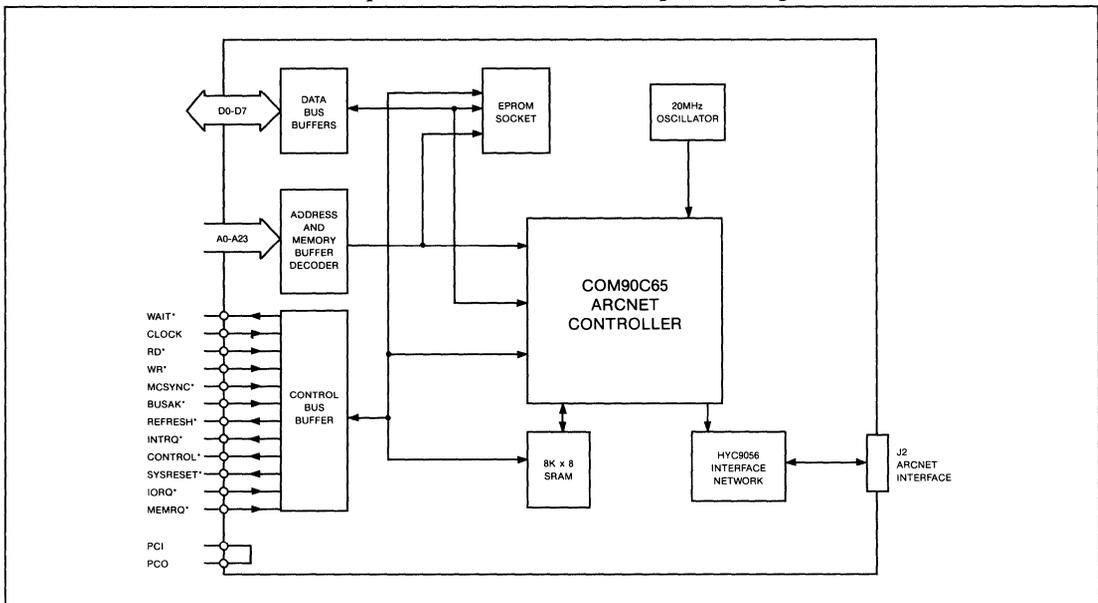
Controller - The LPM/MCM-ANET uses the SMC 90C65 controller which provides all of the control for implementing the complete ARCNET protocol at a 2.5 Mbps data rate. A maximum of 255 nodes can be connected to a network with each node assigned a unique ID.

ARCNET - ARCNET is a baseband, token-passing Local Area Network (LAN) and is one of the easiest LANs to install and use. It is very popular with over 1,000,000 nodes installed worldwide. ARCNET is low cost, reliable, easy to install, and is supported by popular PC-based network operating systems.

Network Topology - The LPM/MCM-ANET is configured as either bus or star network topology. A star topology network is formed by linking nodes, each containing an ARCNET network controller board, to a central component known as a hub. Up to eight LPM/MCM-ANET boards can be connected point-to-point to an Active Hub to form a star network. To expand the network, these hubs are linked to form a "distributed star". This wiring scheme is well suited for widely separated systems and support both coaxial and fiber optic cables. Additional systems can be added to the network by linking active hubs together. Hubs may be placed up to 2,000 feet (609.6m) apart.

With a bus topology network, nodes are connected directly to a coaxial cable with BNC "Tee" connectors. Bus networks offer an "attach and grow" capability. To expand the network, just add another cable segment at any point on the bus. Up to 8 LPM/MCM-ANET or other ARCNET cards can be connected to coaxial cables with BNC "T" connectors to form a bus network. The bus can have a length of 1000 (304.8m) and must be terminated at each end. The network can be expanded by linking two bus cables with a special 2 port hub called an Active Link. Bus and Star networks can be combined by simply connecting one end of a bus cable to any open port of an Active Hub. This enables newer Bus products to work on existing star networks.

Fiber Optics - One optional configuration of the LPM/MCM-ANET uses the Raycom 310 duplex fiber optic transceiver. It offers increased security, is safer in hazardous environments, provides immunity with RFI/EMI, and increases the distance between nodes.

Software - The LPM/MCM-ANET is fully compatible with the SMC hardware interface and will run network software packages such as Novell's NetWare and Western Digital's ViaNet without driver modification. An EPROM socket is provided to support 8K to 64KByte devices for software drivers.

SPECIFICATIONS

Electrical
I/O Addressing: 10-bit
Memory Addressing: 20- or 24-bit decoding
Data Transfer: 8-bits wide

Power Requirements
Vcc = +5V ±5% 600 at mA
     -12V at 100 mA

Mechanical
Dimensions: 4.5" x 6.5" (Connectors extend beyond end of the card)

Connectors
Coaxial: BNC connector for RG62 A/U cable

Environmental
Operating Temperature:
    LPM-ANET   0° to 70°C
    MCM-ANET   0° to 65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-ANET-XB	XT compatible ARCNET card for coaxial bus or star topology
LPM-ANET-XF	XT compatible ARCNET card for fiber optic star topology
LPM-ANET-AB	STD-AT compatible ARCNET card for coaxial bus or star topology
LPM-ANET-AF	STD-AT compatible ARCNET card for fiber optic star topology
MCM-ANET-XB	XT compatible ARCNET card for coaxial bus or star topology
MCM-ANET-XF	XT compatible ARCNET card for fiber optic star topology
MCM-ANET-AB	STD-AT compatible ARCNET card for coaxial bus or star topology
MCM-ANET-AF	STD-AT compatible ARCNET card for fiber optic star topology

WinSystems, Inc.

FEATURES

- Complete STD Bus and CMOS STD Bus Ethernet controller board
- Western Digital 8003EB software compatible
- Supports both Ethernet™ or ThinWire™ Ethernet (Cheapernet)
- 10 Mbps operation, CSMA/CD
- Meets Ethernet II, IEEE 802.3 10BASE5 and 10BASE2 standards
- User selectable interrupts
- Onboard EEPROM to store configuration information and reduce jumper options
- Onboard 8K byte data buffer
- Memory socket for BIOS ROMs
- Can be used with the WinSystems' 16-bit STD-AT or 8-bit STD Bus and CMOS STD Bus XT compatibles
- Optional software drivers available for Novell™, ViaNet™, UNIX™ and DecNet™
- Optional diagnostic software available
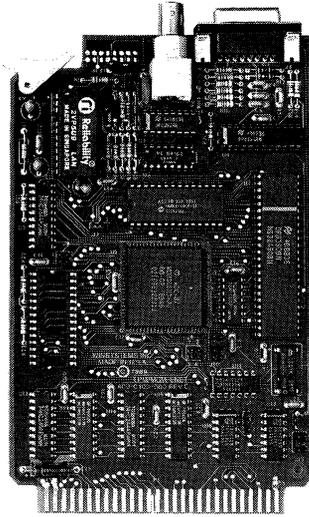
The LPM/MCM-ENET board from WinSystems is a complete local area network (LAN) adapter board designed for the STD Bus and CMOS STD Bus which is compatible with the IEEE 802.3 10BASE5 ETHERNET and 10BASE2 ThinWire ETHERNET standards. It works with either DMA or interrupt mode. The LPM/MCM-ENET card is software compatible with the Western Digital 8003EB board.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-ENET is the CMOS STD Bus version and the MCM-ENET is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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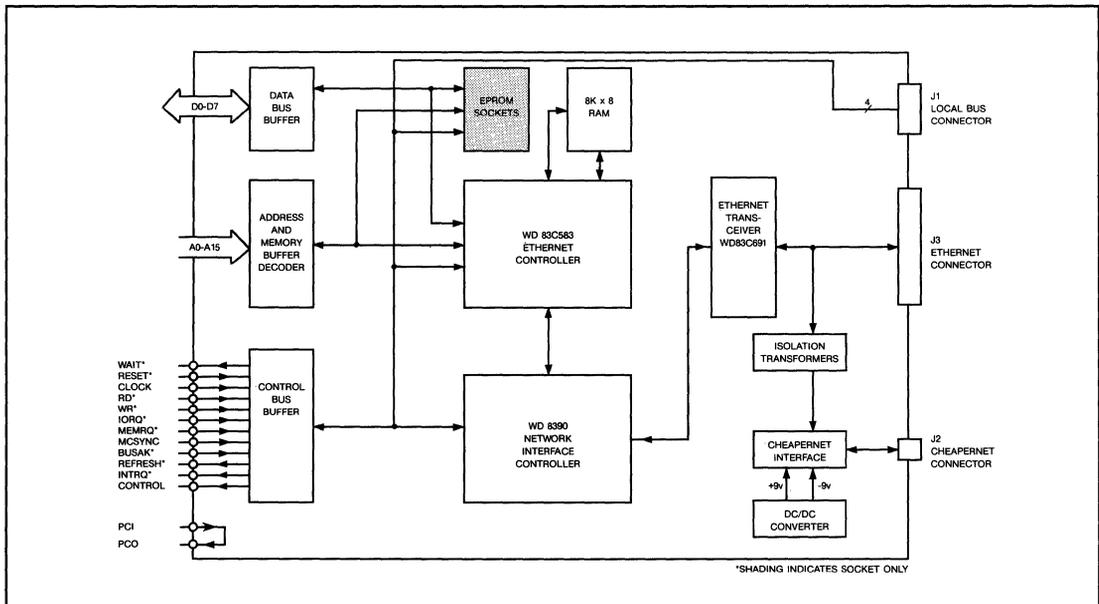
Addressing - The LPM/MCM-ENET supports either 20 or 24-bit addressing for memory and 10-bit for I/O for use with XT or AT compatible STD Bus and CMOS STD Bus processors. Address selection, memory address, memory size, BIOS ROM address, LAN address and system configuration are stored in an EEPROM.

An onboard 8KByte RAM buffer is installed that speeds up network operations and eliminates the need to use direct memory access (DMA) channels. An optional 32KByte RAM can be installed.

An EPROM socket is provided to support 8K, 16K, 32K, and 64KByte devices for software drivers. The mapping is software programmable in the EEPROM.

Ethernet vs Cheapernet - The LPM/MCM-ENET supports both Ethernet and Cheapernet (known as thin wire Ethernet). ThinWire™ is a less costly alternative baseband cabling system that provides full Ethernet capability for personal computers, workstations and low and medium performance systems.

Ethernet Network Connection - The LPM/MCM-ENET is connected to the network through commercially available transceivers and attachment unit interface (AUI) cables. One end of the AUI drop cable is attached to J3 of the LPM/MCM-ENET and the other end to a medium attachment unit (MAU) transceiver connector. MAUs can be connected every 2.5 meters at marked locations on the Ethernet cable.

Cheapernet Network Connection - The LPM/MCM-ENET is connected to an RG-58 type coaxial cable the BNC connector. It can support the standard Thin Ethernet segment or be jumpered for an optional 300 meter segment using no repeaters.

Controller - As a station adapter board, it fully meets both the ETHERNET and IEEE 802.3 standards and supports data transfers of up to 10 Mbps. The LPM/MCM-ENET uses the state-of-the-art Western Digital ETHERNET controller chips that provide all of the control for implementing the complete ETHERNET protocol. The board is software compatible with the Western Digital WD8003EB card on the PC-Bus.

Software - The LPM/MCM-ENET supports TCP/IP. The standard TCP/IP protocol provides file transfer, remote login, and electronic mail, as well as a number of other miscellaneous services such as clock setting, listing active users on a machine, and verifying that a machine is up on the network. TCP/IP is embraced by the industry as the only currently available solution to the problem of interconnecting different computer systems and network technologies.

Also an optional software diskette is available that has software drivers, utility programs and associated documentation for the LPM/MCM-ENET board. It includes a Novell™ Netware™ v2.0a driver, Novell Netware v2.1x driver, NWPATCH Utility for Netware drivers, 3Com 3+ driver, DEC DECnet-DOS and PCSA drivers, UNIX V.3 streams drivers. Also a diagnostic program and SETUP program for the Bus controller device is included.

SPECIFICATIONS

Electrical

I/O Addressing: 10-bit
Memory Addressing: 20 or 24-bit decoding
Data Transfer: 8-bits wide

Power Requirements:

Vcc = +5V ± 5% at 900 mA
       +12V at 500mA (for Ethernet only)

Mechanical

Dimensions: 4.5″ x 7.0″ (Connectors extend card)

Connectors

Cheapernet: BNC connector for RG58 A/U cable
Ethernet: DB-15
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-ENET   0°C to +65°C
    MCM-ENET   0°C to +55°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-ENET	Ethernet LAN card
MCM-ENET	Ethernet LAN card
ENET-UTIL	Driver/Utility/Diagnostic Software

WinSystems, Inc.

FEATURES

- Full Bell 212A/103 and CCITT V.22 and V.21 compatible
- FCC Part 68 Registered onboard DAA
- Recognizes industry standard "AT" Command Set
- Serial interface with 8250B UART emulation
- Call progress monitoring
- DTMF and pulse dialing
- Analog loopback and digital loopback test mode
- Processor independent including 80C186, V50, V40, V20, 80C88, 68008, HD64180, Z80, and 80C85A
- On board wait state generator
- Operation to 8 MHz system clock
- Jumper selectable 8 or 10-bit I/O addressing
- IOEXP supported
- Available for CMOS STD Bus: LPM-MODEM
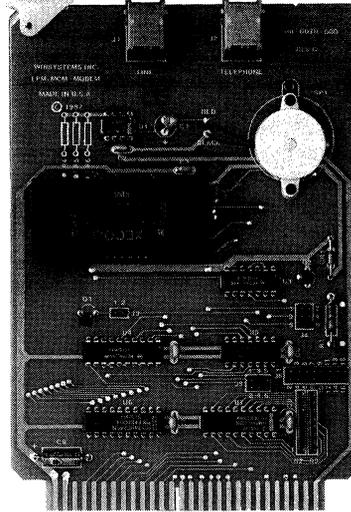
The LPM/MCM-MODEM provides a complete self contained 1200/300 bps Bell 212A/103 compatible modem on a single STD Bus and CMOS STD Bus card. The card contains all circuitry necessary to achieve complete intelligent modem functionality, including an FCC Registered, Data Access Arrangement (DAA) for direct connections to the telephone line and a 8250B UART type interface to the STD Bus and CMOS STD Bus. The card is I/O mapped and processor independent including the 80C186, 80C88, 68008, HD64180, Z80, and 80C85A.
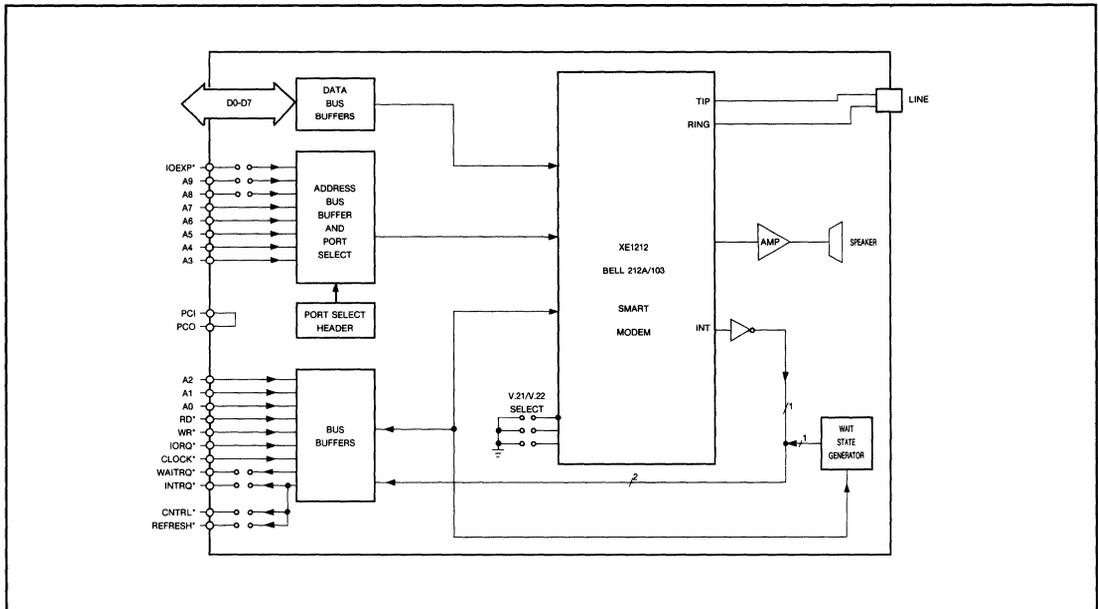
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-MODEM is the CMOS STD Bus version and the MCM-MODEM is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-MODEM is configured for 8 and 10-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8 port boundary. Address lines A0 through A2 select one of eight internal jumper register ports. A3 through A7 selects the card by a 3 selectable decoded combination. A8 and A9 are decoded for the 10-bit addressing mode. IOEXP is decoded as active high, active low, or don't care to double the I/O port addressing range.

MODEM Configuration - The LPM/MCM-MODEM supports the industry standard "AT" Command Set allowing it to be operated from all of the popular communications software. Both Dialing and Other Commands are included to offer the maximum flexibility in a "smart" modem design.

The board contains all the signal processing functions needed for a full duplex, 1200/300 bps Bell 212A/103 or CCITT V.22/V.21 modem. This includes the modulators and demodulators for both PSK and FSK operation, and high and low band analog filters.

The board includes the capability for call progress monitoring (dialtone, busy, ringback) and DTMF tone generation as well as the guard tones required for CCITT V.22/V.21 communication.

Auto Dialing - The DTMF generator will output one of the 16 standard dual tones determined by a value loaded into a control register. Pulse dialing is fixed at 10 pulses per second. It can be programmed as either a 67/33% or 61/39% make/break ratio.

The LPM/MCM-MODEM is software programmable for the number of rings with no answer, waiting time before dial tone, and time between loss of carrier and hang up.

A programmable amplifier is connected to a piezo electric transducer to allow audible monitoring of the telephone line signal. Four levels of amplification (high, medium, low, and off) are provided through the L and M commands as well as the capability to automatically turn the transducer off when a data connection is established.

Auto Answer - When an incoming ring is heard, the LPM/MCM-MODEM goes Off-Hook and returns an answer tone to the remote caller. If a carrier is not detected the LPM/MCM-MODEM terminates the call and goes On-Hook.

The LPM/MCM-MODEM is software programmable for the number of rings before answering a call, waiting time for the carrier of a remote modem, and carrier detect response time.

Self-Test - The LPM/MCM-MODEM provides analog loopback, digital loopback and remote digital loopback functions for testing purposes. Offline analog loopback is done with the telephone line disconnected and loops the data through both the analog and digital circuitry. The Online loopback test is used when a modem is receiving many errors to diagnose whether the problem is in the phone line or remote modem.

The digital loopback causes the modem to automatically resend each received character. It is used for testing a remote modem. Remote Digital loopback enables the remote modem to loop received data back to the transmitting modem. It is useful when meaningless data is received from the remote modem or vice versa.

Serial Controller - The LPM/MCM-MODEM is a full duplex serial asynchronous controller based on an emulation of the 8250B. The card will work with 7 or 8-bit characters. It will handle 1 or 2 stop bits; even, odd, or no parity bit, false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing.

Baud Rate Generation - The LPM/MCM-MODEM has an independent, software programmable, onboard crystal controlled, baud rate generator with standard data rates of 50, 75, 110, 150, 300, and 1200 bps.

Interrupts - The LPM/MCM-MODEM will generate an interrupt whenever any of the interrupt types in the Interrupt Enable Register has an active condition and is enabled. The Interrupt types are prioritized into four levels of conditions as follows: Received Data Available, Transmitter Holding Register Empty, Receiver Line Status and Modem Status. Interrupts can be individually enabled in software for any or all of the 4 possible conditions.

The board can be operated in either the polled or interrupt mode. An interrupt can be jumpered enabled on the INTRQ*, REFRESH*, or CNTRL* lines on the STD backplane or through an external interrupt status connector. Upon detecting the request, the source can be determined by reading the Interrupt Identification Register in the LPM/MCM-MODEM. The interrupt request is cleared after being serviced by the CPU.

This interrupt request is compatible with inputs to an 8259A PIC. The board will not support Z80 mode 2 type interrupts.

WAIT State Generator - The LPM/MCM-MODEM has an onboard jumper selectable WAIT State generator for use with fast CPU's.

Connectors - An RJ-llC modular jack is located at the edge of the card for access to the telephone line.

The product is FCC part 68 registered. It can be connected directly with dial up telephone lines. No connections may be made to party or coin phone lines.

Command Summary

Command	Description		
Prefix, Repeat and Escape Commands			
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands		
A/	Repeat last command line (A/ is not followed by carriage return)		
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry: (The command + + + is not followed by carriage return)		
Dialing Commands			
D	Dial		
P	Pulse		
T	Touch-tone		
,	Pause		
!	Flash		
/	Wait for 1/8 second		
@	Wait for silence		
W	Wait for second dial tone		
;	Return to command state after dialing		
R	Reverse mode (to call originate-only modem)		
Other Commands			
A	Answer call without waiting for ring	O1	Remote digital loopback off*
B/B0	CCITT V.22 and V.21 mode	O2	Remote digital loopback request
B1	Bell 212A and 103 mode*	Q/Q0	Result codes displayed
C/C0	Transmit carrier off	Q1	Result codes not displayed
C1	Carrier on*	Sr?	Requests current value of register 4
E/E0	Characters not echoed	Sr = n	Sets register r to value of n
E1	Characters echoed*	V/V0	Digit result codes
F/F0	Half Duplex	V1	Word result codes*
F1	Full Duplex*	X/X0	Compatible with 300 baud modems*
H/H0	On hook (hang up)*	X1	Result code CONNECT 1200 enabled
H1	Off hook, line and auxiliary relay	X2	Enables dial tone detection
H2	Off hook, line relay only	X3	Enables busy signal detection
I/I0	Request product ID code	X4	Enables dial tone and busy signal detection
I1	Firmware revision number	Y/Y0	Long space disconnect disabled*
I2	Test internal memory	Y1	Long space disconnect enabled
L/L1	Low speaker volume	Z	Software reset: restores all default settings
L2	Medium speaker volume*		
L3	High speaker volume		
M/M0	Speaker always off		
M1	Speaker on until carrier detected*	Note 1.	Default modes are indicated by *
M2	Speaker always on	Note 2.	Commands entered with null parameters
O	Go to on-line state		assume 0. (X is the same as X0).

SPECIFICATIONS

Electrical

All STD BUS and CMOS STD Bus processors with I/O mapping are supported with system clock to 8 MHz.

Data Rates: 300 bps (Bell type 103)
1200 bps (Bell type 212A)

Ringer Equivalence = 0.0B
FCC Registration Number DWE6TM-16564-MD-E

Vcc = +5V $\pm$ 5% at 125mA typ.,
+12V $\pm$ 10% at 40mA. typ.: LPM-MODEM
Vcc = +5V $\pm$ 5% at 250mA typ.,
+12V $\pm$ 10% at 40mA. typ.: MCM-MODEM

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Telephone: RJ-11C
Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-MODEM   1200/300 bps smart modem card

MCM-MODEM   1200/300 bps smart modem card

WinSystems, Inc.

FEATURES

- 2400, 1200, 600, 300 bps operation
- Compatible with CCITT V.22 bis, CCITT V.22, CCITT V.21, Bell 212A and Bell 103
- Supports Hayes "AT" command set
- Optional MNP support through Class 5
- Adaptive Equalization
- Auto Answer
- Auto DTMF and Pulse dialing
- FCC Part 68 Registered onboard DAA
- Telephone Line Audio Monitor
- Call progress monitoring
- Eight LED status indicators
- Diagnostic test command set

The MCM-2400 and MCM-2400MNP are a 2400/1200/300 Bps modem on a single STD Bus card. The card supports synchronous and asynchronous modes plus the industry standard "AT" command set which provides support with all popular communications software written for the PC/XT/AT.

The MCM-2400MNP board is available with Microcom Networking Protocol (MNP) support up to Class 5 for error free data communications which can increase throughput up to 200% above a normal, asynchronous 2400 bps modem.
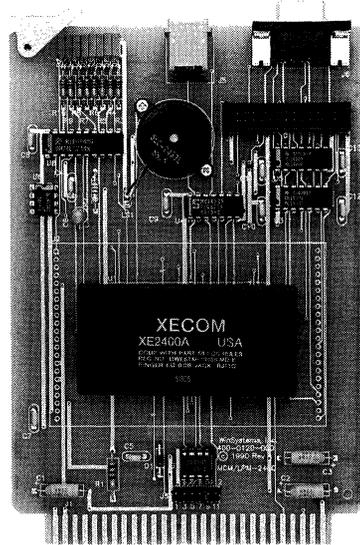
FUNCTIONAL CAPABILITY

STD Bus Interface - The MCM-2400 is a complete 2400 bps modem on a STD Bus card. The card uses
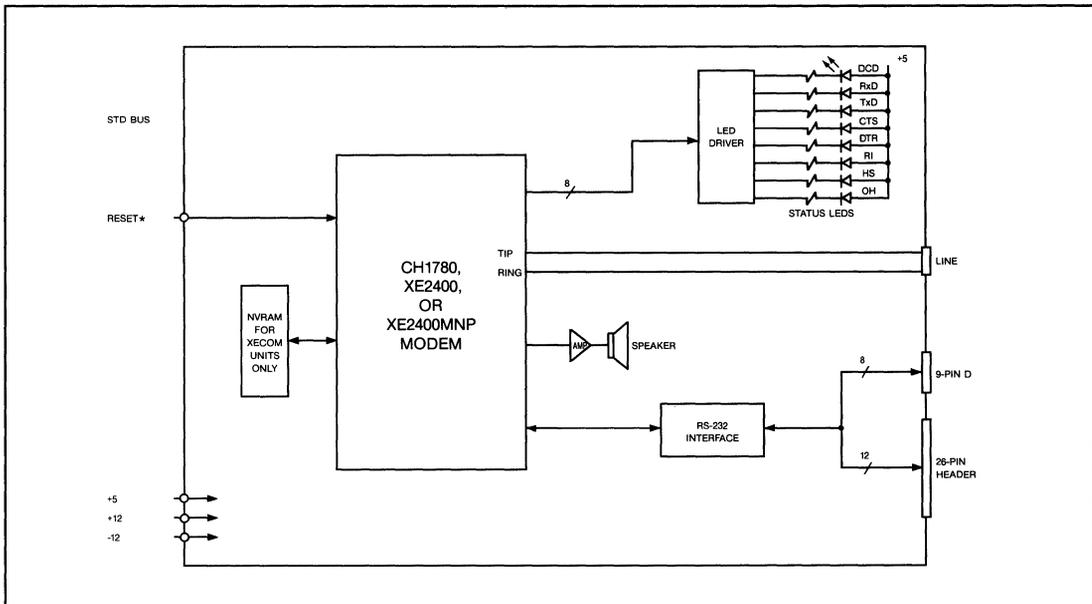
only the STD Bus power and ground. The board uses either the Cermetek or XECOM 2400 bps serial component modem.

Modem Interface - Input to the modem is through either a female DB-9 or 26-pin header on the edge of the board. The unit is wired as Data Communications Equipment (DCE). All levels are RS-232. The DB-9 connector is configured identically to the PC-AT configuration. It is the input connector recommended for WinSystems' boards such as the MCM-286AT, MCM-386SX, and MCM-DSPIO.

The 26-pin cable permits synchronous communications since it supports the transmit and receive clock signals. The 26-pin header is configured to directly accept a DB-25 configuration by using a WinSystems' CBL-101-3 or equivalent cable. It will also accept a direct 26-pin cable attached to WinSystems' boards such as the MCM-7304, MCM-7312, MCM-7314 and MCM-SIO2.

The connection to the phone line is through a RJ-11C jack. An onboard FCC registered DAA provides the required isolation and protection allowing direct connection to dial up phone lines without additional circuitry.

Compatibility - The board supports Bell 103, 212A; CCITT V.21, V.22, and V.22bis. It can communicate with the most commonly used modems at data rates of 2400, 1200, and 0-300 bps.

It also supports the Hayes "AT" Command set allowing the board to answer incoming calls, place outgoing calls (using call progress detection) and execute diagnostic tests.

MNP Support - MNP is an acronym for Microcom Networking Protocol, which was devised to provide a means for error detection and correction for high speed modem transmissions. Poor telephone line connections or noisy lines can cause erroneous data, but this protocol has the ability to detect and correct these errors.

The MCM-2400 MNP is the version of the board that supports MNP. MNP is supported up to Class 5 for error free data communications and can increase throughput up to 200% above a normal, asynchronous 2400 bps modem. MNP connections can only be obtained with another modem capable of and set to use MNP. All of the functions of the MNP are transparent to the user, once the parameters for its use are set up using the "AT" Command Set.

Line Status Indicators - Both a speaker and LEDs are built on the board to provide status to the user. The speaker allows the user to monitor the telephone line status. The speaker volume may be adjusted through software by using the Hayes Volume Command. Eight LEDs on the card edge display the status of Modem Ready, Terminal Ready, Send Data, Receive Data, Off Hook, Carrier Detect, Auto Answer, and High Speed (2400).

Self Test - The board provides analog loopback, digital loopback, and remote digital loopback functions for testing purposes.

Auto Dialing - Both pulse and tone dialing are supported. Pulse dialing is fixed at 10 pulses per second. Tone dialing is from a DTMF generator that supports the 16 standard tones. The board is programmable for number of rings with no answer, waiting time before dial tone, and time between loss of carrier and hang up.

Auto Answer - When an incoming ring is detected, the board goes Off-Hook and returns an answer tone to the remote caller. If a carrier is not detected, the MCM-2400 terminates the call and goes On-Hook.

SPECIFICATIONS

Electrical
Bell 103, 212A and CCITT V.21, V.22, and v.22 bis compatible
Power = +5VDC @ 450 mA
          +12VDC @ 50 mA
          -12VDC @ 50 mA

Mechanical
STD Bus mechanical dimensions: 4.5" x 6.5"

Connectors
STD Bus: 56-pin dual 0.125 inch centers
Telephone: RJ-11C
Serial I/O: DB-9 female amd
          26-pin, 0.100 inch grid in parallel

Environmental
Operating Temperature: 0° to +60°C
Non-condensing relative humidity: 15% to 90%

ORDERING INFORMATION

MCM-2400C	2400/1200/300 modem (Cermetek)
MCM-2400-X	Modem with EEPROM setup (Xecom)
MCM-2400MNP	2400 bps modem with MNP support

WinSystems, Inc.

FEATURES

- Complete Talker/Listener/Controller (TLC) capability using the NEC uPD7210 intelligent GPIB chip
- Software/Register compatible with NI PC-II
- 8 or 10-bit I/O addressing
- Supports polled or interrupt driven transfers
- Memory socket for BIOS extension EPROM
- Single +5 volt supply
- Available in STD and CMOS STD Bus

The LPM/MCM-488 is an IEEE-488 interface board for the STD Bus. It is designed to meet all of the control specifications required for talker, listener and controller as specified by IEEE 488-1978. This interface makes possible the transfer of data between thousands of IEEE-488 compatible devices.

The board, based upon the NEC 7210, is compatible with National Instruments' PC-II to allow its use with STD Bus DOS compatible and ROM-DOS embedded STD Bus systems

FUNCTIONAL CAPABILITY

IEEE-488 Bus - The IEEE Standard 488 is a standard digital interface for programmable instrumentation which has become an industry standard in laboratory and automatic test applications. It is an 8-bit parallel digital bus with full handshake and interface management capabilities. It is often referred to as the IEEE-488 bus, which is synonymous with GPIB.

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*SHADING INDICATES SOCKETS ONLY
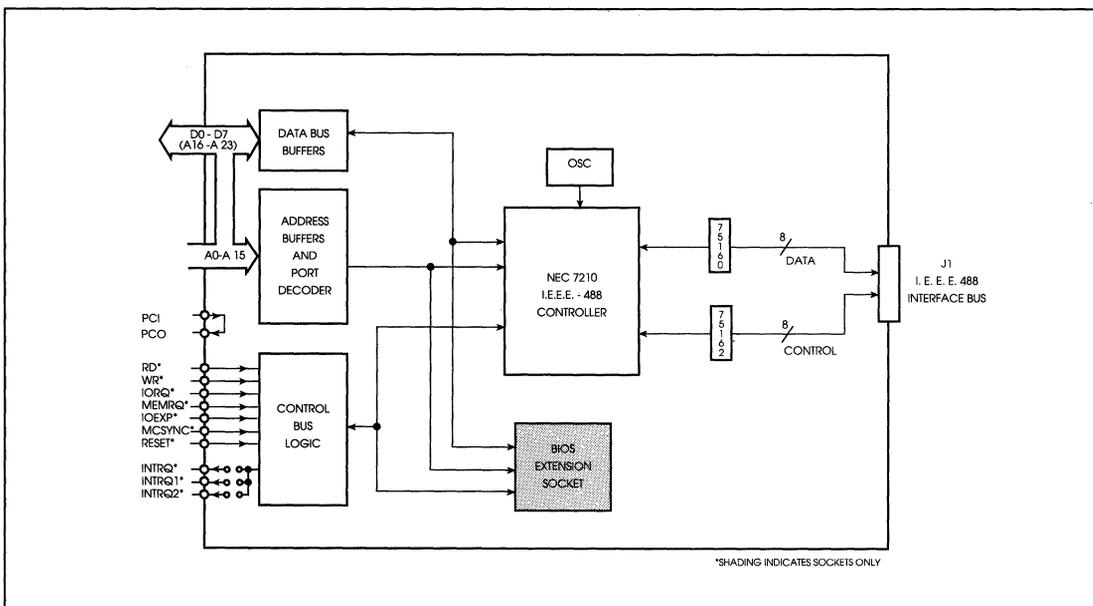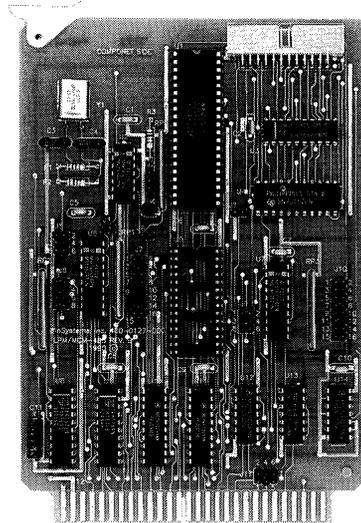
Interface Controller - The LPM/MCM-488 uses the popular NEC uPD7210 which provides most of the IEEE-488 interface functions. This intelligent controller can be programmed to serve as talker, listener, and controller.

The IEEE-488 standard specifies allowable subsets of interface functions. The codes supported by the LPM/MCM-488 are detailed in the following table.

Capability Code Description

SH1	Source Handshake
AH1	Acceptor Handshake
L3, LE3	Listener or Extended Listener
T5, TE5	Talker or Extended Talker
SR1	Service Request
RL1	Remote/Local
PP1, PP2	Local/Remote Parallel Poll
DC1	Device Clear
DT1	Device Trigger
C1 - C5	Controller, all functions

IEEE-488 Bus Transceivers - The LPM/MCM-488 is interfaced to the IEEE-488 bus by 75160A and 75162A transceivers which are designed to provide glitch-free, power-up/power-down bus protection. The CBL-148-2 adapter cable is included to link the LPM/MCM-488 to other GPIB devices.

The LPM/MCM-488 counts as 1 IEEE-488 bus load which allows an additional 14 devices to be connected before exceeding the bus loading restriction.

STD Bus Interface - Full address, data, and control line buffering is provided to and from the STD Bus. It supports the STD-8088 interrupt priority scheme over the backplane with 3 separate jumper selectable priority levels. It can operate with a systems clock up to 8MHz with one Wait State.

The LPM/MCM-488 will work with Intel 80X88 and 80X86 and the NEC "V" series processors as well as with the Z80, HD64180, and 8085 CPUs.

CMOS STD Bus - The LPM-488 is the CMOS STD Bus version of the card using 74HC-type interface circuits. The MCM-488 is the designed with standard LS/TTL integrated circuits for use with regular STD Bus systems. Programming, cable pin-outs, bus pin assignments, and jumper configurations are identical for

both the LPM-488 and MCM-488. The LPM/MCM prefix indicates the card has the same features and functionality but a different bus interface logic, power requirements and operational temperature range.

Addressing - The LPM/MCM-488 supports either 20- or 24-bit addressing for memory and 10-bit for I/O use with XT or AT compatible STD Bus processors. It also supports 8-bit I/O addressing for use with Z80, 8085 and 64180 CPUs. The NEC 7210 is I/O mapped and requires 8 contiguous locations with its base address jumper selectable. IOEXP* is also supported.

An EPROM socket is provided to support 8K to 64K byte devices for software drivers and BIOS extensions. All memory and I/O transfers are 8-bits wide.

Interrupts - An interrupt can be generated by the NEC 7210. The interrupt can be enabled and disabled under program control. They are wired via the INTRQ*, INTRQ1*, and INTRQ2* to the STD Bus backplane.

Software Support - The LPM/MCM-488 is software and register compatible with the National Instruments' PC-II card. It will run polled and interrupt driven software and DOS drivers developed for these cards as well as off-the-shelf application software such as ASYST and Paragon.

SPECIFICATIONS

Electrical
LPM-488: CMOS STD Bus
MCM-488: STD Bus
Data Transfer: 8-bits wide

Power Requirements
LPM-488:   +5 VDC @ 0.45 A typ.
MCM-488:   +5 VDC @ 0.6 A typ.

Mechanical
Dimensions: 4.5" x 6.5"

Environmental
Operating Temperature: 0°C to +65°C

ORDERING INFORMATION

LPM-488   CMOS STD Bus GPIB Controller
MCM-488   STD Bus GPIB Controller

WinSystems, Inc.

Serial and Parallel I/O Product Selector Guide

PRODUCT	TECHNOLOGY	PARALLEL I/O				SERIAL I/O	
		IN	OUT	BIDIRECTIONAL	PRINTER	CHANNELS	DEVICE
LPM-7304	CMOS	—	—	—	—	2 RS-232/485	82C51
MCM-7304	NMOS/TTL						
LPM-7312	CMOS	—	—	—	—	2 RS-232	85C30
MCM-7312	NMOS/TTL						
LPM-7314	CMOS	—	—	—	—	4 RS-232	85C30
MCM-7314	NMOS/TTL						
LPM-7507	CMOS	—	—	24	—	—	—
MCM-7507	NMOS/TTL						
LPM-7508	CMOS	—	—	48	—	—	—
MCM-7508	NMOS/TTL						
LPM-7604	CMOS	—	—	64	—	—	—
MCM-7604	NMOS/TTL						
LPM-7605	CMOS	—	—	32	—	—	—
MCM-7605	NMOS/TTL						
LPM-7614	CMOS	—	—	64	—	—	—
MCM-7614	NMOS/TTL						
LPM-DLPT	CMOS	4	—	—	2	—	—
MCM-DLPT	NMOS/TTL						
LPM-DSIO	CMOS	—	—	—	—	2 RS-232/20mA	UART
MCM-DSIO	NMOS/TTL						
LPM-DSPIO	CMOS	—	—	—	1	2 RS-232/485	8250
MCM-DSPIO	NMOS/TTL						
LPM-PIO	CMOS	—	—	32	—	—	—
MCM-PIO	NMOS/TTL						
LPM-PIO2	CMOS	32	32	—	—	—	—
MCM-PIO2	NMOS/TTL						
LPM-SIO2	CMOS	—	—	—	—	2 RS-232/485/20mA	Z80-SIO
MCM-SIO2	NMOS/TTL						
LPM-SIO4	CMOS	—	—	—	—	4 RS-232/422	82C52
MCM-SIO4	NMOS/TTL						
LPM-SPIO	CMOS	16	16	—	—	1 RS-232	UART
MCM-SPIO	NMOS/TTL						

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WinSystems®

STD BUS, CMOS STD BUS

LPM-7304
MCM-7304
Dual UART I/O

FEATURES

- Two independent, full-duplex serial ports
- RS-232-C on both channels and RS-422/485 on channel B
- Uses the 82C51A UART controller
- Independent software programmable baud rate clocks
- 50 to 19.2K bps asynchronous data rates
- Configurable as DTE or DCE interface with modem controls for each channel
- Processor independent including V53, V20, 80C88, NSC-800, HD64180, CMOS Z80, and 80C85A
- Polled or external interrupts
- IOEXP supported
- Replaces the Pro-Log 73C04
- Available for CMOS STD Bus: LPM-7304

The LPM/MCM-7304 is a dual channel serial board for the STD Bus and CMOS STD Bus. It has two 82C51A UART devices that provide 2 independent, full duplex, asynchronous RS-232-C channels. Channel B also supports RS-422/485 interface levels. It is a replacement for the Pro-Log 73C04.
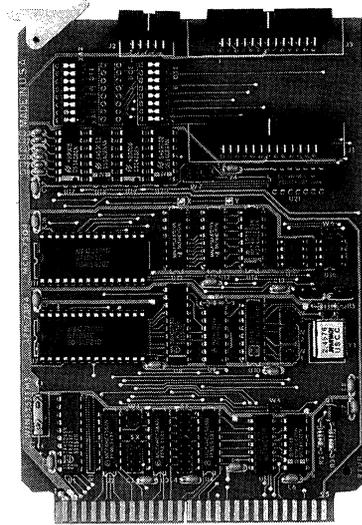
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7304 is the CMOS STD Bus version and the MCM-7304 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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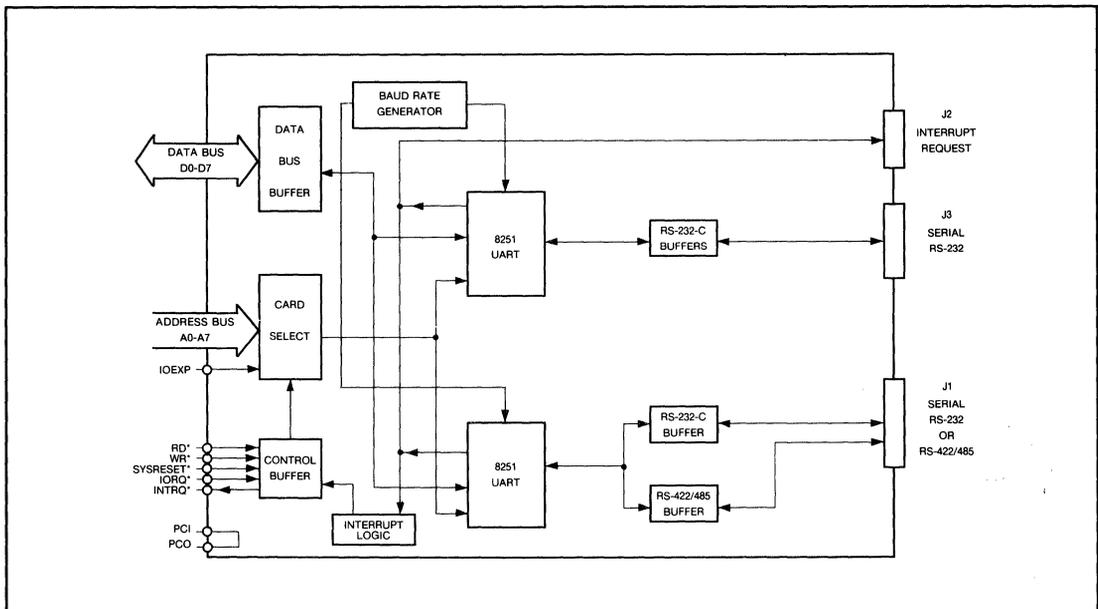
Addressing - The LPM/MCM-7304 is configured for 8-bit I/O addressing. A total of 8 consecutive I/O addresses are required on any even 8 port boundary.

Serial Controller - The LPM/MCM-7304 is a full duplex, 2 channel serial controller based on the 82C51A. The transmitter and receiver registers are doubly buffered. In the asynchronous mode, the card will work with 5 to 8-bit characters. It will handle 1, 1½, or 2 stop bits; even, odd, or no parity bit, false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing.

Baud Rate Generation - Each channel has an independent, software programmable, on board crystal controlled, baud rate generator with data rates from 110 to 19200 bps and all the standard rates (300, 1200, 2400, etc.) in between. Jumpers are available for alternate sets of baud rates.

Serial Configuration - Each channel has 4 modem handshake lines in addition to the transmit and receive lines. They are RTS, CTS, DTR, and DSR. Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation by using shorting plugs.

All signals are RS-232-C levels. Also RS-422/485 interface levels are available on channel B only. Each channel's signals are wired to a 26-pin male header on the card edge which allows easy connections to a flat cable 25-pin "D" type adapter cable. WinSystems offers both male and female type "D" to 26-pin ribbon cables designated CBL-101-3 and CBL-102-3. The signal assignment on the 26-pin headers is as follows:

Serial Channel Pinout

Pin	Description
1, 7	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
20	Data Terminal Ready (DTR)
21	RS422/485 Transmit +
22	RS422/485 Transmit -
23	RS422/485 Receive +
24	RS422/485 Receive -

Interrupts - Each serial channel can be operated in either the polled or interrupt mode. Interrupts can be asserted by the jumper enabled INTRQ* signal on the STD backplane or through an external interrupt status connector.

The LPM/MCM-7304 is plug compatible with the Pro-Log 73C04 board except for the TTY interface which was replaced by the RS-422/485 circuit.

SPECIFICATIONS

Electrical

Serial Interface: RS-232 both channels, RS-422/485 channel B only

LPM-7304:
Vcc = +5 volts $\pm$ 10% at 40mA typ., 75mA max.
+12 volts $\pm$ 10% at 2mA typ., 5mA max.
-12 volts $\pm$ 10% at 2mA typ., 5mA max.

MCM-7304:
Vcc = +5 volts $\pm$ 5% at 400mA typ., 660mA max.
+12 volts $\pm$ 10% at 60mA typ., 120mA max.
-12 volts $\pm$ 10% at 60mA typ., 120mA max.

Mechanical

Meets STD Bus mechanical specifications

Connectors

Serial I/O: Two, 26-pin dual on 0.100″ grid
Interrupt: 10-pin dual on 0.100″grid

Environmental

Operating Temperature:
LPM-7304 -40°C to +85°C
MCM-7304 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7304	Dual RS-232 and RS-422/485 CMOS serial I/O board.
MCM-7304	Dual RS-232 and RS-422/485 serial I/O board.
CBL-101-3	3-ft. ribbon cable, 26-pin ribbon to 25-pin male "D" type connector
CBL-102-3	3-ft. ribbon cable, 26-pin ribbon to 25-pin female "D" type connector

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Four independent, RS-232-C, full-duplex, serial communications channels
- Supports asynchronous and synchronous (BISYNC, SDLC, HDLC, and CCITT-X.25) protocols
- Uses the Z85C30 (CMOS SCC) controller
- Asynchronous data rates 50 to 19.2K bps
- Synchronous data rates to 307.2 Kbps
- Configurable as DTE or DCE Interface with Modem Controls
- Independent programmable baud rate clocks
- 8 or 10-bit I/O mapping
- Programmable Loopback and Auto Echo on each channel
- Interrupts supported
- Available for CMOS STD Bus: LPM-7314
- Requires very low power
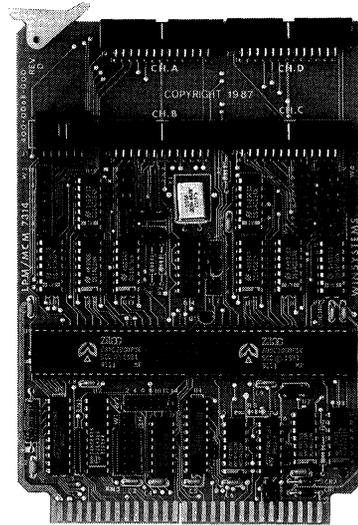
The LPM/MCM-7314 is a STD Bus and CMOS STD Bus compatible, four channel, RS-232-C input/output board, designed to be a multiprotocol asynchronous or synchronous serial communications board based upon the Z85C30 CMOS SCC. Each serial channel is independent from the other and capable of data rates of up to 19.2K baud asynchronous or 307.2K baud synchronous. The unit requires very low power and operates over an extended temperature range.
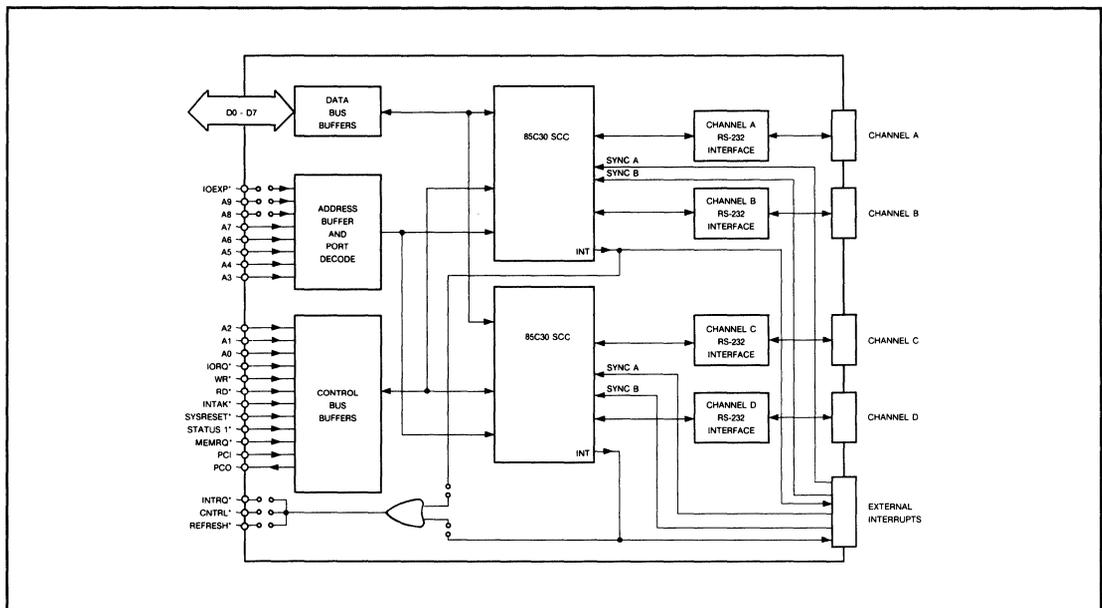
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7314 is the CMOS STD Bus version and the MCM-7314 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-7314 is configured for 8-bit or 10-bit I/O addressing. It is jumper selectable on any even 8 port boundary. IOEXP is decoded as active high, active low, or don't care and can be used to double the addressing range.

Serial Controller - Two Zilog CMOS 85C30 SCC controllers are onboard that provides four independent serial communications channels. The SCC can be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, CRC generation/checking, Digital Phase Locked Loops, and crystal oscillator circuits that reduce the need for external logic.

With access to 14 Write registers and 7 Read Registers per channel, the user can configure the SCC chip so that it can handle all standard asynchronous formats regardless of data size, number of stop bits, or parity requirements. It also supports multiple synchronous protocols including character, byte, and bit-oriented protocols such as BiSync, SDLC, HDLC, etc.

Within each operation mode, the Z85C30 SCC allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation and checking, break and abort generation and detection, and many protocol dependent features.

Asynchronous Communications - In the asynchronous mode, the card will work with 5 to 8-bit characters. Transmission and reception can be handled independently on each channel. Reception is protected by a transient spike-rejection mechanism that checks the signal one-half of a bit time after a low level is detected on the receive data input. If the low level does not persist, the character assembly does not start.

The SCC will handle 1, 1½, or 2 stop bits, optional even or odd parity, false start bit detection, and automatic break detection and handling. A built in checking process avoids the interpretation of a

framing error as a new start bit. Each channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream.

Synchronous Communications - In synchronous mode, the SCC will support both bit and byte oriented sychronous communications including BiSysnc, SDLC, and HDLC. Synchronous byte oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous (Monosync), any 12-bit synchronization pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU. The External Synchronization mode is supported with an input pin from the channel's respective I/O connector or external interrupt input connector. Five or seven bit synchronous characters can also be detected.

The SCC supports Synchronous bit oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. The transmitter can be programmed to send an idle line consisting of continuous flag characters or a steady marking condition. The SCC supports SDLC loop mode in addition to normal SDLC.

NRZ, NRZI, or FM coding may be used. The parity options available in Asynchronous modes are available in Synchronous modes.

Both CRC-16 and CCITT error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes.

Auto Echo and Local Loopback - The SCC is capable of automatically echoing everything it receives. This feature is mainly used in asynchronous modes, but works in synchronous and SDLC modes as well. Auto Echo mode can be used with NRZI and FM encoding with no additional encoding delay.

Baud Rate Generation - The LPM/MCM-7314 has a master 4.9152 MHz crystal oscillator. Each channel contains an independent baud rate generator that can be programmed to generate standard baud rates. It consists of a 16 bit down counter that produces a square wave output. It can be used as a transmit clock, receive clock, or both. It can also drive the Digital Phase-Lock Loop.

Digital Phase-Lock Loop - The SCC contains a Digital Phase-Lock Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL uses the baud rate clock along with the data stream, to construct a clock for the data.

Serial Configuration - Each channel has 4 modem handshake lines and 3 clock lines in addition to the transmit and receive lines. These lines are RTS, CTS, DTR, DSR, TCLK, and RCLK (DA and DD). Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation. All signals are RS-232 levels except for the External Sync signal (pin 26). The signals from each channel are brought out to separate 26-pin male right angle headers on the card edge which allows easy connections to a flat cable 25-pin "D" type adapter cable. WinSystems offers both male and female type "D" to 26-pin ribbon cables designated CBL-101-3 and CBL-102-3.

The signal assignment on the 26-pin headers is as follows:

Serial I/O Channels A - D

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Signal Ground
15	Receive Clock (DB)
17	Receive Clock (DD)
20	Data Terminal Ready (DTR)
24	Transmit Clock (DA)
26	External Sync

Interrupts - The LPM/MCM-7314 will generate interrupts for 80X88 type processors. The interrupts are driven out on the INTRQ* line on the bus. Acknowledgement is a function of the processor's interrupt acknowledgement scheme.

For 80C85, 80C88, V20, V40, and V50 processors, the LPM/MCM-7314 provides inputs to an off board 82C59A PIC or a processor restart input either via the backplane or over the STD Bus and CMOS STD Bus card's front plane. The LPM/MCM-7314 supports the STDMG's STD-8088 Specification Rev 2.3 for interrupts, but will not support a non-standard 80C88 serial daisy chain configuration.

Interrupt requests can be generated by either chip or by ORing each together as a single interrupt per board. The interrupt requests are wired to pins 9 and 11 of the Interrupt Connector on the top of the board. Alternately, the interrupt requests can be jumper selected to drive INTRQ*, CNTRL*, or

REFRESH* on the backplane. This option is provided to allow multiple interrupt souces in a STD BUS and CMOS STD Bus system to input an off board 82C59 PIC without having to connect external wires between boards in a card cage.

Upon detecting an interrupt request by the LPM/MCM-7314, both the vector and status registers in the SCC can be determined by reading Read Register 2 (RR2) and Read Register 3 (RR3) in the respective chip. The interrupt request is simply cleared through software by outputting the correct command word sequence.

External Interrupts - Four external inputs are wired from the external interrupt input connector to the SCC's Sync input pin. These inputs are TTL compatible and serve as either a Sync input or output depending upon the programming. The Sync input can also be programmed to generate an interrupt to the CPU rather than signaling an external sync has been established.

External Interrupt Connector

Pin	Signal
1	Interrupt Request A (input)
3	Interrupt Request B (input)
5	Interrupt Request C (input)
7	Interrupt Request D (input)
9	INTRQ SCC #1 (output)
11	INTRQ SCC #2 (output)
2,4,6,8,10,12	Ground

LPM/MCM-7312 - A dual channel version of the LPM/MCM-7314 is available as the LPM/MCM-7312. It is the same board only depopulated to offer a more cost effective solution when only 2 serial channels are required.

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SPECIFICATIONS

Electrical

System Clock: Up to 8.0 MHz

Serial Interface: Synchronous/Asynchronous operation with modem control and receive clock inputs. Jumper configurable as either DCE or DTE; RS-232 signal levels

Baud Rates: 50 to 78.6 Kbaud (Async)

LPM-7314:
Power: = +5V $\pm$ 10% at 60mA typ.
+12V $\pm$ 10% at 5mA typ.
-12V $\pm$ 10% at 5mA typ.
MCM-7314:
Power: = +5V $\pm$ 10% at 250mA typ.
+12V $\pm$ 10% at 55mA typ.
-12V $\pm$ 10% at 55mA typ.

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

Serial I/O: Four, 26-pin dual on 0.100" grid
Interrupt: 12-pin dual on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature:
LPM-7314   -40°C to +85°C
MCM-7314   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7314   Quad Serial RS-232 Multiprotocol Card

LPM-7312   Dual Serial RS-232 Multiprotocol Card

MCM-7314   Quad Serial RS-232 Multiprotocol Card

MCM-7312   Dual Serial RS-232 Multiprotocol Card

WinSystems, Inc.

FEATURES

- 24 bidirectional lines of fully buffered I/O
- Designed to interface directly to standard industrial isolation I/O module racks (Opto-22, Gordos, etc.)
- TTL compatible I/O ports
- Pull-up resistors on all I/O lines
- Easy to use with no complicated peripheral chip initialization routines required
- Output port controlled power source for module rack power
- Processor independent including V50, 80C88, CMOS Z80, NSC-800, HD64180, and 8085A
- Up to 8 MHz operation
- Replaces Pro-Log 75C07
- Single + 5V operation
- Available for CMOS STD Bus: LPM-7507

The LPM/MCM-7507 is a general purpose parallel input/output cards with a total of 24 bidirectional lines. These I/O lines are organized as three, 8-bit bi-directional I/O ports, that interface directly to industry standard 4, 8, 16, and 24-I/O module mounting racks (Opto-22, Gordos, etc.). The card is I/O mapped and processor independent.
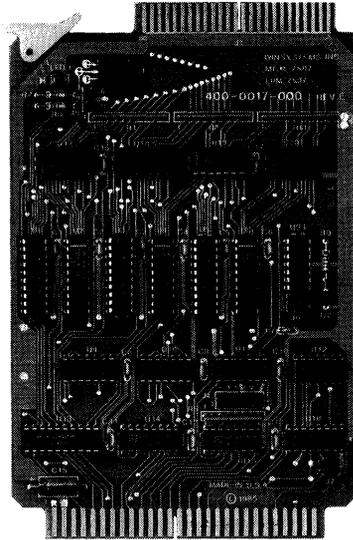
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7507 is the CMOS STD Bus version and the MCM-7507 is the STD Bus version

of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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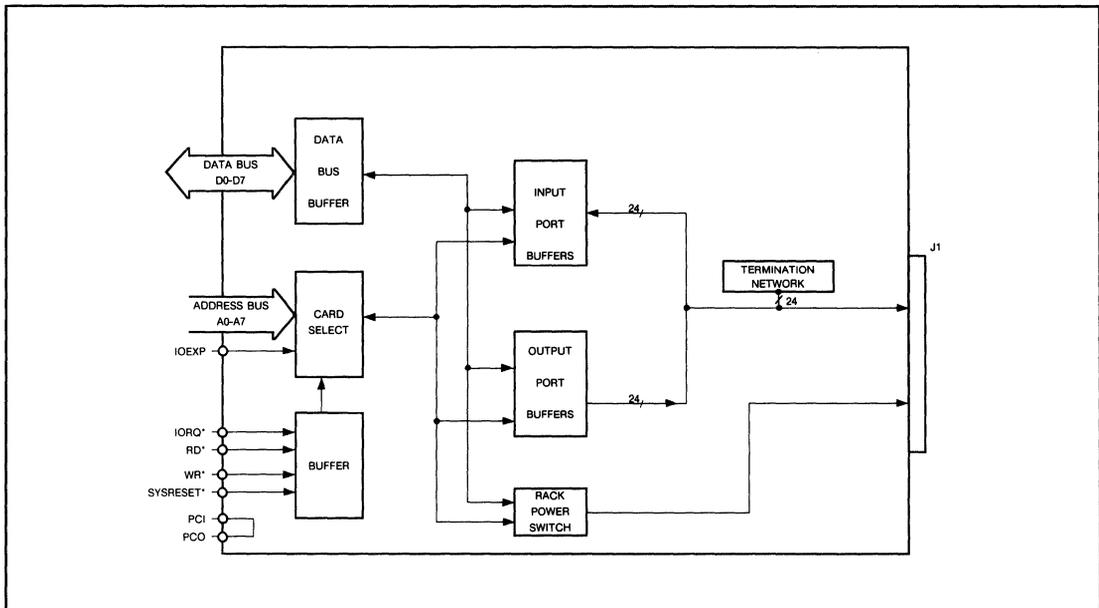
Addressing - The card is configured for 8-bit I/O addressing. A total of 4 consecutive I/O addresses are required and it is selectable on any even 4 port boundary. IOEXP is also decoded.

Configuration - The card is a STD Bus and CMOS STD Bus compatible parallel input/output card with a total of 24 I/O lines. These I/O lines are organized as three 8-bit bidirectional ports so that all 24 channels are individually software selectable as digital inputs or digital outputs.

Each data line can be configured as input, output or output with readback. Each digital output channel is latched and has an open collector driver (with a pull-up resistor) capable of sinking 35 mA of current. The input lines are connected so the current status of its output port can be read from the corresponding input port (readback). If the port is used as input only, then the corresponding output port bit must be cleared.

I/O Connector - The I/O ports are accessed through a 50-pin edge card connector located at the top of the board. The 24 bidirectional data lines are alternated with 24 ground lines (for reduced noise and crosstalk). Also a switched rack power line and ground line are wired to the connector on the LPM/MCM-7507 only. A 50 conductor ribbon cable such as the WinSystems' CBL-114-4 connects the LPM/MCM-7507 to the I/O rack.

The pinout is compatible to an industry standard I/O module mounting rack (Opto-22, Gordos, Crydom, etc.) for use with high level AC and DC signal interfacing. Any type of digital input or output module may be used with the I/O mounting rack (AC input, AC output, DC input, and DC output).

Rack Power - Power for biasing the I/O module rack is supplied on the LPM/MCM-7507 card only. Jumpers are available on the board that connect the +5 volts through a current limiting resistor to the connector. The card is capable of sourcing up to 500 mA to the I/O module mounting rack. Under software control, the rack power can be switched on or off. The unit is jumper selectable to power up with either the power on or off to the rack. With a jumper change, the power source can be permanently enabled.

SPECIFICATIONS

Electrical

Output ports: I_{OH} = - 2.85 mA at 2.4 V
I_{OL} = 35 mA at 0.7 V

LPM-7507 = +5 VDC $\pm$ 10% at 190mA. typ.
(No rack power and no load on inputs or outputs).
MCM-7507 = +5 VDC $\pm$ 10% at 600mA. typ.
(No rack power and no load on inputs or outputs).

Mechanical

Meets STD Bus mechanical specifications

Connector

STD Bus: 56-pin dual 0.125 inch centers
Parallel I/O: 50-pin dual card edge on 0.100 inch centers (LPM/MCM-7507)

Environmental

Operating Temperature:
LPM-7507   -40°C to +85°C
MCM-7507   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7507   24 line digital I/O card with 50-pin edge card

MCM-7507   24 line digital I/O card with 50-pin edge card

CBL-114-4   4 ft. ribbon cable, interfaces the LPM/MCM-7507 to Opto-22 compatible I/O racks

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

WinSystems®

STD BUS, CMOS STD BUS

LPM-7508
MCM-7508
Digital I/O Card

FEATURES

- 48 bidirectional lines of fully buffered I/O
- Designed to interface directly to 2 standard industrial isolation I/O module racks (Opto-22, Gordos, etc.)
- Dual latching header connectors
- TTL compatible I/O ports
- Pull-up resistors on all I/O lines
- Output port controlled power source for module rack power
- 8 or 10-bit I/O address decoding
- Processor independent including V50, V40, 80C88, NSC-800, CMOS Z80, HD64180, 80C85A and 6502
- IOEXP supported
- Up to 8 MHz operation
- Single + 5V operation
- Available for CMOS STD Bus: LPM-7508
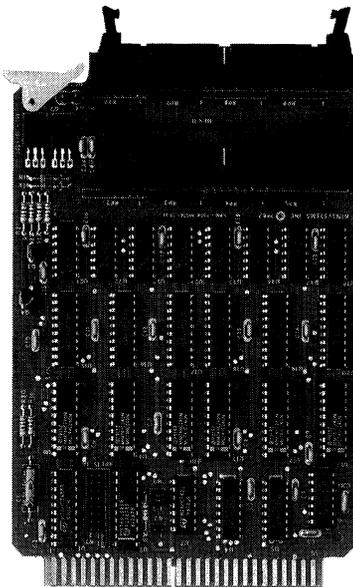
The LPM/MCM-7508 is a general purpose TTL parallel input/output card with a total of 48 bidirectional lines. These I/O lines are organized as 2 groups of three 8-bit bi-directional I/O ports that interface directly to 2 independent industry standard 4, 8, 16, and 24-I/O module mounting racks (Opto-22, Gordos, etc.). The card is I/O mapped and processor independent.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7508 is the CMOS STD Bus version and the MCM-7508 is the STD Bus version of this card. The LPM/MCM prefix indicates the card
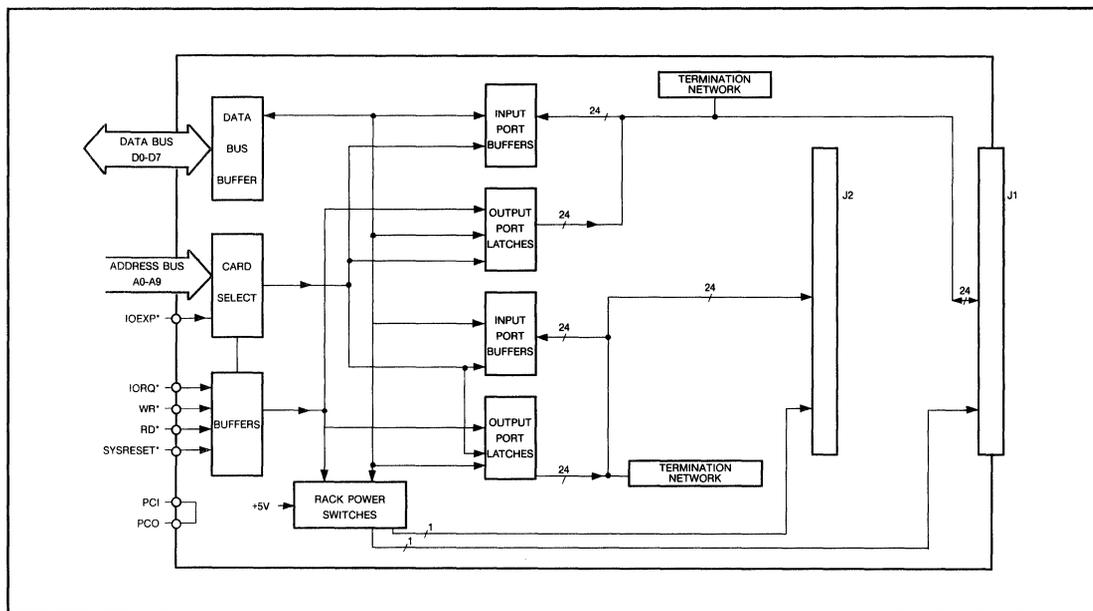
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has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-7508 is configured for either 8 or 10-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8-port boundary. Address lines A0 through A2 select one of eight sequential ports. A3 through A7 selects the card by a jumper selectable decoded combination. A8 and A9 are decoded for the 10-bit addressing mode. IOEXP is also decoded as either active high, active low or don't care.

Configuration - The LPM/MCM-7508 is a STD Bus and CMOS STD Bus compatible parallel input/output card with a total of 48 I/O lines. These I/O lines are organized as two groups of three 8-bit bidirectional ports so that all 48 channels are individually software selectable as digital inputs or digital outputs. This is the equivalent of two LPM/MCM-7507 cards.

Each data line can be configured as input, output or output with readback. Each digital output channel is latched and has an open collector driver (with a pull-up resistor) capable of sinking 20 mA of current. The input lines are connected so the current status of its output port can be read from the corresponding input port (readback). If the port is used as input only, then the corresponding output port bit must be cleared.

I/O Connector - The I/O ports are accessed through two 50-pin right angle latching connectors located at the top of the board. Each connector has 24 data lines. The 24 3bidirectional data lines are alternated with 24 ground lines (for reduced noise and crosstalk). Also a switched rack power line and ground line are wired to each connector. A 50 conductor ribbon cable such as the WinSystems' CBL-115-4 connects the LPM/MCM-7508 to one I/O rack. Two cables are required to fully utilize this card, one for each I/O rack.

The pinout is compatible to an industry standard 4 to 24 position I/O module mounting rack (Opto-22, Gordos, Crydom, etc.) for use with high level AC and DC signal interfacing. Any type of digital input or output module may be used with the I/O mounting rack (AC input, AC output, DC input, and DC output).

The LPM/MCM-7508 is very easy to use. No complicated peripheral chip initialization routines are required to access the board.

Rack Power - Power for biasing each I/O module rack may be supplied through the LPM/MCM-7508. Jumpers are available on the board that connect the +5 volts through a current limiting resistor to the connector. The card is capable of sourcing up to 500 mA to each I/O module mounting rack. Under software control, the rack power can be switched on or off to either or both racks.

SPECIFICATIONS

Electrical

STD Bus and CMOS STD Bus

I/O Capacity: 48 bi-directional I/O lines

Input ports: 74HC240 with 10K ohm pull up resistors
Output ports: I_{OH} = - 3.0 mA at 2.0 V
$\qquad\qquad\quad$ = 20 mA at 0.7 V

LPM-7508:
Power = +5 VDC $\pm$ 10% at 400mA typ.
$\qquad$ (No rack power and no load on
$\qquad$ inputs or outputs).
MCM-7508:
Power = +5 VDC $\pm$ 5% at 750mA typ.
$\qquad$ (No rack power and no load on
$\qquad$ inputs or outputs).

Mechanical

Meets STD Bus mechanical specifications

Connector

STD Bus: 56-pin dual 0.125 inch centers
Parallel I/O: Two 50-pin dual latching 0.100 inch grid

Environmental

Operating Temperature:
$\qquad$ LPM-7508 $\qquad$ -40°C to +85°C
$\qquad$ MCM-7508 $\qquad$ 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7508 $\qquad$ 48 line digital I/O card
MCM-7508 $\qquad$ 48 line digital I/O card
CBL-115-4 $\qquad$ 4 ft. ribbon cable, interfaces the
$\qquad\qquad\qquad$ LPM-7508 to Opto-22 compatible
$\qquad\qquad\qquad$ I/O module racks

WinSystems, Inc.

FEATURES

- Eight, 8-bit I/O ports
- Each port configurable as input, output, or output with readback
- Pull-up resistors on all input ports
- Processor independent including V50, V40, 80C88, NSC-800, HD64180, Z80, and 80C85A
- Replacement for the Pro-Log 76C04
- Operation to 8 MHz
- Jumper selectable I/O addressing
- IOEXP supported
- +5 Volt operation
- Available for CMOS STD Bus: LPM-7604

The LPM/MCM-7604 provides 64 TTL input/output lines between a STD Bus and CMOS STD Bus system and peripheral devices. Grouped as 8 ports of 8 lines, each port can be configured as 8 inputs or 8 outputs with readback. The card is I/O mapped and processor independent including the V50, V40, 80C88, HD64180, CMOS Z80, NSC-800, and 80C85A. It replaces the Pro-Log 76C04.
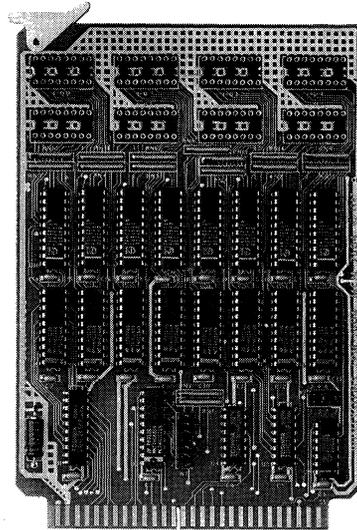
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7604 is the CMOS STD Bus versions and the MCM-7604 is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and function-ality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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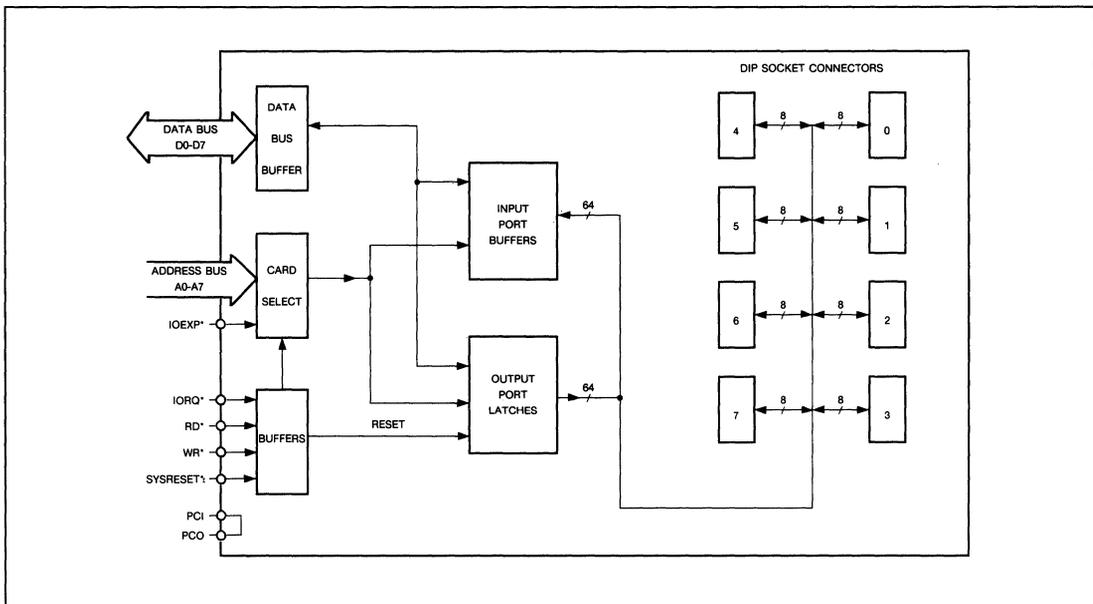
Addressing - The LPM/MCM-7604 is configured for 8-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8-port boundary. Address lines A0 through A2 select one of eight sequential ports. A3 through A7 selects the card by a jumper selectable decoded combination. IOEXP is decoded as active high, active low, or don't care.

Configuration - The LPM/MCM-7604 is a STD Bus CMOS STD Bus compatible parallel input/output card arranged as 8 ports of 8 I/O lines for a total of 64 I/O lines. Each port is organized as eight inputs, 8 outputs or 8 outputs with readback. The LPM/MCM-7604 is very easy to use. No complicated peripheral chip initialization routines are required to access the board.

Input Ports - The noninverting input data bus buffers are connected directly to the connector. Data is gated onto the CMOS STD Bus and STD Bus when the respective port is selected. Each input line is equipped with a pull-up resistor to assure that unconnected lines do not float. Each input line of the MCM-7604 is connected to a 74LS244 type data bus buffer with 0.4 volts of hysteresis. The LPM-7604's input line accepts TTL levels and is connected to a 74HC244 type data bus buffer. The input port on both boards can be used in conjunction with the output ports to provide readback of the output data status.

Output Ports - The MCM-7604's noninverted and the LPM-7604's TTL compatible noninverted output data are latched into a data bus buffer and connected to the output connector. The output latches are cleared by SYSRESET* or by a power-on reset. Additionally, the outputs on the MCM-7604 can drive 17 LSTTL loads. The input port buffers can remain installed on the card to allow monitoring of the output lines.

Both the input buffers and output latches are socketed for removal and board reconfiguration.

Connector - The I/O ports are accessed through eight 16-pin machine tooled DIP connectors located at the top of the board.

Each connector has alternating grounds paired with 16 signal lines for quiet operation for better noise immunity and reduced cross-talk.

SPECIFICATIONS

Electrical

I/O Capacity: Eight, 8-bit input/output ports
I/O Addressing: Jumper selectable on any even 8 port boundary

Vcc = +5V $\pm$ 10% at 25mA typ.: LPM-7604
Vcc = +5V $\pm$ 5% at 560mA typ.: MCM-7604

Mechanical

Meets STD Bus mechnical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Parallel I/O: Eight, 16-pin DIP sockets on 0.100″ grid
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-7604   -40°C to +85°C
    MCM-7604   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7604   64 line CMOS I/O card
MCM-7604   64 line I/O card

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Four independent 8-bit ports with 32 lines
- Configurable as input, output, or output with read-back on a per line basis
- Open collector output drivers
- Interface ICs socketed
- Available as inverting and non-inverting I/O Latching I/O connectors
- IOEXP supported
- +5 volt operation
- Available for CMOS STD Bus: LPM-7605

The LPM/MCM-7605 is a highly versatile, 4 port parallel input/output TTL interface card designed to provide a flexible interface between a processor and peripheral devices. The parallel lines are individually configured as input, output, or output with readback and are accessable at two 40-pin connectors. The board is designed to work with all I/O mapped STD Bus and CMOS STD Bus processors including the 6809, Z80, 80C85A, NSC800, HD64180, 80C88, V40 and V53.
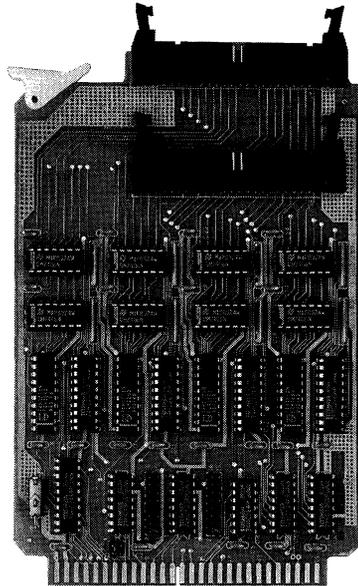
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7605 is the CMOS STD Bus version and the MCM-7605 is the STD Bus version of this card. THE LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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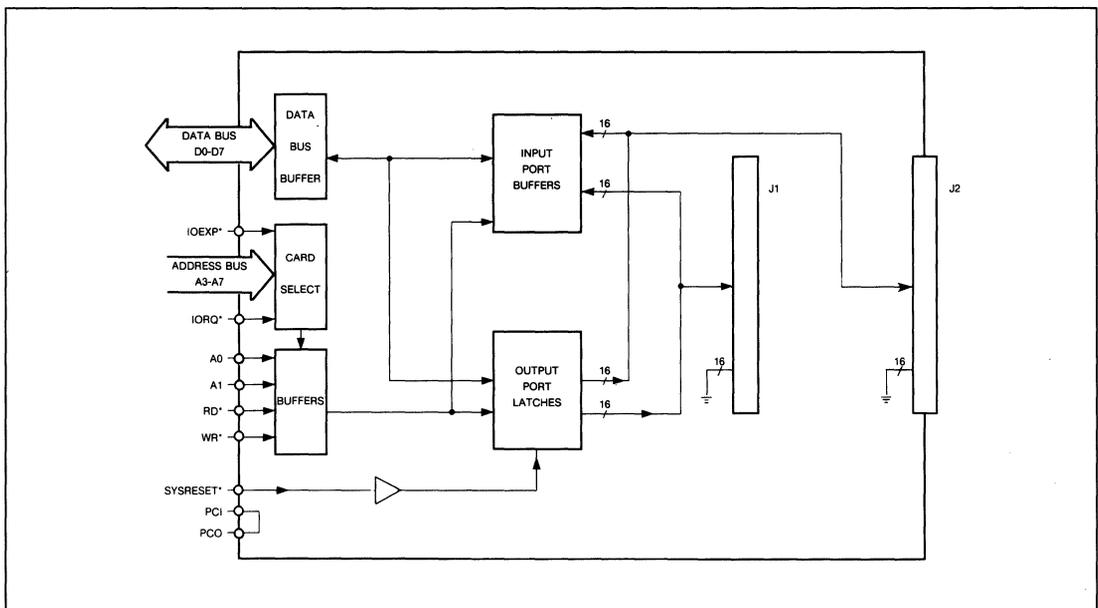
Addressing - The LPM/MCM-7605 occupies 4 consecutive I/O locations in the 256 byte I/O map and is jumper selectable on any even 4 byte boundary. IOEXP is also decoded for expansion.

Data Buffers - The LPM/MCM-7605 provides 32 lines of TTL compatible I/O between the processor and peripheral devices. The board is organized as 4 independent ports capable of input, output, or output with readback on a per bit basis. Any of the 32 I/O lines can be individually programmed as input or output.

Input operations allows the data from the external connector to be buffered and read into the CMOS STD Bus computer. Additional, the MCM-7605's input buffers have Schmitt-triggers which give a 200mV hystersis immunity from noise-induced voltage spikes.

The output port latches the last data written to the respective port bit, buffers it and interfaces it to the external connector. The output drive capability of each line is 15 LSTTL loads for the LPM version, and the MCM version has the capability of 50 LSTTL loads. The output device is an open collector device that is either inverting (LPM/MCM-7605-0) or non-inverting (LPM/MCM-7605-1) depending upon the driver in the socket.

The output lines are TTL compatible open collector drivers with pullup resistors that are tied back to their respective inputs. This provides a readback circuit to allow the user to monitor the status each output line. It also allows each signal to individually be configured as input or output on a per line basis.

The SYSRESET* signal clears the latches on the output port and puts all the lines in the input mode which means that no initialization programming is required at system power-on.

Connector - Two 40-pin latching connectors are located on the top of the board that permits mass termination with flat ribbon cable. All buffered data lines are brought to the connector, two ports per connector. The data lines are interleaved with alternating ground lines to reduce the noise and crosstalk.

J1 and J2 Interface Connector Pinout

Pin	Signal	Pin	Signal
2	+5V	2	+5V
4	+5V	4	+5V
6	A-7	6	C-7
8	A-6	8	C-6
10	A-5	10	C-5
12	A-4	12	C-4
14	A-3	14	C-3
16	A-2	16	C-2
18	A-1	18	C-1
20	A-0	20	C-0
22	+5V	22	+5V
24	+5V	24	+5V
26	B-7	26	D-7
28	B-6	28	D-6
30	B-5	30	D-5
32	B-4	32	D-4
34	B-3	34	D-3
36	B-2	36	D-2
38	B-1	38	D-1
40	B-0	40	D-0

SPECIFICATIONS

Electrical

Input ports: Fourteen 74LS Load Max.

Output ports: I_{OH} = -2.85 mA max. at 2.4V

I_{OL} =35mA max. at 0.7V

Vcc = +5V $\pm$ 10% at 190mA typ.: LPM-7605
Vcc = +5V $\pm$ 5% at 600mA typ., 0.85 A Max.: MCM-7605

Mechanical

Meets STD Bus mechanical specifications

Connectors

Jumpers: 0.025" square posts
Parallel I/O: 40 pin 0.100" grid

Environmental

Operating Temperature:
 LPM-7605   -40° to +85°C
 MCM-7605   0° to +60°C
Non-condensing relative humidity: 0% to 95%

### ORDERING INFORMATION

LPM-7605-0 32-bit parallel I/O card: (inverting)
LPM-7605-1 32-bit parallel I/O card: (non-inverting)
MCM-7605-0 32-bit parallel I/O card: (inverting)
MCM-7605-1 32-bit parallel I/O card: (non-inverting)

WinSystems, Inc.

FEATURES

- Eight 8-bit I/O ports
- Each port configurable as input, output, or output with readback
- Latching I/O connectors for added reliability
- Pull-up resistors on all input ports
- Processor independent including V50, V40, 80C88, NSC-800, HD64180, Z80, and 80C85A
- Compatible with Pro-Log 76C14
- Operation to 8 MHz
- Jumper selectable 8 or 10-bit I/O addressing
- IOEXP supported
- +5 Volt operation
- Available for CMOS STD Bus: LPM-7614
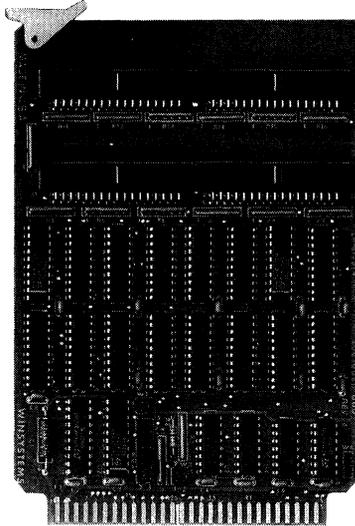
The LPM/MCM-7614 provides 64 TTL input/output lines between a STD Bus and CMOS STD Bus system and peripheral devices. Grouped as 8 ports of 8 lines, each port can be configured as 8 inputs or 8 outputs with readback. The card is I/O mapped and processor independent including the V50, V40, 80C88, NSC-800, HD64180, CMOS Z80, and 80C85A.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7614 is the CMOS STD Bus versions and the MCM-7614 is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and function-ality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges. This board is compatible with the Pro-Log 7614.

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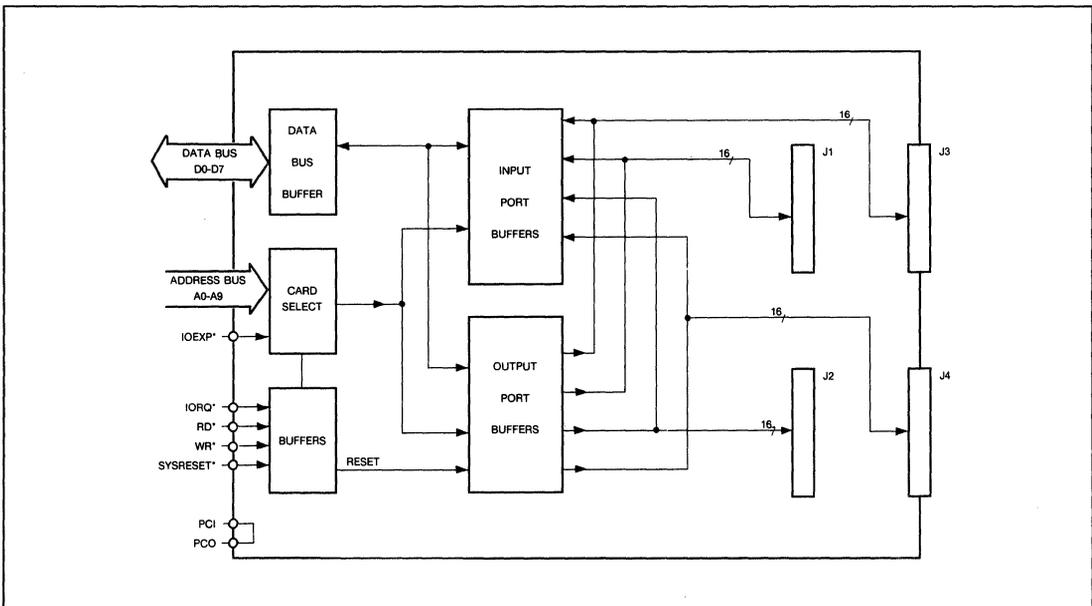
Addressing - The LPM/MCM-7614 is configured for 8 and 10-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8 port boundary. Address lines A0 through A2 select one of eight sequential ports. A3 through A7 selects the card by a jumper selectable decoded combination. A8 and A9 are decoded for the 10-bit addressing mode. IOEXP is decoded as active high, active low, or don't care.

Configuration - The LPM/MCM-7614 is a STD Bus and CMOS STD Bus compatible parallel input/output card arranged as 8 ports of 8 I/O lines for a total of 64 I/O lines. Each port is organized as 8 inputs, 8 outputs or 8 outputs with readback.

The LPM/MCM-7614 is very easy to use. No complicated peripheral chip initialization routines are required to access the board.

Input Ports - The noninverting input data bus buffers are connected directly from the connector. Data is gated onto the CMOS STD and STD Bus when the respective port is selected. Each input line is equipped with a pull-up resistor to assure that unconnected lines do not float. Each input line of the MCM-7614 is connected to a 74LS244 type data bus buffer with 0.4 volts of hysteresis. The LPM-7614's input is connected to a 74HC244 type data bus buffer. The input port on both boards can be used in conjunction with the output ports to provide readback of the output data status.

Output Ports - Noninverted output data is latched into a data bus buffer and connected to the output connector. The output latches are cleared by SYS-RESET* or by a power-on reset. Additionally, the outputs on the MCM-7614 can drive 17 LSTTL loads. The input port buffers can remain installed on the card to allow monitoring of the output lines.

Both the input buffers and output latches are socketed for removal and board reconfiguration.

Connector - The I/O ports are accessed through four 34-pin right angle locking connectors located at the top of the board. These connectors are more reliable and less likely to disconnect than DIP type connectors.

Each connector has alternating grounds paired with 16 signal lines for quiet operation for better noise immunity and reduced cross-talk. The remaining 2-pins on each connector are also wired to ground.

SPECIFICATIONS

Electrical

I/O Capacity: Eight, 8-bit input/output ports
I/O Addressing: Jumper selectable on any even
                8 port boundary

$Vcc = +5V \pm 10\%$ at 39mA typ.: LPM-7614
$Vcc = +5V \pm 5\%$ at 550mA typ.: MCM-7614

Mechanical

Meets STD Bus mechnical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Parallel I/O: Four, 34-pin dual latching on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature:
    LPM-7614   -40°C to +85°C
    MCM-7614   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7614   64 line CMOS I/O card with latching
            connectors
MCM-7614   64 line TTL I/O card with latching
            connectors

WinSystems, Inc.

FEATURES

- Two PC compatible parallel printer ports
- Programmable board I/O address selectable for PC-XT/AT hardware/software compatibility
- PC compatible Joystick port onboard
- Printer interrupt supported
- 10-bit addressing
- Low Cost
- +5 volt only operation
- Available in CMOS as the LPM-DLPT

The LPM/MCM-DLPT is a low cost, dual Centronics parallel I/O and joystick card for the STD Bus for DOS and ROM-DOS applications. It can also be used as a general purpose parallel I/O card if printer support is not needed on one or both channels. It is ideally suited for printer port expansion for applications running DOS programs or languages that require exact register compatible hardware for program execution.

FUNCTIONAL CAPABILITY

Bus Interface - Full address, data, and control line buffering is provided to and from the STD Bus. The LPM/MCM-DLPT supports 10-bit I/O addressing and is mapped into the standard PC locations for printer ports. The joystick port is mapped at I/O locations 200 and 201 hex. Alternative maps are jumper selectable.

Parallel I/O - The LPM/MCM-DLPT contains 2 identical, independent, parallel line printer ports on the card. This card can be used directly with DOS programs that expect hardware compatibility with a PC-XT/AT.

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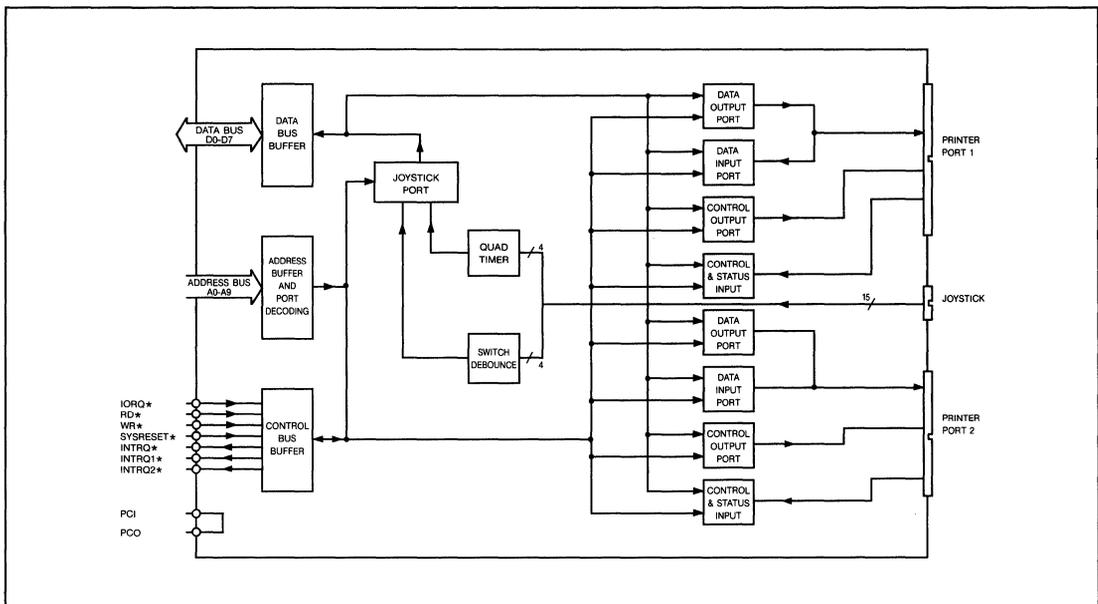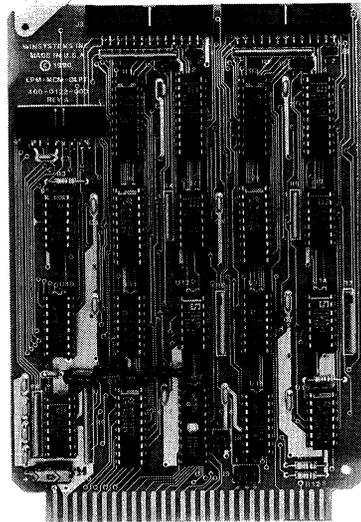
The parallel port is wired as a standard printer port but can be used for other parallel I/O devices for non-DOS embedded systems applications with other I/O maps.

The data port is 8-bits wide and bidirectional. In non-printer applications, data can be written to the port and then read back again to verify proper operation.

The control port sends four different control signals to the printer. These are open collector signals with pull-up resistors. The control input port is used to read back the control signals. The signals are Autofeed, Init, Select, and Strobe.

The status port is input only and provides the printer with different status conditions. Each input has a pull-up resistor to prevent the line from floating. The signals are Error, Acknowledge, Busy, Paper Empty, and Select.

Parallel Port Pinout

Pin	FLOW	Signal
1	OUT	Strobe
2	OUT	Data Bit 0
3	OUT	Data Bit 1
4	OUT	Data Bit 2
5	OUT	Data Bit 3
6	OUT	Data Bit 4
7	OUT	Data Bit 5
8	OUT	Data Bit 6
9	OUT	Data Bit 7
10	IN	Acknowledge
11	IN	Busy
12	IN	Paper Empty
13	OUT	Select
14	OUT	Autofeed
15	I/O	Error
16	OUT	Init. Printer
17	IN	Select Input
18-25		Ground
26	–	Jumper to +5VDC

Printer Interface Connector - Each of the parallel port signal lines are wired to an individual 26-pin right angle connector. Each line is TTL compatible and is capable of sourcing 2.6 mA and sinking 24 mA. The optional WinSystems' CBL-101-3 provides a 3 foot long adapter cable designed to convert a 26-pin ribbon cable to a 25-pin male "D" type connector with strain relief.

Utility Port - A joystick port is also available on the MCM-DLPT. It can also be called the "game port". It

is designed and wired to accept two independent joysticks for use with PC applications programs. The joystick is able to sense movement in two dimensions. Applications programs can read the stick position in the form of X and Y coordinates to follow the movement of the stick. Each joystick support 2 switch closures which are often referred to as "trigger buttons".

For applications not using the joysticks, the 4 button lines can serve as general purpose input lines. Each of these lines has a 1K ohm pull up resistor and a 47 pF capacitor to ground to filter the switch bounce.

Interrupts - An interrupt can be generated by each printer port through the Acknowledge (pin 10) line. The interrupt can be enabled and disabled under program control. They are wired via the INTRQ*, INTRQ1*, or INTRQ2* to the STD Bus backplane.

CMOS STD Bus - The LPM-DLPT is the CMOS STD Bus version of the card for use in very low power and/or extended temperature applications. The MCM-DLPT is designed with standard LS/TTL integrated circuits for use with regular STD Bus systems.

SPECIFICATIONS

Electrical
Bus Interface: STD Bus compatible
Vcc = +5V ±5% @ 250 mA typ. (MCM-DLPT)
         +5V ±10% @ 35 mA typ. (LPM-DLPT)

Mechanical
Dimensions: 4.5" x 6.5"

Connectors
Joystick Port: 16-pin 0.100" grid
Jumpers: 0.025" square posts
Parallel: Two, 26-pin 0.100" grid

Environmental
Operating Temperature: 0° to +70°C (LPM-DLPT)
                          0° to +65°C (MCM-DLPT)
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-DLPT	Dual Parallel I/O card
LPM-DLPT	CMOS Dual Parallel I/O card

WinSystems, Inc.

FEATURES

- Two independent, full duplex, asynchronous, serial communications channels
- RS-232-C or 20 mA opto-isolated current loop levels
- DTE/DCE jumper selectable for each channel
- Processor independent including V50, 80C88, NSC-800, V20, HD64180, CMOS Z80, and 80C85A
- Operation to 8 MHz
- Baud rate jumper selectable from 110 to 9600 bps
- Interrupt on received data
- Jumper selectable I/O addressing
- Available for CMOS STD Bus: LPM-DSIO

The LPM/MCM-DSIO is a dual channel serial card for the STD Bus and CMOS STD Bus. It is populated with 2 universal asynchronous receiver transmitter devices (UARTs) that provide 2 fully independent asynchronous, full duplex, RS-232 and opto-isolated 20 mA current loop channels. The card is I/O mapped and processor independent including the V50, V20, 80C88, NSC-800, HD64180, CMOS Z80, and 80C85A.
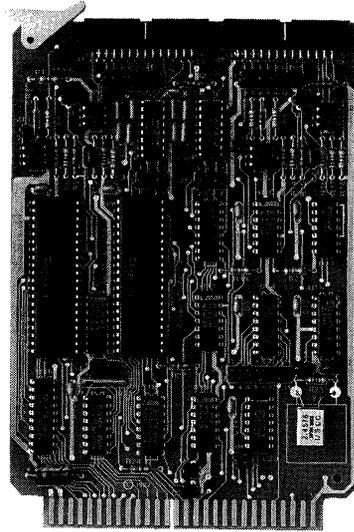
FUNCTIONAL CAPABILITY

Bus Interface - The LPM-DSIO is the CMOS STD Bus versions and the MCM-DSIO is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-DSIO is configured for 8-bit I/O addressing. A total of 4 consecutive I/O addresses are required. It is jumper selectable on any even 4 port boundary above C0h in the I/O map.

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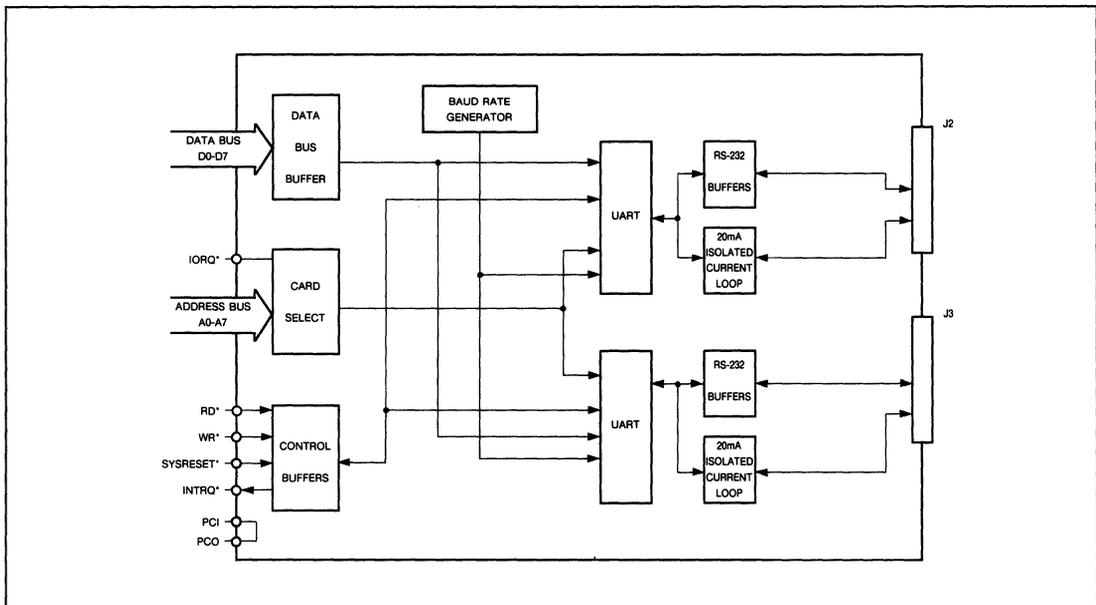
Serial Controller - The LPM/MCM-DSIO card is a fully buffered STD Bus and CMOS STD Bus dual channel serial asynchronous communications board using two UARTs. Each channel is full duplex and both the transmitter and receiver registers are double buffered. The card will work with 5 to 8-bit characters. It will handle 1 or 2 stop bits and false start bit detection. Detection is provided for parity, overrun, and framing errors.

Each LPM/MCM-DSIO contains an independent jumper selectable baud rate generator driven by an on-board crystal oscillator. A total of 8 different frequencies are selectable from 110 through 9600 bps that include all the standard rates (300, 1200, 2400, 4800, etc.) in between for each channel.

Serial Configuration - Each channel has 2 active modem handshake lines in addition to the transmit and receive lines. These lines are RTS and CTS. DTR, DSR, DCD and RI can be tied to a pull-up resistor to generate the correct status indication to a modem requiring these lines. Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation.

Jl and J2 Connector Pinout

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Ground
8	Data Carrier Detect (DCD)
12	20 mA Receive -
13	20 mA Transmit +
20	Data Terminal Ready (DTR)
22	Ring Indicator (RI)
24	20 mA Receive +
25	20 mA Transmit -

Both channels have RS-232-C and 20 mA opto-isolated current loop interface levels. The opto-isolated current loop is ideal for applications that require long distance point to point communication or for applications that require 5 volt operation only. All signals are brought out to a 26-pin male header which allows easy connections to flat cable 25 pin RS-232 "D" type adapter cables.

Interrupts - The LPM/MCM-DSIO can generate an interrupt on receipt of an incoming character. Either or both channels can be jumpered to assert the INTRQ* line on the STD Bus and CMOS STD Bus backplane.

SPECIFICATIONS

Electrical

Serial ports: Two RS-232 and 20 mA opto-isolated channels

$Vcc = +5V \pm 10\%$ at 5mA typ.,
15 mA max.: LPM-DSIO
$Vcc = +5 \pm 5\%$ at 300mA typ.,
465mA max.: MCM-DSIO

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus : 56 pin dual 0.125" centers
Serial I/O: Two 26-pin dual on 0.100" grid

Environmental

Operating Temperature:
LPM-DSIO   -40°C to +85°C
MCM-DSIO   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-DSIO   Dual channel CMOS STD Bus board

MCM-DSIO   Dual channel CMOS STD Bus board

WinSystems, Inc.

FEATURES

- Two independent 82C50A serial channels
- Programmable serial interface characteristics for each channel
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no parity
  - 1, 1½ or 2 stop bits
  - Local loopback for diagnostics
- Independent control of transmit, receive, line status, and data set interrupts on each channel
- RS-232 and RS-485 on both channels with RS-422 levels on channel 1 only
- Asynchronous data rates to 38.4 Kbps
- Software programmable baud rate generator
- Programmable board I/O address selectable for PC-XT/AT hardware/software compatibility
- Frontplane or backplane interrupts supported
- Centronics parallel printer interface onboard mapped as LPT1 or LPT2
- +5 volt only operation
- Available for CMOS STD Bus: LPM-DSPIO
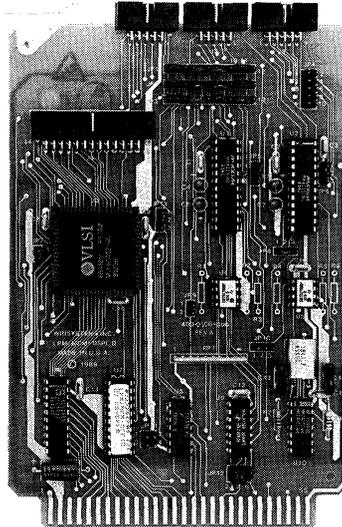
The LPM/MCM-DSPIO is a STD Bus and CMOS STD Bus dual serial 82C50A UART and Centronics parallel I/O card for the STD Bus and CMOS STD Bus based on the VL16C452. It is ideally suited for applications running DOS programs or languages that require exact register compatible hardware for program execution.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-DSPIO is the CMOS STD Bus version and the MCM-DSPIO is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The

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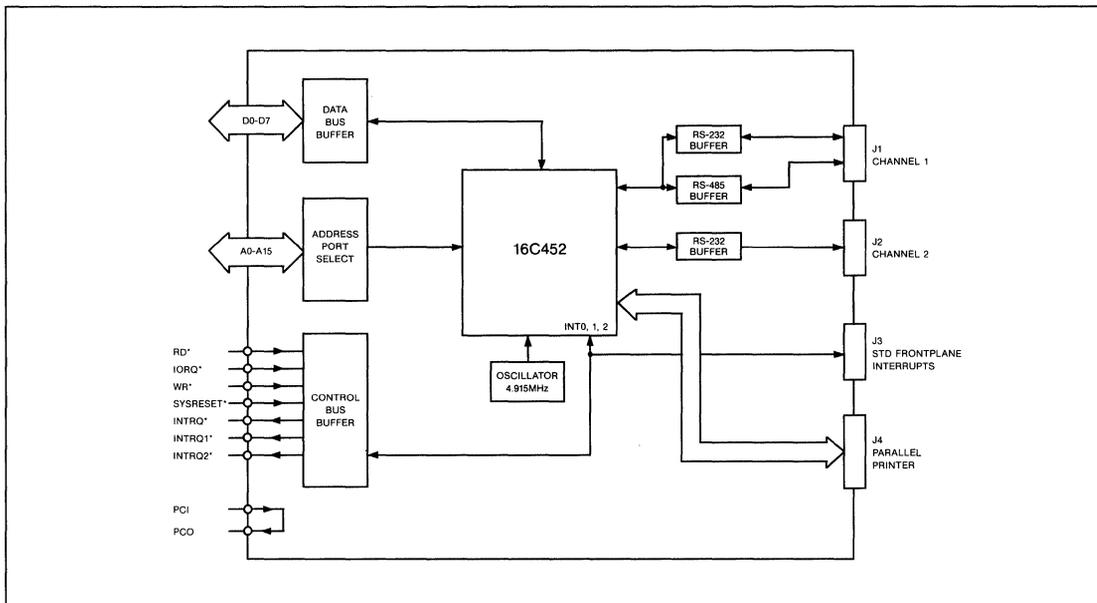
differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Serial I/O - A VLSI technology VL16C452 serves as the serial communication controller. It has two independent, double buffered, serial asynchronous channels that are 82C50A hardware compatible. The unit contains on-chip software programmable baud rate generators selectable through 38.4K bits per second. Each has independent control of transmit, receive, line status and data set interrupts. Individual modem handshake control signals are available for each line.

Each channel will support 5-, 6-, 7-, or 8-bit characters with even, odd or no parity generation/checking. It will handle 1, 1½ or 2 stop bits. Each channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream.

The standard serial I/O map is COM1 and COM2 (3F8-3FF hex and 2F8-2FF hex respectively) for PC compatibility. Alternative maps are jumper selectable.

Both channels support RS-232 and RS-485 electrical interface levels. Channel 1 will also support RS-422 if Channel 2 is jumpered for RS-232. Only +5 volts is required for the system since a Maxim MAX239 chip is used which generates the plus and minus voltages required for RS-232. Higher RS-232 (+10 volt) levels can be obtained by optionally jumpering +12V to the MAX239. This is occasionally required for long cable runs or for certain mouse interfaces.

The RS-422 configuration provides separate balanced transmit and receive signal pairs. For RS-485 multi-drop lines, only one signal pair is used for "party line" network structures. The LPM/MCM-DSPIO is designed to properly disable the transmitter upon reset to prevent potential lock-up problems caused by a transmitter stuck in the ON mode. Both the RS-422/485 transmitter and receiver have 100 ohm termination resistors installed onboard for impedance matching.

Certain PC-compatible BIOS' and communications applications software (i.e. Greenleaf, etc.) will not permit data transmission until the modem input status lines are set to the correct logic levels. The LPM/MCM-DSPIO has an onboard jumper header to permit the user to force the correct binary state for the control interchange circuits.

Both serial channels are configured as a DTE and each wired to an individual 10-pin right angle connector like the PC-AT. This permits easy connections to a standard 9-pin male D-sub connector with the WinSystems' CBL-123-1.

Parallel I/O - The VL16C452 also provides a direct 26-pin Centronics parallel I/O interface from the LPM/MCM-DSPIO. The standard default I/O Map is LPT1 (378-37F hex) with a jumper selectable option or LPT2 (278-27F hex).

The parallel port is wired as a printer port but can be used for other devices. The first 8-bits are available as input or output only. The additional handshake lines are dedicated 5-bits as input only and 4-bits as output only.

Interrupts - Interrupts are generated on error conditions or receive/transmit buffer status for the serial I/O and from the parallel I/O. They can be wired via the INTRQ*, INTRQ1*, and INTRQ2* on the STD Bus and CMOS STD Bus backplane or via the frontplane convention.

SPECIFICATIONS

Electrical

Vcc = +5V ±10% at 170mA typ.,
    +12V ±10% at 20mA (optional): LPM-DSPIO
Vcc = +5V ±5% at 270mA typ.,
    +12V ±5% at 20mA (optional): MCM-DSPIO

Mechanical
Meets STD Bus mechanical specifications

Connectors
Interrupts: 10-pin 0.100" grid
Parallel: 26-pin 0.100" grid
Serial: Two 10-pin 0.100" grid

Environmental
Operating Temperature: 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-DSPIO   Dual Serial/Parallel I/O card
MCM-DSPIO   Dual Serial/Parallel I/O card
CBL-101-3   26-pin ribbon to 25-pin "D" adapter
CBL-123-1   10-pin ribbon to 9-pin "D" adapter

WinSystems, Inc.

FEATURES

- Four independent 8-bit I/O ports with 2 handshake lines per port
- Programmable In only, Out only or Bidirectional I/O
- Output data buffers selectable to provide inverted or non-inverted drive capability
- Two 8-bit ports capable of true Bidirectional I/O
- Jumper options for inverted or non-inverted handshake
- All I/O lines fully buffered
- I/O lines directly TTL compatible with provisions for termination resistor networks
- Interrupt driven data transfer
- Supports Z80 mode 2 vectored interrupts
- Available for CMOS STD Bus: LPM-PIO
- + 5 volt only operation

The LPM/MCM-PIO is a highly versatile, 32 line parallel input/output controller designed to provide a variety of methods of I/O between a processor and peripherals. The card uses two Z80-PIOs which are software programmable and has four operating modes: Byte Input, Byte Output, Bidirectional and Bit Input/Output. The data lines have socketed buffers which can be replaced to obtain complementary signal polarity. Additionally, each port has Z80 mode 2 vectored interrupts.
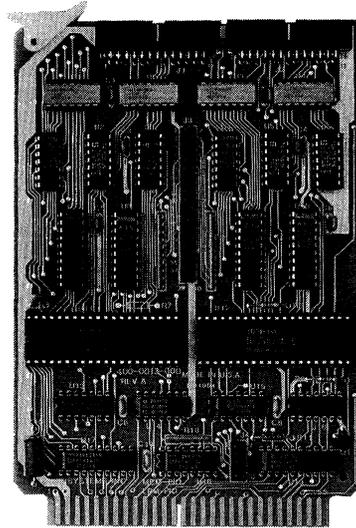
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-PIO is the CMOS STD Bus version and the MCM-PIO is the STD Bus version of this card. The LPM/MCM prefix indicates the card
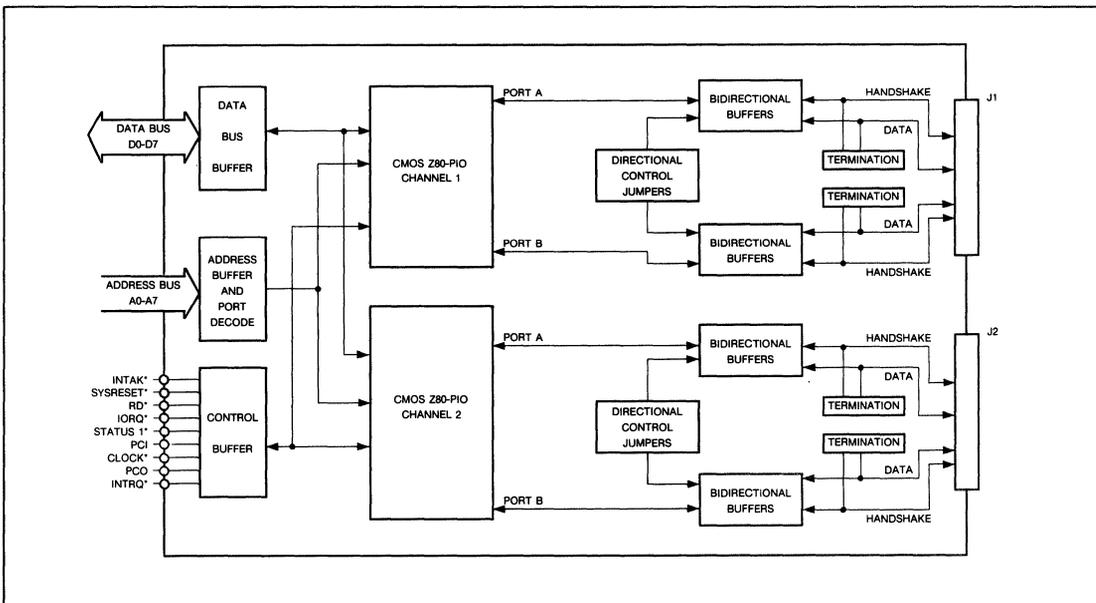
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has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-PIO is configured for 8-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8 port boundary.

Port Controller - Two multifunction CMOS Z80-PIO devices provide a total of four independent 8-bit I/O ports with two transfer control lines per port. Each PIO has an I/O port pair designated A and B with similar interface circuitry. Each port consists of eight data lines plus two handshake lines. All port lines are brought to two 26-pin connectors; two ports per connector.

Data Bus Buffers - The data bus lines are buffered by non-inverting transceivers. The PIO and buffers are programmable to provide 4 distinct modes: Input, Output, Bidirectional (Port A only), and Control. The I/O buffers are configured such that port direction can be selected in 4-bit nibbles. The transceivers are mounted in sockets so that they can be easily replaced with their complements in order to achieve a polarity change if required.

Handshaking - The LPM/MCM-PIO provides independent jumper programmable handshake signals to control the data transfer between the PIO and peripheral device. Each port contains two buffered handshake signals, Ready and Strobe, that are automatically generated in all of the data transfer modes.

Termination - One 14-pin socket is provided per port for resistor dual in line packages so that termination networks may be placed on the data lines. A parallel termination is provided for each data line plus the input Strobe (STB) handshake line. Removable passive terminations allow substitution of alternative networks.

Interrupts - The LPM/MCM-PIO is unique in that all data transfers in all 4 modes are accomplished under total interrupt control. Also it can be programmed to interrupt the CPU on the occurance of specified status conditions in the peripheral device. Z80 mode 2 vectored interrupts are generated for fast system response.

SPECIFICATIONS

Electrical

System Clock: 4 MHz standard; 6 and 8MHz optional

Parallel Interface: 4 TTL compatible I/O ports
Input ports: One 74LS Load Max.

Output ports:
LPM-PIO-4 I_{OH} = -6mA max. at 3.84 V

I_{OL} = 6mA max. at .33V

MCM-PIO-4 I_{OH} = -3mA max. at 2.4 V

I_{OL} = 24mA max. at .5V

Vcc = +5V $\pm$ 10% at 40mA typ.: LPM-PIO
Vcc = +5V $\pm$ 5% at 850mA typ.: MCM-PIO

Mechanical

Meets STD Bus mechanical specifications

Connectors

Jumpers: 0.025″ square posts
Parallel I/O: Two 26 pin on 0.100″ grid

Environmental

Operating Temperature:
    LPM-PIO   -40° to +85°C
    MCM-PIO   0° to +65°C

Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-PIO-4   CMOS STD Bus 32 Channel Programmable Parallel I/O card with manual
LPM-PIO-6   6 MHz version of the LPM-PIO-4
LPM-PIO-8   8 MHz version of the LPM-PIO-4

MCM-PIO-4   STD Bus 32 Channel Programmable Parallel I/O card with manual
MCM-PIO-6   6 MHz version of the MCM-PIO-4
MCM-PIO-8   8 MHz version of the MCM-PIO-4

WinSystems, Inc.

WinSystems®

STD BUS, CMOS STD BUS

LPM-PIO2
MCM-PIO2
64 Line I/O Card

FEATURES

- Four 8-bit input and four 8-bit output TTL level I/O ports
- Outputs can sink 6 mA
- Pull-up resistors on all input ports
- Processor independent including V50, 80C88, NSC-800, V20, HD64180, CMOS Z80, and 80C85A
- Operation to 8 MHz
- Easy to use with no complicated peripheral chip initialization routines required
- Jumper selectable I/O addressing
- Single +5 Volt operation
- Available for CMOS STD Bus: LPM-PIO2

The LPM/MCM-PIO2 provides 32 gated input lines and 32 latched output lines between a STD Bus and CMOS STD Bus system and peripheral devices. It is configured as four 8-bit input ports and four 8-bit output ports. The card is I/O mapped and processor independent including the V50, 80C88, NSC-800, HD64180, CMOS Z80, and 80C85A.

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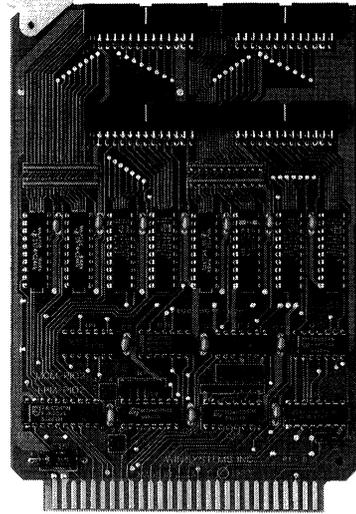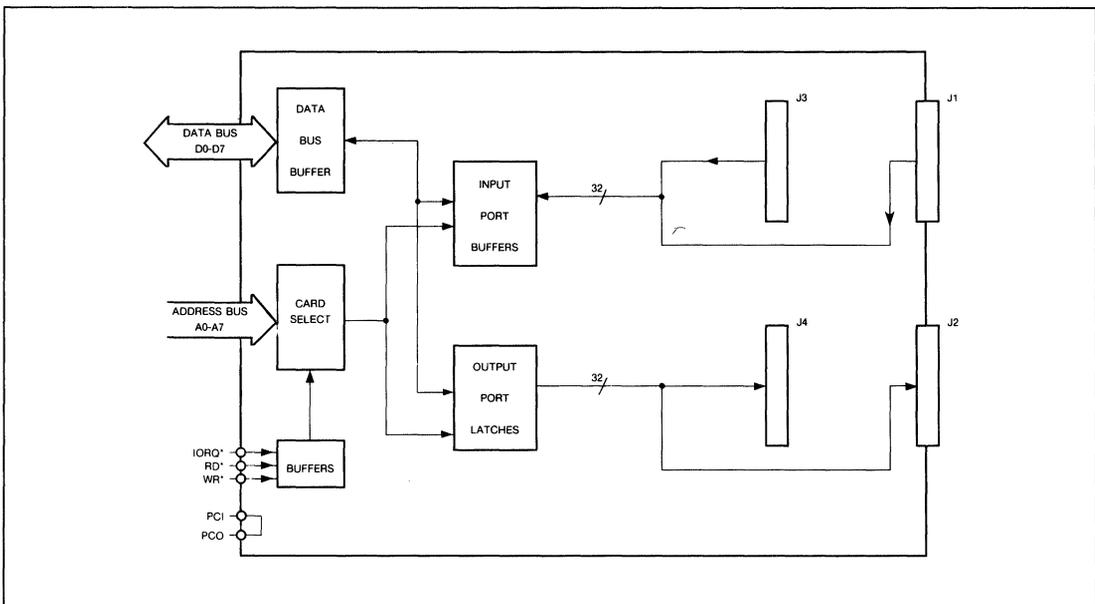
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-PIO2 is the CMOS STD Bus version and the MCM-PIO2 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-PIO2 is configured for 8 or 10-bit I/O addressing. A total of 4 consecutive I/O addresses are required and it is selectable on any even 4 port boundary. Address lines A0 and A1 select one of four sequential ports. A2 through A9 selects the card by a jumper selectable decoded combination.

Configuration - The LPM/MCM-PIO2 is a STD Bus and CMOS STD Bus compatible parallel input/output card with a total of 64 I/O lines. These I/O lines are organized as four 8-bit input ports and four 8-bit output ports.

The I/O ports are accessed through four 26-pin right angle connectors located at the top of the board. These connectors are more reliable and less likely to disconnect than DIP type connectors.

Each connector has a total of 16 I/O lines that are organized as either two 8-bit input port or two 8-bit output ports. Each connector has dedicated lines for +5 VDC and ground for use by external peripheral devices.

The LPM/MCM-PIO2 is very easy to use. No complicated peripheral chip initialization routines are required to access the board.

Input Ports - Each input line is equipped with a pull-up resistor to assure that unconnected lines do not float. Each input line of the MCM-PIO2 is connected to a 74LS244 type data bus buffer with 0.4 volts of hysteresis. The LPM-PIO2's input line is connected to a 74HC244 type data bus buffer.

Output Ports - The output data is latched into a data bus buffer and connected to the output connector. Additionally, the outputs on the MCM-PIO2 can drive 17 LSTTL loads and the LPM-PIO2 will drive 4 LSTTL or 20 CMOS loads.

SPECIFICATIONS

Electrical

Output ports:

LPM-PIO2 I_{OH} = -6mA max. at 3.84 V

I_{OL} = 6mA max. at .33V

MCM-PIO2 I_{OH} = -3mA max. at 2.4 V

I_{OL} = 24mA max. at .5V

V_{cc} = +5V $\pm$ 10% at 20mA typ.,
        35mA max.: LPM-PIO2
V_{cc} = +5V $\pm$ 5% at 450mA typ.,
        650mA max.: MCM-PIO2

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125″ centers

Parallel I/O: Four 26-pin dual on 0.100″ grid

Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-PIO2   -40° to +85°C
    MCM-PIO2   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-PIO2   32 channel input, 32 channel output parallel CMOS I/O board
MCM-PIO2   32 channel input, 32 channel output parallel I/O board

WinSystems, Inc.

FEATURES

- Two independent, full-duplex serial channels
- Supports asynchronous and synchronous (Bisync, SDLC, HDLC, and CCIT-X.25) protocols
- Selectable RS-232-C and RS-422/485 or opto-isolated 20mA current loop interface levels
- Asynchronous data rates 50 to 19.2K bps
- Synchronous data rates to 307.2 Kbps
- Configurable as DTE or DCE interface with modem controls
- Independent programmable baud rate clocks
- Generates Z80 mode 2 interrupts
- Uses the Z80-SIO/2 controller

The LPM/MCM-SIO2 is a STD Bus and CMOS STD-Z80 Bus compatible, dual channel, serial input/output board, designed to be a multiprotocol asynchronous or synchronous serial communications board. Both RS-232-C and RS-422/485 or 20 mA current loop interface levels are available.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-SIO2 is the CMOS STD Bus version and the MCM-SIO2 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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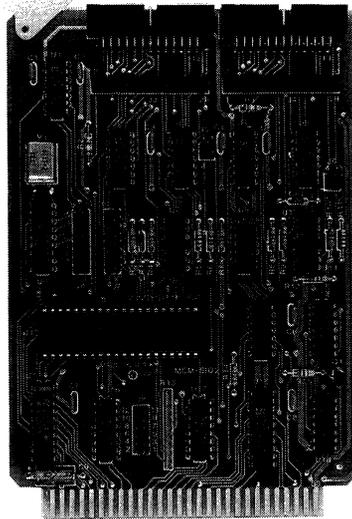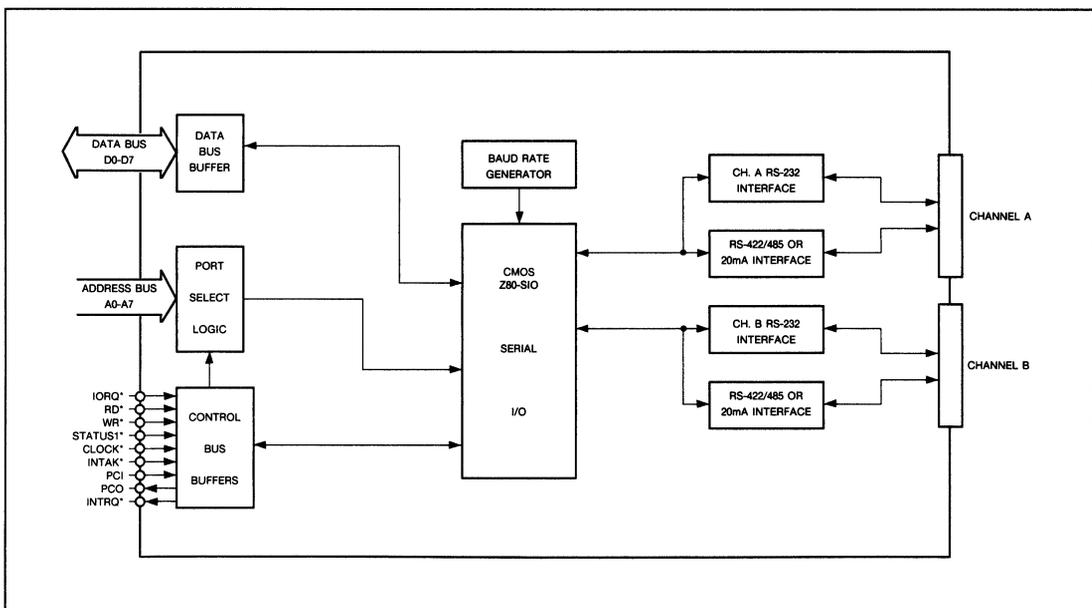
Addressing - The LPM/MCM-SIO2 is configured for 8-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8 port boundary.

Serial Controller - The LPM/MCM-SIO2 is a full duplex, 2 channel serial controller based on the Z80-SIO/2. The LPM/MCM-SIO2's transmitter registers are doubly buffered and the receiver registers are quadruply buffered. Each channel has an independent, jumper programmable, on-board crystal controlled, baud rate generator capable of synchronous rates to 307.2 Kbps and asynchronous rates to 19.2 Kbps.

In the asynchronous mode, the card will work with 5 to 8-bit characters. It will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing.

In synchronous mode, the Z80-SIO/2 will support BiSysnc, SDLC, and HDLC including CRC generation, sync character insertion/deletion and many other protocol dependent features. Synchronous transmitter and receiver clocks can be generated from on or off-board.

Serial Configuration - Each channel has 5 modem handshake lines and 2 clock lines in addition to the transmit and receive lines. These lines are RTS, CTS, DTR, DSR, DCD, and RCLK (DA and DD). Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation.

All signals are RS-232-C levels. Also either RS-422/485 (LPM/MCM-SIO2A) or 20 mA opto-isolated current loop (LPM/MCM-SIO2) levels are available on both channels. Each channel's signals are wired to a 26-pin male header on the card edge which allows easy connections to a flat cable 25-pin "D" type adapter cable. WinSystems offers both male and female type "D" to 26-pin ribbon cables designated CBL-101-3 and CBL-102-3.

SPECIFICATIONS

Electrical

System Clock: 4.0MHz standard, 6 or 8MHz optional

Interrupts: STD-Z80 (and HD64180) compatible with mode 2 interrupts

Serial Interface

LPM/MCM-SIO2: RS-232 on TxD, RxD, CTS, RTS, DTR, and DCD; 20 mA on TxD and RxD (opto-isolated)

LPM/MCM-SIO2A: RS-232 on TxD, RxD, CTS, RTS, DTR, and DCD; RS-422/485 on TxD and RxD

Power:

| LPM-SIO2	LPM-SIO2A
+5 VDC ± 10% at 85 mA	+5 VDC ± 10% at 325 mA
+12 VDC ± 10% at 5 mA	+12 VDC ± 10% at 5 mA
- 12 VDC ± 10% at 5 mA	- 12 VDC ± 10% at 5 mA

MCM-SIO2	MCM-SIO2A
+5 VDC ± 5% at 500 mA	+5 VDC ± 5% at 740 mA
+12 VDC ± 5% at 50 mA	+12 VDC ± 5% at 50 mA
- 12 VDC ± 5% at 50 mA	- 12 VDC ± 5% at 50 mA

Mechanical

Meets STD Bus mechanical specifications

Connectors

Serial I/O: Two 26-pin dual on 0.100″ grid
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-SIO2, LPM-SIO2A   -40° to +85°C
    MCM-SIO2, MCM-SIO2A   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SIO2-4	4.0 MHz Dual Serial RS-232 and 20 mA I/O board
LPM-SIO2-6	6.0 MHz version of the LPM-SIO2-4
LPM-SIO2-8	8.0 MHz version of the LPM-SIO2-4
LPM-SIO2A-4	4.0 MHz Dual Serial RS-232 and RS-422/485 I/O board
LPM-SIO2A-6	6.0 MHz version of the LPM-SIO2A-4
LPM-SIO2A-8	8.0 MHz version of the LPM-SIO2A-4
MCM-SIO2-4	4.0 MHz Dual Serial RS-232 and 20 mA I/O board
MCM-SIO2-6	6.0 MHz version of the MCM-SIO2-4
MCM-SIO2-8	8.0 MHz version of the MCM-SIO2-4
MCM-SIO2A-4	4.0 MHz Dual Serial RS-232 and RS-422/485 I/O board
MCM-SIO2A-6	6.0 MHz version of the MCM-SIO2A-4
MCM-SIO2A-8	8.0 MHz version of the MCM-SIO2A-4

WinSystems, Inc.

FEATURES

- Four independent, full duplex, asynchronous, serial communications channels
- 80C85, 80C88, 80188, V40 and V53 compatible
- Programmable baud rates from 50 to 38.4Kbps
- RS-232 or RS-422 interface levels
- DTE/DCE jumper selectable
- Programmable loopback diagnostic capability
- On board 82C59A progammable interrupt controller
- Supports cascade interrupts on the backplane or front plane for STD-8088 processor cards
- IOEXP supported
- Wait State Generator
- Available for CMOS STD Bus: LPM-SIO4

The LPM/MCM-SIO4 is a powerful, compact STD Bus and CMOS STD Bus four channel UART card offering a high degree of noise immunity, low power consumption, and a wide temperature range. The LPM/MCM-SIO4, populated with four 82C52s, provides 4 fully independent, asynchronous, full duplex, RS-232 and RS-422 serial data channels. Each channel is configurable as either DTE or DCE depending on the specific application.

An onboard 82C59A interrupt controller generates prioritized vectored interrupts for 80C85, 80C88, and 80188 processor cards.
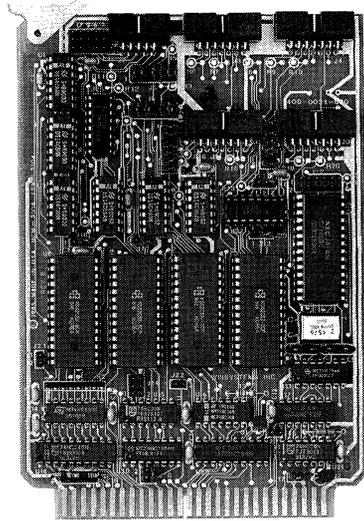
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-SIO4 is the CMOS STD Bus version and the MCM-SIO4 is the STD Bus version of this card. The LPM/MCM prefix indicates the card
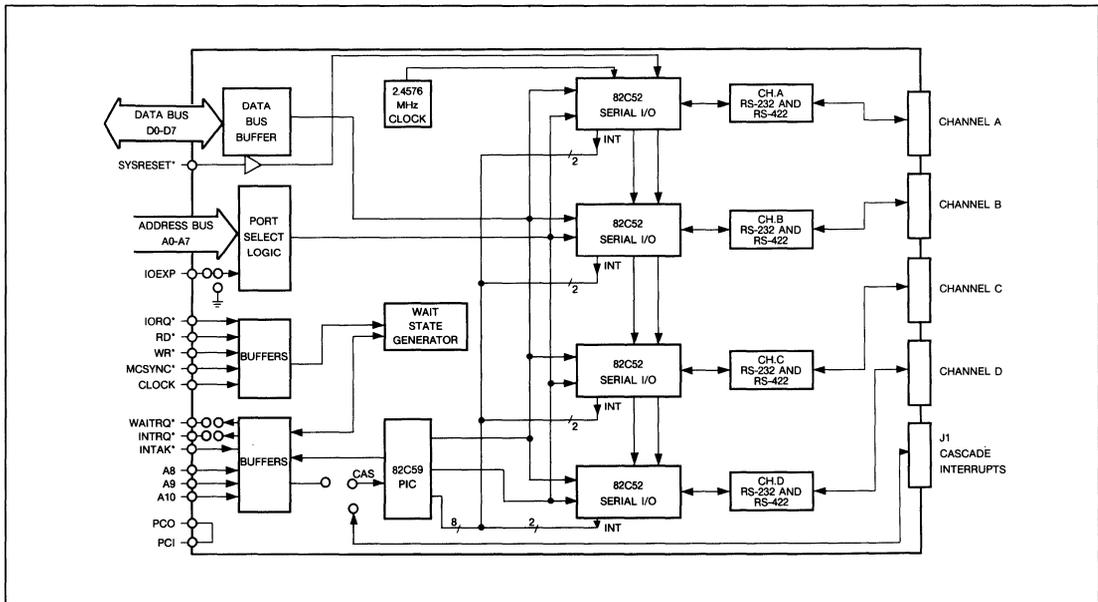
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has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Serial Controller - The LPM/MCM-SIO4 card is a fully buffered STD Bus and CMOS STD Bus four channel serial asynchronous communications board. Each channel is full duplex and both the transmitter and receiver are double buffered. The card will work with 5 to 8-bit characters. It will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Error detection is provided for parity, overrun, and framing. Each channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream.

Each 82C52 contains an independent on-chip programmable baud rate generator driven by a master crystal oscillator. A total of 18 different frequencies are software selectable for each channel. They are 50 through 38.4K bits per second and include all the standard rates (300, 1200, 2400, 4800, etc.) in between.

Serial Configuration - Each channel has 4 modem handshake lines in addition to the transmit and receive lines. These lines are RTS, CTS, DTR, and DSR. Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation. All 4 channels are RS-232 and RS-422 interface levels. Each channel's signals are brought out to a 14-pin male header which allows easy connections to flat cable 25-pin RS-232 "D" type adapter cables.

The LPM/MCM-SIO4 can be depopulated with fewer serial channels if required. Contact the factory for details.

Serial I/O Channels A - D

Pin	Signal
1, 7	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
14	RS422 Transmit Data +
15	RS422 Transmit Data -
16	RS422 Receive Data +
17	RS422 Receive Data -
20	Data Terminal Ready (DTR)

Interrupts - An on-board 82C59A PIC provides vectored interrupts for either 80C85 and 80C88 CPUs. The parallel interrupt priority scheme is implemented on the front plane of the card via a 10-pin right angle connector for processor independent operations. Alternatively when operating as a slave, the LPM/MCM-SIO4 supports the STD-8088 cascade interrupt priority scheme over the frontplane or backplane.

I/O - IOEXP is supported and can be configured in two ways. It can be jumpered to ground or be enabled with an active low. This board requires 16 I/O port addresses and is jumper selectable on any 16 port boundary.

SPECIFICATIONS

Electrical

Serial Interface: RS-232 and RS422 on all Channels.
LPM-SIO4:
Vcc = +5V $\pm$ 10% at 75mA typ.
$\qquad$ $\pm$ 12V $\pm$ 10% at 5mA typ.
Without RS-422 Drivers
Vcc = +5V $\pm$ 10% at 35mA typ., 25mA max.
$\qquad$ = $\pm$12V $\pm$ 10% at 60mA typ.
MCM-SIO4:
Vcc = +5V $\pm$ 5% at 310mA typ.
$\qquad$ $\pm$ 12V $\pm$ 10% at 60mA typ.
Without RS-422 Drivers
Vcc = +5V $\pm$ 5% at 270mA typ.,
$\qquad$ = $\pm$12V $\pm$ 10% at 60mA typ.

Mechanical

Meets STD Bus mechanical specifications

Connectors

Jumpers: 0.025" square posts
Serial I/O: Four, 14-pin on 0.100" grid
Interrupt: 10-pin 0.100" grid

Environmental

Operating Temperature:
$\qquad$ LPM-SIO4 $\qquad$ -40° to +85°C
$\qquad$ MCM-SIO4 $\qquad$ 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

|	
LPM-SIO4	CMOS STD Bus four channel board
MCM-SIO4	STD Bus four channel board
CBL-105-3	3-ft. ribbon cable, 14-pin ribbon to 25-pin male "D" type connector
CBL-106-3	3-ft. ribbon cable, 14-pin ribbon to 25-pin female "D" type connector

WinSystems, Inc.

FEATURES

- Two independent, full duplex, asynchronous, serial communications channels
- RS-232 or 20 mA opto-isolated current loop levels
- DTE/DCE jumper selectable for each channel
- Baud rate jumper selectable from 110 to 9600 bps
- Interrupt on received data
- Two input and two output TTL I/O ports
- One 8-bit input port
- One 8-bit output port
- Two combination ports with 4-bits input and 4-bits output
- Outputs can sink 6 mA
- Pull-up resistors on all input ports
- Processor independent including V50, 80C88, NSC-800, V20, HD64180, CMOS Z80, and 80C85A
- Operation to 8 MHz
- Jumper selectable I/O addressing
- Available for CMOS STD Bus: LPM-SPIO
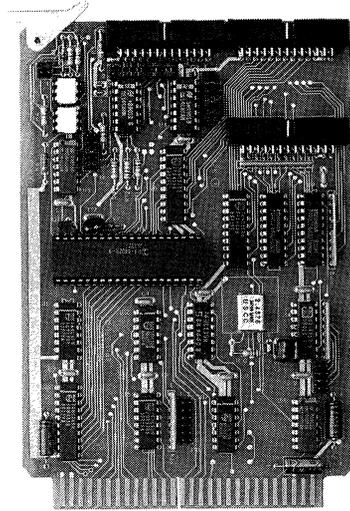
The LPM/MCM-SPIO is serial and parallel input/output card. A UART provides an asynchronous, full duplex, RS-232 and 20 mA current loop serial channel. Also one parallel 8-bit input port, one 8-bit output port, and two ports each with 4 input bits and 4 output bits are provided. The card is I/O mapped and processor independent.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-SPIO is the CMOS STD Bus version and the MCM-SPIO is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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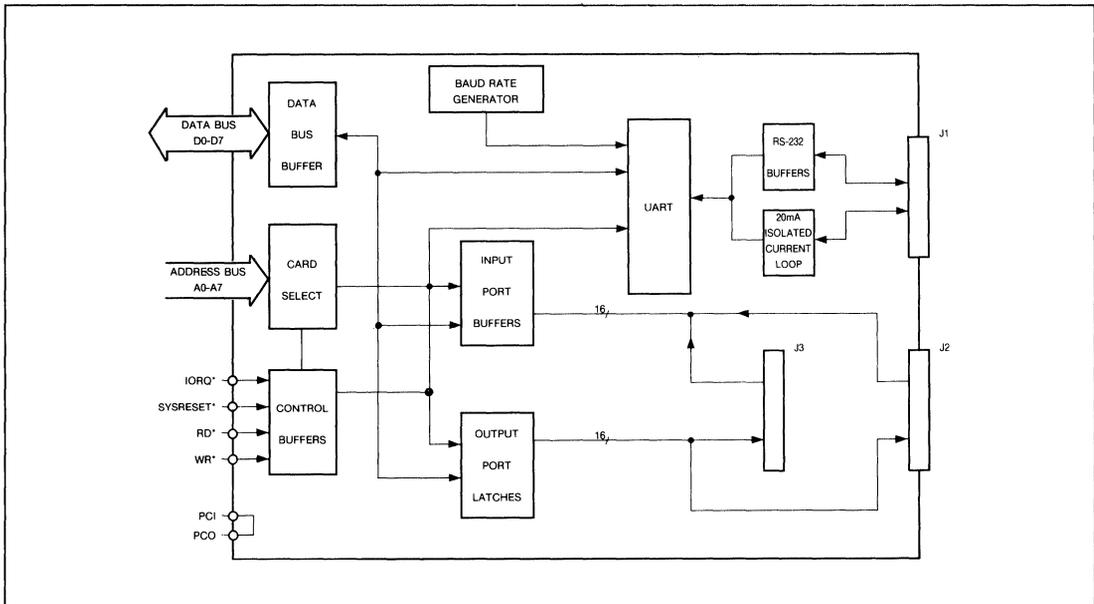
Addressing - The LPM/MCM-SPIO is configured for 8-bit I/O addressing. A total of 4 consecutive I/O addresses are required and it is jumper selectable on any even 4 port boundary.

Parallel Configuration - The LPM/MCM-SPIO has a total of 32 parallel I/O lines organized as one 8-bit input port, one 8-bit output port, and two combination ports each with four bits input and four bits output.

The I/O ports are accessed through two 26-pin right angle connectors located at the top of the board. Each connector has a total of 16 I/O lines. Each connector has dedicated lines for +5 VDC and ground for use by external peripheral devices.

The LPM/MCM-SPIO is very easy to use. No complicated peripheral chip initialization routines are required to access the board.

Input Ports - Each input line is equipped with a full-up resistor to assure that unconnected lines do not float. Each input line of the MCM-SPIO is connected to a 74LS244 type data bus buffer with 0.4 volts of hysteresis. The LPM-SPIO's input line is connected to a 74HC244 type data bus buffer.

Output Ports - The output data is latched into a data bus buffer and connected to the output connector. Additionally, the outputs on the MCM-SPIO can drive 17 LSTTL loads and the LPM-SPIO will drive 4 LSTTL or 20 CMOS loads.

Serial Controller - The LPM/MCM-SPIO card has a fully buffered serial asynchronous communications channel. The channel is full duplex and both the transmitter and receiver registers are double buffered. The card will work with 5 to 8-bit characters. It will handle 1 or 2 stop bits and false start bit detection. Detection is provided for parity, overrun, and framing errors.

The LPM/MCM-SPIO contains an independent jumper selectable baud rate generator driven by an on-board crystal oscillator. A total of 8 different frequencies are selectable from 110 through 9600 bps that include all the standard rates (300, 1200, 2400, 4800, etc.) in between.

Serial Configuration - The serial channel has 2 active modem handshake lines in addition to the transmit and receive lines. These lines are RTS and CTS. DTR, DSR, DCD and RI can be tied to a pull-up resistor to generate the correct status indica-

tion to a modem requiring these lines. Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation.

RS-232-C and 20 mA opto-isolated current loop interface levels are available. The opto-isolated current loop is ideal for applications that require long distance point to point communications or for applications that require 5 volt operation only. All signals are brought out to a 26-pin male header which allows easy connections to flat cable 25-pin RS-232 "D" type adapter cables.

Interrupts - The LPM/MCM-SPIO can generate an interrupt on receipt of an incoming serial character by asserting the INTRQ* line on the STD Bus backplane.

SPECIFICATIONS

Electrical
All STD Bus and CMOS STD Bus processors with I/O mapping

I/O

LPM-SPIO	I_{OH} = -6mA max. at 3.84V
	I_{OL} = 6mA max. at .33V
MCM-SPIO	I_{OH} = -3mA max. at 2.4V
	I_{OL} = 24mA max. at .5V

LPM-SPIO:
Vcc = +5V $\pm$ 10% at 15mA typ., 35mA max.
$\pm$ 12V $\pm$ 10% at 3mA typ., 7mA max.
MCM-SPIO:
Vcc = +5V $\pm$ 5% at 450mA typ., 650mA max.
$\pm$ 12V $\pm$ 10% at 25mA typ., 37mA max.

Mechanical
Meets STD Bus mechanical specifications

Connectors
STD Bus: 56-pin dual 0.125" centers
I/O: Three 26-pin dual on 0.100" grid

Environmental
Operating Temperature:
    LPM-SPIO   -40° to +85°C
    MCM-SPIO   0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SPIO   CMOS STD Bus Serial/Parallel I/O Card
MCM-SPIO   STD Bus Serial/Parallel I/O Card

WinSystems, Inc.

Analog I/O Selection Guide

PRODUCT	Bus INTERFACE	RESOLUTION (BITS)	A/D CHANNELS	D/A CHANNELS
MCM-1260	STD Bus	12	16 SE or 8 DI	—
LPM-1280	CMOS STD Bus	12	—	4 or 8
LPM-7109	CMOS STD Bus	12 (Plus Sign)	16 SE	—
MCM-7109	STD Bus			
MCM-7418	CMOS STD and STD Bus	16	8 DI	—
MCM-7419	CMOS STD and STD Bus	16	16 DI	—
LPM-A/D12	CMOS STD Bus	12	16 SE or 8 DI	—
MCM-A/D12	STD Bus			
LPM-AIO	CMOS STD Bus	12	32 SE	2
MCM-AIO	STD Bus			
LPM-AIO-8	CMOS STD Bus	12	8, 16, or 32 SE	—
MCM-AIO-8	STD Bus			
LPM-D/A12	CMOS STD Bus	12	—	4 or 8
MCM-D/A12	STD Bus			
LPM-D/A8	CMOS STD Bus	8	—	8
MCM-D/A8	STD Bus			
SBX-A/D12	SBX Bus	12	8 SE or 4 DI	—
SBX-D/A12	SBX Bus	12	—	2

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WinSystems®

STD BUS, CMOS STD BUS

LPM-7109
MCM-7109
Integrating A/D Card

FEATURES

- Low Cost
- 12-bit plus sign integrating A/D
- Up to 16 single ended input channels
- Input ranges: $\pm$ 5V
- All input channels protected to $\pm$ 35V
- Jumper selectable onboard test points for system status check
- Up to 30 conversions per second
- I/O mapped, processor independent including 80486/386/286, 80188, 8088, V53, V40, V20, Z80, 8085, and 64180
- Interrupt-on-Conversion complete
- Optional Analog Adapter panel for field wiring termination, 4-20 mA, and signal conditioning
- Supports STD and CMOS STD Bus
- Low power
- Extended temperature range
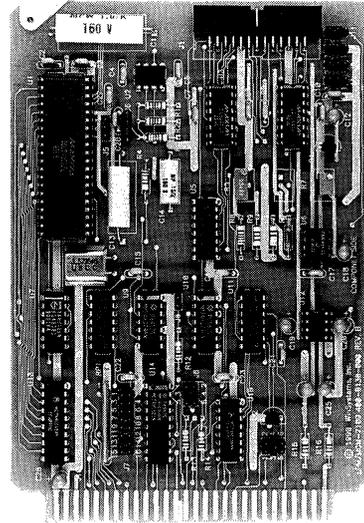
The LPM/MCM-7109 is a low cost, 12-bit (plus sign) integrating A/D converter for use in data acquisition and control applications. A dual slope integrating converter provides the benefits of high frequency noise reduction through signal averaging while offering a rate of up to 30 conversions per second. The polarity bit is also used to provide a relative accuracy of 1 in 8190.

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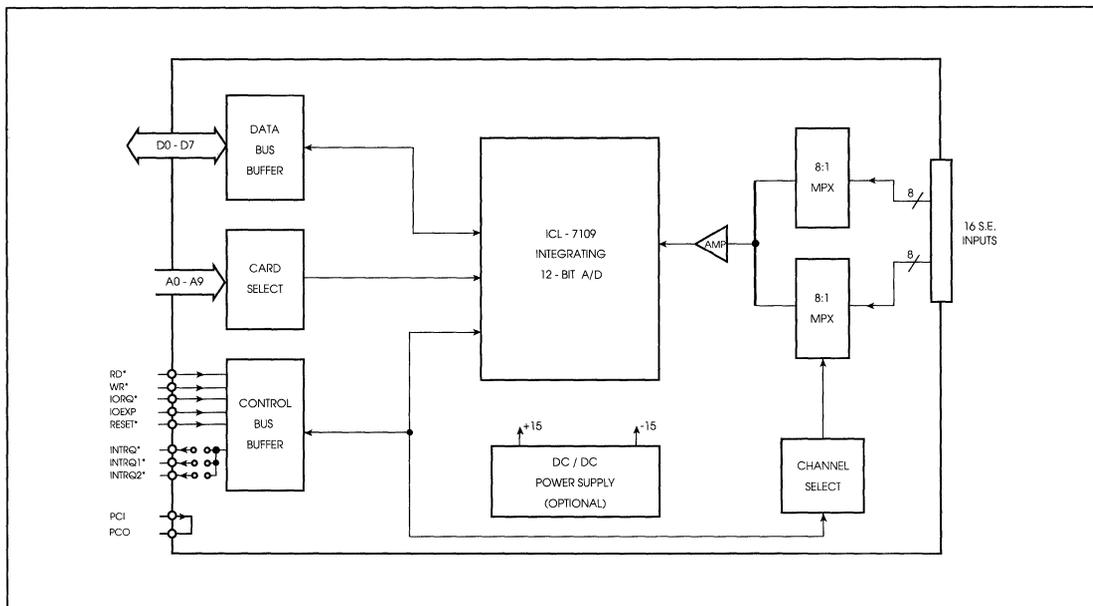
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7109 is the CMOS STD Bus version and the MCM-7109 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature range.

Multiplexer - The LPM/MCM-7109 card contains two, 8 channel fault-protected MAX358 CMOS Analog Multiplexers with overvoltage protection. They can withstand continuous analog input voltages of $\pm$ 35V which eliminates the possibility of damage when the power supplies are turned off. Also, they can withstand brief input transient spikes which would otherwise require complex external protection networks.

Analog to Digital Converter - The LPM/MCM-7109 card contains the monolithic ICL7109 12-bit A/D converter. It provides 12-bits of binary data plus polarity and overrange outputs. It is a dual slope integrating converter which offers high accuracy with high frequency noise rejection and averaging of changes that occur during the sampling period.

The A/D input is biased such that when the single ended input signal is converted, the combination of the 12 data bits with the sign bit will give an effective resolution of 8190 counts (rather than 4096 for a standard 12-bit A/D) for even greater accuracy.

$\pm$5V single ended inputs are accepted on any of the 16 channels. For 4-20 mA sensors, close tolerance 250 ohm termination resistors can be installed on the Analog-ADP termination panel. A directly proportional +1 to +5 volt signal will be generated across the shunting resistor.

Jumper Test Points - Four of the analog inputs can be dedicated to measure specific onboard analog voltages for remote self-testing purposes. These points are jumper selectable at the time the board is installed in the card cage. Input 1 is for onboard temperature. Input 2 is from the calibrated reference voltage to the ICL7109 A/D chip. Input 3 is the system's lithium battery voltage measured from pin 5 of the STD Bus backplane. And input 4 is the system's +5V DC power measured from pins 1 and 2 of the STD Bus.

Interrupts - Conversion is begun each time the channel number is written to the board. An end-of-conversion generates an interrupt which can be jumpered to one of 3 interrupt pins on the STD Bus.

Input Configuration - The analog input channels are wired to a 26-pin, pin-and-socket header connector. Either flat ribbon or discreet wires can be mated to the connectors. The pinout is compatible with WinSystems' Analog-ADP termination board.

Field Wiring - The Analog-ADP termination board is available for terminating field wiring. This is a non-isolated signal conditioning panel for use with WinSystems' STD Bus A/D converter cards. It provides a multitude of termination options including signal protection for the analog input signals plus serves as a field wiring to ribbon cable adapter. The LPM/MCM-7109 and Analog-ADP are connected by the CBL-130-3, 26-pin ribbon cable connector.

SPECIFICATIONS

Electrical
Number of channels: 16 single ended
Input overvoltage: $\pm$ 35V
Input range: $\pm$ 5V
Resolution: 12 bits plus sign
Conversion time: Up to 30 conversions per sec.

Power Requirements:
LPM-7109: $\pm$ 12VDC $\pm$ 10% @30mA
            +5.0 VDC +10% @ 200mA
MCM-7109: $\pm$ 12VDC $\pm$ 5% @30mA
            +5.0 VDC +5% @ 600mA

Mechanical
Dimensions: 4.6" X 6.5"

Connectors
Analog Input: 26-pin dual on 0.100" grid

Environmental
Operating Temperature:
    LPM-7109   -25°C to +70°C
    MCM-7109   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- "Intelligent" STD Bus 8 and 16 channel sensor interface
- Supports any combination of RTD's, thermocouples, strain and pressure gages, thermistors, resistors, or voltage inputs
- Onboard uP intelligence unburdens STD Bus system CPU by performing control, linearization, and conversion to engineering units
- 16-Bit A/D resolution
- True four-wire circuits for resistive sensors
- Pulsed excitation source reduces self-heating in resistive sensors
- Totally electronic calibration - no trimpots to adjust
- Backward compatible with Sensoray's 7408 and 7409
- Includes QUICKSENSE menu-driven software
- Low power required

The MCM-7418/7419 board is a complete 8/16 channel analog subsystem designed to offer a simple and inexpensive way to acquire high precision sensor data for any STD based system. It is optimized for temperature and low level signal measurements and includes signal filtering, sensor excitation and linearization on all channels. The onboard CPU performs all data acquisition control and preprocesses the data, thus reducing the software overhead by the STD Bus host CPU.
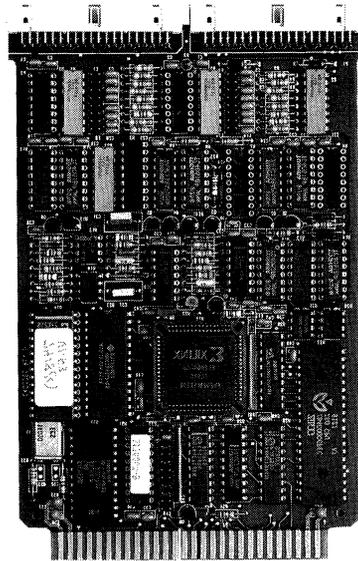
FUNCTIONAL CAPABILITY

STD Bus Interface - Full data, address, and control line buffering is provided to and from the STD Bus. The card is I/O mapped and supports 10-bit addressing and IOEXP*. 74HCT type data bus receivers and
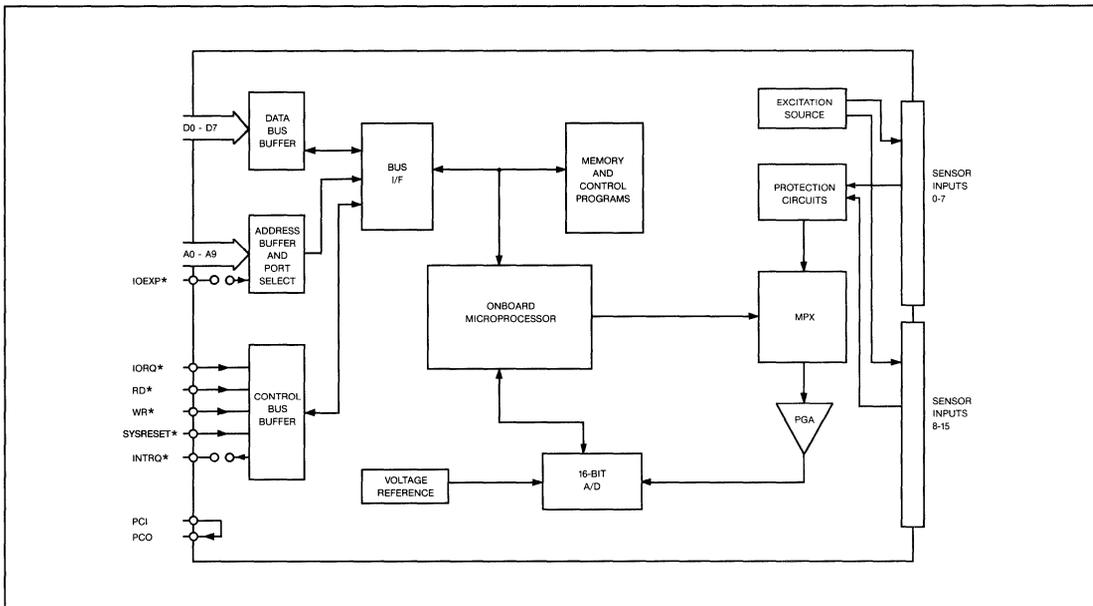
74HCT type data bus transmitters permit the board to work with either STD or CMOS STD Bus systems.

Sensor Input - The MCM-7418 supports eight and the MCM-7419 supports sixteen independent, differential sensor channels with 16-bit resolution. Each channel is over-voltage protected and may be directly connected to an unconditioned sensor. Complete signal conditioning is provided for thermocouples, RTD's, strain and pressure gages, resistors, thermistors, and voltage inputs. A pulsed constant voltage source supplies excitation to other resistive sensors. Constant current excitation combined with true four-wire circuits completely eliminates lead-loss errors for RTD's, thermistors, and resistors.

Sensor Types Supported

Type E thermocouple	10K Ohm thermistor
Type J thermocouple	User-defined resistor
Type K thermocouple	Voltage input 0-100mV
Type T thermocouple	Voltage input 0 to +5V
Type S thermocouple	120 ohm strain gage
Type R thermocouple	4-20 mA current input
Type 385 RTD	Pressure gage/load cell
Type 392 RTD	No sensor

The onboard microcomputer continuously scans the 8 or 16 sensor channels. Each channel is amplified, filtered, digitized, linearized, converted to engineering units, tested against minimum/maximum limits, and stored in onboard memory, independent of the main STD Bus host CPU's activity. Reference junction compensation is automatically performed for thermocouples using a reference transducer on the ADP-7409TA termination board. This reference transducer uses a special dedicated channel so that all sensor channels remain free for application use.

The MCM-7418/7419's internal CPU is programmed to recognize a small but powerful set of commands. One of the Commands, Define Channel Sensor, declares the type of sensor connected to a channel so that the specified channel will automatically be setup properly. This also permits any combination of sensors to input the MCM-7418/7419 card in any mix.

The board periodically calibrates itself by measuring internal references. Reference data is stored in a EEPROM so that the MCM-7418/7419 boards may be quickly interchanged without hassle. Board calibration is easily performed with the aid of a menu-driven calibration procedure.

Software Support - The board includes QUICK-SENSE, a comprehensive menu-driven test program that makes possible the acquisition and display of sensor data in just a few minutes on any PC compatible. The disk also includes a calibration program, sample BASIC and C language programs, and driver source code written in QuickBasic and C.

Field Wiring - The ADP-7409TA screwdriver termination board is available for terminating field wiring for 8 sensor channels. Two units are required for all 16 channels. The ADP-7409TA includes an Isothermal terminal block and temperature sensor that is monitored by the MCM-7418/7419 CMOS microprocessor to perform exact cold compensation for thermocouples. The MCM-7418/7419 and ADP-7409TA are connected by the CBL-126-2, a 24 inch 40-pin ribbon cable.

SPECIFICATIONS

Electrical
STD Bus and CMOS STD Bus Compatible
Common Mode Rejection: 80 dB minimum,
$$@ \; CMV < 5VDC$$
A/D converter: 16-bit, 16.67mS conversion time
Scan Rate: 20mS per channel
Input protection: 63 VAC common mode voltage
Power: $\pm$ 12 VDC to $\pm$ 15 VDC $\pm$ 5%, 35mA
+5 VDC $\pm$ 5%, 100mA

Mechanical
Size: 4.5" X 6.5"

Connectors
Sensor Input: Two, 40-pin on 0.100" centers

Environmental
Operating Temperature: -25°C to +85°C

ORDERING INFORMATION

MCM-7418	8-Channel Sensor Inferface
MCM-7419	16-Channel Sensor Inferface
ADP-7409TA	8-channel field termination panel
CBL-126-2	40-pin, 24 inch ribbon cable

WinSystems, Inc.

FEATURES

- 16 single ended/8 differential input channels
- 12-bit resolution
- User configurable gains of 1 to 1000
- Throughput to 13,333 channels per second
- Interrupt on conversion complete
- Processor independent including V50, V20, 80C88, HD64180, NSC-800, Z80, and 80C85A
- +5V Operation with Optional DC/DC Converter
- Jumper selectable I/O addressing
- Replacement for Analog Devices RTI-1280
- Operational temperature range: -25°C to +85°C

The LPM-A/D12M and LPM-1280 cards provide 8 differential or 16 single-ended 12-bit analog input channels with a throughput of up to 13,333 channels per second. User programmable gains from 1 to 1000 allow effective input ranges from 10 millivolts to 10 volts. Installation of an optional DC/DC converter makes the board require +5 volts only.

FUNCTIONAL CAPABILITY

Bus Interface - Full data, address, and control line buffering is provided to and from the bus. It supports all CMOS STD Bus processors operating with up to a 8 MHz system clock without wait states.

Addressing - The card is configured for 8-bit I/O addressing. A total of 4 contiguous addresses are required and it is jumper selectable.
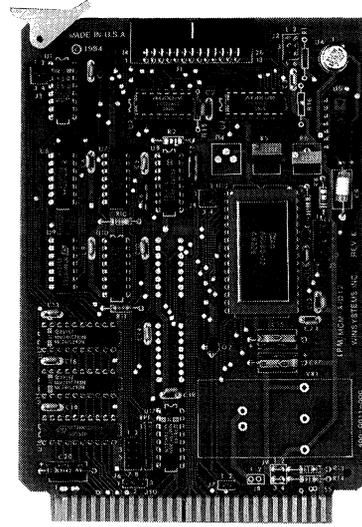
Analog Input Section - The card contains a multiplexer, a pin programmable gain instrumentation ampli-

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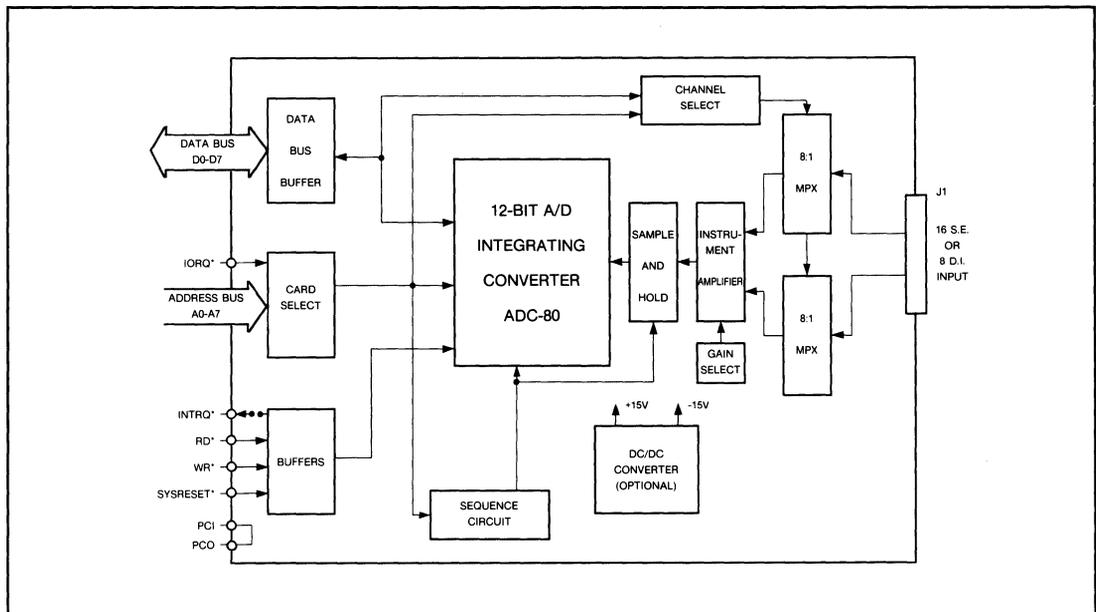
fier, and a sample-hold circuit. The card accepts up to either 16 single-ended or 8 differential inputs. The multiplexer switches' can withstand $\pm$ 20V with the power off, and $\pm$ 32V with the power on. The outputs of the multiplexers are connected to an instrumentation amplifier which is jumper selectable for gains of 1, 10, 100, and 500. Binding posts for an external user selectable resistor allows the user to select a fifth programmable gain from 1 to 1000. The output of the amplifier is connected to a sample-hold circuit which "freezes" the analog input voltage while the A/D converter is performing a conversion. This prevents the voltage from changing while the conversion is in progress.

Analog to Digital Converter - The card contains an Analog Devices ADC-80, 12-bit A/D converter. Coding can be straight binary, offset binary or 2's complement. The input ranges are 0 to +10 VDC and $\pm$10 VDC.

Input Configuration - Each input channel is wired to a pin socket and header connector, J1. Flat ribbon cables or discreet wires can be connected to it.

Two different 12-bit A/D boards are available from WinSystems: LPM-A/D12M and LPM-1280. Both cards are functionally and software compatible with the exception of the pin-out on the analog input connector. The LPM-A/D12M uses the WinSystems standard analog signal pinout and a 26-pin connector. The LPM-1280 uses a 34-pin conector and is compatible with the Analog Devices RTI-1260 board. It permits direct connection with the AC1585-1 screw terminal panel and the 3-B series analog signal conditioning backplanes.

Interrupts - Conversion is begun each time the channel number is written to the board. An end of conversion signal can generate a jumper selectable INTRQ* signal on the CMOS STD Bus. Also the signal sets a BUSY flag for use in a polled mode.

DC /DC Power Supply - The card can be operated from $\pm$ 12 VDC or $\pm$ 15 VDC supplied from the CMOS STD Bus. For $\pm$ 12 VDC operation, the input voltage range is limited to $\pm$ 5 VDC. Other input voltage ranges can be accommodated by installing a single resistor to increase the gain of the instrumentation amplifier.

The LPM-A/D12M and LPM-1280 cards are offered with an optional DC/DC power supply installed and designated as the LPM-A/D12M-DC and LPM-1280-DC. This allows the board to operate directly from the microcomputer's +5 volt supply. The DC/DC supply outputs $\pm$ 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

CMOS STD Bus - The LPM-A/D12M and LPM-1280 cards are limited to a -25°C lower temperature range because of the A/D converter specifications. WinSystems can optionally populate the board with military range devices to extend it to -40°C. Contact the factory for details.

SPECIFICATIONS

Electrical

Number of Channels: 16 single-ended or 8 differential
Input Impedance: Greater than 100 Megohms
Input Overvoltage: $\pm$ 20V
Input Ranges: $\pm$ 2.5 V, $\pm$ 5 V, 0 to +5 V, 0 to +10V, and $\pm$ 10V,
Coding: Straight binary (unipolar)
      Offset binary, 2's complement (bipolar)
Resolution: 12-bits
Nonlinearity: $\pm$ ½ LSB
Gain Error: Adjustable to zero
Offset or Zero Error: Adjustable to zero
Conversion Time: 75 microseconds
Power Requirements: Without DC to DC Converter
      +5 VDC $\pm$ 5% at 75 mA typ.
      +12/15 VDC $\pm$ 5% 20 mA typ.
      -12/15 VDC $\pm$ 5% 15 mA typ.
      With DC to DC Converter
      +5 VDC $\pm$ 5% at 300 mA typ.

Mechanical

Dimensions: 6.5 x 4.5 inches

Connectors

CMOS STD Bus: 56-pin dual 0.125 inch centers
Input: 26-pin dual on 0.100″ grid (LPM-A/D12)
      34-pin dual on 0.100″ grid (LPM-1280)
Jumpers: 0.025″ square posts

Environmental

Operating Temperature: -25°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-A/D12M   12-bit analog input board
LPM-A/D12M-DC 12-bit analog input card with DC/DC converter for +5 VDC operation
LPM-1280   12-bit analog input board compatible with RTI-1280
LPM-1280-DC   12-bit analog input card with DC/DC converter for +5 VDC operation; compatible with RTI-1280

WinSystems, Inc.

**P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553**

FEATURES

- 16 single ended/8 differential input channels
- 12-bit resolution
- User configurable gains of 1 to 1000
- Throughput to 13,333 channels per second
- Interrupt on conversion complete
- Processor independent including 80186, 8088, HD64180, 68008, Z80, and 8085A
- +5V Operation with optional DC/DC converter
- Jumper selectable I/O addressing
- Replacement for Analog Devices RTI-1260
- Optional CMOS version: LPM-A/D12 and LPM-1280

The MCM-A/D12 and MCM-1260 cards provide 8 differential or 16 single-ended 12-bit analog input channels with a throughput of up to 13,333 channels per second. User programmable gains from 1 to 1000 allow effective input ranges from 10 millivolts to 10 volts. Installation of an optional DC/DC converter makes the board require +5 volts only.
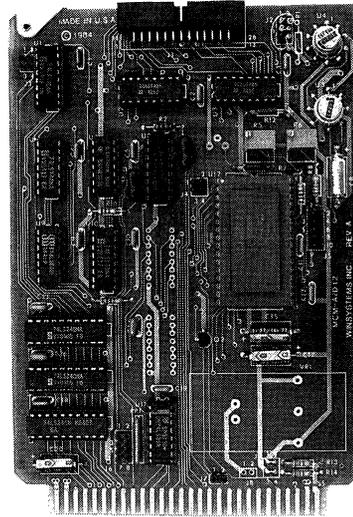
FUNCTIONAL CAPABILITY

Bus Interface - Full data, address, and control line buffering is provided to and from the bus. It supports all STD Bus processors operating with up to a 8 MHz system clock without wait states.

Addressing - The card is configured for 8-bit I/O addressing. A total of 4 contiguous addresses are required and it is jumper selectable.

Analog Input Section - The card contains a multiplexer, a pin programmable gain instrumentation amplifier, and a sample-hold circuit. The card accepts up to

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either 16 single-ended or 8 differential inputs. The multiplexer switches' can withstand ±20V with the power off, and ±32V with the power on. The outputs of the multiplexers are connected to an instrumentation amplifier which is jumper selectable for gains of 1, 10, 100, and 500. Binding posts for an external user selectable resistor allows the user to select a fifth programmable gain from 1 to 1000. The output of the amplifier is connected to a sample-hold circuit which "freezes" the analog input voltage while the A/D converter is performing a conversion. This prevents the voltage from changing while the conversion is in progress.

Analog to Digital Converter - The card contains an Analog Devices ADC-80, 12-bit A/D converter. Coding can be straight binary, offset binary or 2's complement. The input ranges are 0 to +10 VDC and ±10 VDC.

Input Configuration - Each input channel is wired to a pin and socket and header connector, Jl. Flat ribbon cables or discreet wires can be connected to it.

Two different 12-bit A/D boards are available from WinSystems: MCM-A/D12 and MCM-1260. Both cards are functionally and software compatible with the exception of the pin-out on the analog input connector. The MCM-A/D12 uses the WinSystems standard analog signal pin-out and a 26-pin connector. The MCM-1260 uses a 50-pin conector and is compatible with the Analog Devices RTI-1260 board. It permits direct connection with the AC1585-1 screw terminal panel and the 3-B series analog signal conditioning backplanes.

Interrupts - Conversion is begun each time the chanel number is written to the board. An end of conversion signal can generate a jumper selectable INTRQ* signal on the STD Bus. Also the signal sets a BUSY flag for use in a polled mode.

DC/DC Power Supply - The card can be operated from ± 12 VDC or ± 15 VDC supplied from the STD Bus. For ± 12 VDC operation, the input voltage range is limited to ± 5 VDC. Other input voltage ranges can be accommodated by installing a single resistor to increase the gain of the instrumentation amplifier.

The MCM-A/D12 and MCM-1260 cards are offered with an optional DC/DC power supply installed and designated as the MCM-A/D12-DC and MCM-1260-DC. This allows the board to operate directly from the microcomputer's +5 volt supply. The DC/DC supply outputs ± 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

SPECIFICATIONS

Electrical

Number of Channels: 16 single-ended or 8 differential
Input Impedance: Greater than 100 Megohms
Input Overvoltage: ± 20V
Input Ranges: ± 2.5 V, ± 5 V, 0 to +5 V, 0 to +10V, and ± 10V,
Coding: Straight binary (unipolar)
      Offset binary, 2's complement (bipolar)
Resolution: 12-bits
Nonlinearity: ± ½ LSB
Gain Error: Adjustable to zero
Offset or Zero Error: Adjustable to zero
Conversion Time: 75 microseconds
Power Requirements: Without DC to DC Converter
      +5 VDC ± 5% @ 300 mA
      +12/15 VDC ± 5% @ 20 mA
      -12/15 VDC ± 5% @ 15 mA
      With DC to DC Converter
      +5 VDC ± 5% @ 500 mA

Mechanical

Dimensions: 6.5 x 4.5 inches

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Input: 26-pin dual on 0.100" grid (MCM-A/D12)
      50-pin dual on 0.100" grid (MCM-1260)
Jumpers: 0.025" square posts

Environmental

Operating Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM A/D12   12-bit analog input board

MCM-A/D12-DC 12-bit analog input board with DC/DC converter for +5 VDC operation

MCM-1260   12-bit analog input board compatible with RTI-1260

MCM-1260-DC 12-bit analog input board with DC to DC converter for single +5 VDC operation compatible with RTI-1260

WinSystems, Inc.

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FEATURES

- Up to 32 single ended input channels
- Two analog output channels
- 12-bit resolution for A/D and D/A
- Digitally programmable input amplifier
- Sample and Hold
- 125 uS conversion time
- Interrupt on conversion complete
- Processor independent including V50, V40, V20, 80C88, HD64180, NSC-800, CMOS Z80 and 80C85A
- Jumper selectable Memory or I/O addressing
- Low Cost 8, 16, or 32 channel A/D version available: LPM-AIO-8
- +5V Operation with optional DC Converter
- Available for CMOS STD Bus: LPM-AIO
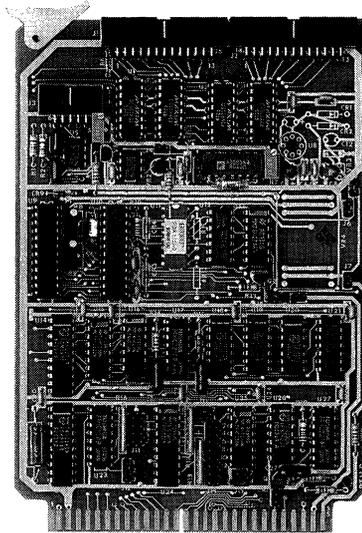
The LPM/MCM-AIO is a multipurpose 12-bit analog input and output board. It has 32 single ended voltage input channels and 2 voltage output channels. User software programmable gains of IX, 10X, and 100X are available. The LPM-AIO is a low power CMOS design which will operate over extended temperature ranges.

Installation of an optional DC/DC converters makes the board require +5 volts only. The board is compatible with all STD Bus and CMOS STD Bus CPU cards.

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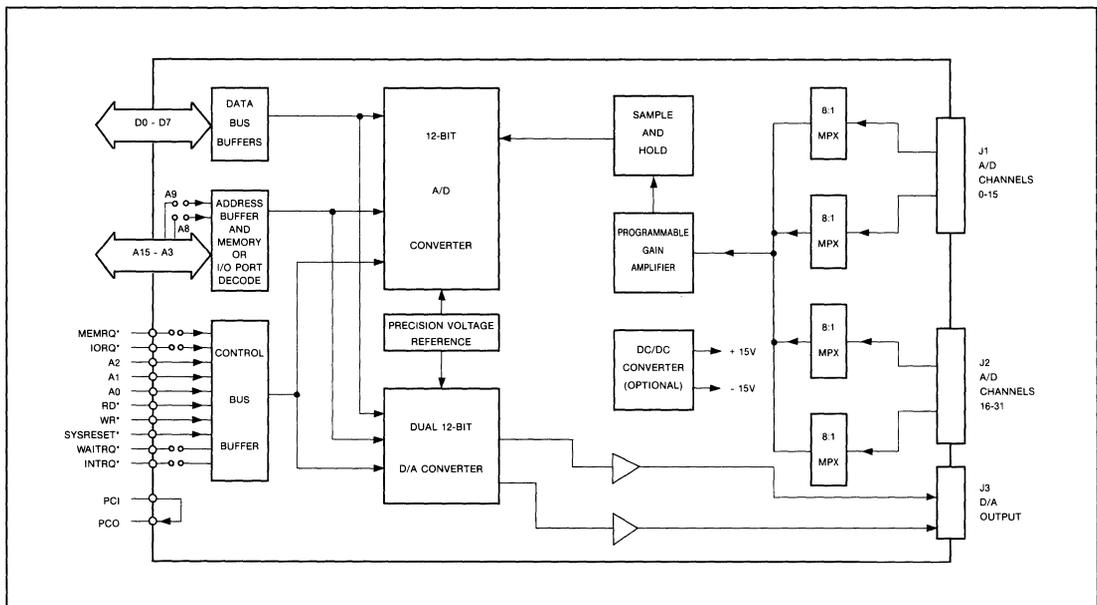
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-AIO is the CMOS STD Bus versions and the MCM-AIO is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Wait States - A jumper selectable Wait State generator is on board to generate 1 Wait State for synchronization with fast processors.

Addressing - The card is configured for two modes of addressing: 8/16-bit I/O or 16-bit memory addressing. This provides direct access of up to 64K I/O ports or memory locations by decoding A0 through A15. Typically 8-bit processors will only generate 256 I/O port addresses (A0 - A7). For 808X, NEC "V" series and HD64180 type CPUs, 64K I/O ports can be decoded if required.

On the LPM/MCM-AIO, IOEXP is jumper selectable to be active high, active low, or don't care to double the I/O port addressing range.

For memory mapped CPU's, 64K locations plus MEMEX* are decoded. A jumper selectable active low MEMEX* is supported for additional address qualification.

Address Selection - A total of 16 contiguous addresses are required by the LPM/MCM-AIO and it is jumper selectable on any even 16 port/byte boundary. Programming is very straight forward. The card can be either addressed as successive bytes of memory or a block of I/O ports from a jumper selectable base address.

LPM/MCM-AIO Base Address Map

D7	D6	D5	D4	D3	D2	D1	D0	Byte ADDR
X	PGl	PG0	M4	M3	M2	M1	M0	0
B7	B6	B5	B4	B3	B2	B1	LSB	1
BUSY	IP	X	X	MSB	B10	B9	B8	2
X	X	X	X	X	X	X	X	3
B7	B6	B5	B4	B3	B2	B1	LSB	4
X	X	X	X	MSB	B10	B9	B8	5
B7	B6	B5	B4	B3	B2	B1	LSB	6
X	X	X	X	MSB	B10	B9	B8	7

Notes: 1. The Symbol X means the bit is not used.
      2. The BUSY Bit equals "1" during conversion and "0" when Done.

3. The Byte ADDR is fixed but the LPM/MCM-AIO board's boundary address is selectable within the map by on-board jumpers.

Byte 0: MUX ADDRESS/GAIN - The first byte address (0), is used to select any random input channel and the software programmable amplifier's gain by writing to its address. The Write command automatically triggers a timer that sets the Sample and Hold into the "Hold" mode and starts the A/D conversion on the selected channel.

M0 through M4 provide a natural binary select of the 32 channels (0 through 31). The amplifier gain select truth table is as follows:

PG1	PG0	Gain Selected
0	0	1 X
0	1	10 X
1	0	100 X
1	1	Undefined

Byte 1: A/D Low Byte - The 8 lowest order bits of the 12-bit A/D word are available at this address.

Byte 2: A/D High Byte - The 4 highest order bits of the A/D 12-bit word are provided at this address. In addition, the "BUSY" bit provides the status of the A/D converter. The CPU can determine the end-of-conversion cycle by reading this byte. A logic "0" indicates that the conversion is complete and the A/D data is valid and can now be read.

The IP bit represents Interrupt Pending. It indicates the end-of-conversion has been completed and the CPU flagged. The IP bit is cleared by reading the low order data in Byte 1.

Byte 4: DAC0 Low Byte - This byte is written to with the 8 Lowest order bits for the first D/A channel's 12-bit word.

Byte 5: DAC0 High Byte - This byte is written to with the 8 most significant bits for the first D/A channel's 12-bit D/A word.

Byte 6: DACl Low Byte - This byte is written to with the 8 lowest order bits for the second D/A channel's 12-bit word.

Byte 7: DAC1 High Byte - This byte is written to with the 8 most significant bits for the second D/A channel's 12-bit D/A word. Writing to this byte commands both D/A converters to update their output with its new value.

Byte 3 and 8 through 15 - These bytes are presently unused by the LPM/MCM-AIO board. Bytes 8 through 15 are reserved but not decoded. Another board in a system can have ports mapped at these locations without redundant addressing conflicts.

Analog Input Section - The LPM/MCM-AIO contains a multiplexer, software programmable gain/fast settling operational amplifier, and a sample-hold circuit. The card accepts up to either 32 single-ended, 0 to +5 volt, unipolar inputs. Total conversion time is 125 uS.

Multiplexer - The LPM/MCM-AIO card contains up to four 8 channel CMOS Analog Multiplexers with overvoltage protection. They can withstand analog input voltages much greater than the supplies. The multiplexer switches' inputs can withstand 10V greater than either supply with the power off, which eliminates the possibility of damage when supplies are off. Equally important, they can withstand brief input transient spikes which would otherwise require complex external protection networks.

Programmable Gain Amplifier - The outputs of the multiplexers are connected to a PGA-102, precision digitally controlled, Programmable Gain/Fast Settling Operational amplifier. The LPM/MCM-AIO is software programmable for gains of 1, 10, and 100.

Sample and Hold Circuit - The output of the amplifier is connected to a sample-hold circuit which "freezes" the analog input voltage while the A/D converter is performing a conversion. This prevents the voltage from changing while the conversion is in progress. A calibration circuit is provided to trim any error voltages from the amplifier or sample and hold circuitry before reaching the A/D converter.

Analog to Digital Converter - The LPM/MCM-AIO contains an Analog Devices AD7578, 12-bit Successive Approximation A/D converter. It has a conversion time of 100 uS. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100 uV. There are no missed codes over the full temperature range. The output code is straight binary.

Digital to Analog Converter - The LPM/MCM-AIO contains an Analog Devices' AD7537 Dual 12-bit DAC. Two independent DACs are on one monolithic chip configured to provide two 0 - 5 volt outputs. The input section is double buffered to allow simultaneous update of both DAC's. A two byte transfer is required to interface an 8-bit CPU byte to the 12-bit D/A.

These registers "memorize" the 12-bit digital word and keeps the D/A converter output constant until it is updated with a new value in one step.

Input Configuration - The analog input channels are wired to two 26-pin, pin-and-socket header connectors, J1 and J2. The first connector inputs channels 0 through 15 and J2 inputs channels 16 through 31. Either flat ribbon cables or discreet wires can be mated to the connectors. The pin-out is identical to the single ended input configuration of the WinSystems' LPM/MCM-A/D12M.

Output Configuration - Each output channel is wired to a 10-pin right angle male connector, J3. Flat ribbon or discreet wires can be connected to it. Alternating ground lines, paired with each output channel's signal line, improves noise immunity and reduces cross-talk.

Interrupts - A/D conversion is begun each time the channel number is written to the board. An end-of-conversion signal can generate a jumper selectable INTRQ* signal on the STD Bus and CMOS STD Bus. This signal also sets an IP flag in bit 6 of Byte 2 for use in a polled mode operation.

DC/DC Power Supply - The card can be operated from $\pm$ 12 VDC or $\pm$ 15 VDC supplied from the STD Bus and CMOS STD Bus. The LPM/MCM-AIO card is offered with an optional DC/DC power supply installed and designated as the LPM/MCM-AIO-DC. This allows the board to operate directly from the microcomputer's +5 volt supply. The DC/DC supply outputs $\pm$ 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

CMOS STD Bus - The LPM-AIO card is limited to a -25°C lower temperature range because of the A/D converter specifications. WinSystems can optionally populate the board with military range devices to extend it to -40°C. Contact the factory for details.

Standard Configurations - Eight different LPM/MCM-AIO boards are available from WinSystems in different population options. They options include no DACs, DC/DC converter, and fewer input channels. The LPM/MCM-AIO boards without the D/A converters (LPM/MCM-AIO-8, LPM/MCM-AIO-16, LPM/MCM-AIO-32) also do not have the programmable gain amplifier and the sample hold circuitry in order to offer the lowest price card. Contact the

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factory if you require a different population other than the ones listed. The standard configurations are as follows:

	AIO CHANNELS	SAMPLE - HOLD	PGA	D/A CHANELS	+5 ONLY
LPM/MCM-AIO	32	Yes	Yes	2	No
LPM/MCM-AIO-DC	32	Yes	Yes	2	Yes
LPM/MCM-AIO-8	8	No	No	0	No
LPM/MCM-AIO-8-DC	8	No	No	0	Yes
LPM/MCM-AIO-16	16	No	No	0	No
LPM/MCM-AIO-16-DC	16	No	No	0	Yes
LPM/MCM-AIO-32	32	No	No	0	No
LPM/MCM-AIO-32-DC	32	No	No	0	Yes

SPECIFICATIONS

Electrical

Analog Input

Number of Channels: Up to 32 single-ended
Input Impedance: greater than 100 Megohms
Input Overvoltage: $\pm$ 10V (with power off)
Input Ranges: 0 to +5 V (with programmable gain)
Coding: straight binary (unipolar)
Resolution: 12-bits
Nonlinearity: 1 LSB
Conversion Time: 125 microseconds (includes sample-hold time and slew rates for the amplifier and multiplexers)

Analog Output

Number of Channels: 2 (LPM/MCM-AIO)
D/A Resolution: 12-bits
Coding: Straight Binary
Output Voltage: 0 to +5 volts
Differential Nonlinearity: $\pm$ 1 LSB
Relative Accuracy: $\pm$ 1 LSB
Output Settling Time: 5 uS

Power Requirements

LPM/MCM-AIO configured with 32 input A/D channels, amplifier, sample-hold and 2 D/A channels

Without DC to DC Converter
+5 VDC $\pm$ 5% at 5 mA (typ.)
+12/15 VDC $\pm$ 5% 44 mA (typ.)
-12/15 VDC $\pm$ 5% 22 mA (typ.)

With DC to DC Converter
+5 VDC $\pm$ 5% at 200 mA (typ.)

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Input: Two 26-pin dual on 0.100" grid
Output: One 12-pin dual on 0.100" grid
Jumpers: 0.025" square posts

Environmental

Operating Temperature:
    LPM-AIO   -25°C to +85°C
    MCM-AIO   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-AIO	12-bit, 32 channel analog input and 2 channel analog output card
LPM-AIO-DC	12-bit analog input/output board with DC/DC converter for single +5 VDC operation
LPM-AIO-8	Low cost 12-bit A/D with 8 S.E inputs
LPM-AIO-8-DC	LPM-AIO-8 with DC/DC converter (+5V only)
LPM-AIO-16	Low cost 12-bit A/D with 16 S.E inputs
LPM-AIO-16-DC	LPM-AIO-16 with DC/DC converter (+5V only)
LPM-AIO-32	Low cost 12-bit A/D with 32 S.E inputs
LPM-AIO-32-DC	LPM-AIO-32 with DC/DC converter (+5V only)
MCM-AIO	12-bit, 32 channel analog input and 2 channel analog output card
MCM-AIO-DC	12-bit analog input/output board with DC/DC converter for single +5 VDC operation
MCM-AIO-8	Low cost 12-bit A/D with 8 S.E inputs
MCM-AIO-8-DC	LPM-AIO-8 with DC/DC converter (+5V only)
MCM-AIO-16	Low cost 12-bit A/D with 16 S.E inputs
MCM-AIO-16-DC	LPM-AIO-16 with DC/DC converter (+5V only)
MCM-AIO-32	Low cost 12-bit A/D with 32 S.E inputs
MCM-AIO-32-DC	LPM-AIO-32 with DC/DC converter (+5V only)

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FEATURES

- Eight independent analog voltage output channels
- 12-bit resolution
- Four output voltage ranges: 0 to +5V, 0 to + 10V, $\pm$ 5V, $\pm$ 10V
- Memory or I/O mapped
- Processor independent including V50, V20, 80C88, HD64180, CMOS Z80, 80C85A, 6502, and NSC-800.
- +5V operation with optional DC/DC convertor
- 8 MHz operation
- Replacement for Analog Devices RTI-1282
- MEMEX and IOEXP supported
- Available for CMOS STD Bus: LPM-D/A12

The LPM/MCM-D/A12 card provides up to eight, 12-bit CMOS digital to analog output channels. Each channel can be configured for one of four output voltage ranges. The LPM/MCM-D/A12 can be memory or I/O mapped making it processor independent. Installation of an optional DC/DC converter makes the board require +5 volts only.
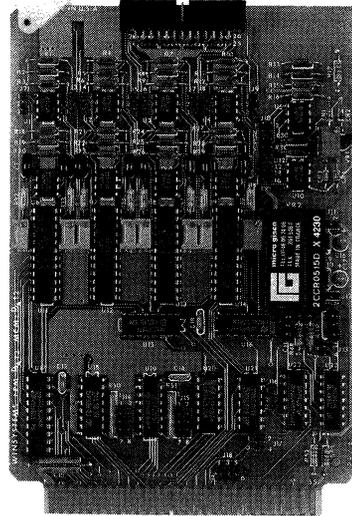
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-D/A12 is the CMOS STD Bus versions and the MCM-D/A12 is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and function-ality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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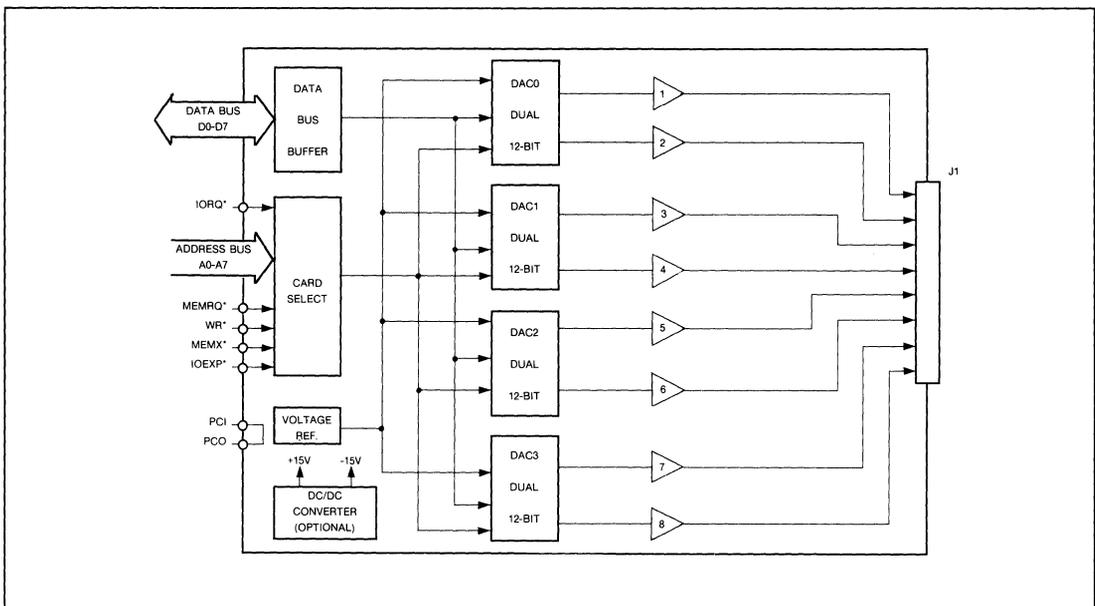
Digital to Analog Converter - The LPM/MCM-D/A12 contains either two or four Analog Devices' AD7537 dual DAC's. The digital to analog conversion is accurate to 12-bits. Each D/A channel can be independently selected and configured for unipolar or bipolar output ranges of 0 to +5 VDC, 0 to +10 VDC, jumper $\pm$ 5 VDC, and $\pm$ 10 VDC. The four output ranges are jumper selectable on a per channel basis. Each channel has its own gain adjustment for calibration.

The analog output card comes in versions: a 4 channel (LPM/MCM-D/A12-4) and 8 channel (LPM/MCM-D/A12-8). Each can optionally be populated with a DC/DC converter.

Two bytes of data are assigned to each channel's D/A converter. Data is output by simply first writing the 8 least significant bits then the 4 most significant bits of D/A data. The converter is double buffered so that both bytes of data are automatically loaded when the high byte is written, thus ensuring a one step update of the D/A output.

Output Configuration - Each output channel is wired to a 26-pin right angle male connector, Jl. Flat ribbon cables or discreet wires can be connected to it. The connector pin-out is compatible with Analog Devices' AC1585-2 screw termination panel or the 3-B signal conditioning backplane.

The LPM/MCM-D/A12 is a replacement for the Analog Devices RTI-1282 except that it does not support the optional 20mA current outputs. Four optional D/A channels were added instead of the current output option.

DC/DC Power Supply - The LPM/MCM-D/A12 is offered with an optional DC/DC power supply installed and designated as the LPM/MCM-D/A12-DC. This allows the board to operate directly on the microcomputer's +5 volt supply. The DC/DC supply outputs $\pm$ 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

SPECIFICATIONS

Electrical
Number of Output Channels: 4 or 8
D/A Resolution: 12-bits (4096 Counts)
A/D Output Code: Binary, offset binary
Output Voltage Range: 0V to +5V, 0V to +10, $\pm$ 10V, and $\pm$ 10V at 5mA (jumper selectable)
Differential Nonlinearity: $\pm$1 LSB
Relative Accuracy: $\pm$ 1 LSB
Output Settling Time: 5 uS
Power Requirements:
Without DC to DC Converter
   LPM-D/A12:   +5VDC $\pm$ 5% at 5mA typ.
                 +15VDC $\pm$ 5% at 50mA typ.
                 -15VDC $\pm$ 5% at 30mA typ.
   MCM-D/A12: +5VDC $\pm$ 5% at 155mA typ.
                 +15VDC $\pm$ 5% at 50mA typ.
                 -12/15VDC $\pm$ 5% at 30mA typ.
With DC to DC Converter
   LPM-D/A12:   +5VDC $\pm$ 5% at 250mA typ.
   MCM-D/A12: +5VDC $\pm$ 5% at 400mA typ.

Mechanical
Meets STD Bus mechanical specifications

Connectors
STD Bus: 56-pin dual 0.125 inch centers
Analog Output: 26-pin dual 0.100 inch grid
Jumpers: 0.025″ square posts

Environmental
Operating Temperature:
     LPM-D/A12   -25°C to +85°C
     MCM-D/A12   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-D/A12-4   CMOS STD Bus 4 Channel, D/A
LPM-D/A12-4-DC LPM-D/A12-4 with DC/DC
LPM-D/A12-8   CMOS STD Bus 8 Channel, D/A
LPM-D/A12-8-DC LPM-D/A12-8 with DC/DC
MCM-D/A12-4   STD Bus 4 Channel, D/A
MCM-D/A12-4-DC MCM-D/A12-4 with DC/DC
MCM-D/A12-8   STD Bus 8 Channel, D/A
MCM-D/A12-8-DC MCM-D/A12-8 with DC/DC

WinSystems, Inc.

FEATURES

- Eight independent analog voltage output channels
- 8-bit resolution
- Four output voltage ranges: 0 to +IV, 0 to +2.5V, 0 to +5V, and 0 to +10V
- Memory or I/O mapped
- Processor independent including V50, V40, 80C88, NSC-800, HD64180, CMOS Z80, 80C85A, and 6502
- +5V operation with optional DC/DC converter
- 8 MHz operation
- Available for CMOS STD Bus: LPM-D/A8

The LPM/MCM-D/A8 is an 8-bit, eight channel digital to analog output board. Each channel can be configured for one of four output voltage ranges. The LPM/MCM-D/A8 can be memory or I/O mapped making it processor independent. Installation of an optional DC/DC converter makes the board require +5 volts only.
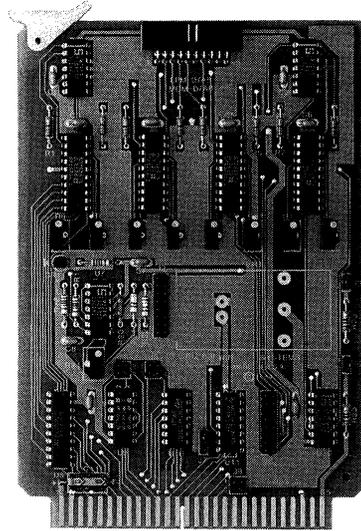
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-D/A8 is the CMOS STD Bus versions and the MCM-D/A8 is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-D/A8 is configured for two modes of addressing: 8-bit I/O or 16-bit memory addressing. Any random output channel can be selected by simply writing data to its corresponding

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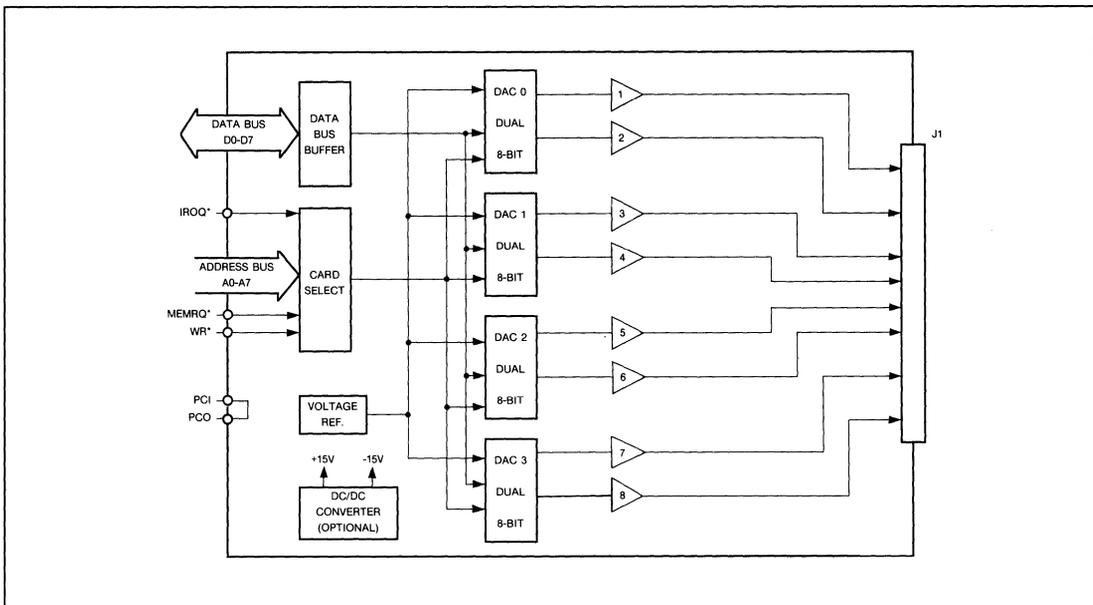
address. A total of 8 contiguous addresses are incremented from the base address. The address selection is jumper selectable.

Digital to Analog Converter - The LPM/MCM-D/A8 contains four Analog Devices' 7528 dual DAC's. The digital to analog conversion is accurate to 8-bits. The 8-bit resolution provides least significant bit values of 39mV on the 0 to +10 volt range. Each D/A channel is independently selected. Four output ranges are jumper selectable on a per channel basis. These ranges are: 0 to +1 VDC, 0 to +2.5 VDC, 0 to +5 VDC, and 0 to +10 VDC. Each channel has its own gain adjustment for calibration.

Output Configuration - Each output channel is wired to a 20-pin right angle male connector, Jl. Flat ribbon cables or discreet wires can be connected to it. Alternating ground lines, paired with each output channel's signal line, improves noise immunity and reduces cross-talk.

J1 - Analog Output Connector

Pin	Description	Pin	Description
1	Channel 0	2	Ground
3	Channel 1	4	Ground
5	Channel 2	6	Ground
7	Channel 3	8	Ground
9	Channel 4	10	Ground
11	Channel 5	12	Ground
13	Channel 6	14	Ground
15	Channel 7	16	Ground
17	Ground	18	Ground
19	Ground	20	Ground

DC/DC Power Supply - The LPM/MCM-D/A8 is offered with an optional DC/DC power supply installed and designated as the LPM/MCM-D/A8-DC. This allows the board to operate directly on the microcomputer's +5 volt supply. The DC/DC supply outputs $\pm$ 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

SPECIFICATIONS

Electrical

Number of Output Channels: 8
D/A Resolution: 8-bits (256 Counts)
A/D Output Code: Binary
Output Voltage Range: 0V to +1V, 0V to +2.5V, 0V to +5V, 0V to +10V at 5mA (jumper selectable)
Differential Nonlinearity: $\pm$ 1 LSB
Relative Accuracy: $\pm$ 1 LSB
Output Settling Time: 15 uS
Power Requirements:
Without DC to DC Converter:
    LPM-D/A8:   +5VDC $\pm$ 10% at 50mA typ.
                     $\pm$ 15VDC $\pm$ 5% at 50mA typ.
    MCM-D/A8: +5VDC $\pm$ 5% at 200mA typ.
                     $\pm$ 12VDC $\pm$ 10 at 5mA typ.
With DC to DC Converter:
    LPM-D/A8:   +5VDC $\pm$ 10% at 250mA typ.
    MCM-D/A8: +5VDC $\pm$ 5% at 400mA typ.

Mechanical

Meets STD Bus mechanical specifications

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Analog Output: 20-pin dual 0.100 inch grid

Environmental

Operating Temperature:
    LPM-D/A12   -25°C to +85°C
    MCM-D/A12   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-D/A8	CMOS STD Bus 8 Channel, 8-bit analog output board with manual
LPM-D/A8-DC	LPM-D/A8 with DC/DC converter
MCM-D/A8	STD Bus 8 Channel, 8-bit analog output board with manual
MCM-D/A8-DC	MCM-D/A8 with DC/DC converter

WinSystems, Inc.

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FEATURES

- Access to all STD Bus and CMOS STD Bus lines and power buses
- Decoded addressing
- Data bus buffers with hystersis
- 8 decoded input and 8 output strobes
- Processor independent
- Large breadboard area on 0.100" grid accepts standard DIP sockets, connectors and press-fit pins in plated through holes
- IOEXP supported
- Single +5V operation
- Replacement for Pro-Log 79C04
- Available for CMOS STD Bus: LPM-7904

The LPM/MCM-7904 is a card designed for prototyping I/O circuitry. The STD Bus and CMOS STD Bus is decoded with input and output logic and STD Bus and CMOS STD Bus buffering to allow a user to construct experimental and custom I/O interfaces with a minimum of effort. A 0.100 inch grid is provided for the breadboard area that accepts standard DIP sockets, connectors, press-fit pins and discrete logic circuitry.
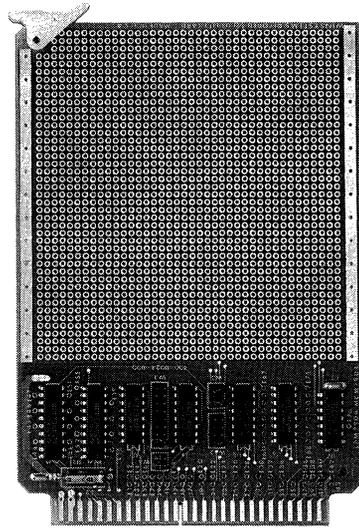
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7904 is the CMOS STD Bus versions and the MCM-7904 is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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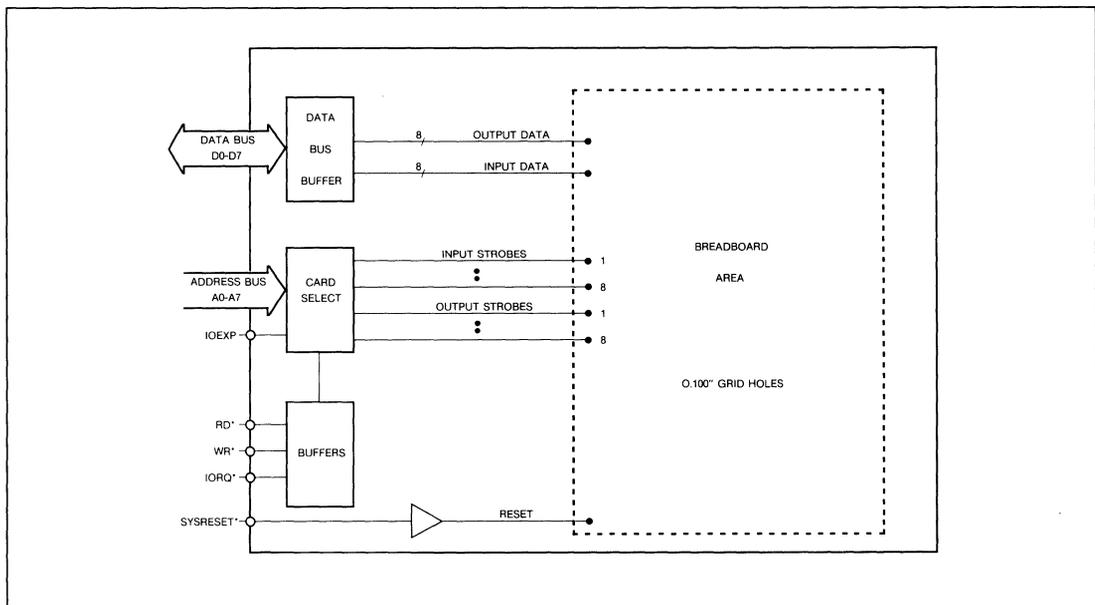
Full data, address, and control line buffering connection points are provided from the bus to the prototyping circuit area.

LPM/MCM-7904 is a replacement for the Pro-Log 7904 and 79C04 card.

Addressing - The LPM/MCM-7904 is configured for 8-bit I/O memory addressing. A total of 8 contiguous addresses are provided by decoding A0 to A2. IOEXP is available and can be decoded as either active low or don't care. The base address is determined by A3 to A7 and can be located on any jumper selectable even 8-port boundary.

Configuration - Beyond the address decoding circuitry is a prototyping breadboard area. This 4.3″ x 3.8″ area is available for prototype and experimental circuit design. It consists of a 0.100 inch grid of 0.042 inch plated through holes that will accept 0.025 inch square posts, standard 8, 14, 16, 24, 28, and 40-pin DIP sockets and discrete components. The entire top of the card is available for installation of one or several 0.100″ right angle connectors or headers at the edge.

Additionally the signal pads, power pads, and ground pads are labeled on the circuit side of the board for easy identification. All chips are socketed for removal or replacement.

Data Bus - Data bus buffers are provided to interface between the STD Bus and CMOS STD Bus and prototype circuit area. Eight input and output strobes are associated with the buffers to either input or output data from up to 8 different ports on the LPM/MCM-7904 card to the host STD Bus and CMOS STD Bus processor.

Input Strobes - Eight input strobe lines are available to the prototype board area and correspond to 8 sequential read ports. These decoded strobes enable input devices when data is requested by the processor and also turn on the data bus buffers to gate the data onto the STD Bus and CMOS STD Bus. Each strobe is generated when a processor Read is made to the respective port.

Output Strobes - Eight output strobe lines are available to the prototype board area and correspond to 8 sequential write ports. The decoded strobes become active during the processor's I/O port Write cycle. They can be used to latch data from the STD Bus and CMOS STD Bus buffer without any additional gating.

SPECIFICATIONS

Electrical

All STD Bus and CMOS STD Bus processors with I/O mapping are supported

I/O Addressing: Jumper selectable on 8-port boundary

Power Requirements:

LPM-7904: +5V $\pm$ 10% at 50mA (plus user circuitry)
MCM-7904: +5V $\pm$ 5% at 100mA (plus user circuitry)

Mechanical

Meets all STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes

Connectors

STD Bus: 56-pin dual 0.125″ centers
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-7904   -40°C to +85°C
    MCM-7904   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7904   CMOS STD Bus Decoded I/O utility card
MCM-7904   STD Bus Decoded I/O utility card

WinSystems, Inc.

FEATURES

- Calendar Clock with battery backup
- Uses the MM58167A
- 24 Hour Clock with BCD Format
- Interrupts generated on alarm or at programmed intervals
- Status bit to indicate rollover during read
- 56 bits of battery backed RAM
- Processor independent
- Precision power fail detect circuit
- On board lithium battery for power down operation
- Optional laser trimmed LCXO clock module
- Single +5 volt supply
- Available for CMOS STD Bus: LPM-CLK

The LPM/MCM-CLK is a STD Bus and CMOS STD Bus compatible, battery backed, calendar clock board that uses the National Semiconductor MM58167A calendar clock chip. The LPM/MCM-CLK provides ten thousandths of seconds, hundredths and tenths of seconds, seconds, minutes, hours, day of week, day of month, and month. Also the LPM/MCM-CLK provides 56 bits of RAM for power down data storage.
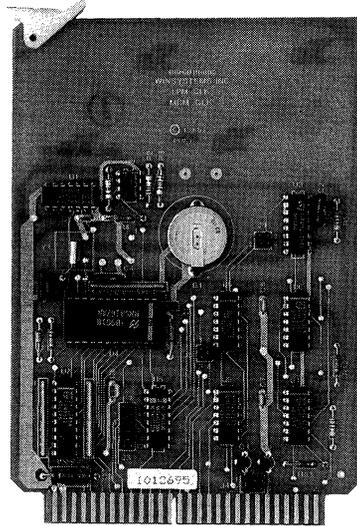
FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-CLK is the CMOS STD Bus versions and the MCM-CLK is the STD Bus

versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

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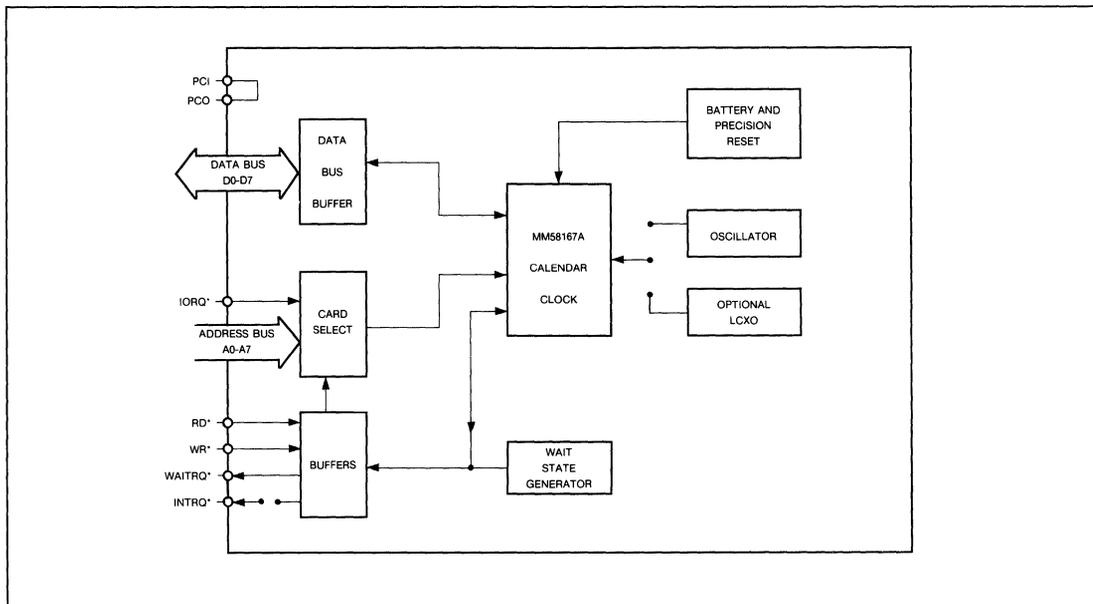
Addressing - The LPM/MCM-CLK is configured for 8-bit I/O addressing. A total of 32 consecutive I/O addresses are required. The base address is jumper selectable by the user.

Clock Calendar - The LPM/MCM-CLK uses the MM58167A clock calendar chip operating on a 32,768 Hz crystal controlled time base. Either a standard tuning fork crystal or optional precision laser trimmed LCXO serve as the oscillator. The chip provides ten thousandths of seconds, hundredths and tenths of seconds, seconds, minutes, hours, day of week, day of month, and month. The data is BCD, 24 hour format.

The MM58167A clock chip is easy to initialize. All that is required is to write to the specific port location (i.e. seconds, hours, etc.) and the chip will accept the data without any need to stop the clock.

The data from the clock is read simply by reading the desired I/O port address. No special synchroniziation is required. A status bit is provided to insure that bad data is not read because of the counter chain rippling or rolling over during the Read operation.

Also the LPM/MCM-CLK provides 56 bits of RAM for power down data storage if the Alarm function is not used.

Interrupts - The LPM/MCM-CLK can generate an· interrupt on the condition of a compare with the RAM (Alarm) or programmed intervals of 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week and once a month. The interrupt is jumper enabled to the STD Bus and CMOS STD Bus.

The interrupt from the LPM/MCM-CLK can be used to generate either a vectored Z80 mode 2 or 8085/8088 non vectored (Z80 Mode 1) interrupt.

Powerfail Detect/Battery - A precision low power detect circuit and a long life Lithium battery is included to allow the calendar clock to operate in a ultra low power mode when the system power is removed.

An 180mA hour battery is supplied standard on the board. Continuous standby service life of the cell is in excess of 3 years and it is extended when the

LPM/MCM-CLK is powered by the STD Bus and CMOS STD Bus Vcc. An optional 750 mAH battery can be ordered. It will quadruple the standby service time.

SPECIFICATIONS

Electrical

All STD Bus and CMOS STD Bus processors with I/O mapping.

Power Requirements:
LPM-CLK: +5VDC ± 10% at 10mA (max.)
MCM-CLK: +5VDC ± 5% at 100mA (max.)

Mechanical

Meets STD Bus mechnical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
    LPM-CLK   -40°C to +85°C
    MCM-CLK   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-CLK   CMOS STD Bus Battery backed
                 Calendar Clock board.
LPM-CLK-LXO CMOS STD Bus Battery backed
                 Calendar Clock board with LXCO
MCM-CLK   STD Bus Battery backed Calendar
                 Clock board.
MCM-CLK-LXO STD Bus Battery backed Calendar
                 Clock board with LXCO

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Nine independent 16-bit Counter/Timers
- Uses 3 standard 82C54 Programmable Interval Timers
- Six programmable counter modes per channel
- Handles inputs from DC to 8 MHz
- Binary or BCD counting
- Clock, Gate, and Out signals from 8 channels buffered and accessed via 2 connectors
- Channel 9 configurable as clock source for other channels
- Optional 82C59A Interrupt Controller
- Configurable Watchdog Timer
- Single +5 volt supply
- Available for CMOS STD Bus: LPM-CTC
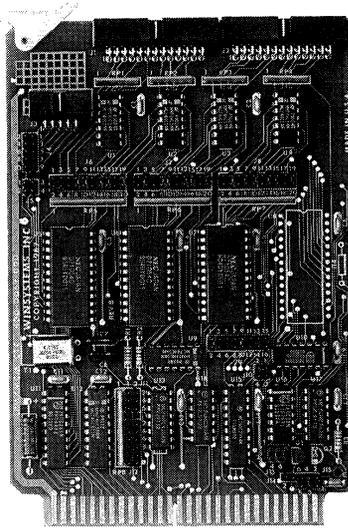
The LPM/MCM-CTC card is designed to solve the common timing problems in industrial systems design. Nine independent 16-bit channels are capable of frequency/event counting from DC to 8 MHz, pulse marker or square wave generation, time interval measurements, and one-shot simulation. Eight channels have a buffered Clock, Gate, and Output available at the top of the card. Jumper headers provide source selection and cascading to yield maximum configuration flexibility.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-CTC is the CMOS STD Bus versions and the MCM-CTC is the STD Bus versions of these cards. The LPM/MCM prefix
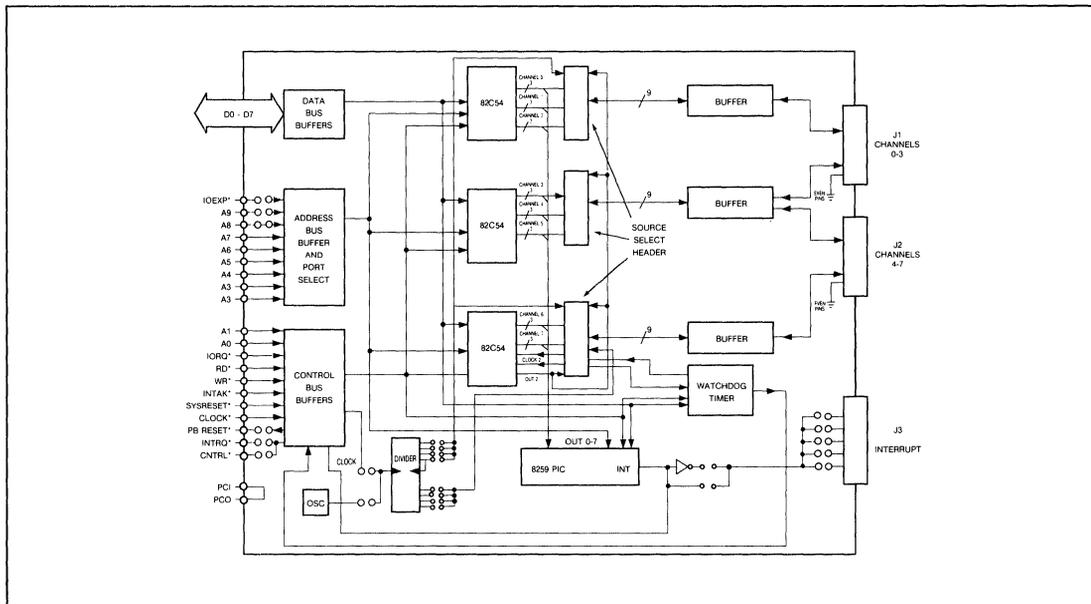
indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-CTC is I/O mapped for either 8 or 10-bit I/O addressing and is jumper configurable to start on any even 16 byte boundary.

Counter/Timers - The LPM/MCM-CTC utilizes three 82C54 programmable interval timers that can be individually configured to be real time clocks, event counters, digital one-shots, square wave generators, or programmable rate generators. Each 82C54 contains three independent software programmable counter/timers yielding a total of nine 16-bit channels. The individual channels can be cascaded for longer count sequences.

The three internal 82C54 counters are identical in operation. Each consists of a single, 16-bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the Control Word Register. The status of the contents of each counter is available to the computer with a simple READ operation for event counting applications. Special logic is included so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

Watchdog Timer - The nineth channel can alternatively be used as a watchdog timer. This channel, programmed in the retriggerable one-shot mode, can have its output jumpered to the PBRESET* line of the STD Bus and CMOS STD Bus which will force a system reset in case of a software malfunction.

Time Base Clock - The nineth channel can also serve as a jumper selectable clock input to any of the other 8 channels for use in interval measurements. Either the System Clock or a onboard 2.4576 MHz crystal oscillator drives a dual divide by 2, 4, 8, or 16 prescaler that is input to Channel 9 and available to the other counters via the configuration header. The output of Channel 9's counter can be used to further scale the clock and its corresponding output is available to the other 8 channels.

Configuration Headers - Access to the Clock, Gate, Out and the boards Time Base Clock is provided for all channels. A select header is provided to permit jumpering clock inputs from the I/O Connectors, Channel 9, or the System Clock.

Connector Configuration - The LPM/MCM-CTC has two, 26-pin connectors that permit access to the Clock, Gate and Out signals for each channel. The connectors are grouped with 4 channels per connector. All the signals are fully buffered on and off the board. Each signal line is paired with a ground line to prevent adjacent noise and crosstalk. All input lines have Schmitt trigger circuits to prevent oscillation from signals with slow rise and fall times.

Interrupts - The LPM/MCM-CTC will generate STD-8088 compatible interrupts when an optional 82C59A PIC is installed (LPM/MCM-CTC-1). The PIC generates a unique, vectored interrupt for each of the 8 CTC channels.

SPECIFICATIONS

Electrical

System Clock: Up to 8 MHz

Interface: Inputs - All inputs are 74HC/TTL levels
Outputs - All outputs are 74HC/TTL levels

Power Requirements:
LPM-CTC: +5V ± 10% at 20mA typ.
MCM-CTC: +5V ± 10% at 215mA typ.

Mechanical

Meets STD Bus mechanical specifications

Connectors

Channel: Two, 26-pin dual on 0.100 grid
Interrupt: 10-pin dual on 0.100 inch grid
Jumpers: 0.025 inch square posts

Environmental

Operating Temperature:
    LPM-CTC   -40°C to +85°C
    MCM-CTC   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-CTC-0   CMOS STD Bus Nine channel 16-bit
            counter/timer card
LPM-CTC-1   CMOS STD Bus Nine channel 16-bit
            counter/timer card with 82C59 PIC
MCM-CTC-0   STD Bus Nine channel 16-bit
            counter/timer card
MCM-CTC-1   STD Bus Nine channel 16-bit
            counter/timer card with 82C59 PIC

WinSystems, Inc.

WinSystems®

FEATURES

- Very low cost STD Bus operator interface
- Supports standard 14 and 16-pin alphanumeric LCD displays up to 4 x 40 characters
- LCD Contrast adjustment onboard
- Mirrored pin-out for easy cabling to displays
- Supports 4 x 4 and 5 x 4 matrix keyboards
- Keyboard controller automatically scans and debounces keypad input
- 2-key rollover
- Polled or interrupt keyboard operation
- 8-bit general purpose output port
- LED onboard for visual program status
- Processor independent
- Available for CMOS STD Bus: LPM-KYBLCD
- Single +5 volt operation

The LPM/MCM-KYBLCD board is suitable where a very low cost keyboard and LCD interface is needed for system control, data entry, status display, and operator prompting. It is also useful for system development, testing and training applications.

It supports 4 x 4 or 5 x 4 matrix keyboard inputs and 1 to 4 line parallel LCD displays with up to 80 characters from companies such as Hitachi, Epson, Seiko, Densitron, Sharp and others.
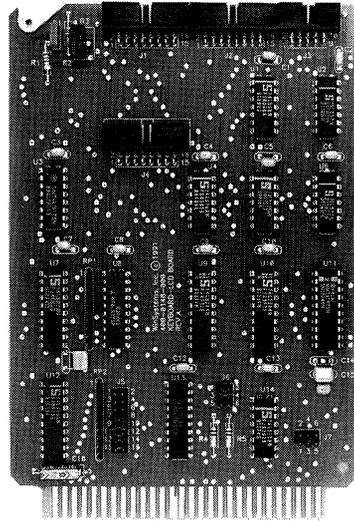
FUNCTIONAL CAPABILITY

STD Bus Interface - The MCM-KYBLCD is the STD Bus and the LPM-KYBLCD is the CMOS STD Bus version

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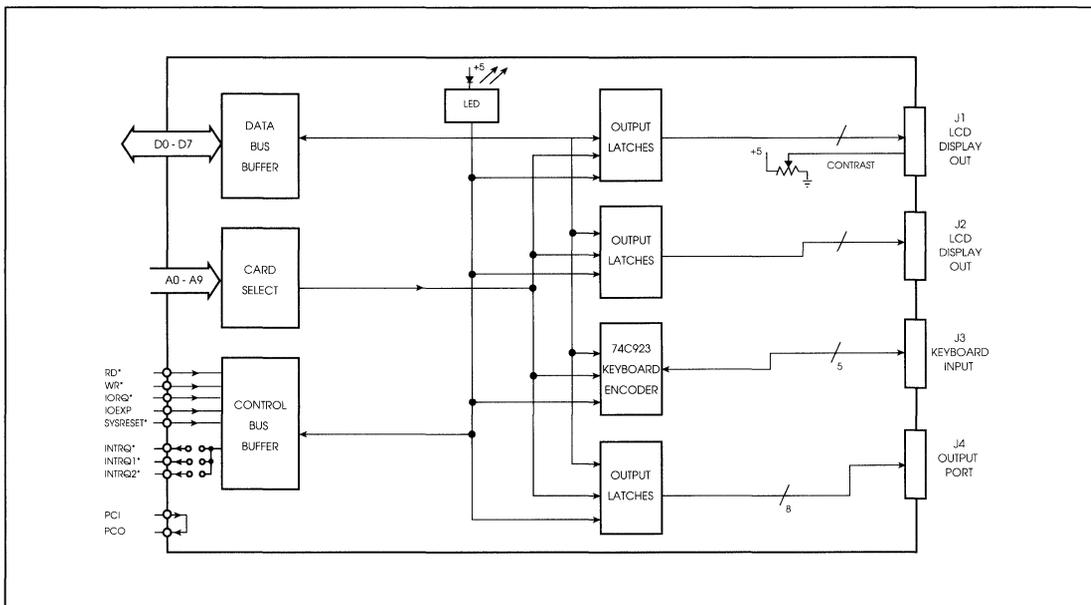
of the board. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operational temperature range.

Addressing - The LPM/MCM-KYBLCD is processor independent supporting 8-bit or 10-bit I/O addressing. It is selectable on any 8 port boundary. IOEXP is decoded as active high, active low, or don't care and can be used to double the addressing range.

Keyboard Encoder - The keyboard controller used is the National Semiconductor 74C923 20-key encoder which supports 2 key rollover. The output coding for the keyboard is straight binary. It automatically scans either 4 x 4 and 5 x 4 matrix style keyboards using switches with up to 50k ohm ON resistance.

When a key is depressed, the switch closure is debounced and the data is latched. The board can be used in either a polled or interrupt mode. The interrupts can be jumpered to one of 3 interrupt pins on the STD Bus backplane.

LCD Interface - The LPM/MCM-KYBLCD is designed to interface directly to HD44780 based displays. The board utilizes a mirrored pin-out to allow a dual row header to be soldered on the back of the LCD module rather than on the component side of the board so that a standard ribbon cable can be used instead of a discrete wired cable. If the header is installed on the component side of the LCD display module, the height of the header and the cable assembly will prevent the user from flush mounting the module to a panel.

The LPM/MCM-KYBLCD card has both a 14- and 16-pin right angle header to support the most popular parallel display interfaces.

LCD Displays - LCD displays are made by Hitachi, Seiko, Epson, Densitron, Sharp and others. Characters per line range from 8 to 40 lines with 1 to 4 lines per display. Call WinSystems' Applications Engineering Department if you have compatibility questions concerning the display you have selected.

Contrast Adjustment - The LPM/MCM-KYBLCD is designed for displays that utilize a single supply voltage both for the display logic and the driving

voltage for the contrast control. The contrast is adjusted by an onboard trimpot to give the maximum viewing at the desired angle.

Parallel Port - The card has one general purpose 8-bit TTL output port wired to a 16-pin right angle header. Data is latched into a data bus buffer during a Write to the data register.

Onboard LED - A red LED is on the board that can be turned ON, OFF or blinking under software control to provide a visual indication of program status or as a debugging aid.

SPECIFICATIONS

Electrical

Interface Bus: LPM-KYBLCD - CMOS STD Bus
　　　　　　　MCM-KYBLCD - STD Bus
System clock: up to 8 MHz
I/O Addressing: 10-bit
Data Transfer: 8-bits wide

Power Requirements (with LED off)
LPM-KYBLCD:　Vcc = +5V $\pm$ 10% at 235 mA
MCM-KYBLCD: Vcc = +5V $\pm$ 5% at 675 mA

Mechanical

Dimensions: 4.5″ x 6.5″

Connectors

Keyboard: 10-pin, 0.100″ grid
LCD: 14-pin, 0.100″ grid
　　16-pin, 0.100″ grid
Parallel I/O: 16-pin, 0.100″ grid

Environmental

Operating Temperature:
　　LPM-KYBLCD:　-40°C to +85°C
　　MCM-KYBLCD:　0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-KYBLCD　　　CMOS STD Bus keyboard/LCD
　　　　　　　　　interface
MCM-KYBLCD　　　STD Bus keyboard/LCD interface

WinSystems, Inc.

FEATURES

- Sockets support two 8-bit SBX Multimodule boards
- User selectable port address on 32-port boundaries
- Reserves 2 blocks of 16 I/O ports per SBX socket
- Optional 82C59 PIC or Z80-CTC support interrupts for V50/80C88/80C85 or Z80/HD64180 CPUs
- Prototyping/breadboard area provided
- IOEXP decoded
- Single +5V operation
- Available for CMOS STD Bus: LPM-SBX
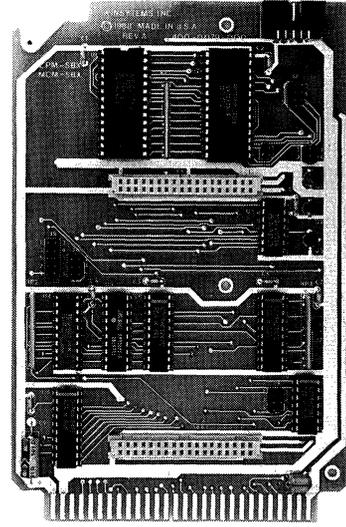
The LPM/MCM-SBX offers processor independent support of up to 2 interrupt driven iSBX multimodule sockets for additional special I/O expansion on the STD Bus and CMOS STD Bus. A complete line of SBX expansion modules are available including analog and digital I/O, high speed math, serial and parallel I/O, floppy and hard disk interfaces, video graphics, Bit-Bus, and other special purpose peripheral controllers.

FUNCTIONAL CAPABILITY

Overview - The LPM/MCM-SBX card generates the physical and electrical interfaces from the STD Bus and CMOS STD Bus to two independent single-wide SBX expansion module sockets. The interface between the LPM/MCM-SBX and SBX single wide multimodules is through two female 36-pin (8-bit) connectors.

STD Bus Interface - The LPM-SBX is the CMOS STD Bus versions and the MCM-SBX is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and function-

ality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.
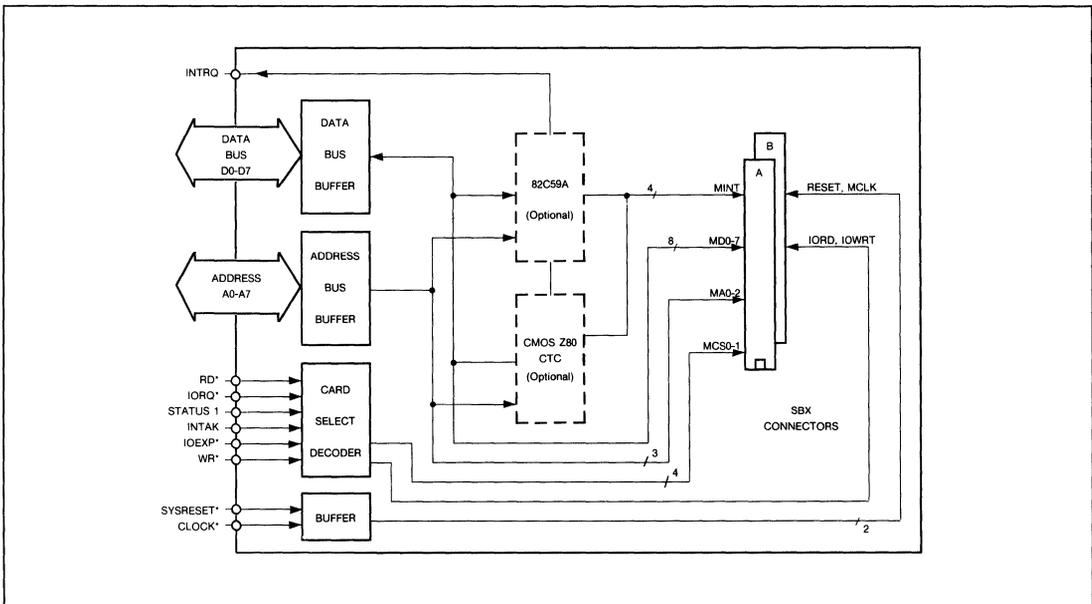
Bus Interface - The LPM/MCM-SBX is I/O mapped and is jumper addressable on 32-port boundaries with two blocks of 16 contiguous I/O ports for each SBX socket.

IOEXP is supported and can be configured in two ways. It can be jumpered to ground or enabled with an active low. DMA and MWAIT operations are not supported by the LPM-SBX board.

Multimodule Mounting - A single wide SBX board dimension's are 3.7 x 2.85 inches. A separate connector and hole is provided on the LPM/MCM-SBX for each multimodule. A nylon screw/spacer assembly for additional mechanical stability is supported.

Interrupts - An interrupt controller can be added as a population option to generate STD Bus and CMOS STD Bus system interrupts. Each processor type has unique interrupt structure requirements that dictates a different VLSI chip to be installed. Either a CMOS Z80 CTC can be installed to support the CMOS Z80/HD64180 processors (LPM/MCM-SBX-1) or the 82C59A installed to support 80C85/80C88/V50 processors (LPM/MCM-SBX-2). If no interrupt support is required, then neither interrupt controllers are installed and it is designated the LPM/MCM-SBX-0.

The LPM/MCM-SBX-2 has an on board master 82C59A type Programmable Interrupt Controller (PIC) that provides 8 vectored priority interrupts. Two vectored interrupts, MINT0 and MINT1, can be generated from each of the SBX modules mounted on the board. The other 4 interrupt lines are brought to the top of LPM/MCM-SBX-2 board.

The 8088 parallel interrupt priority scheme is implemented over the front plane of the card for multiple interrupting cards. Alternatively, the cascade STD-8088 interrupt priority scheme is implemented by supplying the slave cascade address over the STD Bus address lines A8 - A10 during interrupt acknowledge cycles.

The LPM/MCM-SBX-1 has a Z80-CTC on board that will act as a Z80 mode 2 interrupt generator. The MINT lines of both SBX connectors are connected to the TRG0 to TRG3 lines. The Z80-CTC is programmed to serve as an interrupt controller. When an interrupt request is activated by any channel, the Z80-CTC can generate a mode 2 vectored interrupt automatically.

If no interrupt support is required, then the LPM/MCM-SBX-0 is available with no interrupt controller on board.

SPECIFICATIONS

Electrical

SBX compatible for 8-bit non-DMA operation
Bus Interface: STD Bus and CMOS STD Bus
Power Requirements:
LPM-SBX: +5V $\pm$ 10% at 10mA
              +12V dependent upon SBX module used
MCM-SBX: +5V $\pm$ 5% at 60mA
              +12V dependent upon SBX module used

Mechanical

Meets STD Bus mechanical specifications

Connectors

Jumpers: 0.025″ square posts
Interrupt: 10-pin dual 0.100 inch grid
SBX: Two 18/36-pin dual row female on 0.100 inch centers
STD Bus: 56-pin dual 0.125 inch centers

Environmental

Operating Temperature:
    LPM-SBX   -40°C to +85°C
    MCM-SBX   0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-SBX-0 CMOS STD Bus SBX interface card with no interrupt support
LPM-SBX-1 CMOS STD Bus SBX interface card with 80C85/80C88/V50 interrupt support
LPM-SBX-2 CMOS STD Bus SBX interface card with CMOS Z80/HD64180 interrupt support

MCM-SBX-0 STD Bus SBX interface card with interrupt support
MCM-SBX-1 STD Bus SBX interface card with 80C85/80C88/V50 interrupt support
MCM-SBX-2 STD Bus SBX interface card with Z80/HD64180 interrupt support

WinSystems, Inc.

WinSystems®

STD BUS

MCM-STATUS
Switch Input &
LED Display Card

FEATURES

- 32 Light Emitting Diodes for visual status configured as 8 Green and 24 Red LEDs
- Wide viewing angle on the LEDs
- 32 input switches
- Processor independent including 80186, V50, V40, 80188, NSC-800, HD64180, Z80, and 8085
- Simple program control of LEDs and switches
- Operation to 12 MHz
- Jumper selectable I/O addressing
- IOEXP supported
- +5 Volt operation
- Operational temperature range: 0°C to +65°C
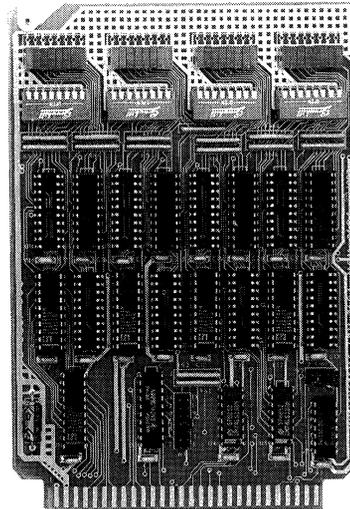
The MCM-STATUS is a general purpose status and diagnostic card that provides 32 switch input and 32 LEDs on a single STD Bus card. It is suitable for applications where a low cost interface is needed for manual switch inputs and visual status for system testing, diagnostics or on-site configuration. The card is I/O mapped and processor independent including the 80186, V50, 80188, V40, 8088, HD64180, Z80, NSC-800, and 8085A.
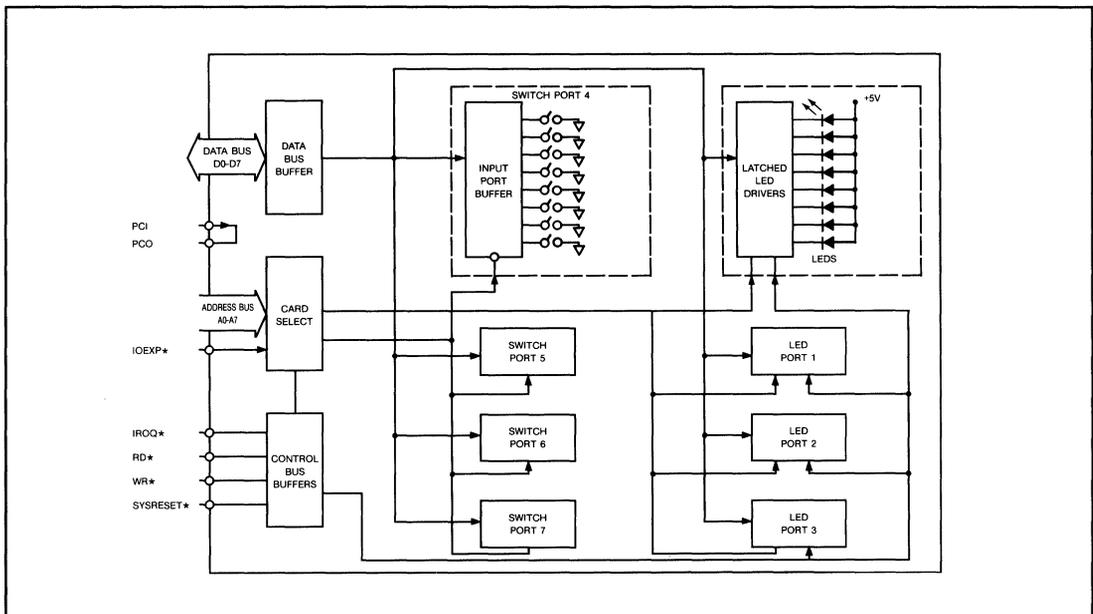
6

FUNCTIONAL CAPABILITY

Bus Interface - Full data, address and control line buffering is provided to and from the bus. All I/O mapped STD Bus processors including the 80286/386sx, 80186, V50, 80188, V40, 8088, HD64180, Z80, NSC-800, and 8085A are supported operating with up to a 12 MHz system clock.

Addressing - The MCM-STATUS is configured for 8-bit I/O addressing. A total of 8 consecutive I/O addresses are required and it is selectable on any even 8-port boundary. Address line A0 through A7 select the card by a jumper selectable decoded combination. IOEXP is decoded as active high, active low, or don't care.

Configuration - The MCM-STATUS is the WinSystems' MCM-7604 parallel input/output card populated with switches and LEDs. The card is decoded as 4 input ports and 4 output ports for a total of 64 I/O lines. The first 4 contiguous ports contain the LEDs and the last 4 port contain the switches. The LEDs are nearest the edge of the board so they can be seen by the user while the card is plugged inside the card cage.

The MCM-STATUS is very easy to use. No complicated peripheral chip initialization routines are required to access the board, just simple I/O port Read or Write commands.

Switch Input Ports - The noninverting input STD Bus data bus buffers are connected directly to each respective SPST piano type DIP switch. Data is gated onto the STD Bus when the respective port is Read.

The switches are organized in four groups of eight stations for a total of 32 points. Each input line is equipped with a pull-up resistor to assure that unconnected lines do not float when the switch is Open. Closing the switch connects the input to ground.

LEDs - Output data from the STD Bus is latched into the data bus buffer of the MCM-STATUS and a visual status of the line is displayed by the respective LED. The output latches are cleared by SYSRESET* or by a power-on reset.

Eight green (port 0) and 24 red (ports 1-3) low profile LEDs are mounted on the board. They have a diffused lens which offer a wide viewing angle.

SPECIFICATIONS

Electrical

All STD Bus processors with I/O mapping are supported with system clock to 12 MHz.

I/O Addressing: Jumper selectable on any even 8 port boundary

Vcc = +5V $\pm$10% at 900 mA typ. (with all LEDs and switches ON)

Mechanical

Dimensions: Meets all STD Bus mechanical specifications; 6.5 x 4.5 inches

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
Jumpers: 0.025" square posts

Environmental

Operational Temperature: 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

MCM-STATUS   Switch input and LED display card

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- High Speed PC Bus to STD Bus Interface
- Direct Bus-to-Bus Interface, no software required
- Supports PC-XT/AT Bus architecture
- Data transfer at PC-XT/AT I/O system clock speed with no WAIT States
- 8-bit data transfers done directly through PC I/O addressing
- Supports 8- and 10-bit STD Bus I/O addressing
- Supports both CMOS STD and STD Bus
- Permits "In Systems Emulation" for quick program development
- Provides access to over 1200+ STD Bus Industrial I/O cards for use with a standard PC-XT/AT
- Voltage optionally supplied to STD Bus card through the data cable
- Supports 5 interrupt levels to the PC Bus
- Polarized data cables with strain relief at the end
- STD Bus SYSRESET* controlled by the PC-XT/AT
- Low cost

The PC-STD Adapter is a low cost solution that permits an IBM PC-XT/AT or compatible host computer access to the IEEE 961 STD Bus I/O cards for industrial applications. The host PC-XT/AT is coupled directly to the STD Bus via a 2 card set. One card is installed in the PC-XT/AT and the other in an STD Bus card enclosure connected by two 34-pin ribbon cables. This is a direct Bus to Bus link operating at full systems speed requiring no software modifications or Wait States to communicate directly from a PC-XT/AT host to the STD Bus I/O cards.
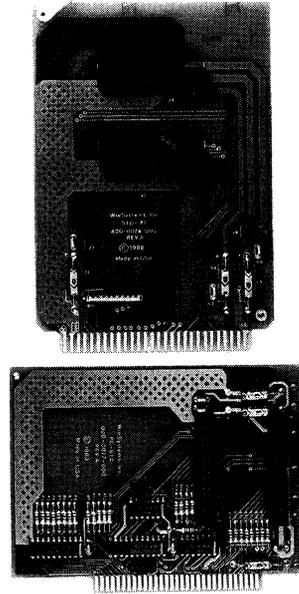
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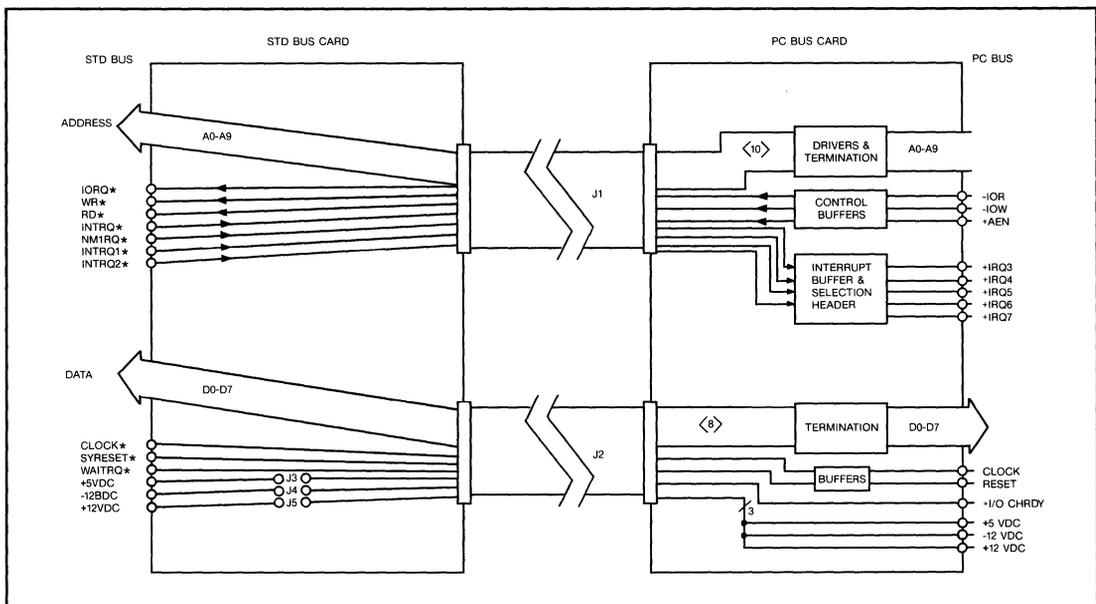
FUNCTIONAL CAPABILITY

Applications - The PC-STD Bus Adapter can be used for 2 main applications: Industrial System Controller and Development System Platform.

The Systems Controller is used for direct control and monitoring by a PC-XT/AT using STD Bus I/O cards. In this mode the PC-XT/AT is used to control all STD Bus I/O devices as simple extensions of its own I/O. STD Bus I/O cards are well suited for industrial I/O because of their rugged design, functionality, open architecture, ease of use, and small size. Over 1200 industrial I/O cards are available from more than 120 companies worldwide at very low cost. The host PC-XT/AT acts as the CPU, storage and display unit. It can also provide access to networks or file servers while the STD Bus cards provide "real world" I/O interfacing. This concept is applicable for additional I/O expansion capability beyond the number of slots available in the host PC-XT/AT.

The PC-STD Bus Adapter is well suited for software development and debugging of the STD Bus systems. The PC-XT/AT serves as an "In Systems Emulator" since it has direct access to the STD I/O cards operating at full bus speed. The programmer has full access to a vast selection of assemblers, high level languages, debuggers and other productivity tools. The final application software can be either PROMed for use in embedded systems or used with STD MS-DOS systems as well. This circumvents the expense of buying a new expensive STD MS-DOS development system by simply allowing you to use your existing PC-XT/AT system.

PC Interface Board - The PC Interface Board is a standard short card requiring 1 card slot within the PC-XT/AT. This board provides an 8-bit parallel data pathway plus control and power signals from the PC Bus to the dual 34-pin ribbon cables. The data transfer rate is at full PC-XT/AT transfer rates without Wait States, typically up to 8 MHz. The I/O CHRDY signal in the host PC-XT/AT is supported to accept Wait State requests for slower I/O devices.

Only I/O transfers are supported. It does not support memory mapped STD Bus cards. Both 8- and 10-bit STD Bus addressing is supported through jumper option J3. For 10-bit addressing, A0 through A9 are fully enable. For 8-bit addressing, the STD Bus cards will be mapped to I/O addresses 100 - 1FF hex only.

These locations prevent potential conflicts with standard existing PC-XT/AT host I/O port locations.

This board generates STD Bus IORQ*, WR*, and RD* from the PC Bus IOR* and IOW* signals. Also IORQ* is inhibited while DMA cycles are occurring in the host PC-XT/AT to prevent any potential bus contention problems.

One hundred ohm series resistors are installed on the Address (A0 - A9), Data (D0 - D7), Clock, IORQ*, RD*, and WR* lines to provide line termination and damping to prevent overshoot, undershoot and ringing.

Five jumper selectable interrupt source input lines are provided to input IRQ3 to IRQ7 to the PC Bus. A jumper header selects the appropriate source from the STD signals INTRQ*, INTRQ1*, INTRQ2*, and NMIRQ*. STD-8088 cascade interrupt acknowledge lines are not supported since the signals are not generated by the host PC-XT/AT.

Data cables - Two CBL-134-6, 34-pin flat cables, link the 2 adapter boards. They are #28 AWG ribbon cables that are each 6-feet long. Each cable end has a polarized, female 34-pin connector with strain relief. The characteristic impedance of the cable is approximately 100 ohms. The data and control signals are separated by alternating ground lines to reduce noise and crosstalk.

DC power can be jumpered through the cable to permit the PC-XT/AT to provide all voltages for small STD Bus systems configurations.

STD Bus Interface Board - This card plugs directly in the STD Bus card rack and terminates the data from the 2 data cables. It also has polarized headers to prevent the cables from being plugged in backwards, The +5 and ±12 volts can be jumpered from the PC-XT/AT into the rack through J3, J4, and J5.

Software - No special routines are needed to address and communicate with the STD Bus cards from the PC-XT/AT. The PC-STD Bus Adapter is a direct hardware link. The exact same software (regardless of language used) will work with either a PC-XT/AT host or a STD Bus 8088 base CPU.

ORDERING INFORMATION

PC-STD ADP PC Bus to STD Bus Interface with Cables.

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6 - 118

FEATURES

- 15W STD Bus in-rack DC/DC power supply
- Three input voltage ranges:
    - 9 - 18 VDC
    - 18 - 36 VDC
    - 36 - 72 VDC
- Wide input voltage range with 2:1 ratio
- Input polarity reversal protection circuit
- Fused input line
- Triple output voltage:
    - +5 VDC at 1500 mA
    - +12 VDC at 310 mA
    - -12 VDC at 310 mA
- Short circuit protection on outputs
- Overvoltage protection on all outputs
- Wide operational temperature range:
    - -25°C to +71°C with no derating
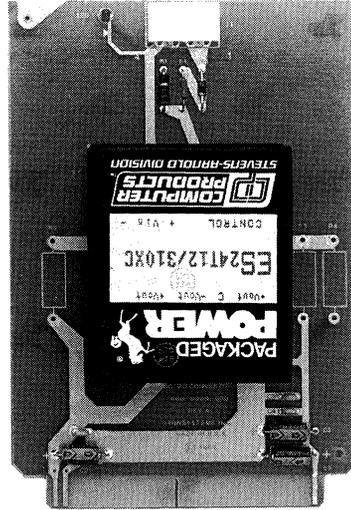
The PS12T12, PS24T12, and PS48T12 are three, 15 Watt STD Bus DC/DC converters that feature a wide input voltage range. The unit plugs directly into an STD Bus card cage to provide a triple output voltage. Nominal DC input voltages of +12, +24, or +48 volts are accepted with a wide input tolerance ratio of 2:1. These units are ideal for applications where only DC input voltage is present and a wide operational temperature range is needed for STD Bus embedded control applications.
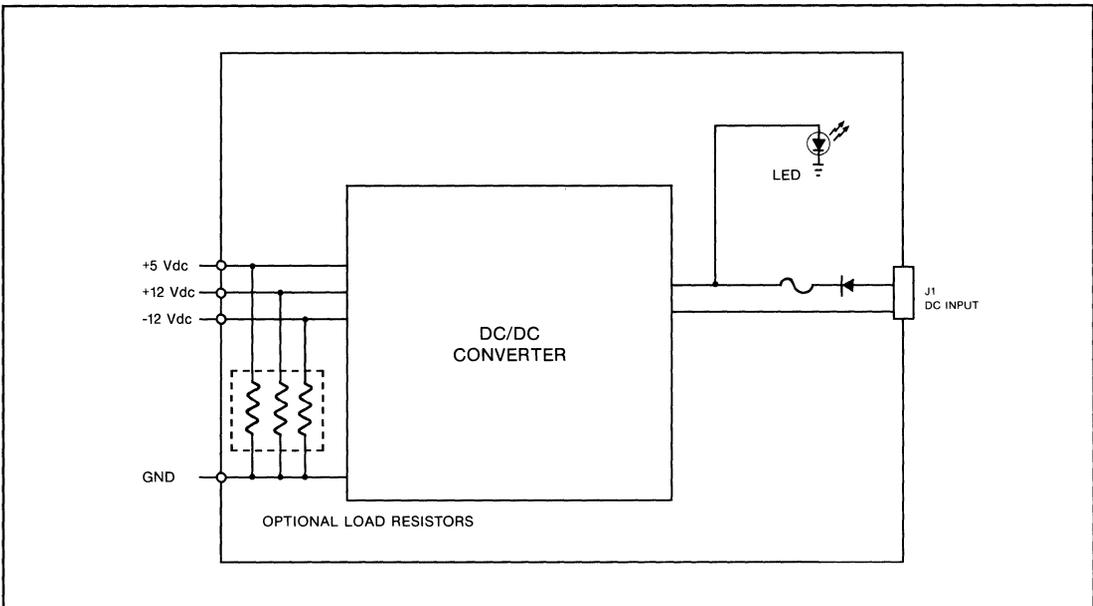
FUNCTIONAL CAPABILITY

Input Voltage Range - The PS12T12 supply accepts 9 - 18 VDC, the PS24T12 accepts 18-36 VDC, and the PS48T12 accepts 36 - 72 VDC input. Each of the power supplies has an input protection circuit that prevents a short circuit if the unit is wired into the main DC supply backwards. An in-line fuse is wired on the input side of the power supply. Also an LED is onboard that will illuminate when DC input power is present.

Output Voltage Range - Three output voltages are present from the power supply: +5 VDC, +12 VDC, and -12 VDC. 1500 mA is available on the +5 volt output. 310 mA is available at both +12 and -12 volts outputs. The onboard high efficiency DC/DC switching power module requires a minimum current loading on each output.

Output Loading and Protection - Thermal shutdown is provided for long-term short circuit and overload clamp protection. Overvoltage protection is provided on each output. The output loading and protection for each output is shown in the table below.

Amperes

VDC	Min	Nom.	Max.	OVP
+5	.250	1.5	2.0	+6.8V
+12	.100	0.31	0.50	+15V
-12	.100	0.31	0.50	-15V

Output Loading and Protection Table

The maximum total power from all outputs is limited to 15 Watts, but no output should be allowed to exceed its maximum current. Minimum current on each output is required to maintain regulation. Solder pads are provided on each output line of the DC/DC converter to accommodate optional user installed resistors to meet the minimum load requirement shown in the table above.

The power supply has a six-sided continuous shield for EMI/RFI protection. Also the unit has input/output isolation of 500 VDC. The efficiency is 78% or higher. Operating temperature is from -25°C to +71°C with no derating.

Mounting - The DC/DC converter is a complete unit that mounts on a STD Bus board. The height of the converter module is 0.83" (21.1mm) which means that the PS12T12, PS24T12, or PS48T12 will require 2 card slots in a card cage if it is not installed in slot 1.

WinSystems, Inc.

Connectors - A Molex 15-24-4041 polarized right angle header is used as the input connector. This is a very common, 4-pin, right angle connector that is used to supply power for the disk drives in PCs.

J1 Input Voltage Pin-Out

Pin	Description
1	+ DC Input voltage
2	+ DC Input voltage
3	Ground
4	Ground

The output voltages are wired to the respective voltage pins on the STD Bus connector. All other pins to the STD Bus are not connected.

STD Bus Voltage Pin-Out

Pin	Description
1	+5 volts DC
2	+5 volts DC
3	Ground
4	Ground
55	+12 volts DC
56	-12 volts DC

SPECIFICATIONS

Electrical

Input Voltage
  12VDC (9 - 18 VDC): PS12T12
  24VDC (18 - 36 VDC): PS24T12
  48VDC (36 - 72 VDC): PS48T12

Output Voltage/Current
  +5VDC at 1500 mA
  +12VDC at 310 mA
  -12VDC at 310 mA

Mechanical
Dimensions: 4.5" x 6.5" x 1.0"

Connectors
Input Power: 4-pin Molex. Mates with AMP
               1-480424-0 housing and 60617-1 pins
Output Power: 56-pin STD Bus card edge

Environmental

Operational Temperature: -25° to +71°C

ORDERING INFORMATION

PS12T12 12 VDC input DC/DC supply
PS24T12 24 VDC input DC/DC supply
PS48T12 48 VDC input DC/DC supply

FEATURES

- Ground plane on component side for reduced noise operation
- Labeled test points on all lines for easy identification and connection to test equipment
- LED's on +5, +12, and -12 volt lines provide visual status indication of power buses.
- Push button reset onboard
- Card length: 7.75 inches

The STD-EXT is a high performance STD Bus and CMOS STD Bus extender card. It is designed to provide a low noise card extender for use in trouble shooting and debugging systems.

FUNCTIONAL CAPABILITY

Configuration - The STD-EXT is a 4.5 x 7.75 inch extender card that can be used to extend cards out of a card rack for easy access. All the STD Bus signals are routed through the card from the card edge to the right angle 56-pin connector. The connector is a gold plated, dual bifurcated bellows designed for high reliability and a good electrical connection.

The component side of the card is a ground plane to provide a low noise environment and a constant impedance for the signal lines. The power supply signal traces are wider for higher current capability.

Labeling - All points on the STD Bus are easily accessed and well labeled on the board's silkscreen for fast signal identification and examination. Signal headers are provided for convenient connections to test equipment for all data, address, control, power and ground lines. The length of the STD-EXT card allows it to be installed in a full card cage yet still provide access to the test points.

LED's - Three LED's are installed to provide a visual indication of the power supplies. A red, green, and yellow LED is used on the respective +5, +12, and -12 volt power lines.

PBRESET - An undebounced pushbutton reset switch is onboard for use in trouble shooting. It generates a low PBRESET* signal when depressed. It is recessed to prevent accidental triggering.
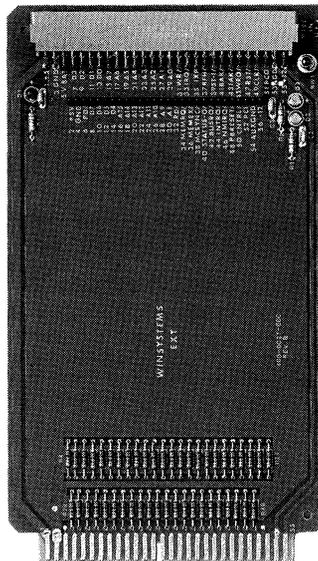
SPECIFICATIONS

Mechanical

Dimensions: 4.5 x 7.75 inches

PC Board: FR4 epoxy glass. Solder mask, screened component legend, and plated through holes

Connectors:

STD Bus: 56-pin dual 0.125" centers

Top extension: 56-pin dual bifurcated bellows 0.125" edge card connector

Environmental

Operating temperature: 0°C to +55°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

STD-EXT   Extender Board

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WinSystems, Inc.

WinSystems
STD BUS

FEATURES

- Permits addition of user designed circuitry for STD and CMOS STD Bus systems
- Access to all STD Bus lines and power buses
- Wire-wrap, point to point or flow soldering
- Processor independent
- Large breadboard area on 0.100" grid accepts standard DIP sockets, connectors and press-fit pins
- Plated through holes
- Provisions for bypass capacitors

The STD-WW2 is designed as a universal prototyping card for user application specific circuitry. It allows STD Bus and CMOS STD Bus users to construct experimental and custom I/O interfaces with a minimum of effort. A 0.100 inch grid is provided for the breadboard area that accepts standard DIP sockets, connectors, press-fit pins and discrete logic circuitry.
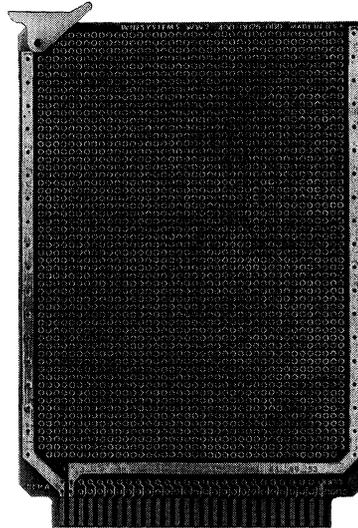
FUNCTIONAL CAPABILITY

Bus Interface - Full access is provided to the 56-pin STD Bus edge connector including address bus, data bus, control, and power. Connection points are provided from the Bus to the prototyping circuit area.

Configuration - A 6.1 x 4.5 inch prototyping breadboard area is available for application specific prototype and experimental circuit design. It consists of a 0.100 inch grid of 0.042 inch plated through holes that will accept 0.025 inch square posts, discrete components, standard 8, 14, 16, 24, 28, and 40-pin solder or wirewrap DIP sockets and connectors. The entire top of the card is available for installation of one or several 0.100" right angle connectors or headers at the edge.

Additionally the signal pads, power pads, and ground pads are labeled on the circuit side of the board for easy identification.

SPECIFICATIONS

Mechanical

Dimensions: Meets all STD Bus mechanical specifications; 4.5 x 6.5 inches

PC Board: FR4 epoxy glass with plated through 0.100 inch holes

Connectors

STD Bus: 56-pin dual 0.125" centers

ORDERING INFORMATION

STD-WW2   General purpose prototyping card

6

WinSystems, Inc.

Card Cages and Accessories

Card Cages

Accessories

7

FEATURES

- Available in 2-, 4-, 6-, 8-, 9-, 12-, 16-, and 21-slot versions
- Rugged alodine aluminum construction including end plates and mounting bars that won't rust
- High strength, precision-construction card cage configurations with backplanes on 0.75 inch spacing
- 50W and 100W power supplies available
- Self-lubricating card guides with retention tabs
- Three mounting configurations:
  - Wall Mount (for NEMA boxes)
  - Rack Mount (for rack enclosures)
  - Table Mount (for flat surface mounts)
- Excellent backplane design
  - Wide ground and power buses
  - Ground plane on assembly side
  - Supports STD Bus 16-bit data transfers
  - Power status LEDs
  - Vcc bypass capacitor at each connector
  - Optional powerfail detect/brown-out circuit
  - Backplane mounting made on the connectors not to the PC board
  - Gold-plated bellows card edge connectors
  - PCI/PCO jumpers per connector
  - Multiple backplanes supported in a card rack
- Accepts CMOS STD Bus cards
- Optional hold down bar and transorbs
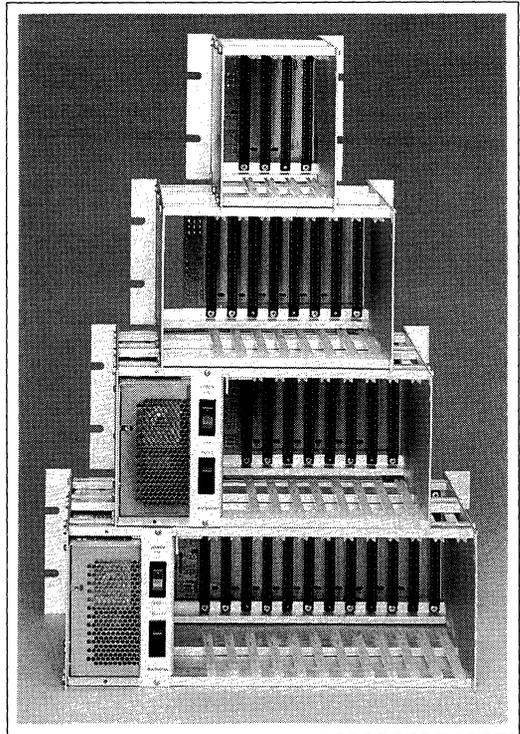
WinSystems' offers a broad line of motherboards, assembled card cages and card cages with power supplies. The card racks and backplanes are available from 2 to 21 slots and are ideal for high performance and demanding STD Bus applications. Specify the size and type of card cage, the number of motherboards and power supply, and WinSystems will ship you a completely assembled and fully tested card cage system.

Motherboards - WinSystems' STD Bus motherboards are available in eight different versions from 2 to 21 slots. Spacing is on 0.75 inch centers. The motherboards support both STD and CMOS STD Bus cards with no termination required.

Card Cages - WinSystems' STD Bus card cages are ideal for industrial environments. The design is based on field-proven engineering techniques in order to offer the highest integrity and reliability. Spacing is on 0.75 inch centers with a vertical card orientation to take advantage of convection cooling. They are constructed of aluminum for light weight and strength.

Power Supplies - Two types of high efficiency switching power supplies are available for the card cages: 50W and 100W. They are available in a number of different configurations for both embedded and DOS compatible systems.

Enclosures - WinSystems also offers a 19" instrument case for use with STD Bus DOS or embedded systems. It is an excellent technical design with high functionality with an aesthetically pleasing two-tone beige finish.

Custom Configurations - Multiple motherboards and other options can be installed in a card cage to allow more that one system to occupy a single container. To configure and price a custom motherboard or assembly, contact the WinSystems' factory with your specifications.

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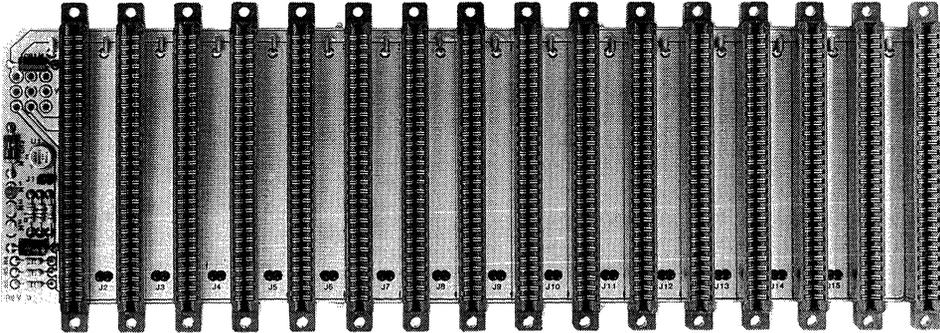
MOTHERBOARDS

16 Slot Motherboard with Power Fail Reset, Transorbs and LEDs

Backplane - The foundation of any multi-board system is the backplane. WinSystems' backplane has been designed for high performance STD Bus processors. They can work with all the processors including the new high performance 16/32-bit processors with full 16-bit data transfers. The assembly side of the backplane is a groundplane which reduces noise and crosstalk on the signal lines. It also provides a constant characteristic impedance necessary for good transmission line design. The signal lines are narrow to reduce adjacent channel coupling.

Each of the STD Bus connectors has a bypass capacitor for Vcc. Wide ground and power traces are used to improve power distribution and reduce the instantaneous voltage shifts due to inductance of the traces.

The motherboard has solder pads on a 3 by 3 grid that will accept up to #16 AWG wire for direct wiring or the WinSystems' cable assembly using a standard Molex 9-pin connector. The Molex connectors, number 03-09-1092 and 03-09-1093 are common industry standard parts. In addition to power and ground, an external battery voltage (VBAT), DC power down signal (DCPD*) inputs are supplied to the backplane through the power connector. Individual motherboards are shipped without a power cable for maximum configuration flexibility.

GND and AUX GND are isolated to allow configuration flexibility and to minimize error voltages due to common ground impedances.

Status LEDs - Three light emitting diodes (LEDs) are on each motherboard to visually indicated the presence or absence of each of the power supply voltages. A different color is assigned to each voltage for easy

Pin	Description
1	+5 volts DC
2	Logic Ground
3	VBAT/VBB#1
4	-12 volts DC
5	Logic Ground
6	DCPD*/VBB#2
7	+12 volts DC
8	AUX Ground
9	PBRESET*

and instant status recognition. Red is assigned to +5VDC, green is assigned to +12VDC, and yellow is assigned to -12VDC.

Connectors - The heart of an interconnect system is the edge card connector itself. WinSystems uses only UL approved connectors with gold-plated bifurcated bellows contacts. They are superior to cantilever beam connectors since they provide two beam contacts with two independent spring members and a constant spring tension on the card edge. The contact design enables the connector to have a lower insertion force, a higher withdrawal force and a higher, more consistent normal force. This translates to higher reliability and a better connection since it can absorb load deflection of a card while maintaining sufficient contact force for good electrical connection. Maximum reliability of the bellows connector is assured through superior contact tolerance through environmental stresses including shock, vibration, temperature and humidity variations. Other parameters such as insulation resistance, contact resistance, durability and contact separation force meet all of industry's (and applicable military) specifications for reliability.

Interrupts - If a card slot is not used, the user can maintain the PCI/PCO priority interrupt chain by jumpering terminal points adjacent to each connector provided on the assembly side of each backplane. The highest interrupt priority on all card cages and backplanes start at slot 1 which is adjacent to the power connector. The PCI/PCO interrupt chain is typically only used for Z80 and HD64180 based systems.

Reset - An optional jumper selectable powerfail and brown-out detection circuit is offered on all the backplanes and card cages. A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This is critically important in order to detect brown-out or powerfail conditions in remote or unattended applications since a microprocessor will act erratically before it shuts down. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on-reset.

A special suffix is assigned to the card cages only to make the ordering code simpler for Option 3. A "P" suffix replaces the last letter of the ordering code. For example, a four slot wall mount card cage with the power-fail-reset circuit changes from CC4-WM to CC4-WP.

You do not need to order the power-on-reset option if you are using WinSystems' CPUs or single board computers with the motherboards and card racks since this ciruit is resident on our boards.

Transient Protection - Optional transient protection is provided on the +5, +12, and -12 volt lines for spike and surge suppression. This is listed as Option 1 for any motherboard, card cage or powered rack.

ORDERING INFORMATION

MB2	2 slot motherboard
MB4	4 slot motherboard
MB6	6 slot motherboard
MB8	8 slot motherboard
MB9	9 slot motherboard
MB12	12 slot motherboard
MB16	16 slot motherboard
MB21	21 slot motherboard
Option 1	Add 3 transorbs on power lines

MODEL NO.	NO. SLOTS	A DIM.	B DIM.
MB2	2	2.05	0.75
MB4	4	3.55	2.25
MB6	6	5.05	3.75
MB8	8	6.55	5.25
MB9	9	7.30	6.00
MB12	12	9.55	8.25
MB16	16	12.55	11.25
MB21	21	16.20	15.00

.128 DIA HOLE THRU CONNECTOR (2)PLCS.
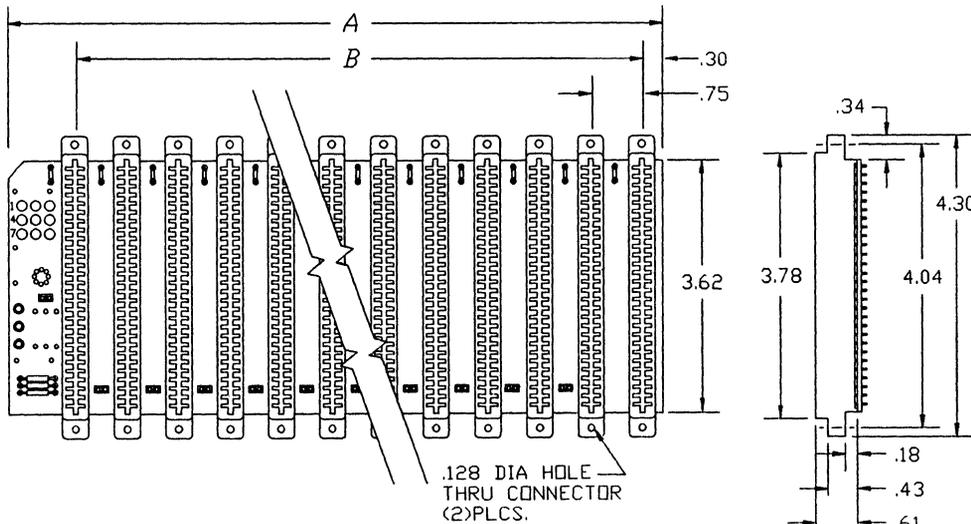
CARD CAGES

Card Cages - The card cages are made from extruded alodine aluminum for the end plates, guide rails and connector rails. This offers both high strength and light weight. The card guides are made from high grade nylon and are self-lubricating, nonconductive, and provide isolation for cards and their components from shock and vibration. The guide tracks have integral card retention tabs to insure a secure fit.

The appropriate WinSystems' motherboard is mounted to the card cage by riveting the connectors to the metal chassis. The connector housing accepts the insertion and withdrawal forces rather than the backplane PCB which adds reliability to the system.

Card Rack Mounting Versatility - Three mounting configurations are available: Rack mount (RM), Table mount with side entry (SE), and Wall mount (WM). All cards cages are supplied with a high performance motherboard and a 6" male power plug.
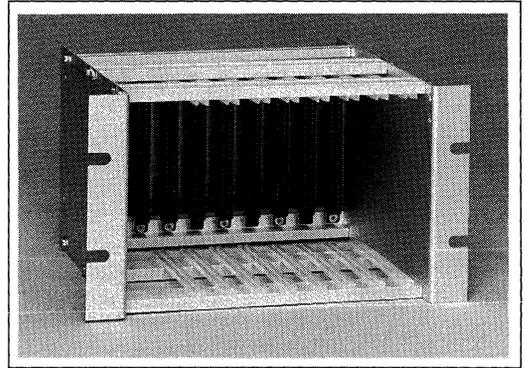
8 Slot Rack Mount Card Cage

The rack mount version uses standard 5.25 inch flanges on all models that allows the card rack to be supported from the front. The table top version allows card racks to be supported by the bottom. The wall mount units are designed to mount to the rear vertical panel of an enclosure.
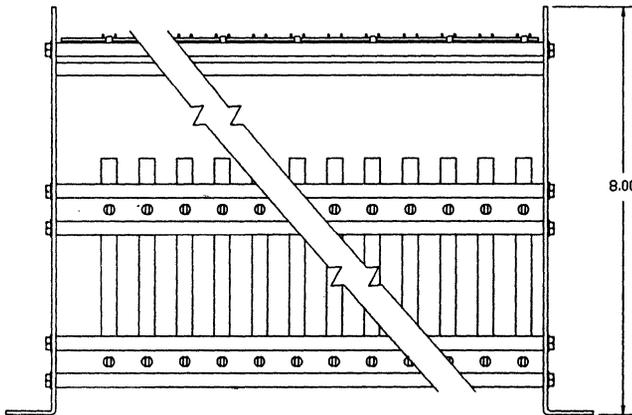
CARD CAGE
RACK MOUNT

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-RM	2	4.20	2.20	0.75
CC4-RM	4	5.70	3.70	2.25
CC6-RM	6	7.50	5.50	3.75
CC8-RM	8	9.50	7.50	5.25
CC9-RM	9	9.50	7.50	6.00
CC12-RM	12	11.70	9.70	8.25
CC16-RM	16	19.00	17.00	11.25
CC21-RM	21	19.00	17.00	15.00
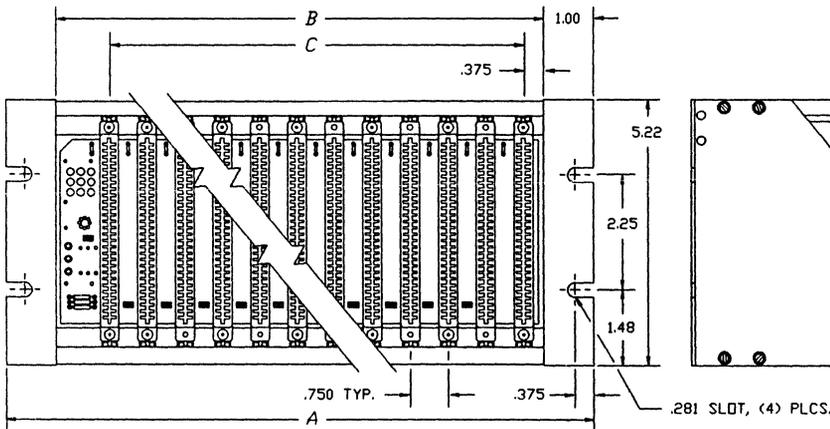
Card Access - All cards are on a 0.75" centers with a vertical orientation to allow maximum convection air circulation.

Termination - Good backplane design involves both an understanaing of high frequency RF, plus good grounding and layout techniques. WinSystems' card cages and motherboards do not require RC passive termination networks and we do not recommend their use. CMOS STD Bus cards should not be used in terminated backplane systems because of the capacitive loading on the bus transceivers.

The "termination networks" offered by some vendors are nothing more than RC filters. These filters are not desirable since they introduce 100 pF to 200 pF of unwanted capacitance which will skew the control, address, and data signals. Also, the extra capacitive loading of the termination networks degrade a system's performance.

Multiple Buses - For distributed processing applications, multiple backplanes can be mounted in a single card rack. This allows more than one STD Bus
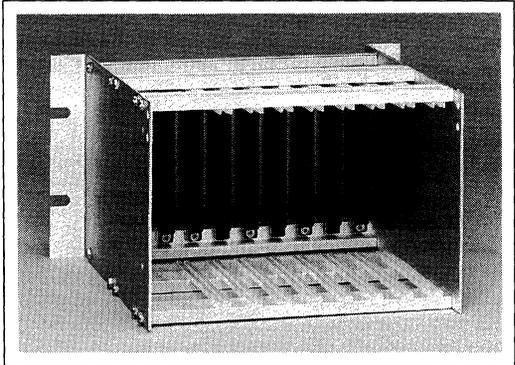
8 Slot Wall Mount Card Cage with Hold Down Bar

controller to reside in a single enclosure. Call WinSystems for exact configurations and specifications.

Hold down bar - An optional latching bar is available to provide additional card restraint. It consists of a 1/4 inch square bar with pins in each end. One of the pins is spring loaded to allow the bar to be installed
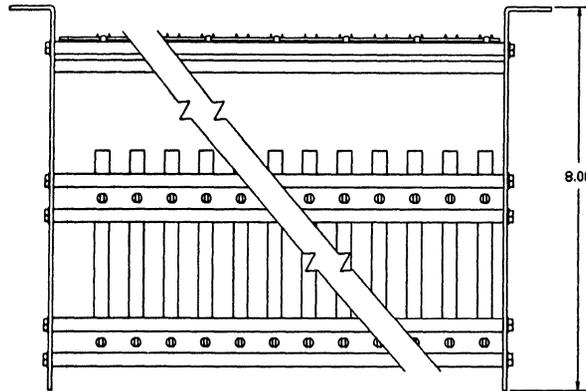
CARD CAGE
WALL MOUNT

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-WM	2	4.20	2.20	0.75
CC4-WM	4	5.70	3.70	2.25
CC6-WM	6	7.50	5.50	3.75
CC8-WM	8	9.50	7.50	5.25
CC9-WM	9	9.50	7.50	6.00
CC12-WM	12	11.70	9.70	8.25
CC16-WM	16	19.00	17.00	11.25
CC21-WM	21	19.00	17.00	15.00
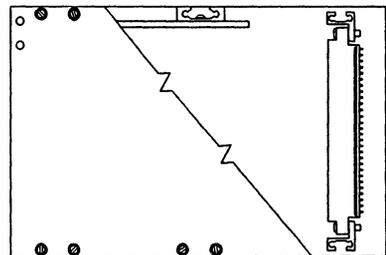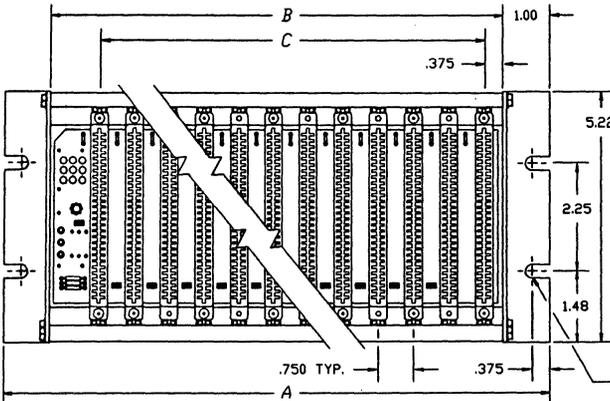
or removed. A knurled finger screw provides a method to securely lock the bar in place. It fastens at both ends of the card cage and then horizontally across the STD Bus card's ejector to hold the cards firmly in the card cage.

Pin-and-Socket Connectors - WinSystems will optionally supply MIL-C-55302/58 type polarized connectors on the backplane instead of card edge connectors for the XIM Series' STD Bus product line. This permits the card cages and backplanes to be used with STD Bus cards that use the pin-and-socket interconnect system. These connectors are superior to DIN-type connectors yet are compatible with WinSystems' XIM series' STD Bus cards. Contact the factory for more information.

19" Rack Mounting - WinSystems' rack mount card cage width varies directly as a function of the number of slots in the backplane. If you desire a rack mount card cage that will fit into a 19" rack regardless of the size of the backplane, then specify Option 4 to fix the "A" dimension at 19 inches. For example, the CC4-RM
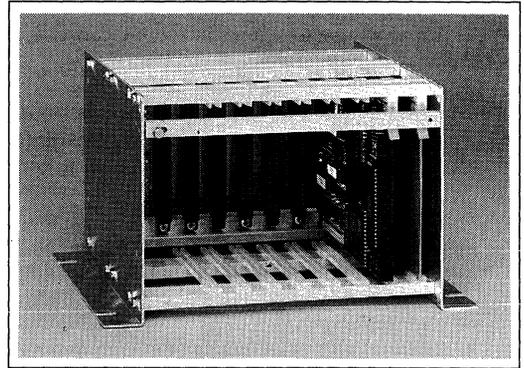
8 Slot Side Entry Card Cage

with Option 4, has a dimension of 5.22" x 19" x 8" rather than 5.22" x 5.7" x 8". The backplane will be left justified within the card cage. Option 4 is valid for rack mount card cages both with and without power supplies.
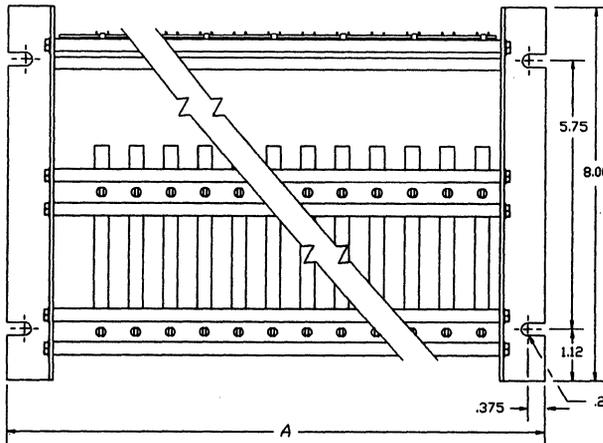
CARD CAGE
SIDE ENTRY

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-SE	2	4.20	2.20	0.75
CC4-SE	4	5.70	3.70	2.25
CC6-SE	6	7.50	5.50	3.75
CC8-SE	8	9.50	7.50	5.25
CC9-SE	9	9.50	7.50	6.00
CC12-SE	12	11.70	9.70	8.25
CC16-SE	16	19.00	17.00	11.25
CC21-SE	21	19.00	17.00	15.00
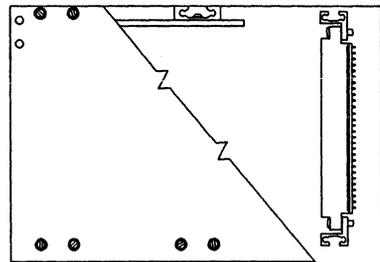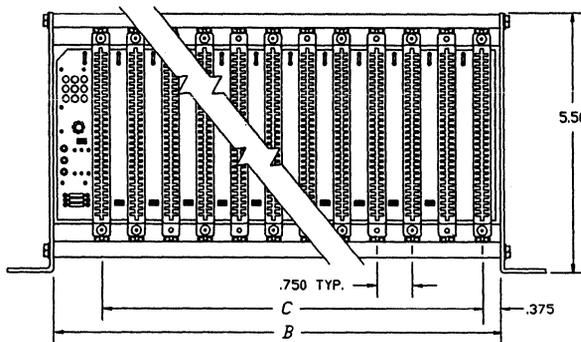
ORDERING INFORMATION

Model	Slots	Mounting Style	Powerfail
CC2-RM	2	Rack Mount	No
CC2-RP	2	Rack Mount	Yes
CC2-SE	2	Table Mount	No
CC2-SP	2	Table Mount	Yes
CC2-WM	2	Wall Mount	No
CC2-WP	2	Wall Mount	Yes
CC4-RM	4	Rack Mount	No
CC4-RP	4	Rack Mount	Yes
CC4-SE	4	Table Mount	No
CC4-SP	4	Table Mount	Yes
CC4-WM	4	Wall Mount	No
CC4-WP	4	Wall Mount	Yes
CC6-RM	6	Rack Mount	No
CC6-RP	6	Rack Mount	Yes
CC6-SE	6	Table Mount	No
CC6-SP	6	Table Mount	Yes
CC6-WM	6	Wall Mount	No
CC6-WP	6	Wall Mount	Yes
CC8-RM	8	Rack Mount	No
CC8-RP	8	Rack Mount	Yes
CC8-SE	8	Table Mount	No
CC8-SP	8	Table Mount	Yes
CC8-WM	8	Wall Mount	No
CC8-WP	8	Wall Mount	Yes
CC9-RM	9	Rack Mount	No
CC9-RP	9	Rack Mount	Yes
CC9-SE	9	Table Mount	No
CC9-SP	9	Table Mount	Yes
CC9-WM	9	Wall Mount	No
CC9-WP	9	Wall Mount	Yes
CC12-RM	12	Rack Mount	No
CC12-RP	12	Rack Mount	Yes
CC12-SE	12	Table Mount	No
CC12-SP	12	Table Mount	Yes
CC12-WM	12	Wall Mount	No
CC12-WP	12	Wall Mount	Yes
CC16-RM	16	Rack Mount	No
CC16-RP	16	Rack Mount	Yes
CC16-SE	16	Table Mount	No
CC16-SP	16	Table Mount	Yes
CC16-WM	16	Wall Mount	No
CC16-WP	16	Wall Mount	Yes
CC21-RM	21	Rack Mount	No
CC21-RP	21	Rack Mount	Yes
CC21-SE	21	Table Mount	No
CC21-SP	21	Table Mount	Yes
CC21-WM	21	Wall Mount	No
CC21-WP	21	Wall Mount	Yes

HDB-4	4-Slot Hold Down Bar
HDB-6	6-Slot Hold Down Bar
HDB-8	8-Slot Hold Down Bar
HDB-12	12-Slot Hold Down Bar
HDB-16/21	16/21-Slot Hold Down Bar

Option 1   Add 3 transorbs on power lines
Option 4   Standard 19" rack width

POWERED RACKS

Power Supplies - WinSystems offers card cages with 50W and 100W power supplies. These are triple output supplies that mount inside the card cage and generate DC output voltages from the AC mains. These are high efficiency, highly reliable switching power supplies. An ON/OFF switch and momentary Reset switch are mounted on a panel for operator convenience. All units are fused and are equipped with a US standard 3-prong power cord with plug.

All powered card cages are supplied with a WinSystems' high performance motherboard and status LEDs.

Card Rack Mounting Configuration - Three mounting configurations are available for the card cages with power supplies: Rack mount (RM), Table mount with side entry (SE), and Wall mount (WM). The dimensions are longer for the powered racks to accomodate for mounting the power supplies inside the racks. For this reason, a 21 slot card cage configuration with power supply cannot be manufactured and stay within the 19" length. Contact the factory if you would like a special configuration with the power supply on the back of the rack.
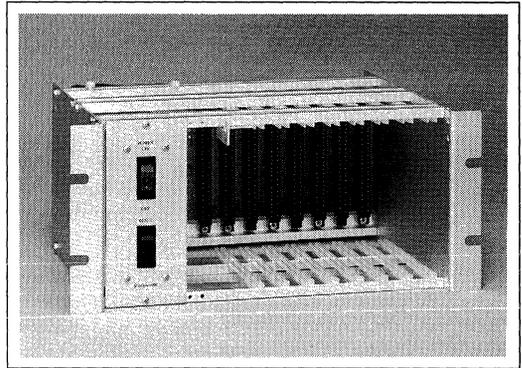
8 Slot Rack Mount Card Cage with 50W Supply

50 Watt Supply - The PS50 is a triple output, 50 Watt power supply. It is designed for CMOS STD Bus or small systems configurations. Although it has a standard 3 prong AC cable, it is a universal input switching design. Universal input voltage eliminates the need for an external 115/220 VAC system switch thereby eliminating failures due to improper input voltage. It will operate from 47 Hz to 440 Hz.
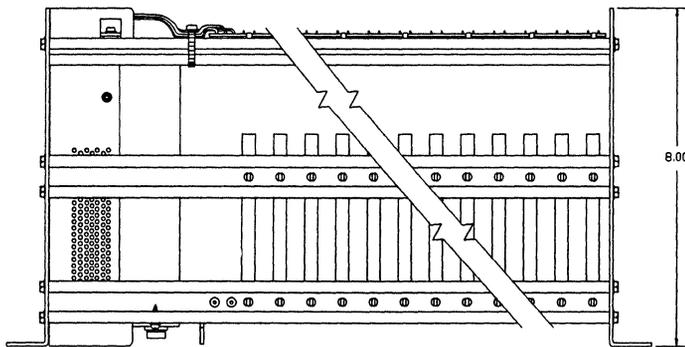
CARD CAGE
RACK MOUNT W/POWER SUPPLY

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-RM-PSXX	2	7.90	5.90	0.75
CC4-RM-PSXX	4	9.40	7.40	2.25
CC6-RM-PSXX	6	11.20	9.20	3.75
CC8-RM-PSXX	8	12.25	10.25	5.25
CC12-RM-PSXX	12	15.40	13.40	8.25
CC16-RM-PSXX	16	19.00	17.00	11.25

PSXX PS50 - 50 WATT POWER SUPPLY
PS100 - 100 WATT POWER SUPPLY
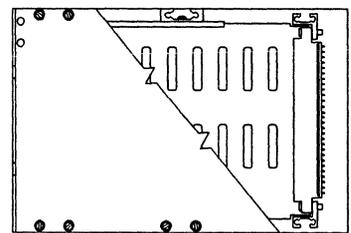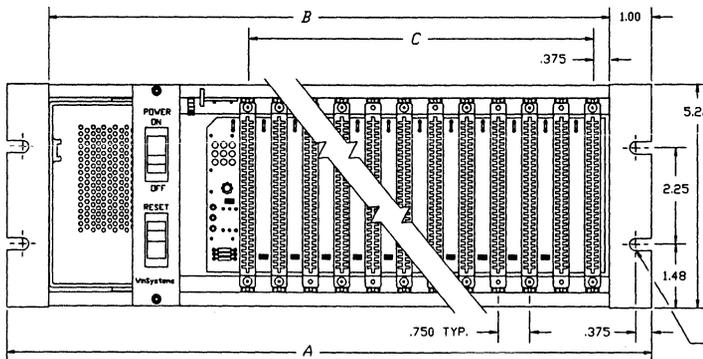
The PS50 is a zero current switcher. It will maintain regulation on all the output voltages down to zero current thus eliminating the need for load resistors at light loads. This makes it ideal for CMOS applications yet there is enough current available for a small DOS system.

The PS50 has overvoltage protection and output short circuit protection. The power supply is convection cooled and should be derated from 50° to 70°C to 25W. The power supply is very reliable with a MTBF of 160,000 hours.

PS50 OUTPUT CHARACTERISTICS

Voltage	Minimum	Maximum
+5	0A	5.0A
+12	0A	2.0A
-12	0A	0.5A

100 Watt power supply - The PS100 is a triple output, high efficiency, 100 Watt power supply. It is designed for medium to large systems configurations. It is a universal input voltage switcher that accepts 85VAC to 264VAC and will work from 47Hz to 63Hz.
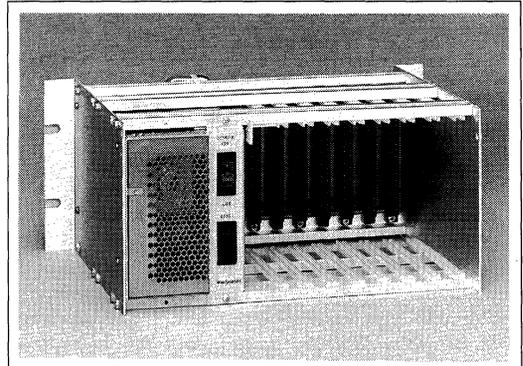
8 Slot Wall Mount Card Cage with 100W Power Supply

The PS100 is a zero current switching power supply that requires no minimum load to maintain regulation on all output voltages lines. It has both overvoltage protection and output short circuit protection.
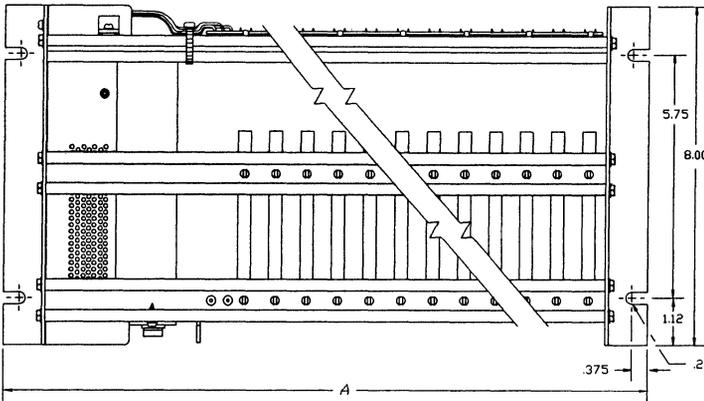
CARD CAGE
SIDE ENTRY W/POWER SUPPLY

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-SE-PSXX	2	7.90	5.90	0.75
CC4-SE-PSXX	4	9.40	7.40	2.25
CC6-SE-PSXX	6	11.20	9.20	3.75
CC8-SE-PSXX	8	12.25	10.25	5.25
CC12-SE-PSXX	12	15.40	13.40	8.25
CC16-SE-PSXX	16	19.00	17.00	11.25

PSXX PS50 - 50 WATT POWER SUPPLY
PS100 - 100 WATT POWER SUPPLY

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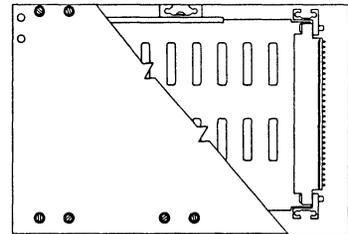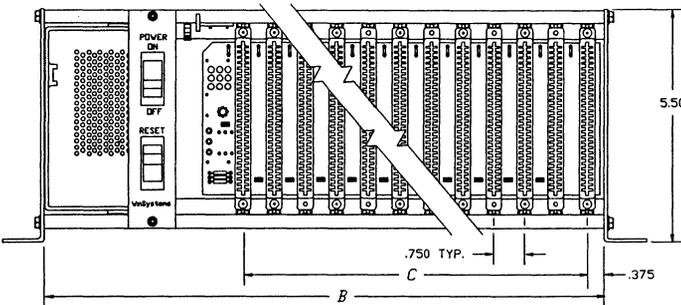
PS100 OUTPUT CHARACTERISTICS

Voltage	Minimum	Maximum
+5	0A	10.0A
+12	0A	3.0A
-12	0A	0.5A

Dimension - The same amount of room is allocated for the power supply for both 50W and 100W power ranges. Therefore the mechanical drawings for the Rack Mount, Wall Mount, and Side Entry reflect no additional room required. The difference is that with the 50W supply, the ON/OFF switch and Reset switch is integral in the power enclosure. The 100W model has an enclosed bracket with the ON/OFF and Reset switch mounted there.

Part Number Assignment - A suffix is added to the standard card cage model number to designate the specific model power supply integrated into the rack.

A PS50 suffix denotes the 50W power supply and a PS100 denotes a 100W power supply. For example a CC8-WM-PS50 designates a 8 slot wall mount card cage with the 50 Watt power supply installed.
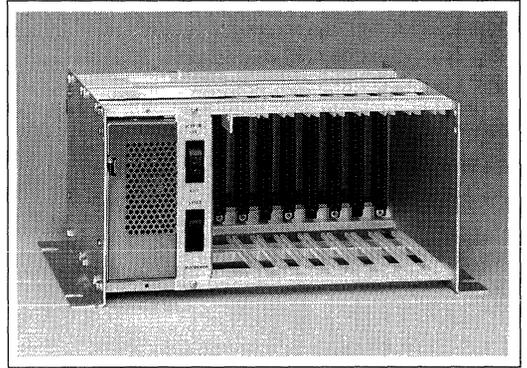
8 Slot Side Entry Card Cage with 100W Supply

Options - Two options are available for the powered card racks. Option 1 consists of installing three transorbs and Option 4 specifies the rack width at 19".
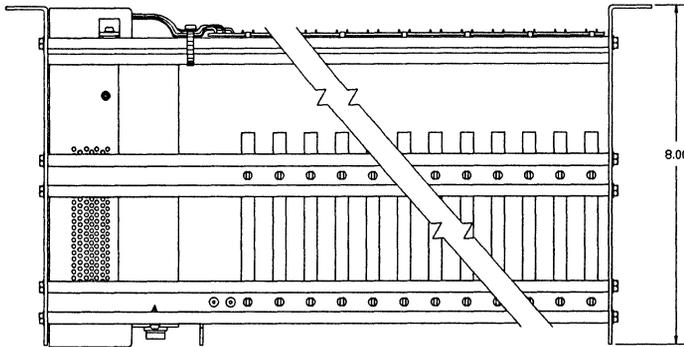
CARD CAGE
WALL MOUNT W/POWER SUPPLY

MODEL NO.	NO. SLOTS	A DIM.	B DIM.	C DIM.
CC2-WM-PSXX	2	7.90	5.90	0.75
CC4-WM-PSXX	4	9.40	7.40	2.25
CC6-WM-PSXX	6	11.20	9.20	3.75
CC8-WM-PSXX	8	12.25	10.25	5.25
CC12-WM-PSXX	12	15.40	13.40	8.25
CC16-WM-PSXX	16	19.00	17.00	11.25

PSXX PS50 - 50 WATT POWER SUPPLY
PS100 - 100 WATT POWER SUPPLY
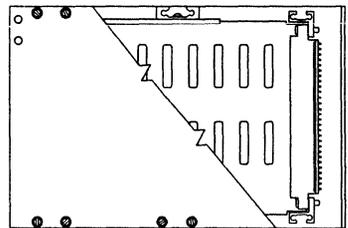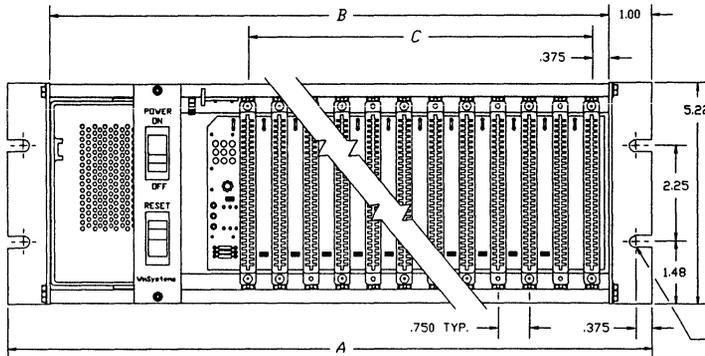
ORDERING INFORMATION

Model	Slots	Mounting Style	Power Supply
CC2-RM-PS50	2	Rack Mount	50W
CC2-SE-PS50	2	Table Mount	50W
CC2-WM-PS50	2	Wall Mount	50W
CC4-RM-PS50	4	Rack Mount	50W
CC4-SE-PS50	4	Table Mount	50W
CC4-WM-PS50	4	Wall Mount	50W
CC6-RM-PS50	6	Rack Mount	50W
CC6-RM-PS100	6	Rack Mount	100W
CC6-SE-PS50	6	Table Mount	50W
CC6-SE-PS100	6	Table Mount	100W
CC6-WM-PS50	6	Wall Mount	50W
CC6-WM-PS100	6	Wall Mount	100W
CC8-RM-PS50	8	Rack Mount	50W
CC8-RM-PS100	8	Rack Mount	100W
CC8-SE-PS50	8	Table Mount	50W
CC8-SE-PS100	8	Table Mount	100W
CC8-WM-PS50	8	Wall Mount	50W
CC8-WM-PS100	8	Wall Mount	100W
CC12-RM-PS50	12	Rack Mount	50W
CC12-RM-PS100	12	Rack Mount	100W
CC12-SE-PS50	12	Table Mount	50W
CC12-SE-PS100	12	Table Mount	100W
CC12-WM-PS50	12	Wall Mount	50W
CC12-WM-PS100	12	Wall Mount	100W
CC16-RM-PS50	16	Rack Mount	50W
CC16-RM-PS100	16	Rack Mount	100W
CC16-SE-PS50	16	Table Mount	50W
CC16-SE-PS100	16	Table Mount	100W
CC16-WM-PS50	16	Wall Mount	50W
CC16-WM-PS100	16	Wall Mount	100W
CC21-RM-PS100	21	Rack Mount	100W
CC21-SE-PS100	21	Table Mount	100W
CC21-WM-PS100	21	Wall Mount	100W

Option 1 Add 3 transorbs on power lines
Option 4 Standard 19″ rack width

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Motherboard and Card Cage Quick Reference

SLOTS	MOTHERBOARDS Only	RACK MOUNT		WALL MOUNT		SIDE ENTRY	
		With Power Supply	Without Power Supply	With Power Supply	Without Power Supply	With Power Supply	Without Power Supply
2	MB2	CC2-RM-PS50	CC2-RM CC2-RP	CC2-WM-PS50	CC2-WM CC2-WP	CC2-SE-PS50	CC2-SE CC2-SP
4	MB4	CC4-RM-PS50	CC4-RM CC4-RP	CC4-WM-PS50	CC4-WM CC4-WP	CC4-SE-PS50	CC4-SE CC4-SP
6	MB6	CC6-RM-PS50 CC6-RM-PS100	CC6-RM CC6-RP	CC6-WM-PS50 CC6-WM-PS100	CC6-WM CC6-WP	CC6-SE-PS50 CC6-SE-PS100	CC6-SE CC6-SP
8	MB8	CC8-RM-PS50 CC8-RM-PS100	CC8-RM CC8-RP	CC8-WM-PS50 CC8-WM-PS100	CC8-WM CC8-WP	CC8-SE-PS50 CC8-SE-PS100	CC8-SE CC8-SP
9	MB9	—	CC9-RM CC9-RP	—	CC9-WM CC9-WP	—	CC9-SE CC9-SP
12	MB12	CC12-RM-PS50 CC12-RM-PS100	CC12-RM CC12-RP	CC12-WM-PS50 CC12-WM-PS100	CC12-WM CC12-WP	CC12-SE-PS50 CC12-SE-PS100	CC12-SE CC12-SP
16	MB16	CC16-RM-PS50 CC16-RM-PS100	CC16-RM CC16-RP	CC16-WM-PS50 CC16-WM-PS100	CC16-WM CC16-WP	CC16-SE-PS50 CC16-SE-PS100	CC16-SE CC16-SP
21	MB21	CC21-RM-PS100	CC21-RM CC21-RP	CC21-WM-PS100	CC21-WM CC21-WP	CC21-SE-PS100	CC21-SE CC21-SP

WinSystems, Inc.

FEATURES

- 3, 6, 9, 12, 15, 18, 21, 24, and 26-slot versions
- Available as backplanes, card cages and powered racks with 5/8" spacing
- Compact design for easy mounting in cramped locations
- Accommodates multiple backplanes within a single card cage
- Rugged aladine aluminum construction including end plates and mounting bars that won't rust
- 50W and 100W switching power supplies available
- Self-lubricating card guides with retention tabs
- Three mounting configurations:
  - Wall Mount (for NEMA boxes)
  - Rack Mount (for racks enclosures)
  - Table Mount (for flat surface mounts)
- Excellent backplane design
  - Wide ground and power buses
  - Ground plane on assembly side
  - Supports STD Bus 16-bit data transfers
  - Power status LEDs
  - Screw terminals on 0.2-inch centers for power cable connections
  - Optional transorbs supported for transient protection on the backplane
  - Backplane mounting made on the connectors not to the PC board
  - Gold-plated bellows card edge connectors
- Accepts CMOS STD Bus cards
- Optional card restraint for shock and vibration
- Replaces Pro-Log's BX series card cages

Often for embedded industrial applications, space is at a premium so that the physical size of the instrument can be held to a minimum. The CX series of STD Bus card racks and backplanes fulfills this demand. Based upon 0.625" centers with vertical card orientation to take advantage of convection cooling, the CX card cages allow either a smaller enclosure size or provides more card slots when compared to a 0.75" spacing.

WinSystems offers a broad line of backplanes, assembled card cages and card cages with power supplies from 3 to 26 slots for housing STD Bus and CMOS STD Bus cards. They are ideal for high performance and demanding STD Bus applications. Specify the size and type of card cage, the number of backplanes and power supply, and WinSystems will ship you a completely assembled and fully tested card cage system.

Custom Configurations - Multiple backplanes and other options can be installed in a card cage to allow
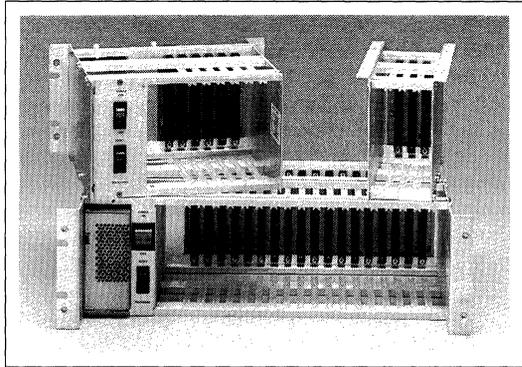
more than one system to occupy a single container. To configure and price a custom backplane or assembly, contact the WinSystems' factory with your specifications.

BACKPLANES

Backplanes - WinSystems' STD Bus backplanes are available in nine different versions from 3 to 26 slots. Spacing between cards is 0.625 inch on centers. Multiple backplanes can be installed in a single card cage. The design and construction allows them to support both STD and CMOS STD Bus cards with no termination required.

WinSystems' backplanes are designed for high performance STD Bus processors. They can work with all the processors including the new high performance 16/32-bit processors with full 16-bit data transfers.

Power Distribution - Except on the BP3, the backplanes have multiple terminal blocks available for power. They have multiple connections on the terminal blocks for GND and +5V to allow use of remote supply sense or redundant leads. GND and AUX GND are isolated to allow configuration flexibility and to minimize error voltages due to common ground impedances. Jumper locations are available for connecting the two.

Status LEDs - Three light emitting diodes (LEDs) are on each backplane to visually indicate the presence or absence of each of the power supply voltages. A different color is assigned to each voltage for easy and instant status recognition. Red is assigned to +5VDC, green is assigned to +12VDC, and yellow is assigned to -12VDC.

7

Connectors - The heart of an interconnect system is the edge card connector itself. WinSystems uses only UL approved connectors with gold-plated bifurcated bellows contacts. This translates to higher reliability and a better connection since it can absorb load deflection of a card while maintaining sufficient contact force for good electrical connection. Maximum reliability of the bellows connector is assured through superior contact tolerance through environmental stresses including shock, vibration, temperature and humidity variations. Other parameters such as insulation resistance, contact resistance, durability and contact separation force meet all of industry's (and applicable military) specifications for reliability.

Transient Protection - Optional transient protection is provided by adding transorbs on the +5, +12, and -12 volt lines for spike and surge protection. This is listed as OPT 1 for any backplane, card cage or powered rack.

ORDERING INFORMATION

Model	Slots
BP3	3 slot backplane
BP6	6 slot backplane
BP9	9 slot backplane
BP12	12 slot backplane
BP15	15 slot backplane
BP18	18 slot backplane
BP21	21 slot backplane
BP24	24 slot backplane
BP26	26 slot backplane
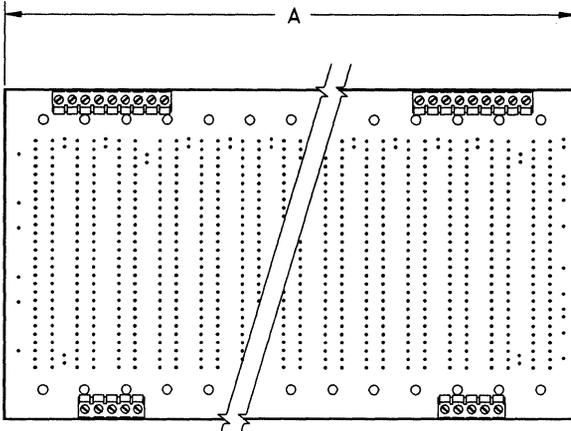
MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS	
		A	B
BP3	3	2.300	1.250
BP6	6	4.175	3.125
BP9	9	6.050	5.000
BP12	12	7.925	6.875
BP15	15	9.825	8.750
BP18	18	11.700	10.625
BP21	21	13.575	12.500
BP24	24	15.450	14.375
BP26	26	16.700	15.625
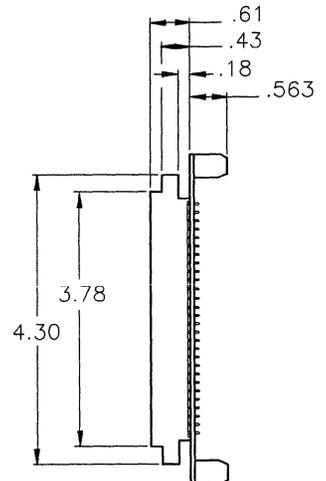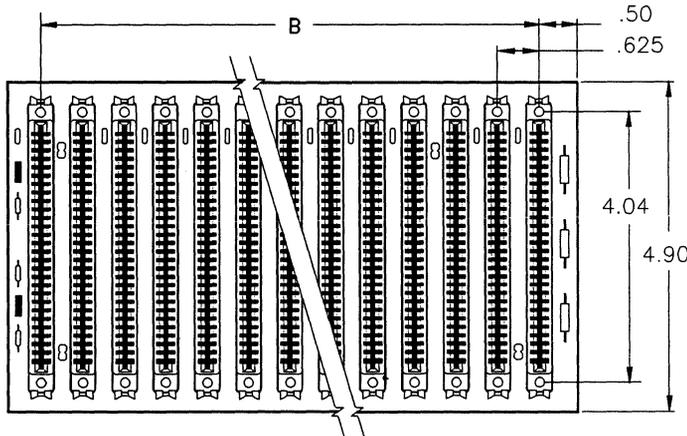
BACKPLANE
5/8" CARD CENTERS

BP-X

CARD CAGES

Rugged, Compact Construction - WinSystems' CX series of card cages are based on field-proven engineering techniques which offer the highest integrity and reliability. Constructed from extruded anodized aluminum for the end plates, guide rails, and connector rails, these racks give manufacturers the ruggedized enclosures required for industrial applications. Aluminum is lighter than steel and will not rust. The card guides are made from high-grade nylon and are self-lubricating, nonconductive, and provide isolation for cards and their components from shock and vibration. The guide tracks have integral card retention tabs to insure a secure fit.

The appropriate WinSystems' backplane is mounted to the card cage by riveting the connectors to the metal chassis. The connector housing accepts the insertion and withdrawal forces rather than the backplane PCB which adds reliability to the system.

Card Rack Mounting Versatility - Three mounting configurations are available — rack, table, and wall mount for flexibility in cramped locations.

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS		
		A	B	C
CX03-R	3	4.62	2.66	1.250
CX06-R	6	6.50	4.54	3.125
CX09-R	9	8.37	6.41	5.000
CX12-R	12	10.25	8.29	6.875
CX15-R	15	12.12	10.16	8.750
CX18-R	18	14.00	12.04	10.625
CX21-R	21	15.87	13.91	12.500
CX24-R	24	17.75	15.79	14.375
CX26-R	26	19.00	17.04	15.625

RACK MOUNT CARD CAGE ASSEMBLY
5/8" CARD CENTERS

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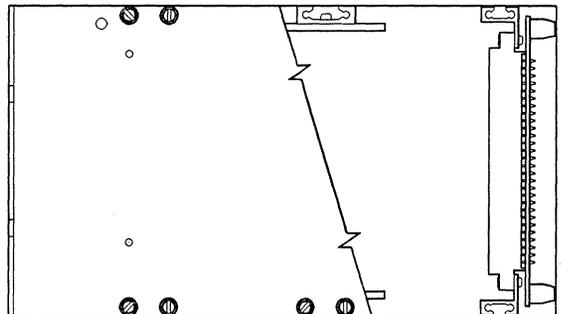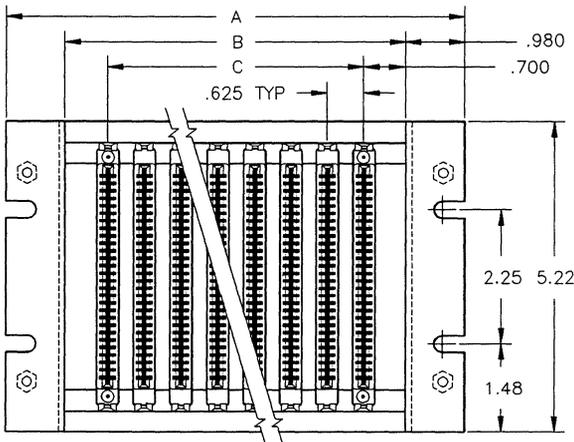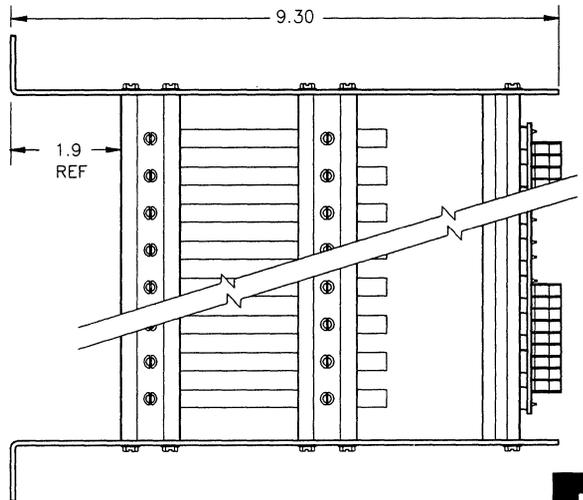
The "R" (rack mount) version has the card cage supported from standard 5.25" flanges on the front of the unit. The "W" (wall mount) version has the flanges mounted in the rear for mounting to a vertical panel of an enclosure. The "T" (table) version has the flanges on the bottom of the card cage. All cards cages are supplied with a WinSystems' high performance backplane.

Card Access - All cards are on a 0.625" centers with a vertical orientation to allow maximum convection air circulation.

Termination - Good backplane design involves both an understanding of high frequency RF, plus good grounding and layout techniques. WinSystems' card cages and backplanes do not require RC passive termination networks and we do not recommend their use. CMOS STD Bus cards should not be used in terminated backplane systems because of the capacitive loading on the bus transceivers.

The "termination networks" offered by some vendors are nothing more than RC filters. These filters are not desirable since they introduce 100 pF to 200 pF of unwanted capacitance which will skew the control, address, and data signals. Also, the extra capacitive loading of the termination networks degrade a system's performance.

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS		
		A	B	C
CX03-W	3	4.62	2.66	1.250
CX06-W	6	6.50	4.54	3.125
CX09-W	9	8.37	6.41	5.000
CX12-W	12	10.25	8.29	6.875
CX15-W	15	12.12	10.16	8.750
CX18-W	18	14.00	12.04	10.625
CX21-W	21	15.87	13.91	12.500
CX24-W	24	17.75	15.79	14.375
CX26-W	26	19.00	17.04	15.625
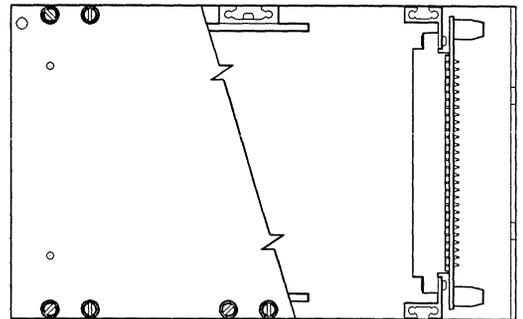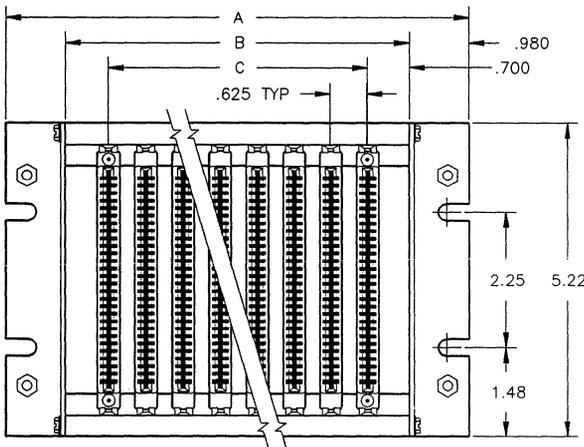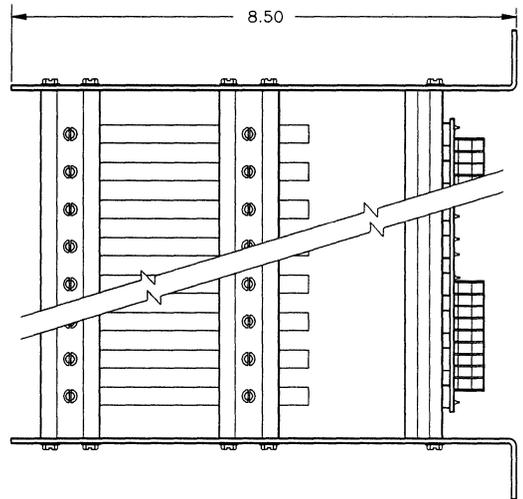
WALL MOUNT CARD CAGE ASSEMBLY
5/8" CARD CENTERS

Multiple Buses - For distributed processing applications, multiple backplanes can be mounted in a single card rack. This allows more than one STD Bus controller to reside in a single enclosure. Call WinSystems for exact configurations and specifications.

Hold down bar - An optional latching bar is available to provide additional card restraint. It consists of a 3/8 inch square bar with pins in each end. One of the pins is spring loaded to allow the bar to be installed or removed. A knurled finger screw provides a method to securely lock the bar in place. It fastens at both ends of the card cage and then horizontally across the STD Bus card's ejector to hold the cards firmly in the card cage. HXB is the prefix for the hold down bar for the CX series of card cages.

This product is ordered as a separate option with the card cages and powered racks.

ORDERING INFORMATION

Model	Slots
HXB-3	3
HXB-6	6
HXB-9	9
HXB-12	12
HXB-15	15
HXB-18	18
HXB-21	21
HXB-24	24
HXB-26	26

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS		
		A	B	C
CX03-T	3	3.92	2.66	1.250
CX06-T	6	5.76	4.54	3.125
CX09-T	9	7.63	6.41	5.000
CX12-T	12	9.51	8.29	6.875
CX15-T	15	11.38	10.16	8.750
CX18-T	18	13.26	12.04	10.625
CX21-T	21	15.13	13.91	12.500
CX24-T	24	17.01	15.79	14.375
CX26-T	26	18.26	17.04	15.625
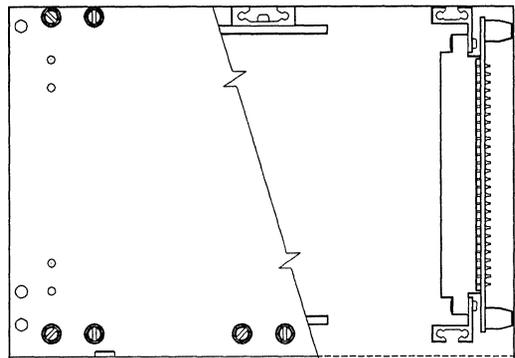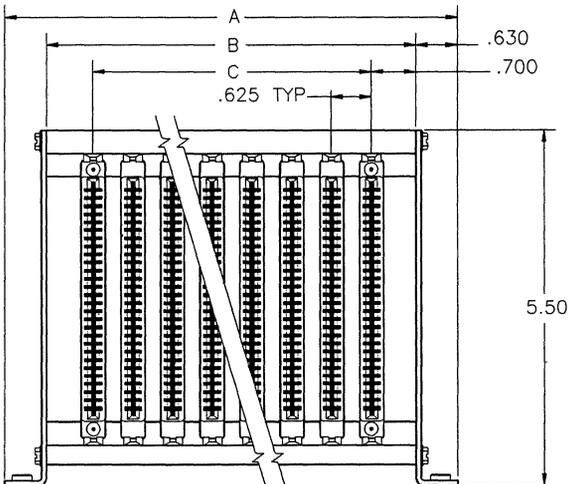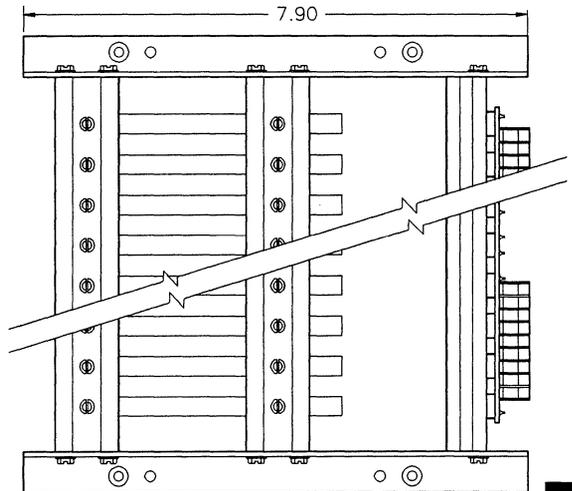
SIDE ENTRY CARD CAGE ASSEMBLY
5/8" CARD CENTERS

ORDERING INFORMATION

CARD CAGES

Model	Slots	Mounting Style	Backplane Installed
CX03-R	3	Rack Mount	BP3
CX03-T	3	Table Mount	BP3
CX03-W	3	Wall Mount	BP3
CX06-R	6	Rack Mount	BP6
CX06-T	6	Table Mount	BP6
CX06-W	6	Wall Mount	BP6
CX09-R	9	Rack Mount	BP9
CX09-T	9	Table Mount	BP9
CX09-W	9	Wall Mount	BP9
CX12-R	12	Rack Mount	BP12
CX12-T	12	Table Mount	BP12
CX12-W	12	Wall Mount	BP12
CX15-R	15	Rack Mount	BP15
CX15-T	15	Table Mount	BP15
CX15-W	15	Wall Mount	BP15
CX18-R	18	Rack Mount	BP18
CX18-T	18	Table Mount	BP18
CX18-W	18	Wall Mount	BP18
CX21-R	21	Rack Mount	BP21
CX21-T	21	Table Mount	BP21
CX21-W	21	Wall Mount	BP21
CX24-R	24	Rack Mount	BP24
CX24-T	24	Table Mount	BP24
CX24-W	24	Wall Mount	BP24
CX26-R	26	Rack Mount	BP26
CX26-T	26	Table Mount	BP26
CX26-W	26	Wall Mount	BP26

POWERED RACKS

Power Supplies - WinSystems offers card cages with triple output, 50W and 100W power supplies. These are high efficiency, highly reliable switching power supplies that accept single phase, 85 to 264 VAC. They will work from 47 to 63 Hz. An ON/OFF switch and momentary Reset switch are mounted on a panel for operator convenience. All units are fused and are equipped with a US standard 3-prong power cord with plug.

All powered card cages are supplied with a WinSystems' high performance backplane and status LEDs.

Card Rack Mounting Configuration - Three mounting configurations are available for the card cages with power supplies: Rack mount (R), Table mount (T),

and Wall mount (W). The dimensions for the powered racks are longer than the card cages to accommodate for mounting the power supplies inside the racks. The 21- and 24-slot card cages have the power supply mounted on the back of the cage so that the unit will stay within the 19" length for a standard equipment rack.

50 Watt Supply - The PS50 is a triple output, 50 Watt power supply. It is designed for CMOS STD Bus or small systems configurations. Although it has a standard 3 prong AC cable, it is a universal input switching design. Universal input voltage eliminates the need for an external 115/220 VAC system switch thereby eliminating failures dues to improper input voltage. It will operate from 47 Hz to 440 Hz.

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS	
		A	B
CX03-T-PS50	3	8.37	6.41
CX06-T-PSXX	6	10.25	8.29
CX09-T-PSXX	9	12.12	10.16
CX12-T-PSXX	12	14.00	12.04
CX15-T-PSXX	15	15.87	13.91
CX18-T-PSXX	18	17.75	15.79
CX21-T-PS100	21	17.75	15.79
CX24-T-PS100	24	19.00	17.04

PSXX PS50 - 50 WATT POWER SUPPLY
      PS100 - 100 WATT POWER SUPPLY
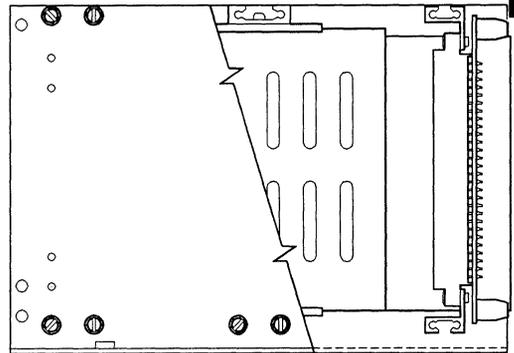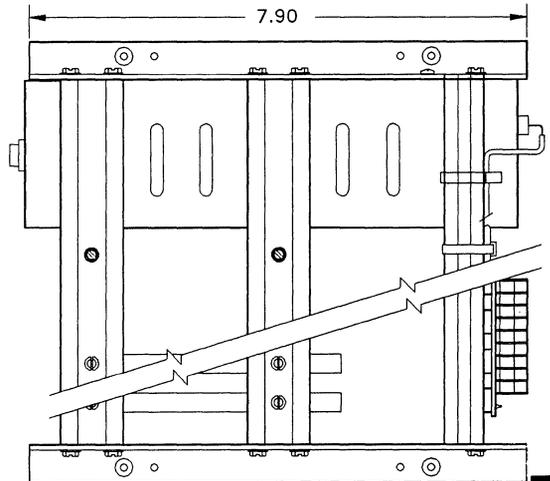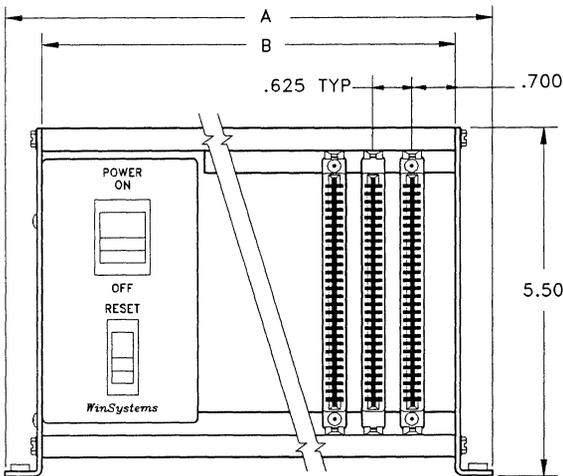
SIDE ENTRY CARD CAGE ASSEMBLY
5/8" CARD CENTERS w/100W PS

The PS50 is a zero current switcher. It will maintain regulation on all output voltages down to zero current thus eliminating the need for load resistors at light loads. This makes it ideal for CMOS applications yet there is enough current available for a small DOS system.

The PS50 has overvoltage protection and output short circuit protection. The power supply is convection cooled and should be derated from 50°C to 70°C to 25W. The power supply is very reliable with a MTBF of 160,000 hours.

100 Watt Power Supply - The PS100 is a triple output, high efficiency, 100 Watt power supply. It is designed for medium to large systems configurations. Although it has a standard 3 prong AC cable, it is a universal input switching design which will accept 85VAC to 264VAC. Universal input voltage eliminates the need for an external 115/220 VAC system switch thereby eliminating failures dues to improper input voltage. It will operate from 47 to 63 Hz.

The PS100 is a switching power supply which does not require a minimum load to maintain regulation on all output voltages lines. It also has overvoltage protection and output short circuit protection.

PS50 OUTPUT CHARACTERISTICS

Voltage	Minimum	Maximum
+5	0A	5.0A
+12	0A	2.0A
-12	0A	0.5A

PS100 OUTPUT CHARACTERISTICS

Voltage	Minimum	Maximum
+5	0A	10.0A
+12	0A	3.5A
-12	0A	0.5A

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS	
		A	B
CX03-W-PS50	3	8.37	6.41
CX03-W-PSXX	6	10.25	8.29
CX09-W-PSXX	9	12.12	10.16
CX12-W-PSXX	12	14.00	12.04
CX15-W-PSXX	15	15.87	13.91
CX18-W-PSXX	18	17.75	15.79
CX21-W-PS100	21	17.75	15.79
CX24-W-PS100	24	19.00	17.04

PSXX   PS50 - 50 WATT POWER SUPPLY
       PS100 - 100 WATT POWER SUPPLY
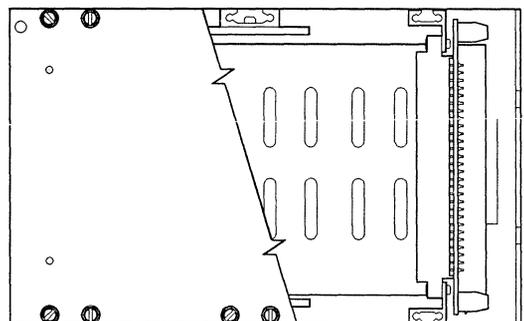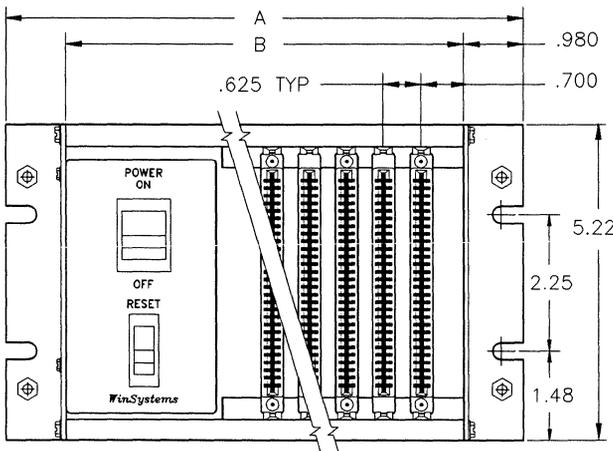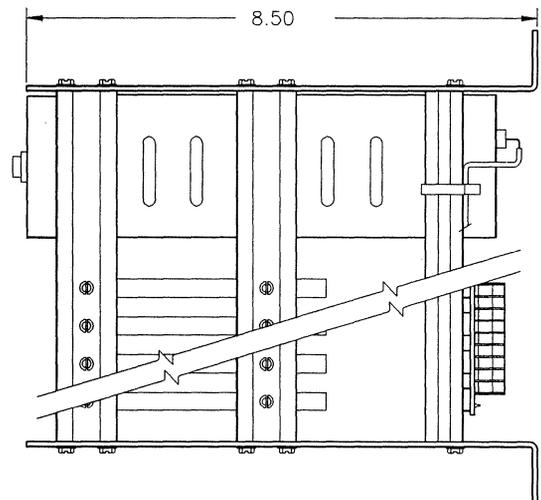
WALL MOUNT CARD CAGE ASSEMBLY
5/8" CARD CENTERS w/50W PS

Dimension - The same amount of room is allocated for the power supply for both power ranges. Therefore the mechanical drawings for the Rack, Wall, and Table versions reflect no additional room required. The difference is that with the 50W supply, the ON/OFF switch and Reset switch is integral in the power enclosure. The 100W model has an enclosed bracket with the ON/OFF and Reset switch mounted there.

The 50W power supply is available for the 3, 6, 9, 12, 15, and 18-slot card cages in all mounting configurations. The 100W power supply is available for the 6, 9, 12, 15, and 18-slot card cages. The 21 and 24 slot card cages have the 100W power supply mounted on the back rails of the card cage and are available for the rack and table versions only.

Part Number Assignment - A suffix is added to the standard card cage model number to designate the specific model power supply integrated into the rack. A PS50 suffix denotes the 50W power supply and a PS100 denotes a 100W power supply. For example a CX09-W-PS50 designates a 9 slot wall mount card cage with the 50 Watt power supply installed.

Options - The hold down bar and transorb options are available for the powered racks.

MODEL NO.	NO. OF SLOTS	REFERENCE DIMENSIONS	
		A	B
CX03-R-PS50	3	8.37	6.41
CX06-R-PSXX	6	10.25	8.29
CX09-R-PSXX	9	12.12	10.16
CX12-R-PSXX	12	14.00	12.04
CX15-R-PSXX	15	15.87	13.91
CX18-R PSXX	18	17.75	15.79
CX21-R-PS100	21	17.75	15.79
CX24-R-PS100	24	19.00	17.04

PSXX PS50 — 50 WATT POWER SUPPLY
PS100 — 100 WATT POWER SUPPLY
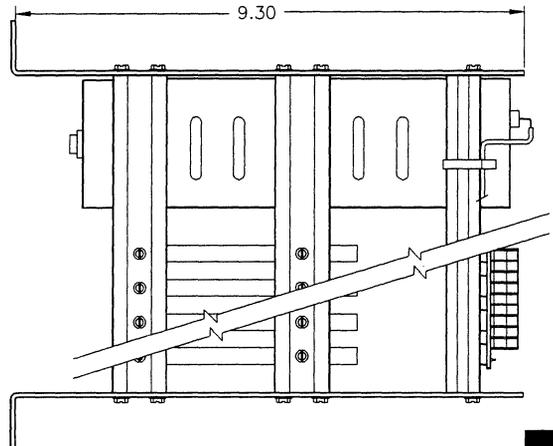
7
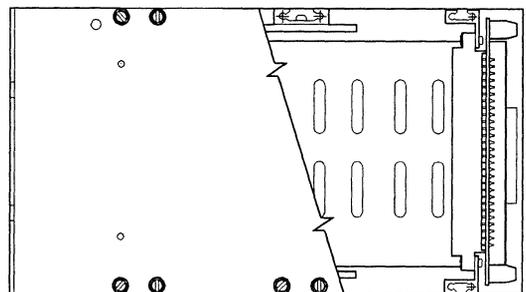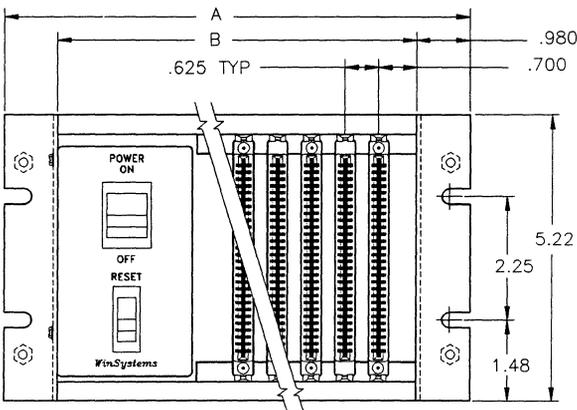
RACK MOUNT CARD CAGE ASSEMBLY
5/8" CARD CENTERS w/50W PS

ORDERING INFORMATION

POWERED CARD CAGES

Model	Slots	Mounting Style	Backplane Installed
CX03-R-PS50	3	Rack Mount	50W
CX03-T-PS50	3	Table Mount	50W
CX03-W-PS50	3	Wall Mount	50W
CX06-R-PS50	6	Rack Mount	50W
CX06-R-PS100	6	Rack Mount	100W
CX06-T-PS50	6	Table Mount	50W
CX06-T-PS100	6	Table Mount	100W
CX06-W-PS50	6	Wall Mount	50W
CX06-W-PS100	6	Wall Mount	100W
CX09-R-PS50	9	Rack Mount	50W
CX09-R-PS100	9	Rack Mount	100W
CX09-T-PS50	9	Table Mount	50W
CX09-T-PS100	9	Table Mount	100W
CX09-W-PS50	9	Wall Mount	50W
CX09-W-PS100	9	Wall Mount	100W
CX12-R-PS50	12	Rack Mount	50W
CX12-R-PS100	12	Rack Mount	100W
CX12-T-PS50	12	Table Mount	50W
CX12-T-PS100	12	Table Mount	100W
CX12-W-PS50	12	Wall Mount	50W
CX12-W-PS100	12	Wall Mount	100W
CX15-R-PS50	15	Rack Mount	50W
CX15-R-PS100	15	Rack Mount	100W
CX15-T-PS50	15	Table Mount	50W
CX15-T-PS100	15	Table Mount	100W
CX15-W-PS50	15	Wall Mount	50W
CX15-W-PS100	15	Wall Mount	100W
CX18-R-PS50	18	Rack Mount	50W
CX18-R-PS100	18	Rack Mount	100W
CX18-T-PS50	18	Table Mount	50W
CX18-T-PS100	18	Table Mount	100W
CX18-W-PS50	18	Wall Mount	50W
CX18-W-PS100	18	Wall Mount	100W
CX21-R-PS100	21	Rack Mount	100W
CX21-T-PS100	21	Table Mount	100W
CX24-R-PS100	24	Rack Mount	100W
CX24-T-PS100	24	Table Mount	100W

Backplane and Card Cage Quick Reference

SLOTS	BACKPLANE Only	RACK MOUNT		WALL MOUNT		TABLE MOUNT	
		With Power Supply	Without Power Supply	With Power Supply	Without Power Supply	With Power Supply	Without Power Supply
3	BP3	CX03-R-PS50	CX03-R	CX03-W-PS50	CX03-W	CX03-T-PS50	CX03-T
6	BP6	CX06-R-PS50 CX06-R-PS100	CX06-R	CX06-W-PS50 CX06-W-PS100	CX06-W	CX06-T-PS50 CX06-T-PS100	CX06-T
9	BP9	CX09-R-PS50 CX09-R-PS100	CX09-R	CX09-W-PS50 CX09-W-PS100	CX09-W	CX09-T-PS50 CX09-T-PS100	CX09-T
12	BP12	CX12-R-PS50 CX12-R-PS100	CX12-R	CX12-W-PS50 CX12-W-PS100	CX12-W	CX12-T-PS50 CX12-T-PS100	CX12-T
15	BP15	CX15-R-PS50 CX15-R-PS100	CX15-R	CX15-W-PS50 CX15-W-PS100	CX15-W	CX15-T-PS50 CX15-T-PS100	CX15-T
18	BP18	CX18-R-PS50 CX18-R-PS100	CX18-R	CX18-W-PS50 CX18-W-PS100	CX18-W	CX18-T-PS50 CX18-T-PS100	CX18-T
21	BP21	CX21-R-PS100	CX21-R	CX21-W-PS100	CX21-W	CX21-T-PS100	CX21-T
24	BP24	CX24-R-PS100	CX24-R	CX24-W-PS100	CX24-W	CX24-T-PS100	CX24-T
26	BP26	—	CX26-R	—	CX26-W	—	CX26-T

7

WinSystems, Inc.

FEATURES

- Instrument case and rack mount enclosures
- Available with and without power supply
- Complete with single or multiple backplanes
- Optional hinged front panel
- Application platform for either DOS or embedded systems
- High strength, precision-construction card cage configurations with backplanes on 0.75 inch spacing
- 50W and 100W power supplies available
- Excellent backplane design
  - Wide ground and power buses
  - Supports STD Bus 16-bit data transfers
  - Power status LEDs
  - Vcc bypass capacitor at each connector
  - Gold-plated bellows card edge connectors
  - Multiple backplanes supported in a card rack
- Accepts CMOS STD Bus cards
- Optional hold down bar and transorbs

WinSystems' STD Bus enclosures provide a foundation for STD DOS XT/AT and non-DOS embedded systems. They serve as a platform for industrial computer based products, enclosures for self contained OEM systems, or as a prototype shell for systems development. They are user configurable since the CPU, I/O and memory boards, disk drives, power supplies can all be added to the unit to customize it to the specific application.

The enclosures are available in three different product styles. The ENC-100 series is a 19" rack mount enclosure for STD Bus cards. The ENC-200 is an instrument case with power supply for STD Bus cards. The ENC-300 is a NEMA 4/4X enclosure to mount WinSystems' SBC88 single board computer and field termination modules.

The different enclosures should be selected based upon the application and its environmental conditions. Each enclosure has a series of options based upon configuration requirements.

ENC-100: Rack Mount Chassis

The WinSystems' ENC-100 is an enclosure designed specifically for rack mounted industrial applications. It is designed to fit in a 7" high, 19" EIA rack. Typical applications include automatic test stands, machine controllers and monitoring systems.

The ENC-100 is a rugged and versatile enclosure complete with 100 Watt power supply, fan and 20 slot
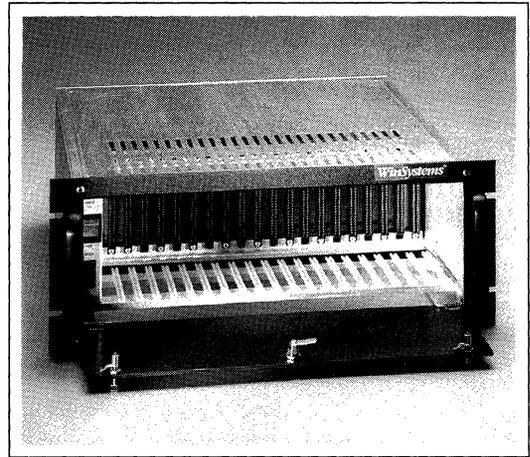
WinSystems' ENC-100 Rack Mount Chassis

STD Bus card cage on 0.75 inch centers. The unit does not contain any STD Bus cards since they are application dependent. A hold down bar is also included for restraint of the STD Bus cards.

Entry to the system is through the front panel access door. The door is hinged at the bottom and secured with two quarter turn locking catches at the top. Also there is a key lock for additional access security.

The ON/OFF switch, Reset and STD Bus cards are behind the panel access door. The STD card cage and power supply are indented from the front door to allow for cabling and extended length STD Bus cards.

Systems can be configured with I/O coming out the front or back of the enclosure. They can be configured with system available from 8088 to 80486 processors equipped with memory, data acquisition, motion control, networks, graphic, I/O and other controller modules from WinSystems and 3rd party STD Bus manufacturers. The ENC-100 supports the FD3-720/144 and HDAT-40/100 in-rack floppy and hard disk drives. For severe environments, where no mechanical disk drives are allowed, the ENC-100 can host a system that can run with solid state disks.

The main back panel is wired for a keyboard, VGA video, COM1, COM2 and LPT 2 port. A removable panel is on the rear to allow the customer to mount custom cables or access to special circuitry. The fan and universal AC connector with fuse holder and line filter are mounted on the back panel.
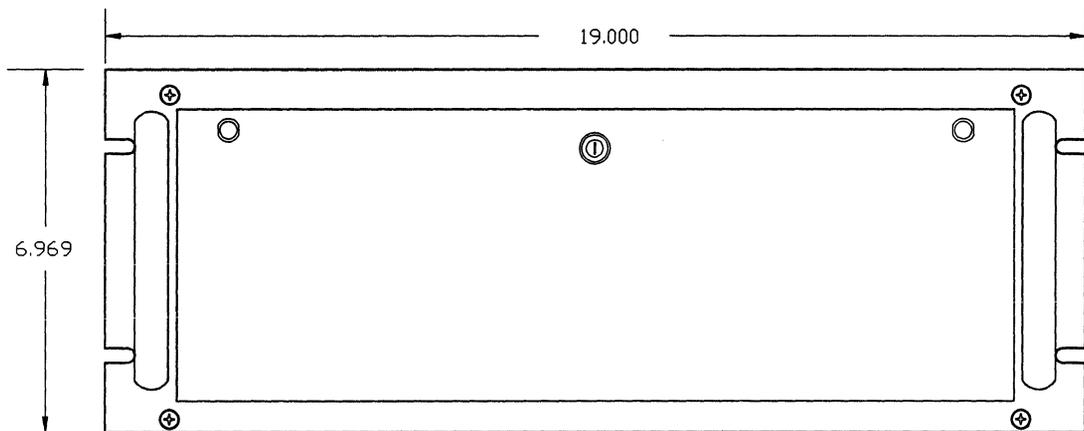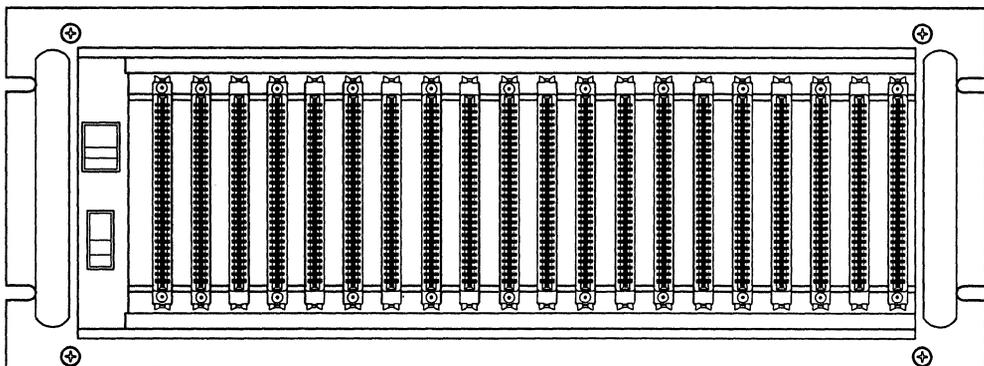
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7 - 27

Front With Door

19.000

6.969

Front Without Door
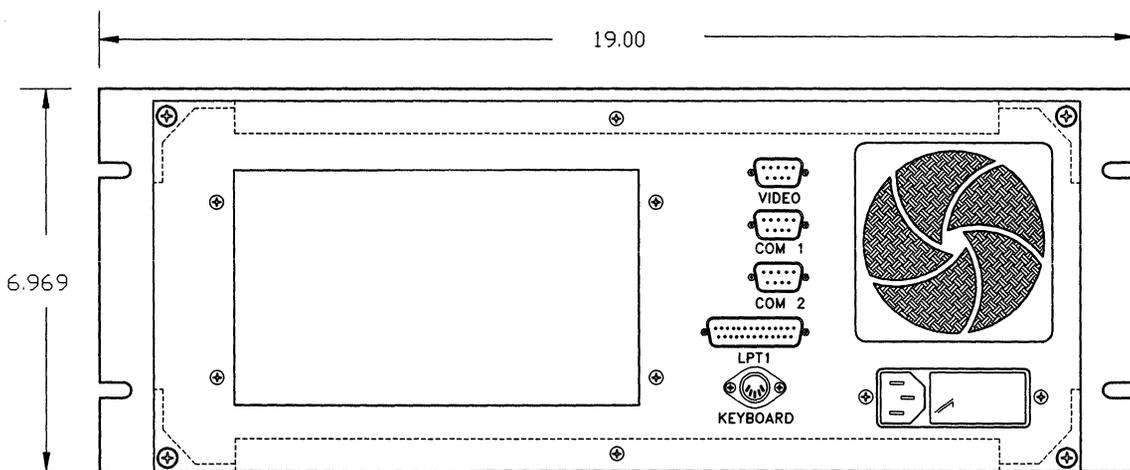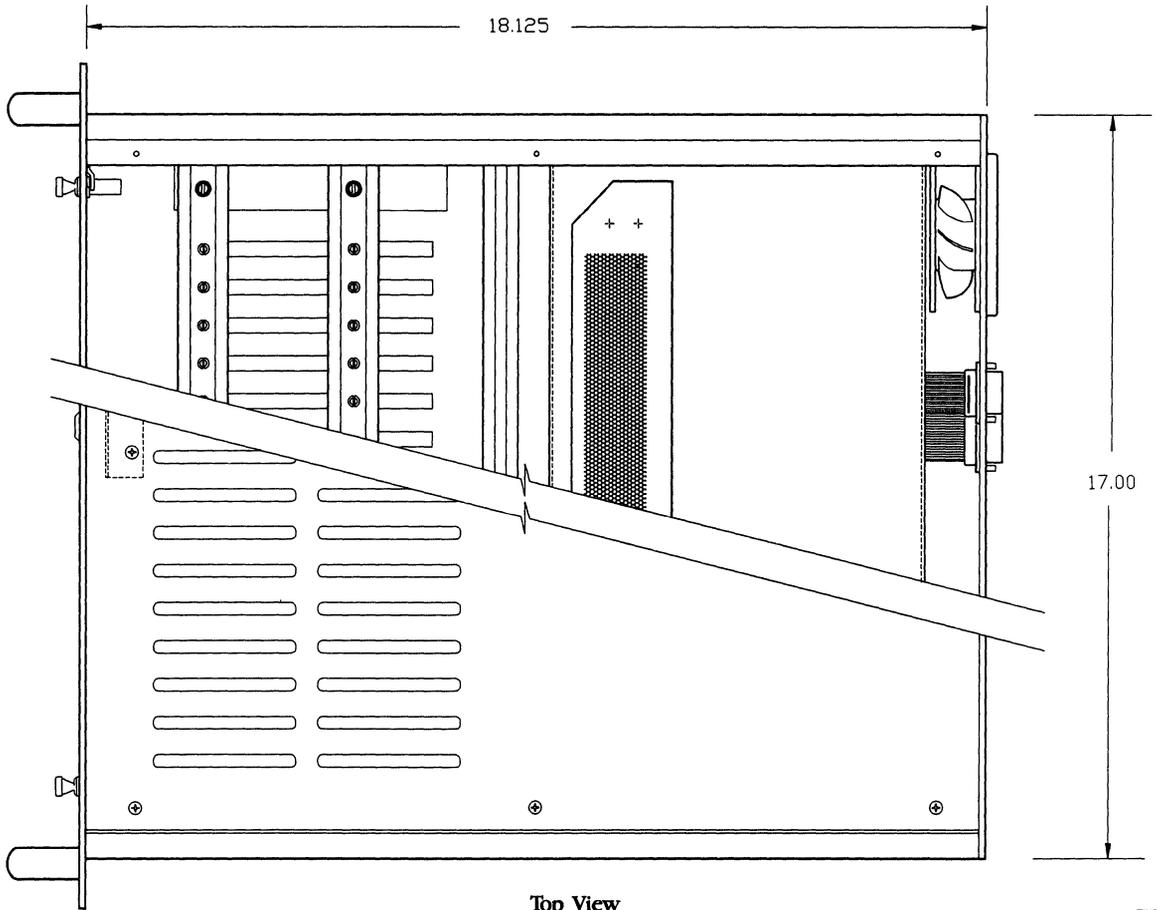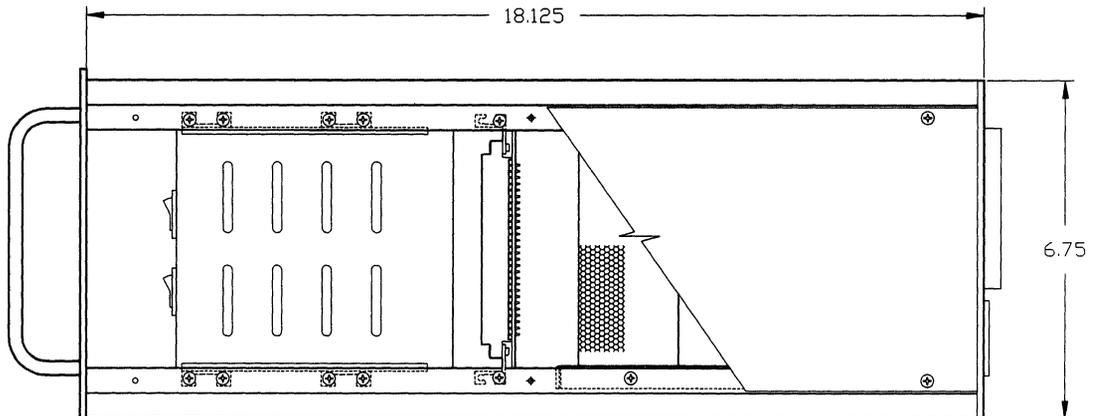
19.00

6.969

VIDEO
COM 1
COM 2
LPT1
KEYBOARD

Back

18.125

17.00

Top View

18.125

6.75

Side View

7

ENC-200: Instrument Case

WinSystems' ENC-200 instrument case enclosure offers a convenient packaging solution for STD Bus systems. The ENC-200 series is 21.02″ wide, 6.53″ high and 11.81″ deep. It is a desktop enclosure with an STD Bus card rack mounted inside. Many custom configurations are provided including 50 and 100 Watt power supplies; 12, 16, and 21 slot backplanes, multiple backplanes, hold down bars, locking front panel, carrying handles, and more.

The unit is made from high strength ABS plastic. A two-tone color scheme enhances the aesthetic appeal of the enclosure. The recessed molded grip in the side wall meets ergonomic requirements. This ensures safe and convenient transport in any situation.
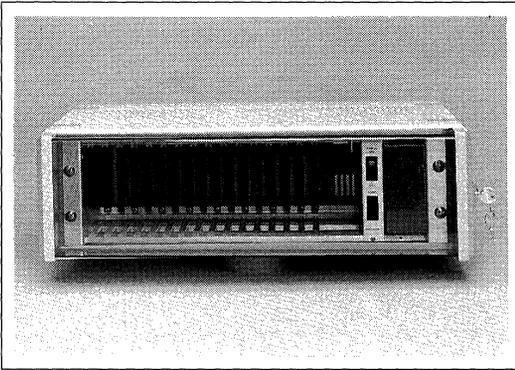
WinSystems' ENC-200 Instrument Case

Fold-out desktop case feet of fiberglass reinforced polyamide ensure safe stacking and eliminate the risk of slippage. Double fold-out capability of the case feet provides for two tilting angles.

The rear wall is secured with cam locks. No screw attachments are required which make installation and removal fast and simple. Vents in the back and top provide air circulation.

The fastening screws for the cover and base are neatly concealed by the support feet making the attachment screws invisible.

Options - Horizontal side carrying handles and a smoked plexiglass front panel are available for the case. Other options include the hold down bar for the card cage, power supply size, and size of card cage installed. Contact the factory for part numbers and pricing.

ENC-100 and ENC-200 Standard Components

Backplanes - Both the ENC-100 and ENC-200 enclosures are supplied with a WinSystems' high performance backplane with voltage status LEDs. WinSystems' STD Bus backplanes are available in a number of versions with up to 20 usable slots. The backplanes support both STD and CMOS STD Bus cards with no termination required. The design is based on field proven engineering techniques in order to offer the highest integrity and reliability. Spacing is on 0.75 inch centers with a vertical card orientation to take advantage of convection or forced air cooling.
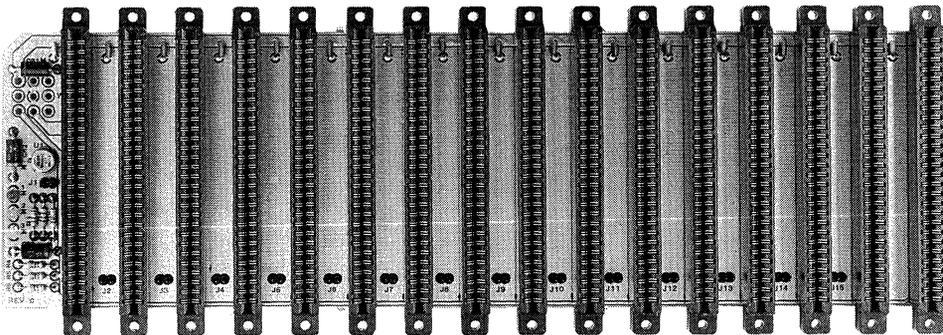
16 Slot Backplane with Power Fail Reset, Transorbs and LEDs

WinSystems' backplanes are designed for high performance STD Bus processors. They can work with all the processors including the new high performance 16/32-bit processors with full 16-bit data transfers. The assembly side of the backplane is a ground-plane which reduces noise and crosstalk on the signal lines. It also provides a constant characteristic impedance necessary for good transmission line design. The signal lines are narrow to reduce adjacent channel coupling.

Multiple Buses - For distributed processing applications, multiple backplanes can be mounted in a single card rack. This allows more than one STD Bus controller to reside in a single enclosure. Call WinSystems for exact configurations and price.

Hold down bar - An optional latching bar is available to provide additional card restraint. It consists of a 1/4 inch square bar with pins in each end. One of the pins is spring loaded to allow the bar to be installed or removed. A knurled finger screw provides a method to securely lock the bar in place. It fastens at both ends of the card cage and then horizontally across the STD Bus card's ejector to hold the cards firmly in the card cage.

Status LEDs - Three light emitting diodes (LEDs) are on each backplane to visually indicated the presence or absence of each of the power supply voltages. A different color is assigned to each voltage for easy and instant status recognition. Red is assigned to +5VDC, green is assigned to +12VDC, and yellow is assigned to -12VDC.

Connectors - WinSystems uses only UL approved connectors with gold-plated bifurcated bellows contacts. They are superior to cantilever beam connectors since they provide two beam contacts with two independent spring members and a constant spring tension on the card edge. The contact design enables the connector to have a lower insertion force, a higher withdrawal force and a higher, more consistent normal force. This translates to higher reliability and a better connection since it can absorb load deflection of a card while maintaining sufficient contact force for good electrical connection.

Transient Protection - Optional transient protection is provided on the +5, +12, and -12 volt lines for spike and surge suppression.

Power Supplies - WinSystems offers enclosures with optional 50W and 100W power supplies. These are triple output supplies that mount inside the card cage and generate DC output voltages from the AC mains.

They are high efficiency, highly reliable switching power supplies. The power supplies are zero current switchers. They will maintain regulation on all output voltages down to zero current thus eliminating the need for load resistors at light loads. This makes it ideal for CMOS applications yet there is enough current available for DOS systems with multiple disk drives.

An ON/OFF switch and momentary Reset switch are mounted on a panel for operator convenience. All units are fused and are equipped with a US standard 3-prong power cord with plug. The power supply has overvoltage protection and output short circuit protection. All WinSystems' power supplies are wide ranging universal inputs that operate from 85 to 264 VAC and 47 to 63 Hz.

Custom Configurations - Multiple backplanes and other options can be installed in the enclosures to allow more that one system to occupy a single container. To configure and price a custom backplane or assembly, contact the WinSystems' factory with your specifications.

ENC-300: NEMA 4/4X Enclosure

The ENC-300 is an integrated enclosure designed for direct applications in harsh environments especially in the areas of petrochemical, energy management, utilities for gas, electric and water, and process control. It consists of the NEMA4/4X enclosure, optional termination cards, power supply and either the WinSystems' SBC88, 16-bit single board computer
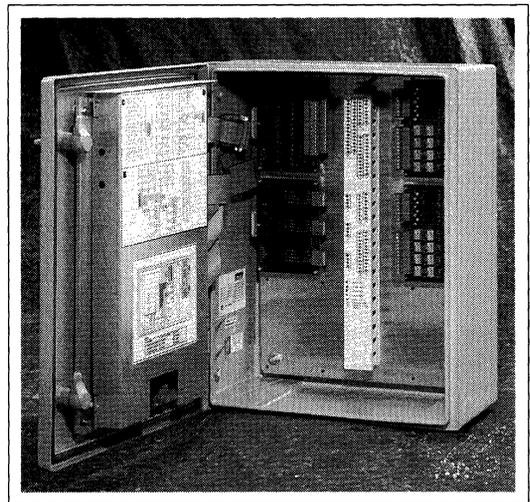
Winsystems' ENC-300 Nema 4/4x Enclosure
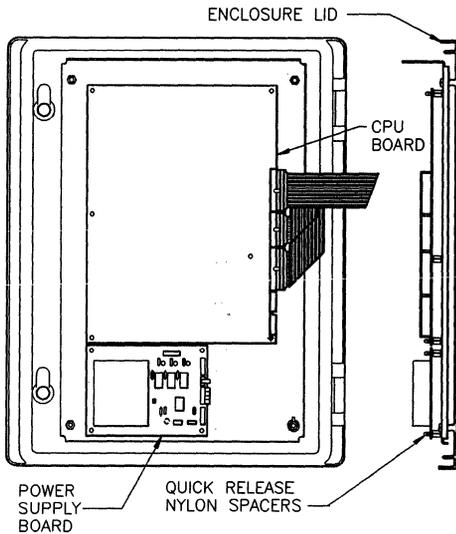
Front and Side View
of Front Door with SBC88 Installed

Front and Side View
with Optional Termination Card

or an STD Bus card cage. It is the common base of hardware upon which a final RTU system can be configured. Various termination panels, software and memory can be added to match the intended application.

The key design philosophy is low cost, flexibility, high reliability, and ease of maintenance. The unit will operate from -20 to +71 degrees Centigrade, requires no ventilation, and draws very little power. It can be powered from solar panels or batteries.

SBC88 - This 80C88-based SBC is a standard WinSystems' product developed as a standalone CMOS extended temperature single board computer that combines a number of proven CMOS STD Bus boards into a more cost effective single board. The SBC88 contains a CPU, memory sockets, clock, interrupt controller, counter/timers, parallel I/O, serial I/O, 16 channel A/D, watchdog timer, precision power fail reset, and SBX expansion modules, as well as optional D/A circuitry. A variety of configuration and population options are available to allow the end user to adapt the computer to the application. In addition to the above mentioned features, a wide assortment of I/O can be added inexpensively via the iSBX bus connectors.

STD Bus Card Cage - For applications requiring more expandability or I/O than the SBC88, an STD Bus card cage can be mounted in the ENC-300. It will permit

the selection a wide variety of CPU and I/O cards to meet a wide range of special functions.

Enclosure - The enclosure is a rugged NEMA4/4X rated box of either fiberglass or polycarbonate construction. The external dimensions are 16 x 20 x 7.5 inches. The SBC88 and power supply are mounted on the hinged door for easy accessibility. The termination boards are mounted on a subpanel which is attached to the back wall of the box. All field wiring is routed from the bottom of the box through a wiring channel in the center of the subpanel. This permits easy wiring to the termination panels and ease of service by field technicians.

Power Supply - A modular DC/DC converter is installed on the door panel. It will allow the user to input anywhere from 9Vdc to 36Vdc and will provide regulated power to the SBC88 and associated signal conditioning boards. Output current is +5Vdc at 1500 mA, +12Vdc at 310 mA, and -12Vdc at 310 mA. The manufacturers guaranteed operational temperature range is -25° to +71°C.

ENC-300 systems using an STD Bus card cage rather than the SBC88 would use the PS12T12/24/48 in-rack DC/DC power supply.

Field Termination Cards - WinSystems offers a series of termination boards that provide connection
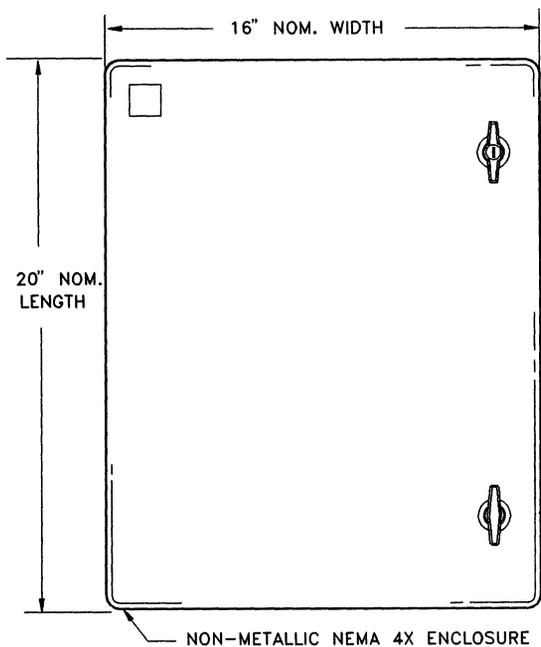
ENC-300 Front View
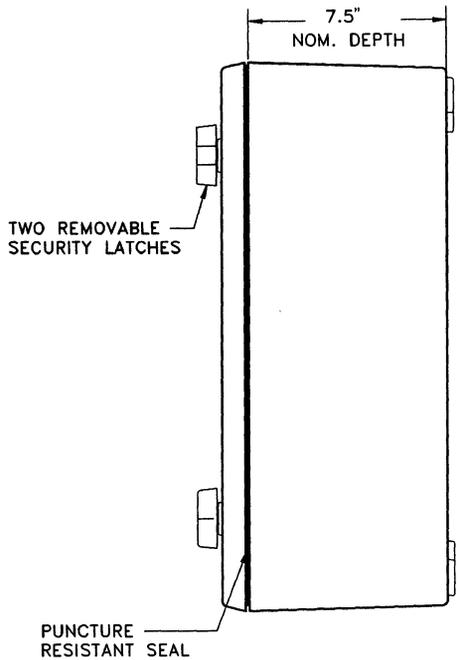
ENC-300 Side View

and signal conditioning from field wiring. These boards will work both with our STD Bus I/O cards and standalone Single Board Computers such as the SBC25 and SBC88. These boards are small, only 4.1 x 5.65 inches. All termination boards are the same size and mounting style so that the same footprint is required for ease of mechanical layout and packaging, while offering excellent configuration flexibility.

The boards are offered with analog input (TRM-100-XX), digital input (TRM-200-XX), digital output (TRM-300-XX), digital input/output (TRM-400-XX), and flow meter input (TRM-500-XX) signal conditioning. The XX refers to the number of channels supported by the board.

The boards accept a Phoenix pluggable connector from the field wiring to insure a reliable connection with easy removal and insertion. Output is to a ribbon cable connector for input to the single board computer or I/O board.

OEM Custom Configurations - It is the responsibility of the end user to provide access to the inside of the box (drill the holes) for the incoming serial I/O, digital I/O, analog I/O, flow meter input, and any other field wiring required for the application. Room is available to mount a RF modem, land line modem or similar sized peripheral device in the enclosure.

WinSystems will mount the SBC88, power supply, and terminator cards on the subpanel inside the NEMA4 box. WinSystems will also supply the cables that are required to connect the SBC88 with the terminator cards. The end user will be responsible for installation of the field wiring to the termination panels.

ORDERING INFORMATION

This product brief outlines the basic concepts of the instrument case and rack mount chassis at the time of the printing of the WinSystems' STD Bus Databook. Please contact the factory for detailed specifications and ordering information for the various options on the enclosures.

WinSystems, Inc.

FEATURES

- Provides screw terminal connections for field wiring from sensors
- Supports 8 differential inputs
- Screw clamp termination for field wiring accepts wide wire ranges up to 14AWG (maximum)
- Connects directly to MCM-7418 or MCM-7419 via 40-pin ribbon cable
- Isothermal termination block and cold reference circuit for thermocouples
- Cable connector on back allows panel mounting
- Small size: 4.6 x 2.0 inches

The ADP-7409TB is an 8 channel, non-isolated, termination board designed for use with WinSystems' MCM-7418 and MCM-7419 sensor boards. It provides a convenient, low cost method of terminating field wiring for input to the sensor boards.

FUNCTIONAL CAPABILITY

Termination Panel - The ADP-7409TB is designed to provide a rugged, industrial interface between field sensor wiring and WinSystems' sensor boards by converting ribbon cable connections to screw terminals. An ADP-7409TB will accept up to 8 differential sensor inputs from various sources such as thermocouples, 4-20 mA current loops, strain and pressure gages, RTD's, resistors, and thermistors in any mix.

Each sensor channel has five terminals: two for voltage input, two for current excitation, and as one shield. The V+ and V- wires are the channel sense inputs to the WinSystems' STD Bus sensor boards. The I+ and I- wires supply the excitation current to the sensor (if required). Only resistive sensors such as RTD's, resistors, thermistors, and strain gages require excitation. A shield drive signal is available for any channels needing it.

Cold Junction Compensation - The ADP-7409TB includes an Isothermal terminal block and temperature sensor that is monitored by the MCM-7418 and MCM-7419's onboard microprocessor to perform exact cold junction compensation for thermocouples. ADP-7409TB boards may be quickly interchanged because each cold-junction sensor is individually calibrated.
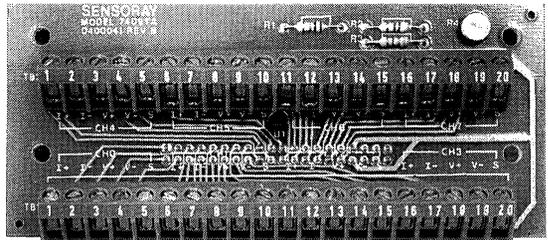
Input Terminal Strip - The field wiring is connected to two, twenty position, screw clamp terminal strips. Each terminal pole is wired consecutively from 1 though 20. These are very rugged connectors that offer captive wire protection. It is designed for solid or stranded, single or multiple wires in a variety of gauges up to 14AWG. The terminal screws are deeply recessed with no metal parts exposed. The ADP-7409TB is rigidly constructed from 1/8-inch thick FR-4 material to prevent flexing from heavy gauge wire loads.

System Interconnection - The ADP-7409TB has a 40-pin header on the back of the board that accepts a mass terminated ribbon cable. WinSystems' CBL-126-2 is the 2 foot long, 40 conductor, #28AWG ribbon cable designed to connect 40-pin header connectors. Each end has a 40-pin, 0.100" polarized connector with strain relief.

SPECIFICATIONS

Mechanical
Dimensions: 4.6" x 2.0"
PC Board: FR4, 0.125 inches thick
Number of signal inputs: 8 differential

ORDERING INFORMATION

ADP-7409TB   8 channel sensor terminator card
CBL-126-2   2 foot, 40 conductor ribbon cable

WinSystems, Inc.

FEATURES

- Convenient and reliable screw terminal connections for user analog input signals
- Supports up to 16 single ended or 8 differential inputs
- Screw clamp termination for field wiring accepts wide wire ranges up to 14 AWG max.
- Extensive passive signal conditioning capabilities
- Blank circuit pads for user-installed filters, transorbs, voltage dividers or current shunts
- Different termination configurations allowed on each channel
- Ribbon cabling directly compatible with WinSystems' MCM-A/D12, LPM-A/D12, MCM-AIO and LPM-AIO
- Two breadboard areas for custom user circuits
- Small size (3.5" x 7.75") for versatile mounting
- Low cost
- Totally passive design, no power required

The Analog-ADP is a non-isolated signal conditioning panel for use with WinSystems STD Bus analog to digital converters. It provides a multitude of termination options for the analog input signals plus serves as a field wiring to ribbon cable adapter.

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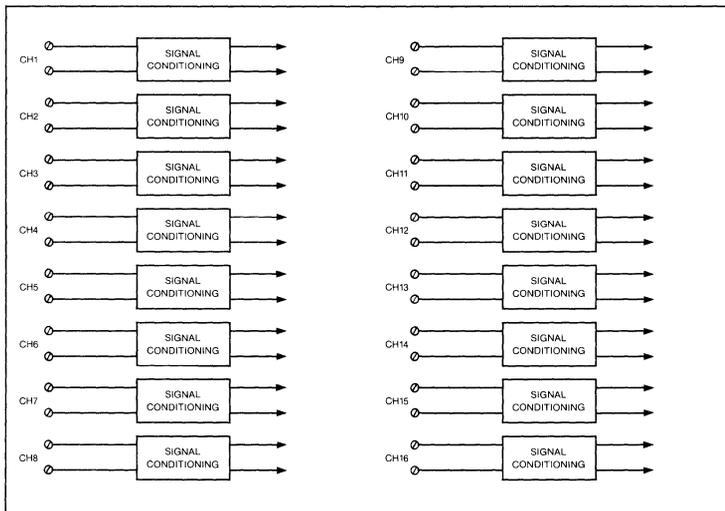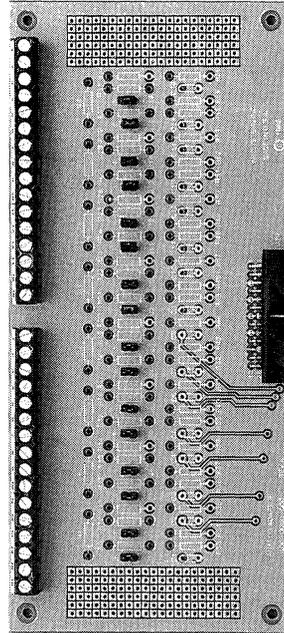
FUNCTIONAL CAPABILITY

Termination Panel - The Analog-ADP is designed to facilitate user connections to WinSystems' MCM/LPM-AIO and MCM/LPM-A/D12 STD Bus A/D converters and to provide a variety of signal conditioning functions. It will accept up to 8 differential or 16 single ended inputs.

When used as a termination panel, the user's signal lines are connected to the panel's screw terminals. These signals are wired straight through the panel to a 26-pin connector that is linked to the A/D board with a ribbon cable. This is the standard shipping configuration from the factory.

Signal Conditioning - The Analog-ADP is designed with blank pads that allow installation of passive components and transorbs to create filters, voltage dividers, or current shunts. The blank pads are divided into 16 identical circuits. Differential inputs may be connected by using the single ended channels in pairs. Each channel is independent of the other and can be configured separately as dictated by the needs of the system.

One of the most common configurations is with a current shunt to convert the current output of sensors into the voltage input required by the A/D boards. With 4-20 mA systems, a 250 ohm close tolerance resistor is installed. The amount of voltage drop is directly proportional to the current flowing through the shunting resistor. A 4 mA current will result in a 1 volt signal and a 20 mA will result in a 5 volt signal. The Analog-ADP will work with current shunts in either single ended or differential modes.

In many applications, input signals must pass through an electrically noisy environment before reaching the connection points on the Analog-ADP. This noise becomes superimposed upon the signal and will cause false and erroneous readings by the high speed A/D board. If the input signal is a relatively low frequency, RC low pass filters can be installed to attenuate the high frequency noise.

The Analog-ADP will also accept two resistors configured as a voltage divider network in order to reduce the input voltage to a range acceptable to the A/D board.

Input Terminal Strip - The field wiring is connected to two sixteen position, screw clamp terminal strips. Each terminal pole is wired consecutively from 1 though 16. These are very rugged connectors that offer captive wire protection. Lateral grooves provide high pull-out resistance. It is designed for solid or stranded, single or multiple wires in a variety of gauges up to 14 AWG without solder dipping or sleeving the wire ends. The terminal screws are deeply recessed with no metal parts exposed. The shape of the insulating case is suitable for automatic screwdrivers.

System Interconnection - The Analog-ADP has a 26-pin header that accepts a mass terminated ribbon cable. A WinSystems CBL-130-3 is a 3 foot long, 26 conductor, #28 AWG ribbon cable designed to connect two, 26-pin header connectors. Each end has a 26-pin, 0.100″ polarized connector with strain relief.

Breadboard Area - Two 0.6″ x 2.2″ breadboard areas are provided on the Analog-ADP. Each consists of a 0.100 inch grid of 0.042 inch plated through holes that accept standard DIP sockets, connectors, press fit pins, and discrete logic circuitry. This allows a user to construct experimental and custom I/O interfaces with a minimum of effort.

Mounting Configuration - The analog termination board has a hole in each corner of the board that will accept 6-32 screws.

OEM Configurations - The Analog-ADP is supplied with no components installed to offer the most flexibility to the user. WinSystems can factory install passive signal conditioning components for volume OEMs that prefer a preconfigured board.

SPECIFICATIONS

Mechanical

Dimensions:	3.5″ x 7.75″
PC Board:	FR4, 0.62 inches thick
Number of signal inputs:	16 SE, 8 differential
Wire size:	14 to 22 AWG

Environmental
Temperature Range: -40°C to +85°C

ORDERING INFORMATION

Analog-ADP	Analog termination panel
CBL-130-3	3 foot long, 26 conductor ribbon cable

WinSystems, Inc.

FEATURES

- Data Communications for DTE and DCE interfacing
- Floppy Disk cabling including the adapters for 8", 5 1/4", and 3 1/2" drives
- Power supply cables
- Opto-22 type I/O rack module cables
- Slotted 'connector for polarization
- Ribbon cables with strain relief

CBL-101-3

The CBL-101-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 26-pin, 0.100" grid connector to a "D" type data communications connector. One end of the cable has a polarized, 26-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin male "D" connector with strain relief. This cable allows WinSystems' STD and CMOS STD Bus cards to provide a RS-232 Data Terminal Equipment (DTE) interface. This cable is used to interface to cards such as the MCM-SIO2, LPM-SIO2, MCM-SIO2A, LPM-SIO2A, MCM-DSIO, LPM-DSIO, MCM-SPIO, LPM-SPIO, MCM-7304, LPM-7304, MCM-7314, LPM-7314, SBX-SCC and LBX-SCC.

CBL-102-3

The CBL-102-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 26-pin, 0.100" grid connector to a "D" type data communications connector. One end of the cable has a polarized 26-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin female "D" connector with strain relief. This cable allows WinSystems' STD and CMOS STD Bus cards to provide a RS-232 Data Communications Equipment (DCE) interface. This cable is used to interface to cards such as the MCM-SIO2, LPM-SIO2, MCM-SIO2A, LPM-SIO2A, MCM-DSIO, LPM-DSIO, MCM-SPIO, LPM-SPIO, MCM-7304, LPM-7304, MCM-7314, LPM-7314, SBX-SCC and LBX-SCC.

CBL-103-3

The CBL-103-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 16-pin 0.100" grid connector to a "D" type data communications connector. One end of the cable has a polarized, 16-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin male "D" connector with strain relief. This cable allows Win-

Systems' STD and CMOS STD Bus cards to provide a RS-232 Data Terminal Equipment (DTE) interface. This cable is used to interface to cards such as the MCM-SBC, MCM-SBC2, MCM-SBC3, LPM-SBC3, and MCM-SBC4.

CBL-104-3

The CBL-104-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 16-pin 0.100" grid connector to a "D" type data communications connector. One end of the cable has a polarized 16-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin female "D" connector with strain relief. This cable allows WinSystems' STD and CMOS STD Bus cards to provide a RS-232 Data Communications Equipment (DCE) interface. This cable is used to interface to cards such as the MCM-SBC, MCM-SBC2, MCM-SBC3, LPM-SBC3, and MCM-SBC4.

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CBL-105-3

The CBL-105-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 14-pin 0.100″ grid connector to a "D" type data communications connector. One end of the cable has a polarized 14-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin male "D" connector with strain relief. This cable allows WinSystems STD and CMOS STD Bus cards to provide a RS-232 Data Terminal Equipment (DTE) interface. This cable is used to interface to cards such as the MCM-SBC50, LPM-SBC50, MCM-SBC8, LPM-SBC8, MCM-SIO4, and LPM-SIO4.

CBL-106-3

The CBL-106-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 14-pin 0.100″ grid connector to a "D" type data communications connector. One end of the cable has a polarized 14-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25 pin female "D" connector with strain relief. This cable allows WinSystems' STD and CMOS STD Bus cards to provide a RS-232 Data Communications Equipment (DCE) interface. This cable is used to interface to cards such as the MCM-SBC50, LPM-SBC50, MCM-SBC8, LPM-SBC8, MCM-SIO4, and LPM-SIO4. This is the cable that is used to connect WinSystems cards to a PC or equivalent for down-line loading of data.

CBL-107-3

The CBL-107-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 10-pin 0.100″ grid connector to a "D" type data communications connector. One end of the cable has a polarized 10-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25 pin male "D" connector with strain relief. This cable allows WinSystems' STD and CMOS STD Bus cards to provide a RS-232 Data Terminal Equipment (DTE) interface. This cable is used to interface to cards such as the MCM-SBC5 and LPM-SBC5.

CBL-108-3

The CBL-108-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 10-pin 0.100″ grid connector to a "D" type data communications connector. One end of the cable has a polarized 10-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin female "D" connector with strain relief. The pin 1 and 7 ground lines are tied together. This cable allows WinSystems'

STD and CMOS STD Bus cards to provide a RS-232 Data Communications Equipment (DCE) interface. This cable is used to interface to cards such as the MCM-SBC5 and LPM-SBC5. This cable is used by the MCM-SBC40 and LPM-SBC40 to connect to a PC/XT/AT to run C-Thru-ROM.

CBL-109-2

The CBL-109-2 is 2 foot long, #28 AWG ribbon cable designed to interface the MCM-SBC to two Shugart compatible SA-820 8″ floppy disk drives. A polarized 50-pin female socket with strain relief is connected to two 50-pin edge connectors that mate with the floppy disk drive's edge card. Six inches separate the two floppy disk connectors for flexible mounting configurations of adjacent drives.

CBL-110-1

The CBL-110-1 is 1 foot long, #28 AWG ribbon cable designed to interface the MCM-SBC to either the ADP-5.0 or ADP-3.5 adapter boards. A polarized 50-pin female socket with strain relief is connected to both ends.

The ADP adapter boards are used to convert the 50-pin cable to either a 34-pin cable for 5 1/4 inch floppy disk drives or a 26-pin cable for 3 1/2 inch floppy disk drives. Both cards have a motor time-out circuit that turns off the motor approximately 5 seconds after the drive is deselected. This prevents premature wear of the media.

CBL-111-2

The CBL-111-2 is 2 foot long, #28 AWG ribbon cable designed to interface the ADP-3.5 board to a 3 1/2 inch Sony OA-D32V or equivalent drive. A polarized 26-pin female socket with strain relief is connected to a 26-pin connector that mates with the drive's card edge.

CBL-112-2

The CBL-112-2 is 2 foot long, #28 AWG ribbon cable designed to interface the ADP-5.0 board to a 5 1/4 inch high density Shugart 475 or Mitsubishi M4854 or equivalent drive. A polarized 34-pin female socket with strain relief is connected to a 34-pin connector that mates with the drive's card edge.

CBL-113-2

The CBL-113-2 is 2 foot long, #28 AWG ribbon cable designed to interface the MCM-SBC to a 8 inch floppy

disk drive and either the ADP-5.0 or ADP-3.5 adapter boards. A polarized 50-pin female socket with strain relief is connected to both ends. Eighteen inches from one end is a 50-pin card edge connector that will plug into the floppy disk drives card edge.

The ADP adapter boards are used to convert the 50-pin cable to either a 34-pin cable for 5 1/4 inch floppy disk drives or a 26-pin cable for 3 1/2 inch floppy disk drives. Both cards have a motor time-out circuit that turns off the motor approximately 5 seconds after the drive is deselected. This prevents premature wear of the media.

CBL-114-4

The CBL-114-4 is a 4 foot long, #28 AWG 50-line ribbon cable designed to interface a MCM-7507 or LPM-7507 card to an Opto-22 module or equivalent PB-4, PB-8, PB-16, and PB24 mounting rack. A 50-pin card edge connector is connected to both ends.

CBL-115-4

The CBL-115-4 is a 4 foot long, #28 AWG 50-line ribbon cable designed to interface a MCM-7508, LPM-7508 or LPM-PI03 card to an Opto-22 module or equivalent PB-4, PB-8, PB-16, and PB24 mounting rack. A 50-pin 0.100″ grid polarized connector with strain relief is on one end of the cable and a 50-pin 0.125″ edge card is on the other.

CBL-116-1

The CBL-116-1 is a 6 inch long, #16 AWG power supply cable to connect a WinSystems' motherboard (MB4, MB6, etc.) to a power plug. Its 9 color coded wires connect to a 9-pin Molex plug. It uses the standard resistor color code for the wire color assignment (pin 1 = brown, etc.). It mates with a CBL-117-1.

This cable is furnished and installed on all WinSystems' card cages. The cable is not furnished with the WinSystems' motherboards.

CBL-117-1

The CBL-117-1 is a 1 foot long, #16 AWG power supply cable to connect a power supply to a power connector. Its 9 color coded wires connect to a 9-pin Molex socket that protects the pins. It uses the standard resistor color code for the wire color assignment (pin 1 = brown, etc.). The Molex connector is polarized with individually recessed high current contacts. It mates with a CBL-116-1.

CBL-118-3

The CBL-118-3 is a 3 foot long, #28 AWG ribbon cable designed to provide access to signals from 16-pin, 0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 16-pin female socket connector with strain relief that plugs into the board and the other end is open. This cable configuration allows users to make their own custom cable termination. This cable is used to interface to cards such as the MCM-SBC, MCM-SBC2, MCM-SBC3, LPM-SBC3, and MCM-SBC4.

CBL-119-3

The CBL-119-3 is a 3 foot long, #28 AWG ribbon cable designed to provide access to signals from 40-pin, 0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 40-pin female socket connector with strain relief that plugs into the board and the other end is open. This cable configuration allows users to make their own custom cable termination. This cable is used to interface to cards such as the MCM-7605 and LPM-7605.

CBL-120-3

The CBL-120-3 is a 3 foot long, #28 AWG ribbon cable designed to provide access to signals from 26-pin, 0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 26-pin female socket connector with strain relief that plugs into the board and the other end is open. This cable configuration allows users to make their own custom cable termination.

This cable is used to interface to cards such as the MCM-A/D12, LPM-A/D12M, MCM-SBC6, LPM-SBC6, MCM-SBC50, LPM-SBC50, MCM-PIO, LPM-PIO, MCM-PIO1, LPM-PIO1, MCM-PIO2, LPM-PIO2, MCM-SIO2, LPM-SIO2, MCM-SIO2A, LPM-SIO2A, MCM-DSIO, LPM-DSIO, MCM-SPIO, LPM-SPIO, MCM-7304, LPM-7304, MCM-7314, LPM-7314, SBX-PIO, LBX-PIO, SBX-SCC and LBX-SCC.

CBL-121-6

The CBL-121-6 is a 6 foot long, #28 AWG ribbon cable designed to provide access to signals from 34-pin, 0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 34-pin female socket connector with strain relief and the other end is open.

CBL-122-1

The CBL-122-1 is a 1 foot long, #28 AWG ribbon cable designed to convert a 26-pin, 0.100″ grid connector

to a 25-pin "D" type that mates with Centronics line printers. One end of the cable has a polarized, 26-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 25-pin female "D" with strain relief. This cable is used by the MCM-386SX, MCM-286AT, MCM-SBC41, MCM-DLPT and MCM-DSPIO as a line printer adapter cable.

CBL-123-1

The CBL-123-1 is a 1 foot long, #28AWG ribbon cable designed to convert a 10-pin, 0.100" grid connector to a 9-pin "D" data communications connector. One end of the cable has a polarized 10-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 9-pin male "D" connector with strain relief. This cable is used with boards that are wired with the 9-pin PC-AT serial communications configuration and provides a interface with the MCM-386SX, MCM-286AT, MCM-SBC41, and MCM-DSPIO.

CBL-124-1

The CBL-124-1 is a 1 foot long, #28 AWG ribbon cable designed to serve as a 10-pin ribbon to 5-pin DIN keyboard adapter cable for the MCM-386SX, MCM-286AT and MCM-SBC40XT boards.

CBL-125-1

The CBL-125-1 is a 9 inch, #28 AWG 34-pin ribbon cable that connects the MCM-DISK-AT and MCM-DISK-XT floppy disk controllers to FD3-720 and/or FD3-144 floppy disk drives. This cable has a twist in the drive select lines and is designed for a single floppy drive selected as A: in an STD Bus card cage.

CBL-126-1

The CBL-126-1 is a 7 inch, #28 AWG 40-pin ribbon cable that connects the MCM-DISK-AT IDE hard disk controller to the HDAT-20, HDAT-40, HDAT-100 or HDAT-200 hard disk drives. This cable is designed for a single hard drive in a STD Bus card cage.

CBL-127-6

The CBL-127-6 is a 6 foot long, #28 AWG ribbon cable designed to provide access to signals from 40-pin 0.100" headers on WinSystems' boards. One end of the cable has a polarized, 40-pin female socket connector with strain relief that plugs into the board and the other end is open.

CBL-128-1

The CBL-128-1 is a 9 inch, #28 AWG 34-pin ribbon cable that connects the MCM-DISK-AT and MCM-DISK-XT floppy disk controllers to FD3-720 and/or FD3-144 floppy disk drives. This cable is identical to the CBL-125-1 except that the CBL-128-1 does not have a twist in the drive select signal lines which selects the drive as B.

CBL-129-1, CBL-129-4

The CBL-129-1 is a 6 inch, #28 AWG 50-pin ribbon cable that connects the MCM-DISK-XT and MCM-SCSI controller to the HDXT-20 or HDXT-40 hard disk drives. This cable is designed for a single SCSI hard drive in a STD Bus card cage.

The CBL-129-4 is a 4 foot version of the CBL-129 used to connect both cards of the LPM/MCM-DPRAM

CBL-130-1, CBL-130-3

The CBL-130-1 is the 4 inch, #28 AWG 26-pin ribbon cable from the MCM-SBC40XT and LPM-SBC40XT single board computers to the SBX keyboard interface module.

The CBL-130-3 is a 3 foot, 26-pin ribbon cable from the ADP-Analog to the MCM/LPM-AIO and MCM/LPM-AIO12 boards.

CBL-131-1

The CBL-131-1 is a #28 AWG, 34 conductor cable connecting the MCM-DISK-AT and LPM-DISK-AT to one 3.5" and one 5.25" floppy disk drive. The cable is 9" from the controller connector to a 3.5" drive located in the STD Bus card cage and 18" from the controller to an externally mounted 5.25" drive. A twist is located in the drive select wires for the 3.5" drive so that it will be selected as drive A.

CBL-132-1

The CBL-132-1 is a 3 inch long, 18 conductor, #28AWG ribbon cable with 3 connectors that serves as the STD-AT local bus cable. The connectors are spaced such that the CPU, disk controller and video card can be linked over the front plane rather than with the backplane.

CBL-133-1

The CBL-132-1 is a 6 inch long, 18 conductor, #28AWG ribbon cable with 2 connectors that serves

as the WinSystems XT-80 PC-XT compatible local bus cable. The connectors are spaced such that the CPU and disk controller can be linked over the front plane rather than with the backplane.

CBL-134-3

The CBL-134-3 is a 3 foot long, #28 AWG ribbon cable designed to connect two 34-pin right angle header connectors. Each end has a 34-pin, 100″ polarized connector with strain relief. This cable permits access from the MCM-7614 and LPM-7614 parallel I/O cards.

CBL-134-6

The CBL-134-6 is a 6 foot long, #28 AWG ribbon cable designed to connect two 34-pin right angle header connectors. Each end has a 34-pin, 100″ polarized connector with strain relief. This cable permits access from the STD Bus Board to the PC Bus Card in the WinSystems' PC-STD Bus Adapter.

CBL-135-3

The CBL-135-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 34-pin ribbon 0.100″ grid connector to a "D" type connector. One end of the cable has a polarized 34-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 37-pin male "D" connector with strain relief. This card will work with cards such as the LPM-7614 and MCM-7614.

CBL-136-3

The CBL-135-3 is a 3 foot long, #28 AWG ribbon cable designed to convert a 34-pin ribbon 0.100″ grid connector to a "D" type connector. One end of the cable has a polarized 34-pin female socket connector with strain relief that plugs into the board and the other end is supplied with a 37-pin female "D" connector with strain relief. This card will work with cards such as the LPM-7614 and MCM-7614.

CBL-137-3

The CBL-137-3 is a 3 foot long, #28 AWG ribbon cable designed to provide access to signals from 20-pin, 0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 20-pin female socket connector that plugs into the board and the other end is open and unterminated. This cable permits access to the MCM-D/A8 and LPM-D/A8 cards.

CBL-138-3

The CBL-138-3 is a 3 foot long, #28 AWG ribbon cable designed to provide access to signals from 20-pin,

0.100″ grid connectors on WinSystems' boards. One end of the cable has a polarized, 37-pin female socket connector that plugs into the board and the other end is open and unterminated.

CBL-139-3

The CBL-139-3 is a #28AWG 34-pin ribbon cable that connects the MCM-DISK-AT and MCM-DISK-XT floppy disk controllers to two FD3-720 and/or FD3-1.44 floppy disk drives. This cable contains a twist for automatic drive selection and is designed for use with two floppy drives in a STD Bus card cage.

ORDERING INFORMATION

CBL-101-3 3 ft. ribbon, 26-pin female socket to 25-pin male "D" type connector

CBL-102-1 9 inch ribbon cable, 26-pin female socket to 25-pin male "D" type connector for STD-AT

CBL-102-3 3 ft. ribbon cable, 26-pin female socket to 25-pin female "D" type connector

CBL-103-3 3 ft. ribbon cable, 16-pin female socket to 25-pin male "D" type connector

CBL-104-3 3 ft. ribbon cable, 16-pin female socket to 25-pin female "D" type connector

CBL-105-3 3 ft. ribbon cable, 14-pin female socket to 25-pin male "D" type connector

CBL-106-3 3 ft. ribbon cable, 14-pin female socket to 25-pin female "D" type connector

CBL-107-3 3 ft. ribbon cable, 10-pin female socket to 25-pin male "D" type connector

CBL-108-3 3 ft. ribbon cable, 10-pin female socket to 25-pin female "D" type connector

CBL-109-2 2 ft., 50-line ribbon cable, interfaces MCM-SBC to two 8" floppy disk drives

CBL-110-1 1 ft., 50-line ribbon cable, interfaces MCM-SBC to either ADP-3.5 or ADP-5.0 adapter boards

CBL-111-2 2 ft., 26-line ribbon cable, interfaces ADP-3.5 board to 3.5 Sony drive

CBL-112-2 2 ft., 34-line ribbon cable, interfaces ADP-5.0 board to 5 1/4" high density drive

CBL-113-2 2 ft., 50-line ribbon cable, interfaces MCM-SBC to one 8" floppy disk drive and to either the ADP-3.5 or ADP-5.0 adapter boards

CBL-114-4 4 ft. ribbon cable, interfaces MCM-7507 and LPM-7507 to Opto-22 racks

CBL-115-4 4 ft. ribbon cable, interfaces LPM-PIO3 and LPM-7508 and MCM-7508 to Opto-22 rack

CBL-116-1 1 ft., 9 wire power supply cable, connects backplane to 9-pin Molex connector plug

CBL-117-1 1 ft., 9 wire power supply cable, connects power supply to 9-pin Molex socket

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CBL-118-3 3 ft. ribbon cable, 16-pin female socket connector with other end unterminated

CBL-119-3 3 ft. ribbon cable, 40-pin female socket connector with other end unterminated

CBL-120-3 3 ft. ribbon cable, 26-pin female socket connector with other end unterminated

CBL-121-6 6 ft. ribbon cable, 34-pin female socket connector with other end unterminated

CBL-122-1 1 ft. ribbon cable, 26-pin female socket to 25-pin female "D" adapter for Centronics line printer

CBL-123-1 1 ft. ribbon cable, 10-pin female socket to 9-pin male "D" adapter with AT style wiring convention for the RS-232 COM channels

CBL-124-1 1 ft. ribbon cable, 10-pin female socket to 5-pin DIN keyboard adapter cable

CBL-125-1 9 inch, 34-pin female socket cable from the MCM-DISK-AT to FD3-720

CBL-126-1 7 inch, 40-pin female socket cable from the MCM-DISK-AT to the HDAT-20, HDAT-40, HDAT-100 or HDAT-200

CBL-127-6 6 ft. ribbon cable, 40-pin female socket connector with other end unterminated

CBL-128-1 34-pin ribbon cable from the MCM-DISK-AT to the FD3-720 with no twist in cable

CBL-129-1 6 inch, 50-pin female socket cable from the MCM-SCSI to SCSI drive cable

CBL-129-4 4 ft. ribbon cable, 50-pin female socket cable for the MCM/LPM-DPRAM

CBL-130-1 4 inch, 26-pin female socket cable from the MCM-SBC40XT to keyboard interface

CBL-130-3 3 inch, 26-pin ribbon cable from the ADP-Analog to A/D boards

CBL-131-1 MCM-DISK-AT, MCM-FLP to one 3.5" and one 5.25" floppy disk drives

CBL-132-1 STD-AT local bus cable

CBL-133-1 XT-80 local bus cable

CBL-134-3 3 ft. ribbon cable, 34-pin female socket connector on each end

CBL-134-6 6 ft. ribbon cable, 34-pin female socket connector on each end

CBL-135-3 3 ft. ribbon cable, 34-pin female socket connector to 37-pin male "D" type connector

CBL-136-3 3 ft. ribbon cable, 34-pin female socket connector to 37-pin female "D" type connector

CBL-137-3 3 ft. ribbon cable, 20-pin female socket connector with the other end unterminated

CBL-138-3 3 ft. ribbon cable, 20-pin female socket connector to 37-pin female "D" type connector

WinSystems, Inc.

WinSystems' Cable Quick Reference Guide

Conductors	Part#	Termination 1	Termination 2	Length	Use
9	CBL-116-1	Tinned	Molex Plug	1 foot	Motherboard power cable
9	CBL-117-1	Tinned	Molex Socket	1 foot	Mate to CBL-116-1
10	CBL-107-3	10-pin ribbon	25-pin male "D"	3 feet	Serial Adapter
10	CBL-108-3	10-pin ribbon	25-pin female "D"	3 feet	Serial Adapter
10	CBL-123-1	10-pin ribbon	9-pin male "D"	1 foot	COM1 & COM 2 Adapter
10	CBL-124-1	10-pin ribbon	5-pin "D"	6 inch	Keyboard Adapter
14	CBL-105-3	14-pin ribbon	25-pin male "D"	3 feet	Serial Adapter
14	CBL-106-3	14-pin ribbon	25-pin female "D"	3 feet	Serial Adapter
16	CBL-103-3	16-pin ribbon	25-pin male "D"	3 feet	Serial Adapter
16	CBL-104-3	16-pin ribbon	25-pin female "D"	3 feet	Serial Adapter
16	CBL-118-3	16-pin ribbon	Unterminated	3 feet	General Purpose Breakout
16	CBL-132-1	16-pin ribbon	16-pin ribbon	1 foot	Local AT Bus
16	CBL-133-1	16-pin ribbon	16-pin ribbon	1 foot	Local XT Bus
20	CBL-137-3	20-pin ribbon	Unterminated	3 feet	D/A Output
20	CBL-138-3	20-pin ribbon	37-pin female "D"	3 feet	D/A Output
26	CBL-101-3	26-pin ribbon	25-pin male "D"	3 feet	Serial Adapter
26	CBL-102-3	26-pin ribbon	25-pin female "D"	3 feet	Serial Adapter
26	CBL-111-2	26-pin ribbon	Sony 3.5" Drive	2 feet	3.5" Floppy Disk (Z-80)
26	CBL-120-3	26-pin ribbon	Unterminated	3 feet	General Purpose Breakout
26	CBL-122-1	26-pin ribbon	25-pin female "D"	1 foot	Printer Adapter
26	CBL-130-1	26-pin ribbon	26-pin ribbon	4 inch	SBC40XT to Keyboard Adapter
26	CBL-130-3	26-pin ribbon	26-pin ribbon	3 feet	ADP-Analog to A/D boards
34	CBL-112-2	34-pin ribbon	5.25" floppy disk	2 feet	5.25" Floppy Disk (Z-80)
34	CBL-121-6	34-pin ribbon	Unterminated	6 feet	General Purpose Breakout
34	CBL-125-1	34-pin ribbon	34-pin ribbon	9 inch	DISK-AT to FD3-720 with twist
34	CBL-128-1	34-pin ribbon	34-pin ribbon	9 inch	DISK-AT to FD3-720 with no twist
34	CBL-131-1	34-pin ribbon	34-pin ribbon	18 inch	DISK-AT TO 3.5" & 5.25" Drive
34	CBL-134-3	34-pin ribbon	34-pin ribbon	3 feet	7614 Adapter
34	CBL-134-6	34-pin ribbon	34-pin ribbon	6 feet	PC-STD Bus Adapter
34	CBL-135-3	34-pin ribbon	37-pin male "D"	3 feet	7614 Adapter
34	CBL-136-3	34-pin ribbon	37-pin female "D"	3 feet	7614 Adapter
34	CBL-139-3	34-pin ribbon	34-pin ribbon	18 inch	Supports 2 FD3-720s in card cage
40	CBL-119-3	40-pin ribbon	Unterminated	3 feet	General Purpose Breakout
40	CBL-126-1	40-pin ribbon	40-pin ribbon	1 foot	DISK-AT to HDAT drive
40	CBL-127-6	40-pin ribbon	Unterminated	6 feet	General Purpose Breakout
50	CBL-109-2	50-pin ribbon	8" Disk Drive	2 feet	Connects two 8 inch disk drives
50	CBL-110-1	50-pin ribbon	50-pin ribbon	1 foot	Adapter to MCM-SBC
50	CBL-113-2	50-pin ribbon	8" Disk Drive	2 feet	8" drive to MCM-SBC
50	CBL-114-4	50-pin card edge	Card edge	4 feet	7507 to Opto 22 panel
50	CBL-115-4	50-pin ribbon	50-pin card edge	4 feet	7508 to Opto 22 panel
50	CBL-129-1	50-pin ribbon	50-pin ribbon	6 inch	SCSI to SCSI drive
50	CBL-129-4	50-pin ribbon	50-pin ribbon	4 feet	LPM/MCM-DPRAM cable

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FEATURES

- Termination boards for analog input, digital input, relay output and analog flow meters
- Convenient and reliable Phoenix-type connectors for field wiring termination
- Ribbon cabling directly compatible with WinSystems' Single Board Computers or individual I/O cards
- All boards are the same small size (4.1" x 5.65") for versatile, common mounting configuration
- Low cost
- Extended temperature operation

WinSystems offers a series of termination boards that provide connection and signal conditioning from field wiring. These boards will work both with our STD Bus I/O cards and standalone Single Board Computers such as the SBC25 and SBC88. These boards are small, only 4.1 x 5.65 inches. All termination boards are the same size and mounting style so that the same physical dimension is required for ease of mechanical layout and packaging while offering excellent config-uration flexibility.

FUNCTIONAL CAPABILITY

Termination Boards - The boards are offered with analog input (TRM-100-XX), digital input (TRM-200-XX), digital output (TRM-300-XX), digital input/output (TRM-400-XX), and flow meter input (TRM-500-XX) signal conditioning. The XX refers to the number of channels supported by the board. The boards are listed with the standard population options; however, they can be modified (fewer channels) for OEMs if required. Please contact the factory for pricing and availability.

The boards accept a Phoenix pluggable connector from the field wiring to insure a reliable connection with easy removal and insertion. Output is directed to a ribbon cable connector for input to the Single Board Computer or I/O board.

Mounting Configuration - The analog termination board has a hole in each corner of the board that will accept 6-32 screws.

TRM-100-16: Analog Input Terminator
The TRM-100-16 is a non-isolated, 16 channel, analog signal conditioning board for use with WinSystems' STD Bus analog to digital converters. It provides a termination options for single ended and pseudo
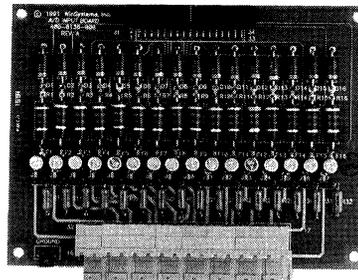
differential analog input signals plus serves as a field wiring to ribbon cable adapter.

The TRM-100-16 is designed to accept either 0 to +5V or 4 to 20mA inputs. The input configuration is jumper selectable on a per channel basis. A transorb and in-line fuse provide transient and short circuit protection.

An optional 250 ohm shunt resistor permits a voltage to be generated by current loop sensors. With 4 to 20 mA systems, a 250 ohm close tolerance resistor is installed. The amount of voltage drop is directly proportional to the current flowing through the shunting resistor. A 4 mA current will result in a 1 volt signal and a 20 mA will result in a 5 volt signal.

The output of the board is to a 34-pin right angle header that will accept an CBL-134-3, 34-pin ribbon cable (or equivalent). The pin-out will work with WinSystems' SBC25, SBC88, MCM-1260, and LPM-1280 cards.

TRM-200-16: Digital Input Terminator
The TRM-200-16 card provides protection for 16 channels of digital (status) input. The input lines are buffered through a passive network consisting of an in-line fuse, transorb and current limiting resistor.
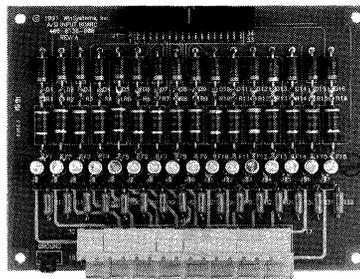
The output of the board is to a 34-pin right angle header. It will work with the LPM/MCM-7614 and SBC88 Single Board Computer.

TRM-300-16: Digital Output Terminator

The TRM-300-16 is a board with sixteen 1 Form C relays on board. The relays have a low pick-up power and will switch up to 2 Amps at 30 VDC. They have a breakdown voltage of 1500V FCC surge between open contacts and 1000 VAC between open contacts. Both the normally open and normally closed contacts are brought to the terminal block. A LED is provided for each channel to show if the relay has been activated.

The output of the board is to a 34-pin right angle header. It will work directly with the LPM/MCM-7614 and SBC88. Other boards are supported if an adapter cable is made. Please contact the factory for more information.

TRM-500-3 : Flow Meter Input Terminator

The TRM-500 is a signal conditioning unit for up to three flow meters. It accepts a low level input and provides a TTL level that is accepted by the timers on the SBC88 and LPM/MCM-CTC board. A jumper block is available to allow selection of either a low level analog or TTL input on each channel. Three independent channels are supported.

The output of the board is to a 34-pin right angle header. It will work directly with the LPM/MCM-7614 and SBC88. Other boards are supported if an adapter cable is made. Please contact the factory for more information.

TRM-400-88: Digital Input/Output Terminator

The TRM-400-88 board is a combination of the TRM-200-XX and TRM-300-XX board. It duplicates the 8 channels of the digital input protection network, and 8 channel of digital output.

SPECIFICATIONS

Mechanical
Dimensions: 4.1" x 5.65"
PC Board: FR4, 0.62 inches thick

Environmental
Temperature Range: -40°C to +85°C

ORDERING INFORMATION

WinSystems, Inc.

Single Board Computers

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FEATURES

- NEC V25 based 80C88 CMOS Single board controller
- Eight 32-pin memory sockets for up to 1024K RAM battery backed RAM, EPROM or EEPROM
- Two SBX connectors for additional I/O expansion
- Very low power consumption with special power off circuitry during idle conditions
- Up to thirty-two 12-bit A/D channels with 0 to +5V or 0 to +10V or single ended or 16 differential inputs
- Two 12-bit D/A channels; 0 - 5 volts
- Two RS-232 serial asynchronous communications channels plus RS-422/485 optional on channel 1
- 24 digital I/O lines
- Centronics parallel printer port
- Programmable interrupt controller
- Alternative register bank for fast context switching
- Two independent 16-bit timers
- Programmable time base counter
- Watchdog timer
- Two standby modes: HALT and STOP
- Jumper selectable power sequence circuit
- Programmable WAIT state generator
- Extended temperature operation: -40° to +85°C

The SBC25 is a small, universal single board computer designed to operate at extremely low power levels over extended temperature ranges in order to acquire,
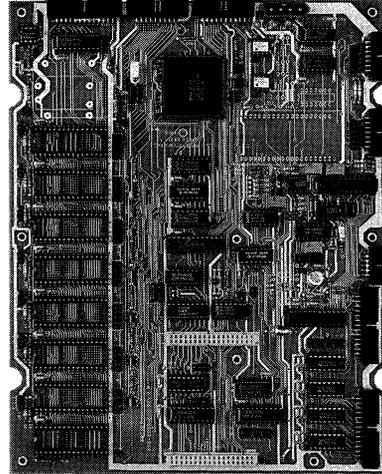
collect, process and transmit data via a modem, RF or other data link.

The SBC25 is ideal for pipeline monitoring, data logging, transportation, production floor monitoring, process control and other harsh industrial applications.
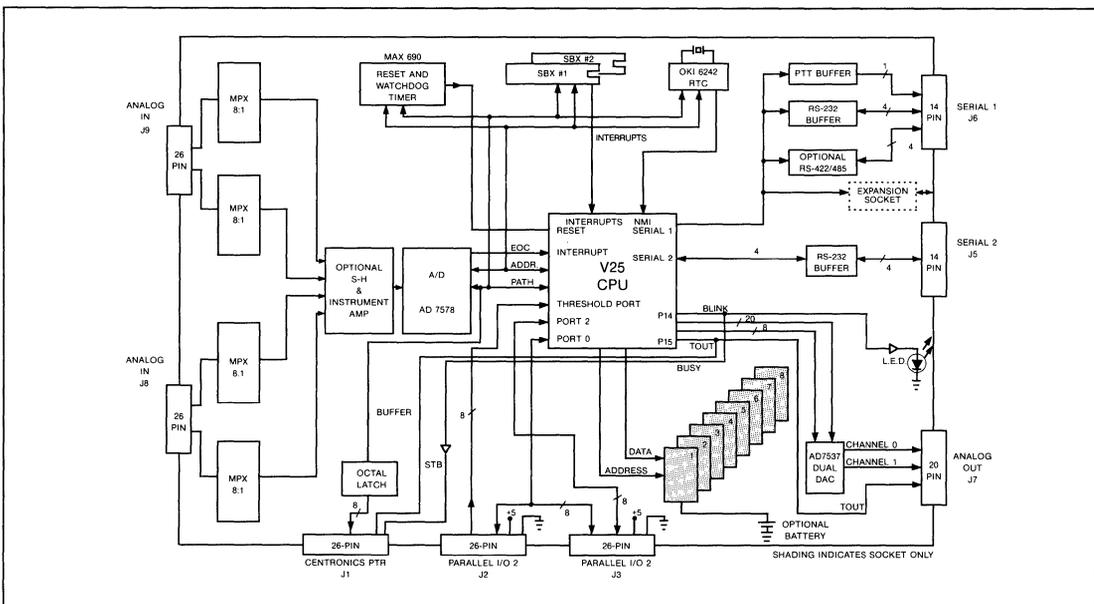
FUNCTIONAL CAPABILITY

Processor - The V25 is the CPU for the SBC25. It is a high performance 16-bit single chip microcomputer combining the power of the 80C88 CPU with many of its associated peripherals. It is fully software compatible with the 80C88. It has improved performance over the 80C88 by virtue of its pipelined architecture, 4 byte instruction prefetch queue, dual internal 16-bit data bus, and powerful instruction superset including bit processing, 8 and 16-bit signed and unsigned arithmetic in binary and BCD including high speed multiplication/division instructions. It has faster memory accessing, superior interrupt processing ability, and enhanced control of internal peripherals. Eight banks of registers are mapped into internal RAM below an additional 256 byte special function register (SFR) area that is used to control on-chip peripherals. Speed improvements are obtained by architectural enhancements such as a dual data bus, 16/32 bit temporary registers/shifters, 16-bit loop counter, and program counter and prefetch pointer.

On-chip peripherals include two 16-bit timers, 2 serial asynchronous, full-duplex UART's, 24 parallel I/O lines, 256 byte internal RAM storage, 2 channel DMA, WAIT state generator and interrupt controller. Also either a Mask ROM or EPROM are available on the chip or special dedicated applications.

The V25 runs all the 8088 instructions and operates at 5 MHz. For a detailed data sheet on the V25 CPU, call NEC Electronics at 1-800-632-3531 or 415-960-6000 and ask for publication 500233.

Sleep Mode - The SBC25 operates in 2 Sleep modes: HALT and STOP. In the normal active operational mode the SBC25 draws an average of 100 mA. When data collection and transmission is complete, it can be set to a "Sleep" mode. The Sleep mode requires approximately 2.5 mA in the STOP mode and approximately 50 mA in the HALT mode. This number is subject to change depending upon the population of the analog I/O, SBX boards, Status LED, and whether RS-422/485 drivers are installed.

The Sleep mode is executed by issuing a STOP mode command in the processor. This mode allows the largest power reduction while maintaining RAM. The oscillator is stopped, halting all internal peripherals. Internal status is maintained. Only a RESET or NMI can release this mode. The NMI is jumper selectable and controlled by the OKI 6242 RTC. It takes approximately 50 mS for the oscillator and V25 to become operational again after release.

In the HALT mode, the processor is inactive and the chip consumes approximately 50% less power than when operational. The external oscillator remains functional and all peripherals are active. Internal status and output port lines are maintained. Any masked interrupt can release this mode.

The absolute lowest power operation is obtained by "Waking up" the processor, sampling and transmitting the data and then returning dormant in the "Sleep" state until the next sample period.

A standby flag in the SFR area of the V25 is reset by rises in the supply voltage. The flag is set when its status is read. Its status is maintained during normal operation and standby and is used to determine whether program execution is returning from standby or from a cold start.

Memory - The V25 processor chip is available with 256 bytes of internal RAM and 16K bytes of either mask programmable, one time programmable or UV erasable EPROM or no EPROM on the chip. The SBC25 standard configuration is with no EPROM or mask ROM internal to the V25 chip. All memory is available through the eight 32-pin JEDEC sockets on board. The sockets will each accept up to 128K byte static RAMs and EPROMs in any mix for a total of 1024K bytes of memory which is the maximum address space of the V25. Either 28 or 32-pin devices can be plugged into the sockets. The sockets are jumper configurable for 32K, 64K, and 128K byte evices. The board will support EEPROMs and can also support low power battery backed RAMs with an optional onboard 750 mAH or 1.5 Amp hour battery.

Memory mapping is done with an EPLD. Additional application specific maps can be generated either by the customer or by WinSystems.

Wait States can be generated to allow direct interface to slower memory devices whose access times cannot meet the CPU read/write timing requirements. The entire 1 Mbyte memory map is divided into 128K blocks. Each block can be programmed for zero, one or two Wait States. Therefore only a specific memory area is slowed, not all memory accesses.

Serial Communications - Two independent, full-duplex UART's are on the SBC25. It supports 7 or 8-bit character lengths, 1 or 2 stop bits, and even, odd, or no parity. Each channel has its own baud rate generator capable of all the standard data transfer rates up to 1.25Mb/s. Request to Send (RTS) is controlled by bits 6 or 7 in Port 1. In addition an

optional reed relay is available for use as a Push to Talk (PTT) output for transmitter keying on channel 1 only. A Clear to Send (CTS) input line is available for handshaking to each serial port. Both ports use RS-232 signal levels while channel 1 can be optionally populated to support RS-422/485.

The RS-422/485 interface uses 75176B devices. These units require high current and should be depopulated for the lowest possible current operation. The RS-422/485 is used in applications requiring long cable lengths, high noise immunity, or high data rates.

Each channel is jumper configurable as either Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) with modem handshake lines (RTS and CTS). Both RS-232 and RS-422/485 signals are wired to their respective 14-pin right angle connectors. This allows easy, direct 1:1 connections between flat cables with 25-pin "D" type connectors such as the WinSystems' CBL-103-3 male and CBL-104-3 female ribbon cables.

Serial Channel 1

Pin	Signal
1	Ground
2	Transmit Data
3	Receive Data
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Ground
14	RS-422/485 Tx +
15	RS-422/485 Tx -
16	RS-422/485 Rx +
17	RS-422/485 Rx -
18	Push to Talk (PTT)
19	Push to Talk (PTT)
20	Data Terminal Ready (DTR)

Serial Channel 2

Pin	Signal
1	Ground
2	Transmit Data
3	Receive Data
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Ground
20	Data Terminal Ready (DTR)

Analog Signal Conversion - The SBC25 uses an Analog Devices' AD7578 successive approximation CMOS 12-bit analog to digital converter for use in data acquisition. Conversion time is 125 micro-

seconds. The card accepts a 0 to +5 volt or 0 to +10V unipolar inputs from various analog sources. Signal conditioning must be done off board. Up to 32 single ended or 16 differential analog inputs can be measured. An optional sample and hold circuit is available to narrow the sample window. An optional instrumentation amplifier is required for differential operation.

The SBC25 contains up to four 8 channel CMOS Analog Multiplexers with overvoltage protection. The multiplexer inputs can withstand 10V greater than either supply with the power off, which eliminates the possibility of damage when supplies are off. Equally important, they can withstand brief input transient spikes which would otherwise require complex protection networks.

A/D conversion is begun each time the channel number is written to the multiplexer. An end-of-conversion signal can generate an interrupt, (INTP2, P1-3) to the V25 CPU.

Two 26-pin right angle input connectors are configured the same as WinSystems' CMOS STD Bus standard LPM-1280 board and will directly interface to the Analog Devices' 3B and 5B Termination networks. The first connector inputs channels 0 through 15 and the second connector inputs channels 16 through 31. These modules are high performance signal conditioners designed for industrial applications. They incorporate a transformer-based isolation design in a compact module housing. Various modules can be mixed, permitting users to address their exact needs without disturbing field wiring. The modules include isolated high level input, thermocouple, RTDs, mV, Volt, and 20 mA inputs. Contact Analog Devices for further information.

Analog Input Connector 1

Pin	Description	Pin	Description
1	CH0 (CH0 High)	2	CH8 (CH0 Low)
3	Common	4	CH9 (CH1 Low)
5	CH1 (CH1 High)	6	Common
7	CH2 (CH2 High)	8	CH10 (CH2 Low)
9	Common	10	CH11 (CH3 Low)
11	CH3 (CH3 High)	12	Common
13	CH4 (CH4 High)	14	CH12 (CH4 Low)
15	Common	16	CH13 (CH5 Low)
17	CH5 (CH5 High)	18	Common
19	CH6 (CH6 High)	20	CH14 (CH6 Low)
21	Common	22	CH15 (CH7 Low)
23	CH7 (CH7 High)	24	Common
25	N/C	26	N/C

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Analog Input Connector 2

Pin	Description	Pin	Description
1	CH8 (CH8 High)	2	CH24 (CH8 Low)
3	Common	4	CH25 (CH9 Low)
5	CH9 (CH9 High)	6	Common
7	CH10 (CH10 High)	8	CH26 (CH10 Low)
9	Common	10	CH27 (CH11 Low)
11	CH11 (CH11 High)	12	Common
13	CH12 (CH12 High)	14	CH28 (CH12 Low)
15	Common	16	CH29 (CH13 Low)
17	CH13 (CH13 High)	18	Common
19	CH14 (CH14 High)	20	CH30 (CH14 Low)
21	Common	22	CH31 (CH15 Low)
23	CH15 (CH15 High)	24	Common
25	N/C	26	N/C

Analog Output - The SBC25 contains an optional Analog Devices' AD7537 Dual 12-bit DAC. Two independent DACs are on one monolithic chip configured to provide two 0 - 5 volt outputs. The input section is double buffered to allow simultaneous update of both DAC's. The settling time is 10 microseconds. Each output channel is wired to a 10-pin right angle male connector which is the same pin out as the LPM-AIO. Flat ribbon or discreet wires can be connected to it. Alternating ground lines, paired with each output channel's signal line, improves noise immunity and reduces cross-talk.

Analog Output Connector

Pin	Description
1	Channel 0
3	Channel 1
5,7	Ground
9	TOUT (buffered P1-5)
Even Pins	Ground

Parallel I/O - The SBC25 has 16 input/output lines and 8 input lines for a total of 24. The parallel I/O is provided through a 82C55 type device onboard the V25 chip. The input/output lines have individual set/reset capability. Only port P0 and P2 are used for I/O. P1 is dedicated for external interrupt capability, RTS control, LED output and timer output. P2 must be shared if DMA is used on the iSBX modules.

Eight additional input only lines are available through the threshold comparator port which are tied to pull up resistors to prevent them from floating.

The sixteen I/O lines are broken into 2 groups of 8 and wired to 2 separate 20-pin connectors. The 8 I/O lines I/O 1 through I/O 8 are wired to both connectors with duplicate functions. Pull-up resistors are provided on each to prevent them from floating with no connection. The input only port is accessed through Connector 1 only and I/O 9 through I/O 16

are accessed through Connector 2 only. Power and ground are supplied at symmetrical pins (1 and 11) and (10 and 20) to power external interfaces.

Parallel I/O Connector 1

Pin	Description	Pin	Description
1	+ 5 V	2	IN 1
3	IN 2	4	IN 3
5	IN 4	6	IN 5
7	IN 6	8	IN 7
9	IN 8	10	Ground
11	+ 5 V	12	I/O 1
13	I/O 2	14	I/O 3
15	I/O 4	16	I/O 5
17	I/O 6	18	I/O 7
19	I/O 8	20	Ground

Parallel I/O Connector 2

Pin	Description	Pin	Description
1	+5 V	2	I/O 9
3	I/O 10	4	I/O 11
5	I/O 12	6	I/O 13
7	I/O 14	8	I/O 15
9	I/O 16	10	Ground
11	+ 5 V	12	I/O 1
13	I/O 2	14	I/O 3
15	I/O 4	16	I/O 5
17	I/O 6	18	I/O 7
19	I/O 8	20	Ground

The SBC25 has a Centronics printer interface using a 74HC273 as a latching octal driver for the 8 data bits. It is the most widely accepted byte-wide interface for computer-to-printer communications. The interface has 8 lines which carry their respective binary bits in parallel. The transmission of these data bits is controlled by the negative edge of the STROBE pulse. The Busy line is monitored that indicates the printer cannot receive data. This port can also be used as a general purpose output port if no printer is required in the system.

The data is wired to a 26-pin right angle connector with the pinout as shown below.

Centronics Parallel Printer Port

Pin	Description
1	STROBE
2	DATA 1
3	DATA 2
4	DATA 3
5	DATA 4
6	DATA 5
7	DATA 6
8	DATA 7
9	DATA 8
11	BUSY
18-25	GROUND

Timers - There are two independent software programmable 16-bit timers internal to the V25 to solve most of the timing problems in microcomputer systems design. These counter/timers are in addition to the baud rate generators for the serial channels. Each of the two 16-bit timer registers has an associated 16-bit modulus register. Timer 0 operates in the interval timer mode or one-shot mode; Timer 1 has only the interval timer mode. The output of Timer 0 is wired to pin 9 of the analog output connector to provide a periodic output function.

A 20-bit free-running time base counter controls internal timing sequences and is available to the user as the source of periodic interrupts at lengthy intervals.

Real Time Clock - An OKI MSM6242 clock calendar is on board. The chip keeps track of seconds, minutes, hours, days of week, date, month, and years. It can operate in either a 12/24 hour format and Leap Year timing is automatic. An onboard 32.768 KHz crystal oscillator determines the time base. It can be battery powered by an optional external battery attached to the board.

The RTC can generate a software selectable interrupt of 1/64 second, 1 second, 1 minute, or 1 hour. This signal is jumper selectable as the NMI input of the V25 CPU to "wake up" or release the processor from the STOP or HALT Mode.

Interrupts - An on-board Programmable Interrupt Controller (PIC) provides priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts can be generated from the 12 internal and 5 external sources including the 2 serial channels, iSBX connectors, timers, A/D converter and NMI. The 3 external interrupt interrupt sources are maskable and edge sensitive and can be selected individually for either the falling edge or rising edge. With the exception of NMI, INT, and INTTB, the interrupts can be processed in any of 3 modes: standard vector interrupt, register context switching, or macro service for high performance operation.

Watchdog Timer - A Maxim MAX690 supervisory circuit serves as a programmable retriggerable watchdog timer. This is important for use in remote and unattended applications. The circuit must be toggled at least once every 1.5 seconds to verify proper software execution. If it is not toggled in time, then the circuit assumes either a hardware or software failure and it restores the V25 to a known condition

by issuing a 50 mS RESET pulse. The watchdog timer output is disabled by a jumper option. RESET will release the V25 CPU from the STOP or HALT mode.

Battery Back-up - Either an optional 750 mAH or 1.5 AH battery can be supplied with the SBC-25 board to provide power for the real time clock and up to 7 RAM memory sockets. The SBC-25 has special circuitry to support both the low power 32K and 128K byte RAM's. A MAX690 supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or stand-by voltage to the calendar clock and the RAM's selected for backup. The battery automatically switches ON when the Vcc of the systems drops below the battery voltage and and back OFF again when Vcc returns to normal.

Reset - A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage status. Upon detection of an out-of-tolerance condition, a RESET is generated. This is critically important in order to detect brown-out or power fail conditions. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to battery backed RAMs or EEPROMs during power fluctuations.

System Expansion - Two 8-bit iSBX multimodule connectors are provided to accommodate interrupt driven I/O expansion modules. These can be either interrupt or DMA driven devices. They can support special purpose peripheral functions such as a AMD9511 high speed math processor, A/D and D/A converters, networking, counter/timer/accumulators, motion control, serial channels and other special purpose peripheral functions.

Status LED - A programmable status LED is available on the top of the board to monitor system activity. It can be programmed to provide a visual indication of the status of a program by turning it on and off at the desired intervals through Port 1 bit 4. This LED is removed for systems requiring the absolute lowest amount of power.

CTR-M-SBC25 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C for use with the SBC25. CTR is designed specifically for embedded systems applications development. It allows one to debug C source, assembly language, or mixed code. The debugger provides excellent visibility through its CodeView

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style windows for source, commands, registers, and expressions. All hardware and software is included to allow any PC-XT/AT compatible computer to function as a development workstation while being linked to the target SBC for direct real time debugging by the source level debugger.

SBC25 Configuration - The SBC25 offers tremendous flexibility for a host of different applications. To be cost effective, WinSystems offers a variety of population options to custom tailor the board to your needs. Specifically, the Analog I/O, Real Time Clock, and battery can be depopulated to reduce the cost. This configuration is called the CDU-25. Contact the factory with your specific configuration.

SPECIFICATIONS

Electrical

System Clock: 5.0 MHz
Serial Interface: RS-232 both channels; RS-422/485
                 channel 1 only

Power Requirements (without memory installed)
Vcc = +5V $\pm$ 10% at 160 mA typ.
    = +15 $\pm$ 10% at 20 mA
    = -15V $\pm$ 10% at 20 mA

Without RS-422/485 Drivers

Vcc = +5V $\pm$ 10% at 100 mA typ.
    = +15 $\pm$ 10% at 20 mA
    = -15V $\pm$ 10% at 20 mA

Memory

Addressing: 1 Megabyte
Capacity: Supports 32K, 64K, and 128K byte 32-pin
          RAM, ROM, EPROM, and EEPROMs.

Mechanical

Dimensions: 8 x 10 inches
Jumpers: 0.025" square posts

Connectors

Serial I/O: 14-pin 0.100" grid
Serial I/O: 14-pin 0.100" grid
Parallel I/O: 26-pin 0.100" grid
Parallel I/O: 26-pin 0.100" grid
Analog Input: 26-pin 0.100" grid
Analog Input: 26-pin 0.100" grid
Analog Output: 10-pin 0.100" grid
iSBX Multimodule: 36-pin 0.100" dual row female
iSBX Multimodule: 36-pin 0.100" dual row female
Printer I/O: 26-pin 0.100" grid

Environmental

Operating Temperature: -40° to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

SBC25	V25 Single board computer
CDU-25	Depopulated version of the SBC25 with no analog conversion capability or SBX modules
CTR-M-SBC25	Remote C and assembly language source level debugger
CTR-M-CDU-25	Remote C and assembly language source level debugger

WinSystems, Inc.

FEATURES

- 80C88 based CMOS single board computer
- Eight 32-pin memory sockets support 1024KB of RAM, RAM, EPROM or EEPROM
- 8087 coprocessor socket
- Battery backed RAM and clock
- Sixteen 12-bit A/D channels with 0 to +10V or 0 to +5V single ended or 8 differential inputs
- Four RS-232 serial communications channels using 85C30 SCC with sync/async operation
- 48 digital I/O lines (two 82C55's)
- 8 channel programmable interrupt controller
- Six independent 16-bit counter/timers (82C54's)
- Watchdog timer
- 2 SBX connectors for I/O expansion
- Low power consumption
- Real time clock
- Precision powerfail reset
- Symbolic C Debugger supported
- ROM-DOS supported
- Expansion to STD Bus card cage
- Temperature range: -40°C to +85°C
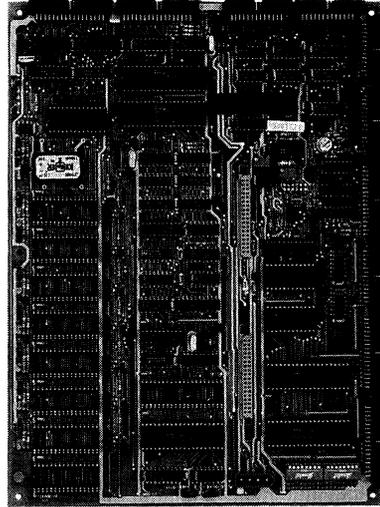
The SBC88 is a small, low cost, universal single board computer designed for embedded control applications. The SBC88 will operate at low power levels over extended temperature ranges in order to acquire, collect, process and transmit data via a modem, RF or other data link. It is ideal for remote and unattended applications such as pipeline monitoring, SCADA, signaling/communications and on the factory floor. It has a wealth of standard features plus CMOS STD Bus I/O expansion capability.
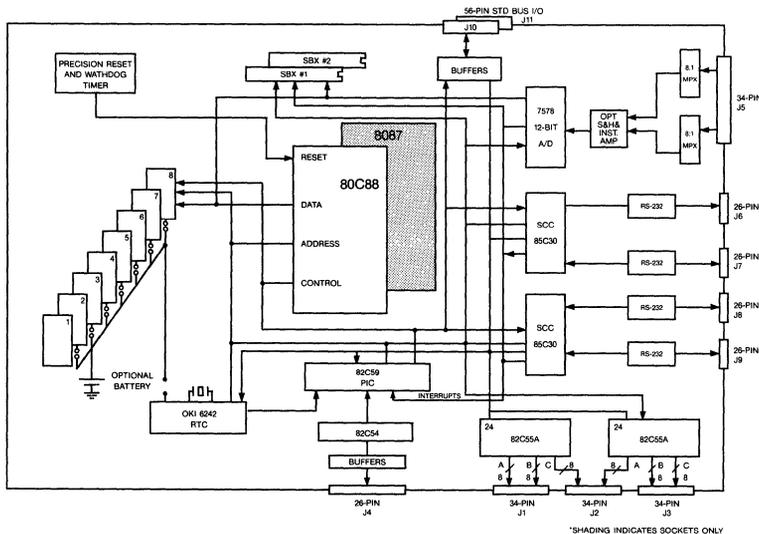
The SBC88 is the equivalent of 6 WinSystems' CMOS STD Bus cards (LPM-SBC8-8, LPM-UMC4, LPM-7314, LPM-CTC, LPM-7614, and LPM-1280) integrated onto one single board computer. The SBC88 contains a V20 (80C88) CPU, 1024KByte CMOS memory capability (8 sockets), 8087 coprocessor socket, 4 serial RS-232 channels, 48 parallel I/O lines, 8 channel interrupt controller, 6 counter/timers, real time clock, 16 channel single ended 12-bit A/D converter (8 channel differential optional). SBX connectors are onboard to provide additional expansion capability for serial I/O, interval timers, D/A converters, and other I/O functions.

Different population options are available to custom configure the board for a specific application.

FUNCTIONAL CAPABILITY

Processor - The SBC88 incorporates the popular 16-bit, 8 MHz, CMOS 80C88 processor which has a 1 MB memory address capability. WinSystems uses the NEC V20 standard since it 100% code compatible plus executes faster than the 80C88 due to its pipelined architecture. It also has a more powerful instruction superset for bit processing and engineering control applications.

8087 Coprocessor - The SBC88 is configured to support a customer supplied 8087 which provides up to 100 times the math performance of the CPU alone.

Memory - Eight 32-pin bytewide memory sockets are available to accept up to 1024K bytes of memory. SRAMs, EPROMs, or EEPROMs are supported. Seven of the 8 sockets will accept 32KB or 128KB battery-backed RAMs. An optional 750 mAH or 1500 mAH battery is onboard for both the memory devices and real time clock.

Serial I/O - Four serial RS-232 channels are provided through two 85C30 SCCs. They are wired to four 26-pin connectors that will adapt directly to DB-25 connectors. The SBC88 will support both synchronous, asynchronous, and "long asynchronous" modes for signaling and communications with multiple independent baud rates. An optional special adapter board will permits 2 of the 4 channels to be configured to support RS-485 levels.

Parallel I/O - The digital I/O is provided via two 82C55 devices. Each 82C55 supports 24 I/O pins which may be individually programmed in 2 groups of 12 in three major modes of operation. There is also a direct bit set/reset capability for control application interface requirements to Opto-22 type interface

panels. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. The 48 lines are wired to 3 connectors (2 ports per connector). The last 16 lines can be wired either to the third connector (standard factory configuration) or with two 8 position DIP switches on the board.

A/D Conversion - A 12-bit 125 uS A/D converter supports 16 single ended or 8 differential 0 to 10V or 0 to 5V inputs. The connectors for the A/D are wired to allow direct connection to Analog Devices' 3B and 5B type signal conditioning modules.

Counter/Timers - There are six independent, software programmable, 16-bit counter/timers available through two 82C54A devices. The clock, gate and output lines are buffered and wired to a connector on the edge of the board for external access.

Interrupts - An onboard master 82C59A type Programmable Interrupt Controller (PIC) provides 8 maskable, vectored, priority interrupts for quick response to various interrupt conditions for real time systems. Vectored interrupts are jumper selectable from the serial channels, RTC, 8087, counter/timers, SBX connectors, or the A/D.

Multimodule Interface - Two single iSBX Multimodule connector is provided to accommodate a single-wide, 36-pin (8-bit) I/O expansion module. SBX modules are available for custom I/O expansion such as serial I/O, parallel I/O, disk controllers, A/D, D/A and other special purpose controllers.

Real Time Clock - A MSM6242 clock calendar is on the SBC88 to provide clock, date, and periodic interrupts to the system. It is battery backed from the optional battery installed onboard.

Watchdog Timer - A jumper selectable, programmable, retriggerable watchdog timer is provided. This circuit is important for use in remote and unattended applications. A precision reset circuit is also integrated into the card to accurately determine the Vcc status and reset the card properly upon an out-of-tolerance condition.

STD Bus Expansion - An interface is provided to permit expansion of the SBC88 to an STD Bus card cage if additional I/O cards are required.

Power - The entire card is CMOS and requires less than 1 Watt. The board requires +5 and $\pm$/-12 volts. The temperature range is -40° to +85°C.

Configuration - To be cost effective, WinSystems offers a variety of population options to custom tailor the SBC88 to your needs. Contact the factory with your specific requirement.

SOFTWARE SUPPORT

C-THRU-ROM-SBC88 - C-THRU-ROM (CTR) is an optional comprehensive, full featured integrated debugging package for generating standalone ROMable programs with Microsoft C for use with the SBC88. C-THRU-ROM allows the user to debug programs at the source level on the actual WinSystems' target hardware in real time, link programs with startup code designed for use with a non-DOS embedded system, and locate code and data anywhere in the 80X86/88 address space. CTR allows the user to locate the debugged software and generate code suitable for programming EPROMs. The debugger provides excellent visibility through its CodeView style windows for source, commands, registers, and expressions.

ROM-DOS - ROM-DOS is a MS-DOS 3.2 compatible ROM based operating system for embedded SBC88 applications. ROM-DOS provides 3 major functions: hardware initialization, file support and standard software drivers. ROM-DOS reduces the ROM, RAM and hardware requirements while providing a flexible application environment that allows the running of standard PC files on non-PC hardware in an embedded environment. It does not require keyboard, video or rotational media to function which is ideal for embedded control applications.

ORDERING INFORMATION

SBC88-1	8MHz CMOS Single Board Computer
SBC88-2	8MHz CMOS Single Board Computer without A/D circuitry
SBC88R-1	SBC88-1 with ROM-DOS
SBC88R-2	SBC88-2 with ROM-DOS
CTR-M-SBC88	CTR for MicroSoft C on the SBC88
CTR-KM-SBC88	CTR Kernel for MicroSoft C on the SBC88
RDOS-SBC88R	ROM-DOS for the SBC88

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WinSystems, Inc.

SBX Modules

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FEATURES

- Low cost, 12-bit A/D
- Up to 8 input channels
- Each channel configurable for Unipolar (0 to +5V) or Bipolar (-2.5 to +2.5V)
- Built-in Sample-and-Hold
- 100KHz sampling rate
- I/O mapped on the SBX Bus
- Processor independent
- Small size: 2.85" x 3.7"
- Very low power, all CMOS components
- Optional extended temperature range: -40°C to 85°C

The SBX-A/D12 card provides up to eight channels of 12-bit analog input on a single SBX module. Any channel can be configured as unipolar or bipolar for maximum flexibility. The board is designed to serve as a complete data acquisition system with a 100KHz sampling rate.

FUNCTIONAL CAPABILITY

SBX Bus Interface - The SBX-A/D12 is I/O port mapped with the unique port address determined by the base board. Two blocks of 8 I/O ports are reserved for the SBX multi-module decoding. The SBX-A/D12 is designed to work with standard NMOS/TTL or CMOS base boards.
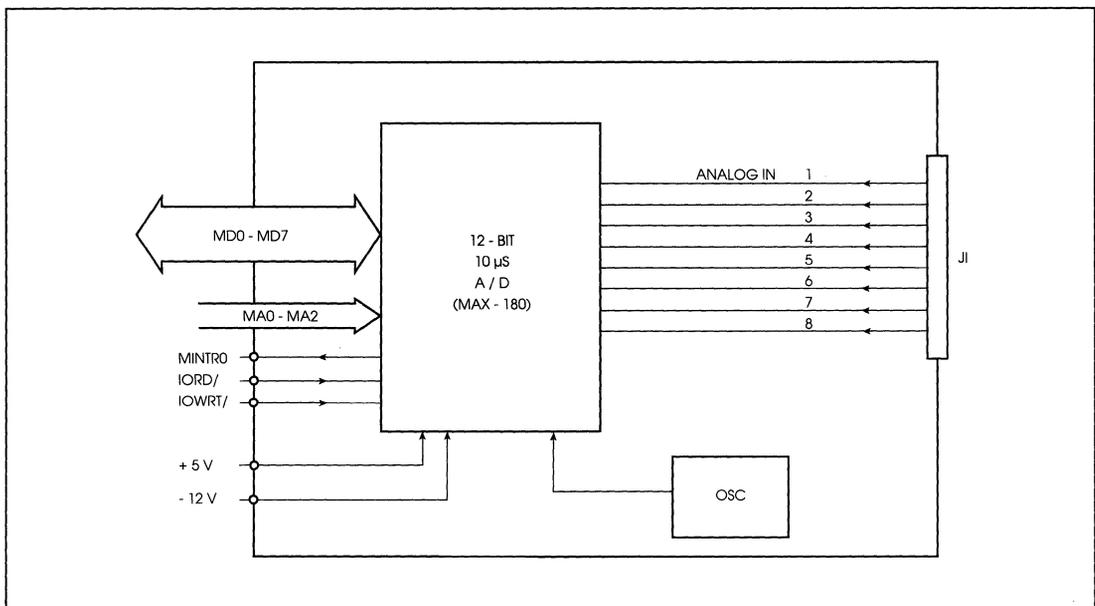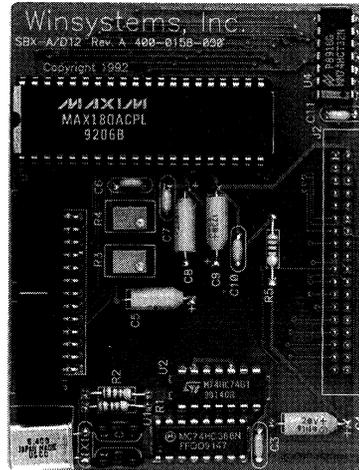
Analog to Digital Converter - The SBX-A/D12 contains the Maxim MAX180, 12-bit data acquisition system. It combines an 8 channel input multiplexer, high bandwidth Sample-and-Hold, low-drift zener reference, and flexible microprocessor interface with a high conversion speed, successive approximation analog to digital converter. The device samples and digitizes at an 100KHz throughput rate.

The MAX180 can be software configured for unipolar or bipolar conversions and single-ended or differential inputs on a per channel basis. Output coding is natural binary for unipolar operation with 1 LSB = 1.22mV (5V/4096). Coding is twos complement for bipolar.

Potentiometers are on the card to permit both gain and offset adjustment.

Starting a conversion - The conversion is begun by writing a word to the control register to select the channel and specify if it is single-ended/differential and unipolar/bipolar. Output data is latched and the SBX-A/D12 signals the base board that conversion is complete and data is available. This board sets a Busy flag for use in a polled mode and can generate an interrupt after each completed conversion.

Input Configuration - Each input channel is wired to J1, a 26-pin right angle male connector. It has the same pin-out as WinSystems' LPM/MCM-A/D12. J1 is configured so that mass termination type flat ribbon cable or discreet wires can be connected to it.

WinSystems offers the CBL-120-3 which is a 3 foot, #28 AWG, ribbon cable designed to provide access to signals from the 26-pin, 0.100″ grid connector on the SBX-A/D12 board. One end of the cable has a polarized, 26-pin female socket connector with strain relief that plugs into the board and the other end is open to allow users to make their own custom termination.

The CBL-130-4 is a 4 foot, ribbon cable that will connect the SBX-A/D12 to the Analog-ADP. This board is a non-isolated signal conditioner and termination panel.

Extended temperature operation - WinSystems can optionally populate the board to operate from -40° to 85° Centigrade. Contact the factory for the part number and availability.

Multimodules - SBX multimodule boards are small (3.70″ x 2.85″), I/O mapped boards which plug into a base board. The SBX boards connect to the SBX bus connector and convert the SBX bus signals to a defined I/O interface. The multimodule is a unique design approach to STD Bus users offering a broad range of expansion boards joined together on the SBX interface. The SBX-A/D12 is designed to fit on all WinSystems' processors, our LPM/MCM-SBX expansion card, and other base boards.

SPECIFICATIONS

Electrical
Number of Channels: Up to 8
A/D Resolution: 12-bits
Input range: 0 to +5 volts; single-ended
-2.5 to +2.5 volts; differential
Coding: Natural binary (unipolar)
Twos' complement (bipolar)
Nonlinearity: ± 1 LSB
Gain error: Adjustable to zero
Conversion speed: 10 microseconds
Power Requirements:
+5 VDC +5% at 10 mA (typ.)
-12 VDC +10% at 10 mA (typ.)

Mechanical
Dimensions: 2.85″ x 3.7″

Connectors
Input: 26-pin dual on 0.100 grid
SBX: 18/36-pin dual 0.100″ dual row male

Environmental
Operational Temperature: 0°C to +65°C

ORDERING INFORMATION

SBX-A/D12	12-bit A/D converter
CBL-120-3	3 ft., 26 conductor ribbon cable unterminated
CBL-130-4	4 ft., 26 conductor, ribbon cable to the Analog-ADP card
Analog-ADP	Analog termination panel

WinSystems, Inc.

FEATURES

- Two independent analog voltage output channels
- Two output voltage ranges:
      0 to +5V and ±5V
- I/O mapped on the SBX Bus
- Processor independent
- Small size: 2.85" x 3.7"
- Very low power, all CMOS components
- Extended temperature operation:
      -25°C to 85°C

The SBX-D/A12 card provides two, 12-bit independent analog voltage output channels. Each channel can be configured for one of 2 ranges. The SBX-D/A12 is I/O mapped only and is designed to run in the 8-bit mode on the iSBX Bus.

FUNCTIONAL CAPABILITY

SBX Bus Interface - The SBX-D/A12 is I/O port mapped with each channel having a unique port address determined by the base board. Two blocks of 8 I/O ports are reserved for the SBX multi-module decoding. This board only uses the first 4 contiguous ports in the map since only MA0 - MA2 and MCS0/ are decoded. The ports begin at XX0h and end at XX3h. The SBX-D/A12 is designed to work with regular or CMOS base boards.
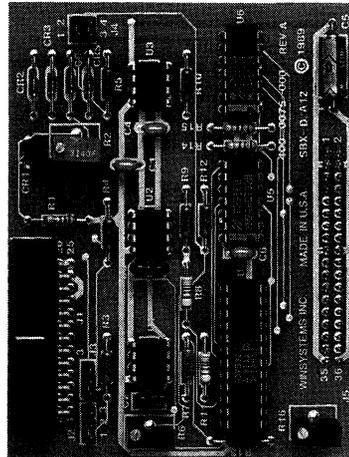
Each port address has a 8-bit byte which designates a specific function. Byte 0 is the DAC Low Byte, Byte 1 is the DAC High Byte, Byte 2 is the DAC 1 Low Byte, and Byte 3 is the DAC1 High Byte. DMA is not supported.
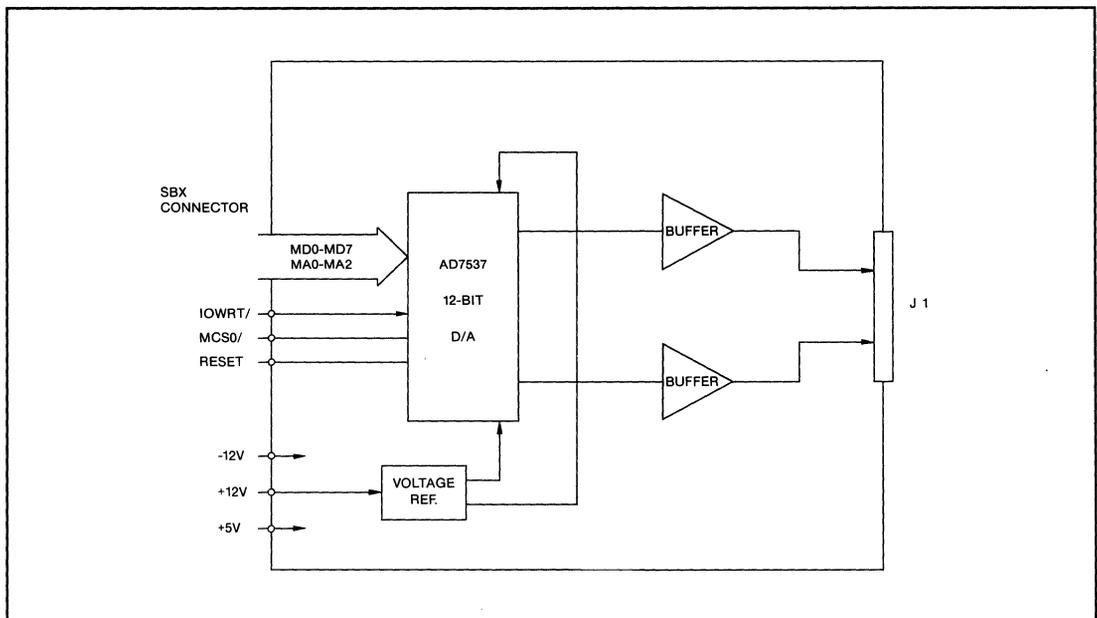
SBX-D/A12 I/O Address Map							
BYTE	D7	D6	D5	D4	D3	D2	D1	D0
0	B7	B6	B5	B4	B3	B2	B1	LSB
1	X	X	X	X	MSB	B10	B9	B8
2	B7	B6	B5	B4	B3	B2	B1	LSB
3	X	X	X	X	MSB	B10	B9	B8

Byte 0: DAC0 Low Byte - This byte is written to with the 8 lowest order bits for the first channel's 12-bit word.

Byte 1: DAC0 High Byte - This byte is written to with the 8 most significant bits for the first D/A channel's 12-bit word.

Byte 2: DAC1 Low Byte - This byte is written to with the 8 lowest order bits for the second D/A channel's 12-bit word.

Byte 3: DAC1 High Byte - This byte is written to with the 8 most significant bits for the second D/A channel's 12-bit D/A word. Writing to this byte commands both D/A converters to update their output with its new value.

Digital to Analog Converter - The SBX-D/A12 contains an Analog Devices AD7537 Dual 12-bit DAC. Two independent DACs are on one monolithic chip configured to provide two unipolar or bipolar outputs. The output range is 0 to +5 or $\pm$5 volts. The voltage range is jumper selectable.

The digital data input section is double buffered to allow simultaneous update of both DAC's. A two byte transfer is required to interface an 8-bit SBX board to the 12-bit D/A. These registers "memorize" the 12-bit digital word and keeps the D/A converter output constant until it is updated with a new value in one step.

Output Configuration - Each output channel is wired to J1, a 26-pin right angle male connector. The wiring is compatible with the LPM-D/A12 and MCM-D/A12's J1 STD Bus D/A output connector. Channel 0 is wired to pin 2 and channel 1 is wired to pin 8. All other pins are grounded. J1 is configured so that mass termination type flat ribbon cable or discreet wires can be connected to it. Alternating ground lines,

paired with each output channel's signal lines improves noise immunity and reduces cross talk.

WinSystems offers the CBL-120-3 which is a 3 foot, #28 AWG, ribbon cable designed to provide access to signals from the 26-pin, 0.100" grid connector on the SBX-D/A12 board. One end of the cable has a polarized, 26-pin female socket connector with strain relief that plugs into the board and the other end is open to allow users to make their own custom termination.

SPECIFICATIONS

Electrical
Number of Channels: 2
D/A Resolution: 12-bits
Coding: Straight binary (unipolar)
Offset binary (bipolar)
Output Voltage Range: 0 to +5V; $\pm$5V @5 mA
Nonlinearity: 1 LSB
Relative Accuracy: $\pm$1LSB
Output Settling Time: 5 uS
Power Requirements:
+5 VDC $\pm$5% at 5 mA (typ.)
+12VDC $\pm$10% at 10 mA (typ.)
-12VDC $\pm$10% at 5 mA (typ.)

Mechanical
Dimensions: 2.85" x 3.7"
PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors
Output: 26-pin dual on 0.100" grid
SBX: 18/36-pin dual 0.100" dual row male

Environmental
Operational Temperature: -25°C to +85°C

ORDERING INFORMATION

SBX-D/A12   2 Channel 12-bit D/A converter on SBX card
CBL-120-3   3 ft. ribbon cable

WinSystems, Inc.

WinSystems®

SBX BUS

SBX-OPTO
48 Channel Opto-22
Rack Interface Card

FEATURES

- 48 I/O lines configured as six, 8-bit parallel I/O ports
- Designed to interface directly to 2 standard industrial isolation I/O module racks (Opto-22 or equivalent)
- Dual 50-pin header connectors
- Single 8-bit iSBX module compatible
- Use two 82C55A PPIs
- No power glitching on I/O lines
- Single +5 volt operation
- Extended operational temperature range: -40° to +85° Centigrade

The SBX-OPTO is a compact, SBX multimodule, general purpose 48-line parallel I/O controller based upon two 82C55A Programmable Peripheral Interface (PPI) devices. These lines are organized as 2 groups of three 8-bit I/O ports that interface directly to 2 independent industry standard 4, 8, 16, and 24-I/O module mounting racks (Opto-22, Gordos, etc.).
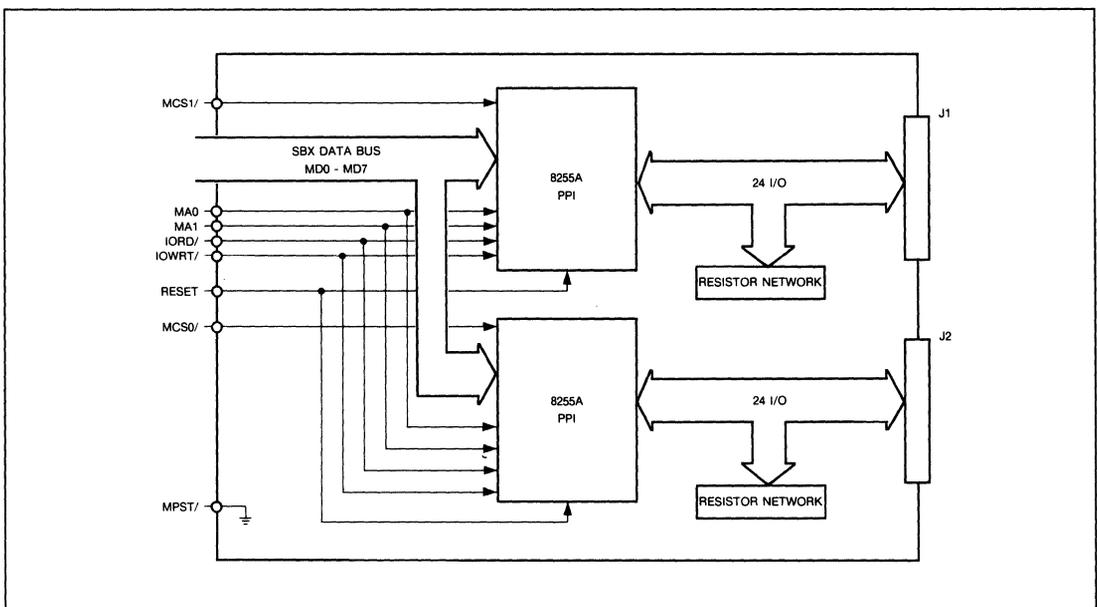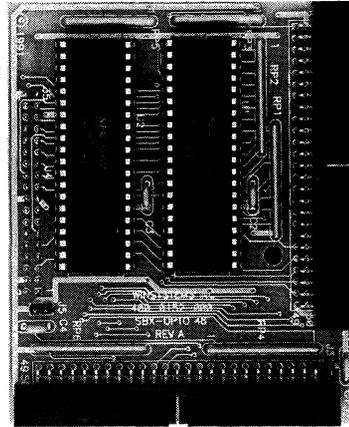
FUNCTIONAL CAPABILITY

SBX Interface - The SBX-OPTO is I/O port mapped with each channel having a unique port address determined by the base board. The board will work with either a regular NMOS/TTL or CMOS base board.

Parallel Controller - Two 82C55A Programmable Peripheral Interface (PPI) devices are on the SBX-OPTO board. Each chip is independent from the other and each supports 24 I/O pins which may be individually programmed in 2 groups of 12 in 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group for handshaking.

Although an 82C55A offers great flexibility as a general purpose parallel interface device, it would be programmed in Mode 0 for use with standard I/O mounting racks. This means that the digital signal conditioning modules must be grouped in sets of 4 as either input or output.

The signal levels are TTL compatible. Each I/O line has a 10K ohm pull-up resistor to keep the input from floating.

I/O Connector - Each 82C55A has its 24 I/O lines connected to a separate 50-pin male right angle connector. The 24 data lines are alternated with 24 ground lines for reduced noise and crosstalk. The pinout is compatible to an industry standard 4 to 24 position I/O module mounting rack (Opto-22, Crydom, Gordos, etc.) for use with high level AC and DC signal interfacing.

A 50 conductor ribbon cable such as the WinSystems' CBL-115-4 connects the SBX-OPTO to one I/O rack. Two cables are required to fully utilize this card, one for each rack. The cable will interface directly to a 4, 8, 16 or 24 module rack.

J1 and J2 - Rack I/O Connector

Pin	Description	Pin	Description
1	PA0	2	Gnd
3	PA1	4	Gnd
5	PA2	6	Gnd
7	PA3	8	Gnd
9	PA4	10	Gnd
11	PA5	12	Gnd
13	PA6	14	Gnd
15	PA7	16	Gnd
17	PB0	18	Gnd
19	PB1	20	Gnd
21	PB2	22	Gnd
23	PB3	24	Gnd
25	PB4	26	Gnd
27	PB5	28	Gnd
29	PB6	30	Gnd
31	PB7	32	Gnd
33	PC0	34	Gnd
35	PC1	36	Gnd
37	PC2	38	Gnd
39	PC3	40	Gnd
41	PC4	42	Gnd
43	PC5	44	Gnd
45	PC6	46	Gnd
47	PC7	48	Gnd
49	+5V	50	Gnd

SPECIFICATIONS

Electrical

SBX compatible for 8-bit operation
Parallel Interface: 48 I/O lines, TTL compatible
Power Requirements: +5V $\pm$ 5% at 40mA typ.

Mechanical

Dimensions: 2.85 x 3.70 inches

Connectors
SBX: 18/36-pin 0.100″ dual row male
Parallel: Two 50-pin dual 0.100″ headers
Jumpers: 0.025″ square posts

Environmental
Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

SBX-OPTO	48-line Opto rack interface
CBL-115-4	4 ft., 50 conductor ribbon cable

WinSystems, Inc.

FEATURES

- 48 I/O lines configured as six, 8-bit parallel I/O ports
- Programmable as in only, out only, or bidirectional
- Pull up resistors on all input lines
- iSBX module compatible
- Uses two 82C55A PPI's
- No power glitching on I/O lines
- Single +5 volt operation
- Optional CMOS version: LBX-PIO

The SBX-PIO is a compact, SBX multimodule, 48-line parallel I/O controller based upon two 8255A Programmable Peripheral Interface (PPI) devices. Each parallel channel is independent from the other and capable of generating interrupts. The board is capable of generating unidirectional or bidirectional input/output data.
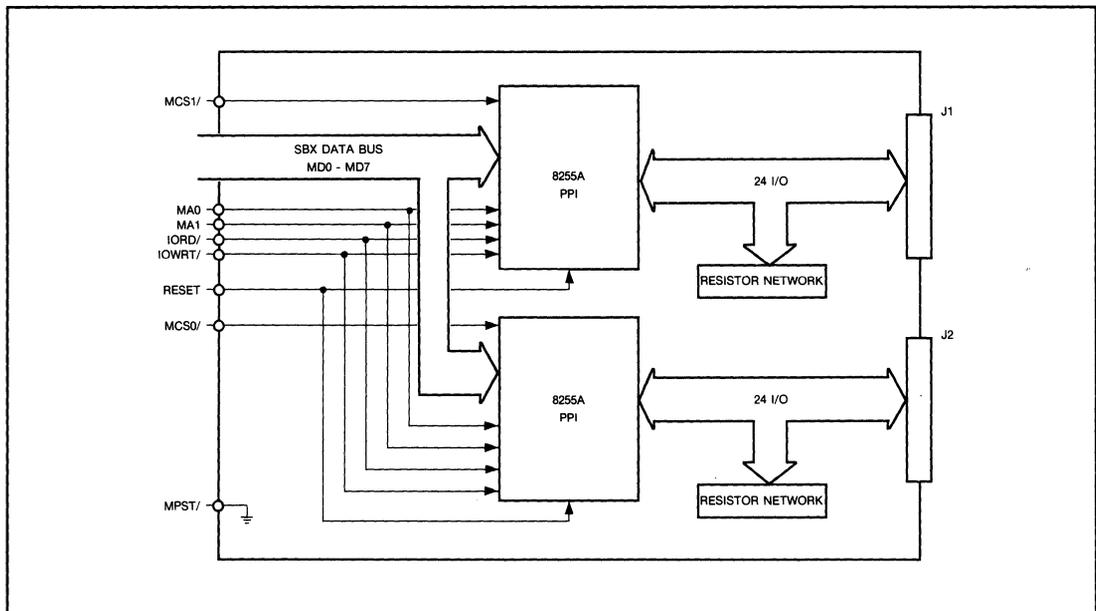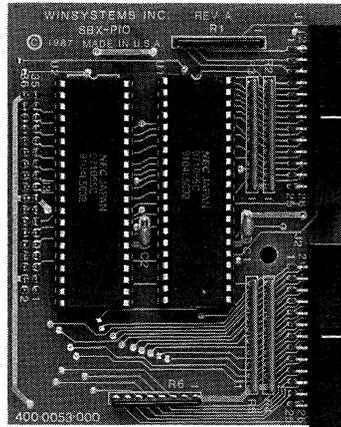
FUNCTIONAL CAPABILITY

SBX Interface - The SBX-PIO is I/O port mapped with each channel having a unique port address determined by the base board. Two blocks of 8 I/O ports are reserved for the SBX multimodule and selected by the MCS0 and MCS1 chip select lines.

Parallel Controller - Two 82C55A Programmable Peripheral Interface devices are on the SBX-PIO board. Each chip is independent from the other and supports 24 I/O pins which may be individually programmed in 2 groups of 12 in 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group for handshaking.

There is direct bit set/reset capability for control application interface requirements. Also one port can be configured for a Centronics type interface. The signal levels are TTL compatible. Each I/O line has a 10K ohm pull-up resistor to keep the input from floating. Each 82C55A has its 24 I/O lines connected to a separate 26-pin male right angle connector.

J1 and J2 - Parallel I/O Connector

Pin	Description	Pin	Signal
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	Ground	26	Ground

Multimodules - The SBX Multimodule boards are small, specialized, I/O mapped boards which plug into base boards. The SBX boards connect to the SBX bus connector and convert the SBX bus signals to a defined I/O interface. The SBX-PIO is designed to plug into a SBX 8-bit multimodule connector and can work with the NMOS/TTL or CMOS STD Bus cards. The multimodule is a unique design approach to STD Bus users offering a broad range of expansion boards joined together on the SBX interface. An application can be tailored directly onboard a single board computer at minimal cost. The SBX board dimensions are 3.7 x 2.85 inches. It is designed to fit on the WinSystems LPM/MCM-SBC8, LPM/MCM-SBC40, SBC-25, SBC-88 or LPM/MCM-SBC50 processors or the LPM/MCM-SBX multimodule expansion board.

SPECIFICATIONS

Electrical

SBX compatible for 8-bit operation

Parallel Interface: 48 I/O lines, TTL compatible

Power Requirements: +5V ± 10% at 20 mA typ.

Mechanical

Dimensions: Meets all SBX single wide mechanical specifications; 2.85 x 3.70 inches

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

Serial I/O: Two 26-pin 0.100" grid
iSBX: 18/36-pin 0.100" dual row male
Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

SBX-PIO   48 line parallel I/O SBX card

WinSystems, Inc.

P.O. Box 121361 / Arlington, Texas 76012 / (817) 274-7553

FEATURES

- Two independent, full-duplex RS-232-C serial communications channels
- iSBX module compatible
- Asynchronous and synchronous (BISYNC, SDLC, HDLC, and CCITT-X.25) protocols
- Programmable baud rates to 19.2K baud
- Generates prioritized interrupts
- Diagnostics can be run with loopback mode
- Configurable as DTE or DCE
- Modem handshake signals
- Uses the Z8530 SCC controller

The SBX-SCC is a powerful, compact, SBX multimodule, two channel programmable communications controller based upon the Z8530 SCC. Each serial channel is independent from the other and capable of baud rates of up to 19.2K baud. Each channel is configurable as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE) and can be used to interface to a terminal, printer, modem, or other peripheral system.
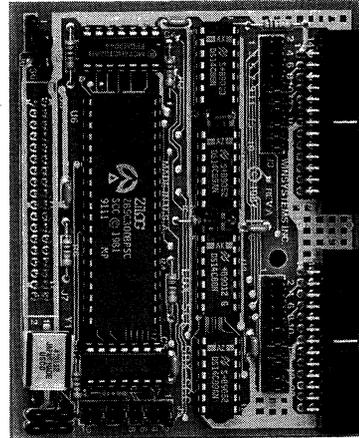
FUNCTIONAL CAPABILITY

SBX Interface - The SBX-SCC is I/O port mapped with each channel having a unique port address determined by the base board. Two blocks of 8 I/O ports are reserved for the SBX multimodule and selected by the MCS0 and MCS1 chip select lines. Interrupts are supported and brought out to the base board through the SBX connector on the MINTR0/-1 lines. The interrupt requests are compatible with the Intel 8259A type programmable interrupt controller.
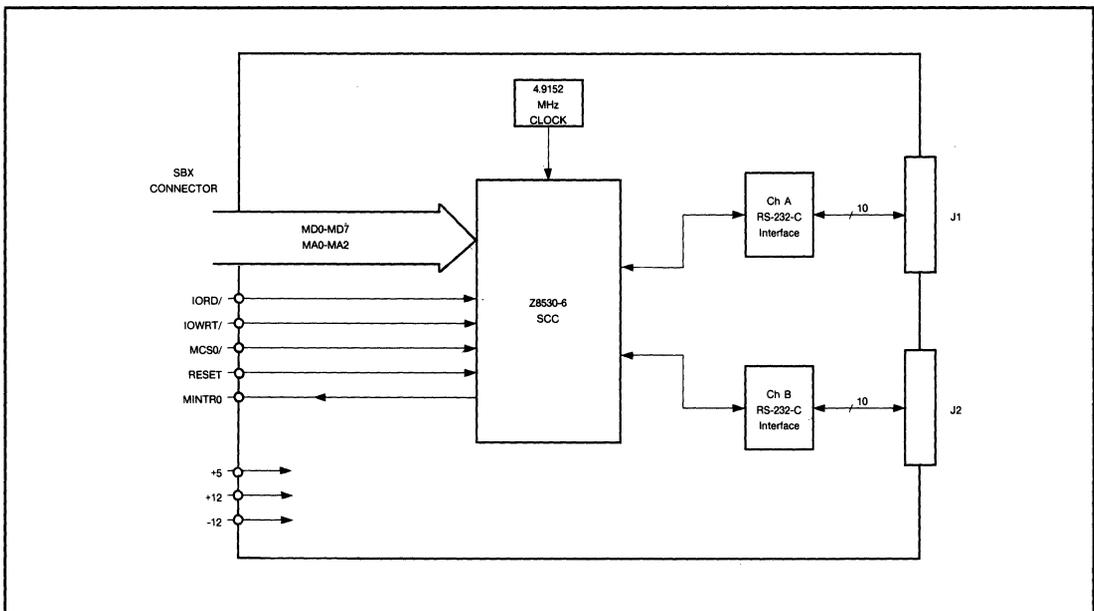
Serial Controller - A 85C30 SCC controller is on-board that provides a dual channel serial communications. It supports both asynchronous and synchronous protocols including BiSync, SDLC, etc. Each channel contains an independent baud rate generator that can be programmed to generate standard baud rates from 50 to 19.2K baud. The 85C30 also has an internal phase lock loop for use in NRZI systems.

In the asynchronous mode, the card will work with 5 to 8-bit characters. It will handle 1, 1½, or 2 stop bits; false start bit detection, and automatic break detection and handling. Each channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream. Error detection is provided for parity, overrun, and framing. In synchronous mode, the SCC will support BiSysnc, SDLC, and HDLC including CRC generation, sync character insertion/deletion and many other protocol-dependent features.

Serial Configuration - Each channel has 4 modem handshake lines and 2 clock lines in addition to the transmit and receive lines. These lines are RTS, CTS, DTR, DSR, and RCLK (DA and DD). Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation. The synchronous clock lines are configured to only receive the clock from the connector. All signals are RS-232 levels. The signals from each channel are brought out to separate 26-pin male right angle headers on the card edge which allows easy connections to a flat cable 25-pin "D" type adapter cable. WinSystems offers both male and female type "D" to 14-pin ribbon cables designated CBL-105-3 and CBL-106-3. The signal assignment on the 14-pin headers is as follows:

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Signal Ground
15	Receive Clock (DB)
17	Receive Clock (DD)
20	Data Terminal Ready (DTR)
24	Transmit Clock (DA)

Multimodules - The SBX Multimodule boards are small, specialized, I/O mapped boards which plug into base boards. The SBX boards connect to the SBX bus connector and convert the SBX bus signals to a defined I/O interface. The SBX-SCC is designed to plug into a SBX 8-bit multimodule connector and can work with the NMOS/TTL or CMOS STD Bus cards. The multimodule is a unique design approach to STD Bus users offering a broad range of expansion boards joined together on the SBX interface. An application can be tailored directly onboard a single board computer at minimal cost. The SBX board dimensions are 3.7 x 2.85 inches. It is designed to fit on the WinSystems LPM/MCM-SBC8, LPM/MCM-SBC40, SBC-25, SBC-88 or LPM/MCM-SBC50 processor or the LPM-SBX multimodule expansion board.

SPECIFICATIONS

Electrical

SBX compatible for 8-bit, DMA or non-DMA operation

Serial Interface: Synchronous/Asynchronous operation with modem control and receive clock inputs. Jumper configurable as either DCE or DTE.

Baud Rates: 50 to 19.2 Kbaud

Power Requirements: +5V ± 10% at 35 mA typ.
+12V ± 10% at 2 mA typ.
-12V ± 10% at 2 mA typ.

Mechanical

Dimensions: Meets all SBX single wide mechanical specifications; 2.85 x 3.70 inches

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

Serial I/O: Two 26-pin 0.100" grid
iSBX: 18/36-pin 0.100" dual row male
Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C
Non-condensing relative humidity: 5% to 95%

## ORDERING INFORMATION

SBX-SCC   Dual serial I/O SBX card

WinSystems, Inc.

FEATURES

- ANSI X3T9.0 Small Computer Systems Interface (SCSI)
- Asynchronous transfer rate up to 4 MBytes/sec
- Multiple host adapters can be attached
- DMA or polled I/O with interrupt on completion
- Uses an NCR 53C80 type controller
- On chip SCSI Bus drivers capable of sinking 48mA
- Onboard termination resistors
- Supports arbitration, selection/reselection, initiator or target roles
- Single +5 volt operation
- Operational temperature: 0°C to +60°C

The SBX-SCSI is a Small Computer Systems Interface (SCSI) host adapter card. It permits multiple peripherals such as disk drives, WORM and optical drives, printers, tape streamers, computers, network gateways, integrated systems, etc. to be linked to a host CPU board with an 8-bit SBX connector in a very low cost manner.
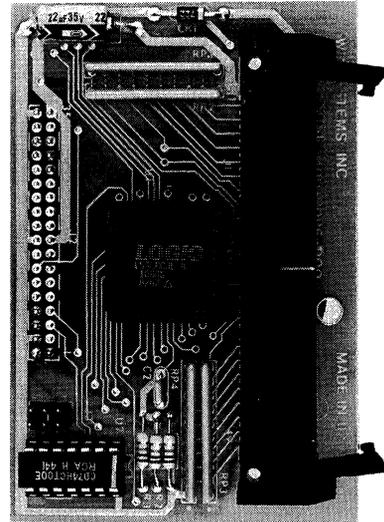
FUNCTIONAL CAPABILITY

SBX Interface - The SBX-SCSI is a single wide SBX board that supports 8-bit transfers. It is I/O port mapped and requires 8 contiguous address.
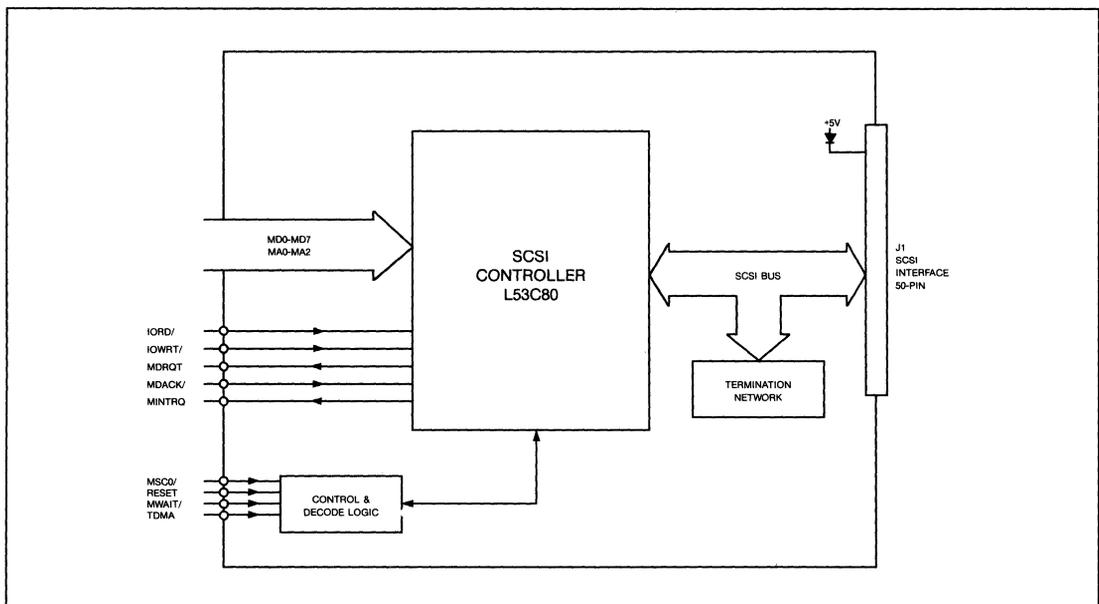
Interrupts and DMA - Both interrupts and DMA are supported on the card. A jumper block is available to select the /EOP signal (End of Process or DMA Terminal Count) on the SCSI controller to be normal or inverted to indicate that a DMA is concluded. Ready is also jumper selectable which provides a way to generate Wait States to control I/O transfer speed.

SCSI Interface - The SBX-SCSI is a complete interface to the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.0 committee. The SBX-SCSI offers the ability to interface different peripherals to the STD Bus through an industry standard architecture. Devices including printers, streaming tapes, disk drives, network gateways, and various other storage devices can be linked with this board. This allows several devices to communicate with either a single host or multiple hosts and devices. When several unlike devices need to be joined together, the SBX-SCSI allows signals from one device to be translated and utilized by the other. This interface determines an entire bus system with clear electrical paths and communication protocols are defined.

SCSI Controller - The SBX-SCSI is a very high performance, low cost, SCSI host adapter which supports the physical layer of the SCSI bus. It uses the Logical Devices' L53C80 controller which is pin and functionally compatible with the NMOS NCR 5380, yet it offers up to a 2.5 times performance improvement while lowering the power requirements by a factor of 10. It is designed to generate interrupts for a variety of error conditions. The L53C80 provides extensive bus status monitoring features, and includes buffers capable of directly driving a terminated SCSI bus for an efficient STD Bus implementation. The SBX-SCSI has the capability to operate in either DMA, or programmed I/O Mode. It can be either an initiator or target which provides 8-bit wide data transfer speeds up to 4 MBytes per second.

Connector - The SBX-SCSI supports the standard 50-pin cable wiring convention. Each signal line is single ended and is capable of sinking 48 mA and has a 220/330 ohm termination network. The board is shipped from the factory with the termination network installed.

J2, SCSI Connector Pin Assignment

Pin	Designation	Signal Name
2	DB0	Data Bus - bit 0
4	DB1	Data Bus - bit 1
6	DB2	Data Bus - bit 2
8	DB3	Data Bus - bit 3
10	DB4	Data Bus - bit 4
12	DB5	Data Bus - bit 5
14	DB6	Data Bus - bit 6
16	DB7	Data Bus - bit 7
18	DBP	Data Parity
20,22,24	GND	Digital Ground
26	TERMPWR	Terminator Power
28,30	GND	Digital Ground
32	ATN	Attention
34	GND	Digital Ground
36	BSY	Busy
38	ACK	Acknowledge
40	RST	Reset
42	MSG	Message
44	SEL	Select
46	C/D	Control/Data
48	REQ	Request
50	I/O	Input/Output
1........49	GND	All odd pins to digital ground, except pin 25 that is open

SPECIFICATIONS

Electrical

8-bit SBX Bus Compatible
Power: +5VDC ±5% @400 mA

Mechanical

Meets SBX Bus mechanical dimensions: 2.85 x 3.7 inches

Connectors

Jumpers: 0.025" square posts
SBX: 18/36-pin 0.100" dual row male
SCSI: 50-pin on 0.100 inch grid

Environmental

Operating Temperature: 0° to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

SBX-SCSI   SBX Bus SCSI host interface card

WinSystems, Inc.

FEATURES

- Permits addition of user designed circuitry for SBX and CMOS SBX Bus systems
- Access to all SBX Bus lines and power buses
- Wire-wrap, point to point or flow soldering
- Processor independent
- Large breadboard area on 0.100" grid accepts standard DIP sockets, connectors and press-fit pins
- Plated through holes
- Provisions for bypass capacitors

The SBX-WW1 is designed as a universal prototyping card for user application specific circuitry. It allows SBX Bus and CMOS SBX Bus users to construct experimental and custom I/O interfaces with a minimum of effort. A 0.100 inch grid is provided for the breadboard area that accepts standard DIP sockets, connectors, press-fit pins and discrete logic circuitry.
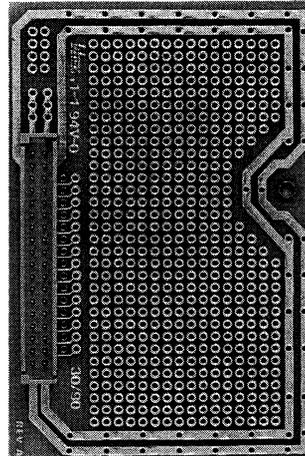
FUNCTIONAL CAPABILITY

Bus Interface - Full access is provided to the 8-bit, 36-pin SBX Bus connector including address bus, data bus, control, and power. Connection points are provided from the Bus to the prototyping circuit area.

Configuration - A 3.75 x 1.85 inch prototyping breadboard area is available for application specific prototype and experimental circuit design. It consists of a 0.100 inch grid of 0.042 inch plated through holes that will accept 0.025 inch square posts, discrete components, standard 8, 14, 16, 24, 28, and 40-pin solder or wirewrap DIP sockets and connectors. The card is available for installation of one or several 0.100" right angle connectors or headers at the edge.

Additionally the signal pads, power pads, and ground pads are labeled on the circuit side of the board for easy identification. Power and ground traces ring the board for easy access to +5 volts.

SPECIFICATIONS

Mechanical

Dimensions: Meets all SBX Bus mechanical specifications; 3.70 x 2.85 inches

PC Board: FR4 epoxy glass with plated through 0.100 inch holes

Connectors

SBX Bus: 18/36-pin male dual row on 0.100" centers

ORDERING INFORMATION

SBX-WW1   General purpose prototyping card

9

WinSystems, Inc.

STD Bus 8- & 16-bit Specification and Application Notes

10

SECTION 1
STD BUS Specifications

SCOPE

Application

The STD BUS defines an 8-bit microprocessor bus standard where the small card size in conjunction with LSI semiconductor technology creates a modular-by-function approach to control-oriented system design. The standard card size, connector and pinout lend itself to a bused motherboard that permits any card to work in any slot.

The bus interface connector as shown in figure 1-1 is dedicated to microprocessor control of the card functions. Peripheral and I/O device connections are made at the edge of the card defined as the user interface. This concept gives an orderly signal flow across the card from the bus interface to the user interface. Peripheral and I/O devices can be connected to the system using their own unique connector and cabling requirements and complete functions can be modularly added to the system.
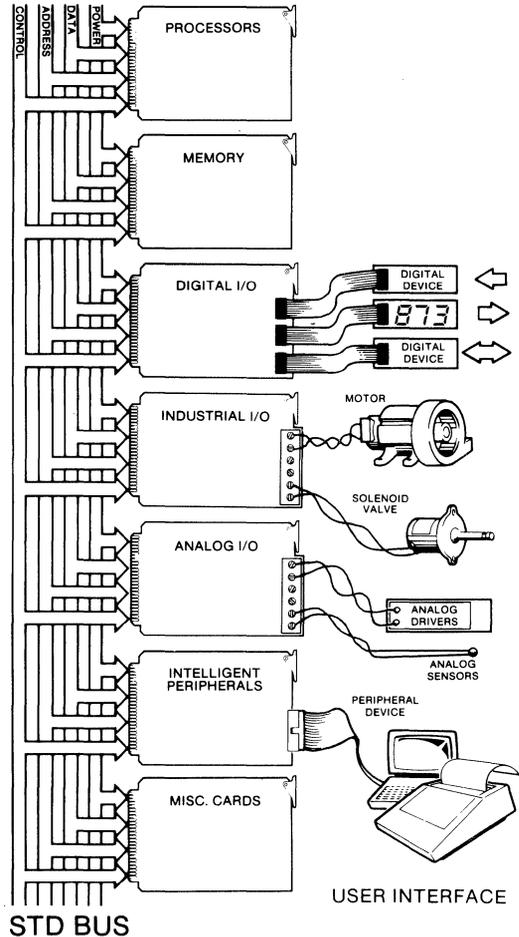
Figure 1-1. Bus Implementation

10

Inclusions

This document specifies:

- Card Dimensions
- Bus Connector
- Bus Pin Assignment
- Signal Definitions
- Electrical Requirements
- Read/Write Timing Sequences
- Read/Write Time Duration Parameters

Exclusions

This document does not specify:

- Card Functions
- User Interface
- Interchangeability

Definitions

- Shall: Shall signifies that which is mandatory
- Should: Should signifies that which is advisory

LOGICAL SPECIFICATIONS

Bus Pin Assignment. The BUS pinout is organized into five functional groups:

- Logic Power Bus: Pins 1-6
- Data Bus: Pins 7-14
- Address Bus: Pins 15-30
- Control Bus: Pins 31-52
- Auxiliary Power Bus: Pins 53-56

The organization and pinouts are shown in figure 1-2. Signal flow direction is referenced to the current master.

	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
		COMPONENT SIDE				**CIRCUIT SIDE**		
LOGIC POWER BUS	1	Vcc	In	Logic Power (+5 VDC)	2	Vcc	In	Logic Power (+5 VDC)
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBB #1/VBAT	In	Logic Bias #1/Bat Pwr	6	VBB #2/DCPD*	In	Logic Bias #2/Pwr Dwn
DATA BUS	7	D3/A19	In/Out	Data Bus/Address Ext	8	D7/A23	In/Out	Data Bus/Address Ext
	9	D2/A18	In/Out		10	D6/A22	In/Out	
	11	D1/A17	In/Out		12	D5/A21	In/Out	
	13	D0/A16	In/Out		14	D4/A20	In/Out	
ADDRESS BUS	15	A7	Out	Address Bus	16	A15	Out	Address Bus
	17	A6	Out		18	A14	Out	
	19	A5	Out		20	A13	Out	
	21	A4	Out		22	A12	Out	
	23	A3	Out		24	A11	Out	
	25	A2	Out		26	A10	Out	
	27	A1	Out		28	A9	Out	
	29	A0	Out		30	A8	Out	
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Pushbutton Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground	54	AUX GND	In	AUX Ground
	55	AUX +V	In	AUX Positive (+12 VDC)	56	AUX -V	In	AUX Negative (-12 VDC)

* Low-level active indicator

Figure 1-2. Bus Connector Pin Assignment

Signal Descriptions

Power Buses (Pins 1-6 and 53-56). The dual power buses accommodate logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns as shown in figure 1-3. Pins 5 and 6 provide for alternate use. If used for their alternate purpose these pins shall provide for disconnect capability on the card for conflict resolutions.

PIN	DESCRIPTION	COMMENT
1 & 2	Logic Power	Logic Power Source (+5 VDC)
3 & 4	Digital Ground	Logic Power Return Bus
5	Logic Bias Voltage	Low-current Logic Supply #1 (-5 VDC)
*5	Battery Backup Voltage	Alternate use as Battery Backup Voltage
6	Logic Bias Voltage	Low-current Logic Supply #2 (-5 VDC)
*6	DC Power Down	Alternate use as DC Power Down Signal
53 & 54	Auxiliary Ground	Auxiliary Power Return Bus
55	Auxiliary Positive	Positive DC Supply (+12 VDC)
56	Auxiliary Negative	Negative DC Supply (-12 VDC)

*PIN 5 VBAT—Battery Backup Voltage. VBAT is a DC voltage.
PIN 6—DCPD DC Power Down Signal. DCPD* is a logic signal that indicates Vcc has dropped below the recommended operating limit.

Figure 1-3. Power Bus Pin Assignments

Data Bus (Pins 7-14). (8-bit, bidirectional, 3-state, Active-High). Data Bus direction is controlled by the current master and is affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

All cards should release the data bus to a high-impedance state when not in use. The permanent master shall release the data bus in response to bus request (BUSRQ*) input from a temporary master, as in DMA transfers.

The Data Bus lines may be Multiplexed for address space expansion. The pin assignment for address expansion shall be as shown in figure 1-2.

Address Bus (Pins 15-30). (16-bit, 3-state, Active-High). The address originates at the current master. The permanent master shall release the address bus in response to a BUSRQ* input from a temporary master.

The address bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations. The particular microprocessor that is used determines the number of address lines and how they are applied.

The address bus may be extended by multiplexing on the data bus. The pin assignment for address expansion shall be as shown in figure 1-2.

PROCESSOR	NO. OF MEM ADDRESS LINES	ADDRESS LINES DURING REFRESH	No. of I/O Address Lines	
			I/O MAPPED I/O	MEMORY MAPPED I/O
8080	16	—	Lower 8	16
8085	16	—	Lower 8	16
Z80	16	Lower 7	Lower 8	16
6800	16	—	—	16
6809	16	—	—	16
6502	16	—	—	16
NSC800	16	Lower 8	Lower 8	16
8088	20	—	Lower 16	20

Figure 1-4. Examples of Address Bus Utilization

Control Bus (Pins 31-52). The control bus signal lines are grouped into five areas: memory and I/O control, peripheral timing, clock and reset, interrupt and bus control, and serial priority chain.

Memory and I/O Control lines provide the signals for fundamental memory and I/O operations. Simple applications may only require the following six control signals. All STD BUS cards shall support the memory and I/O control lines.

PIN 31 WR*—Write to memory or output (3-state, active-low). WR* originates from the current master and indicates that the BUS holds or will hold valid data to be written to the addressed memory or output device. WR* is the signal which writes data to memory or output ports.

PIN 32 RD*—Read from memory or input (3-state, active-low). RD* originates from the current master and indicates that it needs to read data from memory or from an input port. The selected input device or memory shall use this signal to gate data onto the BUS.

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PIN 33 IORQ*—I/O request (3-state, active-low). IORQ* originates from the current master and indicates an I/O read or write or a special operation. It is used on the I/O cards and is gated with either RD* or WR* to designate I/O operations. For some processors, IORQ* is gated with other processor signals to indicate a special operation, IORQ* with STATUS 1* (M1*) indicates interrupt acknowledge for the Z80.

PIN 34 MEMRQ*—Memory request (3-state, active-low). MEMRQ* originates from the current master and indicates memory read or memory write operations or a special operation. It is used on memory cards and is gated with either RD* or WR* to designate memory operations. For some processors, MEMRQ* is gated with other processor signals to indicate a special operation, MEMRQ* with STATUS 1* (DT/R*) and STATUS 0* (SS0*) indicates Passive for the 8088.

PIN 35 IOEXP—I/O expansion (high expand, low enable). IOEXP may originate from any source and should be used to expand or enable I/O port addressing. An active-low shall enable primary I/O operations. I/O slaves shall decode IOEXP.

PIN 36 MEMEX—Memory expansion (high expand, low enable). MEMEX may originate from any source and should be used to expand or enable memory addressing. An active-low shall enable the primary system memory. MEMEX may be used to allow memory overlay such as in bootstrap operations. A control card may switch out the primary system memory to make use of an alternate memory. Memory slaves shall decode MEMEX.

Peripheral Timing Control Lines provide control signals that enable the use of the STD BUS with microprocessors that service their own peripheral devices. The STD BUS is intended to service any 8-bit microprocessor. Most peripheral devices work only with the microprocessor they are designed for. Four control lines of the bus are designated for peripheral timing. They are defined specifically for each type of microprocessor, so that it can best serve its own peripheral devices. In this way, the bus is not limited to only one processor.

PIN 37 REFRESH*—(3-state, active-low). REFRESH* may originate from the current master or from a separate control card and should be used to refresh dynamic memory. The nature and timing of the signal may be a function of the memory device or of the processor. In systems without refresh, this signal can be any specialized memory control signal. Systems with static memory may disregard REFRESH.*

PIN 38 MCSYNC*—Machine cycle sync (3-state, active-low). MCSYNC* shall originate from the current master. This signal should occur once during each machine cycle of the processor. MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal are processor-dependent. MCSYNC* keeps specialized peripheral devices synchronized with the processor's operation. It can also be used for controlling a bus analyzer, which can analyze bus operations cycle-by-cycle.

MCSYNC* should be used to de-multiplex extended addressing on the data bus.

PIN 39 STATUS 1*—Status control line 1 (3-state, active-low). STATUS 1* shall originate from the current master to provide secondary timing for peripheral devices. When available, STATUS 1* should be used as a signal for identifying instruction fetch.

PIN 40 STATUS 0*—Status control line 0 (3-state, active-low). STATUS 0* shall originate from the current master to provide additional timing for peripheral devices.

PROCESSOR	REFRESH* Pin 37	MCSYNC* Pin 38	STATUS 1* Pin 39	STATUS 0* Pin 40
8080	—	SYNC*	M1*	—
8085	—	ALE*	S1*	S0*
NSC800	REFRESH*	ALE*	S1*	S0*
8088	—	ALE*	DT/R*	SS0*
Z80	REFRESH*	(RD+WR+ INTAK)*	M1*	—
6800	—	Φ1*	VMA*	R/W*
6809	—	EOUT* (Φ2*)	—	R/W*
6809E	—	EOUT* (Φ2*)	LIC*	R/W*
6502	—	Φ2*	SYNC*	R/W*

*Low-level active
— Not used
R/W* Read high, write low
DT/R* Data transmit high, receive low

Figure 1-5. Peripheral Timing-Control Lines
for Various 8-Bit Microprocessors

Interrupt and bus control lines allow the implementation of such bus control schemes as direct memory access, multiprocessing, single stepping, slow memory, power-fail-restart, and a variety of interrupt methods. Priority for multiple interrupts or bus requests can be supported by either serial or parallel priority schemes.

PIN 41 BUSAK*—Bus acknowledge (active-low). BUSAK* originates from the permanent master and is used to indicate that the bus is available for use by a temporary master. The permanent master shall respond to a BUSRQ* by releasing the bus and giving an acknowledge signal on the BUSAK* line. BUSAK* should occur at the completion of the current machine cycle. The signal should be combined with a priority signal if multiple controllers need bus access.

PIN 42 BUSRQ*—Bus request (active-low, open collector/drain). BUSRQ* originates from a temporary master and causes the permanent master to suspend operations on the bus by releasing all 3-state bus lines. The bus should be released when the current machine cycle has been completed. BUSRQ* shall be used in applications requiring direct memory access (DMA). This signal can be an input, or an output, or it can be bidirectional, depending on the supporting hardware.

PIN 43 INTAK*—Interrupt acknowledge (active-low). INTAK* originates from the permanent master to indicate to the interrupting device that it is ready to respond to the interrupt. For vectored interrupts, the interrupting device shall place the vector address on the data bus during INTAK.* This signal can be combined with a priority signal, if multiple controllers need access to the permanent master. INTAK* is used in vectored interrupt schemes.

PIN 44 INTRQ*—Interrupt request (active-low, open-collector/drain. INTRQ* originates from any slave function to interrupt the processor on the permanent master. It should be masked and ignored by the processor, unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it should acknowledge by asserting INTAK* (pin 43). Other actions depend on the specific type of processor, the interrupt-related program instructions, and the hardware support of the interrupt mechanism.

PIN 45 WAITRQ*—Wait request (active-low, open-collector/drain). WAITRQ* may originate from any master or slave and shall cause the current master to suspend operations as long as it remains low. The current master should hold in a state that maintains a valid address on the address bus. WAITRQ* can be used to insert wait states in the processor cycle. Examples of its use include slow-memory operations and single stepping.

PIN 46 NMIRQ*—Nonmaskable interrupt (active-low, open-collector/drain). NMIRQ* may originate from any master or slave and shall be used as an interrupt input of the highest priority to the permanent master. It should be used for critical processor signaling, e.g., power-fail indications.

Clock and reset lines provide the bus with basic clock timing and reset capability.

PIN 47 SYSRESET*—System reset (active-low, open-collector/drain). SYSRESET* originates from any system reset circuit, which may be triggered by power-on detection, or by the pushbutton reset. All cards with circuits requiring initialization should decode SYSRESET.*

PIN 48 PBRESET* — Pushbutton reset (active-low, open-collector/drain). PBRESET* may originate from any card as an input to the system reset circuit.

PIN 49 CLOCK*—Clock from processor. CLOCK* originates from the permanent master and is a buffered, processor clock signal, for use in system synchronization or as a general clock source.

PIN 50 CNTRL*—Control. CNTRL* may originate from any card as an auxiliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real-time clock signal, or an external input to the processor.

Priority chain lines are provided for serial interrupt or bus control. Two bus pins are allocated to the chain, which requires logic on the card to implement the serial priority function. Cards not needing the chain shall jumper PCI to PCO on the card.

PIN 51 PCO-Priority chain out (active-high). PCO originates from every card as a signal sent to the PCI input of the next lower card in priority. A card that needs priority shall hold PCO low.

PIN 52 PCI—Priority chain in (active-high). PCI originates directly from the PCO of the next higher card in priority. A high level on PCI gives priority to the card sensing the PCI input.

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Timing Specifications

Signal Time Sequence. The bus signal sequences are given for memory and I/O, read and write operations. The signal sequences are defined at the bus to guarantee card compatibility.

Address Selection Signal Sequences. The expansion signals, the address bus signals, and the request signals are used to select the data location for memory and I/O, read and write operations. These signals are referred to as the address selection signals.

- The expansion signal (MEMEX, IOEXP) is intended for selection of alternate memory or I/O address space.

- The address bus signals (A0-A23) are used to uniquely identify a data location within the memory or I/O space.

- The request signals (MEMRQ*, IORQ*) provide the selection between memory and I/O operations.

- The address selection signals may occur in any sequence. The last signal to become active and the first signal to become inactive determine the signal timing.

- The address selection signals shall all be stable prior to memory and I/O read and write operations.
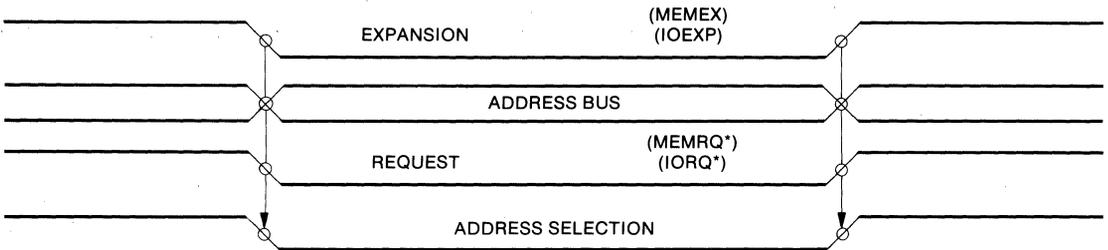
Figure 1-6. Address Selection Signal Sequence

Read Signal Sequences. The read sequence shown in figure 1-7 is controlled from the current master except for the data bus signals which are a response from the memory or I/O card.

The read signal causes a read operation to occur at the selected memory or I/O location. The read signal should change state within the address selection signal but may change at the same time. The trailing edge of the read signal shall indicate that the data has been transferred. The read signal shall hold the data bus active until the master accepts the data.

The data bus signals contain the data byte to be transferred to the master. These signals shall remain stable until the read signal is removed.
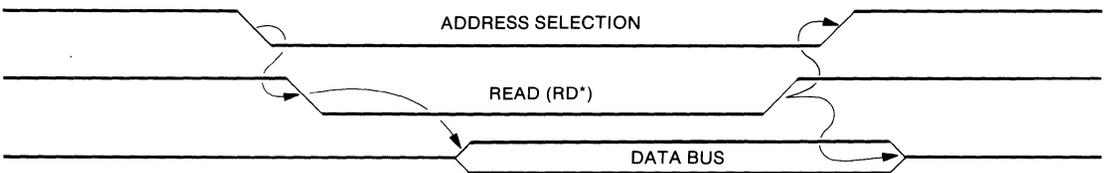
Figure 1-7. Read Signal Sequences

Write Signal Sequences. The write sequence shown in figure 1-8 is controlled from the current master. The address selection, data and write signals all originate from the current master.

The data bus signals contain the data byte to be transferred to memory or I/O. The data may occur before or after the leading edge of the write signal. The write signal shall change state within the address selection signal.
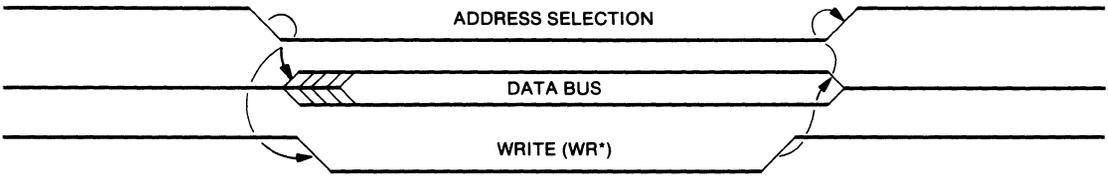
Figure 1-8. Preferred Write Signal Sequence

Signal Time Durations. Signal time durations are defined which will enable users to determine card compatibility for memory or I/O, read and write operations.

Read Timing. Critical read timing is shared between the current master and the memory or I/O card. The current master controls the read data access time (tARD) and has a requirement of a read data set-up time (tSRD). The memory or I/O device has a read access time (tAR) requirement. These timing relationships are shown in figure 1-9.
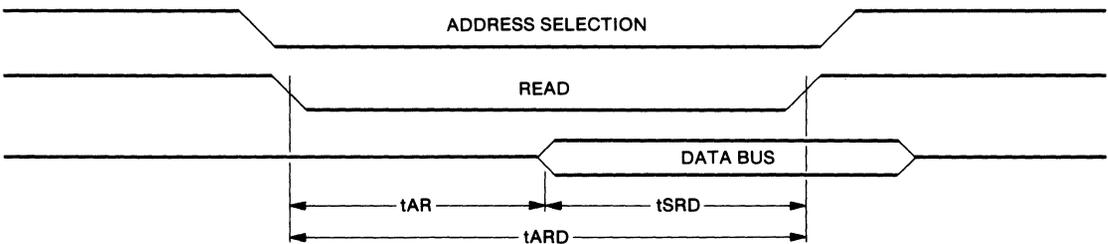
Figure 1-9. Critical Read Timing

Card compatibility for read operations shall be determined by comparing the specified required read access time of a memory or I/O card against the available read access time of a master card. Master card tAR shall be greater than or equal to Memory or I/O card tAR.

Master cards shall specify:

- tAR, maximum available Read Access time where tAR equals tARD minimum less tSRD minimum.

Memory or I/O cards shall specify:

- tAR, maximum required Read Access time. Since address selection may occur at the same time as Read, tAR must specify the worst case access time.

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Write Timing. Critical write timing for compatibility is limited to the write data set-up time (tSWD) and write data hold time (tHWD) required by the memory or I/O card as shown in figure 1-10.

Card compatibility for write operations shall be determined by comparing the specified required write data set-up and hold times of a memory or I/O card against the available write data set-up and hold times of a master card.

- Master tSWD shall be greater than or equal to Memory or I/O tSWD.
- Master tHWD shall be greater than or equal to Memory or I/O tHWD.

Master cards shall specify:

- tSWD, minimum available write data set-up time.
- tHWD, minimum available write data hold time.

Memory or I/O cards shall specify:

- tSWD, minimum required write data set-up time.
- tHWD, minimum required write data hold time.
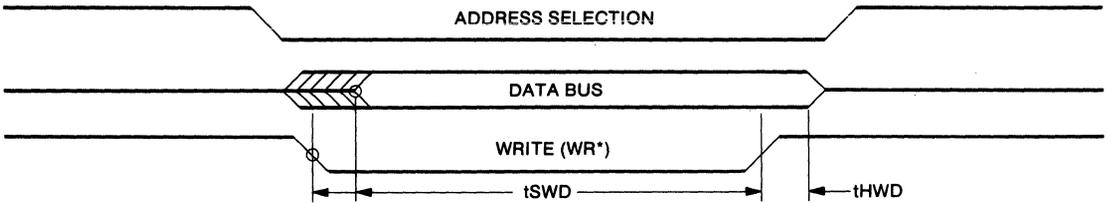
Figure 1-10. Critical Write Timing

Electrical Specifications

Maximum Ratings. The maximum ratings given in figure 1-11 for the bus card edge connector pins shall not be exceeded. These ratings are not recommended operating conditions as damage to card components is possible above these values.

PARAMETER	LIMIT	REFERENCE
Positive voltage applied to logic input or disabled 3-state output	+Vcc + 0.5 V	GND pins 3,4
Negative DC voltage applied to a TTL logic input or disabled 3-state output	-0.4V	
Negative DC voltage applied to a CMOS logic input or disabled 3-state output	-0.5V	

Figure 1-11. Maximum Voltage Ratings

Power Bus Voltage Tolerances. STD BUS cards require +5V for logic operations. Other operating voltages may be needed, according to individual card function and device types. The power signals measured at the card pins, not at the backplane traces, shall meet the voltage requirements given in figure 1-12.

CARD PIN	SIGNAL NAME	SUPPLY VOLTAGE	TOLERANCE	REFERENCE
1,2	TTL Vcc	+5V	±0.25V	GND pins 3,4
1,2	CMOS Vcc	+5V	±0.50V	GND pins 3,4
5	VBB #1	-5V	±0.25V	GND pins 3,4
5	VBAT	*	—	GND pins 3,4
6	VBB #2	-5V	±0.25V	GND pins 3,4
55	AUX +V	+12V	±0.5V	AUX GND pins 53,54
55	AUX -V	-12V	±0.5V	AUX GND pins 53,54

*VBAT may range from +3.5V to Vcc

Figure 1-12. Power Bus Voltage Ratings

Logic Signal Characteristics. The STD BUS is designed for compatibility with industry-standard TTL or high-speed CMOS logic levels. All logic signals shall meet the voltage requirements given in figure 1-13.

TTL BUS CARD PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V$_{OH}$ (high-state output voltage)	Vcc = MIN I$_{OH}$=-3 mA	2.4	—	V
V$_{OL}$ (low-state output voltage)	Vcc = MIN I$_{OL}$=24 mA	—	0.5	V
V$_{IH}$ (high-state input voltage)		2.0	—	V
V$_{IL}$ (low-state input voltage)		—	0.8	V
CMOS BUS CARD PARAMETER	TEST CONDITIONS (−40° to 85°C)	MIN.	MAX.	UNITS
V$_{OH}$ (high-state output voltage)	Vcc = MIN I$_{OH}$=-6 mA	3.76	—	V
V$_{OL}$ (low-state output voltage)	Vcc = MIN or MAX I$_{OL}$=6 mA	—	0.37	V
V$_{IH}$ (high-state input voltage)	Vcc = MIN[1]	3.15	—	V
	Vcc = MAX	3.85	—	V
V$_{IL}$ (low-state input voltage)	Vcc = MIN	—	0.9	V

[1]The worst case V$_{IH}$ occurs at Vcc = MAX.

Figure 1-13. Logic Signal Voltage Ratings

Bus Drive and Load Characteristics. Each card should present only one load per bus signal. Bus drivers should meet the IOL current sink requirements indicated in figure 1-13.

Mechanical Specifications

Card Dimensions. The circuit card shall meet the dimensions given in figures 1-14, 1-17, 1-18, 1-19 and 1-20. The dimensions exclude the card ejector and I/O interface connections.

Cards not meeting the minimum spacing of figure 1-14 shall specify actual spacing requirements.

CARD DIMENSIONS	INCHES		MILLIMETERS	
	NOMINAL	TOLERANCE	NOMINAL	TOLERANCE
Card Length	6.500	±0.025	165.10	±0.64
Card Height	4.500	+0.005,−0.025	114.30	+0.13,−0.64
Plated Board Thickness	0.062	+0.007,−0.003	1.58	+0.18,−0.08
Card Spacing	0.500	MIN	12.70	MIN

Figure 1-14. Card Dimensions

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Card Profile Dimensions. Minimum card spacing requires a consideration for component height, lead protrusion, and card clearance, in addition to board thickness. Cards designed for minimum spacing shall meet the requirements of figure 1-15.

RECOMMENDED DIMENSIONS FOR MINIMUM CARD SPACING	INCHES		MILLIMETERS	
	MAXIMUM	MINIMUM	MAXIMUM	MINIMUM
Component Height	0.375	—	9.52	—
Component Lead Protrusion	0.040	—	1.02	—
Adjacent Card Clearance	—	0.010	—	0.25

Figure 1-15. Card Profile Dimensions for Minimum Spacing

Bus Connector. Bus connections shall be made via a printed circuit board card edge connector. The mating connector shall be a 56-pin (dual 28) card edge connector on 0.125 inch (3.18 mm) centers.

Card Ejector. Each card should use a single card ejector mounted on the top right corner as shown in figures 1-17 and 1-19.

Card Keying. Cards should be polarity keyed to prevent upside-down card insertion. Cards keyed for polarity shall have a single, offset keyslot located between pins 25 (26) and 27 (28) as shown in figure 1-16.

Cards keyed for position shall not use the slot between pins 27 (28) and 29(30), as this would invalidate the polarity keying.

0.050 ±0.005
(1.27 ±13 mm)

KEY SLOT

0.390
(9.9 mm)

25 (26)   EVEN
27 (28) } PINS ON
29 (30)   OPPOSITE SIDE

COMPONENT SIDE
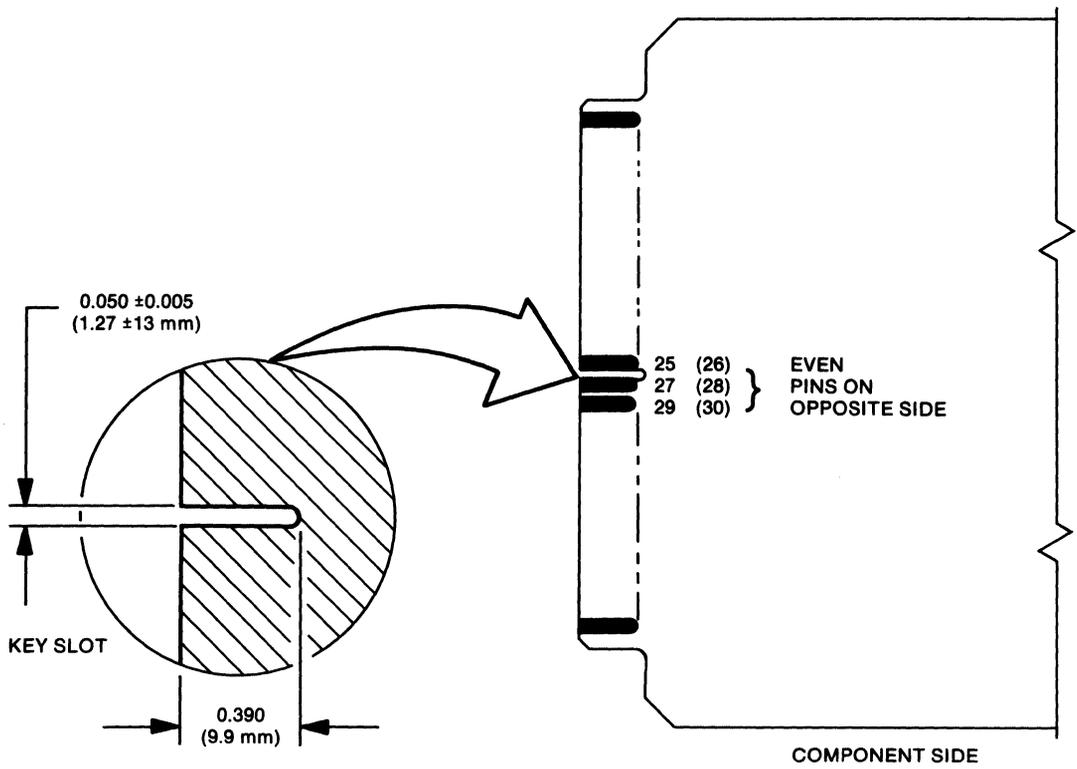
Figure 1-16. Key Slot Placement and Dimensions for Card Polarity Keying
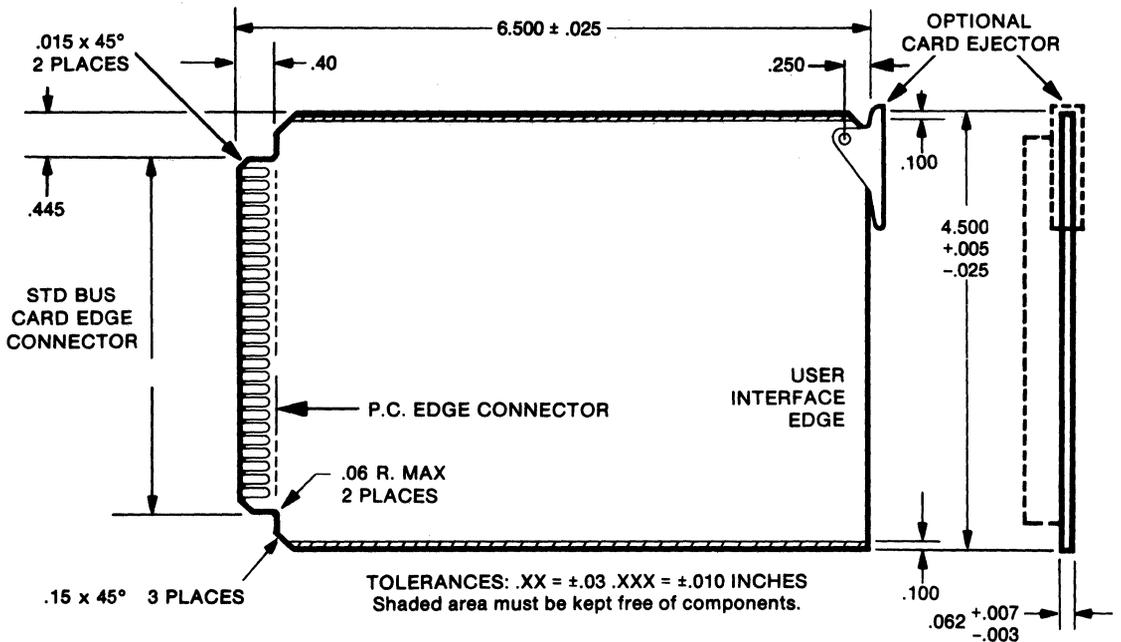
Figure 1-17. Bus Card Outline—Inches
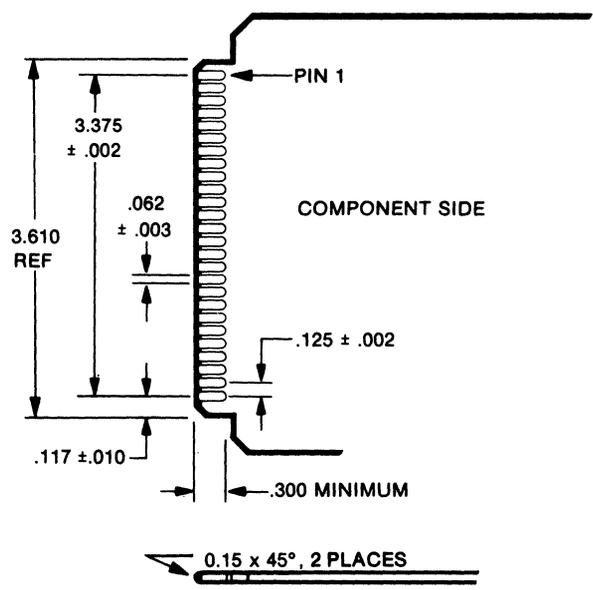
Figure 1-18. Bus Edge Card Finger Design—Inches
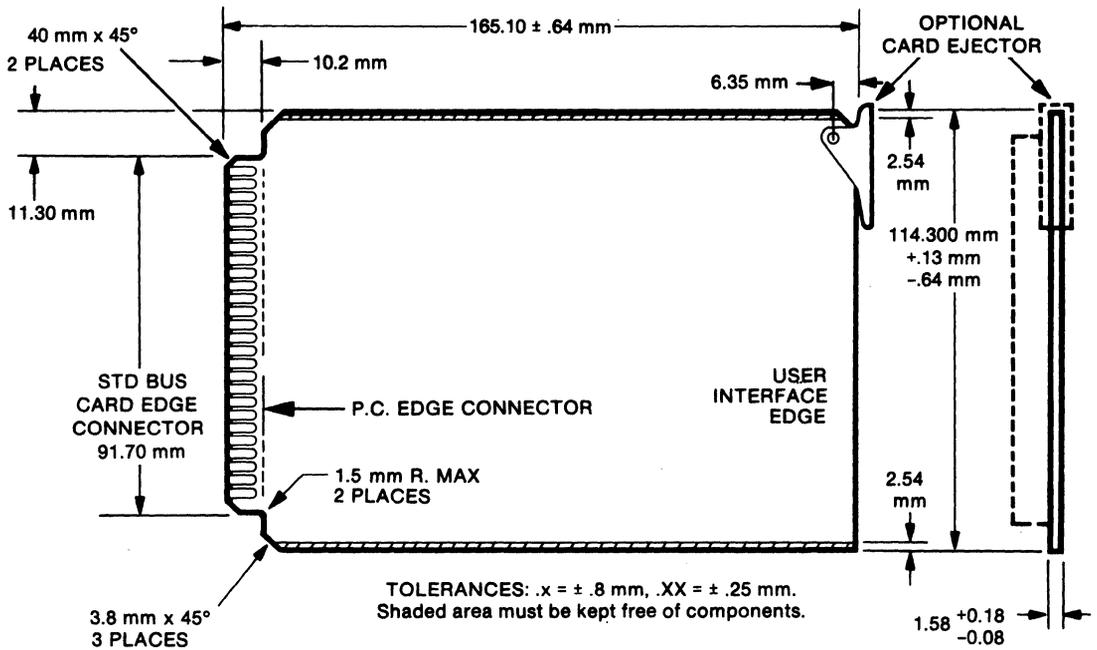
Figure 1-19. Bus Card Outline—Metric
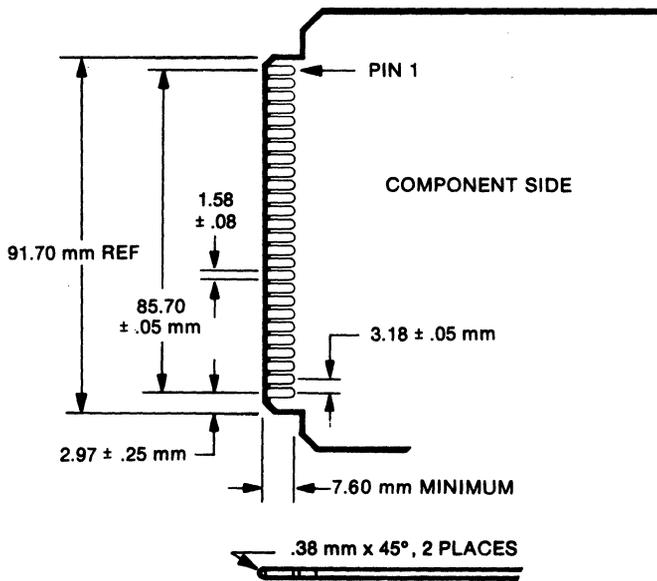
Figure 1-20. Bus Edge Card Finger Design—Metric

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SECTION 2
STD BUS Practice

The industry-based STD Manufacturers Group has resolved the following recommended practices for the design of STD BUS cards. The STD Practice is supplemental to the STD specification and is to be applied at the discretion of the user. The current STD Practice relates to:

- Compatiblity Designation Practice
- Bus Timing Practice
- Interrupt Priority Practice
- Bus Priority Practice
- Memory Expansion Practice
- Backplane Practice
- Open-Collector/Drain Bus-Signal Practice
- CMOS Load Capacitance Practice
- CMOS User Edge Input Practice
- CMOS Pull-Up Resistor Practice

Compatibility Designation Practice

STD BUS cards that use peripheral chips usually depend on specific timing signals from the processor. This dependency prevents peripheral cards from being used interchangeably with cards from other families.

The STD Practice for designating compatibility is to label cards that are processor-timing-dependent, with reference to the CPU device: STD-Z80/CMOS Z80, STD-8085/80C85A, STD-6800, etc.

Bus Timing Practice

Card designers require bus timing definitions to insure compatibility. The recommended STD Practice for cards that source the bus control signals is for each card to specify the waveforms and timing information. Bus timing is further defined in the family timing specifications.

- STD-65/68XX
- STD-8085/80C85A
- STD-Z80/CMOS Z80
- STD-8088/80C88
- STD-NSC800

Interrupt Priority Practice

The STD BUS provides signal lines for interrupt requests. In systems with only a single interrupting device, these lines are sufficient to allow direct implementation. In systems with multiple interrupting devices, a priority scheme is necessary. This practice explains a serial priority scheme and defines a request signal for the user interface which allows implementation of a parallel priority scheme for interrupts.

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Serial Priority for Interrupts. The STD BUS includes a priority-chain bus signal for serial priority schemes. Serial priority, using PCI and PCO signals, requires that each peripheral needing priority must have logic on the card to service the request, as shown in figure 2-1. This scheme is practical with peripheral devices designed to service a serial priority chain such as the Z80 family of devices.
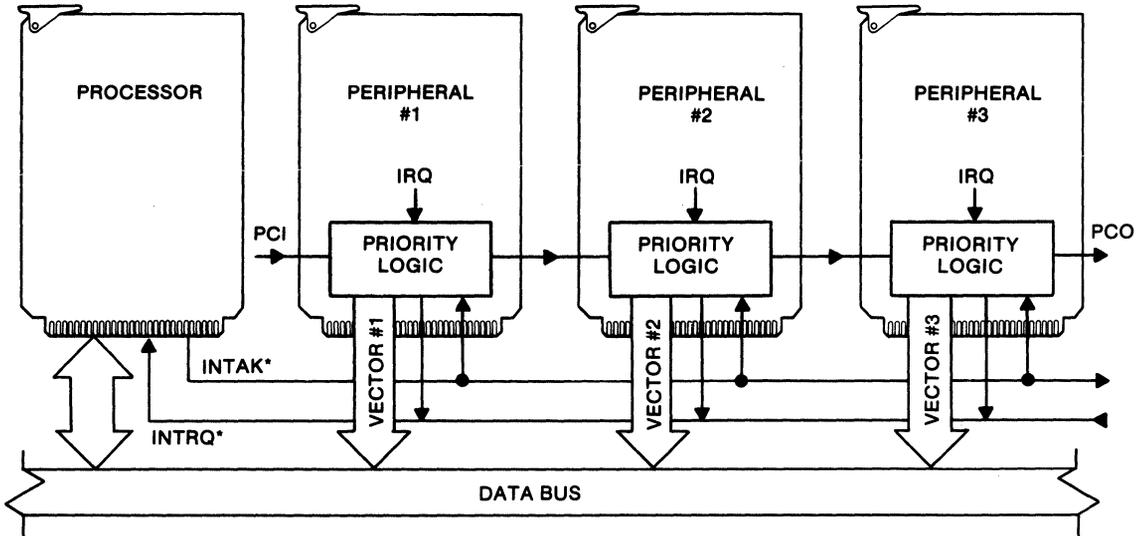
Figure 2-1. Serial Scheme for Interrupt Priority

Parallel Priority for Interrupts. A parallel priority scheme for interrupts can be implemented on the STD BUS, so that the priority logic rides on a separate card and not on each peripheral card. The parallel priority card is a modular function that can be tailored to individual processor requirements. This scheme allows peripheral cards to be processor-independent. It requires that the individual requests be made from the user edge of the card, as shown in figure 2-2. The parallel priority encoder could be included on the processor card.
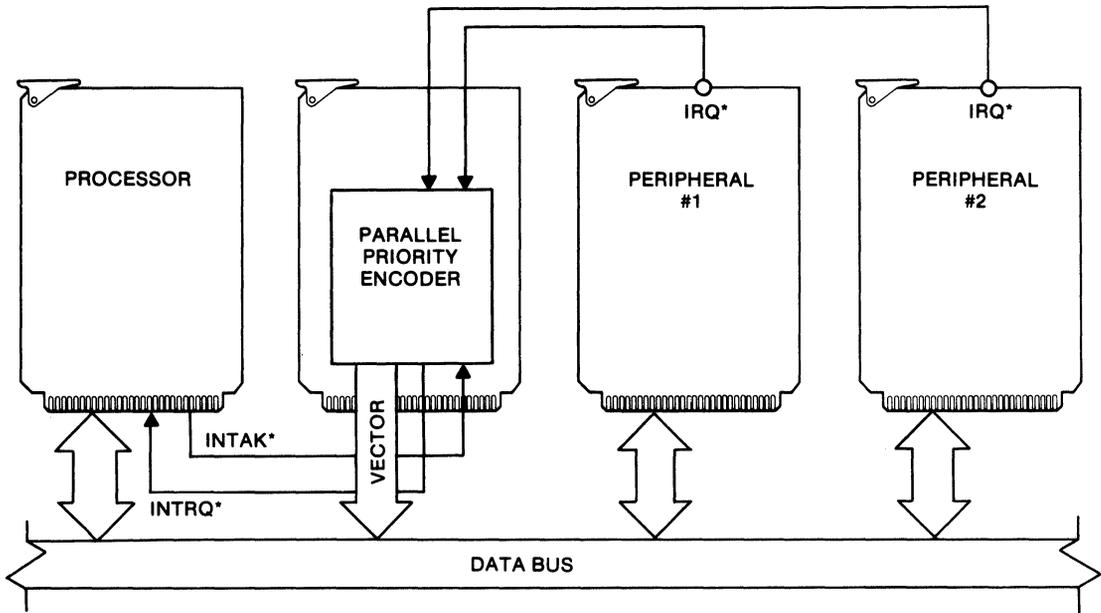
Figure 2-2. Parallel Scheme for Interrupt Priority

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User Interface Signal for Parallel Priority. This practice defines a signal for the user interface which allows implementation of the parallel priority scheme as shown in figure 2-2.

IRQ* — Internal Interrupt Request. This signal indicates that the card is requesting an interrupt. IRQ* is passed separately by each card to a priority resolver card via the user interface. The priority resolver shall control INTRQ* and respond to INTAK*.

Interrupt — Parallel Priority Interface Practice. Cards designed to work with the parallel priority scheme require circuit connections at the user interface edge of the card. The STD Practice for compatibility is:

Mechanical:

- Two connections for each request channel: a request signal and a ground signal.

- Connector layout for priority encoder cards is as shown in figure 2-3. The ground pins are the top row and the request pins are the bottom row.

- Connector pins are 0.025-in. square posts or equivalent.

- Requesting cards provide the cable and mating connector. This practice does not define the method for fastening the cable to the requesting card. The cable end at the requesting card may be permanently wired or connected via any desired connector means.

- Mating cables can be twisted pairs or flat cable.

- Mating connectors are two pins per channel, in any size from single channel (2-pin) to multiple channel.

Electrical:

- Low-level active signal.

- LSTTL or high speed CMOS logic levels.

- Drive sink capability of 16 mA at 0.4V minimum for TTL or 6 mA at 0.37V minimum for CMOS.

- Open-collector/drain driver with 10K pull-up minimum.

- Load on encoder input: 4 LSTTL or CMOS loads in parallel with 4.7K (TTL) or 10K (CMOS) pull-up resistor.

Pull-up resistors on the encoder card inputs are recommended to disable the request if no connection is made. Open-collector/drain drivers on requesting cards are recommended, to allow wire-ORing of multiple requests on a single channel. This scheme is useful to low-level requests and requires the processor to poll to identify the requester.
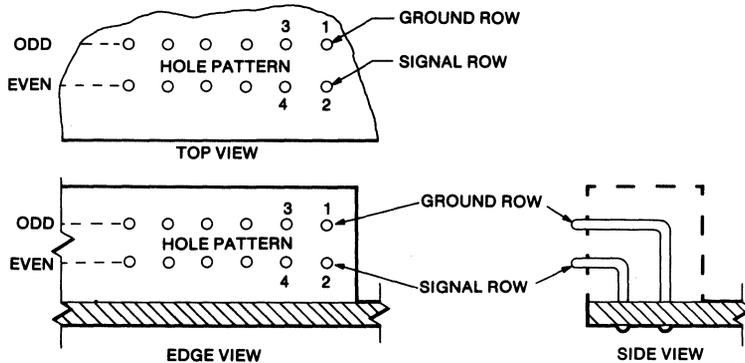
Figure 2-3. Recommended Connector Arrangement for Priority Encoder Cards

Bus-Priority Practice

The STD BUS provides signal lines for servicing bus requests. In systems with only a single alternate controller, these lines are sufficient to allow direct implementation. In systems with multiple bus controllers, a priority scheme is necessary. This practice defines three signals for the user interface which allow implementation of either a serial or parallel scheme for bus priority.

Serial Priority Bus Control. The STD BUS includes a priority-chain for serial priority schemes, however, this chain is generally used for interrupt priority. This practice defines a separate alternate chain for BUS-priority via the user interface as shown in figure 2-4. Serial priority requires that each peripheral needing priority must have logic on the card. This scheme is practical with devices designed to service a serial priority chain such as the Z80 family of devices.
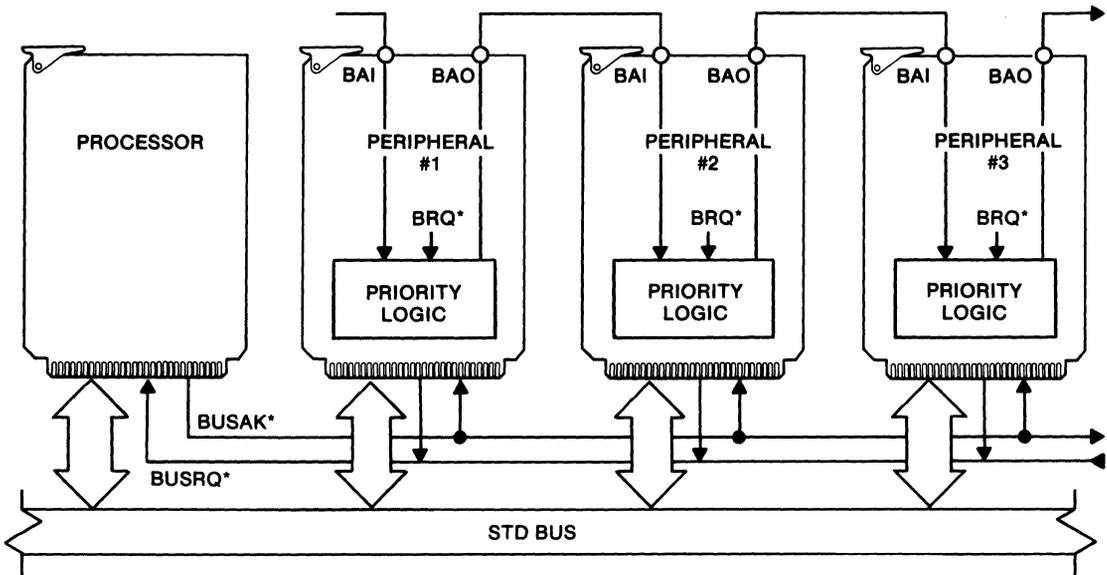
Figure 2-4. Serial Scheme for Bus Priority

User Interface Signals for Serial Priority Bus Control. This practice defines three signals for the user interface which allow implementation of the serial priority scheme shown in figure 2-4. The three signals are:

● BRQ* - Internal Bus Request

● BAI - Bus Acknowledge In

● BAO - Bus Acknowledge Out

BRQ* — Internal Bus Request (active low). This signal indicates that the card is requesting bus control. BRQ* drives BUSRQ* on the bus. BRQ* shall not originate if BUSAK* is low. When BRQ* and BUSAK* are low and BAI is high, bus control is given to this card.

BAI — Bus Acknowledge In (active high, 1K ohm (TTL) or 10K ohm (CMOS) pull-up). In serial priority if BAI is high and BRQ* and BUSAK* are low, bus control is given to this card.

BAO — Bus Acknowledge Out (active high). In serial priority BAO is high during a BUSAK* cycle if BRQ* is high. BAO is connected to BAI of the next lowest priority controller.

Serial Priority Signal Sequence. The signal sequence for serial priority is shown in figure 2-5.

● BRQ* shall not occur if BUSAK* is low.

● BUSRQ* occurs in response to BRQ*.

● BUSAK* occurs in response to BUSRQ* (see STD specification).

- BAI occurs in response to BUSAK*.

- BAO occurs in response to BAI and BUSAK*.

Serial Priority, Interface Practice. Cards designed to work with multiple bus requests using serial priority require circuit connections at the user interface edge of the controller cards. The STD Practice for compatibility is defined for each controller.
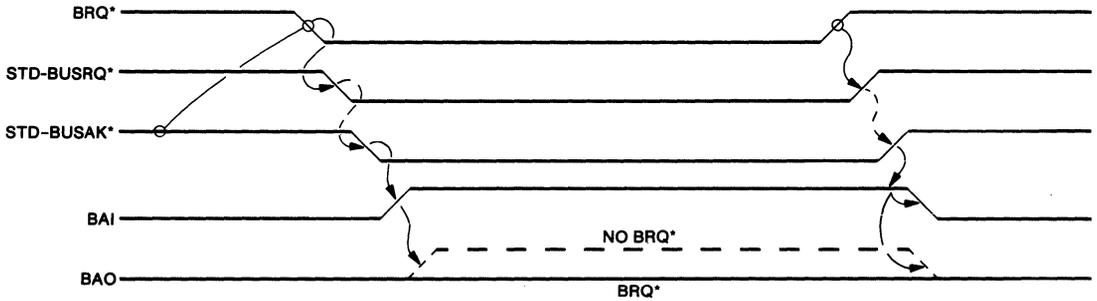
Figure 2-5. Serial Priority Signal Sequence

Mechanical:

- Connector layout for controller cards is as shown in figure 2-6. The ground pins are the top row and the signal pins are the bottom row.

- Connector with a minimum of six pins: three signal lines and three ground lines.

- Connector pins are 0.025-in. square posts or equivalent.

- Mating cables are twisted pairs.

Electrical:

- LSTTL or high speed CMOS logic levels.

- Connector pin assignments:

Pins 1, 3, 5	Ground
Pin 2	BAI
Pin 4	BAO
Pin 6	BRQ*
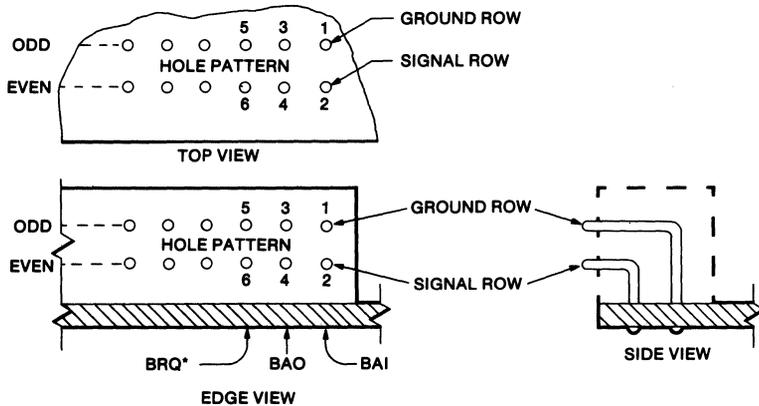
Figure 2-6. Recommended Connector Arrangement for Bus Controller Cards Using Serial Priority

Parallel Priority Bus Control. A parallel scheme for bus priority can be implemented on the STD BUS, so that the priority logic rides on a separate card and not on each peripheral card. The parallel priority card is a modular function that can be tailored to individual processor requirements. This scheme allows peripheral cards to be processor-independent. It requires that individual requests and acknowledges be made from the user edge of the card, as shown in figure 2-7. The parallel priority encoder could be included on the processor card.
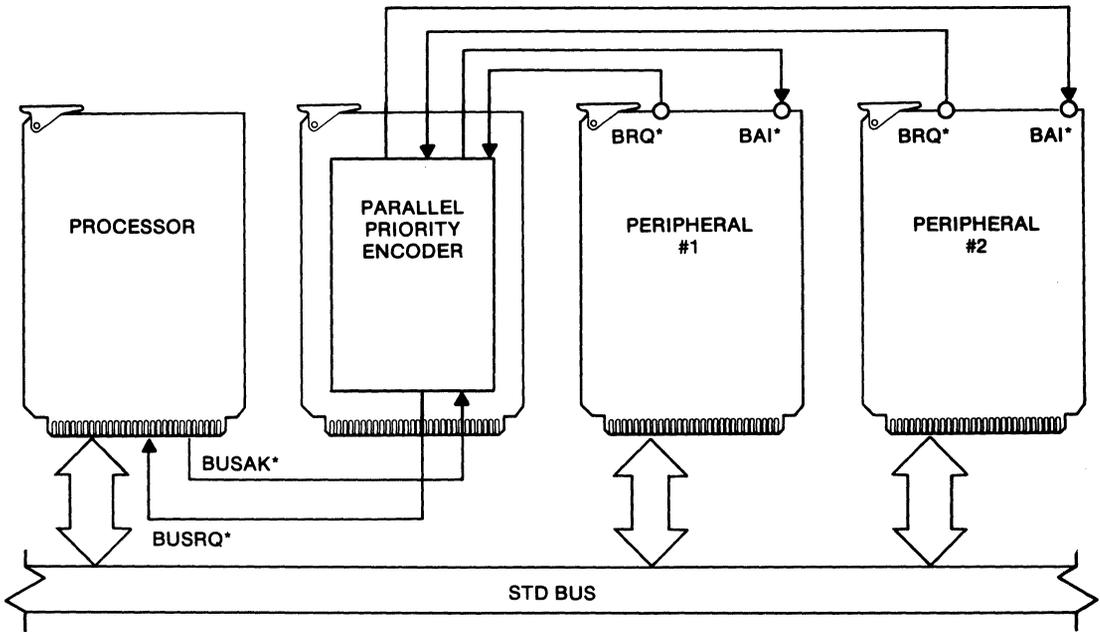

Figure 2-7. Parallel Scheme for Bus Priority

User Interface Signals for Parallel Priority Bus Control. This practice defines two signals for the user interface which allow implementation of the parallel priority scheme shown in figure 2-7. The two signals are:

- BRQ* — Internal Bus Request
- BAI* — Bus Acknowledge In

BRQ* — Internal Bus Request (active low). This signal indicates that the card is requesting bus control. BRQ* is passed separately by each controller card to a priority resolver card via the user interface. The priority resolver shall control BUSRQ* and respond to BUSAK* on the STD BUS.

BAI* — Bus Acknowledge In (active low, 1K ohm (TTL) or 10K ohm (CMOS) pull-up). BAI* is passed separately from the priority resolver card to each controller card via the user interface. Bus control is given to the controller card that senses BAI* low.

10

Parallel Priority, Interface Practice. Cards designed to work with multiple bus requests using parallel priority require circuit connectons at the user interface edge of the card. The STD practice for compatibility is:

Mechanical:

● Connector layout for priority resolved cards is as shown in figure 2-8. The ground pins are the top row and the signal pins are the bottom row.

● Four connections for each request channel: two signal lines and two ground lines.

● Connector pins are 0.025-in. square posts or equivalent.

● Mating female connectors are four pins per channel, in any size from single channel (4-pin) to multiple channel.

● Mating cables can be twisted pairs or flat cable.

Electrical:

● LSTTL or high speed CMOS logic levels.
● Connector pin assignments:

Pins	1,3	5,7	9,11	—,—	—,—	Two ground pins for each channel.
Pin	2	6	10	—	—	One BAI* signal for each channel.
Pin	4	8	12	—	—	One BRQ* signal for each channel.
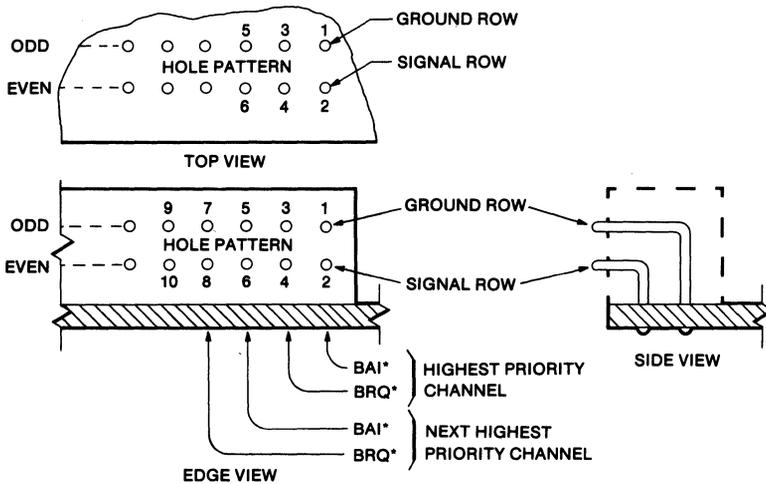
Figure 2-8. Recommended Connector Arrangement for Priority Resolver Cards for Parallel Priority Bus Control

Memory Expansion Practice

The STD BUS supports a primary memory space of 64K. Expansion of memory to 128K is supported by the MEMEX line on the bus. This practice discusses using the MEMEX line for expansion and suggests other methods.

MEMEX Memory Bank Selection. The MEMEX line is one of the signals for controlling fundamental memory operations. MEMEX must be included in the memory selection decoders for the STD compatible memory cards. When MEMEX is low the primary system memory is enabled. MEMEX may be used to enable an alternate 64K memory bank if the memory cards can be strapped for either high or low level enable by the MEMEX signal.
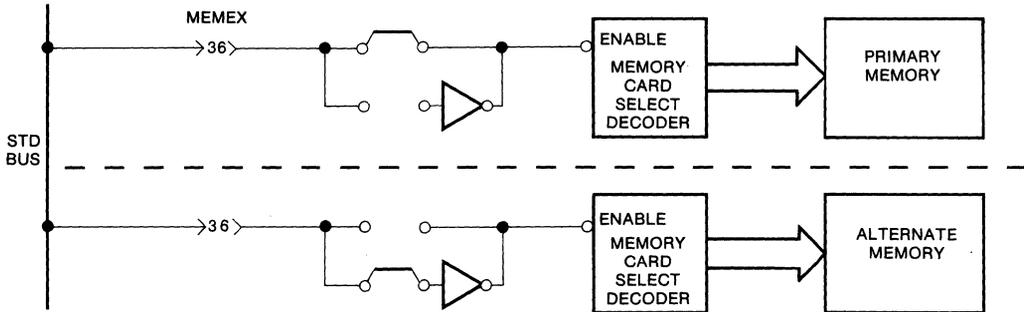
Figure 2-9. MEMEX Memory Bank Selection

Output Port Memory Bank Selection. Multiple banks of 64K memory may be selected by using an output port to enable individual banks. Various schemes are possible. The use of output port decoding to expand memory requires additional support logic on the memory cards.

On-Board Port Memory Selection. The on-board port scheme of memory expansion suggests using port address FF to decode and latch a strappable memory enable signal on each memory card. This scheme is represented in figure 2-10. Port address FF is decoded to enable latching the card select from the data bus. The latch outputs are jumper selectable to allow bank assignment for individual cards. System reset forces selection of memory bank 1 for compatibility with existing software.
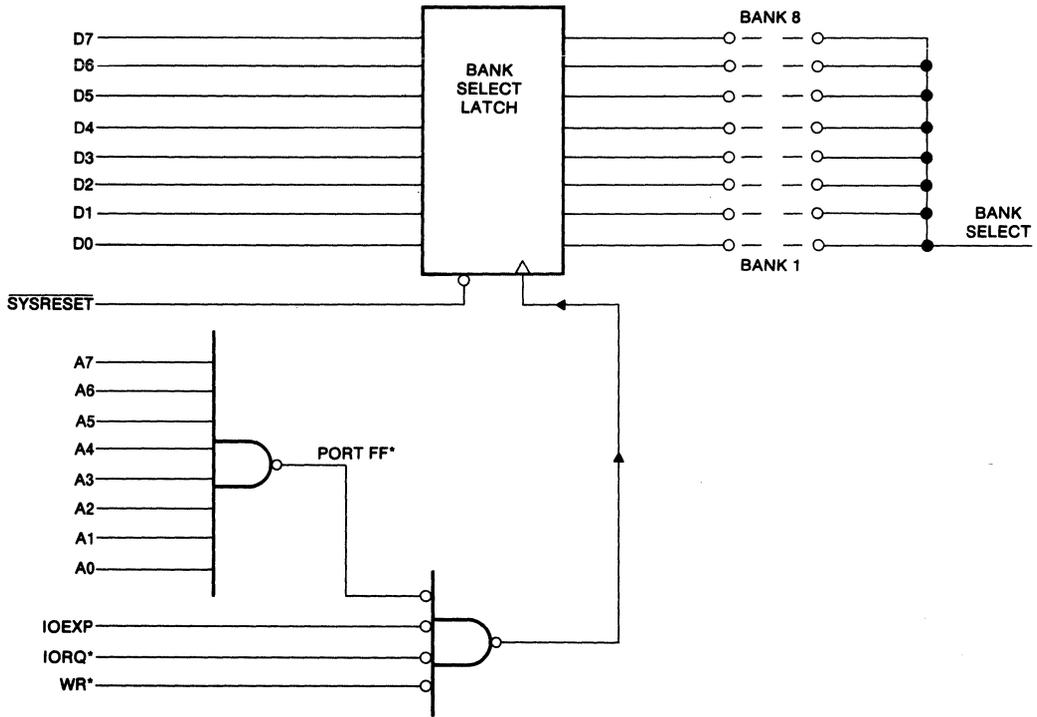
Figure 2-10. On-Board Port Memory Selection

Off-Board Port Memory Selection. The off-board port scheme of memory expansion suggests using a standard output port and wiring to special memory cards via the user interface. The memory cards require a user interface connection into the memory selection decoder on the card as shown in figure 2-11.
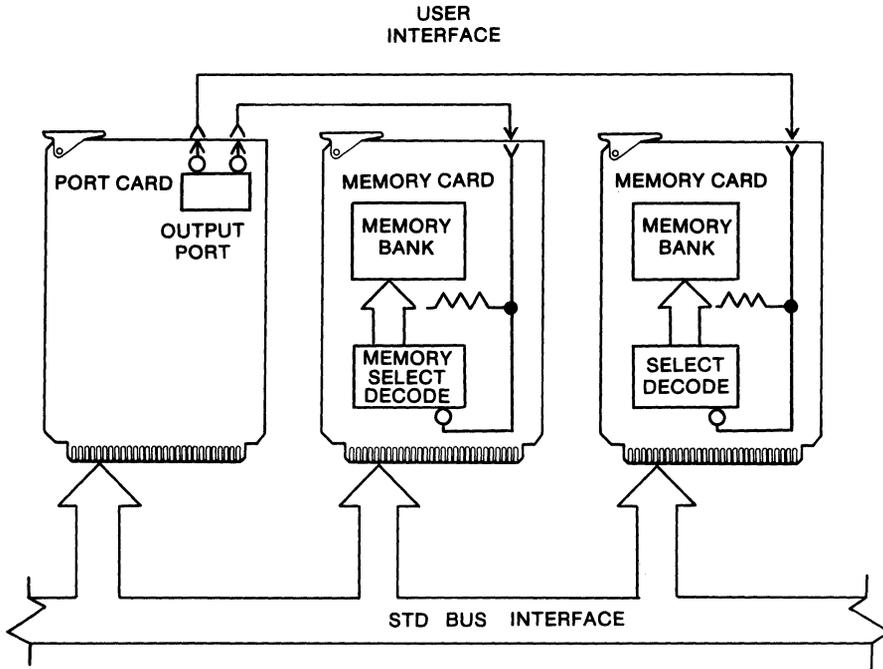
Figure 2-11. Off-Board Port Memory Selection

Multiplexed Memory Addressing. Processors on the STD BUS with more than 16 address lines can be accommodated by multiplexing up to 8 additional address lines on the data bus. This scheme assumes the processor timing can accommodate multiplexed addressing.

Multiplexed addressing requires special memory cards capable of demultiplexing and decoding the upper address lines.

The STD BUS pins are defined as shown in figure 2-12 for multiplexed data bus operation.

BUS PIN	SIGNAL NAME	SIGNAL DESCRIPTION
8	D7/A23	High order data/adr segment.
10	D6/A22	
12	D5/A21	
14	D4/A20	
7	D3/A19	
9	D2/A18	
11	D1/A17	
13	D0/A16	Low order data/adr segment.

Figure 2-12. Multiplexed Data Bus Pin Definitions

10

Backplane Practice

Extending the STD BUS Off the Backplane. The STD BUS backplane is sensitive to layout, length and loading and is subject to speed limitations. The bus is confined to the backplane so that its characteristics can be predicted and controlled. The backplanes are engineered to be reliable with properly buffered STD cards. Because of the critical nature of the BUS, extension of the bus off the backplane is not recommended.

Functions can be extended away from the backplane when properly buffered.

Backplane Bus Design Considerations. The physical nature of the bus with its ordered layout of parallel signal traces causes the bus to act as a controlled transmission line. Transmission lines of this nature have the undesirable signal properties of crosstalk and line reflections. The ordered bus layout allows these properties to be predicted and controlled.

Crosstalk on a printed circuit bus backplane cannot be eliminated, however some element of control is possible with proper layout considerations. Uniform track spacing and the use of ground planes or ground track shielding are some techniques that should be considered. A uniform distribution of signal track to ground capacitance will provide some rise time control which will act to reduce crosstalk.

Backplane Terminations. The reflection characteristics of the bus signal lines can and should be controlled by proper termination. Ideal termination requires terminating each signal in its theoretical characteristic impedance. The backplane bus impedance by itself is predictable, however as cards are introduced into various slots along the bus the impedance can only be estimated.

There are various methods of providing physical termination. An example using passive AC termination for TTL is shown in figure 2-13. This circuit does not affect the DC drive and loading of the bus signal; however, high frequency ringing is effectively terminated to the characteristic impendance of the bus line.

Termination networks can be optimally located if the exact bus loading configuration is known and fixed. Since loading changes with the number and location of cards on the bus optimal termination location is impossible. Considering only first order effects, termination networks can be located either on the backplane motherboard or on a separate terminator card.

Signal Pull-Ups. Bus driving devices for LSTTL do not pull the bus signals to the full 5 volt high level. Full 5 volt logic swings can be achieved by the addition of pull-up resistors to the bus signals. Pull-ups may be located on the backplane motherboard or on a separate card.

A 1K ohm resistor is recommended for the LSTTL STD BUS as shown in figure 2-13.
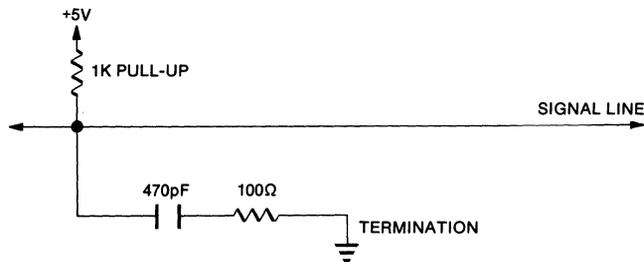
Figure 2-13. Passive AC Termination and Signal Pull-Up

Typical practice in a CMOS STD BUS system is to use the bus without termination. Any termination that is used should not exceed the rated load capacitance. The power drawn by termination should also be allowed for, since some termination schemes can draw a significant portion of system power. The need for termination is related to bus length and processor speed, as well as other factors.

Open-Collector/Drain Bus-Signal Practice

Bus control inputs to the processor card are often wire-OR connected, which requires open-collector/drain drivers. It is recommended, as STD Practice, that the following signals be open-collector/drain on any source card and pulled up on any destination card:

- BUSRQ* — Pin 42
- INTRQ* — Pin 44
- WAITRQ* — Pin 45
- NMIRQ* — Pin 46
- SYSRESET* — Pin 47
- PBRESET* — Pin 48

Also, it is recommended that these lines be specified as follows:

- Low-Level active signal.
- LSTTL or high speed CMOS logic levels.
- Driver sink capability of 16 mA at 0.4V for TTL or 6 mA at 0.37V for CMOS.
- Open-collector/drain driver with 10K pull-up.
- Destination load pull-up of 4.7K (TTL) or 10K (CMOS).

CMOS Load Capacitance Practice

The maximum load capacitance seen by any card should not exceed 150 pF. This load capacitance includes bus capacitance and input capacitance of all other cards in the system. Input capacitance for each card should not exceed 10 pF.

CMOS User Edge Input Practice

Typical practice is to have no protection circuitry at the user edge of the STD card. However, if voltage transients are expected on the inputs, protective circuitry can be used to prevent latch-up and possible chip damage. Typically, the protective circuit is a current-limiting series resistor, or voltage-clamping diodes.

CMOS Pull-Up Resistor Practice

Since CMOS gates draw the most power when inputs are floating, pull-up resistors are sometimes required. It is recomended that these pull-ups be on the interior of the STD card whenever possible. Floating STD BUS lines are the responsibility of the current bus master. In the event of the transfer of bus control, the requester is responsible for floating STD BUS lines.

10

STD BUS SPECIFICATION

16-Bit Data Transfers

I. INTRODUCTION

This document lists the changes and additions to the STD-80 rev 2.3 Bus Specification to support 16-bit data transfers for memory and I/O cards and expands memory addressing from 20- to 24-bits. These changes provide the foundation for more powerful 16 and 16/32-bit processor families such as the 680X0 and 80X86. The key design goal is downward compatibility with all existing STD Bus I/O mapped cards while supporting full 16-bit data transfers.

Assumptions

The following assumptions are made for 16-bit transfers:

*   The card dimensions, bus connector, electrical requirements, and power supply voltage definitions remain the same as defined in the STD Bus Specification.

*   CPU cards that support 16-bit transfers must be compatible with existing 8-bit I/O cards.

*   New 16-bit memory cards may be required for CPU cards that support 16-bit transfers.

*   MEMEX* is used (in conjunction with A0) to control 16-bit transfers.

*   Interrupts are supported as in the STD Bus Recommended Practice.

*   Supports CMOS and TTL STD Bus.

This specification allows new memory, I/O, and CPU cards to use a full 16-bit data path on the STD Bus, with data transferred as a low byte, high byte, or full word. New CPU cards must also switch between 8- and 16-bit data transfer modes in order to maintain compatibility with existing I/O cards, which always assume a low byte transfer.

II. FUNCTIONAL DESCRIPTION

16-Bit Bus Pinout

The Bus Connector Pin Assignment in Figure 1 shows the organization and pin-out. Signal flow direction is referenced to the current master. Descriptions of the signals that are redefined by this specification from the STD Bus 8088 rev 2.3 Specification are listed below.

16-Bit Signal Definitions

Data Bus (Pins 7-14, 16, 18, 20, 22, 24, 26, 28, 30). (16-bit, bidirectional, 3-state, active-high). Data Bus direction is controlled by the current master and is affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

All cards should release the data bus to a high-impedance state when not in use. The permanent master shall release the data bus in response to bus request (BUSRQ*) input from a temporary master, as in DMA transfers.

All data bus lines are multiplexed with 16 or the 24 bits of the address bus for address space expansion. The pin assignments for address expansion shall be as shown in Figure 2, the Bus Connector Pin Assignment table.

10

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power	2	+5VDC	In	Logic Power
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBATT	In	Battery Power	6	DCPWRDWN*	In	DC Power Down
DATA BUS	7	D3 (A19)	In/Out (Out)	Low-Order	8	D7 (A23)	In/Out (Out)	High Order
	9	D2 (A18)	In/Out (Out)	Low-Order	10	D6 (A22)	In/Out (Out)	High Order
	11	D1 (A17)	In/Out (Out)	Low-Order	12	D5 (A21)	In/Out (Out)	High Order
	13	D0 (A16)	In/Out (Out)	Low-Order	14	D4 (A20)	In/Out (Out)	High Order
ADDRESS BUS	15	A7	Out	Low-Order	16	A15 (D15)	Out(In/Out)	High Order
	17	A6	Out	Low-Order	18	A14 (D14)	Out(In/Out)	High Order
	19	A5	Out	Low-Order	20	A13 (D13)	Out(In/Out)	High Order
	21	A4	Out	Low-Order	22	A12 (D12)	Out(In/Out)	High Order
	23	A3	Out	Low-Order	24	A11 (D11)	Out(In/Out)	High Order
	25	A2	Out	Low-Order	26	A10 (D10)	Out(In/Out)	High Order
	27	A1	Out	Low-Order	28	A9 (D9)	Out(In/Out)	High Order
	29	A0	Out	Low-Order	30	A8 (D8)	Out(In/Out)	High Order
INTRQI* CONTROL BUS	31	WR*	Out	Write Mem or I/O	32	RD*	Out	Read Mem or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Mem Address Select
	35	IOEXP	Out	I/O Expansion	36	MEMEX	Out	Memory Expansion
	37	INTRQ1*	In	Interrupt Req 1	38	MCSYNC*	Out	CPU Mach Cycle Sync
	39	STATUS1*	Out	CPU Status 1	40	STATUS0*	Out	CPU Status 0
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Int Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Int
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-button Reset
	49	CLOCK*	Out	Processor Clock	50	CNTRL*	In/Out	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUX GND	In	AUX Ground (bussed)
	55	AUX +V	In	AUX Positive (+12V DC)	56	AUX -V	In	AUX Negative (-12V DC)

* Low-level active indicator

NOTE: Address lines A16-A19 are multiplexed on data lines D0-D3 on each address cycle. Typically PCO and PCI are not
used on peripheral cards and should be connected together.

Bus Connector Pin Assignment

Address Bus (Pins 7-30). (24-bit, 3-state, active-high). The address originates at the current master. The permanent master shall release the address bus in response to a BUSRQ* input from a temporary master. The address bus provides 24-address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations.

PIN 36 MEMEX* - Byte high enable (3-state active-low). MEMEX* may originate from the current master and should be used to designate upper byte of full word transfers.

PIN 38 MCSYNC* - Machine Cycle Sync (3-state, active-low). This signal occurs once during each machine cycle of the processor. (Machine cycle is defined as the sequence that involves addressing, data transfer, and execution.) MCSYNC* keeps any peripheral device synchronized with the processor's operation. All STD Bus masters must provide MCSYNC* that meets the STD Bus Timing Specification.

MEMEX	A0	CHARACTERISTIC
0	0	Whole word transfer (A8-15, D0-7)
0	1	Upper byte transfer (A8-15)
1	0	Lower byte transfer (D0-7)
1	1	None

This rising edge of this signal is used to latch the upper 8 address lines (A16-A23) on the low-to-high transition. On 16-bit memory and I/O cards, the rising edge is also used to latch address lines A8-A15.

16-Bit Data Transfers

The 16-bit data transfers are supported both for memory and I/O operations. Sixteen bit transfers consist of two simultaneous 8-bit transfers. A word is defined as two contiguous 8-bit bytes that begin on even address boundaries. Two signals on the STD Bus, A0 and MEMEX, uniquely specify the type of data transfer characteristic as either low byte, high byte or full word transfer. A0, the least significant bit of the Address Bus, specifies even or odd byte. MEMEX, the STD Bus memory expansion signal, defines upper byte or full word transfers. The truth table for data transfers to 16-bit cards is:

The 80X86 family of processors generates the MEMEX and A0 signals directly through the use of the CPU control lines A0 and BHE* (byte high enable). The 68000 family uses the upper data strobe (UDS*) and lower data strobe (LDS*) to generate these control lines.

The MCSYNC* control signal is also generated by the 80X86 and 68000 family of processors as well. The relation of these control lines to the STD Bus is as follows:

STD BUS	80X86	68000
MCSYNC*	ALE	AS*
MEMEX	BHE*	UDS*
A0	A0	LDS*

10

Figure 2 diagrams both the 16-bit data transfer and 24-bit memory address relationships. The STD Bus Address and Data signals are divided into three groups: Low Address, Middle Address/High Data Bus, and Upper Address/Lower Data. The lower 8 address bits are latched and presented to the STD Bus on signal lines A0-A7. The upper 8 data bits, D8-D15 are multiplexed on the middle 8 address bits on the STD Bus A8-A15 signal lines. The upper eight bits of memory address (A16-A23) are multiplexed onto the data bus (D0-D7) respectively and are latched by memory cards on the rising edge (low-to-high transition) of MCSYNC*.

The relative timing for 16-bit data transfers is shown in Figure 2. Detailed timing is in Section 3.
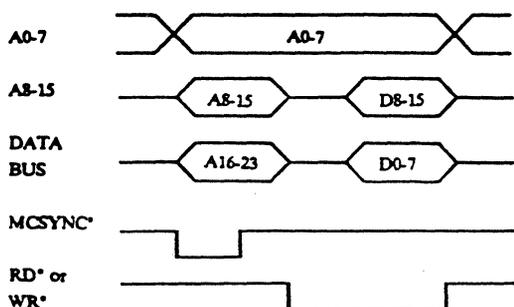

Figure 2. 16-Bit Data Multiplexing.

For full 16-bit data on the STD Bus, it simply requires multiplexing the high order data bits D8-D15 with the high order address bits A8-A15. Mapping is one-to-one so that D8-D15 is multiplexed on A8-A15, respectively. The combination of an active MEMEX (low) with the active edge of RD* or WR* shall latch the upper data byte. Timing requirements are the same as with the STD-80 rev. 2.3 specification so that D8-D15 shall be stable to meet the set-up and hold times required for proper transfers with respect to the Read (RD*) or Write (WR*) signals.

To remain compatible with existing 8-bit memory and I/O cards, buffer swap logic must be placed on 16-bit CPU cards to correctly route the data during I/O operations to 8-bit cards. When a high (odd) byte I/O read or write is issued to an 8-bit STD Bus

I/O card, the CPU card must route the data to or from D0-D7 on the STD Bus vendor's and user's 8-bit I/O cards. Since MEMEX* is not decoded by most existing 8-bit I/O cards, then the MEMEX* signal becomes a don't care status during these data transfers to 8-bit cards.

24-Bit Memory Addressing

The 16-bit specification expands the memory range of the STD Bus from 20 to 24-bits to allow up to 16 megabytes of direct addressing. In the STD-80 rev. 2.3 Specification, 20-bit memory addressing is supported by multiplexing address and data at the beginning of each STD Bus cycle. The same decoding concept used in the 20-bit standard is valid for 24-bit memory addressing by defining four extra address lines, A20-A23, to be multiplexed on the data lines D4-D7 respectively.

III. ELECTRICAL SPECIFICATIONS

The Bus Write and Bus Read Timing from the STD-80 revision 2.3 specification is reproduced on the following pages with the addition of the address and data timing for 16-bit data transfers.

Data Transfer

The Read and Write timing for 16-bit data transfers is shown in Figures 3 and 4. The timing is quite simple. It only requires specifications for set up and hold times to multiplex the data onto the bus. For full 16-bit data on the STD Bus, it simply requires multiplexing the high order data bits D8-D15 with the high order address bits A8-A15. The high order bits are latched into the card by RD* or WR*.

Addressing

Setup and hold timing for signals associated with the MCSYNC* and A16-A23 for latching the upper 8 address bits during 24-bit memory addressing are the same as defined in the STD-80 specification for latching A16-A23 for 20-bit addressing.

IV. MECHANICAL SPECIFICATIONS

No changes are required to the physical and mechanical specifications as detailed in Chapter 4 of the STD-80 rev 2.3 specification.
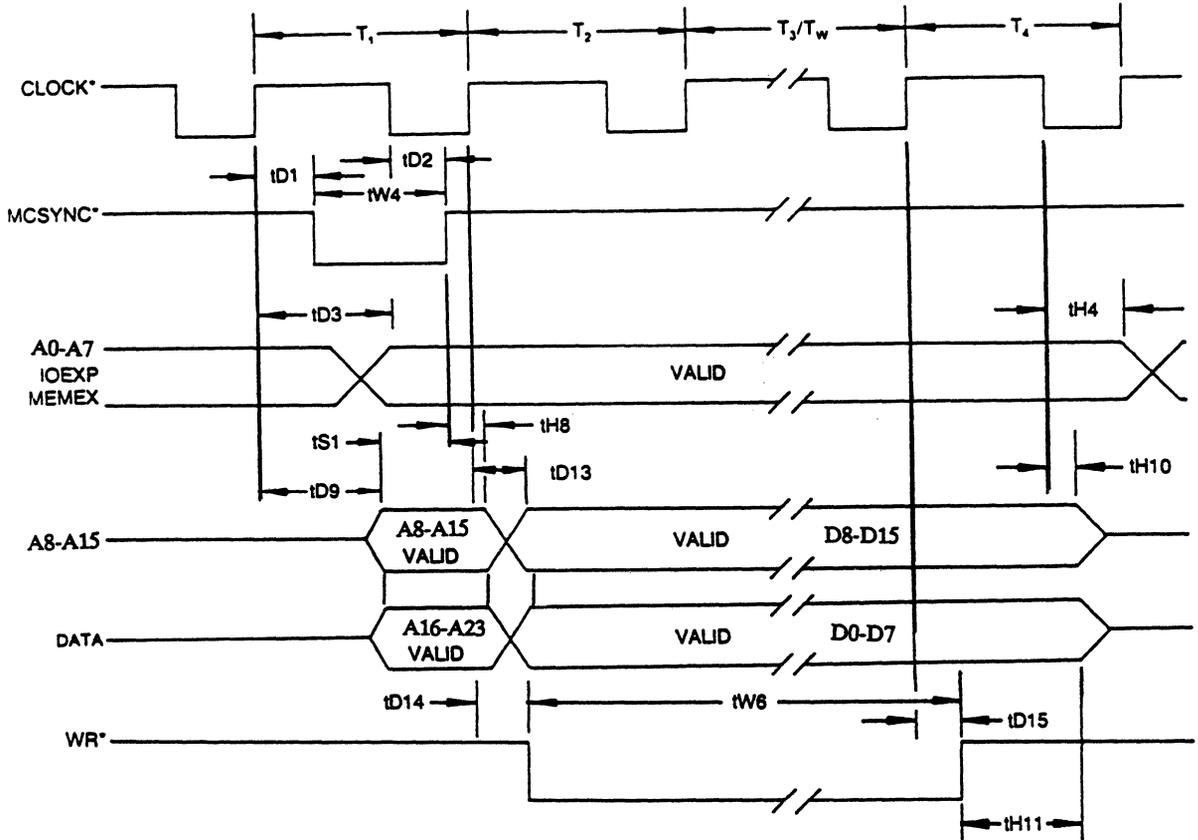
SYMBOL	PARAMETER	5.0 MHz		8.0 MHz	
		MIN.	MAX	MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low (1)	0	98	4	60
tD2	Delay from CLOCK* to MCSYNC* high	3	85	3	50
tD3	Delay from CLOCK* to Address 0- 7, MEMEX, IOEXP		130		75
tD9	Delay from CLOCK* to Address 8-23	0	125	0	73
tD13	Delay from CLOCK* to Data valid		122		97
tD14	Delay from CLOCK* to Advanced WR* low	0	92	8	86
tD15	Delay from CLOCK* to Advanced WR* high	0	90	8	71
tH4	Address 0- 7 MEMEX, IOEXP hold after CLOCK*	0		0	
tH8	Address 8-23 hold after MCSYNC*	20		10	
tH10	WR* Data hold after CLOCK*	0		0	
tH10	Data hold after Advanced WR* high	58		24	
tS1	Address 8-23 setup to MCSYNC*	15		15	
tW4	MCSYNC* pulse width	59		43	
tW6	Advanced WR* pulse width	335		210	

All times given in nanoseconds
(1) When the CPU inserts an I/O wait state, the MCSYNC* timing for 5MHz may be changed as follows: tD1 min. 0; max. 170. Although this allowance was not part of the original Bus Specification, it allows some manufacturers to generate MCSYNC* in a different manner. However, since it may not be compatible with some WAITRQ* implementations, caution is advised.

16-Bit Bus Write Timing.
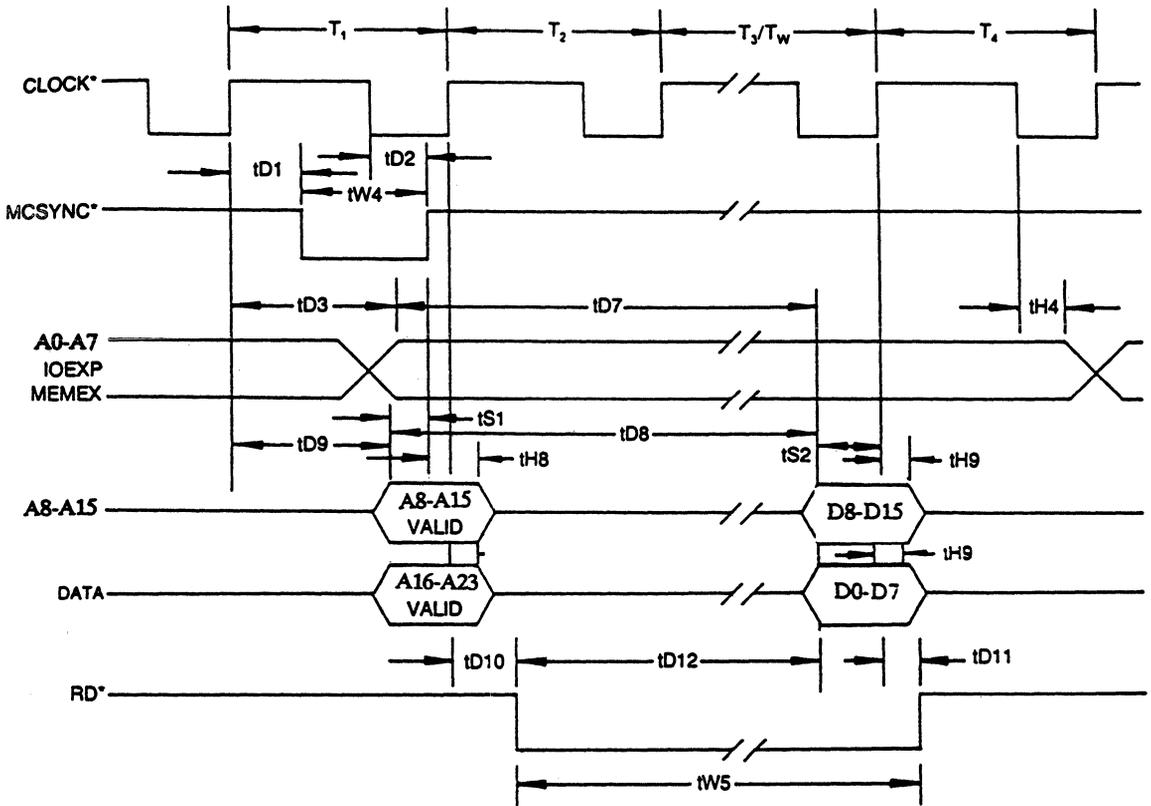
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CLOCK*

MCSYNC* tD1 tD2 tW4

A0-A7 IOEXP MEMEX tD3 tD7 tH4

A8-A15 tS1 tD8 tS2 tH9 tD9 tH8

A8-A15 VALID   D8-D15

DATA A16-A23 VALID   D0-D7 tH9

RD* tD10 tD12 tD11

tW5

SYMBOL	PARAMETER	5.0 MHz		8.0 MHz	
		MIN.	MAX	MIN.	MAX
tD1	Delay from CLOCK* to MCSYNC* low (1)	0	98	4	60
tD2	Delay from CLOCK* to MCSYNC* high	3	85	3	50
tD3	Delay from CLOCK* to Address 0- 7		130		75
tD7	Delay from Address 0- 7 MEMEX, IOEXP to data valid	415		255	
tD8	Delay from Address 8-23 to data valid	415		255	
tD9	Delay from CLOCK* to Address 8-23	0	125	0	73
tD10	Delay from CLOCK* to RD* low	3	95	3	80
tD11	Delay from CLOCK* to RD* high	3	87	3	75
tD12	Delay from RD* to Data valid	260		140	
tH4	Address 0- 7 MEMEX, IOEXP hold after CLOCK*	0		0	
tH8	Address 8-23 hold after MCSYNC*	20		10	
tH9	RD* Data hold after CLOCK*	6		6	
tS1	Address 8-23 setup to MCSYNC*	15		15	
tS2	Data setup to CLOCK*	55		45	
tW4	MCSYNC* pulse width	59		43	
tW5	RD* pulse width	340		200	

All times given in nanoseconds
(1) When the CPU inserts an I/O wait state, the MCSYNC* timing for 5MHz may be changed as follows: tD1 min. 0; max. 170. Although this allowance was not part of the original Bus Specification, it allows some manufacturers to generate MCSYNC* in a different manner. However, since it may not be compatible with some WAITRQ* implementations, caution is advised.

16-Bit Bus Read Timing.

V. BUS PRACTICE

I/O Addressing - Because data is multiplexed on address lines A8-A15 during 16-bit-data I/O transfers, 16-bit-data I/O cards must latch A8-A15 on-card with MCSYNC* (as is done with memory addressing).

Most current 8-bit-data I/O cards decode at least 10 bits of I/O address (A0-A9) plus I/O expand (IOEXP), but do not latch any of the address lines. Since data is multiplexed on the upper address lines during 16-bit-data I/O transfers, some method must be used to prevent these cards from being incorrectly selected during a 16-bit I/O cycle, as these upper address lines will change when data is present during the I/O read or write cycle.

One method would be to use IOEXP as an enable for non-latching 8-bit-data I/O cards. IOEXP inactive (low) is currently used as an enable for I/O cards that decode only 8 address lines (A0-A7), and is driven low only for accesses to one block of 256 I/O ports (usually 0100-01FFh). I/O cards that decode a 10-bit I/O address and support IOEXP could also be mapped into this block of ports.

Another approach would be to leave possible conflicting I/O addresses vacant. For example, if a 16-bit-data I/O card were mapped at 01F0h, no current (non-latching) 8-bit-data card would be mapped at 0F0h, 2F0h, or 3F0h. Address lines A8 and A9 could then change during accesses to the 16-bit-data card without selecting an 8-bit-data card. In PC-compatible systems, port address ranges x50h-x5Fh and xE0h-xEFh can be used for 16-bit-data I/O ports without conflicting with any of the PC's reserved 8-bit-data ports.

It is recommended that 16-bit-data I/O cards decode the full 16-bit I/O address to make use of redundant addresses. It is also recommended that new 8-bit-data I/O cards latch A8-15, to avoid addressing problems in 16-bit systems.

8-bit Memory and I/O Compatibility: Compatibility with older 8-bit memory and I/O cards is possible with a number of different techniques. No specific technique is required by this specification.

One method allocates space in the memory and I/O maps which is defined for 8-bit data transfers only. For accesses to these areas, the master CPU is forced into 8-bit data transfers without regard for the instruction being executed. All data is routed to D0-D7 for transfers within this memory and I/O space, and word transfer operations are converted into two successive STD Bus byte operations for compatibility with existing 8-bit memory and I/O cards. Other memory and I/O areas are defined as 16-bit data, and have data routed over D0-D7 and/or D8-D15 as required.

Another technique, referred to as automatic bus sizing, lets the master CPU sample a status line driven by the memory or I/O card and decide whether that card will support 16-bit data transfers. If the response indicates an 8-bit boards, the CPU will automatically switch to 8-bit data transfers with all data routed to D0-D7. If the response indicates a 16-bit card, data is routed over D0-D7 and/or D8-D15 as required.

Automatic bus sizing is an option that can be implemented in both 16-bit CPU and I/O card designs. No STD Bus signals are allocated for use as 16-bit memory or 16-bit I/O status lines. If implemented, the practice for compatibility of these two 16-bit status lines is defined as:

Mechanical:

* Two connections for each 16-bit status line, with one being the status line and the other a ground.

* Connector pins are 0.025-in. square posts or equivalent

* This practice does not define the method for fastening the cable to the requesting card.

* Mating cables can be twisted pairs or flat cable.

Electrical:

* Low-level active signal

* LSTTL or high speed CMOS logic levels

* Drive sink capability of 20 mA at 0.4V

* Open collector/drain drive with 330 ohm pull-up resistor minimum.

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16-bit Data Transfers - Word-wide data transfers to 16-bit memory and I/O card are handled in the same manner. MEMEX = 0 and A0 = 0 indicate a 16-bit data transfer on the STD Bus. All 16-bit data transfers must be on even word boundaries: A0 must always equal 0. The data is transferred in parallel on both the high and low data bytes of the STD Bus, D0 - D15.

8-bit Data Transfers to 16-bit Cards - Byte read and write operations are supported to 16-bit cards. MEMEX and A0 indicate whether the high or low byte of the 16-bits is being transferred. For both memory and I/O operations, an 8-bit low byte (A0 = 0 , MEMEX = 1) is transferred on the STD Bus low data bits D0 - D7, and an 8-bit high byte (A0 = 1, MEMEX = 1) is transferred on the STD Bus high data bits, D8 - D15.

Some 16-bit data cards designed prior to the release of this specification use D0 - D7 for 8-bit high byte data transfers. These cards can be used as 16-bit data cards in systems designed to this specification if 8-bit high byte data transfers are not used. Full 16-bit data transfers and low byte transfers are identical. Data transfers to 8-bit only I/O cards are not affected. CPU instructions that access these cards should be restricted to those that perform word or low byte access only. Manufacturers of these cards should note this in their literature.

STD80/MPX
STD-80 Series Multiprocessor Extension Addendum

Version 1.0
5/29/92

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STD80/MPX

STD-80 SERIES MULTIPROCESSOR EXTENSION ADDENDUM

Version 1.0   5/29/92

1.0 INTRODUCTION

The STD-80 Series Specification created by the STD BUS Manufacturers' Group has been a firm foundation that has allowed both manufacturers and customers to create reliable, cost effective systems. With the ever increasing integration of LSI circuits, STD BUS processor cards can now be entire computer subsystems on a single card. There is no physical limitation on having a number of complete computer subsystems residing in the same STD BUS cardrack. However, there has been no standardized protocol for such multiple processor systems to transfer control of the STD BUS backplane between them.

STD80/MPX adds a well-documented, reliable method for providing multiprocessing within standard STD BUS cardracks. By conforming to this Addendum, manufacturers can assure that their multiprocessor products will perform reliably in multi-vendor systems.

2.0 SCOPE

This STD80/MPX Addendum to the STD-80 Series Bus Specification and Designer's Guide published by the STD Manufacturers' Group (STDMG) specifies an arbitration protocol that MUST be followed for STD80/MPX compatibility.

Section 5 is the actual STD80/MPX "Standard". It gives timing and state diagrams required to transfer control of the STD BUS from one processor to another, and to resolve priorities on multiple simultaneous requests.

Section 6 includes the "Practice" topics of STD80/MPX, including a discussion of some of the design considerations when implementing STD80/MPX.

STD80/MPX designers have a range of choices concerning when to allow requests for the STD BUS. For instance, the designer may include arbitration for the STD BUS in order to receive off-board interrupt vectors. This Addendum does not standardize these features. Optional features will sometimes require additions to the "Standard" state machines. In all cases, the state transitions and timings specified in this Addendum can be supplemented, but they must not be altered.

Because the STD Series 80 specification is targeted for Intel architecture processors, this Addendum has been developed and tested with the Intel architecture. However, this does not preclude the use of STD80/MPX with other processor architectures if sufficient consideration is given to the various design constraints.

3.0 DEFINITIONS

Arbiter. The circuitry that resolves the priority of multiple STD BUS requests and performs the transfer of control from one processor to the next.

BUSLOCK. A mode of operation where a processor prevents all other processors from accessing the STD BUS by ignoring any requests for the bus. This mode is entered by the processor by setting the PORTLOCK bit in an I/O port and gaining control of the STD BUS.

CPU Number. Each STD80/MPX processor is assigned a unique CPU Number from 1 to 7, inclusive. Each processor is numbered from right (highest priority) to left, starting with CPU Number 1. The rightmost processor must be CPU 1, and is also given the title HOST CPU. CPU Number also establishes the address to write to to cause an interprocessor interrupt.

This specification does not dictate the CPU number implementation method. On-board switches, jumpers, traces, registers, or CMOS/EEPROM memory are possible implementations to establish CPU Number.

Global. Memory and I/O resources that are accessible over the STD BUS by any processor. Global resources may physically reside on an STD80/MPX processor card, or they may reside on cards plugged into the

STD BUS cardrack.

HOST CPU. The highest priority processor.
The HOST CPU is the rightmost processor,
and is always CPU Number 1. The HOST CPU
always acquires control of the STD BUS upon
system reset. The HOST CPU ignores its PCI
input so that no processors of higher
priority can exist.

Interprocessor Interrupts. The ability of
the processor that currently has control of
the STD BUS to interrupt a selected other
processor by writing to a special global
I/O port. The specific port is based upon
the CPU Number of the processor that is to
be interrupted.

Local. Memory and I/O resources that can
be used during periods when the processor
does not have control of the STD BUS.

Lock. The processor that currently control
the STD BUS has the bus "locked" as long as
it ignores requests by another processor to
release the bus. A processor locks the bus
a) during any global STD BUS cycle, b)
between byte cycles created from word-
operand transfers, c) between cycles
automatically locked by the CPU, d) between
cycles locked by the software LOCK prefix,
and e) while the PORTLOCK bit is set.

Multiple Bus Master. A type of
multiprocessor system where each processor
can obtain control of the backplane
address, data, and control lines. An
arbitration method must be used to ensure
that one and only one processor can drive
the backplane at any one time. STD-80/MPX
is a Multiple Bus Master system.

Multiprocessor. A generic term for a
system where multiple processors operate in
the same system. Can be implemented with
single bus master and I/O or memory mapped
slaves, with networks, or with multiple bus
master schemes.

PORTLOCK. A control bit in an I/O port
that, when set, causes the processor to
arbitrate for control of the STD BUS. Once
acquired, all other processors are
prevented from gaining access until the
PORTLOCK bit is cleared. PORTLOCK is
always set by system reset. The PORTLOCK
bit is to be on the processor's local bus
so that access to the STD BUS is not needed
to read or write to it.

Processor. An STD BUS CPU card with, in
the context of this Addendum, STD80/MPX
arbitration logic on-board.

STD BUS. A modular board-level
microcomputer system, as defined in IEEE
961 and the STD-80 Series Bus Specification
and Designer's Guide published by the STD
BUS Manufacturers' Group.

4.0 TECHNICAL OVERVIEW

The STD80/MPX protocol uses the following
STD BUS backplane signals to arbitrate
multiprocessor access to the STD BUS:

Signal	Usage
BUSRQ*	Bus Request. Used by a processor to request STD BUS access to global STD BUS resources.
BUSAK*	Bus Acknowledge. Used to indicate that a processor currently has control of the STD BUS.
PCI	Priority Chain In. Signifies during arbitration that no processor of higher priority is currently requesting access to the STD BUS.
PCO	Priority Chain Out. Notifies processors of lower priority whether or not they may get STD BUS control at end of current arbitration cycle.
CNTRL*	Control. Fixed timing signal used by the arbitration circuitry on all processors to synchronize priority resolution and granting of control of the STD BUS between processors. Not to exceed 8MHz.

STD80/MPX implements a "latching" bus grant
scheme. That is, whenever a processor is
granted control of the STD BUS, it keeps
control indefinitely, driving address,
data, and control lines. A processor will
only release control of the STD BUS when
another processor requests access to the
bus. This can often result in a single
arbitration cycle followed by a number of
STD BUS read/write cycles.

Methods for "locking" the STD BUS are

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provided so that a processor, upon gaining control of the STD BUS, can assure that critical global operations can be performed without intervening arbitration cycles and loss of the STD BUS.

STD80/MPX uses a serial priority chain for resolution of STD BUS requests that arrive within the same CNTRL* clock cycle. The PCI-PCO priority chain is implemented such that the rightmost processor card in the STD BUS cardrack is the highest priority. Each processor successively installed to the left is of decreasing priority.

The rightmost processor has special significance in STD80/MPX, and is termed the "HOST CPU". The HOST CPU will always gain control of the STD BUS upon system reset. Other processors cannot get access to the STD BUS until the HOST CPU first initializes the system, then unlocks its own arbiter so that other processors can be granted control of the STD BUS.

STD80/MPX supports interprocessor interrupts. Any processor, upon gaining control of the STD BUS, can generate a hardware interrupt at any of the other processors. Global I/O port addresses that are unique for each processor are used for interprocessor interrupts.

The STD80/MPX arbitration process takes three CNTRL* clock cycles. Synchronization

between a processor card's CPU logic and the arbiter requires additional time, and can be specified by each STD80/MPX design.

The physical installation of processor cards under STD80/MPX is shown in Figure 1.

4.1 BUS ARBITRATION

The heart of the STD80/MPX standard is the arbitration logic onboard each processor card. The bus arbitration logic ensures that only one processor has control of the STD BUS at any one time. The STD BUS signals PCI and PCO (the priority chain), BUSRQ*, and BUSAK* are used for the arbitration process. CNTRL* (the STD BUS auxiliary clock signal) is used to synchronize the arbitration logic on all processor cards in the system.

When a processor is executing programs from its own onboard local memory, or accessing onboard local I/O resources, it does not need control of the STD BUS. Control of the bus is only required to access global STD BUS memory or I/O cards. Only one processor can have control of the STD BUS at any one time to access these global resources.

When a processor needs to access global resources, and it did not have control of
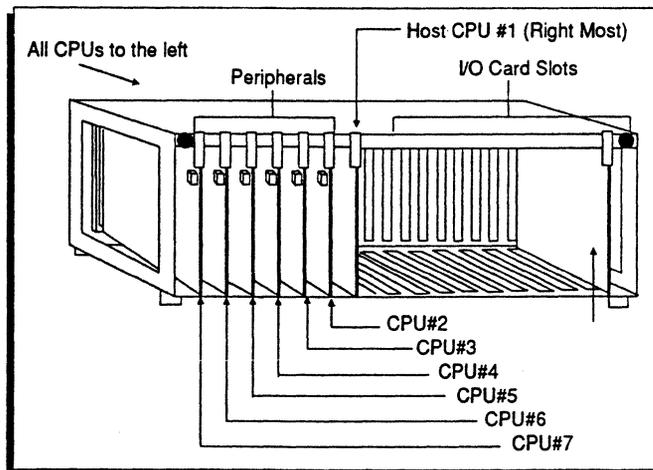

Figure 1. STD80/MPX Card Installation

the STD BUS during the last machine cycle,
its bus arbiter initiates an arbitration
cycle to gain control of the STD BUS. The
CPU will be placed in a wait state until
the arbiter signals that it can now control
the STD BUS.

Two methods of wait states can be
implemented by STD80/MPX processors. The
first is a hardware wait generated by
bringing the CPU "ready" line inactive
until the arbiter signals that the STD BUS
is available. The other is a software wait
where the program loops on the arbiter
status port until the STD BUS is
available. See Section 7 for comparisons
of the two methods.

Figure 2 shows STD BUS control being passed
between three STD80/MPX processors.

The case of simultaneous requests for
control of the STD BUS must be handled by
the bus arbiters themselves during the bus
arbitration cycle, using the PCI-PCO
priority chain. Each processor (starting
with the rightmost, highest priority
processor) gains control of the STD BUS for
its requested memory or I/O cycle plus the
processor's release time. It then releases
the bus and there is another bus
arbitration cycle, after which control of
the STD BUS is granted to the next lower
priority processor. All processors that
activated BUSRQ* during the same CNTRL*

clock period will be granted the bus before
any other processors can add their BUSRQ*
to the queue of waiting processors.

If 'n' processors request the STD BUS
simultaneously, the lowest priority
processor will have to wait 'n' bus
arbitration cycles (three CNTRL* clocks
each), plus the time each of the n-1 higher
priority processors uses the bus, plus the
release time of each of the n-1 higher
priority processors. See Sections 7 and 8
for the implications of this wait.

The STD-80/MPX system is designed for a
high degree of "fairness" in relation to
bus access. Low priority processors cannot
be denied access to the bus by highly
active higher priority processors. All
processors have nearly equal access to the
bus.

Control of the STD BUS remains "latched" to
the last processor that had control of the
bus and is given up only when another
processor tries to access the STD BUS.
This latched feature allows a processor to
arbitrate for the bus once and then
continually access the bus as desired
without arbitration as long as no other
processor requests access to the STD BUS.
Arbitration is only needed when a processor
tries to access global resources and does
not at that time have control of the STD
BUS, that is, another processor has
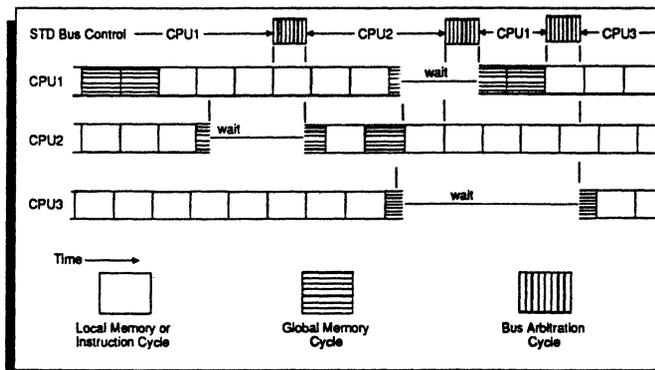
Figure 2. STD80/MPX Arbitration

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arbitrated for and accessed global resources since the last bus access of this processor.

The bus arbitration cycle does not affect processors that are not trying to gain control of the STD BUS. They continue accessing their local memory and I/O without any impact from the backplane arbitrations in process.

4.2 BUS LOCK

Bus "locking" can be performed by STD80/MPX processors for single instructions, or for blocks of instructions. The assembly language LOCK prefix provided by most CPU's is used by the arbiters to ensure that critical read-modify-write operations are not interrupted. Exchange and increment operations on global memory are examples of this type of operation.

For blocks of instructions, a hardware method is implemented. By setting the PORTLOCK bit in an I/O port, a processor can request and be granted exclusive control of the STD BUS. This action has latency issues for access by other processors, and its use must be carefully considered in system design. PORTLOCK is always used on system initialization to insure proper system start-up.

4.3 PRIORITY CHAIN

The PCI-PCO priority chain is used to resolve STD BUS access priorities whenever multiple processors request the bus simultaneously. The STD BUS specification calls for the PCO output from each card slot to be connected to the PCI input of the next card to the left (viewed from the plug-in side of the backplane). This wiring can be found on all STD BUS cardracks.

During arbitration cycles, a processor can, by lowering its PCO output, disallow processors to the left from gaining access to the bus. The rightmost processor card plugged into the cardrack is therefore the highest priority, and is called the HOST CPU.

Because the PCI-PCO chain can be used by I/O cards for other purposes such as interrupt prioritization, the HOST CPU does not use its PCI input. Therefore, there can be no higher priority processor ever requesting the STD BUS. This breaks the PCI-PCO chain into two distinct sections, the I/O card section and the STD80/MPX priority section.

5.0 STD80/MPX TECHNICAL SPECIFICATION

This section presents definitions, state diagrams, timing diagrams, and design considerations for proper design of STD80/MPX systems.

5.1 STD80/MPX ARBITRATION LOGIC

Figure 3 shows a block diagram of the major components of the STD80/MPX arbitration logic. The arbitration logic is divided into two sections, the ARBITER section and the ARBITER-CPU SYNC section.

The ARBITER section is further subdivided into the CPU REQUEST section and the BUS ACCESS section. The BUS ACCESS section is composed of two state machines and STD BUS interface logic. The BUS ACCESS section operates synchronously with all other BUS ACCESS sections on other processors to actually transfer STD BUS control from one processor to another. The CPU REQUEST section interfaces the needs of the local CPU into the BUS ACCESS controller.

The ARBITER-CPU SYNC section handles synchonization issues between different synchronous systems, and also handles all aspects of bus locking.

5.2 BUS ACCESS CONTROLLER STATE MACHINE

The BUS ACCESS CONTROLLER (BAC) State Machine must be present on all STD80/MPX processor cards.

BAC handles BUSRQ*, BUSAK*, PCI, and PCO signals, and is clocked by the falling edge of the CNTRL* clock distributed to all arbiters on STD BUS backplane pin 50. All BAC state transitions are synchronous. Figure 4 shows the state transition diagram for BAC.

Upon RESET, BAC enters the BUSRQ state.

When the local processor needs to access STD BUS resident resources, signified by the REQUEST input, BAC enters the BUSRQ state if the BUSRQ* signal on the backplane is inactive (i.e. no arbitration cycle is currently underway). During the BUSRQ state, BAC lowers PCO, and asserts BUSRQ*

onto the backplane. If PCI is active (no higher priority requester) and BUSAK* is inactive (previous bus controller off of bus), BAC generates the GRANT signal.

When in the BUSRQ state, BAC advances to the GRANT state when PCI is active and BUSAK* is inactive. The GRANT state signifies that the local processor can now use the STD BUS. While in the GRANT state, BAC propagates PCI to PCO, and asserts GRANT and BUSAK*.

When in the GRANT state, a RELEASE input causes a return to the IDLE state. In the IDLE state, BAC propagates PCI to PCO.

5.3 CPU REQUEST CONTROLLER STATE MACHINE

The CPU REQUEST CONTROLLER (CPURQC) State Machine must be present on all STD80/MPX processor cards.

CPURQC controls the interaction of local processor requests for offboard resources with the Bus Access Controller State Machine (BAC). CPURQC generates the REQUEST signal to BAC when access is needed, and handles the GRANT signal from BAC when control of the STD BUS is acquired. In addition, CPURQC generates the RELEASE signal to BAC. CPURQC is clocked by the falling edge of CNTRL* from the backplane. CPURQC state transitions are synchronous with CNTRL* except where noted. Figure 5 shows the state transition diagram for CPURQC.

When in the LOCAL state, CPURQC asserts no outputs, and the local processor is accessing local resources. When local circuitry detects a need for STD BUS control, it asserts STDCYCLE. This may be merely an address decode. After deglitching and synchronization, SYNCSTDCYCLE is issued, which causes CPURQC to asynchronously enter the REQUEST state.

When in the REQUEST state, CPURQC asserts the REQUEST signal to BAC. CPURQC remains in the REQUEST state until BAC returns the GRANT signal, signifying that STD BUS control is now with the local card. Upon receiving GRANT, CPURQC advances to the STD state.

When in the STD state, CPURQC asserts
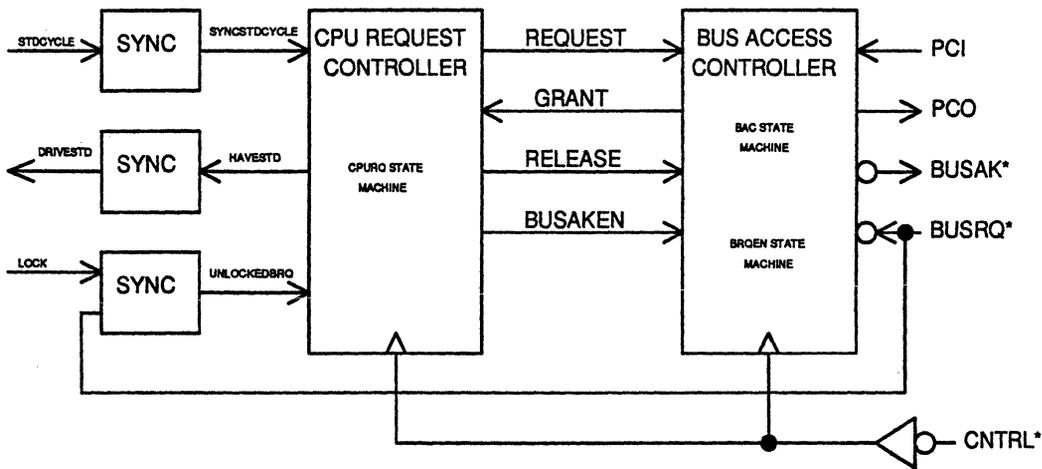
Figure 3. STD80/MPX Arbiter
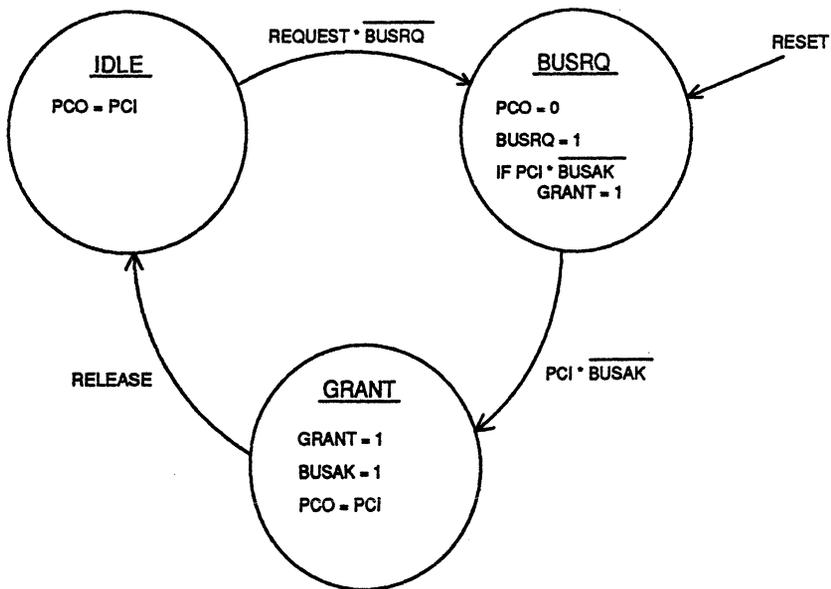
Figure 4. BUS Access Controller State Machine

BUSAKEN to enable the BUSAK* signal offboard signifying acceptance of STD BUS control. The STD state also asserts the HAVESTD signal to onboard logic to indicate that the STD BUS is now available for use. HAVESTD is synchronized to the CPU timing.

CPURQC remains in the STD state until an UNLOCKEDBRQ input is received, indicating that a synchronized, request from another STD80/MPX processor has been detected, and the local processor does not have the STD BUS locked. UNLOCKEDBRQ causes CPURQC to asynchronously enter the RELEASE state.

When in the RELEASE state, CPURQC asserts the RELEASE signal to BAC. BUSAKEN is still held asserted so that the local BUSAK* signal remains driven on the STD BUS. CPURQC remains in the RELEASE state until the GRANT signal from BAC is deasserted, indicating that the STD BUS control has been lost. CPURQC then returns to the LOCAL state.

CPUQRC enters the REQUEST state upon RESET.
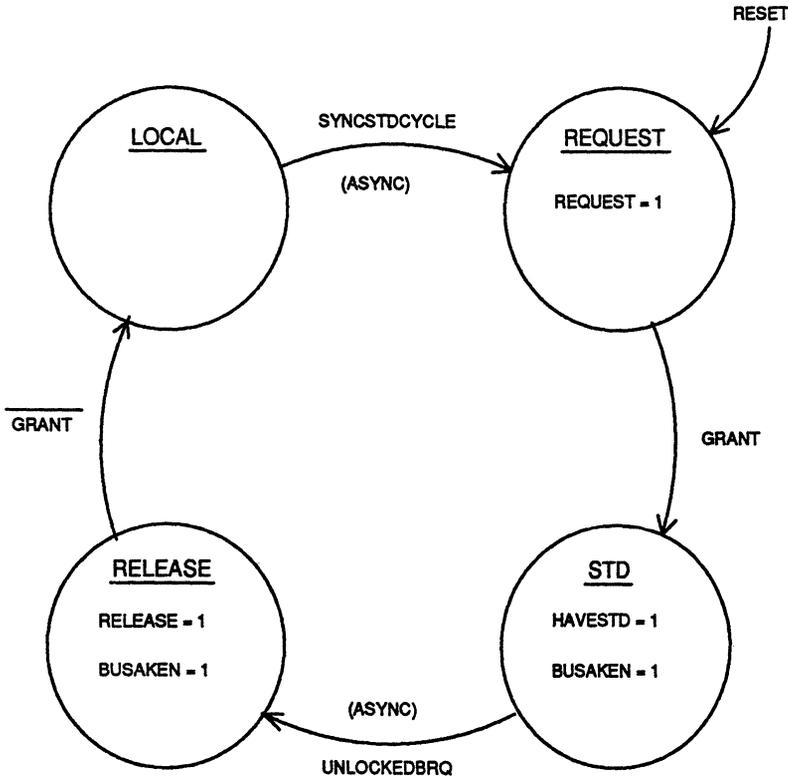
Figure 5. CPU Request Controller State Machine

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5.4 BUSRQ ENABLE STATE MACHINE

The BUSRQ Enable (BRQEN) State Machine must be present on all STD80/MPX processor cards.

BRQEN controls the enabling of the local BUSRQ signal onto the STD BUS BUSRQ* signal line. BRQEN is an asynchronous state machine. Figure 6 shows the state transition diagram for BRQEN.

Upon RESET, BRQEN enters the IDLE state, and no outputs are asserted. When the Bus Access Controller (BAC) is in its BUSRQ state, BUSRQ* is not asserted on the backplane, and PCI input is asserted, BRQEN enters the BRQEN state.

When in the BRQEN state, the BUSRQEN signal is asserted to allow the local BUSRQ signal to drive the STD BUS BUSRQ* line. BRQEN remains in the BRQEN state until either PCI input is lost, or BAC is in the GRANT state and the STD BUS BUSRQ* signal is deasserted. Upon either of these conditions, BRQEN returns to the IDLE state.
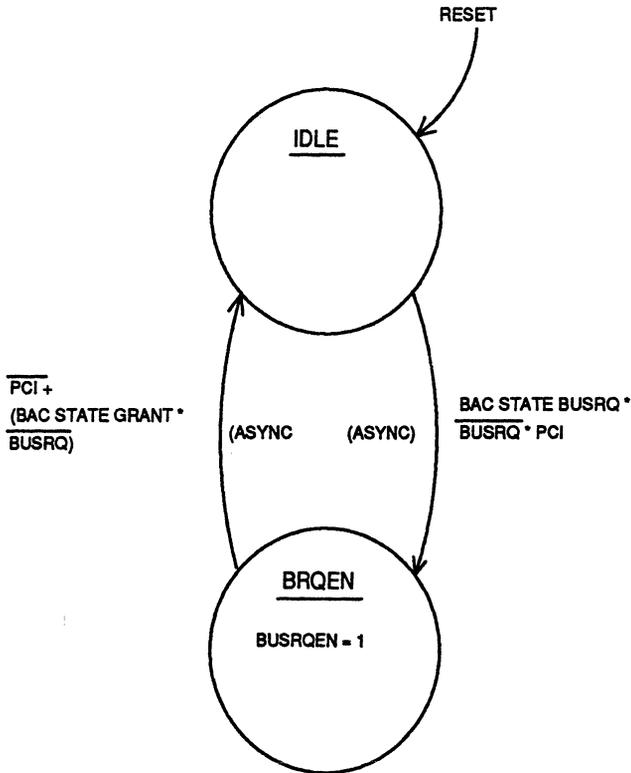
Figure 6.   BUSRQ Enable State Machine

5.5 STD80/MPX ARBITRATION TIMING

Figure 7 shows timing for the following situation: CPU 1 (highest priority, or HOST CPU) has control of the STD BUS. CPU 2 and CPU 3 both determine they need STD BUS accesses within the same CNTRL* clock period. CPU 2 and CPU 3 both enter BAC state REQUEST. PCI-PCO priority chain settling before the next CNTRL* edge grants access to CPU 2.

After CPU 2 releases the STD BUS, CPU 3 gains control. No other STD80/MPX processor card is allowed to assert BUSRQ* while CPU 3 already has it asserted.

5.6 STD CYCLE REQUEST SYNCHRONIZATION

When onboard logic decodes an offboard access, it generates STDCYCLE. Because the CPU Request Controller (CPURQC) transitions to the REQUEST state asynchronously, this decode must be deglitched before being presented to CPURQC.

The deglitched signal SYNCSTDCYCLE can be set with the trailing edge of a signal signifying stable addresses, such as ALE. Once set, SYNCSTDCYCLE can be cleared when READY is returned to the CPU, as this can only happen after STD BUS access has been gained, and the transfer completed.

5.7 STD BUS GRANT SYNCHRONIZATION

The HAVESTD signal from the CPU Request Controller (CPURQC) is synchronous with CNTRL*. It should be resynchronized with the CPU clock, or a clock associated with backplane cycles (i.e. BUSCLK) before it is used to continue a CPU cycle held up in wait states.
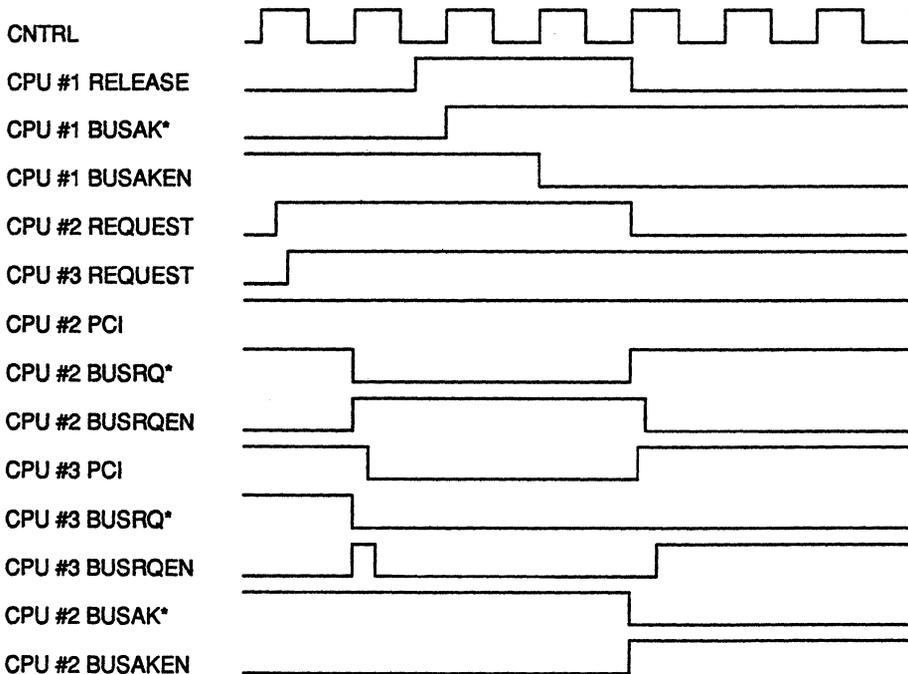
Figure 7. STD80/MPX Arbitration Timing

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5.8 UNLOCKEDBRQ GENERATION

The proper generation of UNLOCKEDBRQ is critical for a "clean" release of the STD BUS. BUSRQ* signals from other processors attemting to gain control of the STD BUS must be delayed until the local processor is in a state where the STD BUS can be given up. This is done through the LOCK signal, which is composed of a number of different types of locks.

The STD80/MPX arbiter is running on its own clock, and is capable of giving up control of the STD BUS at any time, including just at the beginning of an STD BUS cycle, or even in the middle of one. In the case of single STD BUS cycles, it is imperative that control of the STD BUS is not lost until the entire machine cycle has been completed. Therefore, a signal must be generated that locks the arbiter from the instant an STDCYCLE is sensed until that cycle is completed.

Attention must also be paid to CPU word operations that external circuitry divides into a number of sequential transfers of smaller size (i.e. bus converstion cycles in ISA and EISA chipsets). A lock signal must be generated across the entire set of transfers so that the processor does not lose the STD BUS in the middle of an instruction execution and hang until control of the STD BUS can be regained.

Word accesses to odd addresses are a special case. STD80/MPX does not require lock to cover the multiple accesses in this case. See section 7.5.2 for a discussion of this case.

The LOCK signal from the CPU must also be handled so that instructions which the processor (automatically) or the programmer (with the LOCK prefix) indicate as locked cannot be interrupted by loss of the STD BUS.

Finally, the PORTLOCK control bit from an I/O port must lock the bus.

In order to release the bus cleanly, all lock signals should be synchronized to the CPU clock, or an associated bus clock. UNLOCKEDBRQ will cause CPURQC to exit the STD state asynchronously, so it does not need to be synchronized to CNTRL*.

UNLOCKEDBRQ should be asserted synchronously with the CPU related clock, and should only be allowed to be asserted if CPURQC is currently in the STD state.

5.9 LOCAL CPU WAIT STATES

If the local CPU initiates a transfer to a global resource while it does not have STD BUS control, the processor must be placed into wait states. The wait states will continue until the DRIVESTD signal is received. DRIVESTD is synchronous with a CPU related clock, and can be used to initiate the release of the wait state.

Note that it may be necessary to recreate the earlier portion of the machine cycle that executed prior to entering the wait state.

As outlined in Section 7.1, PORTLOCK can be used to request control of the STD BUS without entering CPU wait states.

5.10 INTERPOCESSOR INTERRUPTS

STD80/MPX supports interprocessor interrupts with a single I/O write cycle to a global I/O port address. The CPU Number setting on each processor determines the port address that it will cause it to recognize and interprocessor interrupts.

Note that there is no information content in the actual interprocessor interrupt itself. It is merely an "event" that one processor causes in another. System software will need to react to the event in an appropriate manner.

To interrupt a particular processor, an I/O write to the following address is performed:

CPU #	I/O Write to Port #
1	1330h
2	2330h
3	3330h
4	4330h
5	5330h
6	6330h
7	7330h

7.0 LATENCIES

When an STD-80/MPX processor executes a machine cycle that accesses the STD BUS, the machine cycle will execute full speed if the processor is currently in control of the bus. However, if the processor must arbitrate for the bus, the machine cycle will be extended.

There are a number of components that make up the total delay time that a requesting processor might experience.

If the processor currently in control of the bus does not have any locks active, i.e. it is currently doing local on-board accesses and does not have PORTLOCK set, the bus access time will be a) the amount of time required by the releasing processor's UNLOCKEDBRQ logic to synchronize to the BAC state machine, and b) the three CNTRL* clock cycles required for bus control changeover. This is the best case, where a requesting processor will receive control of the STD BUS at the earliest possible time.

Worst case access times are calculated by the following:

1) If any processor has PORTLOCK set, thereby locking out other processors, the requesting CPU will have to wait until PORTLOCK is released. This is application dependent.

2) If other higher priority processors requested the bus by asserting BUSRQ* in the same CNTRL* clock, each of these processors will obtain the bus and execute at least one STD BUS cycle before the requesting processor is granted the bus.

In 2) above, each processor will complete one STD BUS cycle, assuming that PORTLOCK is not set. The worst case time of this cycle can be calculated from the processor's speed, the longest instruction execution possible, and the releasing processor's UNLOCKEDBRQ synchronization timing.

Worst case timing may be caused if each higher priority CPU is executing a locked 32-bit access to an odd address. In this case, up to 36 STD BUS CLOCK* cycles may be needed by each CPU for data transfer, followed by the UNLOCKEDBRQ synchronization time for each processor.

This latency in receiving STD BUS control may be significant to the lowest priority processor. It should be considered from a system level perspective. Although not required by the STD-80/MPX specification, an abort timer may be beneficial to abort an STD BUS access that is delayed beyond a specified time limit.

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7.0 STD80/MPX PRACTICE

This section contains further discussions on features not covered in the STD80/MPX standard, and how they may affect STD80/MPX design. Also, further discussions on interfacing STD80/MPX arbitration logic into specific designs are included.

7.1 ELIMINATING CPU WAITS WITH PORTLOCK

The PORTLOCK I/O control bit can be set by the programmer to request control of the STD BUS. Software can then poll the DRIVESTD status input to determine when to access the global resource. After transfer to the global resource, PORTLOCK can be released. This method, while it incurs additional execution time overhead, eliminates CPU wait states until control of the STD BUS is gained.

During wait states, the local CPU is in many cases unable to honor any request except reset. No interrupts, DMA, or, in some cases, refresh of dynamic RAM can take place. Because of the possible bus access latencies discussed in Section 7, the worst case bus access time may not be acceptable in some applications. Use of PORTLOCK in these situations is advised.

7.2 STD BUS INTERRUPTS

The INTRQ*, INTRQ1*, and NMIRQ* lines on the STD BUS provide interrupt inputs to processor cards. STD80/MPX systems must be designed such that a single processor responds to each of these signals. These signals should only be enabled and unmasked on the one STD80/MPX processor card that is assigned to handle each specific interrupt.

If external interrupting I/O cards are expected to provide interrupt vectors on the STD BUS during interrupt acknowledge cycles, and the responding processor does not have control of the bus, logic on the processor card must arbitrate for the STD BUS before performing interrupt acknowledge cycles in response to INTRQ* or INTRQ1*. Consideration must be given to possible latencies in responding to the interrupting device due to this arbitration cycle.

If on-board vectors are generated, control of the STD BUS is not an issue during interrupt acknowledge cycles, and no arbitration is necessary at that point. However, when the Interrupt Service Routine (ISR) attached to this offboard interrupt is run, any access to the interrupting I/O card will automatically cause normal arbitration cycles if the interrupted processor card did not have control of the STD BUS. This can cause the ISR to take longer to execute.

NMIRQ* does not require interrupt acknowledge cycles. The only issue in STD80/MPX system design with NMIRQ* is to assign its handling to none, one, or multiple processors by enabling or disabling it on each processor.

7.3 TRADITIONAL STD BUS DMA

The STD-80/MPX standard uses BUSRQ* and BUSAK* for uses different that STD-80 DMA usage. These two usages are incompatible.

In some cases, it may be desirable to support existing DMA-based I/O cards in an STD-80/MPX system. In these cases, the designer may opt to include DMA lock capabilities on the HOST CPU.

DMALOCK can be implemented when the HOST CPU sets PORTLOCK. In this state, all SLAVE CPU's will be locked off of the STD BUS for extended periods, so the system must be able to accomodate this. While in DMALOCK, the HOST CPU can honor BUSRQ* with BUSAK* in the standard STD-80 manner. This allows, for instance, a DMA-based floppy disk card on the STD BUS to be used to read and write to floppy disks using DMA transfers. The HOST CPU can release PORTLOCK, thereby exiting DMALOCK mode, upon completion of the disk transfers.

Implementation details of DMALOCK mode are outside the scope of this standard.

7.4 SIGNAL TERMINATION

Signal termination on STD-80/MPX systems may be required on one or both ends of the STD BUS backplane. Termination in STD-80/MPX systems is left as a system-level consideration.

Care should be taken, in multiple processor systems, to insure that the addition of

processors does not significantly affect termination values. For example, signals should not be terminated on all CPU's, as this would reduce impedances and change DC current levels.

7.5 SOFTWARE CONSIDERATIONS

Software in STD-80/MPX systems is application dependent, and not under the scope of this standard. However, there are a number of software considerations that merit discussion.

7.5.1 INITIALIZATION

Upon powerup, all STD-80/MPX processors resident in the cardrack request access to the STD BUS. This is because the BAC and CPURQ state machines initialize in a request state. In addition, PORTLOCK is initialized in the on state. This guarantees that each processor will obtain the bus for initialization, and not be interrupted during initialization.

STD-80/MPX processors may have widely varying reset startup times. Processors with standard BIOS firmware may require seconds before multiprocessor initialization code executes. Processors programmed directly in dedicated applications may arrive at multiprocessor initalization code much earlier after power on or reset than other processors. The STD-80/MPX arbitration method guarantees a systematic system startup if the following procedure is used.

The HOST CPU, which is guaranteed to gain STD BUS control on reset, should perform any multiprocessor global initialization necessary, then release PORTLOCK. This action will allow PCI to go high on the second processor. The second processor will be granted control of the STD BUS in three CNTRL* clock cycles, even if the processor is not yet executing multiprocessor initialization code. Because PORTLOCK is set on the second processor, it will keep control of the STD BUS until it is fully operational and has performed its multiprocessing initialization. It can then release PORTLOCK.

This sequence will propagate down the PCI-PCO chain until every processor in the system, in priority order, has performed its multiprocessing initialization.

The HOST CPU will not be able to regain control of the STD BUS until all SLAVE CPU's have had control of the bus. Therefore, the HOST CPU can, immediately after releasing PORTLOCK, verify that it no longer has the bus, then set PORTLOCK again to request the bus. When the HOST CPU again regains bus control, it is guaranteed to be after all SLAVE CPU's have executed their initialization routines.

7.5.2 UNLOCKED ODD WORD ACCESSES

An artifact of the Intel 80X86 architecture can create undesirable results in any multiple processor system. Whenever a word-wide transfer is made to an odd address, the CPU automatically performs two independent, back-to-back machine cycles to effect the transfer. A high byte transfer is followed by a low byte transfer.

Whenever an odd address word-wide transfer is made, logic external to the CPU has no way of differentiating this "indivisible pair" of transfers from truly independent, divisible byte transfer instructions. If the LOCK prefix is used during assembly language programming, external logic can use this to ensure that control of the STD BUS is not given up between the two transfer cycles. However, when programming in a higher level language, control over the LOCK prefix may not be possible.

Therefore, it is strongly suggested that whenever designing STD-80/MPX global data structures, that all items be word aligned, or that alternative approaches be taken. If control of the STD BUS were lost between these two cycles, the CPU would be locked in the middle of a single instruction for an indeterminate amount of time (until control of the bus was re-granted).

Note that this is not unique to STD-80/MPX, but is instead an artifact of the operation of Intel processors.

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AN0101

STD Bus, the Industrial I/O Bus

Robert A. Burckle
Vice-President

Abstract - The STD Bus is often referred to as the "Blue Collar Bus" due to its popularity for use in disguised and embedded OEM applications. Its small format, low cost, and wealth of I/O cards coupled with ease of design of special purpose interface make it a natural for machine control, factory automation, test and medical instrumentation. The STD Bus differs significantly from other industrial bus structures even though it may not be obvious from a macro view.

Market Overview

The best way to visualize the STD Bus in relation to other bus structures is to view the industrial bus board market as a three-tiered pyramid, with three distinct characteristics: Cost, Performance, and Installed base.

The top level of this pyramid is the super minicomputer such as offered from such manufacturers as DEC and IBM. The product cost is high as well as the processor performance. The high performance 16- to 32-bit microcomputers offered by the VMEBus, Multibus II, and NuBus is the second tier. The base of the pyramid is dominated by the standard performance processors offered by the STD Bus and PC Bus. These buses are the lowest cost solutions offering satisfactory performance from 8-bit processors like the 8088 through to the 80486.

Notice that the product cost is directly proportional to performance and inversely proportional to the installation base of product. Contrary to the diagram, the lines are not distinct between bus architectures and levels but rather "fuzzy" because of the range of processors and their performance in each group.

Often referred to as the "Blue Collar Bus", the STD Bus was designed for the factory and industrial environment. Developed in 1978 as an 8-bit industrial microcomputer bus, the STD Bus is a much different bus structure than what was originally designed. With the ever increasing demands for more data, improved efficiency, and higher productivity in the factory, the STD Bus has evolved to meet the customers' changing needs. Designated as

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Industrial Computing Spectrum

Processing Power

Cost

VAX
Futurebus

VME, Multibus,
NuBus, Q-Bus

STD Bus   PC Bus

Installed Base
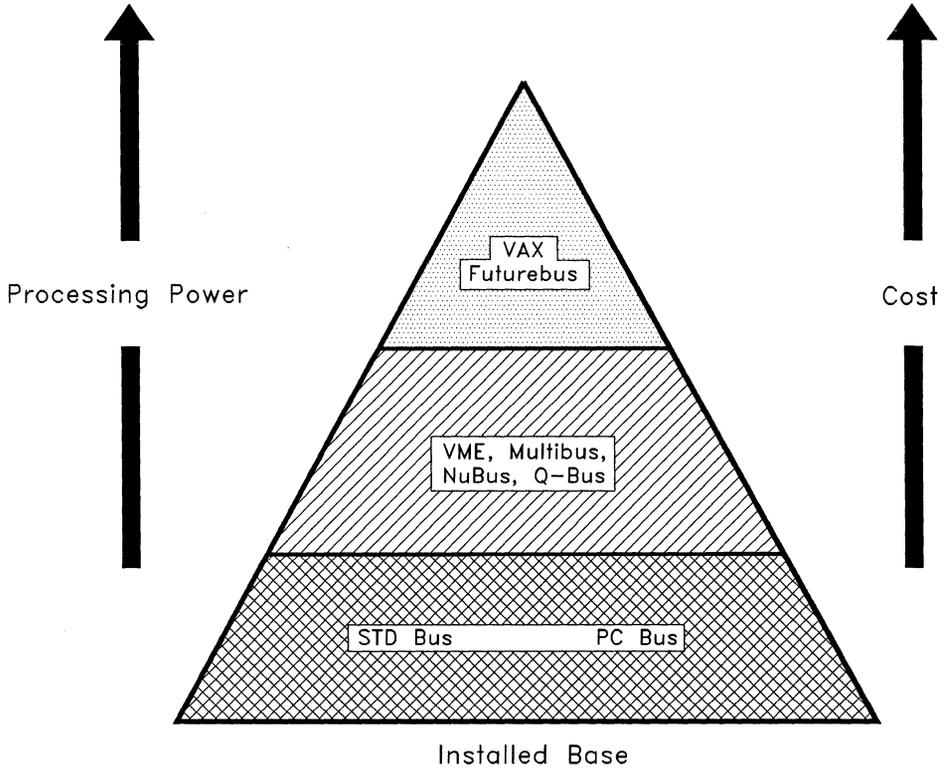
the IEEE standard 961, it is available as a full 16-bit wide bus. Currently the STD Bus Manufacturers Group (STDMG) is exploring ways of implementing a 32-bit wide structure as well.

The STD Bus has used up to 80486DX processors combined with highly integrated supported chip sets and BIOS to allow full wealth of I/O cards available for industrial applications. The prime factor was an upward migration path for existing cards to assure orderly, progressive growth. The result is a lasting standard for industrial applications not threatened by obsolescence or abandonment every 5 years. Its' popularity, due to the open architecture, rugged industrial design, small size, low cost, and ease of I/O interfaces, is well documented with over a half million STD Bus systems presently installed.

Comparison of the Styles

The STD Bus processor utilizes advance technology; although it is not always on the cutting edge with RISC/CISC, SPARC and other processor types. The bus retains a moderate profile focusing on finding solutions to real world problems, not thriving on winning the MIPS race. The STD Bus can be compared to a mid-size family car. It offers the customer a solid, stable mode of transportation rather than the lavish luxury of an expensive American sedan or the high-speed performance of an European import.

However, don't forget there is a wealth of advanced technology available on today's STD Bus products. These include full PC and AT equivalents, 80486 processors, DSPs, video frame grabbers, networks, speech synthesizers, servo controllers, multiprocessor systems and extended temperature (-40°C to $+85^{\circ}$C) CMOS STD Bus cards to name just a few.

Systems Design Methodology

System design has reversed itself over the past 10 years. Previously hardware architectural issues were the major concern because of cost and maintenance, with software being much less of a issue. Today the selection criteria has reversed with software as the driving factor. What has evolved is a standard "Software Bus" built upon a MS-DOS environment assuming a 80X86 PC-AT class machine. AT-compatible machines now exist on the industry standard buses such as STD Bus, Multibus, VMEBus, and others which make the software bus a reality. Now, after the application software direction is set, the optimum hardware can be selected depending upon packaging, form factor, cost, survivability in harsh environments, and industrial interface board selection/availability.

One key factor is that BIOS compatible 8088/80286/80386/80486 PC-XT/AT systems

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architecture - NOT the PC, XT, or AT per se, is a defacto standard for an increasing number of designs. MS-DOS, compatible applications programs and executives, and its requisite hardware platform have created a "Software Bus". The reason for this is that users want solutions to problems not just the latest technology. Plug-and-play software transportable across various bus structures is becoming a reality. Now users can focus on getting the software job done which is the real cost for systems integrators rather than trying to create their own system from the ground up. The selection of a data bus for an industrial design will depend upon the nature of the application as well as the engineer's ability to design and support the product.

With the advent of the "Software Bus" given to us from the pervasive PC, design engineers and systems integrators should reevaluate all alternatives. Users of bus boards choose the applications software first, then select a bus that fits the performance, environmental, packaging and economic criteria. Given compatible software, a wealth of industrial I/O boards, hardware compatibility with the development workstation, small form factor, and low cost, the STD Bus is a very attractive alternative to the PC on the factory floor.

Decisions based on standards

A customer needs to decide upon standards not a company. The electronics industry has seen numerous examples of companies introducing a product line and then abandoning it later. Even a large company does not guarantee stability. Examples include Motorola dropping the Exorbus for the VME, RCA dropping the Monoboards, Zilog dropping the Z-bus, National dropping the CIM bus, and IBM dropping support of the XT/AT bus in favor of the PS-2.

A lasting standard

One factor that the STDMG has not forgotten is the customer and the installed product base. Upgrading to a higher performance processor simply requires replacing the processor/memory elements while all the existing I/O boards remain compatible. This means that all existing STD Bus manufacturer's products - and more importantly, the customers' custom-design I/O boards - are not obsolete. The customer does not have to throw away previous work and spend valuable time recreating a new design to work with a new generation processor. The customer needs only to buy the latest technology to solve the problem while knowing that more processor horsepower is available, should it be required. This gives the engineer a known, predictable, and cost-effective "migration path".

AN0102

STD Bus Directions for the 1990's

Robert A. Burckle
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WinSystems, Inc.

The "New STD Bus"

The STD Bus was originally designed and introduced in 1978 as a small-form factor (4.5 in. x 6.5 in.), highly reliable, low-cost industrial solution for embedded systems. A wealth of I/O for nearly any industrial interface, coupled with IEEE 961 recognition, has made it a well-known industrial standard with over 500,000 installed systems worldwide. The STD Bus is known as the "blue collar bus" because of its industrial orientation and because of its moderate profile when compared to other high-profile buses such as VME or PC Bus.

New STD Bus designs are based on 16- and 32-bit processor-based units such as the 8088, 80188, V40, 80186, 80286, 80386SX, 80486DX/SX and 68030. A new world of applications has evolved with the availability of software productivity tools, operating systems and application programs. Although previous 8-bit CPU designs based on Z80, 6809 and 8085 microprocessors are now maturing, the industrial marketplace demands stability of supply. Consequently, these older designs still are in volume production.

Exciting new enhancements to the STD Bus that include full PC/XT and PC/AT compatibility, 16-bit data transfers, networking on ARCNET and Ethernet, very low cost single board computers, all CMOS extended temperature operation, intelligent slave I/O cards, and high-speed graphics have created a "NEW" STD Bus. This "NEW" bus is alive, well, and very much in a growth mode. A whole new world of embedded operating systems, development tools, utilities, and application software has become available with the DOS compatibility to the extent that the "new" STD Bus is evolving to become the true industrial PC. Major, dynamic new growth is a result of these developments.

The STD Bus is an evolutionary, not revolutionary bus. Rather than abandon its customers as the Exorbus, Versabus, Multibus I, and PC/XT/AT did, STD Bus continues to support a migration path philosophy to permit existing I/O cards designed by vendors and customer alike to coexist on the same bus structure. For example, a 33MHz 80486DX CPU will work well with the same industrial I/O designed for the original 8085s. Thus, STD Bus provides the user with a known, predictable, stable, and cost-effective migration path.

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STD Bus Applications

An incredibly diverse spectrum of embedded and dedicated applications are candidates for STD Bus technology. Some typical applications include:

* Machine Control
* Robotics
* Medical Instruments
* Military
* Process Control
* Printing
* Telecommunications
* Data acquisition
* Weighing/inventory
* Factory Automation
* Inspection/Quality
* Energy Management
* Communications controllers
* Test/Measurement Equipment
* Semiconductor Manufacturing
* Specialized Test fixtures

The STD Bus serves two markets. The first market is for industrial OEMs embedding low cost, non-DOS computers. This is the traditional market that STD continues to serve well.

A second newer market is for systems integrators requiring PC-XT/AT compatibility using the STD Bus platform for reliability and small size. These systems can be embedded into a machine, process, or act as a standalone computer.

WinSystems offers the STD-AT which blends the industry proven STD Bus hardware with MS/PC-DOS, the defacto "Software Bus" for hosting operating systems, utilities, real time executives, development tools, networking, and application specific programs.

The open architecture of the system allows for 8 or 16-bit I/O expansion modules and upgrades to meet new requirements while operating under a DOS environment. Since it is 100% DOS compatible, it can support other operating systems or real-time operating systems. It runs the thousands of software applications and utility packages developed for the PC-XT/AT. Additionally it will run the growing selection of DOS programs targeted at industrial and commercial applications as well. The STD-AT provides the core hardware foundation for industrial control systems.

STD Bus Overview

Unlike other bus types, the STD Bus is specifically designed for process control and industrial applications. Its simple bus interface contributes to lower overall cost and high reliability (typical MTBF of 15 to 25 years, depending on card type).

I/O interfaces are available for pressure and temperature measurement, stepper and large motor control, analog and digital interface, networking, video graphics, and so on. Users who need special I/O functions can easily design and construct their systems, since the STD Bus offers a larger variety of interface cards than any other bus. In fact, many special I/O interfaces that must be custom made for other buses are often off-the-shelf products with the STD Bus. Currently over 150 manufacturers worldwide produce more than 2000

different kinds of STD Bus boards.

The 16-bit STD Bus architecture is quite similar in power and functionality to the AT bus, yet designed specifically for the rigors of industrial applications. The STD Bus is well known for the wealth of real world interface cards that links it to most any industrial sensor. The STD Bus has an active manufacturers group (STDMG) to monitor standards, specifications, and new technical developments to assure orderly evolutionary growth. The PC-XT/AT Bus has been abandoned by its developer while the STD Bus has continued to evolve to meet the new challenges of customer applications by adapting to newer technology for higher performance and more cost-effective solutions. The result is a lasting standard for industrial applications not threatened by obsolescence or abandonment every 5 years.

CMOS STD Bus

A CMOS STD Bus is a design that offers very low power, improved noise immunity, and extended temperature operation. The temperature range is wider than with an NMOS equivalent and the power requirement is much less. Low power means low system operating temperatures, reduced internal heating, no fans, smaller power supplies, and sealed enclosures.

Here today, Here tomorrow

The industry standard IEEE 961 STD Bus hardware standard is very popular because of its small size, rugged design, high quality, and support from multiple vendors worldwide. As an approved IEEE standard, it provides a well documented scheme for combining microprocessor and peripheral devices. Nine out of every 10 major American manufacturers use the STD Bus because of its reliability, flexibility and cost effectiveness. These users include large and small OEMs who use the STD Bus to bring their products to life. Other users include chemical engineers, technicians and scientists who build custom systems with off-the-shelf convenience. Whether users are skilled computer programmers or first-time designers, they know they can rely on the STD Bus for ease-of-use and long-term support from manufacturers.

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AN0103

Do you really need a 32-bit bus?

Much has been written concerning the power of 32-bit processors; however the key factor driving industrial applications is I/O rather than raw CPU power.

In the fast moving market of today, vendors and users of instruments and industrial control systems must be increasingly cost and performance driven to survive. Both must be ever alert to new technologies that can increase the speed and capabilities of control devices and systems, which ultimately lead to improved productivity of factories and plants.

One such technology is that of the 32-bit processor. These devices offer levels of performance previously seen only in expensive mini and mainframe computers. As a result, a move from 16-bit to 32-bit processors often is a wise decision. However, this doesn't mean that this move should be accompanied by a switch from a 16-bit bus to a 32-bit bus. Specifically for industrial applications based upon the STD Bus, a careful analysis of your individual product or project requirements will show that a 8/16-bit bus is still that best route to take.

Processor bandwidth as opposed to I/O bandwidth.

Processor bandwidth is the amount of throughput afforded the processor(s) for code execution and data manipulation, without considering the source of the data or code. For 32-bit single board computers

with large stores of local memory, this throughput can be much greater than needed bus bandwidth.

I/O bandwidth is the communication capability between remote devices and the processor(s). These devices may include other processors and internal subsystems. In multiprocessor systems, bandwidth is required not only for actual useful data, but also for communication between tasks and processes.

Smart I/O boards solve the bandwidth problem.

Some classes of I/O will never require moving beyond 8-bits such as serial, parallel, modems, motor controllers, etc. Despite the migration to a STD Bus 16-bit data path, very few I/O cards have appeared other than memory cards and A/D boards.

WinSystems' research indicates that most STD Bus users will continue to be served adequately by the I/O performance of the 8 and 16-bit STD Bus for industrial and embedded systems applications. Their needs for greater overall system performance can be handled by increases in tightly coupled on board CPU and memory per-

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formance and with distributed intelligent I/O boards.

If your system bandwidth assessment calls for more power than what a single CPU can supply, don't immediately assume that you must upgrade to a 32-bit bus. You may be able to increase bus performance without increasing bandwidth through an intelligent I/O card.

An intelligent I/O card provides parallel processing system with the CPU. The I/O card performs the activity processing and the CPU performs the information processing. Consider the case for high speed communications. A single smart I/O card such as WinSystems' MCM-SBC42 can handle 4 high speed 19.2KB serial lines easily with very little processor intervention. A simple quad serial board connected to a 386/486-based PC-AT would overrun the processor with data, preventing it from doing any additional work.

WinSystems and other STD Bus manufacturers have identified task intensive I/O that require smart I/O and have begun introducing cards to target this application area. For example, WinSystems has the MCM-ENET Ethernet card and MCM-ANET ARCNET card for use with networks. A MCM-DSP32C board is available for applications requiring the power of 32-bit floating point Digital Signal Processor. The MCM-SENSOR is a complete analog subsystem on a single card that performs control, linearization, and conversion for a variety of up to 16 industrial sensors per board. The MCM-SBC42 is a general purpose intelligent I/O card that can execute an number of tasks to off-load processor intensive I/O from the host CPU. An optional communications application

program allows it to act as a 4 channel high speed serial I/O or it can even run industrial control applications under the ROM-DOS embedded operating system. The MCM-488 is an IEEE-488 talker/listener/controller board.

The common feature with all these cards is a standalone onboard CPU that runs independently from the master CPU while maintaining communications across the STD Bus backplane. This approach offers more performance, more control, more modularity, and more system development flexibility at less cost than by using a single CPU with high data rates.

32-bit solutions for the STD Bus

STD32 has been presented as the only solution for 32-bit processing on the STD Bus. However the more popular alternative is the STD Bus using 32-bit CPUs and either 8- or 16-bit I/O. Increased I/O power (if required) is augmented with intelligent I/O cards. 80386, 80486 and 68030-based CPUs are available on the STD Bus that have the main memory on the CPU board with 16-bit data transfers of the CPU card and down the backplane. This concept is the same as used by the ISA bus and is called the "Local" bus. This gives hardware and software access to the powerful 32-bit processors while remaining STD Bus compatible with the I/O cards.

Reasons for considering a 32-bit data bus.

Needed bandwidth. If large blocks of data must be moved across the bus, and there is no other efficient method of reaching or processing this data, a 32-bit bus may

be imperative. With the growing move toward graphical user interfaces comes the need for creating, manipulating, and storing the image data. The latter process can be a voracious consumer of bus bandwidth. Another use of massive data might be a high speed data acquisition system, although the use of DMA may alleviate the need for a wider bus bandwidth. Clearly, this is not the marketplace for the industrial STD Bus.

* *Image.* There is understandably a certain panache to the latest bus structure. This can be seen as a marketing tool, even if the capability is not truly needed.

Making the decision.

Most industrial embedded applications simply don't need the higher performance offered by a 32-bit I/O bus. The I/O is a constraint to system performance not the time constraints presented by the CPU. There are some applications, however, for which I/O performance is critical. Transaction processing, formerly the exclusive domain of multiuser minicomputers (but now migrating over to high-end PCs), may require 500 to 1000 percent more I/O bus performance of todays machines. File servers, multiuser databases, and vision systems will also require more I/O bandwidth as well.

Nonetheless, the industrial user, whether in standalone mode or as a node on a network, will not require much of an increase in I/O performance. Industrial I/O based systems simply do not need and cannot accept 32-bits of data. Industrial I/O is 8- and 16-bit oriented, not 32-bit. The bus is not the performance bottleneck with this hardware for these applications. How fast does one need to turn a relay On and Off? Why make STD Bus users pay additional cost in interface complexity to go to STD-32, when in fact you can get 32-bit performance on the CPU.

High-end 32-bit boards are suited for LAN servers, high-speed graphics, large data storage, and workstation applications. Clearly, this is not the marketplace for the industrial STD Bus.

Conclusion.

WinSystems and other STD Bus companies believe that the very small benefit gained by the 32-bit memory and I/O bus transfers on a 32-bit STD Bus do not warrant the complexity of the ensuing hardware design. We are not opposed to 32-bit CPUs on the STD Bus and in fact offer the MCM-386SX and MCM-486DX/SX. We believe the standard STD Bus architecture supports both high CPU performance and 16-bit industrial I/O at a much reduced cost.

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Important Questions about 32-bit
Processing on the STD Bus

What is the status of a 32-bit STD Bus?

A. WinSystems and other STD Bus manufacturers have designed and are shipping 32-bit 80386, 80486 and 680X0 based CPUs for the STD Bus. It is a natural technical evolution to higher CPU performance because of the application software, real-time operating systems, development tools and high level language support. Since 32-bit CPUs are available, then the key to system performance is the I/O.

Consider the STD Bus marketplace. It serves the industrial embedded computer applications with one of the broadest ranges of industrial I/O functions. Few if any peripherals or controllers need 32-bits. The 32-bit bus wars are interesting but not relevant to most industrial engineers because of the nature of the applications. The vast majority of I/O is only 8-bits with 16-bits appearing only recently. LANs, video, A/D and D/A, keypad input, displays, relays, etc. neither can use nor do not require 32-bit data transfers for I/O operations.

The STD Bus continues to evolve to meet the requirements of the industrial marketplace. The best way to visualize the STD Bus is to think of it as the industrial ISA Bus. The market has clearly shown us that ISA is here to stay. The same claim cannot be made concerning EISA. EISA simply is not being accepted for general purpose, low cost computing applications.

The STD Bus Manufacturers Group (STDMG) has defined and adopted a specification to permit 8- and 16-bit memory and I/O transfers on the backplane. There is no specification for 32-bit transfers.

Do you need a 32-bit Bus for 32-bit CPUs?

A. No. New 32-bit CPU designs have all the main memory on the processor card. Putting all the computing power with its associated memory on a single card rather than on separate cards linked with a bus makes the most sense. With system clocks now at 33 MHz and continuing to increase, the bus becomes a bottleneck rather than a gateway because of the problems associated with high speed data transfers which include increased susceptibility to noise and reflection errors.

The latest trend in the market is to adopt a "local bus" interface for high speed peripheral functions. Such an interface makes it easier to attach high-speed peripheral chips - such as VGA or XGA controllers, SCSI controller, etc. - directly to the CPU bus rather than to a much slower I/O bus. This design trend is very apparent both in new STD and ISA bus designs.

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The STD Bus is a "Blue Collar" Bus that has evolved into a proven 16-bit bus for I/O control rather than a general purpose interconnect scheme of computer architecture. If an application really needs very fast 32-bit data transfers for server or graphics support, then the VME Bus is a better solution with more upside computing power.

What is STD32?

A. STD32 is an alternative form factor EISA bus with 8-bit STD Bus I/O compatibility. It is a more expensive, proprietary bus interconnect scheme that has adopted practices from both the STD Bus and EISA. Both 16- and 32-bit STD32 data transfers are non-standard and incompatible with the STD Bus.

What is the status of the STD Bus?

A. The STD Bus is a very reliable, low cost, ISA-like, industrial I/O channel. With the advent of the high performance/high integration CPUs, it has allowed the STD Bus to evolve into an I/O expansion channel rather than a general purpose computer architecture. As a 16-bit I/O channel, the STD Bus provides one of the broadest ranges of industrial I/O functions including analog, digital, remote I/O subsystems, motion control, networking and PLC connectivity.

The STD Bus is a popular, worldwide standard on a straight path continuing to become the best I/O channel to support integrated, advanced CPU/memory boards. It offers the most cost effective migration path from simple to complex computing support designed specifically for the rigors

of industrial applications. The result is a lasting standard not threatened by obsolescence or abandonment every 5 years.

There is only one STD Bus. It is not trademarked, copyrighted, patented and it doesn't have a number after it.

Does the STD Bus support multiprocessing?

A. Yes. Since 1983, master/slave multiprocessing has been popular on the STD Bus. In the master/slave scheme, loosely coupled processor communicate through dual-ported memory or I/O ports and can never control the bus.

STDMG multiprocessing subcommittee has finalized a scheme to allow up to seven master CPUs on the same bus. Multimaster systems consist of multiple CPU cards, each capable of controlling the bus. Each CPU operates with local onboard memory and has the ability to access the STD Bus for global memory and I/O. Any multimaster CPU may also have local onboard I/O. Data and control parameters are passed between masters through global memory on the bus. A full bus arbitration and priority scheme is implemented to allow this. The bus arbitration is performed by the hardware and does not affect the software.

Who should use the STD Bus?

A. For designers facing pressures of tight budget constraints, lower system costs, and an upward migration path for increased performance while developing and bringing their systems to market quickly, the STD Bus is an excellent choice.

WinSystems' 3/4" Card Cages
Functional Considerations

WinSystems' practice of designing extra value into their products is evident in their card cage and backplane design. Several important features were incorporated to lighten the task of the systems designer.

Signal integrity and processing speed.

New packaging/interconnect requirements which are dictated by the solid structured STD Bus have been answered by WinSystems. Backplanes were carefully designed for minimal crosstalk on signal lines. Ground noise contribution was another important consideration.

WinSystems selected the assembly side of the backplane as the groundplane which reduces noise and crosstalk of signal lines. It also provides a constant characteristic impedance necessary for good transmission line design. The signal lines are narrow to reduce adjacent channel coupling.

Each STD Bus 56-pin connectors has a bypass capacitor for Vcc. Wide ground and power traces are used to improve power distribution. The motherboard has solder pads on a 3 by 3 grid that will accept up to #16 AWG wire for direct wiring or the WinSystems' cable assembly using a standard Molex 9-pin connector. In addition to power and ground, an external battery voltage (VBAT), DC power down signal (DCPD*) inputs are supplied to the backplane through the power connector. Indi-

vidual backplanes are shipped with no power cable for maximum configuration flexibility.

WinSystems uses only UL-approved connectors with gold-plated bifurcated bellows contacts. They are superior to cantilever beam connectors since they provide two beam contacts with two independent spring members and a constant spring tension on the card edge. The contact design enables the connector to have a lower insertion force, a higher withdrawal force and a higher, more consistent normal force. This translates to higher reliability and a better connection since it can absorb load deflection of a card while maintaining sufficient contact force for good electrical connection. Maximum reliability of the bellows connector is assured through superior contact tolerance through environmental stresses including shock, vibration, temperature and humidity variations. Other parameters such as insulation resistance, contact resistance, durability and contact separation force meet all of industry's specifications for reliability.

An optional jumper selectable powerfail and brown-out detection circuit is offered on all the backplanes and card cages. A precision 4.5 volt band gap voltage comparator circuit is used to accurately determine the Vcc voltage statue. Upon detection of an out-of-tolerance condition, a PBRESET* is generated. This is critically impor-

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tant in detecting brown-out or powerfail conditions in remote on unattended applications since a microprocessor will act erratically before it shuts does. Also the reset circuit ensures that the power is a nominal 4.5 volts before executing a power-on-reset.

System modularity and expandability.

Three mounting configurations are available: Rack mount (RM), Table mount (SE), and Wall mount (WM). All cards cages are supplied with a high performance motherboard and a 6" male power plug. The rack mount version uses standard 5.25 inch flanges on all models that allows the card rack to be supported from the front. The table top version allows card racks to be supported be the bottom. The wall mount units are designed to mount to the rear vertical panel of an enclosure.

For distributed processing applications, multiple backplanes can be mounted in a singled card rack. This allows more than one STD Bus controller to reside in a single enclosure.

WinSystems will optionally supply MIL-C-55302/57-type polarized connectors on the backplane instead of card edge connectors. This permits the card cages and backplanes to be used with STD Bus cards that use the pin-and-socket interconnect system. These connectors are superior to DIN-type connectors yet are compatible with WinSystems' XIM series STD Bus cards.

WinSystems will quote specially configured card racks with power supplies. These supplies will mount within the card and generate DC-output voltages from the AC mains.

Rugged, Dependable Construction.

WinSystems' card cages are made from extruded anodized aluminum for the end plates, guide rails and connector rails. This offers both high strength and light weight. The card guides are made from high grade nylon and are self-lubricating, nonconductive, and provide isolation for cards and their components from shock and vibration. The guide tracks have integral card retention tabs to insure a secure fit.

The backplane is mounted to the card cage by riveting the connectors to the metal chassis. The connector housing accepts the insertion and withdrawal forces rather than the backplane PCB which adds reliability to the system. An optional latching bar is available to provide additional card restraint. It fastens at both ends of the card cage and horizontally across the STD Bus card's ejector to hold the cards firmly in place.

Factory Assembly Convenience.

WinSystems ships fully assembled units...not kits. WinSystems' manufacturing expertise and aggressive quality control have produced a respected line of STD Bus products known for their reliability and their tolerance of the rigors of industrial, military and scientific applications. WinSystems demands the highest quality workmanship standards in all of its products. All elements of the product from design, layout, fabrication, testing, and inspection are carefully checked and monitored for conformance to industrial standards.

AN0301

Questions about the ROM-DOS
Embedded Operating System

What is ROM-DOS?

A.   ROM-DOS is an embedded operating system. The task of an operating system is basically to supervise and direct the work of the computer and its associated peripheral devices. ROM-DOS couples the familiarity and wide range of high level languages and compilers of MS-DOS with enhanced facilities for embedded systems applications where the need is to control real data and not just process data.

ROM-DOS is best described by comparisons with MS-DOS. MS-DOS appears to be a single program but is actually a multitude of programs that can be classified into three major parts: Managing of devices, Control of programs, and Command processing. ROM-DOS likewise handles these same tasks. Management of devices involves interaction with the mini-BIOS as well as organizing the disk space, efficient storage of data, and retrieval. Control of programs involves the loading of programs, setting up the system for program execution, and provision for DOS services. Finally Command processing provides direct user interaction with DOS.

ROM-DOS is focused on building DOS functionality optimized for an embedded system, and thus has eliminated many portions of DOS which are "excess baggage". Only the minimum necessary BIOS is required. Among other functions, ROM-DOS supports memory management, MS-DOS compatible file support, time functions, and installable device drivers.

Why Use ROM-DOS?

A.   ROM-DOS is designed especially for programmers designing embedded systems software to run on Intel family CPUs that are not necessarily 100% PC compatible. This allows the user to optimize both hardware and software development for the application.

ROM-DOS provides a DOS level environment that minimizes ROMing restrictions of the application code. Programs can be written in assembly, C, or high level languages such as Pascal or compiled BASIC. It supports standard MS-DOS file structures that greatly simplify data storage and retrieval. Since the programmer is familiar with the PC operating environment, a shorter learning curve will occur. All development can be done on a PC and the code debugged on either on a PC or the target system which completes the project in the shortest time. The application will boot from ROM and run MS-DOS executable (.EXE and .COM) files.

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Which applications need an Embedded Operating System?

A.   ROM-DOS is suitable for a number of rugged applications such as embedded controllers, portable instruments, industrial data acquisition and control, vehicle data logging, security systems, and medical instrumentation which require a diskless operating system. The key features of embedded applications are that they are ROM based, require a standard software interface for common compilers, are diskless (or at least no rotational media), don't require keyboard or video as input devices and are memory efficient.

What hardware is required for ROM-DOS?

A.   ROM-DOS has been optimized to run on WinSystems' Single Board Computers (SBCs) and requires a minimum of hardware which lowers system costs. ROM-DOS uses a minimum amount of memory which also reduce costs. Designed to reside in ROM and use only the necessary amount of RAM during operation, ROM-DOS is frugal on memory space. With all functions included, ROM-DOS takes only 29 KB of ROM, and employs as little as 5KB of RAM when running. MS-DOS would require more than 75KB of ROM which must be loaded into 75KB of RAM during the boot procedure. Memory conservation saves both board space and the cost of memory.

Additionally, ROM-DOS does not require a keyboard, video or rotational media to function which is ideal for embedded control applications. RAM/ROM disks are supported for data storage with the standard DOS file structure.

ROM-DOS is ported to many of WinSystems single boards computers some of which are fully PC compatible and others that are not. ROM-DOS is designed to communicate through a serial channel rather than a standard keyboard and video display. Programs should not attempt to bypass ROM-DOS and manipulate the PC style hardware directly. Embedded systems typically do not have screens or PC style keyboards and programs that do output by writing directly to the screen memory (i.e. QuickBASIC) will not function as desired. This is not to say that the system hardware cannot be manipulated by a custom application program or driver, but only that some canned programs or library routines will not be cognizant of the actual hardware present.

ROM-DOS is currently supported on several WinSystems' boards that are STD Bus, CMOS STD Bus and non-bus based: LPM-SBC40, LPM-SBC41, LPM-SBC53, LPM-286AT, LPM-386SX, MCM-SBC40, MCM-SBC41, MCM-SBC53, MCM-286AT, MCM-386SX, MCM-486DX/SX and SBC-88.

AN0401

Why ARCNET on
the FACTORY FLOOR?

ARCNET, a 2.5 Megabit/sec token passing network, was the first network in worldwide use. In fact, ARCNET was used in commercial service before Ethernet as we know it was standardized. ARCNET is a defacto standard with over 3 million nodes installed. Because of its reliability, ARCNET is used extensively in hospitals and factories.

Long known for its ruggedness and flexibility as a network, ARCNET can make claims that other networks cannot. For instance, an ARCNET network can be physically cut anywhere without destroying the network. This will just make two fully functioning but independent nets. An ARCNET network can be subjected to short circuits and static electricity and still stay up.

Because it is not a baseband like Ethernet and is essentially a modulated carrier, ARCNET does not suffer from ground current problems. An ARCNET does not become "fully loaded" since it equally distributes the available bandwidth among all participants with efficiency increasing with heavier loads!

Other key features include:

ARCNET response is predictable. Factory floor automation applications are often more concerned with the worst-case response time than the data-transmission rate. Because ARCNET allows you to calculate the worst-case response time of the network, you can monitor and control critical machines and processes within guaranteed times. This is critical for command dependent real-time environments that cannot tolerate unknown and occasionally lengthy delays.

ARCNET performs well under heavy loads. As network traffic increases, the token passing ARCNET protocol suffers no performance degradation from CSMA/CD type packet collisions (like Ethernet). Problems with CSMA/CD protocol arise when a network traffic increases to the point where collisions become common and network throughput is drastically degraded due to network contention problems. When such a situation occurs, the data transferred per unit time can drop substantially.

ARCNET is fast. Factory-floor network communications are often dominated by short messages - process monitoring data, for instance, which consist of several bytes and is sent at short, regular intervals. Because of this modest packet size, efficient packet formatting, and relatively simple design, numerous

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independent performance reviews have concluded that ARCNET's throughput is actually equal to (and for some applications, better than) Ethernet or Token Ring networks.

ARCNET is inexpensive. Cabling costs can amount to half the cost of a network, and this is specially true in factory floor applications where cabling runs can be long. ARCNET networks normally use RG-62/U coaxial cable, which cost around $.30 per ft. which is about a third the cost of standard Ethernet cabling.

ARCNET is flexible. It allows either star or bus topology configurations, and can be run over coaxial cable, twisted pair wiring or fiber optic cabling systems (fiber optic cable is particularly attractive on the factory floor, because of its immunity to electrical interference around it).

ARCNET is simple and reliable. Most of the sophisticated circuitry is contained in a VLSI chip set.

ARCNET is easy to install and maintain. Troubleshooting can be accomplished by simply unplugging each network node until the problem area is isolated. In the event of a node failure or damage to the cable itself, the system will reconfigure around the problem and keep on operating.

ARCNET is a mature and proven technology. ARCNET was first introduced by Datapoint Corporation in 1977, and has become a true "de facto" standard, with over 3,000,000 nodes installed worldwide.

ARCNET enjoys the backing by an active support organization, the ARCNET TRADE ASSOCIATION. Current ATA activities include the review and adoption of a universal protocol standard, the enhancement of ARCNET's structure to address "the year 2000 and beyond" network needs and a variety of educational and technical support programs for ARCNET designers, integrators, installers, and network users.

AN0402

What is MNP?

MNP is an acronym for Microcom Networking Protocol, which was devised to provide a means for error detection and correction of high speed modem transmission. Poor telephone line connections or noisy lines can cause erroneous data, but this protocol has the ability to detect and correct these errors.

MNP has a number of different transmission schemes, each having certain levels of error correction and most having the same or higher throughput (actual data transmitted) than a standard 2400 bps modem.

When a WinSystems' MNP compatible modem tries to initiate an MNP connection, it will transmit a link request containing information such as service class, maximum user data size and maximum flow control window size. If the receiving modem responds with a link acknowledgement, MNP will be established at the highest class both modems are capable of performing. If no link acknowledgment is received, the modem will establish a non-MNP (normal) connection when in auto reliable mode.

Data packets are sent along with a 16 bit Cyclic Redundancy Check (CRC) character. If the received CRC bit doesn't match the locally computed one, a negative acknowledgment is sent and the remote modem will retransmit the packet. This method not only allows for error detection, but, with the retransmission of the data, will actually correct the error.

MNP connections can only be obtained with another modem capable of and set to use MNP. All of the functions of MNP are transparent to the user, once the parameters for its use are setup using the "AT" commands.

The WinSystems' MCM-2400MNP incorporates all the standard and extended "AT" commands, plus additional "AT" commands for controlling the features of MNP.

MNP Service Classes:

Class 1: MNP Class 1 uses an asynchronous, byte-oriented format. Standard byte framing techniques are used (start and stop bits) and transmission is half duplex.

*Class 2: MNP Class 2 uses an asynchronous, byte-oriented format. Standard byte framing techniques are used (start and stop bits) and transmission is full duplex.

*Class 3: MNP Class uses a synchronous, bit-oriented format. Standard byte framing techniques are removed, thereby increasing throughput by 20% (8 bits transmitted per byte instead of 10).

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With a 20% reduction in actual bits transmitted, overall throughput is increased to approximately 2600 bps.

*Class 4: MNP Class 4 uses more efficient framing techniques and allows for larger data block transmission. Data block size is adjusted larger for high quality connections and smaller for poorer lines. This technique reduces the number of retransmissions and maximizes transfer rate on varying quality lines.

The automatic adaptiveness of this class can maximize data transmission at rates up to 2900 bps.

*Class 5: MNP Class 5 includes the features of Class 4, plus adds data compression techniques. Data is compressed using a real-time adaptive algorithm. Both downloaded and interactive, real-time data is compressed.

This class can realize up to a 200% increase in throughput, producing an actual data transfer rate of up to 4800 bps.

* *Overall throughput greater than 2400 bps can only be realized when the communication between the WinSystems' MCM-2400MNP modem and the terminal equipment (DTE) is greater than 2400 bps (up to a maximum speed of 9600 bps) and flow control is used.*

28/32 PIN JEDEC Footprint Standard for SRAMs

4M BITS (512k x 8)

2M BITS (256k x 8)

1M BIT (128k x 8)

512k BITS (64k x 8)

32-PIN DIP
0.6 IN. WIDE
TOP VIEW

←A18	NC	NC		1			32		Vcc		→
←		A16		2			31		A15		→
←			A14	3	1	28	30	Vcc	Vcc	A17	→
←			A12	4	2	27	29	WR			→
←			A7	5	3	26	28	A13			→
←			A6	6	4	25	27	A8			→
←			A5	7	5	24	26	A9			→
←			A4	8	6	23	25	A11			→
←			A3	9	7	22	24	OE/VPP	OE		→
←			A2	10	8	21	23	A10			→
←			A1	11	9	20	22	CE			→
←			A0	12	10	19	21	DQ7			→
←			DQ0	13	11	18	20	DQ6			→
←			DQ1	14	12	17	19	DQ5			→
←			DQ2	15	13	16	18	DQ4			→
←			Vss	16	14	15	17	DQ3			→

10
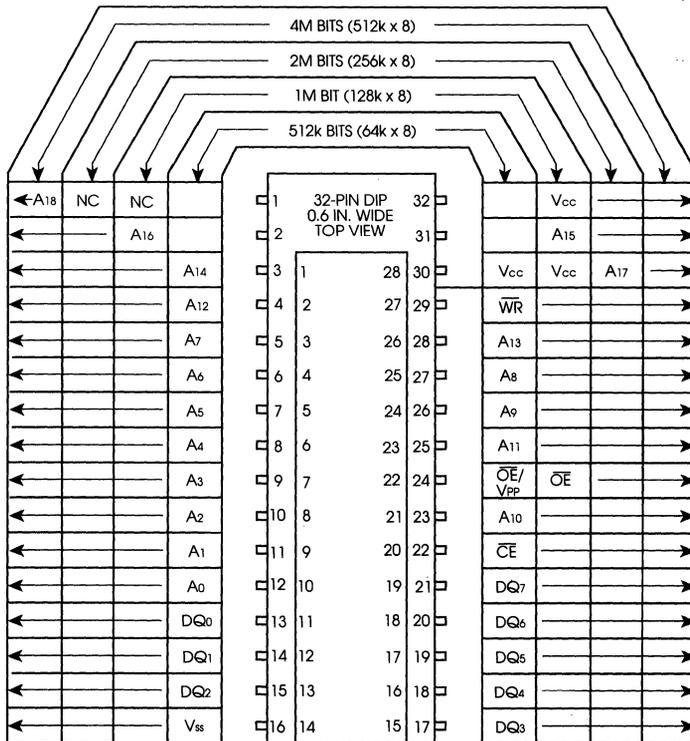
EPROM Memory Socket Configuration

8M BITS (102k x 8)	4M BITS (512k x 8)	2M BITS (256k x 8)	1M BIT (128k x 8)	512k BITS (64k x 8)	Pin	28-pin	DIP pin	DIP pin	28-pin	Pin	512k BITS (64k x 8)	1M BIT (128k x 8)	2M BITS (256k x 8)	4M BITS (512k x 8)	8M BITS (102k x 8)
A_{19}			V_{PP}		1		32	V_{CC}								
	A_{16}				2		31	$\overline{PGM}$	A_{18}							
		A_{15}			3	1	28	30	V_{CC}	NC	A_{17}					
		A_{12}			4	2	27	29	A_{14}							
		A_{7}			5	3	26	28	A_{13}							
		A_{6}			6	4	25	27	A_{8}							
		A_{5}			7	5	24	26	A_{9}							
		A_{4}			8	6	23	25	A_{11}							
		A_{3}			9	7	22	24	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}/V_{PP}$					
		A_{2}			10	8	21	23	A_{10}							
		A_{1}			11	9	20	22	$\overline{CE}$							
		A_{0}			12	10	19	21	DQ_{7}							
		DQ_{0}			13	11	18	20	DQ_{6}							
		DQ_{1}			14	12	17	19	DQ_{5}							
		DQ_{2}			15	13	16	18	DQ_{4}							
		V_{SS}			16	14	15	17	DQ_{3}							

32-PIN DIP 0.6 IN. WIDE TOP VIEW

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About the PC/104 Standard

THE NEED FOR AN EMBEDDED-PC STANDARD

Over the past decade, the PC architecture has become an accepted plat-
form for far more than desktop applications. Dedicated, rather than
"personal", applications for PCs are everywhere! PCs are used as con-
trollers within vending machines, laboratory instruments, communications
devices, and medical equipment, to name a few examples.

By standardizing hardware and software around the broadly supported
PC architecture, embedded system designers can save substantial devel-
opment costs, risks, and time. This means faster time-to-market and
hitting critical market windows with timely product introductions. Anoth-
er important advantage of using the PC architecture is that its widely
available hardware and software are significantly more economical than
traditional bus architectures such as VME and Multibus. This means
lower product costs.

For these reasons, companies that embed microcomputers as controllers
within their products seek ways to reap the benefits of using the PC archi-
tecture. However, the standard PC bus form-factor (12.4" x 4.8") and its
associated card cages and backplanes are too bulky (and expensive) for
most embedded control applications.

The only practical way to embed the PC architecture in space- and power-
sensitive applications has been to design a PC — chip-by-chip — directly
into the product. But this runs counter to the growing trend away from
"reinventing the wheel." Wherever possible, top management now en-
courages out-sourcing of components and technologies, to reduce devel-
opment costs and accelerate product design cycles.

A need therefore arose for a more compact implementation of the PC
bus, satisfying the reduced space and power constraints of embedded
control applications. Yet these goals must be realized without sacrificing
full hardware and software compatibility with the popular PC bus stan-
dard. This would allow the PC's hardware, software, development tools,
and system design knowledge to be fully leveraged.

PC/104 was developed in response to this need. It offers full architecture, hardware, and software compatibility with the PC bus, but in ultra-compact (3.6" x 3.8"), stackable modules. PC/104 is ideally suited to the unique requirements of embedded control applications.

A PROPOSED EXTENSION TO IEEE-P996

PC/104 is being advanced as a proposed Appendix to the IEEE-P996 draft specification, with the title: "PC/104 — A Compact Embedded-PC Standard." The name "PC/104" comes from the total number of bus connector pins (64 pins on P1, plus 40 pins on P2).

Products compatible with the proposed PC/104 standard are already offered by over a dozen companies. Like the IEEE-P996 PC bus specification itself, PC104 is therefore an expression of an existing "de facto" standard, rather than a theoretical bus developed by committee.

The major differences from the existing IEEE-P996 (PC bus) standard are:

- **Extremely small form-factor.** 3.6 by 3.8 inches (Figure 1).

- **Unique self-stacking bus.** Eliminates the cost and bulk of back-planes and card cages (Figure 2).

- **Relaxed bus drive requirement (6 mA).** Lowers power consumption (typically 1-2 Watts) and reduces component count.

TWO WAYS TO USE PC/104 MODULES

Although configuration and application possibilities with PC/104 modules are practically limitless, there are two basic ways they tend to be used in embedded system designs.

Standalone module stacks. As shown in Figure 2, PC/104 modules are self-stacking. In this approach, the modules are used like ultra-compact bus boards, but without the need for backplanes or card cages. Stacked modules are spaced .6 inches apart when installed. The three-module stack shown in Figure 2 measures just 3.6 by 3.8 by 2 inches. Companies incorporating PC/104 module stacks within their products frequently create one or more of their own "application-specific" PC/104 modules.
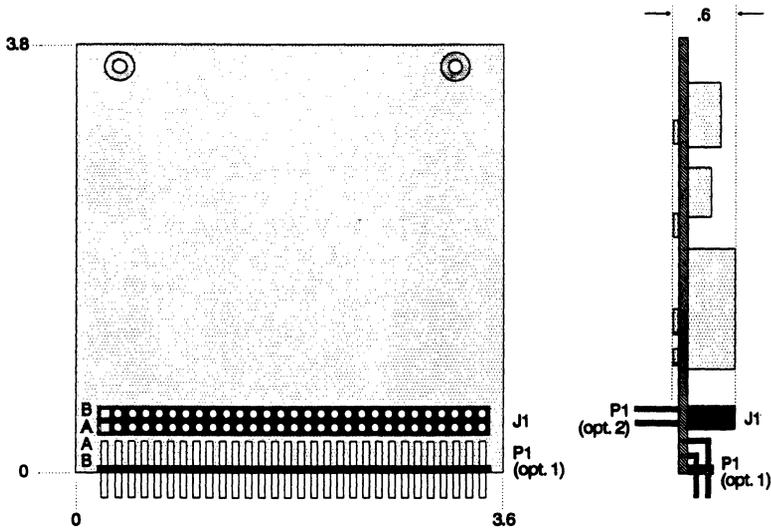
Figure 1. Basic Mechanical Dimensions (8-bit Version)
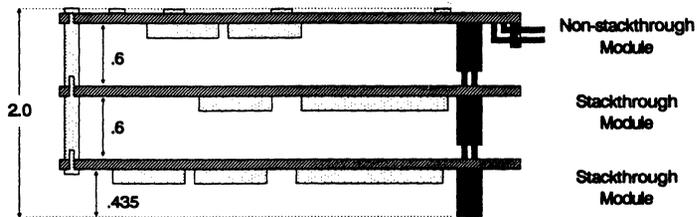
Figure 2. Standalone Module Stacks

Component-like applications. Another common way to use PC/104 modules is illustrated in Figure 3. In this type of application, the modules function as highly integrated components, plugged into custom carrier boards which contain application-specific interfaces and logic. The modules' self-stacking capability can be useful for installing multiple modules in one location. This facilitates future product upgrades or options, and allows temporary addition of modules during system debug or test.

POWER CONNECTOR — REAR PANEL CONNECTORS —

POWER SUPPLY COMPONENTS

PC/104 EXPANSION MODULE OPTION

SYSTEM ENCLOSURE

APPLICATION - SPECIFIC CARRIER BOARD

PC/104 CPU MODULE

PC/104 EXPANSION MODULE OPTION

— FRONT PANEL CONTROLS —
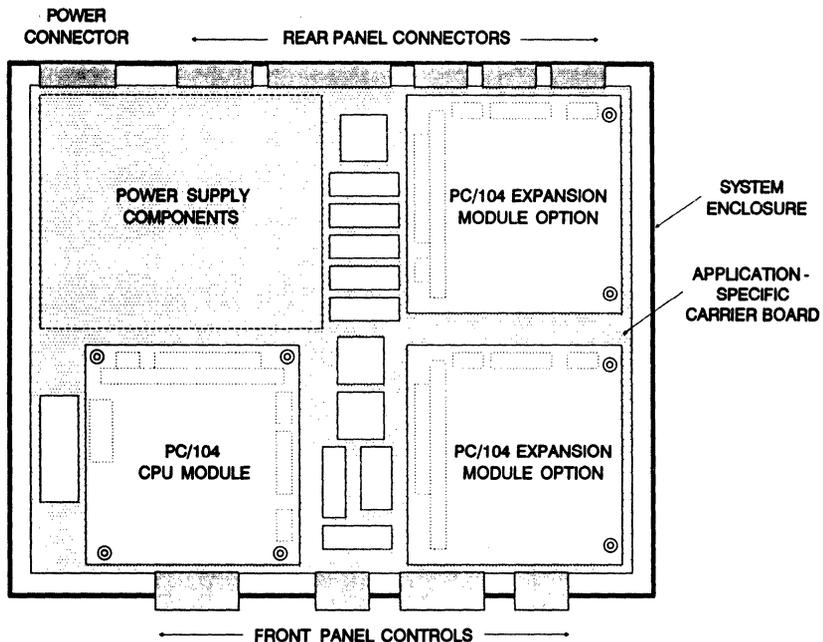
Figure 3. Component-like Applications

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