MAINTENANCE MANUAL

NPC 764

LOGIC ANALYSIS SYSTEM

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SAFETY PRECAUTIONS

The notations shown in the box below are used in this manual to draw the attention of the user to particular items within the text. Personnel hazards (WARNING) exist as noted in the specific operations described in this manual. Equipment damage potential (CAUTION) exists in the following cases: Mechanical damage as noted in specific operations described in this manual. Electrical damage when power cord is connected and/or power is applied as noted in speciic procedures within this manual.

WARNING

A WARNING NOTATION IS USED TO DESCRIBE AN OPERATING OR MAINTENANCE PROCEDURE, PRACTICE, CONDITION OR STATEMENT, WHICH, IF NOT STRICTLY OBSERVED, COULD RESULT IN INJURY TO, OR DEATH OF PERSONNEL.

CAUTION

A CAUTION NOTATION IS USED TO DESCRIBE AN OPERATING OR MAINTENANCE PROCEDURE, PRACTICE, CONDITION OR STATEMENT, WHICH, IF NOT STRICTLY OBSERVED, COULD RESULT IN DAMAGE TO, OR DESTRUCTION OF EQUIPMENT OR LOSS OF EQUIPMENT EFFECTIVENESS.

NOTE

A NOTE IS USED TO DESCRIBE AN ESSENTIAL OPERATING OR MAINTENANCE PROCEDURE, CONDITION OR STATEMENT WHICH MUST BE HIGHLIGHTED.

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INTRODUCTION

1.1 MANUAL CONTENTS

This manual contains technical information useful for the maintenance and repair of the Nicolet Paratronics Corporation NPC 764 Logic Analyzer. Each section of this manual contains the pertinent schematics, technical description and parts list. The manual is arranged as follows:

Section I - Introduction

Includes a general description of the NPC 764 including principles of operation, block diagram description, and performance characteristics. A brief description of the performance checks is also given.

Section II - Self Tests

Description of automatic and keyboard self-tests. In addition, a step-by-step illustration of self-tests performed with the Logic Analyzer Test Card is provided.

Section III - Chassis

Mainframe, power supply, PCB arrangement and motherboard layout.

Section IV - Keyboard

Description of keyboard, operation and circuitry.

Section V - Display Module

Maintenance details of the Display module contained in the NPC 764.

Section VI - Processor/Video

Microprocessor, memory, video display circuitry, and IEEE-488 interface details including a block diagram.

Section VII - State Control Board

Block diagram, schematic and theory of operation for the state analyzer control.

Section VIII - State Memory Boards

Block diagram, schematic and theory of operation for the State Memory Board.

Section IX - Timing Control Board

Block diagram, schematics and theory of operation for the Timing Control Board.

Section X - Timing Memory Boards

Block diagram, schematics and theory of operation for the two Timing Memory Boards.

Section XI - CT/SA Board

Description of the optional Counter-Timer and Signature Analyzer Plug-in Board.

Section XII - Waveform Board

Schematic and theory of operation for the optional Waveform Board.

Section XIII - Disk Drive, Controller, Dynamic RAM

Description, operation and circuitry of the Disk Drive/Controller/Dynamic RAM.

Section XIV - Input Probes

Describes the three probes used with the NPC 764. The Model 80 probe is used to apply input signals to the timing analyzer. The Model 90 probe is used for CT/SA readings of external signals and to apply input signals to the CT/SA Board or Waveform Board. The Model 51A probe is used to apply signals to the state section.

Section XV - Signal/Connection Tables

Contains complete wiring and pin assignments for the NPC 764 in tabular form.

Section XVI - Glossary

A glossary of terms used in this manual and logic analysis in general.

1.2 NPC 764 OPERATION

Instrument operation is covered in detail in the NPC 764 Operator's Manual shipped with each unit. Additional copies are available from Nicolet Paratronics.

The Operator's Manual contains several sections that may be useful from a maintenance point of view. These sections should be reviewed for a greater understanding of the product operation. The sections on KEYBOARD, MENUS AND DISPLAYS and REFERENCE should be particularly helpful. The section on REFERENCE contains solutions to many common operating problems.

In general, the maintenance information in this manual can be used without reference to the operating information in the Operator's Manual.

1.3 BLOCK DIAGRAM DESCRIPTION

Refer to Figure 1-1. The NPC 764 is interconnected by a 60-wire system bus that forms an I/O path for all the functional modules.

The CPU incorporates an Intel 8085 microprocessor that utilizes up to 48K bytes of ROM, and 48K bytes of RAM. The processor controls system operation including data collection, keyboard scanning, display and interfacing.

The **State Input** circuitry consists of Model 51A probes connected to **State Memories** A, B and C. Data is latched into these memories at rates up to 12.5 MHz. The data is continuously examined by the state control trigger detectors. When the data meets user-selected trigger conditions, it causes a **Main Memory** data collection.

Timing Input data from two Model 80 probes is fed to data comparators on **Timing Memory** Boards A and B. The data is sent from the probes in 16-bit parallel data streams. Data is continuously latched into these comparators. The data is sent from the comparators to the **Main Memory**, at user-selected clock rates up to 100 MHz. The comparators continuously compare the incoming data with arm and trigger words entered from the keyboard at set-up time. When arm and trigger conditions are met, a snapshot of 1000 words of current data is locked into the Main Memory. This snapshot subsequently may be displayed and examined. The 1000-word snapshot also can be divided between pre-trigger and post-trigger words as selected from the keyboard at set-up time.

The Main Memory retains the last data entered until a new set of data is loaded. The new set of data is loaded using the COLLECT (soft) key. Also, the contents of the Main Memory can be transferred to the **Auxiliary Memory**. There it may be retained for comparison with subsequent Main Memory data collection. The contents of either the Main or Auxiliary Memory can be displayed under keyboard control.

The **CRT Display** is a raster scan unit with a 9-inch (23 cm) diagonal screen. The driving circuitry resides on the CPU board. A composite video output on the rear panel of the NPC 764 allows use of a large-screen monitor if desired.

The **Keyboard** provides user access to the NPC 764 parameter/ measurement set, menus, display formats, trigger modes and interfaces. The keys are a combination of direct entry, menu selection and software-defined "soft" keys.

An **RS-232 Interface** is provided as standard on the NPC 764. This interface permits output of display-formatted data to a printer or other peripheral. The NPC 764 also is provided as standard with an instrument-bus **IEEE-488 Interface**. That allows the NPC 764 to be talker, listener or controller.

Optional measurement features are added to the NPC 764 by adding the CT/SA (Counter-Timer/Signature Analyzer) PCB to the unit.

The Waveform Analyzer board can optionally be included in the NPC 764 to obtain added analog measurement capabilities.

Mnemonic Disassembly accessories are available for a variety of microprocessors. Disassembly operates by loading programs from disk and collecting data using dedicated probes.

1.4 DETAILED OPERATION

The NPC 764 analyzer collects data under specified conditions and stores the data in memory for detailed examination.

To start data collection, the user presses COLLECT (soft key) on the keyboard. When the trigger conditions are met, data collection is automatically stopped by the analyzer. Alternately, selection may be made for data collection to continue after the trigger event. The user must specify the amount of post-trigger data to be collected. Once data collection has stopped, the data can be displayed in various formats for convenient analysis.

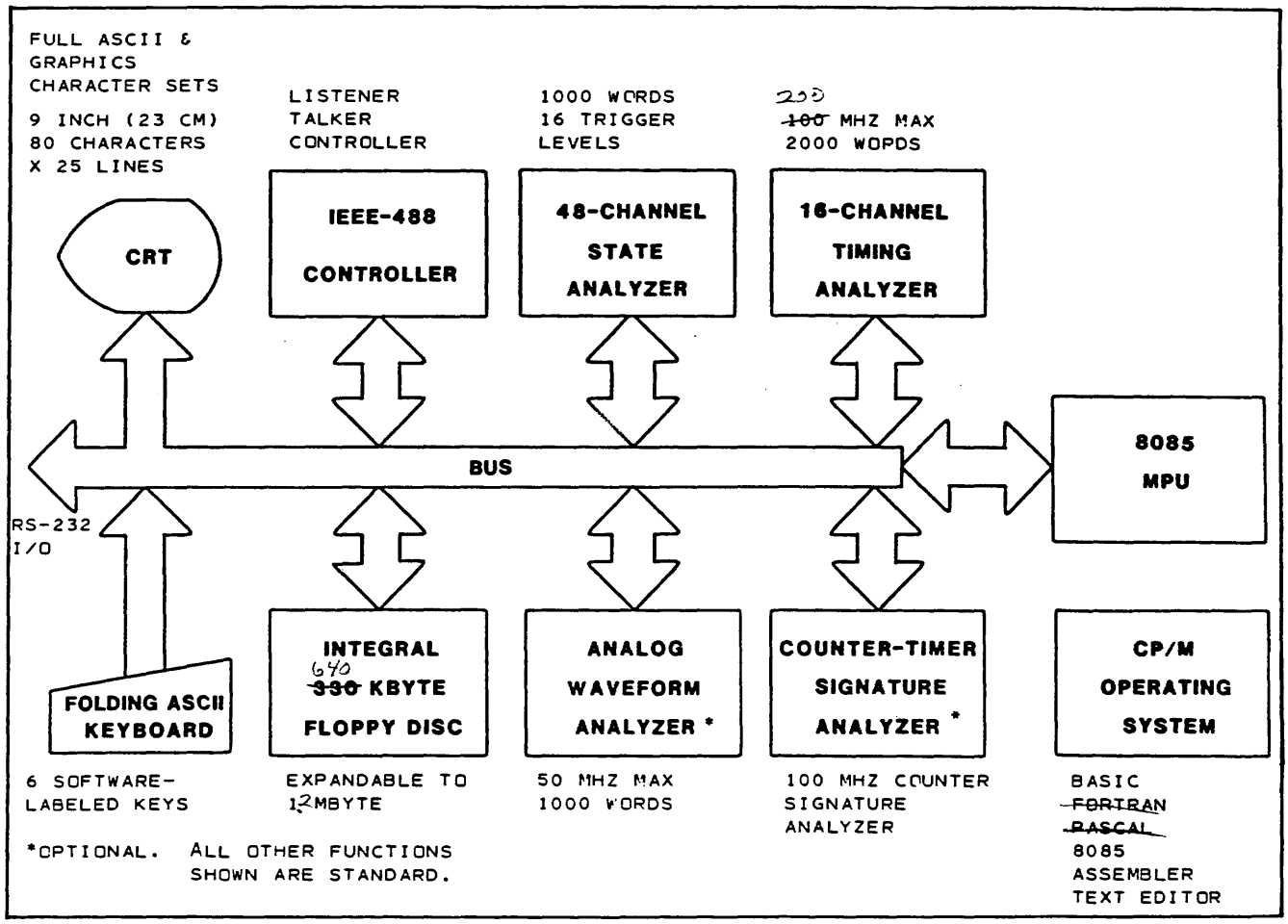


Figure 1-1 NPC-764 Simplified Block Diagram

SELF TESTS

SECTION 2: SELF TESTS

SECTION II
SELF TESTS

2.1 INTRODUCTION

The NPC 764 provides three types of self-tests that can be useful in assessing the condition of the instrument. First, an automatic self-test is performed every time power is turned on. Second, there are self-tests that can be performed with the Logic Analyzer Test Card, NPC part number 143-0046-002. Third, there are self-tests that can be performed using a system disk.

2.2 AUTOMATIC SELF TEST

The automatic self-test is performed during the first two seconds each time power is applied to the analyzer. This test goes through a set of performance checks of the NPC 764 memories and other subsystems. The test reads the setting of the power-line frequency selector switch, S1-1, on the Processor Board. The CRT vertical SYNC frequency is set to a matching 50 or 60 Hz. Although this self-test does not provide a 100% check, it offers a high confidence level that the analyzer is operating properly.

Successful completion of the test is announced by a short beep followed by a display of the Configuration Menu. If the test is not successful, there will be no beep.

2.2.1 PROCESSOR TEST

The 764 system software contains a test that automatically checks the processor board. To run this test proceed as follows:

a. Turn the 764 OFF.

b. Short pins 2 and 3 of the RS-232 connector, located on the back panel of the unit. (See Figure 2-1).

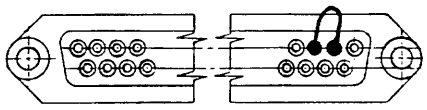


Figure 2-1 Connector Jumper

c. Turn the 764 on.

d. Press the BREAK key.

e. Verify that the display appears as shown in Figure 2-2.

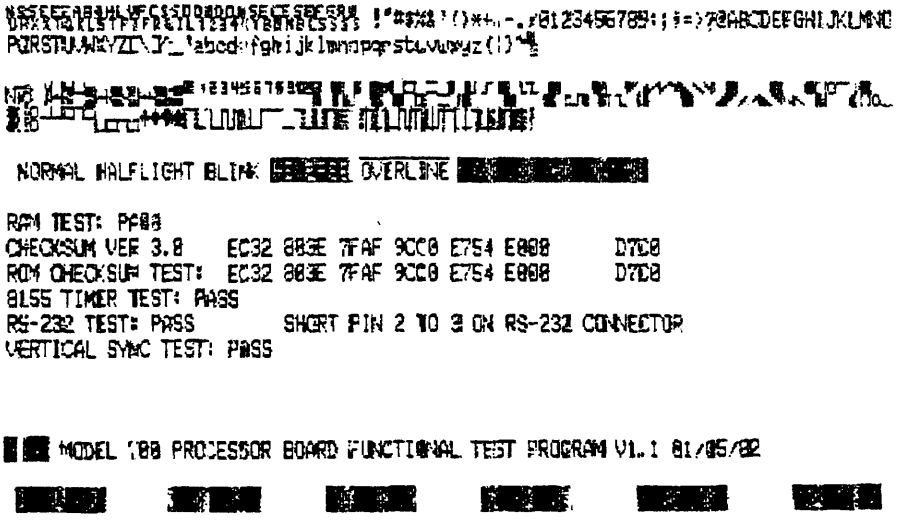


Figure 2-2 Screen

To abort the test hold down the RESET key for three seconds and press the ESCape key.

2.2.2 SYSTEM DISK SELF-TESTS

Each CP/M system disk contains three tests. They are as follows: The RAM test, the keyboard test and the disk drive test. To run any of these tests, insert a system disk into drive A and press the ESCape key. The CRT display will then look like Figure 2-3.

```
NICOLET-PARATRONICS 780K 48K CPM 2.2 OF 9-3-81

A)
```

Figure 2-3 Screen

To run the RAM test type RAMTEST <return>. This test writes a walking 1's pattern into the dynamic RAM, reads the data back and indicates any errors. The test runs continuously, and takes about 20 minutes for each pass. The total number of errors and the number of test runs is indicated on the screen. See Figure 2-4. To abort the test, press the RESET key. To reboot, press the ESCape key.

```
48K DYNAMIC RAM TEST PROGRAM 08/17/81
WALKING 1'S TEST:  1'S ADDR: 8898

TESTING ADDRESS:    ----
LAST FAILED ADDRESS: ---- EXPECTED: -- READ: --
TOTAL FAILURES:      0
PASSES COMPLETED:    0
```

Figure 2-4 Screen

To run the keyboard test type KYBDTEST <return>. Observe the keyboard display on the CRT. See Figure 2-5.

To test the keyboard strike each key displayed on the screen once. As each key is struck, it will disappear from the screen.

DISK TEST

To test a drive, boot up the CP/M system disk by pressing ESCape (if not already booted up). Enter DSK5TEST <return> on the keyboard. Refer to Figure 2-6. You will then be asked to select a drive to be tested. If you have only one drive, enter the letter "A". The 764 will respond with the question "How many retrys?" Enter a number between zero and nine. You will then be asked for a full track seek. If you enter "Y", the read/write head will restore to track 0 after each track is read. If you enter "N", each track will be read consecutively. After selecting "Y" or "N", strike RETURN to start the test. The test will take between five and ten minutes to complete depending on the parameters you have selected.

2.3 BASIC TESTS WITH THE LOGIC ANALYZER TEST CARD

NPC Logic Analyzer Test Card, Part Number 143-0046-002, provides a comprehensive functionals test of the NPC 764 Logic Analysis system. A suitable procedure is given in the following paragraphs. All

```
F1  F2  F3  F4  F5  F6  LABELS

ESC 1 2 3 4 5 6 7 8 9 0 - = ^ BS BK
 TAB q w e r t y u i o p [ ] LF DEL
    a s d f g h j k l ; ' ( RETURN
S1    z x c v b n m , . /        S2
            SPACE

UNLOCK CAPS LOCK KEY

PRESS EACH KEY ON KEYBOARD. ALL KEY LABELS SHOULD DISSAPPEAR
```

Figure 2-5 Screen

```
NICOLET-PARATRONICS 7008 48K CPM 2.2 OF 9-3-81

A)DSK5TEST

TARBELL DISK DIAGNOSTIC
STANDARD VERSION 1.8
77 TRACKS   16 SECTORS

SELECT DRIVE. (A/B/C/D) A
HOW MANY RETRYS? (0-9) 0
SELECT STEP RATE. (S/M/F)
FULL TRACK SEEK? (Y/N) N
TO START TEST TYPE RETURN.

0000 READ ERRORS DETECTED.

REPEAT TEST? (Y/N/C=CONTINUOUS) C
```

Figure 2-6 Screen

steps necessary for a comprehensive evaluation are presented. This procedure assumes the user has some familiarity with the operation of the NPC 764. If necessary, refer to the Operator's Manual.

2.3.1 PRELIMINARY TESTS

Perform the following tests to confirm operation at the most primitive level.

a. Disconnect the power cord from the analyzer. The power fuse and voltage cord must be visually inspected to verify correct installation for the current application. Refer to the discussion of the Mains Module in the Chassis section for more information. Reconnect the power cord.

b. Check the setting of SW1-1 on the Processor Board. The video vertical sync frequency is set to match the power mains frequency. ON = 60 Hz, OFF = 50 Hz.

2.3.2 TEST CARD DESCRIPTION

The Logic Analyzer Test Card consists of two 8-bit CMOS counters (A and B), a clock, and simple decoding logic. Refer to Figure 2-7 and schematic #127-0046-001 at the end

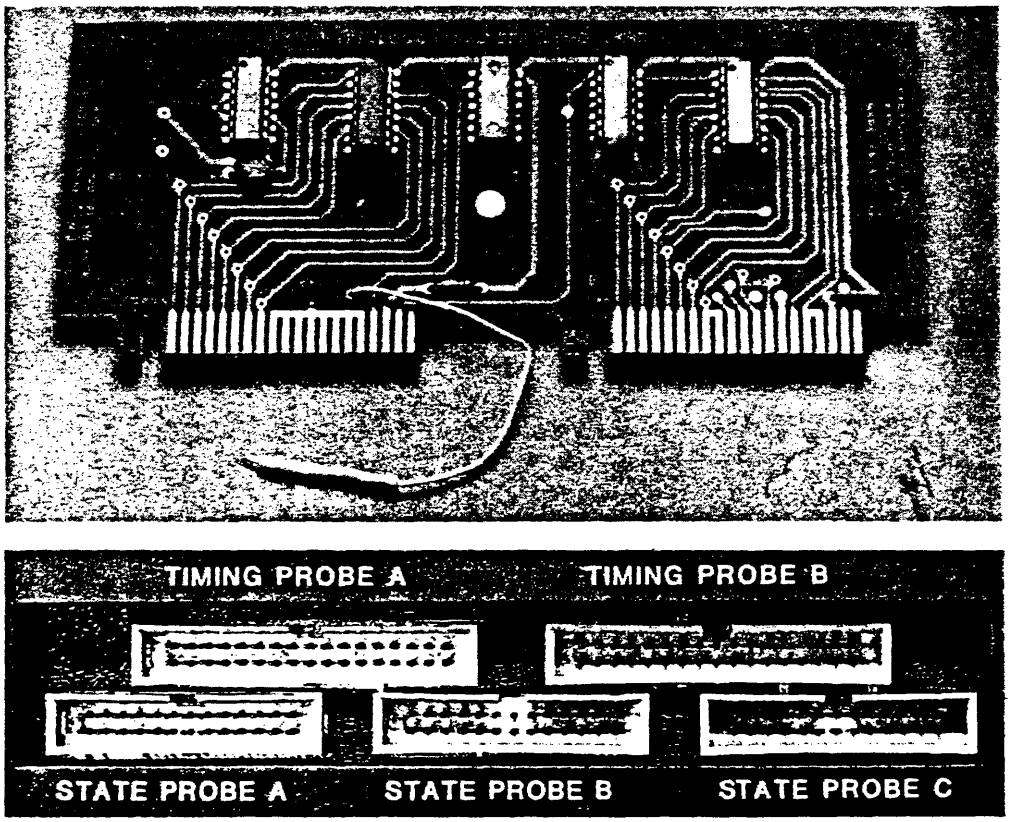


Figure 2-7 Logic Analyzer Test Card and Probe Connectors

of this section. Each CMOS counter normally counts from $(00)_{HEX}$ to $(FF)_{HEX}$. When the A counter reaches $(40)_{HEX}$, the decode logic resets the B counter to $(00)_{HEX}$.

The A channel connector is wired with the eight least significant bits corresponding directly to the output of the A counter. The eight most significant bits are tied to ground. Thus, the A channel provides a 16-bit word to the analyzer that sequences from $(0000)_{HEX}$ to $(00FF)_{HEX}$.

The B channel connector is wired so that the 16 output bits toggle nonsequentially. A typical binary count sequence at the B channel connector is as follows:

COUNT	BINARY PATTERN*	HEX PATTERN
0	00000000 00000000	00 00
1	10000000 00000001	80 01
2	01000000 00000010	40 02
3	11000000 00000011	C0 03
.	. .	. .
.	. .	. .
.	. .	. .
15	11110000 00001111	F0 0F

Note the difference in pin-outs between the 16-channel state probes and the 8-channel timing probes. Due to the difference, this exact pattern will be displayed on the NPC 764 only when using the state probe.

Power to the test card is supplied by the +5 V output at either probe connector.

The A counter is generally used as a signal source for the A state or timing probe. The B counter output feeds the B state or timing probe. The third 16-channel state probe (C) is not normally connected to the test card.

2.3.3 SET-UP

Before using the test card, proceed as follows:

a. Connect the A and B state probe cables to the NPC 764. LEAVE THE C PROBE UNCONNECTED.

b. Connect the A probe to the left-hand connector of the test card and the B probe to the right-hand connector. Set both probes for TRUE and TTL operation.

c. Turn the NPC 764 power switch ON and wait for the self-test beep and Configuration Menu. Refer to Figure 2-8.

2.3.4 BASIC STATE TESTS

To test the basic state analysis capabilities of the NPC 764 do the following:

a. Select a menu.

b. Enter in a trigger word.

c. Press the COLLECT(F6) key.

Captured data can be then formatted in a variety of ways.

The six soft function keys are labeled F1 to F6 from left to right. They are identified by labels on the bottom line of the CRT. These labels differ from menu to menu, as selected with the SEL DOWN or SEL UP keys.

Examples using these keys are given below:

a. To select the 48-CHANNEL STATE mode, press the STATE(F1) key to call the state menu illustrated in Figure 2-9.

b. The 48-channel state menu should be set up with the default values in all fields except the trigger word field. Advance the blinking cursor to the trigger stack field, level 0, with the NEXT(F2) key. Press the H key to format this field for a hexadecimal trigger word. Now enter the following trigger word: 0040. Observe the field at the lower right of the CRT. Other formats can be selected from this field using the indicated keys.

c. Press COLLECT(F6) to take a data collection beginning at 0040. Then

```
NE   NICOLET PARATRONICS 764 CONFIGURATION  VER 4.0

 1 - 48 CHNL STATE
 2 - 16 CHNL TIMING
 3 - 48 CHNL STATE/16 CHNL TIMING
 4 - 8 CHNL TIMING (100MHZ 2000 WORD)
 5 - 48 CHNL STATE/8 CHNL TIMING
 6 - 8 CHNL TIMING GLITCH
 7 - 48 CHNL STATE/8 CHNL GLITCH
 8 - WAVEFORM RECORDER
 9 - 48 CHNL STATE/WAVEFORM
10 - COUNTER/TIMER
11 - SIGNATURE ANALYZER
12 - PI 70 SERIAL PROBE TRANSMIT

ESC - DISK OPERATING SYSTEM

BREAK - PROCESSOR SELF-TEST

I - I/O CONFIGURATION MENU
```

```
STATE                                  SEL DOWN     SEL UP     COLLECT
```

Figure 2-8 Configuration Menu

```
                    48 CHANNEL STATE MENU

FORMAT:  AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA
          A HEX
CLK SEL:  A PRB: ∫  B PRB: A  C PRB: A   QUALIFIERS: -ABBBCC EL
CLK QUAL: OFF
     OR  OFF
  PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART:  OFF
TRIGGER:
 0       00 40 XX XX XX XX -XXXXXX XX
 END


                                                          H - HEX
                                                          O - OCTAL
                                                          Z - DEC
                                                          N - BINARY
                                                          Y - ASCII
    31 - DATA DISPLAY                                     U - USER

PREVIOUS       NEXT                              CONFIG     COLLECT
```

Figure 2-9 48 Channel State Screen

press the LABELS key. Reformat the display in octal, decimal, binary and ASCII by pressing the O, Z, N, and Y keys in turn. Press the H key for the hexadecimal format. Refer to Figure 2-10.

d. Scroll the display up and down by holding the SCRL UP(F2) key, then the SCRL DOWN(F1) key. Locate the end of the data collection (word +999) by pressing the LOCATE(F3) key then the E key. Then locate word +101 by pressing LOCATE(F3) followed by +101. Finish with the trigger word at the top of the CRT by pressing the LOCATE(F3) and T keys.

2.3.4.1 Saving Data

To test the SAVE mode, press the LABELS key in the top row. Perform the SAVE function by pressing the S key. This action causes the entire data collection, the test codes (SIG), and the menu parameters to be stored in the NPC 764 auxiliary RAM memory. Press the MEMSEL(M) key to cause the auxiliary memory to be displayed. Press M again to return the main memory to the screen.

2.3.4.2 HOLD≠ MODE

The HOLD≠ mode is used to detect and isolate intermittent faults. Press the # key (SHIFT and 3) to activate the HOLD≠ mode. Note that the flashing status messages indicate the analyzer is automatically collecting and comparing main and auxiliary data.

Hold the shorting wire on pad 5 on the right-hand side (B side) of the test card. Note that the flashing status message now reads HOLDING, and data are displayed. Remove the shorting wire from pad 5.

Press the M key to compare main and auxiliary test codes. Notice that one of the main memory test codes differs from the corresponding auxiliary memory test code. This indicates that somewhere in the new data collection, one or more bits differ

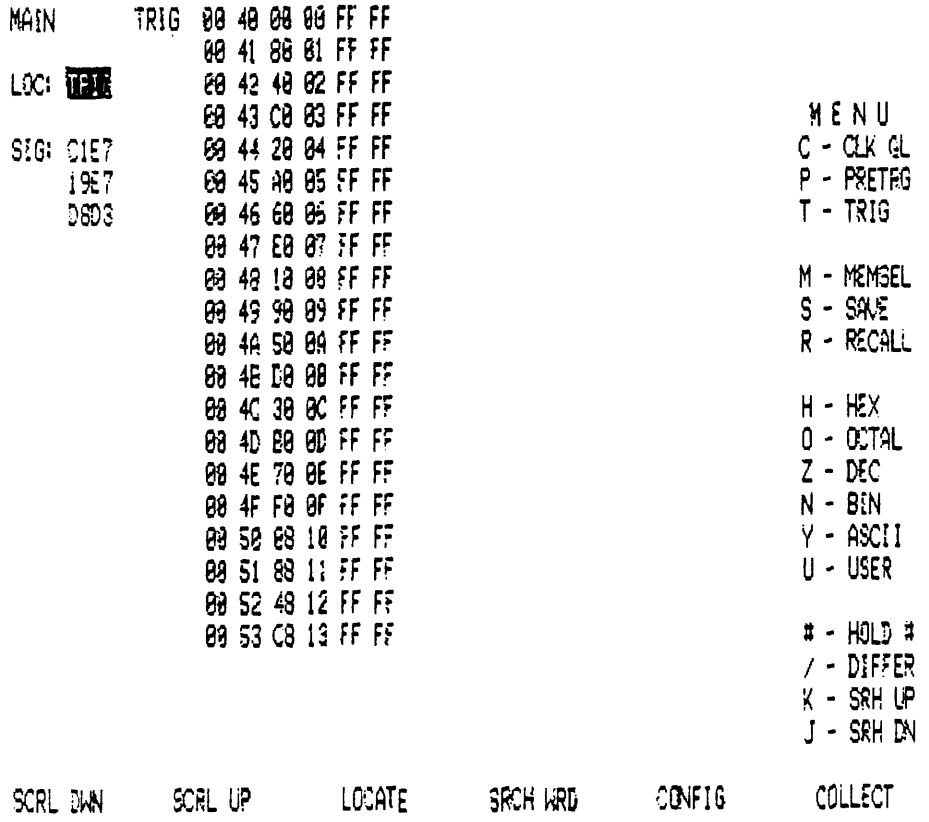


Figure 2-10 Hexademical Format Screen

```
MAIN        +027  000 091 216 027 255 255
            +028  000 092 056 028 255 255
LOC: [redacted]  +029  000 093 184 029 255 255
            +030  000 094 120 030 255 255
SIG: C1E7   +031  000 095 248 031 255 255
     79E7   +032  000 096 000 000 255 255
     D8D3   +033  000 097 120 001 255 255
            +034  000 098 064 002 255 255
HOLD# MODE  +035  000 099 192 003 255 255
 H          +036  000 100 032 004 255 255
            +037  000 101 160 005 255 255
DIFFERENCE  +038  000 102 096 006 255 255
            +039  000 103 224 007 255 255
            +040  000 104 016 008 255 255
            +041  000 105 144 009 255 255
            +042  000 106 080 010 255 255
            +043  000 107 208 011 255 255
            +044  000 108 048 012 255 255
            +045  000 109 176 013 255 255
            +046  000 110 112 014 255 255

                                                    LABELS

SCRL DWN    SCRL UP     LOCATE     SRCH WRD     CONFIG     COLLECT
```

Figure 2-11 Difference Menu Screen

```
MAIN        +027  00060000 01011011 11011000 00011011 11111111 11111111
            +028  00000000 01011100 00111000 00011100 11111111 11111111
LOC: [redacted]  +029  00000000 01011101 10111000 00011101 11111111 11111111
            +030  00000000 01011110 01111000 00011110 11111111 11111111
SIG: C1E7   +031  00000000 01011111 11111000 00011111 11111111 11111111
     79E7   +032  00000000 01100000 00000000 00000000 11111111 11111111
     D8D3   +033  00000000 01100001 10000000 00000001 11111111 11111111
            +034  00000000 01100010 01000000 00000010 11111111 11111111
            +035  00000000 01100011 11000000 00000011 11111111 11111111
            +036  00000000 01100100 00100000 00000100 11111111 11111111
            +037  00000000 01100101 10100000 00000101 11111111 11111111
DIFFERENCE  -038  00000000 01100110 01100000 00000110 11111111 11111111
            -039  00000000 01100111 11100000 00000111 11111111 11111111
            -040  00000000 01101000 00010000 00001000 11111111 11111111
            -041  00000000 01101001 10010000 00001001 11111111 11111111
            -042  00000000 01101010 01010000 00001010 11111111 11111111
            -043  00000000 01101011 11010000 00001011 11111111 11111111
            -044  00000000 01101100 00110000 00001100 11111111 11111111
            -045  00000000 01101101 10110000 00001101 11111111 11111111
            -046  00000000 01101110 01110000 00001110 11111111 11111111

                                                    LABELS

SCRL DWN    SCRL UP     LOCATE     SRCH WRD     CONFIG     COLLECT
```

Figure 2-12 Binary Difference Screen

between the main and auxiliary memories. Now return to the main memory.

2.3.4.3 Difference Mode

The DIFFERENCE mode is used for rapid identification of differences between and previously-saved auxiliary memory data and main memory.

Press the / key to activate the DIFFERENCE mode. This key toggles the DIFFERENCE mode so that repeated keystrokes turn it on and off. In this mode, only data words that differ between the main and auxiliary memories are displayed at full-intensity. Data words that match are displayed at half-intensity. Press the SCRL UP(F2) key to find the first difference word. (Simultaneously press the REPEAT key if desired). Refer to Figure 2-11.

Press the N key to view the difference in binary. Then press M and REPEAT to locate the specific bits responsible for the differences. Refer to Figure 2-12.

Return to the main memory and press the H key. Press LOCATE(F3) followed by D to place the first difference word at the top of the screen. This is an alternative and faster way of locating the first difference word. Now press LOCATE followed by S to find the next group of half-intensified words that are the same. Press the SCRL DWN key once to verify this. Refer to Figure 2-13.

Press LOCATE followed by T to place the trigger word at the top of the CRT. Then press the / key to disable the DIFFERENCE mode.

2.3.4.4 Search Word Mode

The SEARCH WORD mode allows you to locate any particular bit pattern within a data collection. You specify the word to search for and then the direction of search.

Press the SRCH WRD(F4) key to obtain the menu shown in Figure 2-14.

In the example, 009E is used as the word to be found in the data collection. (NOTE: This word occurs only once in the data memory). Key in 0-0-9-E (the rest of the field are X's - DON'T CARE). Press S2 to display the data again, then press K to search the data for 009E. Refer to Figure 2-15.

2.3.5 BASIC TIMING TEST

To test the basic timing analysis capabilities of the NPC 764 do the following:

a. Select the menu.

b. Choose a sampling clock and a trigger point.

c. Press the COLLECT(F6) key.

Before starting this test, disconnect the M51A state probes from the test card. Connect the two A and B Model 80 Timing Probes to the NPC 764. Then connect these probes to the test card A and B outputs, respectively. The state probes may be left connected to the NPC 764. Proceed as follows:

a. Press the F5 key to return to the Configuration List.

b. To select the 16-CHANNEL TIMING mode, press the SEL DOWN(F4) key. Call the menu with the TIMING(F1) key.

c. Use the PREVIOUS(F1) or NEXT(F2) key to step to the CLOCK field, if necessary. An external clock with a rising edge is selected by pressing P. Use the NEXT(F2) key to step to the TRIGGER field. Specify a trigger word of 0-0-0-0-0-0-0-0 1-0-0-1-1-0-0-0. Use the NEXT key to step down to the PRETRIGGER field. Set this field to 00%. Leave all other menu entries set at the default value as shown in Figure 2-16.

```
MAIN          +864  00 80 82 40 FF FF
              +865  00 81 82 41 FF FF
LOC: [redacted]  +866  00 82 42 42 FF FF
              +867  00 83 C2 43 FF FF
SIG: C1E7     +868  00 84 22 44 FF FF
     79E7     +869  00 85 A2 45 FF FF
     D8D3     +870  00 86 62 46 FF FF
              +871  00 87 E2 47 FF FF
              +872  00 88 12 48 FF FF
              +873  00 89 92 49 FF FF
              +874  00 8A 52 4A FF FF
DIFFERENCE    +875  00 8B D2 4B FF FF
              +876  00 8C 32 4C FF FF
              +877  00 8D B2 4D FF FF
              +878  00 8E 72 4E FF FF
              +879  00 8F F2 4F FF FF
              +880  00 90 0A 50 FF FF
              +881  00 91 8A 51 FF FF
              +882  00 92 4A 52 FF FF
              +883  00 93 CA 53 FF FF

                                                          LABELS

 SCRL DWN     SCRL UP      LOCATE      SRCH WRD     CONFIG      COLLECT
```

Figure 2-13 First Difference Word

```
FORMAT: AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA AAAAAAAA
          A HEX

SEARCH WORD:

        00?EXXXXXXX
```

```
                                                          H - HEX
                                                          O - OCTAL
                                                          Z - DEC
                                                          N - BINARY
                                                          Y - ASCII
    S2 - DATA DISPLAY                                     U - USER

 PREVIOUS     NEXT        SELECT      DEFAULT      CONFIG      COLLECT
```

Figure 2-14 Search Word

```
MAIN        +094  00 9E 7A 5E FF FF
            +095  00 9F FA 5F FF FF
LOC: [redacted] +096  00 A0 02 40 FF FF
            +097  00 A1 82 41 FF FF
SIG: C1E7   +098  00 A2 42 42 FF FF
     79E7   +099  00 A3 C2 43 FF FF
     D8D3   +100  00 A4 22 44 FF FF
            +101  00 A5 A2 45 FF FF
            +102  00 A6 62 46 FF FF
            +103  00 A7 E2 47 FF FF
            +104  00 A8 12 48 FF FF
DIFFERENCE  +105  00 A9 92 49 FF FF
            +106  00 AA 52 4A FF FF
            +107  00 AB D2 4B FF FF
            +108  00 AC 32 4C FF FF
            +109  00 AD B2 4D FF FF
            +110  00 AE 72 4E FF FF
            +111  00 AF F2 4F FF FF
            +112  00 B0 0A 50 FF FF
            +113  00 B1 8A 51 FF FF

                                                        LABELS

SCRL DWN    SCRL UP     LOCATE     SRCH WRD    CONFIG     COLLECT
```

Figure 2-15 Difference Menu Screen

```
                16 CHNL TIMING/STATE MENU

          EXT ∫ CLOCK   CLK QUAL: X
  TRIGGER WHEN:
              TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
            CHNL NO. A76543210 B76543210  FILTER  LINKAGE
 ARM (0,1,X):          XXXXXXXX XXXXXXXX   OFF     NONE
 TRIG (0,1,X):         00000000 10011000   OFF     NONE
 INPUT MODE (S,L):     SSSSSSSS SSSSSSSS
 PRE-TRIGGER (0-9):  00%
                       AAAAAAAA BBBBBBBB
 DISPLAY ORDER (0-7,X): 76543210 76543210
 DISPLAY POLARITY (+,-): ++++++++ ++++++++
        THRESHOLD:     A PROBE     B PROBE    HYSTERESIS
     (-6.4V - +6.35V)   +1.60       +1.60        ON




    S1 - STATE DISPLAY
    S2 - TIMING DISPLAY

PREVIOUS      NEXT                                CONFIG     COLLECT
```

Figure 2-16 16 Channel Timing Menu

d. Press COLLECT(F6) key. When a data capture is complete, the screen fills with the timing diagram display. Refer to Figure 2-17.

e. The inverse video graticule represents the entire 1000 samples in the memory. See Figure 2-17. Observe the 00 indicator at the left end of the graticule is intensified. This indicates the 00% pre-trigger value set in previously. With 00% pre-trigger, the first word in the data collection (word 000) is the trigger word. The cursor reads the binary and hexadecimal values of each location in the data memory where the cursor is placed. Thus, the trigger word at cursor location 000 should be $(0098)_{HEX}$. In Figure 2-17, this trigger word appears at the upper right-hand corner of the CRT.

f. Figure 2-17 also shows the 16 timing channels and the corresponding binary values at cursor location 000. The four most significant A channels (A7-A4) are at ground as described previously. The cross-hatched areas on certain channels indicate that data in the memory are occurring too close together. The current X1 magnification factor is unable to resolve this visually.

g. Sweep the expansion symbol, E, towards the middle of the CRT by pressing F2 and REPEAT. Stop the symbol at location 500 as indicated by the EXPAND FROM: readout in the

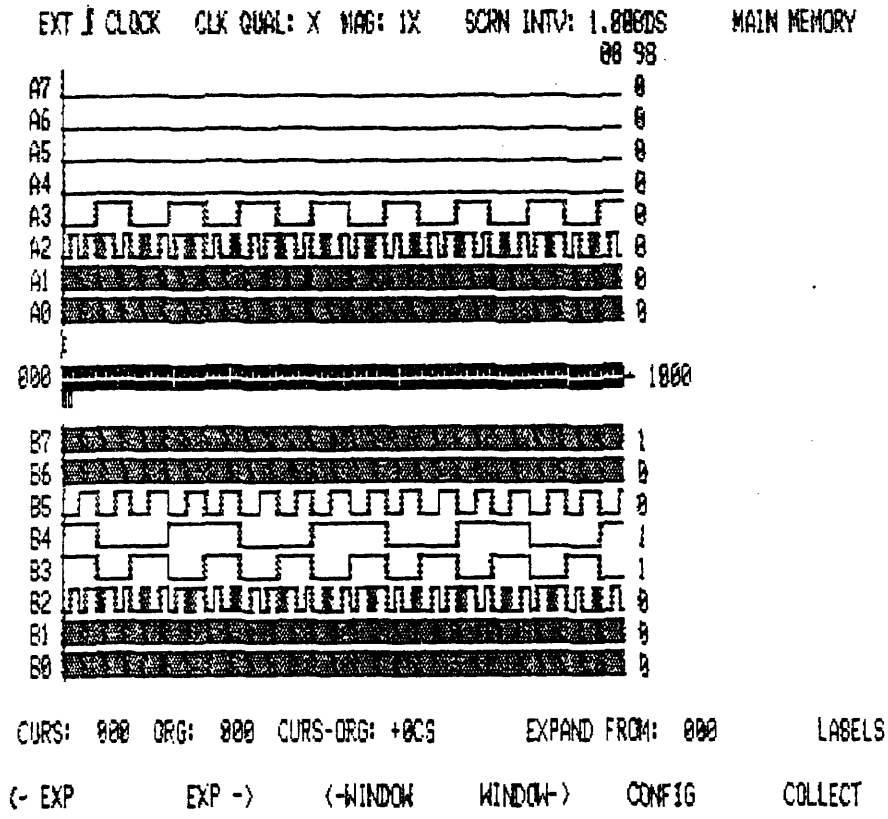


Figure 2-17 Timing Diagram Display

lower right-hand portion of the CRT. Refer to Figure 2-18.

h. Next press the LABELS key. Try magnification factors between 2X to 20X using the 2 to 5 numeric keys as indicated in the LABEL MENU. After higher magnification keys are pressed, the inverse video indicator at the bottom of the screen reduces proportionately in size. This indicator shows the location and amount of timing data currently being displayed relative to the entire 1000-word data collection. At 20X magnification, note that the inverse video indicator is only 5% of the original (1X) size. The screen now displays timing data between memory locations 500 and 550. Refer to Figure 2-19. Finish by setting the magnification at 10X.

i. View other segments of the memory by pressing the WINDOW(F3) or the WINDOW (F4) keys and the REPEAT key simultaneously. Return to a data window of 500 to 550 as shown in Figure 2-19. Also return the expansion symbol to the left-hand side of the CRT.

j. To quickly move the cursor from 000 to the left side of the screen interval, press the L (LOCATE CURSOR) key. This is indicated in the LABELS menu. Bring the cursor to the center of the CRT by pressing the SPACE BAR and the REPEAT keys simultaneously. Overshoot can be

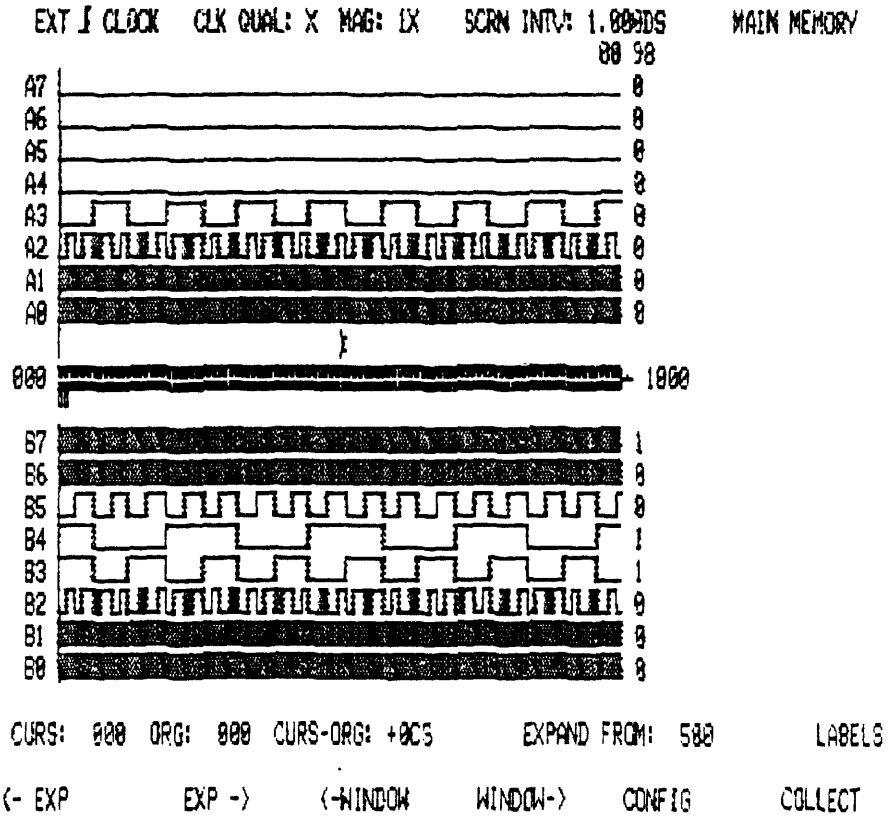


Figure 2-18 Timing Display at Location 500

lower right-hand portion of the CRT. Refer to Figure 2-18.

h. Next press the LABELS key. Try magnification factors between 2X to 20X using the 2 to 5 numeric keys as indicated in the LABEL MENU. After higher magnification keys are pressed, the inverse video indicator at the bottom of the screen reduces proportionately in size. This indicator shows the location and amount of timing data currently being displayed relative to the entire 1000-word data collection. At 20X magnification, note that the inverse video indicator is only 5% of the original (1X) size. The screen now displays timing data between memory locations 500 and 550. Refer to Figure 2-19. Finish by setting the magnification at 10X.

i. View other segments of the memory by pressing the WINDOW(F3) or the WINDOW (F4) keys and the REPEAT key simultaneously. Return to a data window of 500 to 550 as shown in Figure 2-19. Also return the expansion symbol to the left-hand side of the CRT.

j. To quickly move the cursor from 000 to the left side of the screen interval, press the L (LOCATE CURSOR) key. This is indicated in the LABELS menu. Bring the cursor to the center of the CRT by pressing the SPACE BAR and the REPEAT keys simultaneously. Overshoot can be remedied by pressing the BACKSPACE key.

k. In this step we will measure the relative time between the edges in two channels. Visually select an edge (rising or falling) in channel A2 and another edge (later in time) in channel B6. Step the cursor so that it aligns with the selected

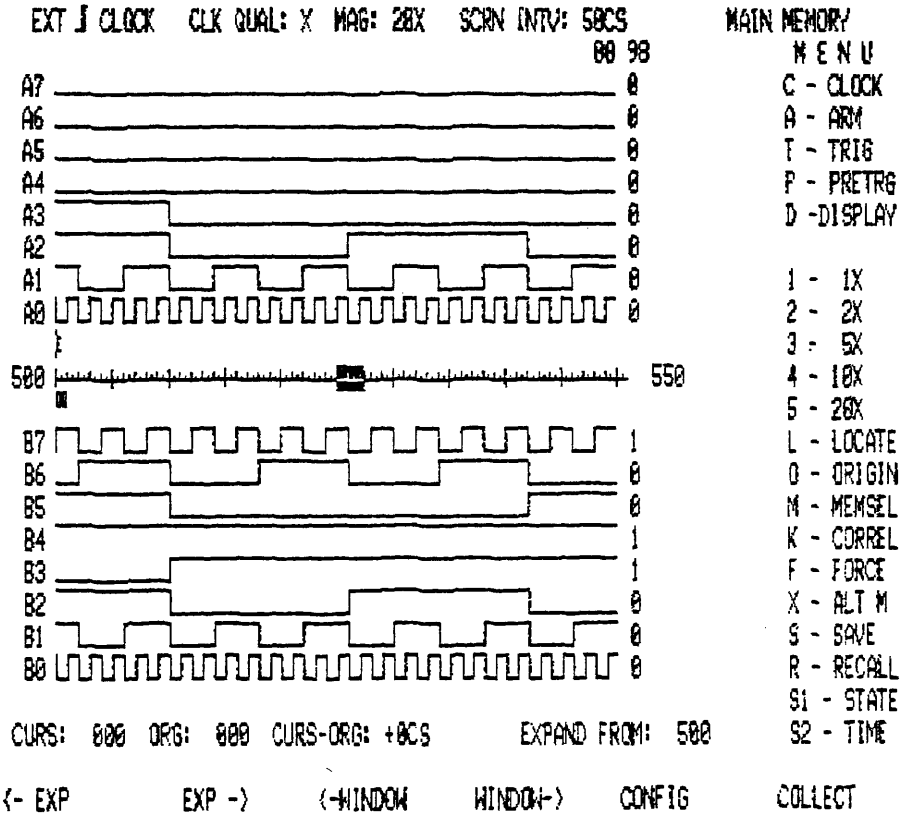


Figure 2-19 Timing Display and Menu

edge in Channel A2. Note the value of the cursor position indicator at the lower left of the screen. Now press the letter O to reset the origin from 000 to the current cursor location. The CURS-ORG indicator should now read +0CS, where CS stands for clock samples. When an internal clock is being used, the indicator reads in units of time. Next, step the cursor to the selected edge on channel B6. The CURS-ORG indicator will now directly read the time (in clock samples) between these two edges. Figure 2-20 demonstrates one sample using this measurement procedure.

l. Press the COLLECT key to take a new data collection. Then press the SAVE(S) key and observe the flashing SAVED message. To compare main and auxiliary data press K(CORREL) key. Note that a correlation factor of 1.000 is displayed at the right of each channel. This factor indicates that the 1000 bits in each main memory channel compares with the 1000 bits in the corresponding auxiliary memory channel. Comparisions are done on a bit-for-bit basis. Refer to Figure 2-21. Thus, if a correlation factor of .995 were displayed, it would indicate that 5 bits out of 1000 were different.

m. Now short out the pad labeled 5 on the B side of the test card. While holding the short in place, press COLLECT. Now remove the short. To see which channel was affected by the short, again press K. Note that the correlation factor for channel B5 is significantly lower than 1.000. The other channels still have correlation factors of 1.000. This results from the use in this example of an external, synchronous clock from the test card. If the internal, asynchronous clock were used, the correlation factors of the other channels would probably never be exactly 1.000. This is due to normal sampling uncertainties.

n. In order to view the actual effect of the short on channel B5, press the X(ALT MEMORY) key. As shown in Figure 2-22, channel B5 should cycle between a 1 and a 0. Return to the main memory by pressing M. Also return to a 1X magnification by pressing the 1 key.

To view the timing data in a state format, press S1. The state data can be displayed in HEX, OCTAL, DECIMAL, BINARY or ASCII. Refer to Figure 2-23. Press the LABELS key to display the menu of formats available in this mode. Return to the timing diagram display by pressing S1 again.

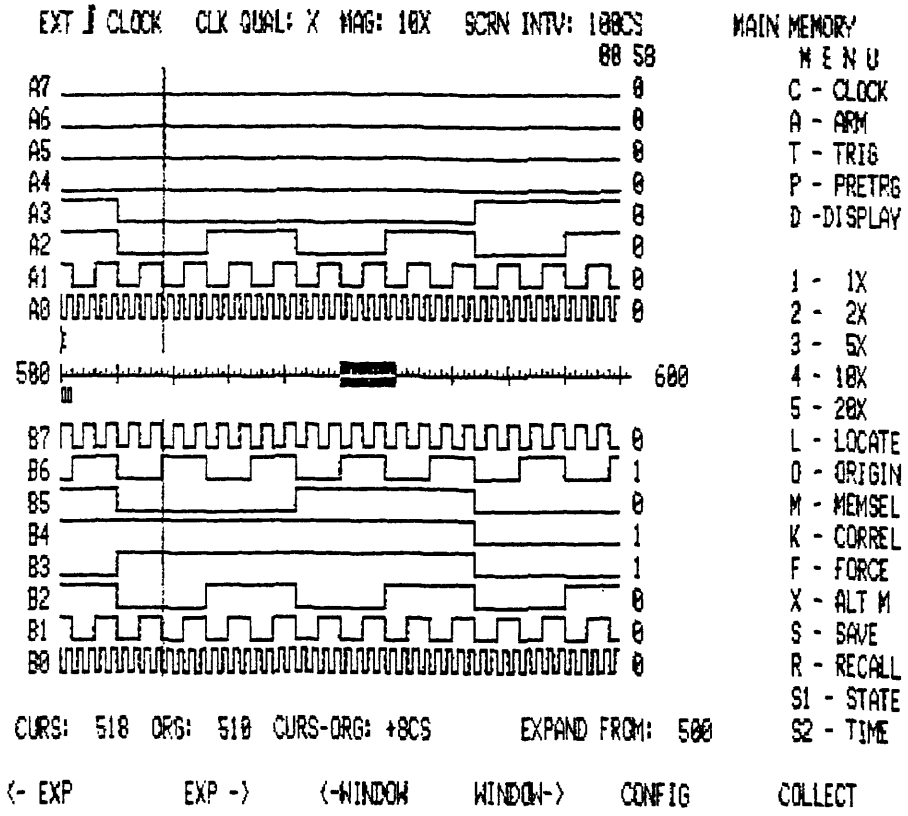


Figure 2-20 Clock Timing Samples

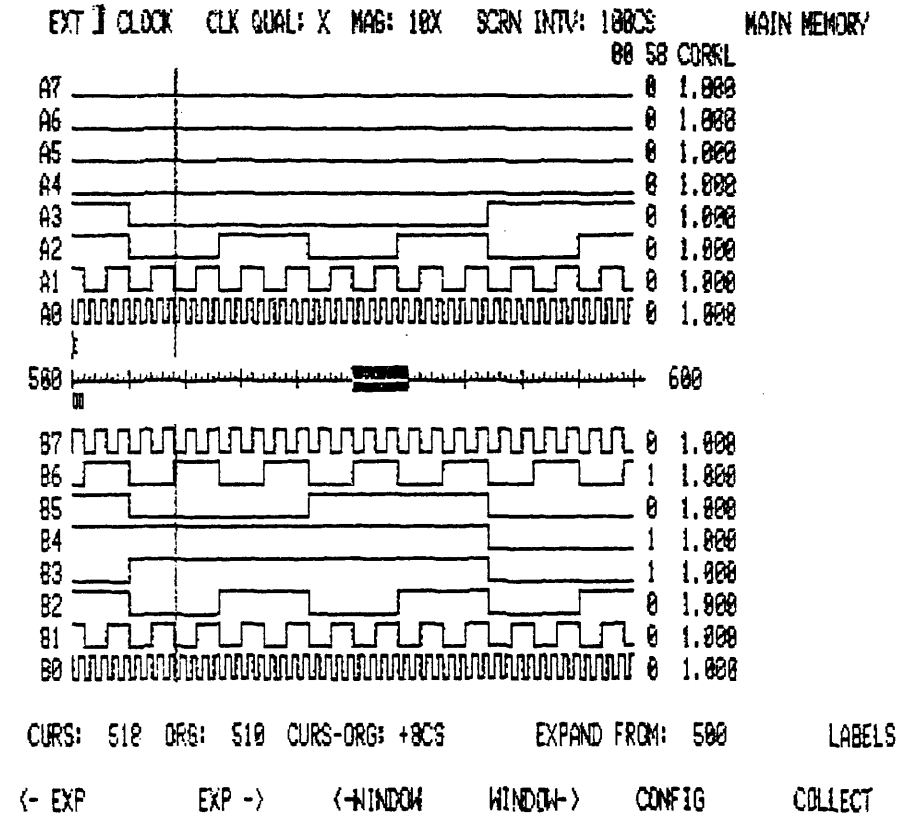


Figure 2-21 Correlation Display

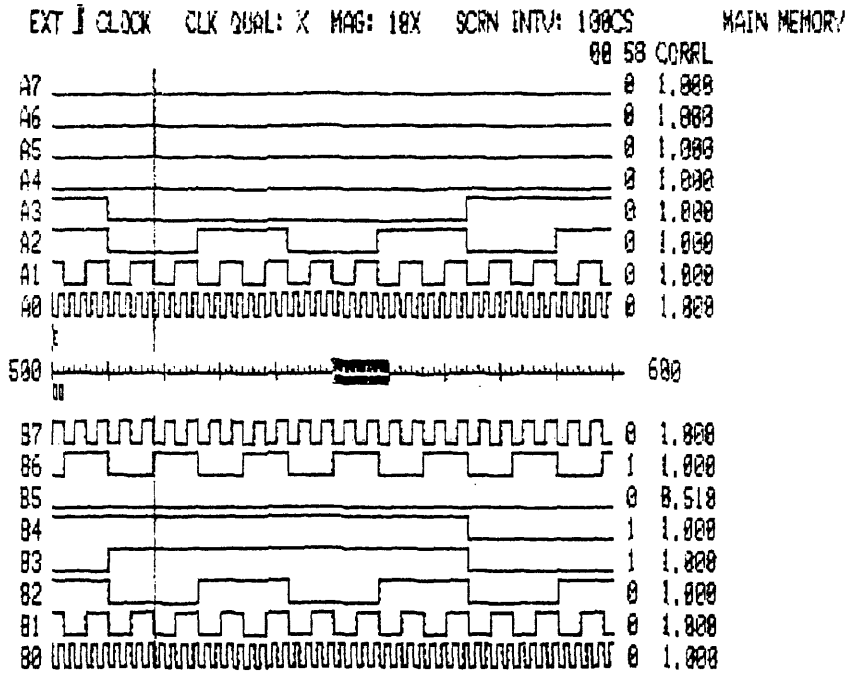


Figure 2-22 Correlation Display

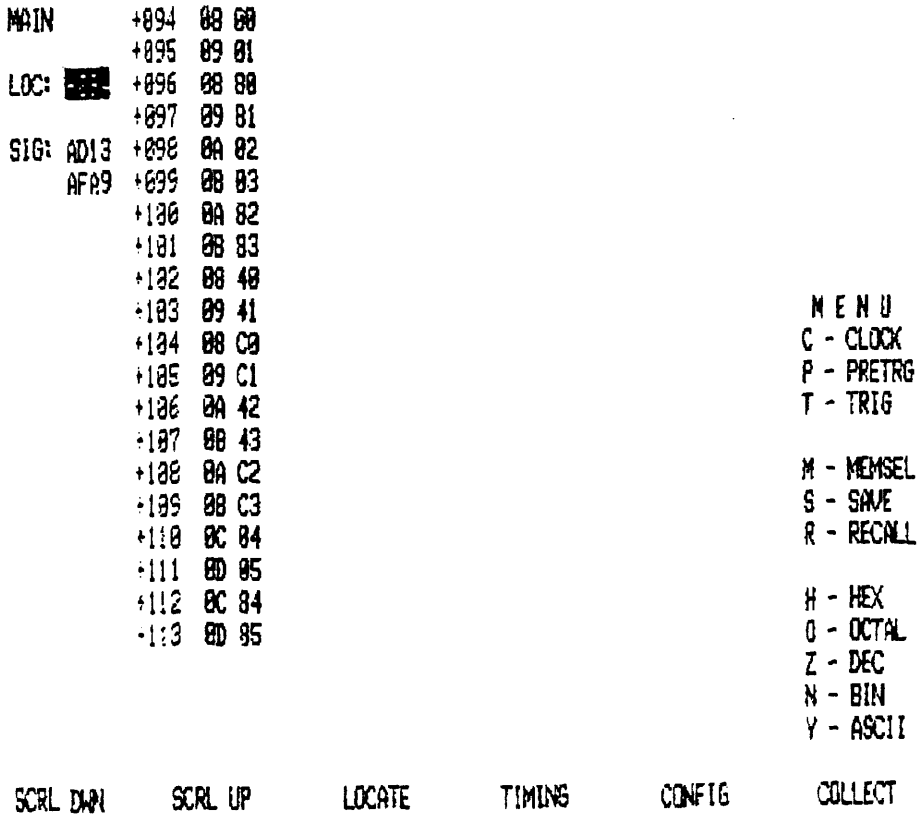
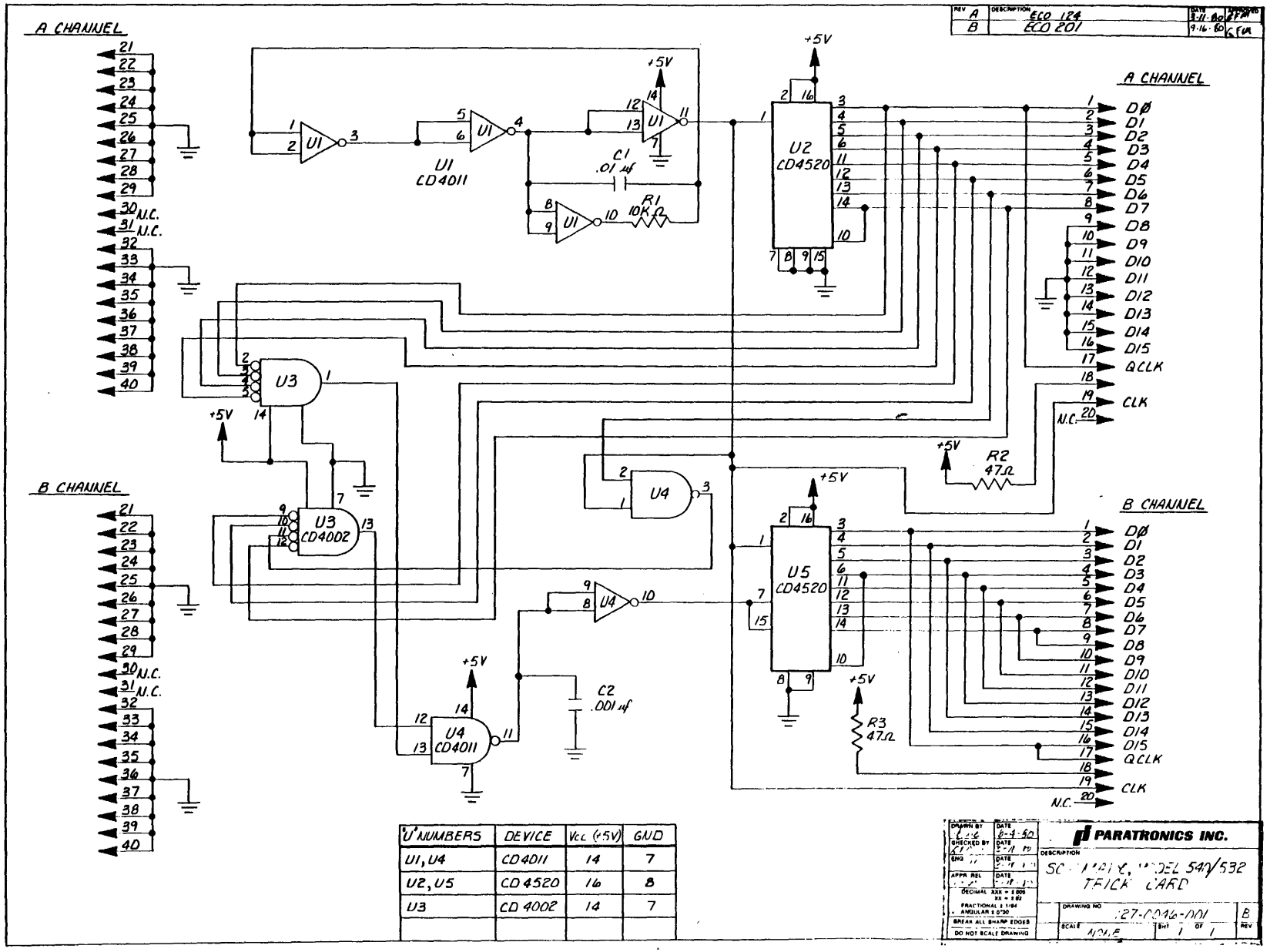


Figure 2-23 State Menu

PARENT ITEM 143-0046-0002 | CROSS REF ITEM | DESCRIPTION LOGIC ANALYZER DEMO CARD ENGR DRAW 261 D | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0031	47 OHM 1/4W 5% CF RES R2 R3		2.000	EA	4C				2/25/80	
	06	110-0005-0039	100 OHM 1/4W 5% CF RES		1.000	EA	4C					
	06	110-0005-0087	10K OHM 1/4W 5% CF RES R1		1.000	EA	4C					
	06	111-0004-0066	.01 UF 25V CD CAP C1		1.000	EA	4C					
	06	111-0006-0050	.001 UF 50V CD CAP C2		1.000	EA	4C				2/25/80	
	04	113-0023-0001	I.C. CD4520 U2 U5		2.000	EA	4C				2/25/80	
	04	113-0039-0001	I.C. CD4011 U1 U4		2.000	EA	4C				2/25/80	
	04	113-0046-0001	I.C. CD4002 U3		1.000	EA	4C				2/25/80	
	05	117-0115-0001	JUMPER RUBBER STEM 322-2		4.000	EA	4C				2/25/80	
	07	119-0002-0001	SHRINK TUBE 1/8 WHITE		1.000	IN	4C				6/24/80	
	04	119-0055-0002	#26 AWG STRANDED WIRE BLK 4.5		1.000	EA	4C				1/15/81	
	04	126-0046-0001	LOGIC ANALYZER DEMO CARD PCB	ECO 160 REV 2	1.000	EA	4C				2/25/80	
	04	127-0046-0001	DEMO CARD PCB SCHEMATIC		.000	EA	0				2/10/82	



REV	DESCRIPTION	DATE
A	ECO 124	3-11-80
B	ECO 201	9-16-80

'U' NUMBERS	DEVICE	Vcc (+5V)	GND
U1, U4	CD4011	14	7
U2, U5	CD4520	16	8
U3	CD 4002	14	7

PARATRONICS INC.

DESCRIPTION: SC[illegible], MODEL 540/532 TRICK CARD

DRAWING NO: 27-0046-001 B

SCALE: NONE SHT 1 OF 1 REV

CHASSIS, MOTHERBOARD, POWER SUPPLY, DISK DRIVE

SECTION 3: CHASSIS, MOTHERBOARD, POWER SUPPLY, DISK DRIVE

SECTION III
CHASSIS, MOTHERBOARD, POWER SUPPLY AND DISK DRIVE

3.1 INTRODUCTION

Refer to the schematic diagrams, board layouts, interconnection diagram, and the parts lists located at the end of this section. Tables of connector pins versus signals names for all motherboard connectors are provided in the SIGNAL AND INTERCONNECTION TABLES section. An alphabetical list of all interboard signals is included. The GLOSSARY offers explanations for acronyms or terms that may be unfamiliar.

3.2 CHASSIS FUNCTIONAL DESCRIPTION

The chassis provides the supporting structure for the Front Bezel, the Display Module, the Card Cage Assembly, the Rear Panel and Power Supply. The top cover, a part of the chassis, gives complete protection to the internal components and adds structural strength to the complete assembly.

The units that will be discussed as part of the chassis group are the following: The chassis, the cover, the carrying handle, the Mains Module, the auxiliary power transformer, the cooling fan, and the interconnecting wiring.

Refer to Figure 3-1. The **Chassis** consists of an aluminum bottom pan that mounts the front casting, rear panel, and extrusion rails. The front casting is joined to the rear panel by the longitudinal extrusion rails . The rails accept the side edges of the cover and bottom pan. There is a large rectangular hole in the front casting through which the CRT screen is viewed. A plastic face plate is attached directly to the CRT tube. The face plate protects the CRT and is lightly tinted to enhance the contrast of the display.

The shielded Display Module is mounted to the bottom pan by three threaded studs set into the bottom pan. The Card Cage Assembly is mounted to the bottom pan by three screws through the bottom pan. The cooling fan fastens to the rear panel by three screws through the rear panel. The auxiliary power transformer fastens to the rear panel by nuts on two threaded studs set into the rear panel. The Mains Module mounts into a rectangular hole in the rear panel with snap-in fasteners. The BNC connectors, Serial and GPIB connectors mount onto the card cage and project through openings in the rear panel.

WARNING

DISCONNECT THE A-C POWER CORD AT THE BACK OF THE CHASSIS BEFORE REMOVING THE COVER. THE DISPLAY MODULE CONTAINS A VERY HIGH VOLTAGE OF 9 KV THAT CAN BE LETHAL. EXTREME CAUTION MUST BE USED WHENEVER POWER IS APPLIED TO THE NPC 764 WITH THE COVER REMOVED.

The **cover** folds around the top and half way down the sides of the instrument. It fits into grooves in the extrusion rails. Clips that fit under the front casting secure the front of the cover. The cover is held in place at the rear by two quarter-turn fasteners that mate into fittings in a flange on the rear panel.

The **carrying handle** attaches to the extrusion rails. When the analyzer is in use, the handle can be folded underneath to act as a stand. This props up the front of the instrument so the keyboard is at a convenient height.

The **Mains Module** is mounted in a rectangular cutout in the rear panel. It is held in place by snap-in fasteners attached to the sides of the module. Refer to the chassis wiring diagram.

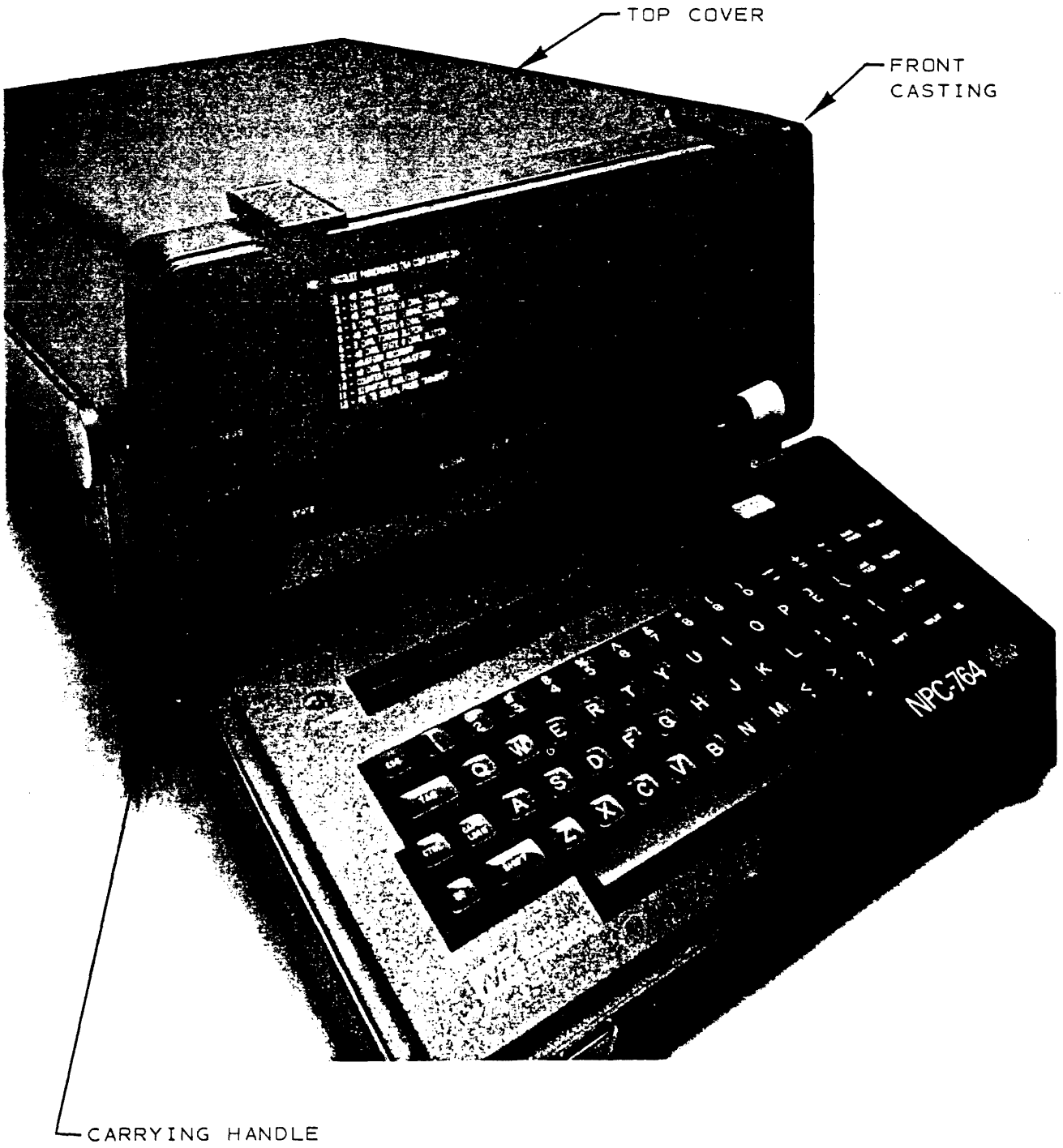
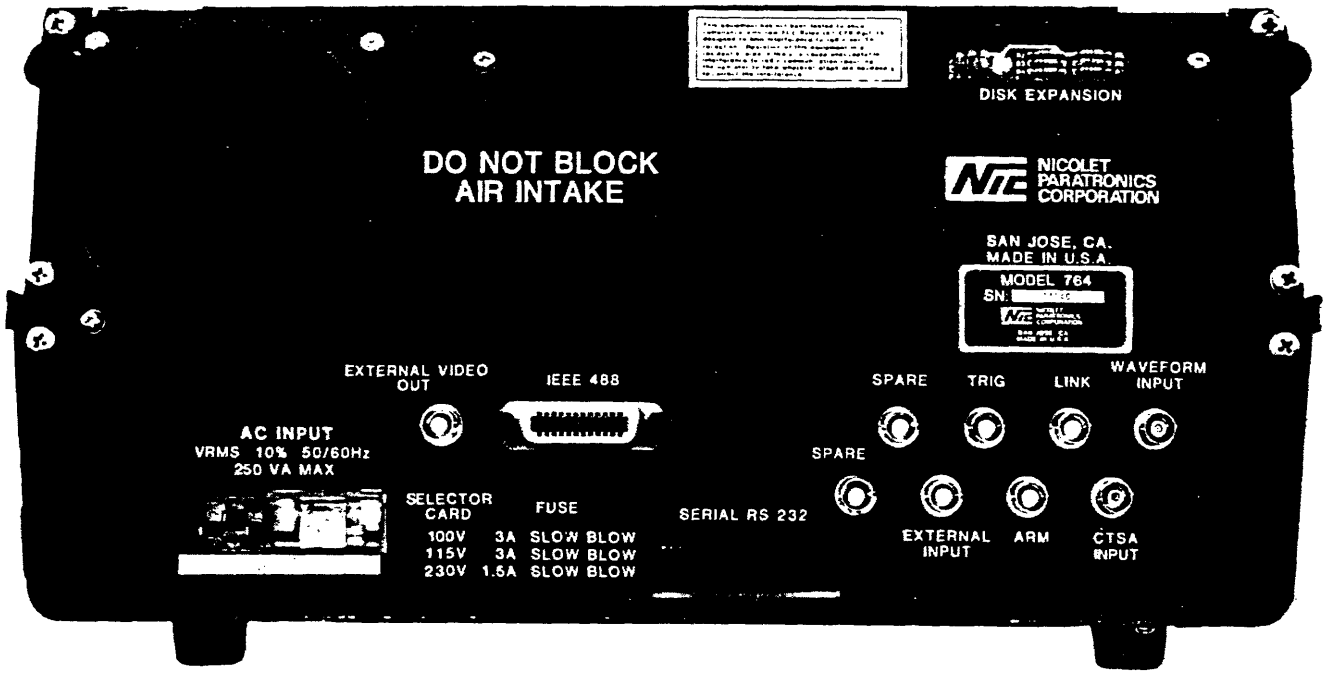
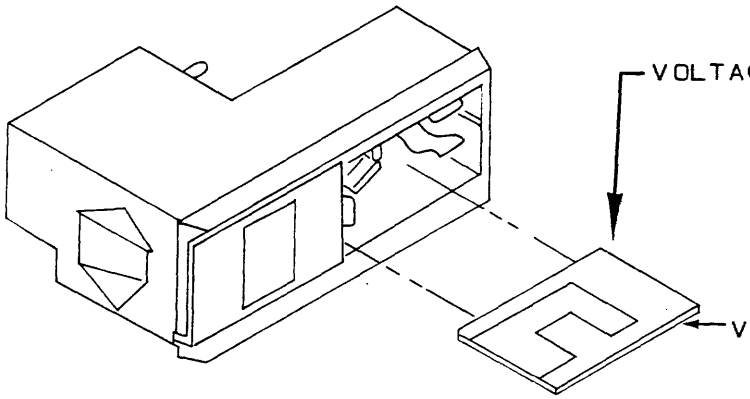


Figure 3-1 NPC 764 Logic Analysis System

A Voltage PCB in the Mains Module allows selection of the power mains voltage for the instrument. The sliding cover for this Voltage PCB can be opened only when the power cord is unplugged from the module. Voltage designators are etched in copper near the edges of the Voltage PCB. The voltage designator programmed by the PCB is visible on the rear edge when the board is in place. Refer to Figure 3-2.





SELECT:
100 V NOMINAL
115 V NOMINAL
230 V NOMINAL

AS APPROPRIATE

NOTE: THE CARD MUST BE ORIENTED SO THAT THE SELECTED VOLTAGE CAN BE READ WITH THE CARD INSTALLED.

Figure 3-2 Rear Panel and Voltage Select Card

CAUTION

BEFORE APPLYING POWER TO THE NPC 764, MAKE CERTAIN THAT THE PROGRAMMED MAINS VOLTAGE CORRESPONDS TO THE VOLTAGE BEING USED. OTHERWISE, SERIOUS DAMAGE TO THE INTERNAL POWER SUPPLY MAY RESULT.

To change the voltage programmed, remove the PCB, change the orientation, and re-insert it. The voltages available for selection are shown in Table 3-1.

The power-mains fuse is located on the Mains Module just above the Voltage PCB. The rating of the fuse depends on the voltage programmed. The required fuse ratings are included in Table 3-1.

Table 3-1 Power Source Requirements

Selector Card	Operable Range, V	Fuse Req'd
100 V	90-110	3 AMP Slow Blow
115 V	105-125	3 AMP Slow Blow
230 V	210-250	1.5 AMP Slow Blow

The auxiliary transformer is mounted on two threaded studs set into the rear panel just above the Mains Module. The primary of this transformer acts as an autotransformer. It supplies a nominal 115 VAC to the fan motor regardless of the programmed mains voltage. The secondary supplies 17 VAC to the Power Supply for an auxiliary supply circuit, also independent of the mains voltage.

The cooling fan is mounted in a 4-inch round, air-intake hole in the rear panel. This hole is covered by a replaceable air filter. The fan motor is supplied with 115 VAC power from the auxiliary transformer. There are air vent slots in the cover for air exhaust. The fan draws air in through the rear panel air filter and exhausts it from these vents. This air flow lowers operating temperatures within the cabinet to safe levels. The air filter can be removed by loosening the three screws holding the filter retaining clips. The filter should be cleaned by washing in soapy water monthly (more often in dirty environments).

CAUTION

IF THE FAN IS NOT FUNCTIONING, OR IF THE AIR FILTER IS DIRTY OR OTHERWISE OBSTRUCTED, DO NOT OPERATE THE NPC 764. DOING SO MAY RESULT IN SERIOUS DAMAGE TO COMPONENTS THROUGHOUT THE INSTRUMENT.

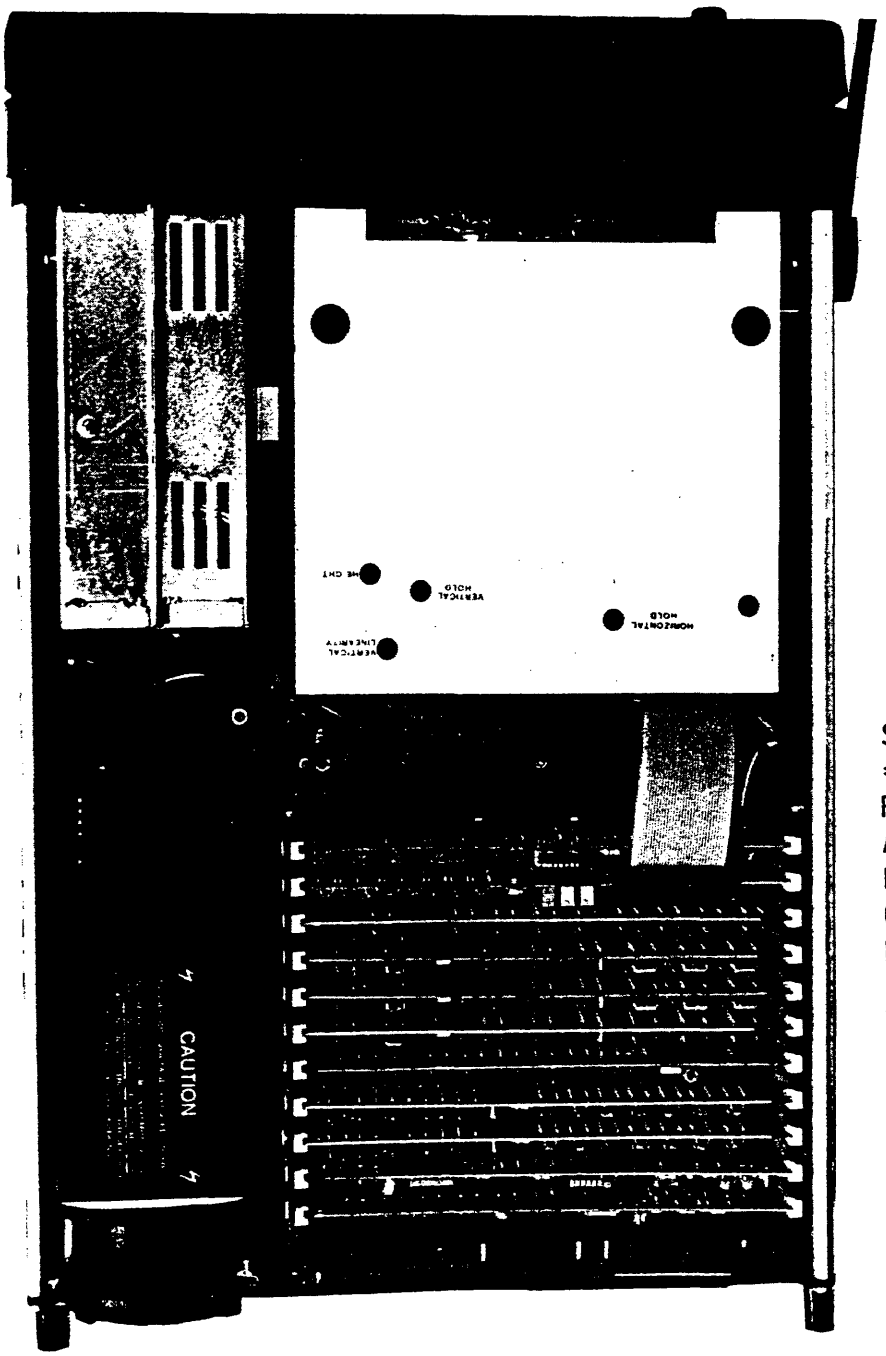
The interconnecting wiring is shown in the wiring diagram at the end of this section. All interconnections to the Display Module, Card Cage assembly, Front Panel, and Power Supply are made through connectors. Any of these units can be removed without unsoldering wires.

3.3 MOTHERBOARD FUNCTIONAL DESCRIPTION

A Motherboard in the NPC 764 contains sockets, card guides and supporting structure for the individual PC boards. Refer to Motherboard schematic #127-0123-001 and the board layout drawing #126-0123-001. The Motherboard contains sockets, card guides and interconnections for 11 circuit boards. The slot assignments for individual PC boards are fixed and boards are keyed to interface only into the correct slots. Refer to Figure 3-3.

CAUTION

DO NOT ATTEMPT TO FORCE A PCB INTO AN INCORRECT SLOT OR DAMAGE TO THE CONNECTOR OR PCB MAY RESULT.



SLOT	CIRCUIT BOARD
FRONT	
A	Processor
B	RAM DISK
C	State Control
D	State Memory-C (LSB)
E	State Memory-A (MSB)
F	State Memory-B
G	Timing Control
H	Timing Memory-A
I	Timing Memory-B
J	Waveform
K	Counter-Timer/SA

The location and part numbers of the boards are listed below:

SLOT	CIRCUIT BOARD	PART NUMBER
FRONT		
A	Processor	143-0130-001
B	RAM DISK	143-0112-001
C	State Control	143-0128-001
D	State Memory-C (LSB)	143-0127-001
E	State Memory-A (MSB)	143-0127-001
F	State Memory-B	143-0127-001
G	Timing Control	143-0071-001
H	Timing Memory-A	143-0065-003
I	Timing Memory-B	143-0065-004
J	Waveform	143-0072-001
K	Counter-Timer/SA	143-0099-001
REAR		

Note that the three State Memory boards are identical and may be interchanged. The two timing Memory boards contain different decoded PROMs U52. The PROM marked 113-4035-14 is required for the A Timing Memory board in slot H. The PROM marked 113-4035-15 is required for the B Timing memory board in slot I.

The Clock Qualifier Gate (U6) and the Clock Multiplexer (U2), both part of State Control, are contained on the Motherboard. These circuits are described in the STATE CONTROL BOARD section. Additional circuitry (U1, U3, U5, U7) interfaces the link control signals and provides additional clock selection control. Components U4, U7, U8, U9, 10 and U11 are shown on the board layout drawing. The circuitry is shown on the Motherboard schematic. The signals that must be sent to the Keyboard are fed to connector S2. This connector mates with P2 via a flat ribbon cable connected to the Keyboard.

The PC Board sockets are interconnected as described in the SIGNAL AND INTERCONNECTION TABLES section. Some inversion of address lines to S1 is done so that electrically identical boards (Memory) can occupy unique address spaces.

3.4 POWER SUPPLY FUNCTIONAL DESCRIPTION

The Power Supply is mounted to the bottom pan of the instrument and is enclosed in a protective housing. The Power Supply is a pulse-width modulated, half-bridge, 25 KHz switching circuit operating directly off the a-c power line. It supplies +/-5 V and +/-15 V to the Keyboard and Card Cage, +12 V to the Display Module and +5 V or +12 V to the disk drive. Also, it provides very effective overvoltage and overcurrent protection for both the Power Supply itself and the circuits that it supplies.

Refer to schematic #127-0122-001. The major functional units of the Power Supply circuit are the High Voltage Section, Control Section and Output Section. These units are discussed further in the following subsections. Refer to assembly drawing 143-0122-001 for major component location, disassembly and assembly information. Assembly drawing 126-0122-201 depicts the PC Board component locations.

WARNING

THIS POWER SUPPLY CIRCUIT IS CONNECTED DIRECTLY TO THE A-C MAINS WITH NO INTERVENING ISOLATION TRANSFORMER. WHEN POWER IS APPLIED, LETHAL VOLTAGES ARE PRESENT. ONLY QUALIFIED SERVICE PERSONNEL FAMILIAR WITH LINE-OPERATED SWITCHING POWER SUPPLIES SHOULD UNDERTAKE SERVICE OF THIS SUPPLY, AND THEN ONLY WITH THE ISOLATING TEST SET-UP DESCRIBED BELOW. FAILURE TO OBSERVE THESE PRECAUTIONS MAY RESULT IN SERIOUS INJURY OR DEATH.

3.4.1 TEST SET-UP

The a-c input power is fed directly from the mains to rectifier circuit DB1 without an intervening isolation transformer. Therefore, it is essential that an isolation transformer be incorporated in the test set-up as shown in Figure 3-4.

WARNING

MEASUREMENTS OR TESTS UNDERTAKEN WITHOUT THE USE OF AN ISOLATION TRANSFORMER MAY RESULT IN SERIOUS INJURY OR DEATH TO PERSONNEL.

To gain access to the Power Supply, proceed as follows:

NOTE

READ THE ENTIRE PROCEDURE ONCE BEFORE STARTING.

a. Disconnect the power cord. Wait three minutes after the power is turned off to allow the capacitors to fully discharge.

b. Remove the top cover by loosening the two quarter-turn fasteners at the rear of the cover and slide cover back.

c. Remove the two nuts holding down the power supply cover. These are located between the power supply cover and disk drive bracket. Be careful not to damage the ground straps connected to the grounding stud.

d. Turn the unit over to expose the bottom cover. Then remove the two screws near the rear that hold down the power supply cover. The cover may now be removed, exposing the supply.

To remove the supply proceed as follows:

a. Unplug the power cords connecting the power supply to the disk drive, CRT and main Motherboard.

b. Remove the six screws mounting the power supply heatsink to the bottom pan. These may be accessed from the bottom.

c. The supply is now free and may be lifted up. Complete removal is accomplished by unplugging the six-conductor a-c plug.

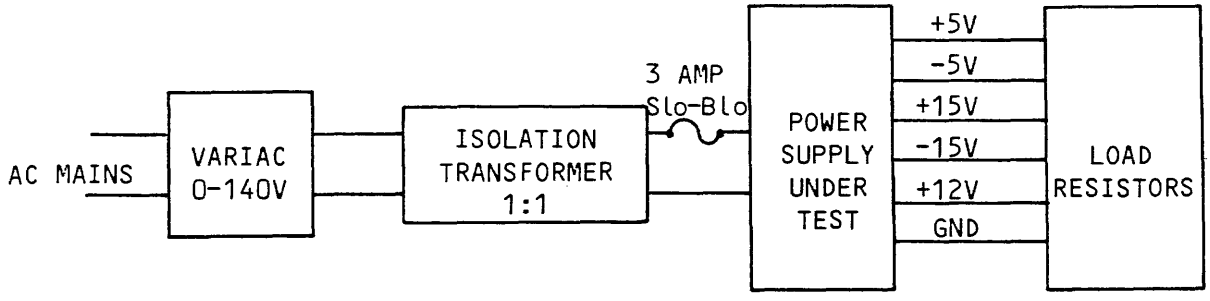


Figure 3-4 Power Supply Test Set-Up

CAUTION

DO NOT RISK DAMAGE TO VALUABLE CIRCUIT BOARDS BY USING THE ANALYZER AS A TEST LOAD FOR THE SAKE OF CONVENIENCE.

USE RESISTORS AS DESCRIBED IN THE FOLLOWING PARAGRAPH. **NOTE** THAT NO LOAD IS NEEDED ON THE +12 V SUPPLIES UNLESS THEY ARE SPECIFICALLY UNDER INVESTIGATION.

To load the power supply outputs, proceed as follows:

a. Obtain a mating connector for P12 (see parts list). Make an adapter to connect the load resistors between the outputs and ground returns. Load resistance values are shown below:

MINIMUM LOADING

OUTPUT	CURRENT	RESISTANCE	RATING
+5 V	5 A	1 ohm	25 W
-5 V	5 A	1 ohm	25 W
+12 V	---	(no load needed)	
+15 V	200 mA	75 ohms	5 W
-15 V	200 mA	75 ohms	5 W

b. Bring power to the Power Supply by connecting the Mains Module through an isolation transformer to the power mains.

3.4.2 HIGH VOLTAGE SECTION

The High Voltage Section consists of the following: DB1, a VH 648 bridge rectifier; Q1 and Q2, Motorola MJE13007 power switching transistors; CR1,2, 1N3600 diodes; CR3,4, 1N4637 diodes; transformers T1 and T2; thermistor R1; and various resistors and capacitors.

This circuitry converts a nominal 100, 110 or 220 VAC, 50-60 Hz mains voltage to a center-tapped nominal +/-162 d-c voltage. This d-c voltage is converted to a fixed-frequency, pulse-width modulated, a-c voltage across T1. The conversion is performed by the action of Q1, Q2, T2 and the control section. The output voltages of T1 are a nominal 5 and 15 VAC RMS at a nominal frequency of 25 KHz.

Input from the power mains is sent directly to the rectifier DB1 with no intervening isolation transformer. Consequently, all components within the High Voltage Section are at mains potential! **PLEASE SEE PRECEDING WARNINGS AND CAUTIONS!** A Mains Module contains a Voltage PCB that is used to select the a-c mains voltage that will be used to power the analyzer. This was described previously under CHASSIS. The three selection options are 100, 110 and 230 VAC.

If a mains voltage of 230 VAC is selected, it is applied across input pins P1-2 and P1-6. DB1 acts as a full-wave bridge rectifier and produces a nominal 325 V. This d-c voltage is filtered by filter capacitors C3 and C4 connected in series. The junction of C3 and C4 is a center tap of the 325 V. This provides +/-162 V for the switching circuit and transformer T1. R3 and R4 stabilize the center tap and act as bleeders. C5 and C6 are for EMI reduction. Fuse F1, a 3 A Fast-Blow type, provides circuit board protection in case Q1 or Q2 shorts out. Any failure of Q1 or Q2 will happen faster than the fuse can blow.

If a mains voltage of 100 or 110 VAC is selected, it is applied across input pins P1-2 and P1-3. With this connection, DB1 acts as a full-wave doubler rectifier. DB1 produces a nominal 325 V across series-connected C3 and C4 as before.

By means of transformer T2, the Control Section turns transistor Q1 ON and OFF in alternation with Q2. The cycle time is a nominal 40 microseconds. NOTE that Q1 and Q2 are never both ON at the same time. This alternately applies +162 and -162 V across the primary of transformer T1. The resulting a-c voltages across the secondaries of T1 are rectified and averaged in

the Output Section. The longer Q1 and Q2 are ON during each cycle, the higher the d-c output voltages from the Output Section. The width of the ON-pulse thus provides a means of voltage control. This is used by the Control Section for voltage regulation.

Capacitor C8 blocks any d-c bias that might otherwise result from a mismatch between Q1 and Q2. Components R8 and C9 reduce ringing and transient spikes. CR1, R4, C10 and CR2, R6, C11 speed up the turnoff times for Q1 and Q2.

3.4.3 CONTROL SECTION

The Control Section consists of U1, a National DS3632 dual peripheral driver; U2, a Silicon General SG3524 regulating pulse-width modulator; Q4, a 2N3904 transistor; Q3, a 2N3905 transistor; Q5, a Motorola MCR101 SCR; CR5-7,9,10,17,all 1N3600 diodes; CR8, a 1N588 Zener diode; and DB2, an MDA100 bridge rectifier.

This circuit provides drive pulses through transformer T2 that switch Q1 and Q2 ON and OFF. It controls the width of these drive pulses in response to voltage feedback from the Output Section. The circuit provides good voltage regulation of the output voltages. Also, it detects any overcurrent condition and reacts by shutting down the Power Supply.

The nucleus of the Control Section is the circuit U2. It is powered by a nominal +20 V from the bridge rectifier DB2. DB2 is fed, via P1-1 and P1-4, with a nominal 17 VAC at 50-60 Hz from a small transformer, T3. T3 is mounted on the rear panel, refer to Chassis wiring diagram. Circuit U2 produces drive pulses at outputs CA and CB (pins 12 and 13). These are used, via U1 and transformer T2, to turn Q1 and Q2 ON and OFF. The repetition rate of the pulses is established by an oscillator in U2. The frequency is set by the values of R18 and C16 at pins 6 and 7 to a nominal 50 KHz. There are two U2 drive pulses for one cycle of the Q1-Q2 switching circuit. This sets the switching frequency of the power supply to a nominal 25 KHz.

The drive pulses from U2 acts as follows. When CA is low and CB is high, U1 output 5 is turned OFF and output 3 is turned ON. The +20 V applied through R9 drives a current through winding 2-3 of T2. The current is driven in the direction making the dot end of the winding positive. This current in 2-3 induces voltages in windings 7-4 and 6-1, making their respective dot ends positive. The connections to these windings are such that Q2 is turned ON and Q1 remains OFF. The base of Q1 is driven even further negative.

The -162 V applied to Q2 drives current through T1 7-5 and T2 8-5 in the direction making the dot end of 8-5 positive. This regenerative action reinforces the base drive to Q2. Transformer T2 acts as a current transformer. Thus, the base drive current to Q2 is proportional to the T1 primary current through T2 8-5. The current ratio is such that Q2 is assured of being fully ON and out of the linear region.

Q2 is turned OFF again by the blanking pulse within U2 that brings CA high with CB. This turns U1 outputs 3, 5 ON, short circuiting T2 2-3 and turning OFF Q2 drive current at T2 6-1. This short circuit condition lasts for the duration of the blanking pulse, a nominal three microseconds. During this time Q2 and Q1 are both forced to remain OFF. This ensures that Q1 cannot be turned ON until Q2 is OFF. The turn-on time of these transistors is shorter than the turn-off time. Without a long enough blanking pulse, it would be possible for Q1 to turn ON while Q2 was still ON. For example, under conditions of low mains voltage and a compensating maximum pulse width for the switching circuit. This would put a short circuit across the $\pm$ 162 V supply and cause component damage.

The next half of the 20 KHz switching cycle starts with the leading edge of the blanking pulse. Any drive pulse that would turn Q1 ON is inhibited within U2 for the duration of the blanking pulse. At the end of the blanking pulse, the voltage regulation circuitry in U2 is again in control. That circuitry determines when to start the Q1 drive pulse, and CB is brought low. This

turns U1 output 3 OFF and drives current through 2-3 of T2. The current is driven in the direction to turn Q1 ON and hold Q2 OFF. The rest of the action is analogous to that of the first half cycle.

Inputs to the U2 voltage regulation circuit are V+, pin 2, and V-, pin 1. The V+ input is supplied with a nominal +2.5 V reference voltage. The reference voltage is obtained, via R15, R17 and potentiometer R16, from regulated +5 V of U2, pin 16. Pin 16 output is also used as a source of +5 V power for other parts of the circuit.

The V- input is supplied with a nominal +2.5 V of negative feedback, via R32, R27 and R25. This is derived from the regulated +5 V output of the power supply. R28, R29 and C19 provide gain control and phase lag to the feedback amplifier. Lead compensation for the +5 V feedback signal is provided by C28.

If the feedback voltage at V- exceeds the reference voltage at V+, U2 acts to reduce the drive pulse width. This reduces the output voltages of the power supply. If the feedback voltage at V- falls below the reference at V+, the action is the opposite. This regulating action does not appreciably affect the 25 KHz switching frequency, only the ON times of Q1 and Q2.

The variable resistor R16 is adjusted so that the Power Supply output voltage at the +5 V test point is +5.1 V $\pm$0.05 V. This adjustment should be made with both Power Supply output plugs connected to the analyzer, all circuit boards in place, and after the analyzer has had power applied for a period of 10 minutes.

As mentioned previously, the U2 clock frequency is set to a nominal 50 KHz by R18 and C16. The clock signal is a short-duty-cycle pulse that is also used as the blanking pulse. The pulse width is approximately 0.5 microseconds, which is not enough for the blanking pulse in this application.

The output of the clock oscillator circuit is made available at pin 3. The Q3-Q4 circuit connected to this pin is used to stretch the clock/blanking pulse to a nominal three microseconds. This provides blanking protection for Q1 and Q2.

The SCR Q5, Zener diode CR8, and diodes CR6 and CR7 constitute an overcurrent shutdown circuit that functions as follows. A component of the voltage across winding 2-3 of T2 is proportional to the current in winding 8-5. Normally the voltage across winding 2-3 results in less than 7.5 V at the cathode of CR8 via CR6 or CR7. If the rated current in winding 8-5 is exceeded, the voltage at CR8 cathode will exceed 7.5 V and CR8 will conduct.

When CR8 conducts, SCR Q5 is triggered and shorts both sides of winding 2-3 to ground through CR6 and CR7. This holds both Q1 and Q2 OFF, shutting down the power supply indefinitely until the power is turned OFF. When power is turned ON, the supply will function normally if the cause of the shutdown has been removed.

Diodes CR17 and CR5 serve to clip any ringing voltages that appear at winding 2-3 of T2.

3.4.4 OUTPUT SECTION

The Output Section consists of VR1, an LM340T-12 +12 V series regulator; VR2, an LM350K +12 V regulator; DB3, a Varo VJ248X bridge rectifier, CR13 through CR17, all 1N6096 rectifiers; CR12, a 1N9578 6.8V Zener diode; and CR11, a 1N721A 20 V Zener diode.

This section contains rectifier and filter circuits for the four major output voltages of +5, -5, +15 and -15 volts. These circuits are fed with 25 KHz pulse-width modulated power from secondary windings on switching transformer T1.

Also contained in this section is the low-power series regulator, VR1, that provides +12 V for the Display Module. A second regulator, VR2, provides +12 V for the disk drive circuitry. Both low-power regulators are fed from the +15 V supply. The current ratings for these supply voltages are as follows:

VOLTAGE		MAXIMUM CURRENT
+5		20.0 A
-5		12.0 A
+15		1.0 A
-15		1.0 A
+12	CRT	1.5 A
+12	DISK	3.0 A
+5	DISK	1.0 A

DB3 acts as a full-wave bridge rectifier for both the +15 and -15 V supplies. It is fed from secondary windings, 11-10-12, on the switching transformer T1. L1-C23 and L2-C24 act as pulse-averaging and ripple filters for the +15 V and -15 V supplies, respectively. R31 is a bleeder for the -15 V supply. R30 and C20 suppress transient ringing in the secondary.

Series regulator VR1 drops part of the +15 V output to +12 V for the Display Module. C19 provides additional filtering and decoupling for the +12 V.

The two diodes CR13 and CR14 are rectifiers for the +5 V supply. They are each fed from the center tapped secondary windings, on switching transformer T1. The cathodes of the diodes are connected to the L3-C25-C26 pulse-averaging and ripple filter. R33 and C29 suppress transient ringing in the 5 V secondaries.

The -5 V output circuit is the same as the +5 V except for the differences to accomodate opposite polarity.

Zener diodes CR12 and CR11 form a shutdown circuit for over-voltage protection. If the +5 V output voltage rises above +6.8 V, Zener diode CR12 conducts. This causes SCR Q5 to trigger and shuts down the supply. CR11 provides similar overvoltage protection fo the +15 V output. The minus voltages are not protected explicitly but have protection due to the cross regulation with the positive voltages.

The feedback voltage for the Control Section is applied from the +5 V output through phase compensation network R32-C28. The +5 V output is therefore tightly regulated. The other output voltages are regulated, but to a lesser degree than the +5 V output. The +12 V outputs benefit from the additional regulation afforded by the series regulators VR1, VR2.

L5 and C27 provide a second L-C filtering stage for the +5 V supply to the Disk Drive. This reduces noise to the drive via power supply coupling.

3.5 DISK DRIVE REMOVAL

The disk drive is removed by disconnecting the plug-in cables and ground strap, then removing the four mounting screws. Replacement is made in the reverse order from removal. The step-by-step removal procedure is as follows:

a. Remove the power cord and top cover as previously described.

b. Disconnect the two plug-in cables at the rear of the drive. Note the orientation of the cable connectors.

c. Disconnect the ground strap.

d. Tilt the 764 on the rear panel feet. The disk drive is held in place with four screws, two on top and two on the bottom. The bottom screws are reached through access holes in the bottom cover. Remove the two bottom screws.

e. Tilt the 764 back down into its normal bench position. Remove the two top screws. Carefully remove the drive from the chassis.

3.6 SCHEMATICS, BOARD LAYOUTS AND PARTS LISTS

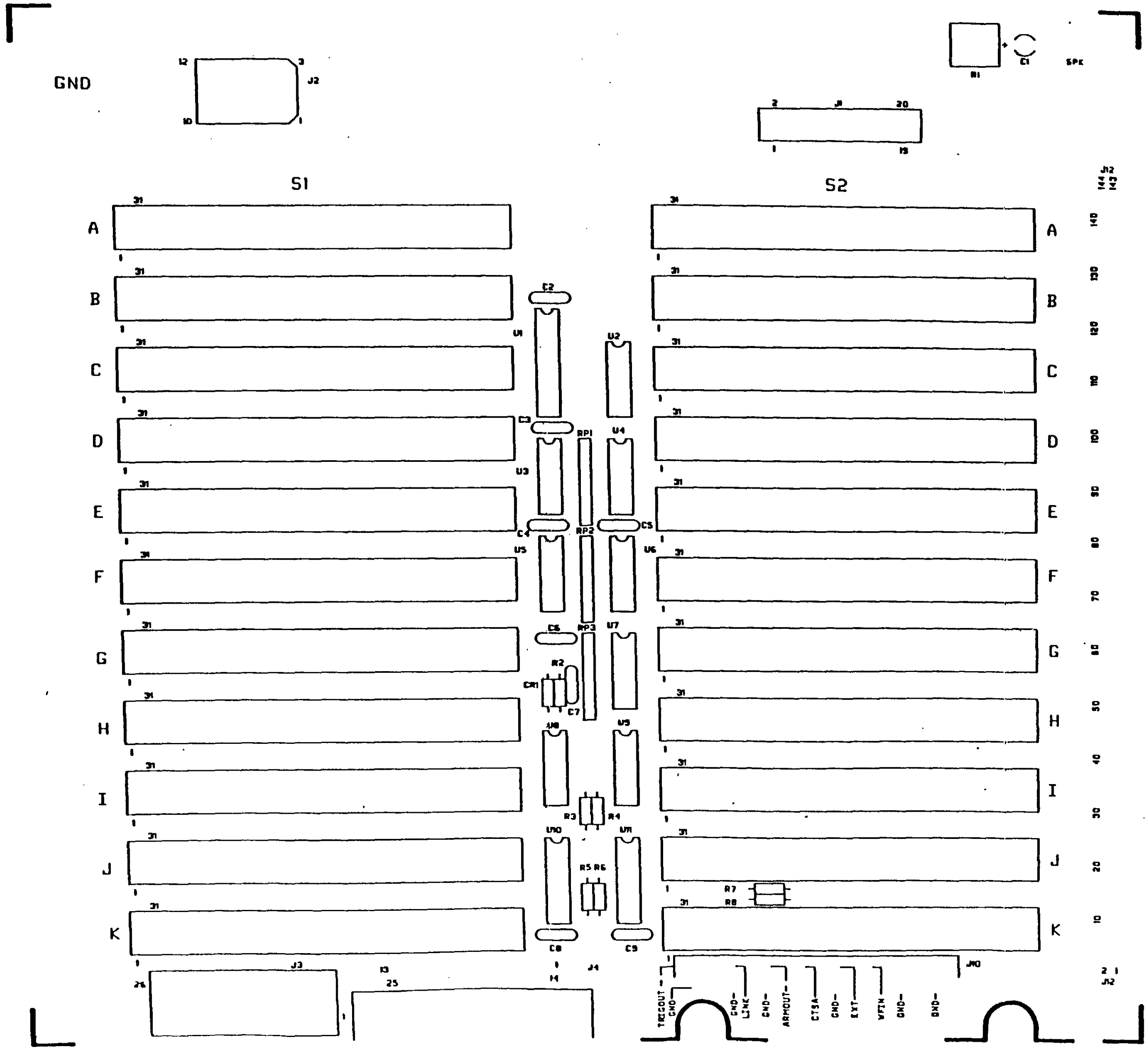
The schematic diagrams, board layouts and parts lists for the Power Supply, Motherboard and Chassis (as applicable) are contained at the end of this section.

PARENT ITEM 143-0123-0090 | CROSS REF ITEM | DESCRIPTION M764 MOTHER BOARD O/S ASSY. ENGR DRAW ECO 477 REV D | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 04 | EFFC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0037	R2 OHM 1/4W 5% CF RES R5		1.000	EA	4C				4/29/81	
	06	110-0005-0041	120 OHM 1/4W 5% CF RES R6		1.000	EA	4C				4/29/81	
	06	110-0005-0045	180 OHM 1/4W 5% CF RES R3		1.000	EA	4C				4/29/81	
	06	110-0005-0049	270 OHM 1/4W 5% CF RES R4		1.000	EA	4C				4/29/81	
	06	110-0005-0065	470 OHM 1/4W 5% CF RES R2 R7 R8		3.000	EA	4C				4/29/81	
	06	110-0203-0001	POT, 5K 3386P-1-502 BOURNS R1		1.000	EA	4C				4/29/81	
	06	110-0308-0001	RN 470 OHM X7 8 PIN SIP RP2		1.000	EA	4C				3/09/82	
	06	110-0309-0001	RN 4.7K OHM X7 8 PIN SIP RP1		1.000	EA	4C				3/04/82	
	06	110-0327-0001	RN 2.2K OHM X7, 8 PIN SIP RP3		1.000	EA	4C				10/22/81	
	06	111-0004-0072	.1 UF 25V CD CAP C2 C3 C4 C5 C6 C7 C8 C9		8.000	EA	4C				4/29/81	
	07	111-0054-0074	1 UF 35V TANT DROP CAP C1		1.000	EA	4C				4/29/81	
	07	112-0204-0001	DIODE 1N3600 1N4148 4149 4150 CR1		1.000	EA	4C				4/29/81	
	06	114-0005-0001	CONN 30PIN DUAL H4210Z1-30 TI S1A S1B S1C S1D S1E S1F S1G S1H S1I S1J S1K S2A S2B S2C S2D S2F S2H S2G S2H S2I S2J S2K		22.000	EA	4C				4/29/81	
	06	114-0054-0002	GAFXCON 09.13.5121 ALLEX J2		1.000	EA	4C				4/29/81	
	06	114-0057-0001	CONN 26 PIN PC MALE HEADER J1		1.000	EA	4C				3/09/82	
	06	115-0003-0001	SOCKET 14PIN U2 U3 U4 U5 U6 U7		7.000	EA	4C				9/27/81	
	06	115-0005-0001	SOCKET 16PIN U10 U11		2.000	EA	4C				4/29/81	
	06	115-0009-0001	SOCKET 40PIN U1		1.000	EA	4C				4/29/81	
	06	123-0123-0001	M764 MOTHER BOARD P.C. BA	ECO 477 REV C	1.000	EA	4C				4/29/81	

PARENT ITEM 143-0123-0001 | CROSS REF ITEM | DESCRIPTION M764 MOTHER BOARD I/S ASSY. ENGR DRAW ECO 477 REV D | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 03 PLANNER

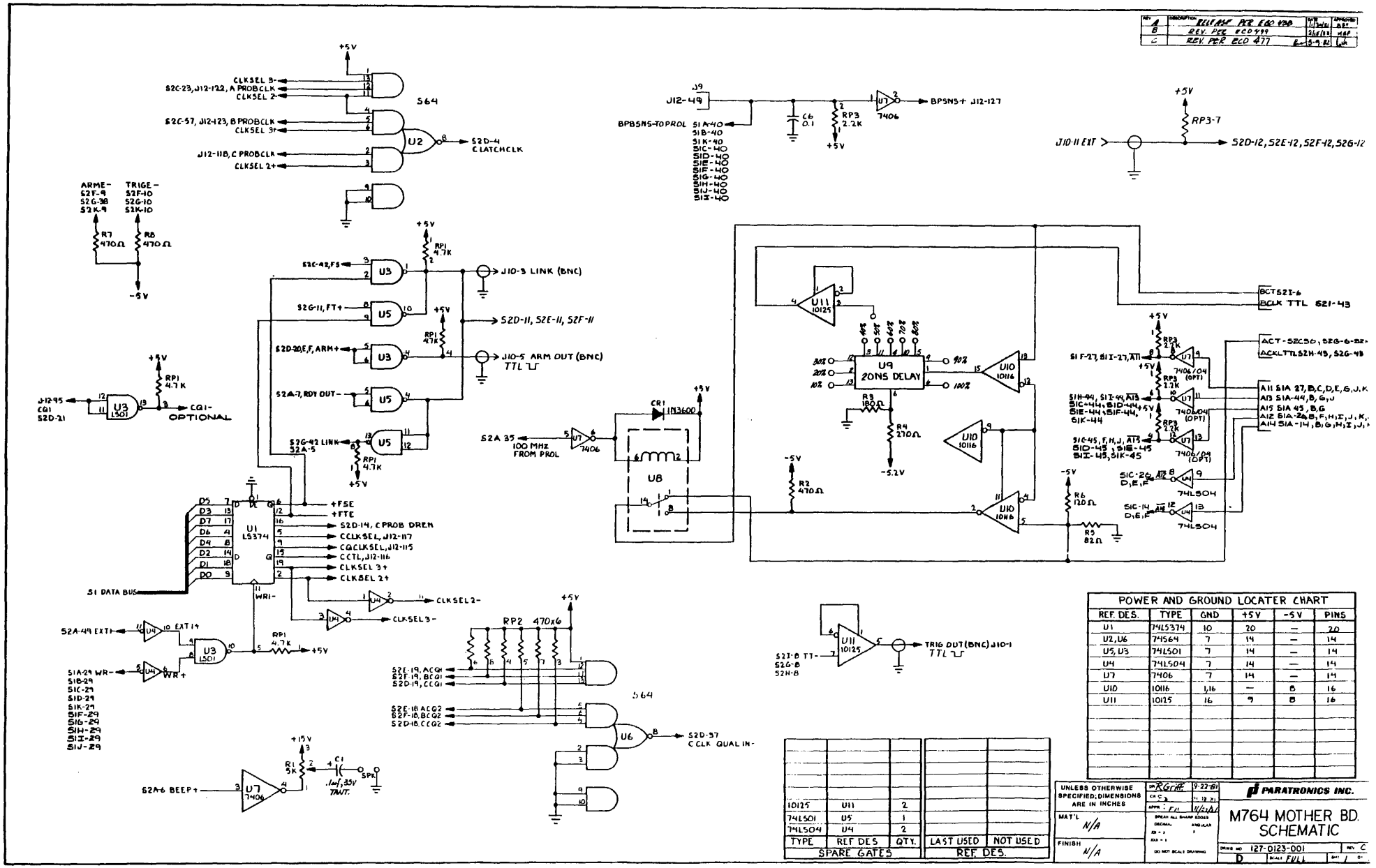
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	112-0306-0002	REED RELAY 191TEICI-5S U3		1.000	EA	4C				10/20/81	
	03	113-0001-0006	I.C. 7406 U7		1.000	EA	4C					
	04	113-0002-0064	I.C. 74S64 U2 U6		2.000	EA	4C					
	04	113-0003-0001	I.C. 74LS01 U3 U5		2.000	EA	4C					
	03	113-0003-0004	I.C. 74LS04 U4		1.000	EA	4C					
	05	113-0003-0374	I.C. 74LS374 U1		1.000	EA	4C					
	04	113-0046-0003	DELAY LINE,LC02021003,PE21182 U9		1.000	EA	4C				8/10/81	
	05	113-0200-0116	I.C. MC10116 U10		1.000	EA	4C					
	03	113-0200-0125	I.C. MC10125 U11		1.000	EA	4C					
	04	114-0022-0002	CONN DBL RT/ANGL STR 2X36 PIN J12		2.000	EA	4C				3/10/82	
	04	114-0043-0001	RECP 90 DEG 25 PIN 206584-2 AM J4	ECO REV	1.000	EA	4C				10/22/81	
	04	143-0123-0090	M764 MOTHER BOARD O/S ASSY.	ECO 477 REV D	1.000	EA	1C					



NICOLET PARATRONICS

126-0123-0201 Rev. B

Motherboard



POWER AND GROUND LOCATER CHART					
REF. DES.	TYPE	GND	+5V	-5V	PINS
U1	74LS374	10	20	—	20
U2, U6	74S64	7	14	—	14
U5, U3	74LS01	7	14	—	14
U4	74LS04	7	14	—	14
U7	7406	7	14	—	14
U10	10116	—	8	16	
U11	10125	16	9	8	16

SPARE GATES				
TYPE	REF DES	QTY.	LAST USED	NOT USED
10125	U11	2		
74LS01	U5	1		
74LS04	U4	2		

REF. DES.

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DR R.GRIFF 9-22-81
CH C.J. 11-12-81
APPR: F.H. 11/12/81
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
DO NOT SCALE DRAWING

PARATRONICS INC.

M764 MOTHER BD. SCHEMATIC

DRWG NO 127-0123-001 REV C
D SCALE FULL SHT 1 OF 1

PARENT ITEM 143-0122-0001 | CROSS REF ITEM | DESCRIPTION M764 POWER SUPPLY I/S ASSY. ENGR DRAW ECO 635 REV J | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	110-0009-0031	47 OHM 1W 5% CF RES R33		1.000	EA	4C				10/14/81	
	03	110-0011-0045	180 OHM 2W MF/CF RESISTOR R31		1.000	EA	4C				8/09/82	
	03	110-0024-0015	10 OHM 5% 4W RESISTOR R34		1.000	EA	4C				8/09/82	
	06	110-0103-0001	THERMISTOR,MIDWEST COMP. 20754 +1		1.000	EA	4C				1/14/82	
	07	111-0012-0065	.01MF +80% -20%/GMF 1KDVC CAP C29		1.000	EA	4C				10/21/81	
	05	111-0213-0143	CAP. 470 UF,50V ELECT.RADIAL C12 C23 C24 C32	ECO 651 REV -	4.000	EA	4C				7/15/82	
	03	111-0217-0155	1000 MF 200V ELECT AC CAP C3 C4		2.000	EA	4C					
	05	112-0027-0002	VOLTAGE REG. LM340T-5 VR1	ECO 550 REV A	1.000	EA	4C				3/25/81	
	03	112-0075-0001	VOLTAGE REG. LM350K VR2	ECO 550 REV A	1.000	EA	4C					
	06	112-0110-0001	TRANSISTOR MJE13007 Q1 Q2		2.000	EA	4C				3/25/81	
	06	112-0206-0002	DIODE IN6096 TRW CR13 CR14 CR15 CR16		4.000	EA	4C				7/29/82	
	05	112-0252-0001	RECTIFIER VJ149X VARO D83		1.000	EA	4C				3/25/81	
	03	112-0253-0001	RECTIFIER VH649 VARO D81		1.000	EA	4C					
	03	112-0361-0005	FUSE, 3A 250V FAST F1	ECO 661 REV -	1.000	EA	4C				10/13/82	
	03	112-0363-0001	INSULATOR 43-03-2AP THERMALO		1.000	EA	4C				4/07/81	
	05	113-0049-0001	I.C. SG3524 U2		1.000	EA	4C				3/25/81	
	05	113-0050-0001	I.C. DS3632		1.000	EA	4C				3/25/81	
	06	117-0006-0001	TEST JACK RED 402-102 MHS +15 +5		2.000	EA	4C				8/27/81	
	06	117-0006-0002	TEST JACK BLK 402-103 MHS GND		1.000	EA	4C				8/27/81	
	06	117-0006-0003	TEST JACK BLUE 402-105 MHS -15 -5		2.000	EA	4C				8/27/81	
	05	117-0013-0001	BELLEVILLE WASHER 5306-4-15 1 EA J1 1 EA J2 1 EA VR1		3.000	EA	4C				3/25/81	

PARENT ITEM 143-0122-0001 | CROSS REF ITEM | DESCRIPTION "754 POWER SUPPLY I/S ASSY. ENGR DRAW ECO 635 REV J | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	117-0020-0001	SPACER KEYSTONE 3143 1 EA Q1 1 EA Q2		2.000	EA	4C				3/25/81	
	06	117-0021-0001	SHOULDER BUSHING KEYSTONE 3052 1 EA Q1 1 EA Q2		2.000	EA	4C				3/25/81	
	06	117-0032-0001	BUSHING 951547F012 MOT CR13 CR14 CR15 CR16		4.000	EA	4C				3/25/81	
	06	117-0112-0001	SIL-PAD 7403.09ER.20 BERQUIST		4.000	EA	4C				11/04/81	
	06	117-0133-0001	WASHER THERMALOX MTG 1 EA Q1 1 EA Q2		2.000	EA	4C				3/25/81	
	03	117-0136-0001	TERM RING 22-13AWG #10 LUG 2EA ON C3 2EA ON C4		4.000	EA	4C				1/14/82	
	03	117-0141-0001	#6 TINNERMAN CLP,C10132-632-67 2 EA.FOR CAP MTG. CLAMPS.		2.000	EA	4C				9/23/82	
	07	117-0150-0001	TIE WRAP PLT 1.5M-CP		4.000	EA	4C				3/25/81	
	03	117-0204-0001	CAP.MTG.CLAMP MALLORY		2.000	EA	4C				8/16/82	
	03	117-0210-0001	SPACER .120 I.D.X3/16 OD.X.125 INSTALL IN HEAT SINK HOLES WHERE SCREWS FASTEN VR2 TO PCB		2.000	EA	4C				9/23/82	
	06	117-0325-0001	#2 INTERNAL TOOTH LOCK WASHER 1 EA Q1 1 EA Q2		2.000	EA	4C					
	05	117-0827-0001	#6 INT. TOOTH LOCKWASHER STL/C TO MOUNT Q91 AND Q93 FROM HEAT SINK TO PCB		2.000	EA	4C				1/14/82	
	03	117-0829-0001	#10 INT TOOTH LOCKWASHER 1 EA CR13 1 EA CR14 1 EA CR15 1 EA CR16		4.000	EA	4C				3/25/81	
	06	117-0901-0001	2-56 HEX NUT STL/CAD 1 EA Q1 1 EA Q2		2.000	EA	4C				3/25/81	
	04	117-0902-0003	4-40 KEP NUT EXT TOOTH STL/CAD 2 EA FOR VR2 1 EA L1 1 EA L2 1 EA J-1		5.000	EA	4C				8/15/82	
	06	117-0903-0001	4-40 1/4" AF HEX NUT STL/CAD TO MOUNT Q91 AND Q93 FROM HEAT SINK TO PCB		2.000	EA	4C				1/14/82	

PARENT ITEM 143-0122-0001 | CROSS REF ITEM | DESCRIPTION M764 POWER SUPPLY I/S ASSY. PWR DRAW ECO 685 REV J | BATCH QTY 1 | EFFEC 12/08/82 | ITEM TYPE 1 | UNIT MEAS EA | LOW LEVEL 02 | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	117-0903-0003	6-32 HEX NUT KEPS EXT TOOTH 4 EA TO MOUNT CAP MTG.CLAMPS TO HEAT SINK.		4.000	EA	4C				9/23/82	
	05	117-0903-0004	6-32 HEX NUT STANLESS STL 1 EA L3 1 EA L4		2.000	EA	4C				3/25/81	
	06	117-0906-0001	10-32 HEX NUT STL/CAD 1 EA CR13 1 EA CR14 1 EA CR15 1 EA CR16		4.000	EA	4C				3/25/81	
	06	117-1102-0009	2-56X3/8 PHMS PHILLIPS CAD 1 EA J1 1 EA J2		2.000	EA	4C				10/14/81	
	06	117-1202-0005	4-40X3/8 PHMS PHILLIPS STL/CAD 1 EA VR1		1.000	EA	4C				3/25/81	
	06	117-1202-0007	4-40X1/2 PHMS PHILLIPS 2 EA VR2		2.000	EA	4C				8/27/81	
	03	117-1202-0017	4-40X1 1/4 PHMS PHILLIPS STL/Z 1 EA L1 1 EA L2		2.000	EA	4C				11/04/81	
	06	117-1306-0005	6-32X3/8 SEMS PH PHIL INT 2 EA TO MOUNT HEAT SINK TO BOARD		2.000	EA	4C				8/27/81	
	03	117-1306-0009	6-32X5/8 SEMS PHMS PH INT 1 EA DR1 1 EA DR3		2.000	EA	4C				8/27/81	
	03	118-0061-0062	#18 7x6 STR.WIRE-VINYL BLK 3.5 TO CONNECT 1000 MF CAPACITORS TO POWER SUPPLY PCB.		2.000	EA	4C				1/18/82	
	03	118-0061-0065	#18 7 X 6 STR.WIRE-VINYL RED 3.5 TO CONNECT 1000 MF CAPACITORS TO POWER SUPPLY PCB.		2.000	EA	4C				1/18/82	
	03	121-0029-0001	INDUCTOR 560 MH RENCO L1 L2		2.000	EA	4C					
	03	121-0034-0001	INDUCTOR, 210H L3 L4	ECO 661 REV A	2.000	EA	4C				8/09/82	
	05	122-0004-0001	WASHER FIBRE	ECO 150 REV A	2.000	EA	4C				3/25/81	
	03	122-0079-0001	HEAT SINK M764 POWER SUPPLY	ECO 635 REV C	1.000	EA	4C					
	03	124-0031-0004	M764 AC POWER PLUG	ECO 421 REV A	1.000	EA	1C					
	03	124-0032-0003	M764 12V POWER CABLE	ECO 410 REV A	1.000	EA	1C				10/14/81	
	03	124-0033-0003	M764 DC POWER PLUG ASSY	ECO 561 REV B	1.000	EA	1C					
	03	124-0303-0001	M764 AUX POWER PLUG ASSY	ECO 703 REV C	1.000	EA	1C					
	03	143-0122-0001	M764 POWER SUPPLY I/S ASSY.	ECO 685 REV J	1.000	EA	1C				3/25/81	

PARENT ITEM 143-0122-0090 | CROSS REF ITEM | DESCRIPTION M764 POWER SUPPLY O/S ASSY. ENGR DRAW ECO 695 REV J | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 03 PLANNER

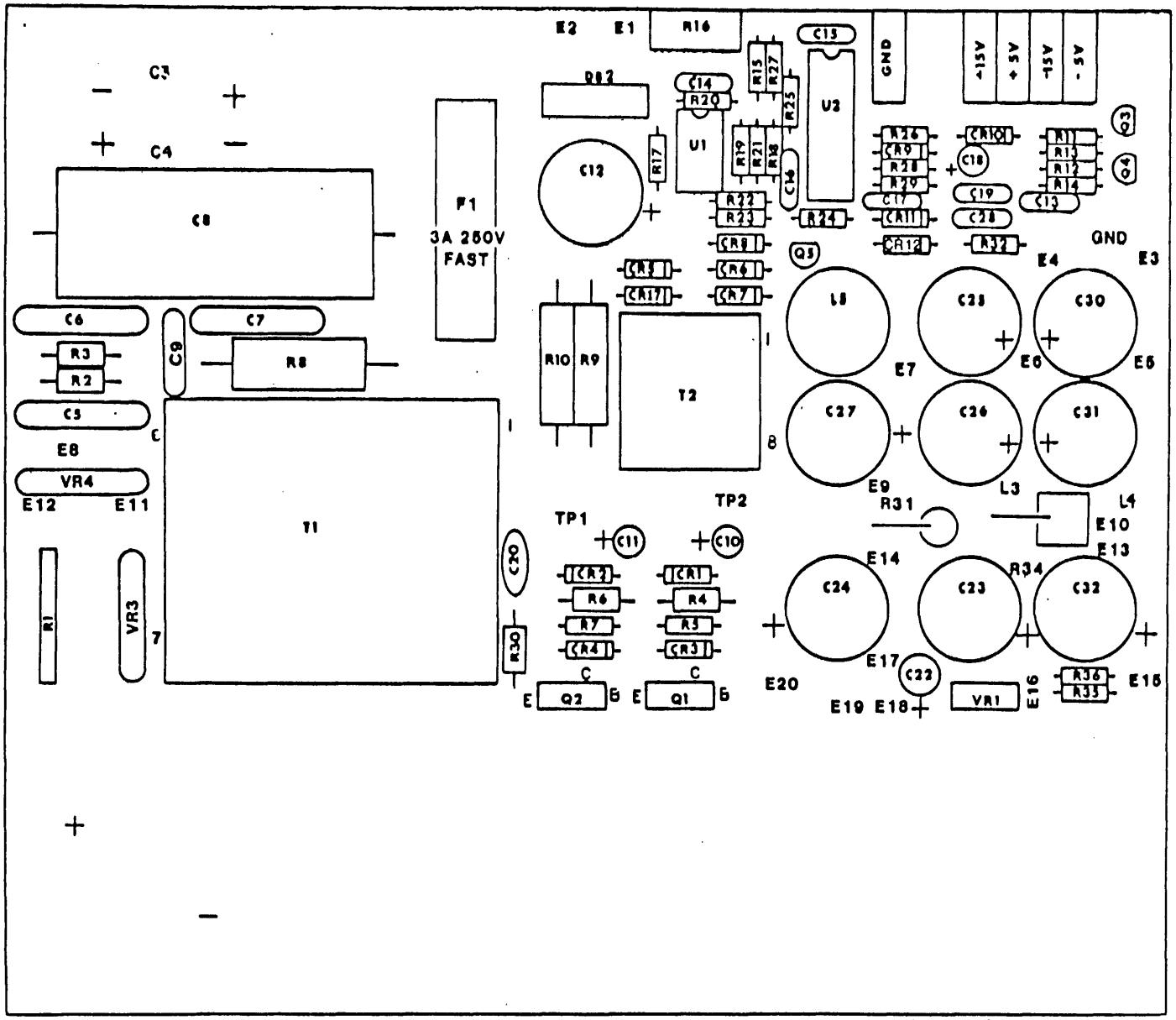
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	110-0003-0290	243 OHM 1/4W 1% MF RES R35		1.000	EA	4C				6/29/82	
	04	110-0004-0070	2.0K 1/4W,2% CF RES. R13 R36		2.000	EA	4C				6/29/82	
	06	110-0005-0039	100 OHM 1/4W 5% CF RES R22 R5 R7		3.000	EA	4C				3/25/81	
	07	110-0005-0047	220 OHM 1/4W 5% CF RES R15 R17		2.000	EA	4C				3/25/81	
	05	110-0005-0063	1K OHM 1/4W 5% CF RES R21 R24		2.000	EA	4C				3/25/81	
	06	110-0005-0079	2K OHM 1/4W 5% CF RES R13 R23		2.000	EA	4C				8/27/81	
	07	110-0005-0079	4.7K OHM 1/4W 5% CF RES R19 R20		2.000	EA	4C				3/25/81	
	06	110-0005-0086	9.1K OHM 1/4W 5% CF RES R25		1.000	EA	4C				3/25/81	
	06	110-0005-0087	10K OHM 1/4W 5% CF RES R11 R12 R14		3.000	EA	4C				3/25/81	
	06	110-0005-0091	15K OHM 1/4W 5% CF RES R27 R29		2.000	EA	4C				3/25/81	
	06	110-0005-0095	22K OHM 1/4W 5% CF RES R32		1.000	EA	4C				3/25/81	
	06	110-0005-0107	68K OHM 1/4W 5% CF RES R23		1.000	EA	4C				3/25/81	
	05	110-0005-0111	100K OHM 1/4W 5% CF RES R26		1.000	EA	4C				3/25/81	
	07	110-0007-0007	4.7 OHM 1/2W 5% CF RES R4 R6		2.000	EA	4C				3/25/81	
	06	110-0007-0031	47 OHM 1/2W 5% CF RES R30		1.000	EA	4C				3/25/81	
	07	110-0007-0119	220K OHM 1/2W 5% CF RES R2 R3		2.000	EA	4C				3/25/81	
	06	110-0009-0055	470 OHM 1W 5% CF RES R10 R9		2.000	EA	4C				3/25/81	
	07	110-0015-0033	56 OHM 2W 5% CF RES R8		1.000	EA	4C				3/25/81	
	06	110-0104-0001	MOVISTOR,130VRMS V130LA10A GE VR4		1.000	EA	4C				7/29/82	
	06	110-0105-0001	MOVISTOR, 275VRMS V275LA15A GE VR3		1.000	EA	4C				7/29/82	
	06	110-0200-0001	POT, 20% OHM X201R251E CTS R15		1.000	EA	4C				3/25/81	

PARENT ITEM 143-0122-0090 | CROSS REF ITEM | DESCRIPTION 4764 POWER SUPPLY D/S ASSY. ENGR DRAW ECO 635 REV J | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	111-0012-0038	180 PF 1KV CD CAP C15		1.000	EA	4C				3/25/81	
	06	111-0012-0050	.001 UF 1KV CD CAP C20		1.000	EA	4C				8/09/82	
	07	111-0012-0062	.0047 UF 1KV CD CAP C7		1.000	EA	4C				3/25/81	
	07	111-0012-0066	.01MF +80% -20%/SMF 1KDVC CAP C5 C6		2.000	EA	4C				7/29/82	
	04	111-0025-0183	100JPF 500V MICA CAP C9	ECO 661 REV-	1.000	EA	4C				9/14/82	
	06	111-0050-0095	10 UF 6V TANT DROP CAP C10 C11		2.000	EA	4C				3/25/81	
	07	111-0204-1155	1000 UF 10V ELEC RAD UC CAP C25 C26 C27 C30 C31		5.000	EA	4C				12/07/82	
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C18 C24		2.000	EA	4C				3/25/81	
	06	111-0313-0072	.1 UF C620C104K CD RADIAL CAP C14 C15 C19		3.000	EA	4C				3/25/81	
	07	111-0413-0063	.01 UF 50V MYLAR CAP C17 C16 C28		3.000	EA	4C				3/25/81	
	04	111-0417-0096	10 UF 200V MYLAR CAP C8		1.000	EA	4C					
	06	112-0100-0001	TRANSISTOR 2N3704 Q4		1.000	EA	4C				3/25/81	
	06	112-0101-0001	TRANSISTOR 2N3905 Q3		1.000	EA	4C				3/25/81	
	05	112-0200-0003	RECTIFIER 40A 100A D16		1.000	EA	4C				3/25/81	
	07	112-0204-0001	DIODE 1N3600 1N4148 4149 4150 CR1 CR10 CR17 CR2 CR5 CR6 CR7 CR9		8.000	EA	4C				8/27/81	
	04	112-0216-0001	DIODE ZENER 1N957B CR12		1.000	EA	4C				3/25/81	
	04	112-0217-0001	DIODE ZENER 1N721A CR11		1.000	EA	4C				3/25/81	
	06	112-0220-0001	DIODE ZENER 1N960B 1N757A CR4		1.000	EA	4C				1/14/82	
	04	112-0223-0001	RECTIFIER,1N4937,1N4946,1N5619 CR3 CR5		2.000	EA	4C				8/09/82	
	07	112-0241-0001	TRANSISTOR MCR101 2N5060 Q5		1.000	EA	4C				3/25/81	
	05	115-0001-0001	SOCKET 3 PIN U1		1.000	EA	4C				3/25/81	

PARENT ITEM 143-0122-0090 | CROSS REF ITEM | DESCRIPTION M764 POWER SUPPLY O/S ASSY. ENGR DRAW ECO 695 REV J | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 03 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	115-0005-0001	SOCKET 16PIN U2		1.000	EA	4C				3/25/81	
	10	117-0030-0001	TERMINAL 120-1032-04 CAMDION TP1 TP2		3.000	EA	4C				8/09/82	
	15	117-0117-0001	FUSE CLIP 102048 LITTLFUSE F1		2.000	EA	4C				3/25/81	
	06	121-0010-0001	TRANSFORMER DRIVE T2	ECO 272 REV A	1.000	EA	4C				3/25/81	
	04	121-0030-0001	TRANSFORMER M764 MAIN T1	ECO 661 REV D	1.000	EA	4C					
	04	121-0031-0001	INDUCTOR 39 MH RENCO L5		1.000	EA	4C					
	04	126-0122-0001	ALLADIN POWER SUPPLY PCB	ECO 695 REV C	1.000	EA	4C				3/25/81	



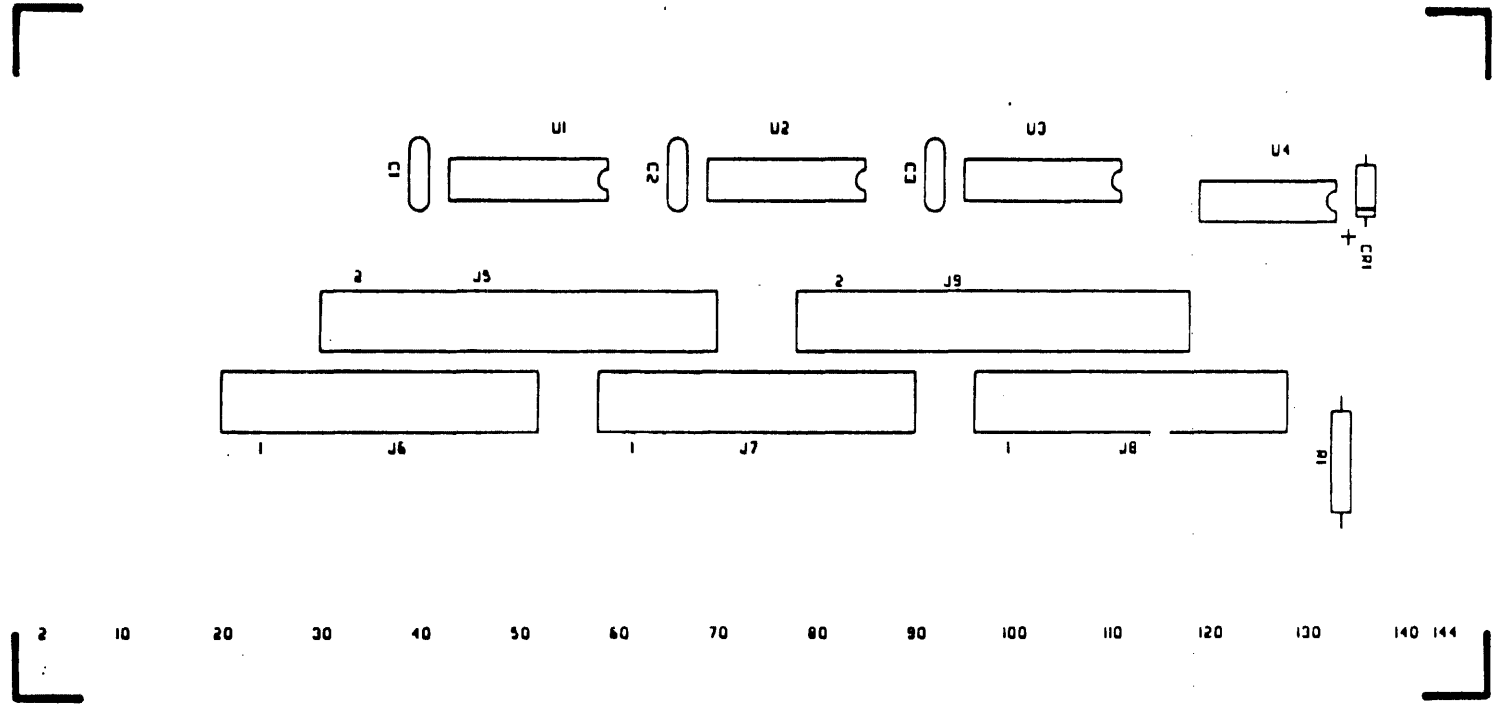
Power Supply

NICOLET PARATRONICS

126-0122-0201 Rev. C

PARENT ITEM 143-0124-0001 | CROSS REF ITEM | DESCRIPTION M764 DAUGHTER BD. ASSY. ENGR DRAW ECO 396 REV A | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

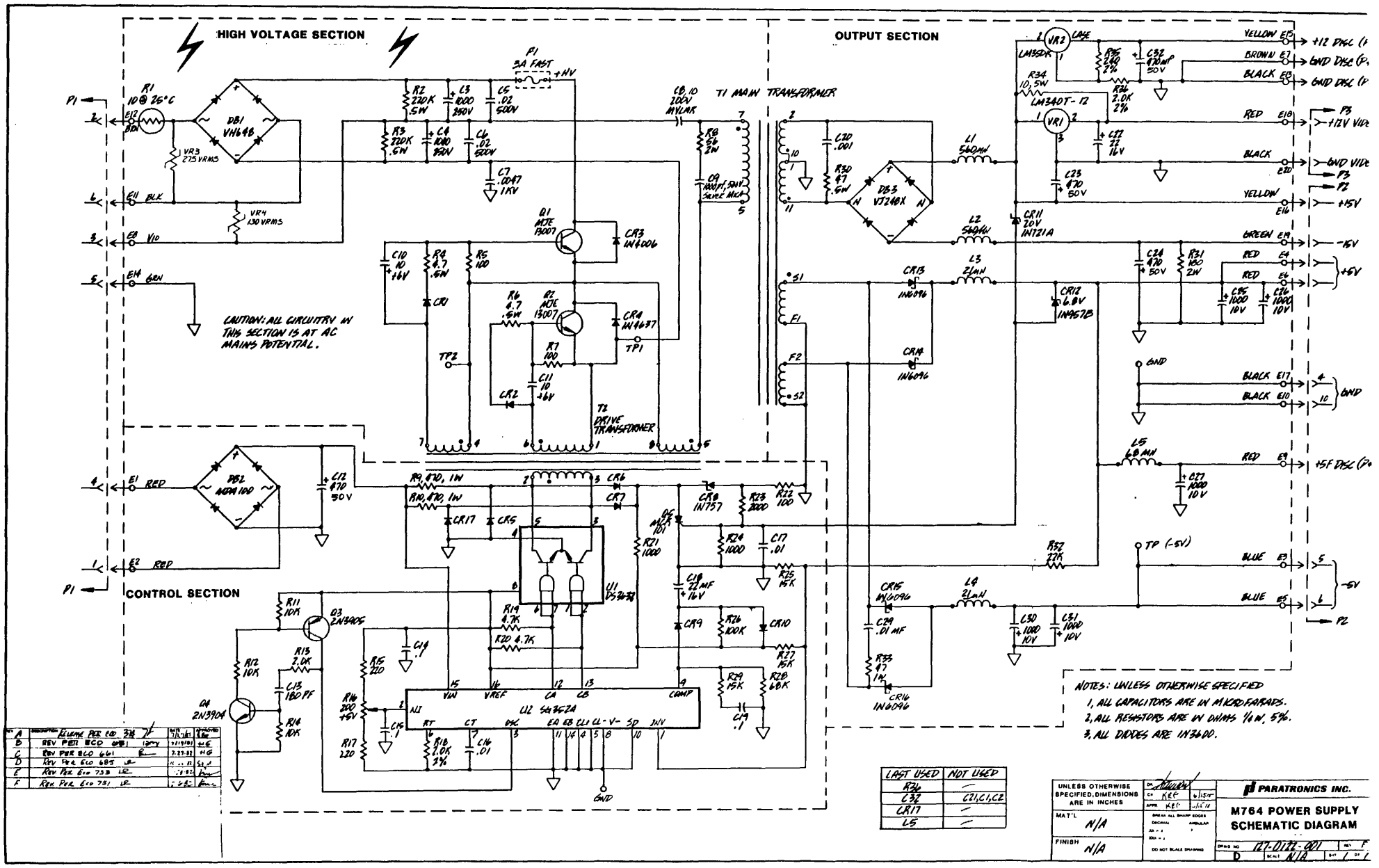
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	EFFECTIVE DATES TO
	05	110-0009-0031	47 OHM 1/4 5% CF RES R1-INSTALL ON CIRCUIT SIDE OF BOARD.		1.000	EA	4C					
	06	111-0004-0072	.1 UF 25V CD CAP C1 C2 C3		3.000	EA	4C					
	07	112-0204-0001	DIODE 1N3600 1N4148 4149 4150 CR1		1.000	EA	4C					
	04	112-0308-0001	REED RELAY 171TE1A1-55 SIGMA		1.000	EA	4C				10/21/81	
	05	113-0200-0116	I.C. MC10116 U1 U2 U3		3.000	EA	4C					
	04	114-0037-0001	PC HEADER 26 PIN 609-2657 ANSY J6 J7 J8		3.000	EA	4C					
	04	114-0039-0001	PC HEADER 34 PIN 609-3457 ANSY J5 J9		2.000	EA	4C					
	04	126-0124-0001	M764 DAUGHTER BD PC FAB	ECO 396 REV A	1.000	EA	4C					



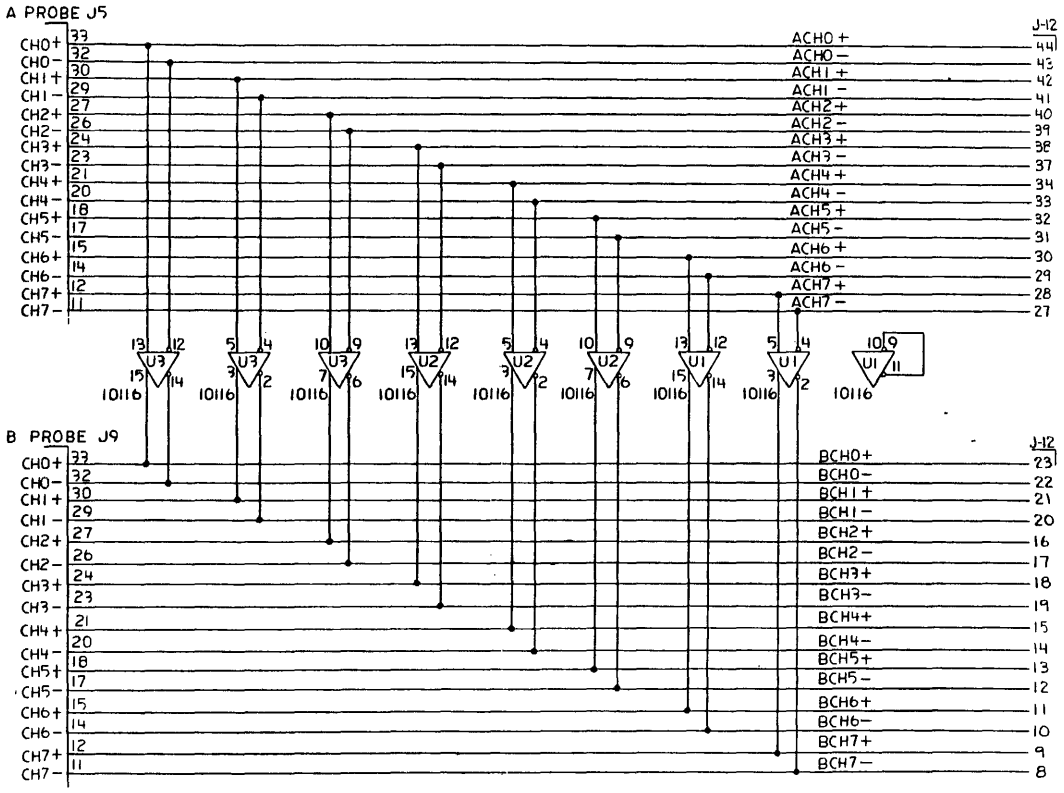
Daughterboard

NICOLET PARATRONICS

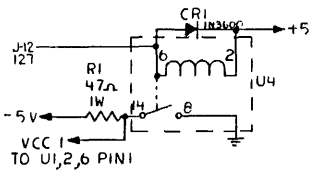
126-0124-0201 Rev. A


HIGH VOLTAGE SECTION
OUTPUT SECTION
CONTROL SECTION
T1 MAIN TRANSFORMER
T2 DRIVE TRANSFORMER
CAUTION: ALL CIRCUITRY IN THIS SECTION IS AT AC MAINS POTENTIAL.
P1
3A FAST
+HV
DB1 VH648
DB2 40PM 100
DB3 VJ240X
VR1 LM340T-12
VR2 LM350K
VR3 275 VRMS
VR4 130 VRMS
R1 10 @ 25°C
R2 220K .5W
R3 220K .5W
R4 1000 250V
R5 .02 500V
R6 56 2W
R7 100
R8 4.7 .5W
R9 4.7 .5W
R10 470, 1W
R11 10K
R12 10K
R13 2.0K
R14 10K
R15 220
R16 200 +5V
R17 220
R18 2.0K 2%
R19 4.7K
R20 4.7K
R21 1000
R22 100
R23 2000
R24 1000
R25 15K
R26 100K
R27 15K
R28 60K
R29 15K
R30 47 .5W
R31 100 2W
R32 2.0K 2%
R33 47 1W
R34 10, 5W
R35 240 2%
R36 22K
C1 .1
C2 .001
C3 1000 250V
C4 1000 250V
C5 .02 500V
C6 .02 500V
C7 .0047 1KV
C8,10 200V MYLAR
C9 1000pf, 5KV SILVER MICA
C10 10 16V
C11 10 16V
C12 470 50V
C13 180 PF
C14 .01
C15 1000 10V
C16 .1
C17 .01
C18 22MF 16V
C19 .1
C20 .001
C21,C1,C2
C22 22 16V
C23 470 50V
C24 470 50V
C25 1000 10V
C26 1000 10V
C27 1000 10V
C28 22K
C29 .01 MF
C30 1000 10V
C31 1000 10V
C32 470MF 50V
L1 560MH
L2 560MH
L3 2MH
L4 2MH
L5 4.8 MH
Q1 MJE 15007
Q2 MJE 15007
Q3 2N3905
Q4 2N3904
Q5 MCR 101
U1 DS3632
U2 SG3524
CR1
CR2
CR3 IN4006
CR4 IN4697
CR5
CR6
CR7
CR8 IN757
CR9
CR10
CR11 20V IN121A
CR12 6.8V IN4578
CR13 IN6096
CR14 IN6096
CR15 IN6096
CR16 IN6096
CR17
TP1
TP2
TP (-5V)
GND
E1 RED
E2 RED
E3 BLU
E4 BLK
E5 GRN
E6 YEL
E7 BRN
E8 BLK
E9 RED
E10 BLK
E11 BLK
E12 RED
E13 BLU
E14 YEL
E15 GRN
E16 BLK
E17 BLK
E18 RED
E19 BLK
E20 BLK
YELLOW E6 → +12 DISC (
BROWN E7 → GND DISC (P
BLACK E8 → GND DISC (P
RED E18 → P3 → +12V VIDE
BLACK E20 → GND VIDE
P3
YELLOW E16 → P2 → +15V
GREEN E19 → -16V
RED E4 → +6V
RED E4 → +6V
BLACK E17 → 4
BLACK E10 → 10 → GND
RED E9 → +5F DISC (P
BLUE E3 → 5
BLUE E5 → 6 → -6V
P2
NOTES: UNLESS OTHERWISE SPECIFIED
1, ALL CAPACITORS ARE IN MICROFARADS.
2, ALL RESISTORS ARE 1/4 OHMS 1/4 W, 5%.
3, ALL DIODES ARE IN3600.
LAST USED
NOT USED
R36
C32
CR17
L5
C27,C1,C2
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
PARATRONICS INC.
M764 POWER SUPPLY SCHEMATIC DIAGRAM
DRWG NO 127-0122-001
REV F
SCALE N/A
SHT 1 OF 1

REV	DESCRIPTION	DATE
A	RELEASE PER ECO 428	11/81
B	PER ECO 635 LR	9-11-81



U9	U1, U2, U3, U4
ER1	
R1	
C3	
U4	
LAST USED	NOT USED
REF. DESIGNATORS	



NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE WIRE LIST FOR J6, J7, J8 INTEL CONNECTIONS.
2. THIS SCHEMATIC TO BE USED WITH 126-0124-0001 REV "A" "B" PC FAB.

POWER AND GROUND LOCATER CHART

REF DES	TYPE	GND	+5V	-5V	PINS
U1, U2, U3	10116	1, 16	—	8	16

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	DR RG 9-2-81	PARATRONICS INC.
MAT'L N/F	CK [illegible] 9-9-81	M764 DAUGHTER BD SCHEMATIC
FINISH N/A	APPD [illegible] 9/9/81	DRWG NO 127-0124-001 REV B
BREAK ALL SHARP EDGES	DECIMAL ANGULAR	SIZE D SCALE NONE SHT 1 OF 1
DO NOT SCALE DRAWING		

KEYBOARD AND FRONT PANEL

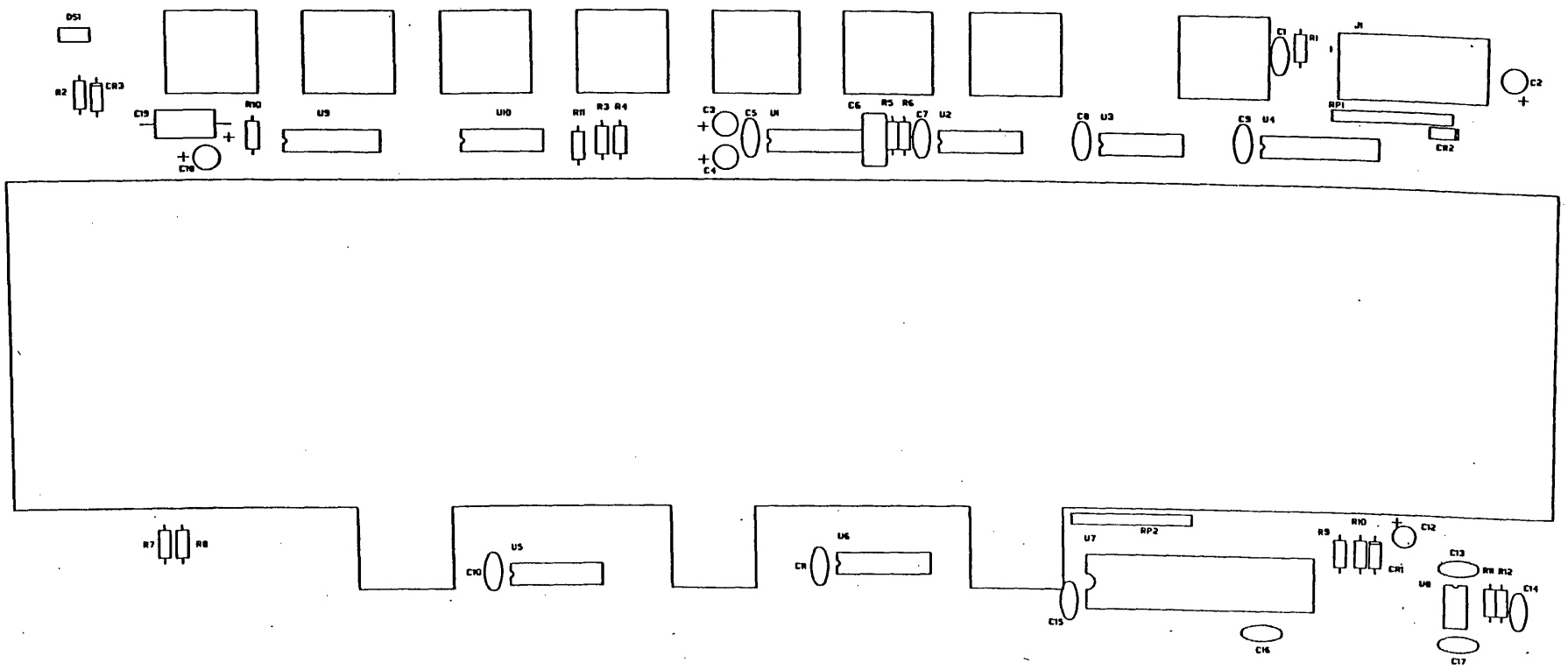
SECTION 4: KEYBOARD AND FRONT PANEL

PARENT ITEM 143-0121-0001 | CROSS REF ITEM | DESCRIPTION ALLADIN KEYBOARD ASSY I/S ENGR DRAW ECO 612 REV F | BATCH QTY 1 EFFEC 1/04/83 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 02 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C2		1.000	EA	4C				1/14/82	
	03	112-0378-0001	KEY ARRAY SWITCH HI-TEK		1.000	EA	4C				2/12/81	
	04	112-0379-0001	KEY SWITCH HI-TEK		8.000	EA	4C				8/27/81	
	03	113-0003-0033	I.C. 74LS33 U3		1.000	EA	4C				8/27/81	
	03	113-0003-0074	I.C. 74LS74 U2		1.000	EA	4C				2/12/81	
	03	113-0003-0132	I.C. 74LS132 U10		1.000	EA	4C				6/07/82	
	06	113-0003-0138	I.C. 74LS138 U5 U6		2.000	EA	4C				2/12/81	
	05	113-0019-0001	I.C. NE555N SIG U8		1.000	EA	4C				2/12/81	
	03	113-0062-0002	PROM 6348-1 M764 KEYBOARD U4 U4 PROGRAM THIS PROM WITH NPC BLANK PROM NUMBER 113-0062-0000.	ECO REV	1.000	EA	4C				8/27/81	
	03	113-0073-0001	I.C. 9602 FAIRCHILD U1 U9		2.000	EA	4C				6/07/82	
	03	113-0074-0001	I.C. MSM 3914A OKI U7		1.000	EA	4C				2/12/81	
	03	124-0024-0002	M764 KEYBD. INTERFACE CBL. ASSY.	ECO 487 REV C	1.000	EA	4C				10/13/81	
	03	143-0121-0090	ALLADIN KEYBOARD ASSY O/S	ECO 612 REV F	1.000	EA	1C				2/12/81	

PARENT ITEM 143-0121-0090 | CROSS REF ITEM | DESCRIPTION ALLADIN KEYBOARD ASSY O/S ENGR DRAW ECO 612 REV F | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE I UNIT MEAS EA | LOW LEVEL 03 PLANNER

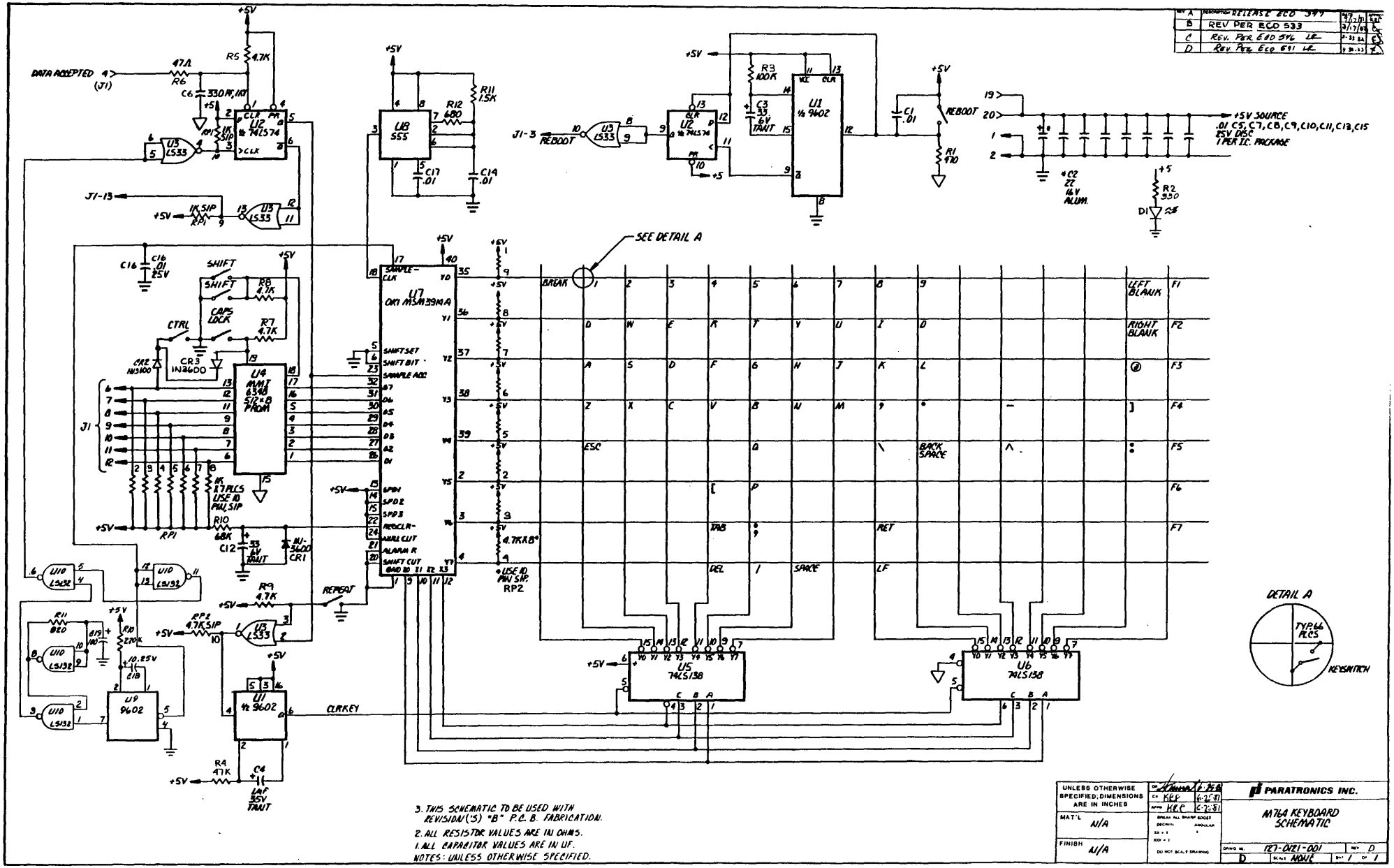
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0031	47 OHM 1/4W 5% CF RES R6		1.000	EA	4C				8/27/81	
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R2		1.000	EA	4C				2/12/81	
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R1		1.000	EA	4C				9/15/81	
	06	110-0005-0059	680 OHM 1/4W 5% CF RES R12		1.000	EA	4C				2/12/81	
	04	110-0005-0061	820 OHM 1/4W 5% MF RES R11 BETWEEN U10 AND R3		1.000	EA	4C				6/07/82	
	05	110-0005-0067	1.5K OHM 1/4W 5% CF RES R11 BETWEEN U8 AND R12		1.000	EA	4C				2/12/81	
	07	110-0005-0079	4.7K OHM 1/4W 5% CF RES R5 R7 R8 R9		4.000	EA	4C				9/17/81	
	04	110-0005-0103	47K OHM 1/4W 5% CF RES R4		1.000	EA	4C				2/12/81	
	06	110-0005-0107	68K OHM 1/4W 5% CF RES R10 BETWEEN CR1 AND R9		1.000	EA	4C				9/15/81	
	06	110-0005-0111	100K OHM 1/4W 5% CF RES R3		1.000	EA	4C				2/12/81	
	04	110-0005-0119	220K 1/4W 5% MF RES R10 NEAR C19		1.000	EA	4C				6/29/82	
	05	110-0314-0001	RN 4.7K OHM X9 10 PIN SIP RP2		1.000	EA	4C				8/27/81	
	04	110-0319-0001	RN 1K OHM X9, 10 PIN SIP RP1		1.000	EA	4C				8/27/81	
	06	111-0004-0065	.01 UF 25V CO CAP C1 C5 C7 C8 C9 C10 C17 C11 C13 C15 C16 C14		12.000	EA	4C				9/17/81	
	06	111-0012-0039	330 PF 1KV CO CAP C6		1.000	EA	4C				9/17/81	
	05	111-0050-0107	33 UF 6V TANT DROP CAP C3 C12		2.000	EA	4C				8/27/81	
	07	111-0054-0074	1 UF 35V TANT DROP CAP C4		1.000	EA	4C				2/12/81	
	04	111-0125-0123	1000F 6.3V ELECT AXIAL CAP C17		1.000	EA	4C				6/07/82	
	05	111-0209-0096	10 UF 25V ELECT RADIAL CAP C13		1.000	EA	4C				6/07/82	
	07	112-0204-0001	DIODE 1N4148 4149 4150 CR1 CR2 CR3		3.000	EA	4C				4/28/82	
	04	126-0121-0001	M764 KEY CARD FG EA	ECO 546 REV C	1.000	EA	4C				9/15/81	



NICOLET PARATRONICS

126-0121-0201 Rev. B

Keyboard



REV	DESCRIPTION	DATE	APPD
A	RELEASE ECO 349	3/2/81	KAK
B	REV PER ECO 533	3/17/81	KAK
C	REV. PER ECO 596 LR	4-30-81	KAK
D	REV. PER ECO 691 LR	9-30-81	KAK

3. THIS SCHEMATIC TO BE USED WITH REVISION (5) "B" P.C.B. FABRICATION.
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR	4-28-81
	C+K	6-22-81
	APPD	6-22-81
MAT'L N/A	BREAK ALL SHARP EDGES	
	DECIMAL	ANGULAR
	XX ± .1	±
	XXX ± .1	
FINISH N/A	DO NOT SCALE DRAWING	

PARATRONICS INC.

M764 KEYBOARD SCHEMATIC

DRWG NO.	REV
127-0121-001	D
SIZE D	SCALE NONE
SHT 1 OF 1	

CRT DISPLAY MODULE

SECTION 5: CRT DISPLAY MODULE

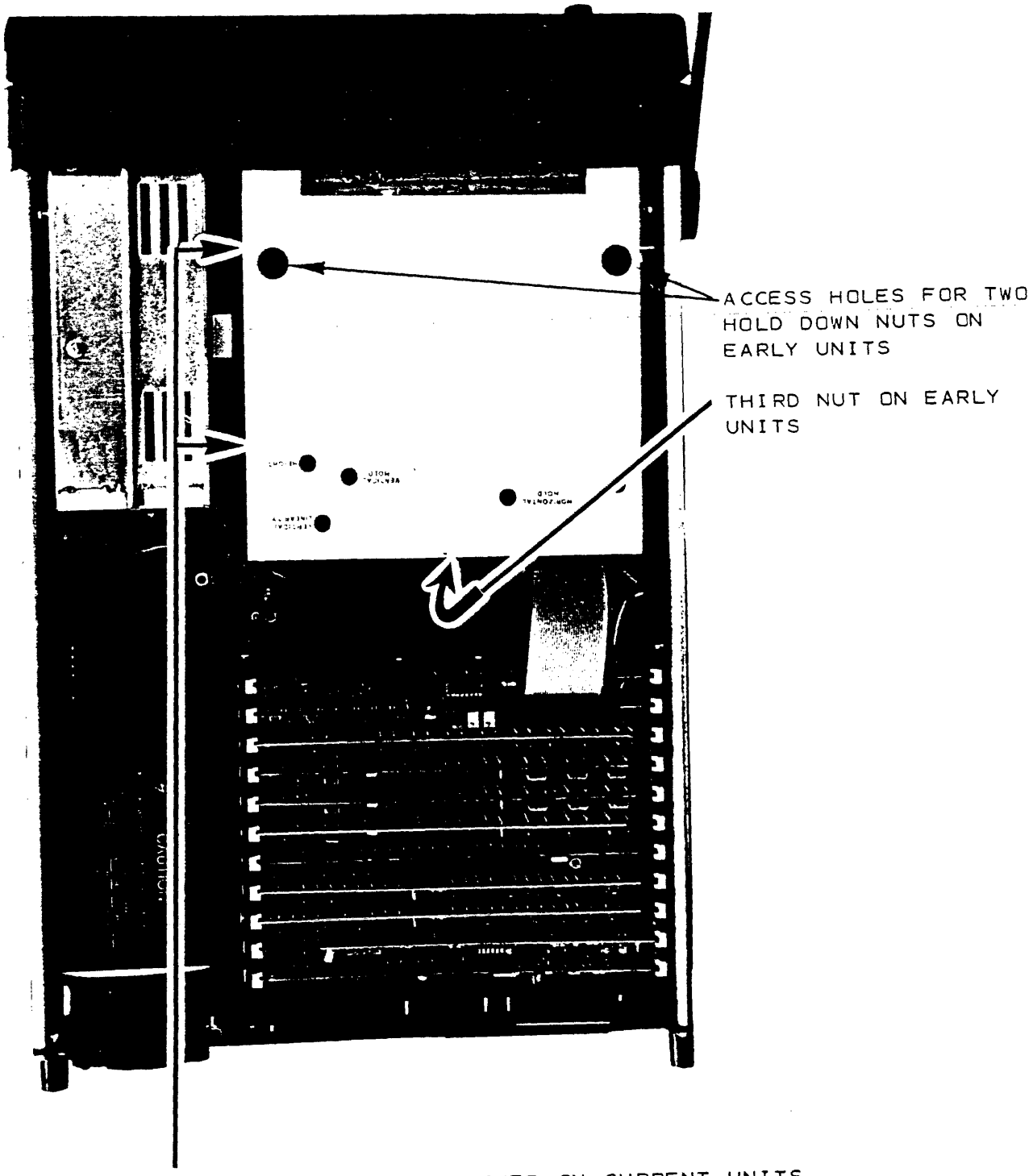


Figure 5-1 CRT Module Cover Removal

SECTION V
CRT DISPLAY MODULE

5.1 INTRODUCTION

The display module is a nine-inch CRT monitor. It accepts a composite video signal sent from the Video Display Board and produces a raster-scan video display. The front panel BRIGHTNESS and CONTRAST controls are provided, and internal controls are provided for maintenance adjustments. The input power required by the module is provided by the 764 power supply.

WARNING

HIGH VOLTAGE IS USED IN THE DISPLAY MODULE. OBSERVE EXTREME CAUTION WHEN POWER IS APPLIED AND THE COVER REMOVED.

5.2 A-C LINE FREQUENCY

The Display Module does not use any line power directly. Primary line power is brought into the 764 to operate the Power Supply. As a consequence, there are line-frequency fields within the instrument that may produce minor interaction with the CRT display. To minimize interaction, the frequency of the vertical sync signal is adjusted as closely as possible to the line frequency. The vertical sync signal is produced on the Video Display Board. It is contained in the composite video signal sent to the Display Module from the Video Display Board.

This adjustment of the vertical sync frequency is automatically made by the Control Program at power-ON time. For details, refer to the Sync Generator discussion in the Video Display section.

5.3 CRT ADJUSTMENT PROCEDURE

The Display Module, and in particular the CRT, is subject to component aging and may require occasional adjustment. Any adjustments that are found necessary should be made in accordance with the following instructions:

WARNING

THE DISPLAY MODULE CONTAINS A VERY HIGH VOLTAGE OF 9 KV THAT CAN BE LETHAL. THE FOLLOWING PROCEDURES SHOULD BE UNDERTAKEN ONLY BY EXPERIENCED TECHNICAL PERSONNEL FAMILIAR WITH TELEVISION OR CRT MONITOR ADJUSTMENT PROCEDURES.

a. With power switch OFF, unplug the power cord. Loosen both quarter-turn screws at the rear of the top cover. Remove the cover by sliding it to the rear of the instrument and upwards.

b. Remove the screws and cover of the display module so that access to the adjustments is obtained. Refer to Figure 5-1. Note that early production units necessitate removing the module from the chassis. Refer to step c. for these units.

c. Early production units require that the display module be removed from the chassis. This allows access to the screws holding the module cover. To remove the display module use a long (8") socket extension to reach the three nuts as shown in Figure 5-1. Carefully remove the display module from the chassis sufficiently to loosen the module cover screws and cover. If necessary, temporarily disconnect connecting wires to obtain slack necessary for removal.

WARNING

MAKE ALL ADJUSTMENTS WITH PLASTIC ADJUSTING WANDS DESIGNED FOR THIS PURPOSE. DO NOT USE METAL SCREWDRIVERS OR ANY METAL TOOL. LETHAL VOLTAGES ARE PRESENT AND COULD CAUSE INJURY OR DEATH.

Replacement monitors are supplied by NPC with adjustments already made. Only minor touch-up of horizontal and vertical hold may be necessary after installation.

Before installing a replacement monitor, ALWAYS check for 12 volts at the heavy red and black leads to monitor PCB. Voltages lower than 11.50 V or more than 12.5 V will distort the display. (Refer to Figure 5-2.)

Touch up adjustments are made as follows:

a. Verify that the three disconnects are properly connected. (Power, external video and processor.)

b. Turn power on. Wait a few seconds for the beep, then depress S2 key for processor test.

c. Turn EXTERNAL (on bracket) brightness control fully on (CW). Then turn EXTERNAL contrast to about one half rotation or mid-point. At this point a display of some sort will appear on screen.

d. Coarse adjustment of horizontal hold must be made with **PLASTIC** screwdriver. Turn horizontal hold either way. Display will go to diagonal lines. Turn control in opposite direction and diagonal lines will appear in other direction. The coarse adjustment will be between these two points. The display will appear to be running straight up and down.

e. The display may be stable or appear to be rolling vertically. Using the PLASTIC screwdriver, adjust the vertical hold control until the display is rolling slowly downward. Turn the vertical hold slightly counterclockwise until the display appears to snap into a locked position. The display should be locked and stable at this time, showing "Processor Test".

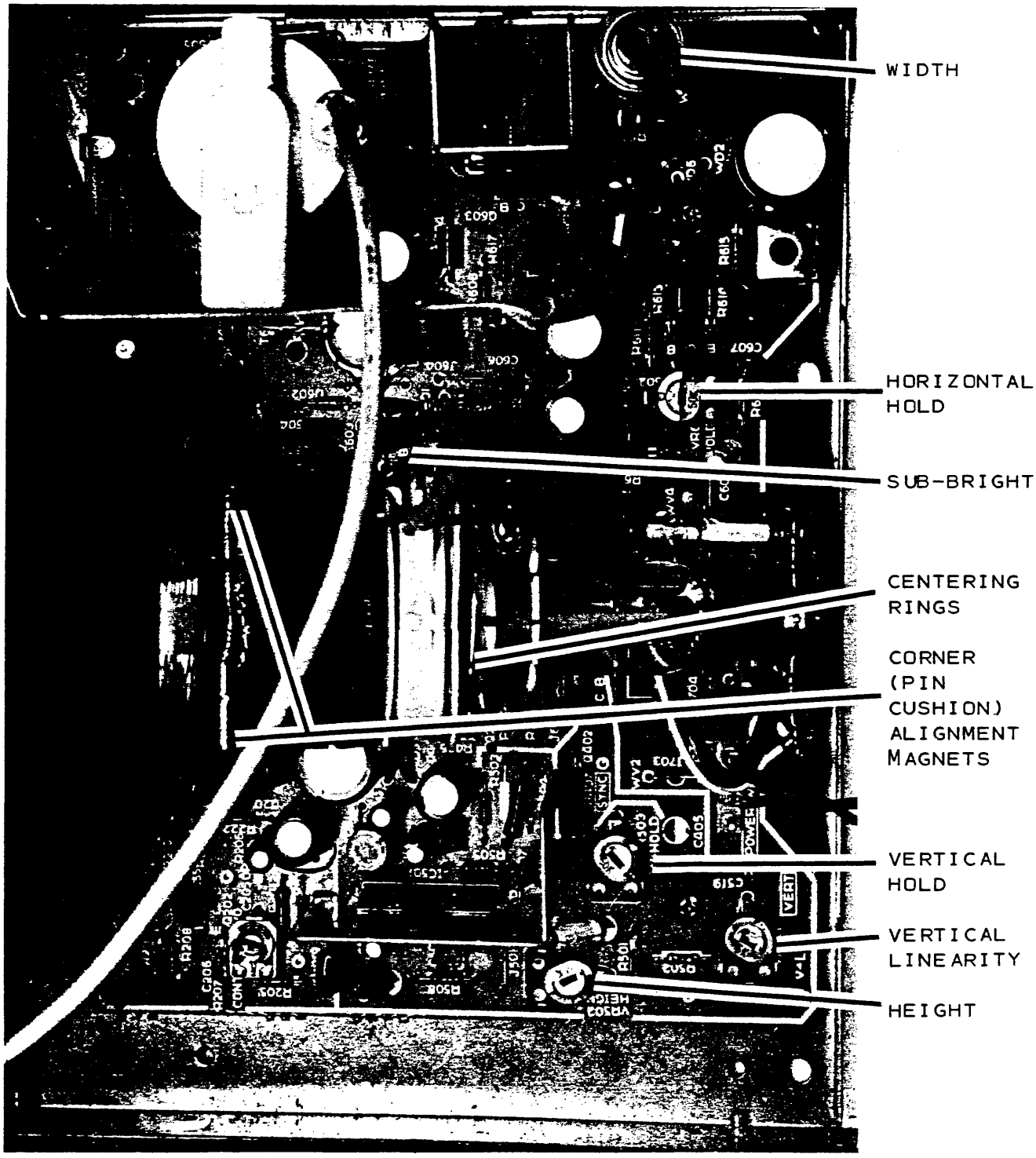
f. Note REVERSE on the display, located about one third down the screen. Adjust the external contrast control until this block is brightest, just before edges of block start to distort. Any distortion of this block means the contrast is set too high. The brightness now may be reduced slightly for HALF LIGHT adjustment.

g. Note the alphabet in the upper right corner of display. VERY SLIGHTLY move the horizontal hold control back and forth, until the "O" appears undistorted. This is a sensitive adjustment. Moving too far will cause the display to drop out diagonally.

h. Turn power off, wait five seconds, turn power on. The display should show a locked, completely stable display of the Configuration Menu. Try this test several times. Any tendency to pull sideways or roll should be cured by very small adjustments of the horizontal or vertical controls. Now press the Processor Test key. The display should be completely stable.

THIS COMPLETES THE ADJUSTMENT PROCEDURE

Turn the power off, disconnect the power cord, and reassemble in the reverse order from disassembly.



NOTE: BRIGHTNESS AND CONTRAST CONTROLS ON EXTERNAL BRACKET AT FRONT PANEL.

Figure 5-2 CRT Adjustments

PROCESSOR/VIDIO

SECTION 6: PROCESSOR/VIDEO

SECTION VI
PROCESSOR/VIDEO

6.1 INTRODUCTION

The Processor Board contains the microcomputer system. The system controls all analyzer hardware functions and performs other operations, including keyboard interface and video display.

The major components on the board include the 8085 microprocessor, 64K of EPROM, 4K of RAM, video generator, a RAM/IO/Timer IC, an IEEE-488 interface and related circuitry. All the schematics, board layout, and parts list, are included at the end of this section.

6.2 FUNCTIONAL DESCRIPTION

Refer to schematic drawing 127-0130-001. The functions described include microprocessor, video generator, and parallel interface. Each processor function will be discussed separately in the following paragraphs.

6.2.1 MICROPROCESSOR

Refer to sheet 1. The program execution is performed by U36, the 8085 microprocessor. The system clock (CPUCLK) is derived by U42 from the DOT Clock generator output at U6-14 on sheet 4. The 8085 is interfaced to the bus by U35 and U46 via U50. These circuits also perform the necessary demultiplexing functions for the 8085 data bus.

On-board device address decoding is performed by U37, U38 and U51. Addresses are decoded by U51, that in turn controls U37 and U38 to provide the appropriate device select signal. U51 also provides the appropriate signals for pins 18 and 21 of the EPROMs. The functions of these pins may vary according to the type of EPROM used. In addition, U51 controls data bus buffer U52. Note that if the TEST signal is high, U51 is disabled, and the processor reads from switch S1. The outputs received from U38 are deglitched by enabling them only when ALE is low.

Refer to sheet 2. The program is stored in EPROMs (2532 or 2564) U1-U4, U14-U17. EPROM type and number installed will vary, according to program requirements (ie, some sockets might not be used). The 4K RAM is provided by U18-U21 and U27-U30. Each RAM is 4K x 1 bit organization, a 2141 device. The RAM data outputs are buffered by U52 on sheet 1, the inputs by U39.

U40 is an 8155 that contains 256 bytes of RAM, three I/O ports, and a timer. It provides many Processor Board I/O and control functions and is connected to the data bus via U10 and U39. Signal CCLK is the clock used for the timer function. CCLK is derived by U43, pin 2, from the DOT Clock oscillator output at U6, pin 8 (sheet 4). Port A provides a number of control functions, primarily for the video display.

Refer to sheet 3. Switches SW1-1 through SW1-8 are read by the processor via U5. When an SW1 switch is ON, the input to U5 is low (logic 0). Conversely, OFF is high (logic 1). These switches allow the user to specify certain parameters to the Control Program. SW1-1 selects the line frequency for the Video Generator. SW1-2 through SW1-8 change parameters of the RS-232C and IEEE-488 interfaces. The parameters specified by the switches are different for the two interfaces. Details are provided in this section for the IEEE-488 interface. The detailed information on the RS-232C interface is contained in Section XIII, DISK-RAM board.

6.2.2 VIDEO GENERATOR

Refer to sheet 4. The Video Generator circuitry utilizes the Intel 8275 CRT Controller, U33. U31 provides 2K bytes of video RAM that is accessed by both the CRT and the processor. U53 and U7 buffer the

Video Data Bus connection with the system data. U22, U23 and U24 select either the processor address bus or the output of the display character counter, U8. The selection is determined by the device that is currently accessing the video RAMs. U10, U11 and U41 generate DACK that determines which device is accessing the RAM by controlling MUXs U22, U23, U24.

U6, Y1, U42 and U43 pin 2 generate the timing signals CCLK, CPUCLK, and DOTCLK. These signals are used to produce the video signal. In addition, U43 synchronizes the CURCT and EXTVID signals. The count output from U42 represents the horizontal dot position within a character. The CURCT signal is high when the count from U42 matches the position from the 8155 outputs, compared by U54.

Video data is produced by U33, U25, U26, U10, U34, U45, U12, U44 and U13. U33 outputs a character code and line count to character ROM U25. The ROM produces the 8-bit pattern for that line of that character. This is loaded into U26, a shift register. Simultaneously, U34 latches the appropriate display attribute signals (reverse video, half light, etc.). These signals are sent to the DOT Logic PROM, U45 with the serial bit pattern from U26. Thus, signals DOT and HALFLIGHT (VIDEO + HALF) are produced. These are resynchronized by U43 at pins 10, 12, buffered by U13, and sent to the base of Q1. Emitter follower count generator, Q1, produces a composite video output.

LS165 shift registers U12, U44 produce horizontal and vertical sync pulses with the horizontal and vertical retrace periods (HRTC, VRTC). These are buffered by U13, and mixed with the video signals in Q1. The VRTC signal is buffered by U9 and sent as a processor interrupt, BV, for software synchronization.

The value of the vertical retrace period is set at power-on initialization. At this time, the Control Program reads the setting of switch SW-1. The Control Program then loads a vertical retrace period based on the switch setting into the 8275 CRT Controller. Switch SW1-1 should be set by the user to match the power mains frequency as follows:

SW1-1	Mains Frequency
ON	60 Hz
OFF	50 Hz

Some slight adjustment of the CRT monitor may be required when switching from 50 to 60 Hz refresh rate.

Signals HRTC, VRTC and DOTCLK are fed to the optional Waveform Board via U9, a 16-pin DIP socket. The ready-for-display waveform signal is sent from the Waveform Board via J1-10 as EXTVID-. Signal EXTVID- is resynchronized by U43 and sent to DOT Logic PROM U45.

6.2.3 IEEE-488 PARALLEL INTERFACE

The NPC 764 is equipped with an IEEE-488-1975 parallel interface. The IEEE-488 interface is implemented primarily by U58, a TMS 9914 GPIB Interface Controller (see schematic sheet 3). The U58 data lines are buffered by U57, a 75160 transceiver. The U58 control lines are buffered by U59, a 75161 tranceiver. Bus driver U57 can be configured in either open-collector or three-state mode. This is determined by the logic level at pin 11. A low level produces open-collector operation, and a high level produces three-state operation. The Processor Board is supplied with a jumper that produces open-collector operation. This jumper can be removed if three-state operation is desired (see sheet 3 and board layout drawing).

The IEEE-488 connector on the rear panel is wired to J3, a 26-pin connector on the motherboard. The motherboard connects these lines to the Processor Board socket S2A. Signal flow is shown in Table 6-1.

Some parameters required by the Control Program to operate the interface are obtained from the setting of SW1-2 through SW1-8. The meaning and values of these switches for the IEEE-488 interface are

Table 6-1 IEEE-488 Signal Flow

Signal	U58 Pins IN/OUT	U58 Pins OUT/IN	S2A Pin	J2 Pin	Rear Panel IEEE-488 Connector Pin
DIO8	12	9	38	4	16
DIO7	13	8	39	3	15
DIO6	14	7	9	2	14
DIO5	15	6	40	1	13
DIO4	16	5	10	21	4
DIO3	17	4	41	22	3
DIO2	18	3	11	23	2
DIO1	19	2	42	24	1
	U59 Pins IN/OUT	U59 Pins OUT/IN			
DAV	15	6	28	19	6
EOI	14	7	58	20	5
NDAC	17	4	27	17	8
NRFD	16	5	57	18	7
IFC	18	3	56	16	9
REN	19	2	26	5	17
SRQ	12	9	59	15	10
ATN	13	8	29	14	11

Table 6-2 DIP Switch 1 Selections

SWITCH	DESCRIPTION	CONTROL
SW1-2	KEYBOARD STATE	DISABLED = ON ACTIVE = OFF
SW1-3	INTERFACE STATE (IEEE-488 I/F)	DISABLED = ON ACTIVE = OFF
SW1-4	TERMINATOR CHARACTER TYPE	CR -> LF = ON CR = OFF
SW1-5	ADDRESS BIT 1	LOW = ON HIGH = OFF
SW1-6	ADDRESS BIT 2	LOW = ON HIGH = OFF
SW1-7	ADDRESS BIT 3	LOW = ON HIGH = OFF
SW1-8	ADDRESS BIT 4	LOW = ON HIGH = OFF

NOTE: Address bit 0, handled entirely by the Control Program, is 0 (low) for the NPC 764 as LISTENER, or 1 (high) for the NPC 764 as TALKER.

shown in Table 6-2. The location and orientation are shown in Figure 6-1. Note that these DIP switches also affect the RS-232C interface parameters described in Section XIII.

6.3 SCHEMATICS, BOARD LAYOUTS AND PARTS LIST

The schematics, board layout and parts list are provided at the end of this section.

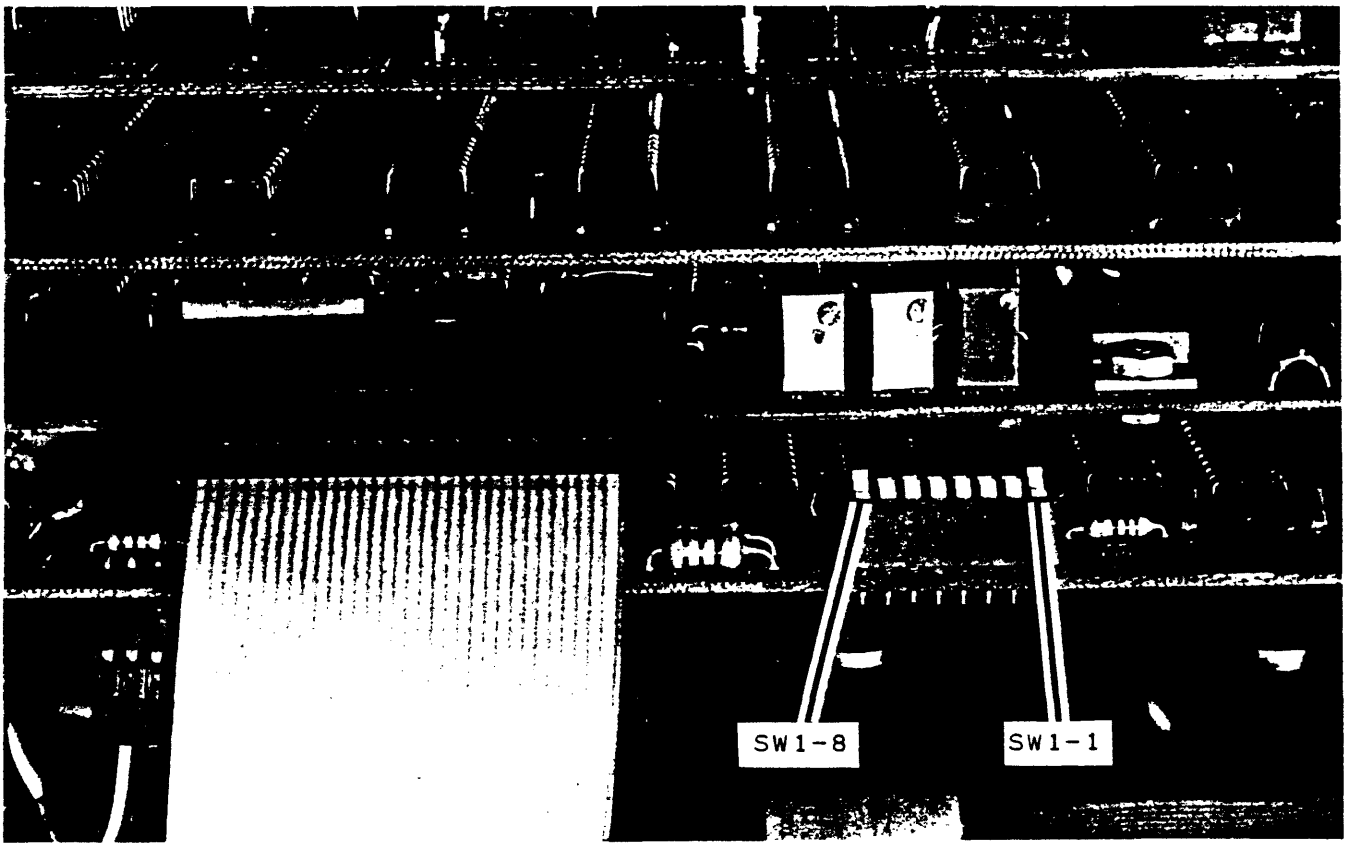


Figure 6-1 Dip Switch Location

PARENT ITEM 143-0130-0002 | CROSS REF ITEM | DESCRIPTION M764 PROCESSOR ASSY I/S 50HZ ENGR DRAW ECO 749 REV J | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE I UNIT MEAS EA | LOW LEVEL 01 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R15 R17 R19		3.000	EA	4C				11/11/82	
	02	112-0317-0001	CRYSTAL 13.056 MHZ Y1		1.000	EA	4C				10/02/81	
	05	113-0001-0001	I.C. 7401 U13		1.000	EA	4C				4/24/80	
	05	113-0003-0000	I.C. 74LS00 U7		1.000	EA	4C				11/11/82	
	04	113-0003-0002	I.C. 74LS02 U10		1.000	EA	4C				4/24/80	
	05	113-0003-0004	I.C. 74LS04 U6		1.000	EA	4C				4/24/80	
	05	113-0003-0008	I.C. 74LS08 U9 U35		2.000	EA	4C				4/24/80	
	04	113-0003-0010	I.C. 74LS10 U41		1.000	EA	4C				4/24/80	
	02	113-0003-0038	I.C. 74LS38 U46		1.000	EA	4C				11/11/82	
	03	113-0003-0074	I.C. 74LS74 U11		1.000	EA	4C				4/24/80	
	06	113-0003-0138	I.C. 74LS138 U37 U38		2.000	EA	4C				4/24/80	
	03	113-0003-0151	I.C. 74LS151 U42		1.000	EA	4C				4/24/80	
	03	113-0003-0165	I.C. 74LS165 U12 U44		2.000	EA	4C				4/24/80	
	04	113-0003-0166	I.C. 74LS166 U26		1.000	EA	4C				4/24/80	
	05	113-0003-0174	I.C. 74LS174 U34 U43		2.000	EA	4C				4/24/80	
	05	113-0003-0244	I.C. 74LS244 U5 U47 U48		3.000	EA	4C				4/24/80	
	06	113-0003-0257	I.C. 74LS257 U22 U23 U24		3.000	EA	4C				4/24/80	
	05	113-0003-0373	I.C. 74LS373 U40		1.000	EA	4C				4/24/80	
	02	113-0012-0002	8085A-2 3MHZ MICROPROCESSOR U36		1.000	EA	4C				10/02/81	
	05	113-0014-0002	I.C. DP8304N NSC U34 U50 U52 U53	ECO 462	4.000	EA	4C				2/02/82	
	05	113-0024-0001	I.C. DP8100 NSC U54		1.000	EA	4C				4/24/80	

PARENT ITEM 143-0130-0002 | CROSS REF ITEM | DESCRIPTION M764 PROCESSOR ASSY I/S 50HZ ENGR DRAW ECO 749 REV J | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 01 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

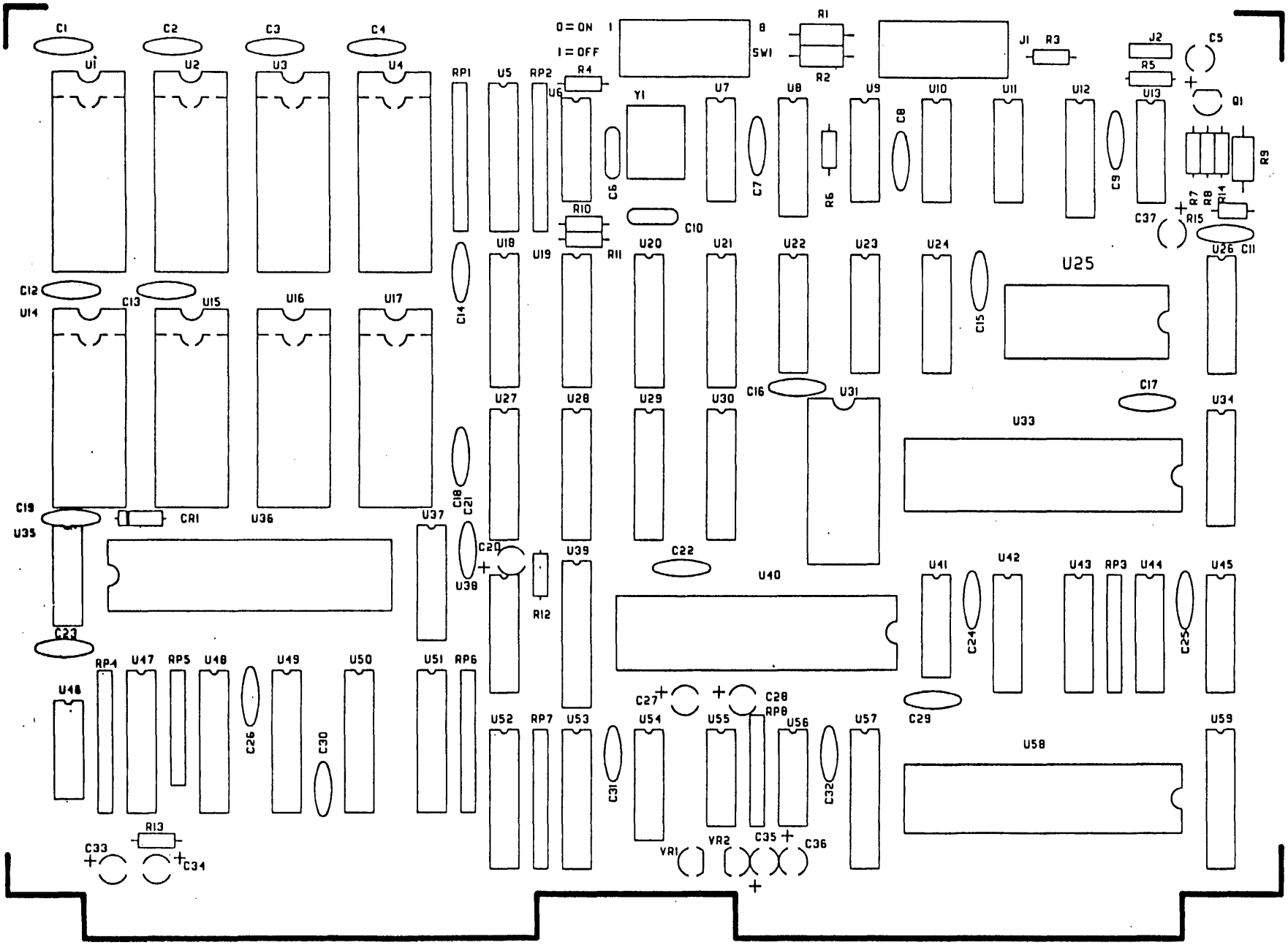
REF NUM	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NUM	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	03	113-0036-0001	I.C. P8275 INT CRT CONTRLR U33		1.000	EA	4C				4/24/80	
	02	113-0060-0002	AM 9116-2.10MHZ I/O TIMER U40		1.000	EA	4C				10/02/81	
	03	113-0061-0001	RAM,4KX1,2141,4ST4044,92448PC U13 U19 U20 U21 U27 U28 U29 U30		8.000	EA	4C				4/24/80	
	04	113-0063-0001	CMOS COUNTER, CD4040BE, RCA U8		1.000	EA	4C				4/24/80	
	03	113-0064-0001	I.C. 75160 U57		1.000	EA	4C				10/02/81	
	03	113-0065-0001	I.C. 75161 TI U59		1.000	EA	4C				10/02/81	
	03	113-0066-0001	I.C. 16K RAM HM6116LP-4 200NS U31		1.000	EA	4C				9/09/81	
	02	113-0067-0001	I.C. TMS9914 IEEE-488 CONTR U58		1.000	EA	4C				10/02/81	
	02	113-4035-0011	PROM 6301-1 M700 PROC U45 U45 PROGRAM WITH NPC BLANK PROM NUMBER 113-0035-0000.	ECO 496 REV	1.000	EA	4C				2/02/82	
	02	113-4062-0005	PROM 6308-1,M764 PROC W/IO-U51 U51 PROGRAM WITH NPC BLANK PROM NUMBER 113-0062-0000	ECO 746 REV A	1.000	EA	4C				11/10/82	
	02	113-6104-0001	EPROM 2532 M700 PROC U25. U25	ECO 496 REV A	1.000	EA	1C				2/02/82	
	02	113-6109-0001	EPROM 2532 M700 PROCESSOR,U17 U17	ECO 747 REV C	1.000	EA	1C				2/02/82	
	05	114-0047-0001	CONN.3PIN 22-23-2031 MOLEX J2		1.000	EA	4C				11/22/82	
	02	143-0130-0090	M764 PROCESSOR ASSY O/S 60 HZ	ECO 693 REV F	1.000	EA	1C				2/02/82	
	02	160-0005-0001	M764 SOFTWARE SET-1K WORD MEM	ECO 747 REV C	1.000	EA	0				8/11/82	
	03	113-0062-0001	EPROM 2564 M764 FIRMW W/1K U1	ECO 600	1.000	EA	1				8/02/82	
	03	113-0062-0002	EPROM 2564 M764 FIRMW W/1K U2	ECO 600	1.000	EA	1				8/02/82	
	03	113-0062-0003	EPROM 2564 M764 FIRMW W/1K U3	ECO 600	1.000	EA	1				8/02/82	
	03	113-0062-0004	EPROM 2564 M764 FIRMW W/1K U4	ECO 600	1.000	EA	1				8/02/82	
	03	113-0062-0005	EPROM 2564 M764 FIRMW W/1K U14	ECO 600	1.000	EA	1				8/02/82	
	03	113-0062-0005	EPROM 2564,M764 FIRMW W/1K-U15	ECO 746 REV A	1.000	EA	1				11/10/82	

PARENT ITEM 143-0130-0090 | CROSS REF ITEM | DESCRIPTION: 7754 PROCESSOR ASSY O/S 50 HZ ENGR DRAW ECO 633 REV F | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF DES	LL CO	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NEW	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	00	110-0005-0031	47 OHM 1/4W 5% CF RES R15		1.000	EA	4C	.			5/04/82	
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R4 R10		2.000	EA	4C	.			4/24/80	
	05	110-0005-0055	470 OHM 1/4W 5% CF RES R7 R9 R11 R14		4.000	EA	4C				11/10/80	
	06	110-0005-0059	660 OHM 1/4W 5% CF RES R5		1.000	EA	4C				7/16/81	
	07	110-0005-0079	4.7K OHM 1/4W 5% CF RES R3 R6 R13		3.000	EA	4C				2/02/82	
	06	110-0005-0107	68K OHM 1/4W 5% CF RES R12		1.000	EA	4C				4/24/80	
	07	110-0007-0007	4.7 OHM 1/2W 5% CF RES R1 R2		2.000	EA	4C				4/24/80	
	04	110-0007-0036	75 OHM 1/2W 5% CF RES R9		1.000	EA	4C				4/24/80	
	06	110-0300-0001	RN 10K 510-9-1 10 PIN SIP RP1 RP2 RP4		3.000	EA	4C				4/24/80	
	05	110-0309-0001	RN 4.7K OHM X7 8 PIN SIP RP3		1.000	EA	4C				7/16/80	
	05	110-0314-0001	RN 4.7K OHM X9 10 PIN SIP RP5		1.000	EA	4C				4/24/80	
	05	110-0316-0001	RN 2.2K OHM X9, 10 PIN SIP RP7		1.000	EA	4C				4/24/80	
	04	110-0317-0001	RN 10K OHM X7, 8 PIN SIP RP6		1.000	EA	4C				2/02/82	
	06	111-0004-0072	.1 UF 25V CD CAP C1 C2 C3 C4 C7 C8 C9 C11 C12 C13 C14 C15 C16 C17 C19 C23 C21 C22 C24 C25 C26 C29 C30 C31 C32		25.000	EA	4C				9/13/82	
	06	111-0006-0060	.001 UF 500 CD CAP C6		1.000	EA	4C				4/24/80	
	04	111-0012-0018	15 PF 1KV CD CAP C10		1.000	EA	4C				4/24/80	
	06	111-0050-0107	33 UF 6V TANT DROP CAP C5 C56		2.000	EA	4C					
	05	111-0209-0046	10 UF 25V ELECT RADIAL CAP C33 C34 C37		3.000	EA	4C				5/04/82	
	06	112-0100-0001	TRANSISTOR 2N3904 Q1		1.000	EA	4C				4/24/80	
	07	112-0204-0001	DIODE 1N5820 1N4148 4148 4150 CR1		1.000	EA	4C				4/24/80	

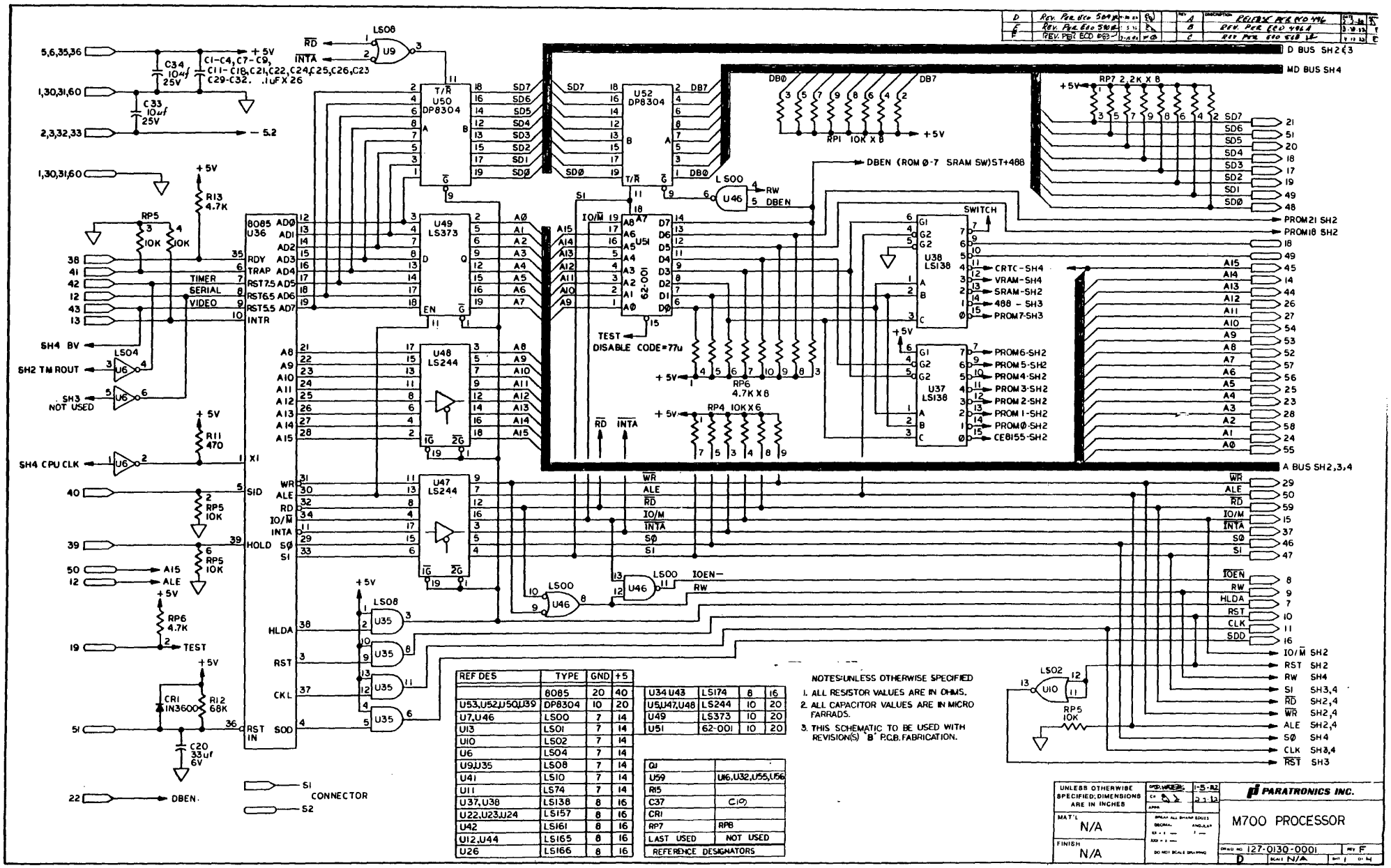
PARENT ITEM: 143-0130-0090 | CROSS REF ITEM: | DESCRIPTION: M764 PROCESSOR ASSY C/S 50 HZ | BATCH QTY: 1 | ITEM TYPE: 1 | LOW LEVEL: 02
ENGR DRAW: CO 683 REV F | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER:

REF SDM	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	115-0005-0001	SOCKET 14PIN U6 U7 U9 U10 U11 U13 U35 U41 U43		9.000	EA	4C				2/02/82	
	05	115-0005-0001	SOCKET 16PIN U8 U12 U22 U23 U24 U26 U54 U36 U37 U38 U42 U43 U44 U45		14.000	EA	4C				2/01/82	
	06	115-0008-0001	SOCKET 18PIN U18 U19 U20 U21 U27 U28 U29 U30		8.000	EA	4C				10/02/81	
	05	115-0009-0001	SOCKET 20PIN U5 U47 U48 U49 U50 U51 U52 U53 U57 U58 U39		11.000	EA	4C				4/24/80	
	06	115-0011-0001	SOCKET 24PIN U17 U25 U31		3.000	EA	4C				2/02/82	
	06	115-0012-0001	SOCKET 28PIN U1 U2 U3 U4 U14 U15		6.000	EA	4C				10/20/81	
	06	115-0013-0001	SOCKET 40PIN U33 U35 U40 U51		4.000	EA	4C				4/24/80	
	04	115-0017-0001	16 PIN SOCKET 516-AG110 ADG J1		1.000	EA	4C				1/15/81	
	04	116-0019-0001	SWITCH 8 POSITION DIP SW1		1.000	EA	4C				4/24/80	
	03	126-0130-0001	M790 PROCESSOR PC BAR	ECO 749 REV C	1.000	EA	4C				10/02/81	



Processor

Nicolet Paratronics
126-0130-0201 Rev.B



REF DES	TYPE	GND	+5
	8085	20	40
U53,U52,U50,U39	DP8304	10	20
U7,U46	LS00	7	14
UI3	LS01	7	14
UI0	LS02	7	14
U6	LS04	7	14
U9,U35	LS08	7	14
U41	LS10	7	14
UII	LS74	7	14
U37,U38	LS138	8	16
U22,U23,U24	LS157	8	16
U42	LS161	8	16
U12,U44	LS165	8	16
U26	LS166	8	16

U34 U43	LS174	8	16
U5I,U47,U48	LS244	10	20
U49	LS373	10	20
U5I	62-001	10	20

QI	
U59	U16, U32, U55, U56
RI5	
C37	C10
CRI	
RP7	RP8
LAST USED	NOT USED
REFERENCE DESIGNATORS	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICRO FARRADS.
3. THIS SCHEMATIC TO BE USED WITH REVISION(S) 'B' P.C.B. FABRICATION.

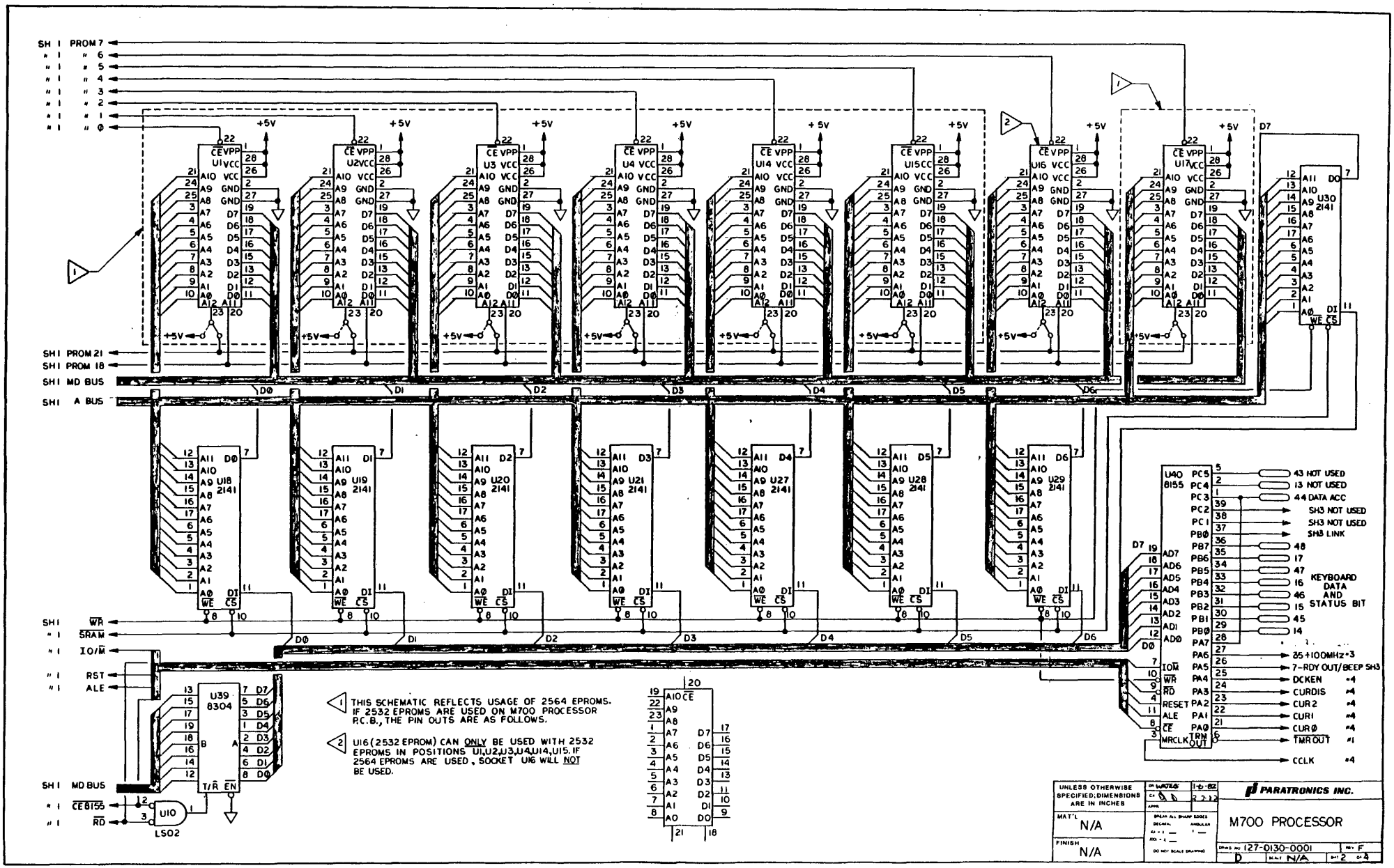
REV	DESCRIPTION	DATE
A	RELEASE PER ECO 496	3-5-82
B	REV PER ECO 496A	3-18-82
C	REV PER ECO 568	9-13-82
D	REV PER ECO 580	3-5-84
E	REV PER ECO 583	5-31-84
F	REV PER ECO 693	12-6-84

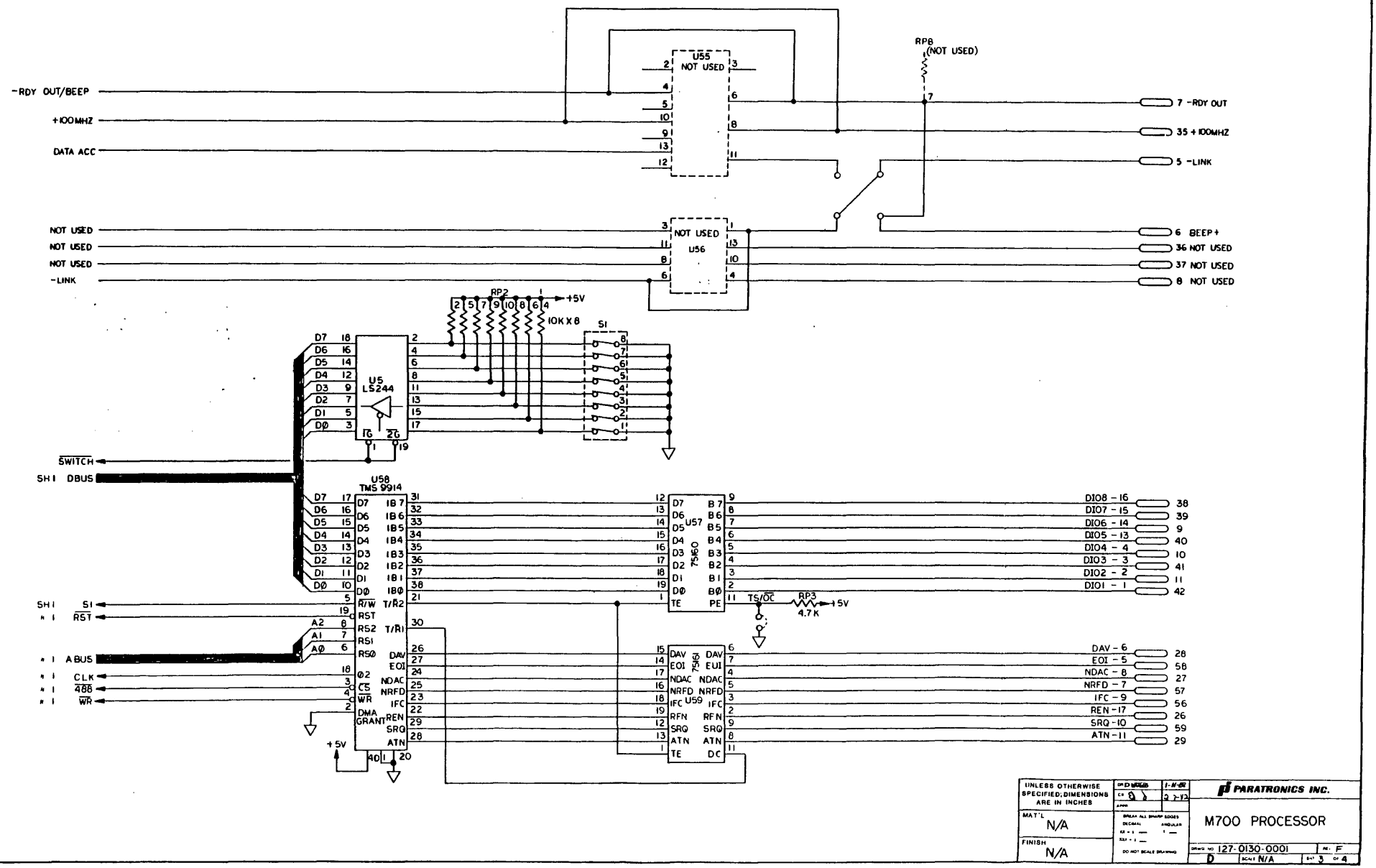
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DRWD. [illegible] 1-5-82
CHK'D. [illegible] 2-1-82
APPR.
DO NOT SCALE DRAWING

PARATRONICS INC.

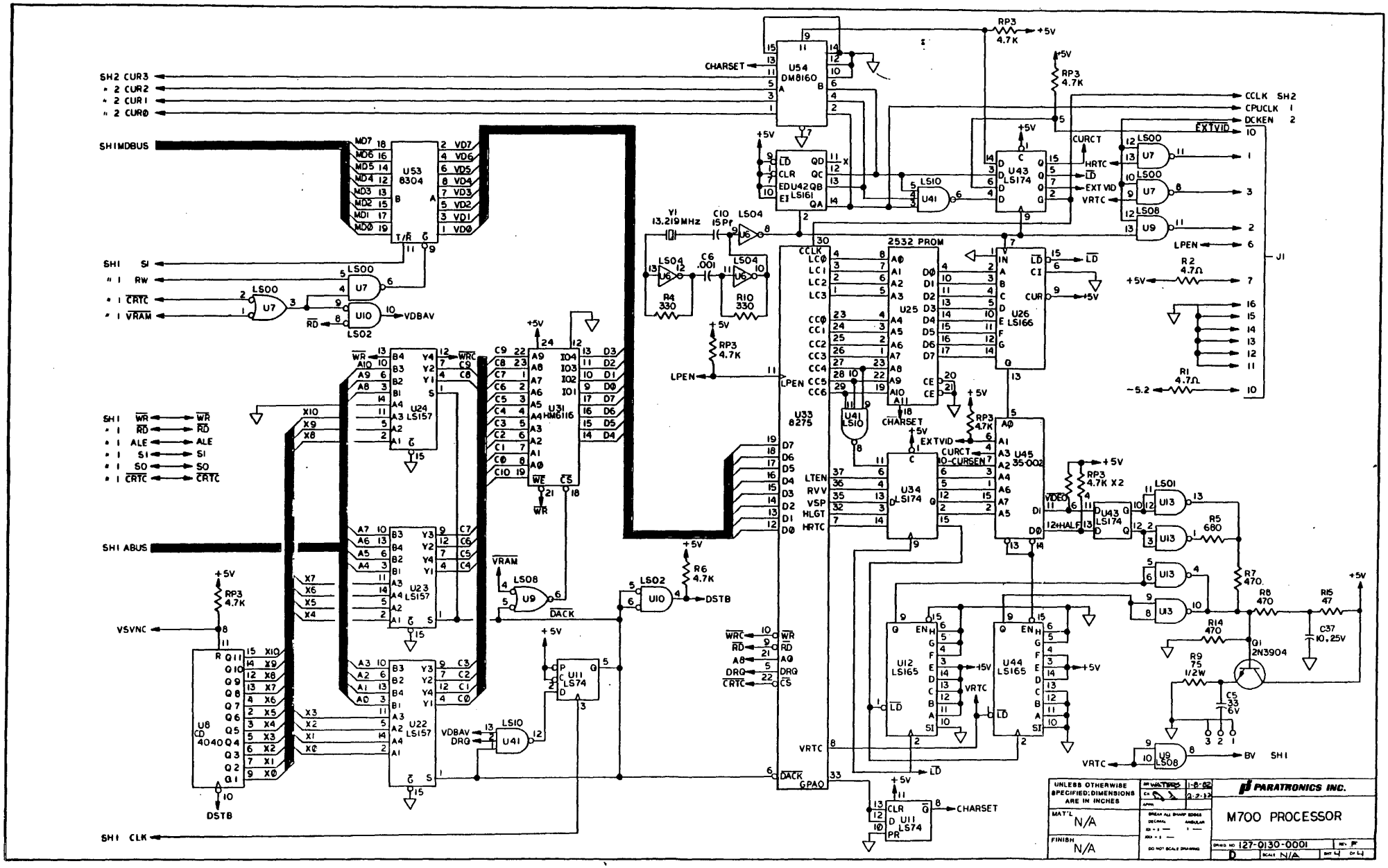
M700 PROCESSOR

DRWG NO. 127-0130-0001 REV F
SIZE D SCALE N/A SHT 1 OF 84


SH 1 PROM 7
" 1 " 6
" 1 " 5
" 1 " 4
" 1 " 3
" 1 " 2
" 1 " 1
" 1 " 0
+5V
U1 VCC
U2 VCC
U3 VCC
U4 VCC
U15 VCC
U16 VCC
U17 VCC
CE VPP
A10 VCC
A9 GND
A8 GND
A7 D7
A6 D6
A5 D5
A4 D4
A3 D3
A2 D2
A1 D1
A0 D0
A12 A11
SH 1 PROM 21
SH 1 PROM 18
SH 1 MD BUS
SH 1 A BUS
D0
D1
D2
D3
D4
D5
D6
D7
U18 2141
U19 2141
U20 2141
U21 2141
U27 2141
U28 2141
U29 2141
U30 2141
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
DI
WE
CS
SH 1 WR
" 1 SRAM
" 1 IO/M
" 1 RST
" 1 ALE
U39 8304
T/R
EN
SH 1 MD BUS
" 1 CE 8155
" 1 RD
U10
LS02
1 THIS SCHEMATIC REFLECTS USAGE OF 2564 EPROMS. IF 2532 EPROMS ARE USED ON M700 PROCESSOR P.C.B., THE PIN OUTS ARE AS FOLLOWS.
2 U16 (2532 EPROM) CAN ONLY BE USED WITH 2532 EPROMS IN POSITIONS U1,U2,U3,U4,U14,U15. IF 2564 EPROMS ARE USED, SOCKET U16 WILL NOT BE USED.
U40 8155
PC5
PC4
PC3
PC2
PC1
PB0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
IO/M
RESET
ALE
CE
MRCLK
TRN OUT
43 NOT USED
13 NOT USED
44 DATA ACC
SH3 NOT USED
SH3 NOT USED
SH3 LINK
48
17
47
16
46
15
45
14
KEYBOARD DATA AND STATUS BIT
35+100MHz*3
7-RDY OUT/BEEP SH3
DCKEN *4
CURDIS *4
CUR2 *4
CURI *4
CUR0 *4
TMR OUT *1
CCLK *4
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
PARATRONICS INC.
M700 PROCESSOR
DRAG NO. 127-0130-0001
REV F
SIZE D
SCALE N/A
SHT 2 OF 4



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DRAWN 1-16-80	PARATRONICS INC.
MAT'L N/A	CHK 2-7-80	M700 PROCESSOR
FINISH N/A	DO NOT SCALE DRAWING	DRWG NO 127-0130-0001 REV F
		D SCALE N/A SHT 3 OF 4


SH2 CUR3
SH2 CUR2
SH2 CUR1
SH2 CUR0
SH1MDBUS
SH1 ABUS
SH1 CLK
CHARSET
U54 DM8160
U53 8304
U25 2532 PROM
U26 LS166
U33 8275
U34 LS174
U45 35-002
U24 LS157
U23 LS157
U22 LS157
U31 HM6116
U8 CD 4040
U11 LS74
U12 LS165
U44 LS165
U43 LS174
U41 LS10
U7 LS00
U10 LS02
U9 LS08
U13 LS01
Y1 13.219MHz
C10 15PF
C6 .001
R4 330
R10 330
RP3 4.7K
R1 4.7Ω
R2 4.7Ω
R5 680
R6 4.7K
R7 470
R8 470
R9 75 1/2W
R14 470
R15 47
C37 10.25V
C5 33 6V
Q1 2N3904
CCLK SH2
CPUCLK 1
DCKEN 2
EXTVID
CURCT
HRTC
EXT VID
VRTC
LPEN
VDBAV
DSTB
DACK
VRAM
VSVNC
12HALF
VIDEO
BV SH1
J1
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
PARATRONICS INC.
M700 PROCESSOR
DRWG NO 127-0130-0001
SCALE N/A
SHT 4 OF 4

STATE CONTROL BOARD

SECTION 7: STATE CONTROL BOARD

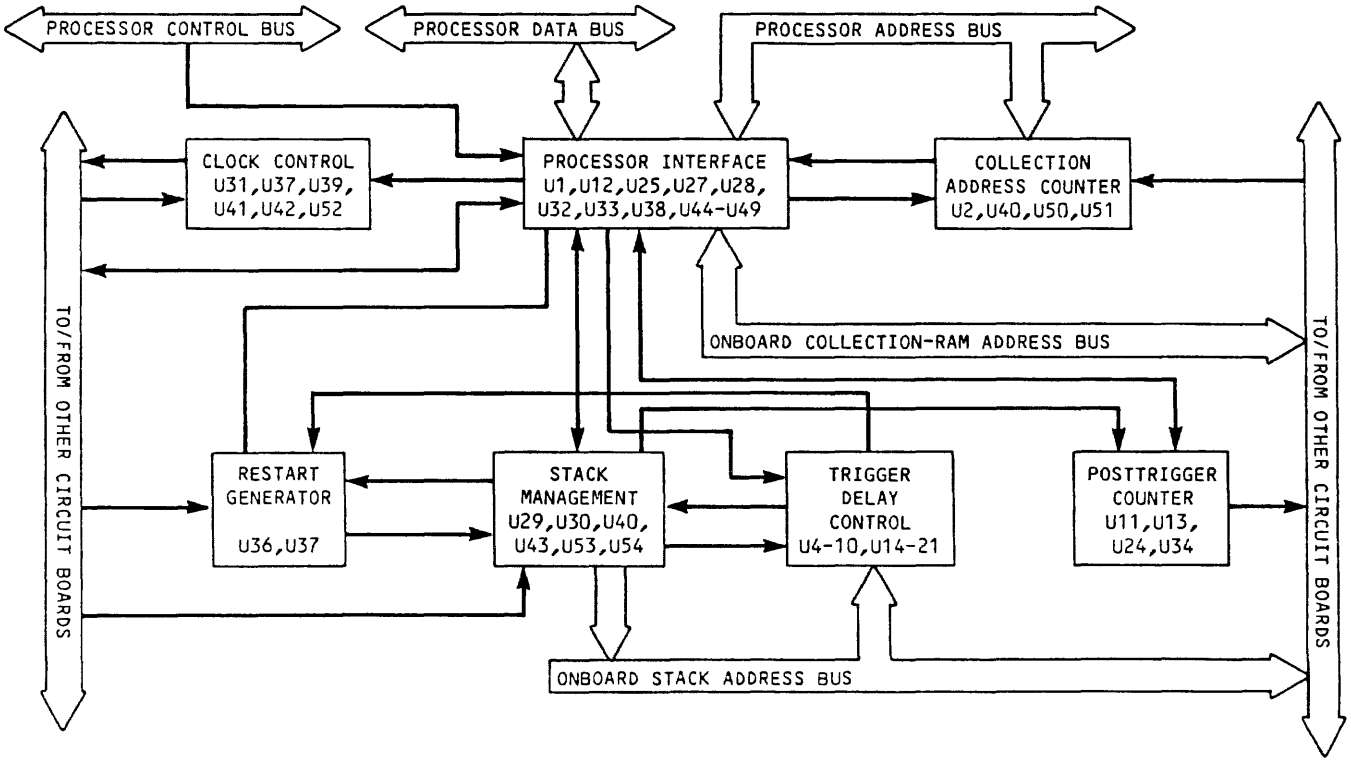


Figure 7-1 State Control Board Block Diagram

SECTION VII
STATE CONTROL BOARD

7.1 INTRODUCTION

Hardware registers, counters and RAMs on the State Control Board are loaded by the Control Program. The loading information is entered from the keyboard under the guidance of the STATE menu. Using the parameters and modes specified, the State Control Board implements the various State analysis operations.

7.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Control Board is shown in Figure 7-1. Also refer to the schematic diagram, board layout and parts list included at the end of this section. Tables of connector pins versus signal names for all motherboard connectors are provided in SIGNAL AND INTERCONNECTION TABLES. An alphabetical list of all interboard signals is included. The GLOSSARY section offers explanations for acronyms or terms that may be unfamiliar.

The functional units of the State Control Board are the Processor Interface, Stack Management, Clock Control, Collection Address Counter, Post-trigger Counter, Restart Generator, and Trigger Delay Control. These units are discussed in the following subsections.

7.2.1 PROCESSOR INTERFACE

Refer to schematic #127-0128-001. The Processor Interface (sheet 1) is comprised of the Address Decoder, Status Ports, Interface Output Ports, and Interface Shift Register. This circuitry allows the processor, under the direction of the Control Program, to load user-supplied information. This information is entered from the keyboard with the aid of menus. To prepare the analyzer for the intended application, the information is entered into registers, RAMs, and counters. The interface allows the processor to interrogate status and signal lines and to send various control signals when appropriate.

The **Address Decoder** consists of the following: U33, a 74LS10 triple 3-input NAND gate; U1, sections of a 74LS00 quad NAND gate; and U44 and U45, 74LS138 3-to-8 decoders. This circuitry allows the processor to read and write to the Interface Status and Output Ports, respectively. I/O read and write commands are used to perform these functions. Also, one port output signal, RDALMEM- (U44-14), is sent to the Collection Address Counter.

The **Interface Output Ports,** U46 and U47, are both 74LS374 octal-D flip-flops. Both flip-flops store software-generated control signals. U46 stores signals for the State Control Board. U47 for the A, B Probes and the A, B State Memory Boards.

The **Status Ports,** U48 and U49, are both 74LS244 octal line receivers. The processor reads status signals from the State Control Board. These are read via U49, U48-8,15 and from the A and B Probes via U48-11,17. Data collection addresses are read by the processor from the State Control Board through U49 and U48.

The **Interface Shift Register** has a part shown on each sheet of the schematic. The register consists of the following components:

a. U38, a 74LS164 8-bit shift register, sheet 1.

b. U32B, one-half of a CMOS 4015 dual 4-bit shift register, sheet 2.

c. U11, U25, 4015s, sheet 3.

d. U27, U28 and U32A, all 4015s, sheet 4.

These six 4015 devices have parallel read-out and allow the processor to store five sets of eight control bits. Only one daisy-chained data line is required instead of running the 8-bit Processor Data Bus to each of the five devices. The data line is SRDATA, that is sent from Interface Output Port U46-19. This 48-bit shift register stores control bits (U38, U32A) and preset counts (U32B, U12, U27, U28). The last bit in the last shift register, U25-2, is sent back to the Status Port at U48-6. This allows the Control Program to monitor the Shift Register load status.

7.2.2 STACK MANAGEMENT

Stack Management (sheet 2) is comprised of the Stack Address Counter, Stack Address Latches, and Stack Control circuits. This circuitry maintains the stack pointer by means of the Stack Address Counter. It also evaluates a number of input signals to determine when to POP (advance) or reset the stack pointer.

The **Stack Address Counter**, U43, a 74S169 synchronous 4-bit binary counter, generates signal NSA (Next Stack Address). This signal is sent to the address inputs of the Delay Count RAM (sheet 4). It is also sent, via stack address latches U43, U54, to the Trigger Stack RAM on each State Memory Board. The trigger **stack address** on the circuit board is the equivalent of the trigger **level** on the menu.

The stack RAMs have terminal addresses of 0F hex (15 dec). The Stack Address Counter is preset by the Control Program (through U32B) and always operates in POP direction (always counts **up**). For example, if the menu specified trigger levels 0 through 8, the Stack Address Counter would be preset with 0F - 8 = 07. This RAM location, address 07, would contain the word for the first trigger level on the menu, level 0. The ending counter address, 0F, would contain the word for the last trigger level entered on the menu, level 8. At count 0F, the ripple-carry counter output at U43, pin 15 produces the stack-empty signal, STKE-. This is used by the Stack Control circuitry.

The **Stack Address Latches**, U53 and U54, are both 74S74 dual D flip-flops. They latch the address produced by the Stack Address Counter. This allows it to be stabilized for the Trigger-word and Qualifier-Word RAMs on the State Memory Boards.

The **Stack Control** circuits consist of the following logic:

a. U52A,B,D, sections of a 74S86 quad exclusive-OR gate.

b. U37C,D, sections of a 74S02 quad NOR gate used as inverters.

c. U31, a 74S02 quad NOR gate. Sections A and B are used as negative-input AND gates.

d. U38B, one-half of a 74S74 dual D flip-flop.

e. Multiplexer U29, a 74S64 4-2-3-2 AND-NOR gate.

f. U30, a 74S74 dual D flip-flop.

g. U23B, a section of a 74LS32 quad OR gate.

This circuitry produces signals used by Stack Management and a number of signals used elsewhere on the board. These signals include the following:

a. POPEN- (POP Enable -), that advances the level in the trigger- and qualifier-word stacks on the State Memory Boards.

b. POPSTK+ (POP Stack +, a clock derived from POPEN-), that advances the level in the delay-mode stack.

c. PTENB+ (Post-trigger Enable +), derived from the Stack Address Counter ripple-carry signal, STKE-. PTENB+ is sent to the Post-trigger Counter. That causes the count to start for collection of the specified number of post-trigger data words.

7.2.3 CLOCK CONTROL

Clock Control is comprised of the Clock Multiplexer (sheet 2) and the Clock Qualifier Gate (sheet 3). This circuitry implements the keyboard-entered selection of clock source and provides the final logic in the process of clock qualification.

The **Clock Multiplexer** consists of U39, a 74S64 4-2-3-2 AND-NOR gate; U41A, one-half of a 74S51 dual AND-NOR gate; and U42, one-fourth of a 10125 quad ECL-to- TTL translator. Signal CLKSEL allows the Clock Multiplexer to implement menu selection of clocks for probe-data latches on the Memory Boards. CKLSEL is received from the Interface Shift Register. The A-board clock, ALATCHCLK, may be menu-selected from either the positive or negative-going edge of APROBCLK (the A-probe incoming clock). The B-board clock, BLATCHCLK, may be menu-selected from APROBCLK or the +/- going edge of BPROBCLK. BPROBCLK is the B-probe incoming clock. The CLATCHCKK selections are performed on the 764 motherboard.

The **Clock Qualifier Gate,** U41 (sheet 3), is not used. The signal CLKQUALIN- is generated on the motherboard in the following cases:

a. If the incoming clock qualifier signals ACQ1, BCQ1 and CCQ1 are active.

b. If ACQ2 and BCQ2 and CCQ2 are active.

The signals ACQ1,2, BCQ1,2 and CCQ1,2 are received from pre-collection comparator RAMs on the State Memory Boards. ACQ1 is active high if the following statement is true regarding the first clock-qualifier word specified in the menu: The first 16 data bits, first two qualifier bits and one link bit are matched by the bits received from the A-probe lines. In a similar manner, BCQ1 is high if the first clock-qualifier word specified in the menu meets the following statement: The second 16 data bits and second two qualifier bits are matched by the bits received from the B-probe lines. CCQ1 operates similarly. If the entire first clock-qualifier word is matched, ACQ1, BCQ1 and CCQ1 are high and BCLKQUALIN- goes active low. Similarly, ACQ2 and BCQ2 represent the second clock-qualifier word on the menu.

Note the distinction between qualifier **words,** used with the menu, and qualifier **bits,** used with the probe leads. The A, B and C probes each have two qualifier leads. Either or both of the two leads on each of the probes can be used for trigger or clock qualification. The selection is made on the STATE menu. On the STATE menu, the qualifier bits appear in the clock-qualifier word or trigger word as -XXXXXX. The Xs mark the positions, left to right, of AQ1, AQ2, BQ1, BQ2, CQ1, CQ2. If a value is given to the first X in the clock-qualifier word, such as -0XXXXX, then AQ1 is used as a **clock** qualifier. If the first X is also given a value in a trigger word, then AQ1 is **also** used as a **trigger** qualifier.

7.2.4 COLLECTION ADDRESS COUNTER

The Collection Address Counter (sheet 3) consists of U50, U51 and U2, 74LS191 synchronous 4-bit binary counters; and U40A, one-half of a 74S74 dual D flip-flop. This circuitry supplies 1024 sequential storage addresses for the Data Collection RAMs on the State Memory Boards. During display and analysis, the same circuitry allows the processor to address those RAMs when reading the collected data.

The three 4-bit counters are connected in cascade to form a 12-bit counter. This provides a capacity of 4096 counts, but is limited to 1024 by software. Outputs RA0 through RA9 are sent as address bits to the Data Collection RAMs on the State Memory Boards. In the load mode, the counters send the input levels through without change. This allows the processor to directly address the RAMs. The load mode

is initiated by RDALMEM- (Read All Memory -), a Control Program Signal received from the Processor Interface. Before the Control Program releases RDALMEM-, it places zeroes on the counter input lines. Thus, when RDALMEM- is released, the counter is preset to 000.

With the RDALMEM- load signal inactive (high), the counters are ready to generate sequential addresses for the Data Collection RAMs. The count is advanced with each BWE+ clock pulse. BWE+ (B Write Enable +) is the **qualified** data collection clock. It is received from State Memory Board and is selected by the processor.

As the counters sequence 000 through 400, the QC at U2-6 (occurring at count 400) is sent to flip-flop U40. This circuitry generates signal ROLLOVER1+ the first time address 400 is reached. This signal is sent to Interface Status Port U48 for use by the Control Program.

The counter sequences through the RAM address range until the trigger conditions are met. The BWE+ clock is subsequently stopped by signal BCKLINH+ and is discussed below. In some instances, this clock interruption may occur before the first rollover. In other instances, the interruption may not occur until manual intervention, such as a FORCE DISPLAY or a menu call.

7.2.5 POST-TRIGGER COUNTER

The Post-trigger Counter (sheet 3) is comprised of the Counter and the Clock Inhibit circuits. This circuitry causes data collection to continue for the menu-specified number of data words after the trigger. The menu expresses this parameter as **pre-trigger count**, but the Control Program converts the number to **post-trigger count**. This allows more efficient circuit implementation.

The menu allows a pre-trigger count range of 0 to 999 words.

The post-trigger **Counter** consists of U11, U13 and U24, 74LS161 synchronous 4-bit binary counters. They are combined to form a 12-bit counter with a maximum count of 400h. This counter serves to count the postrigger count. The program limits the counter load so that the maximum count is 999.

At set-up time, the Control Program presets the counter to the proper calculated value. The value loaded is 400-c, where c is the post-trigger count. The actual loaded value may vary by one or two counts from 400-c. This allows for compensation of pipeline delays in associated circuitry.

When the trigger conditions have been met, signal PTENB+ (PostTrigger Enable) goes high. This disables the load inputs and enables the count function. The counter advances at each pulse of BWE+, the qualifier data-collection clock. The count completion is signaled by the ripple-carry output at U24-15.

The **Clock Inhibit** circuit consists of U35B,C,D, each one-fourth of a 74S00 quad NAND gate (B and C are used as negative-input OR gates); U23C, one-fourth of a 74S32 quad OR gate; and U34, a 74S74 dual D flip-flop. When the post-trigger count has been reached, this circuitry generates clock-inhibit signals as described below.

When the Counter reaches terminal count, the ripple-carry output at U24-15 goes high, producing signal ACTDN+ (A Countdown +). This signal is sent, via U23, to set flip-flop U34. The Q- output of U34 is sent to U35 to produce signal BCLKINH+ (B Clock Inhibit +). This signal is sent to all Memory Boards and inhibits further clocking of collected data. The Q output of U34 is returned via U23. This latches the set condition of U34 past the duration of the ripple-carry pulse.

The Q- output of flip-flop U34A produces the signal PTCTDN+ (Post-trigger Countdown +). This signal is sent to Interface Status Port U48 to inform the Control Program that the post-trigger countdown is complete.

If the post-trigger count is 0, signals PSTTG0+ (Post-trigger 0) and PTENB+ are

high at NAND gate U35D inputs. The resulting low output from U35D then presets flip-flop U34A and clears flip-flop U34B. This produces the signals BCLKINH+ and PTCTDN+ without any counting having occurred.

The Control Program can also produce BCLKINH+. This is done by sending signal SWCLKINH- (Software Clock Inhibit) to the inputs of negative OR gates U35B and U35C.

7.2.6 RESTART GENERATOR

The Restart Generator (sheet 3) consists of U37A,B, two sections of a 74S02 quad NOR gate (used as negative input AND gates); and U36, a 74S64 4-2-3-2 AND-NOR gate. This circuit generates the RST- (Restart) signal. This is used by Stack Management to reload the trigger Stack Address Counter with the address for level 0. This address is still latched in the Interface Shift Register section U32B. The system is then restarted, testing for a match of trigger conditions. Signal RST- is produced under any of the following conditions:

a. The NNNNth clock is reached when the ON-NNNNth-CLOCK delay mode is in effect.

b. The NNNNth clock is reached when the BEFORE-NNNNth-CLOCK delay mode is in effect.

c. The menu-specified RESTART word is recognized.

d. The Control Program outputs the signal LDSTKAD+ (Load Stack Address) from Interface Output Port U46-2.

7.2.7 TRIGGER DELAY CONTROL

Trigger Delay Control (sheet 4) is comprised of the Delay Count RAM, Delay Counter, Delay-Mode RAM, and Delay-Mode Control. These circuits implement the menu-selectable trigger-delay functions. The circuits produce signals that allow the search for trigger words to proceed to the next level. The specified delay conditions are met on a level-by-level basis. Note that the trigger word at level 0 has no delay function.

The **Delay Count RAM** consists of U16, U17, U18 and U19, all 74S189 16-word x 4-bit static RAMs. They are connected in cascade to form a 16-word x four 4-bit digit RAM. This RAM is loaded by the processor at set-up time with the menu-selected delay count (the count range is 0-9999d). This is done for each of the 15 delayable trigger-word levels. The stored delay counts are used to preset the Delay Counter as each trigger-word level is reached during processing.

The four address lines of each RAM are applied in parallel with signal NSA (Next Stack Address). Signal NSA is generated by the Stack Address Counter. The four address bits decode into 16 stack addresses that correspond to the 16 trigger-word levels on the menu. When loading the RAM at set-up time, the Control Program addresses it through the transparent Stack Address Counter (U43, sheet 3). The signal is received via section U32B of the Interface Shift Register (sheet 2). Delay-count data for the RAM, shown on sheet 4, is loaded using sections U27 and U28 of the Shift Register. After loading is completed, the Control Program presets the Stack Address Counter with the address count. This number corresponds to the number of trigger levels specified on the menu.

After RESET, the SAM addresses are sent from the counting Stack Address Counter and start with trigger-word level 0. Although there can be no delay specified for trigger-word level 0, the level is stepped through for simplicity of logic. Note that trigger-word level 0 does **not** correspond to stack address 0 unless all trigger-word levels are specified. As each trigger stack level is entered, the stored 4-digit delay count for that level is determined. This data is sent from the Delay Count RAM to the Delay Counter as four 4-bit sections in parallel.

The **Delay Counter** consists of U3B,C,D, sections of a 74S08 quad AND gate; U20, also

a 74S08; U5 through U8, all 74S162 synchronous 4-bit decade counters; and U26A, one-fourth of a 74S00 quad NAND gate. At the start of processing for each stack level, signal POPEN- (from Stack Control) is brought low. This loads the Delay Counter with the count stored in the Delay Count RAM for that stack level. The count value stored and loaded is 9999d-c, where c is the menu-specified count. This conversion is done so the ripple-carry out of U8-15 can be used to indicate terminal count. The actual loaded value may vary a few counts from 9999d-c. This allows for compensation of propagation delays in the associated circuitry. When POPEN- returns high, the counter begins to count.

The count is advanced by DBCLK+ (Delayed B Clock +, derived from BWE+, the qualified data collection clock). This occurs when the count-enable inputs at P (pin 7 on U5 through U8) are high. U3B,C,D and U20A,B provide carry load-ahead to speed up the counter. The P inputs receive TRIGCTEN+ (Trigger Count Enable +) from Delay Mode Control. This signal is sent via U3B-5, U3C-10 and U20B-5. If the menu-entered delay mode specifies counting **clocks**, Delay Mode Control holds the P inputs continually high. If the delay mode specifies counting trigger-word **recognitions**, then each recognition is counted. This is accomplished by Delay Mode Control holding the P inputs high so that one clock pulse is counted.

When the terminal count is reached, the resulting ripple-carry out of U8-15 is sent to U20D,C and U26A. This produces signals DLYCTDN+ and DLYCTDN- (Delay Countdown + and -).

The **Delay-Mode RAM**, U21, is a 74S189 16-word x 4-bit static RAM. As with the Delay Count RAM, the 16 word-addresses represent the 16 levels of the trigger stack. This RAM is loaded by the processor at set-up time using sections U32A and U32B of the Interface Shift Register. The RAM is loaded with the menu-selected delay mode for each of the 15 delayable trigger-word levels. The four data bits output to the Delay Mode Control flip-flops U9, U10 encode the mode information as follows:

a. D2, D3 and D4 constitute a 3-bit code for the five available delay modes.

b. D1 is high if triggering is to occur on or after the trigger word.

c. D1 is low if no triggering is to occur on or after the trigger word.

The mode encoded by D1 is not, strictly speaking, a delay mode. It applies to both delayed and undelayed trigger recognition. For reference, the available trigger-word delay modes and stored codes are shown below:

MENU DELAY MODE	D4	D3	D2
AFTER NNNNth CLOCK	0	0	0
BEFORE NNNNth CLOCK	1	0	0
ON NNNNth CLOCK	0	1	0
NOT ON NNNNth CLOCK	1	1	0
OCCURS NNNN TIMES	0	0	1

Delay-Mode Control consists of U9 and U10, two 74S74 dual D flip-flops; U4, a 74S64 6-2-3-2 AND-NOR gate; U15A, one-half of a 74S74; and U14A, one-half of a 74S51 dual AND-NOR gate.

Flip-flops U9 and U10 latch the delay-mode code bits, read out of the Delay-Mode RAM at NSA time. This data is for use during the processing of the current stack level. The U15A flip-flops generate a one-clock interval pulse on the NNNNth clock for use by the U4 multiplexer.

Signal TRIGCTSEL+ (Trigger Count Select +), is the latched D2 mode-code bit. AND-NOR gate U14 uses TRIGCTSEL+ to determine the nature of output signal TRIGCTEN+ (Trigger Count Enable +). Signal TRIGCTEN+ is sent to the P enable inputs of the Delay Counter. IF TRIGCTSEL+ is high, then TRIGCTEN+ usually is held low. The exception to this is when TRIG- (Trigger-word recognized -) pulses it high at each trigger-word recognition. It is held high long enough for the Delay Counter to count one clock. In this mode (D2=1), the Delay Counter counts trigger-word occurences. In this mode (D2=0), the Delay Count counts clock pulses.

The U4 multiplexer combines the Delay Counter terminal-count signals, DLYCTDN- and DLYCTDN+, with the current delay mode information. This produces signal DLYTC+ (Delay Terminal count +). This signal is sent to Stack Control multiplexer U29 (sheet 2). This enables the next trigger-word recognition (signal TRIG+) to generate POPEN-. If other conditions are favorable, POPEN- advances the stack level. In some delay modes, DLYCTDN+ or DLYCTDN- will cause the Restart Generator to produce signal RST-. This signal overrides DLYTC+ and starts the trigger-word search process over again.

7.3 SCHEMATIC, BOARD LAYOUT AND PARTS LIST

The schematic diagram, board layout and parts lists for the State Control Board are contained on the following pages.

PARENT ITEM 143-0128-0001 | CROSS REF ITEM | DESCRIPTION IN STATE CONTROL PC ASSY I/S | ENGR DRAW ECO 434 REV 3 | BATCH QTY 1 | EFFEC 12/08/82 | ITEM TYPE 1 | UNIT MEAS EA | LOW LEVEL 01 | PLANNER

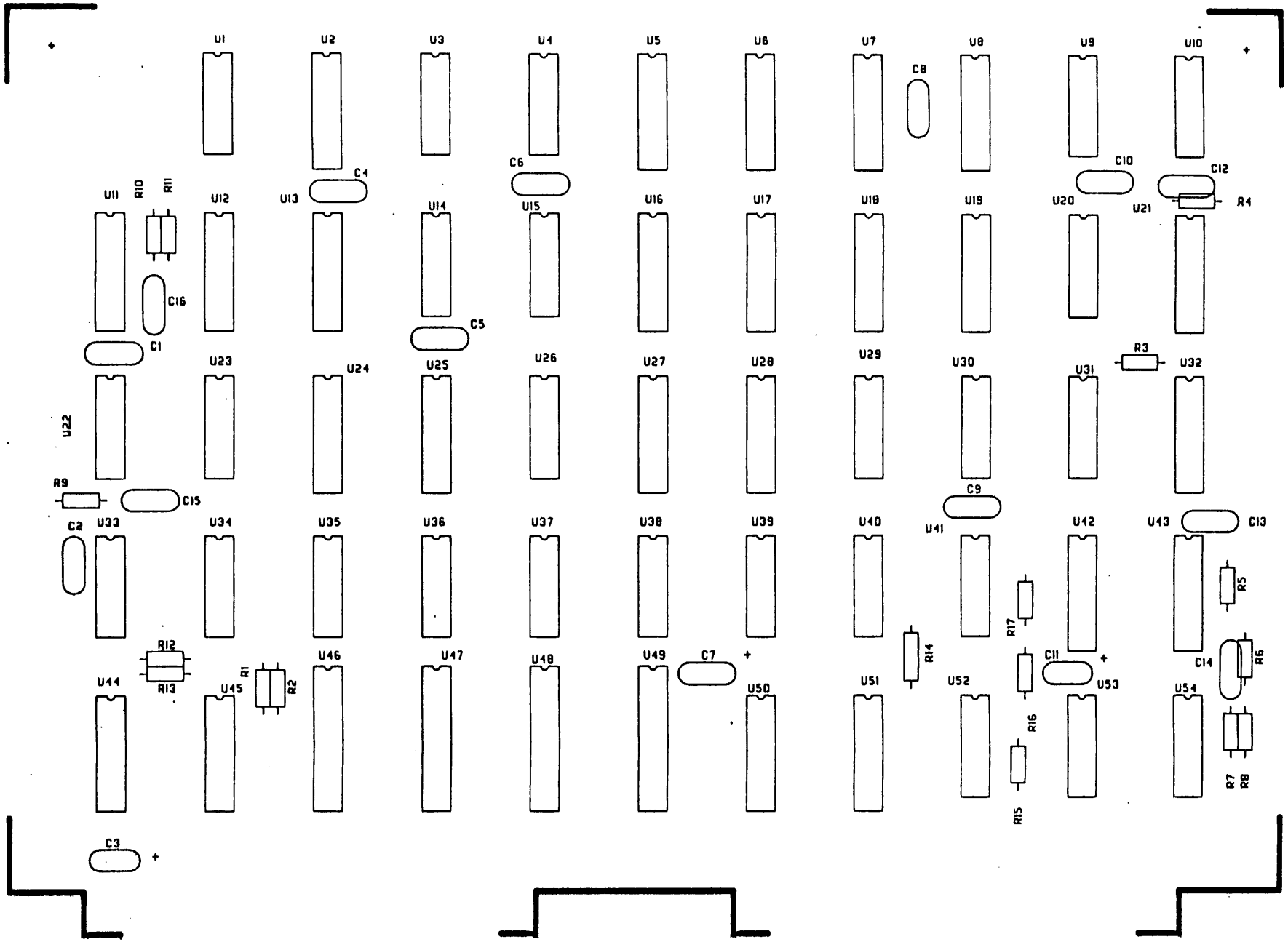
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	UM	ITEM TYP	OPT NCR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	113-0002-0000	I.C. N74S00N U25 U35		2.000	EA	4C				8/07/81	
	04	113-0002-0002	I.C. 74S02 U31 U37		2.000	EA	4C				8/07/81	
	05	113-0002-0008	I.C. 74S08 U3 U26		2.000	EA	4C				8/07/81	
	03	113-0002-0032	I.C. 74S32 U23		1.000	EA	4C				11/03/81	
	05	113-0002-0051	I.C. 74S51 U14 U41		2.000	EA	4C				8/07/81	
	04	113-0002-0064	I.C. 74S64 U4 U29 U36 U39		4.000	EA	4C				8/07/81	
	05	113-0002-0074	I.C. 74S74 U9 U13 U15 U22 U30 U34 U40 U53 U54		9.000	EA	4C				11/03/81	
	05	113-0002-0086	I.C. 74S86 U52		1.000	EA	4C				8/07/81	
	03	113-0002-0162	I.C. 74S162 U5 U6 U7 U8		4.000	EA	4C				8/07/81	
	05	113-0002-0169	I.C. 74S169 U43		1.000	EA	4C				8/07/81	
	03	113-0002-0189	I.C. 74S189 AM27S03 U16 U17 U18 U19 U21		5.000	EA	4C				8/07/81	
	05	113-0003-0000	I.C. 74LS00 U1		1.000	EA	4C				8/07/81	
	04	113-0003-0010	I.C. 74LS10 U33		1.000	EA	4C				8/07/81	
	06	113-0003-0138	I.C. 74LS138 U44 U45		2.000	EA	4C				8/07/81	
	05	113-0003-0161	I.C. 74LS161 U11 U12 U24		3.000	EA	4C				8/07/81	
	04	113-0003-0164	I.C. 74LS164 U38		1.000	EA	4C				8/07/81	
	05	113-0003-0191	I.C. 74LS191 U2 U50 U51		3.000	EA	4C				8/07/81	
	05	113-0003-0244	I.C. 74LS244 U42 U49		2.000	EA	4C				8/07/81	
	05	113-0003-0374	I.C. 74LS374 U46 U47		2.000	EA	4C				8/07/81	
	04	113-0042-0001	I.C. SCL4015?? U17 U25 U27 U28 U35		5.000	EA	4C				8/07/81	

PARENT ITEM	CROSS REF ITEM	DESCRIPTION 1K STATE CONTROL PC ASSY I/S	BATCH QTY 1	ITEM TYPE 1	LOW LEVEL 01
143-0128-0001		ENGR DRAW ECO 434 REV B	EFFEC 12/08/82	UNIT MEAS EA	PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	113-0200-0125	I.C. MC10125 (42)		1.000	EA	4C				8/07/81	
	02	143-0128-0090	1K STATE CONTROL PC ASSY O/S	ECO 434 REV B	1.000	EA	1C				8/07/81	

PARENT ITEM	CROSS REF ITEM	DESCRIPTION	BATCH QTY	ITEM TYPE	LOW LEVEL
143-0126-0090		1K STATE CONTROL PC ASSY O/S ENGR DRAW ECO 434 REV B	1 EFFEC 12/08/82	1 UNIT MEAS EA	02 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R3 R4 R5 R6 R7 R8		6.000	EA	4C				6/07/81	
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R10 R11 R12 R13 R14 R15 R16 R17		8.000	EA	4C				11/03/81	
	07	110-0005-0079	4.7K OHM 1/4W 5% CF RES R1 R2 R9		3.000	EA	4C				6/07/81	
	06	111-0004-0072	.1 UF 25V CO CAP C1 C2 C4 C5 C6 C7 C8 C9 C10 C13		10.000	EA	4C				8/07/81	
	05	111-0012-0030	100 PF 1KV CO CAP C12 C14		2.000	EA	4C				8/07/81	
	06	111-0012-0039	330 PF 1KV CO CAP C15		1.000	EA	4C				8/07/81	
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C3 C11		2.000	EA	4C				8/07/81	
	06	115-0003-0001	SOCKET 14PIN U1 U3 U4 U9 U10 U20 U26 U22 U28 U29 U30 U31 U33 U34 U35 U36 U37 U38 U39 U40 U41 U52 U53 U54 U14 U15		26.000	EA	4C				11/03/81	
	05	115-0005-0001	SOCKET 16PIN U2 U5 U6 U7 U8 U11 U12 U13 U16 U17 U18 U19 U21 U24 U25 U27 U28 U32 U42 U43 U44 U45 U50 U51		24.000	EA	4C				8/07/81	
	05	115-0009-0001	SOCKET 20PIN U46 U47 U48 U49		4.000	EA	4C				8/07/81	
	03	125-0126-0001	1K STATE CONTROL PC BAR	ECO 501 REV B	1.000	EA	4C					

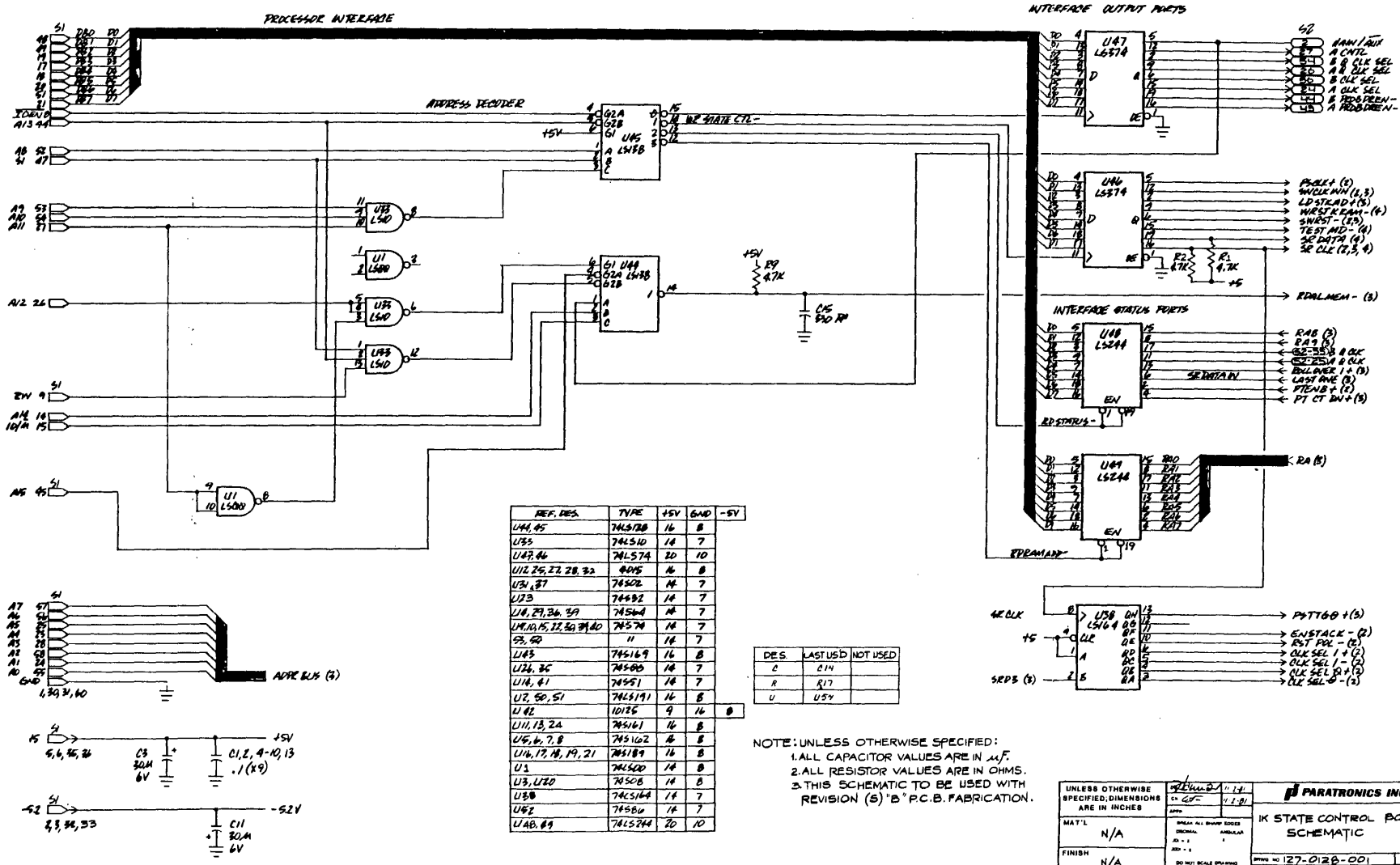


1K Control

NICOLET PARATRONICS

126-0128-0201 Rev. B

REV	DESCRIPTION	BY	DATE	APPROVED
A	RELEASE PER ECO 501			
B	REV PER ECO 623			



REF. DES.	TYPE	+5V	GND	-5V
U44, 45	74LS138	16	8	
U33	74LS10	14	7	
U47, 46	74LS74	20	10	
U12, 25, 27, 28, 32	8095	16	8	
U31, 37	74S02	14	7	
U23	74S32	14	7	
U18, 29, 36, 39	74S64	14	7	
U9, 10, 15, 17, 30, 31, 40	74S74	14	7	
53, 60	"	14	7	
U43	74S169	16	8	
U26, 35	74S00	14	7	
U16, 41	74S51	14	7	
U2, 50, 51	74LS191	16	8	
U42	10136	9	16	8
U11, 13, 24	74S161	14	8	
U5, 6, 7, 8	74S162	16	8	
U14, 17, 18, 19, 21	74S189	16	8	
U1	74LS00	14	8	
U3, U20	74S08	14	8	
U38	74LS164	14	7	
U62	74S86	14	7	
U48, 49	74LS244	20	10	

DES.	LAST USD	NOT USED
C	C14	
R	R17	
U	U54	

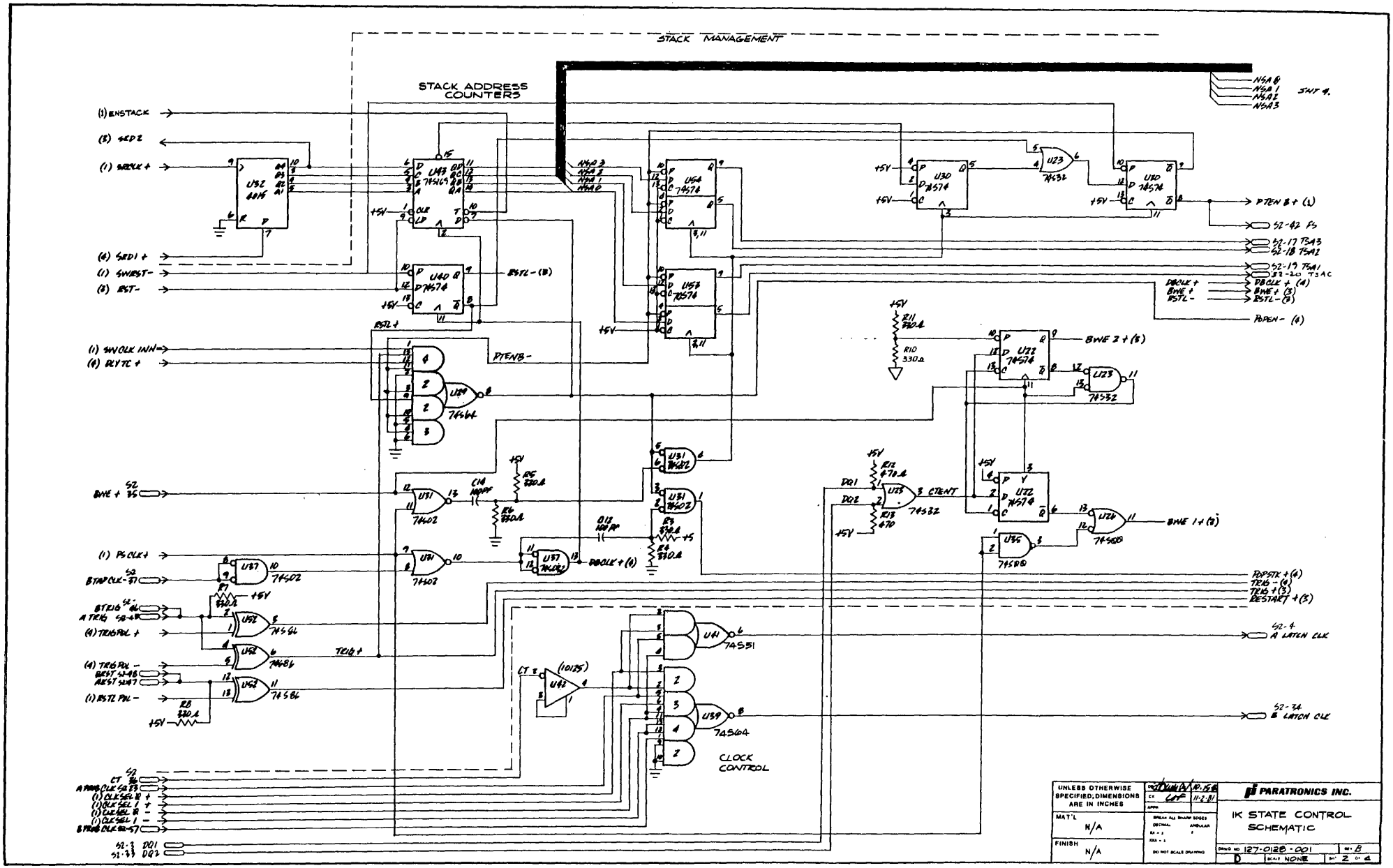
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	DRAWN	11-1-81
MAT'L N/A	BREAK ALL SHARP EDGES DECIMAL ANGULAR .XX ± .1 .XXX ± .1	
FINISH N/A	DO NOT SCALE DRAWING	

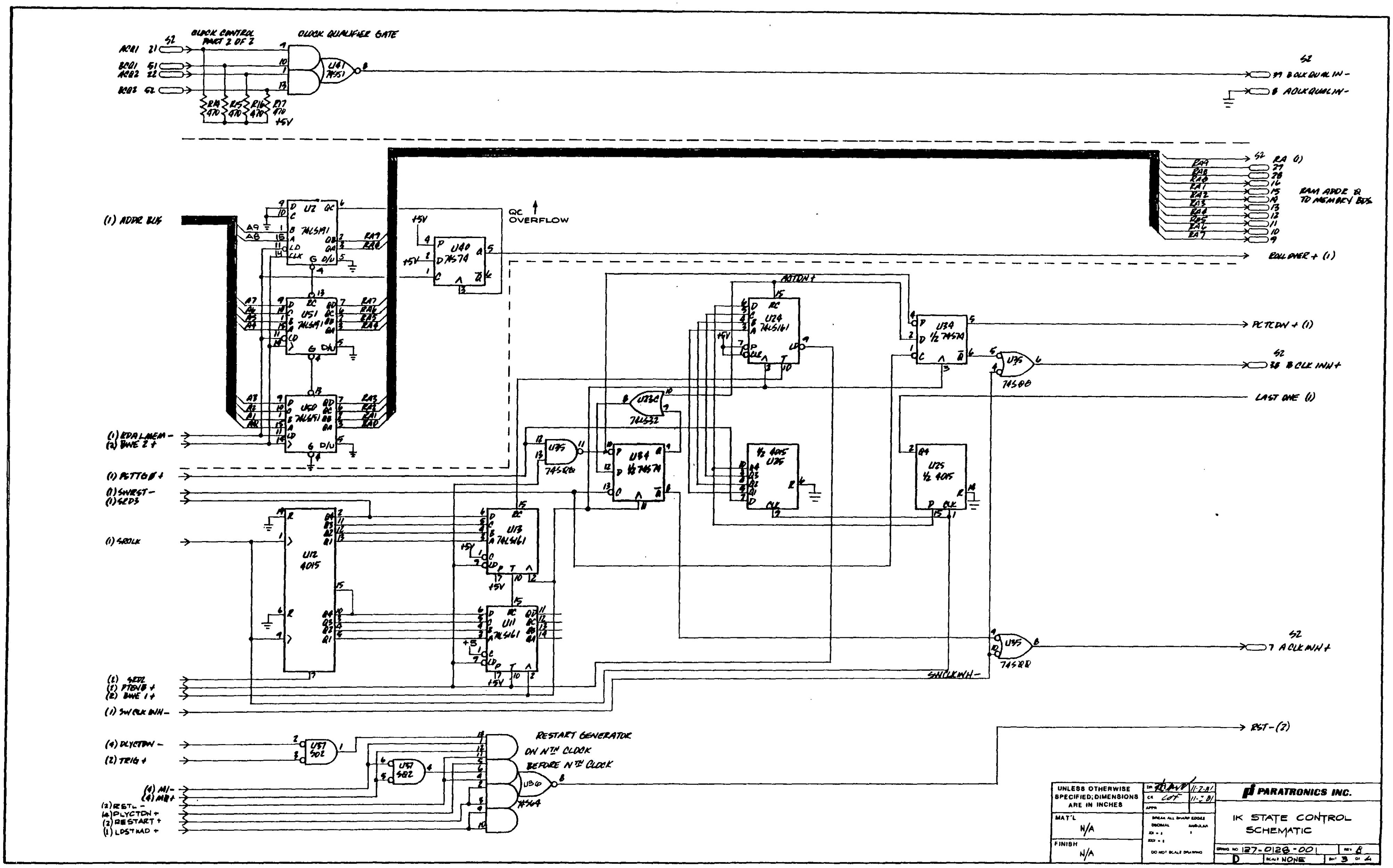
PARATRONICS INC.

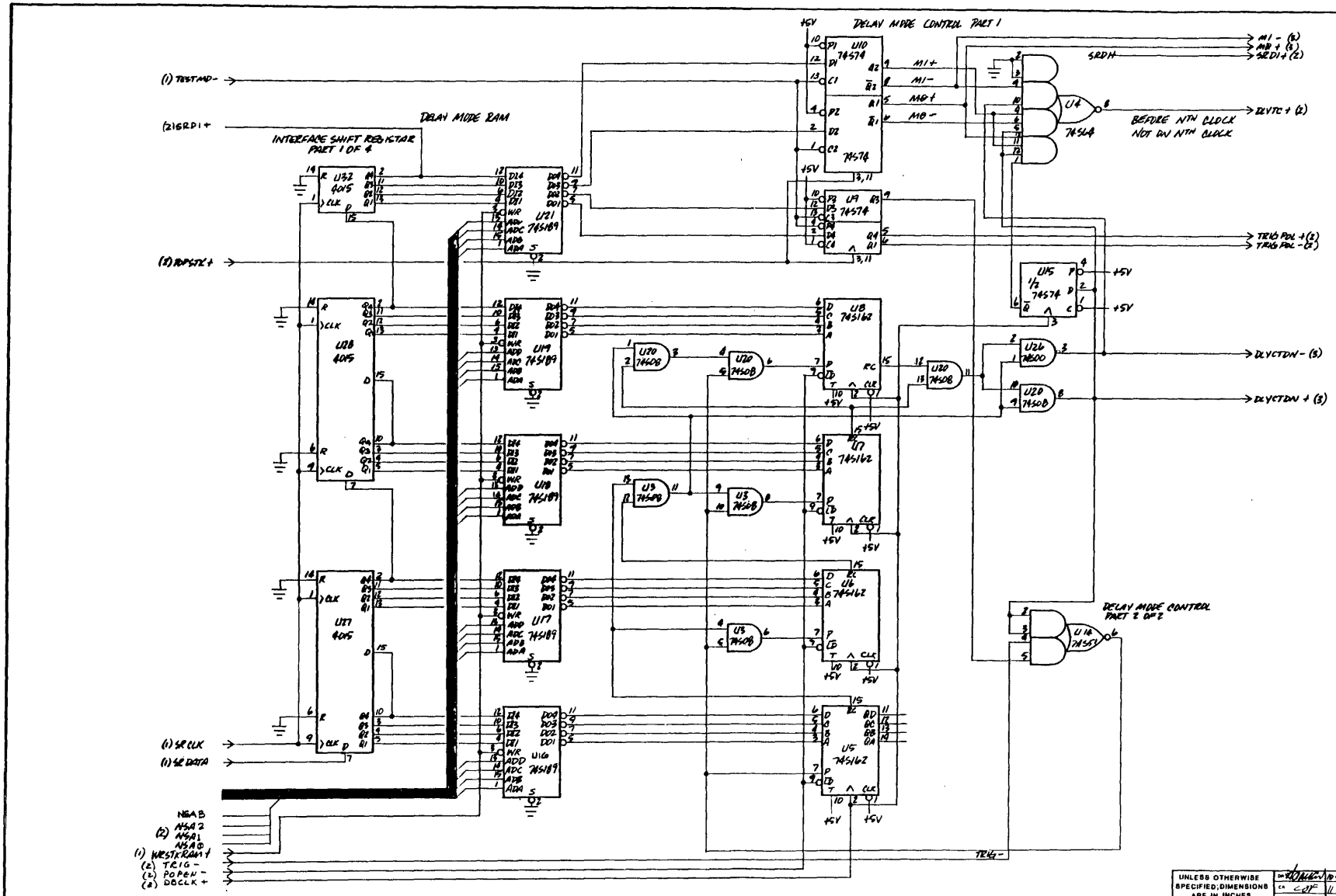
IK STATE CONTROL BOARD SCHEMATIC

DRWG NO 127-0128-001 REV B

D SCALE NONE SHT 1 OF 4


STACK MANAGEMENT
STACK ADDRESS COUNTERS
(1) ENSTACK
(8) SEDZ
(1) SECLK +
(6) SEDI +
(1) SWRST -
(8) RST -
(1) SWCLK IN
(6) RLYTC +
(1) PS CLK +
BTRIG
A TRIG
(4) TRIG POL +
(4) TRIG POL -
(1) RSTZ POL -
CT
(1) CLK SEL B +
(1) CLK SEL B -
(1) CLK SEL A +
(1) CLK SEL A -
SZ-1 DQ1
SZ-33 DQ2
NSA 3
NSA 2
NSA 1
NSA 0
NSA 0
NSA 1
NSA 2
NSA 3
SHT 4.
PTEN B + (1)
SZ-17 TSA3
SZ-18 TSA2
SZ-19 TSA1
SZ-20 TSA0
DBCLK + (4)
BWE + (3)
RSTZ - (8)
PDPEN - (4)
BWE 2 + (5)
BWE 1 + (5)
PDPSTR + (4)
TRIG - (4)
TRIG + (3)
RESTART + (5)
SZ-4 A LATCH CLK
SZ-34 B LATCH CLK
CLOCK CONTROL
PTENB -
RSTZ + (8)
RSTZ - (8)
DBCLK + (4)
U82 4016
U83 74S163
U84 74S74
U85 74S74
U86 74S74
U87 74S02
U88 74S32
U89 74S74
U90 74S74
U91 74S64
U92 74S02
U93 74S02
U94 74S02
U95 74S08
U96 74S08
U97 74S02
U98 74S32
U99 74S74
U100 74S32
U101 74S02
U102 74S86
U103 74S86
U104 74S51
U105 74S64
U106 (10125)
R10 330Ω
R11 330Ω
R12 470Ω
R13 470
R14 330Ω
R15 330Ω
R16 330Ω
R17 330Ω
R18 330Ω
C14 .0047F
C15 .001F
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
DO NOT SCALE DRAWING
PARATRONICS INC.
1K STATE CONTROL SCHEMATIC
DWG NO 127-0128-001
REV B
SCALE NONE
SHT 2 OF 4


CLOCK CONTROL PART 2 OF 2
CLOCK QUALIFIER GATE
(1) ADDR BUS
QC OVERFLOW
RAM ADDR TO MEMORY BUS
RESTART GENERATOR
ON Nth CLOCK
BEFORE Nth CLOCK
PCTCDN + (1)
LAST ONE (1)
RST - (2)
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DO NOT SCALE DRAWING
PARATRONICS INC.
1K STATE CONTROL SCHEMATIC
127-0128-001
SCALE NONE



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
MAT'L N/A	CK		1K STATE CONTROL SCHEMATIC
FINISH N/A	APPR		DRWG NO 127-028-001 REV B
DO NOT SCALE DRAWING			D SCALE NONE SHT 4 OF 4

STATE MEMORY BOARD

SECTION VIII
STATE MEMORY BOARD

8.1 INTRODUCTION

The State Memory Board accepts data from 16 incoming data lines. If directed by State Control, the data is stored for later analysis and display. The NPC 764 contains three State Memory Boards. Each board receives 16 data lines from the associated Probe Pod A, B, or C. The boards are designated State Memory Board A, B and C, respectively. The three boards are identical and interchangeable. However, certain connections to the Function Motherboard sockets plugged into each allocated socket operate differently. The following discussion will apply to all the State Memory Boards, except as noted.

8.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Control Board is shown in Figure 8-1. When appropriate also refer to the schematic diagram, board layout and parts list at the end of this section. Tables of connector pins versus signal names for motherboard connectors are provided in SIGNAL AND INTERCONNECTION TABLES. An alphabetical list of all interboard signals is included. The GLOSSARY section offers explanations for acronyms or terms that may be unfamiliar.

Major functional units of the State Memory Board circuitry include the following: Qualifier-Word RAM, Trigger-Word RAM, Data-Collection RAM, AUX RAM, Address Decoder, Clock Generator, and I/O buffers.

The qualifier-word memory and trigger-word memory can be considered as comparison devices. The data-collection and auxiliary RAM memory are typical storage devices. These memories operate as described below.

The Control Program stores the two menu-specified clock-qualifier words in the Qualifier-Word RAM. It also stores all the specified trigger words, level by level, in the Trigger-Word RAM. At run-time, an incoming data word is clocked into the Probe Input Buffer by the primary external clock. A data word consists of 18 parallel bits. These are comprised of 16 data bits and two qualifier bits. From the buffer, the data is sent to the Qualifier-Word RAM and the Trigger-Word RAM. The data is sent later to the Data Collection RAM.

The Qualifier-Word RAM compares the data word received with the two clock-qualifier words. The Trigger-Word RAM compares the incoming data word with the trigger word at the current trigger stack level. If the data word matches either of the clock-qualifier words, the current clock period is considered qualified for data collection. Then the data in the Probe Input Buffer is stored in the Data Collection RAM. In this case, the trigger-word comparison that took place concurrently with the Qualifier-Word comparison is processed.

If the qualifier-word comparison does not qualify the current clock period, the data word is not stored in the Data Collection RAM. Note that the menu may be specified with all bits as "don't care" Xs. In that case all clock periods will qualify.

This operation is described further in the following subsections.

8.2.1 INPUT/OUTPUT BUFFERS

Refer to schematic #127-0127-001, sheet 1. The Input/Output Buffers are comprised of the following buffers: Probe Input Buffer, Probe Output Buffer, Setup Data Buffer, Read-TSA (Trigger Stack Address) Buffer, Collection Address Buffer, Collection Input Buffer, and Collection Output Buffer.

The **Probe Input Buffer** consists of U20 and U23, both 74S374 octal D flip-flops; and U36A, one-half of a 74S274. The 16-bits of data at the probe pod are applied to U20 and U23 via S2. The 16 data outputs are sent to three locations as follows: To the Collection Input Buffer and to address inputs on the Qualifier-Word RAM and the Trigger-Word RAM. The reason for sending this data to the address lines of the two RAMs will be discussed later.

Two qualifier bits, Q1 and Q2, are sent from the probe via S2 to two of the four inputs of U36A. The trigger output, FT, of the timing analyzer section is applied via S2 to the third input of U36A. The external input EXT, at the BNC connector on the rear panel, provides the fourth input via S2. The four outputs of U36A are sent to address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM.

U20, U23 and U36A are clocked by the menu-selected primary external clock, LATCHCLK. The signal LATCHCLK is received from the State Control Board via S2. The outputs of all three devices are enabled at pin 1 by signal DATEN- (Data Enable -). This signal is received from the Address Decoder U9, pin 10.

The **Probe Output Buffer** consists of U21 and U22, both 74S374 octal D flip- flops. This buffer is used to send data from the processor to optional or custom probes designed to accomodate data output.

The eight inputs of U21 (DB0-DB7) are connected in parallel with those of U22 on the Processor Data Bus. The outputs of U21 and U22 are sent in cascade via S2 to the 16 probe data lines. The 8-bit input is demultiplexed to the 16-bit output using two strobe signals, PROBEDREN 0-7 and PROBEDREN 8-15. The three-state outputs are enabled by PROBDREN (Probe Data Remote Enable) that is generated at the State Control Board.

The **Setup Data Buffer** consists of U19 and U24, both 74LS244 octal buffers and U28B, one-half of a 74LS244. This buffer is used to load set-up data into the Qualifier-Word and Trigger-Word RAMs shown on sheet 2. This is described later in the Qualifier-Word RAM and Trigger Word RAM descriptions.

The 20 buffer outputs are sent in cascade via the On-board Data-In Bus to the Qualifier-Word and Trigger-Word RAMs. The four Qualifier-Word RAM input lines are demultiplexed to 20 output lines using the five write signals, W0- through W4-. In the case of the Trigger-Word RAM, demultiplexing is accomplished with the aid of the RAM organization. The Buffer three-state outputs are enabled by STBUFEN- (Setup Data Buffer Enable -). This signal is sent from the Address Decoder.

The **Read-TSA Buffer** consists of U28A, one-half of a 74LS244 octal buffer. It is used by the processor to read the trigger stack address supplied to the Trigger-Word RAM by State Control. The four input signals (TSA0-TSA3) are received from the State Control Board via P2. The four output lines of U28A are loaded onto the Processor Data Bus. The outputs are enabled by signal RDSTK- (Read Stack -) received from the Address Decoder.

The **Collection Address Buffer** consists of U3 and U8, both 74LS373 octal D latches. The 10 input signals (RA0-RA9) are received by U3 and U8 via S2 from the State Control Board. They are sent to the 10 address inputs of the Data Collection RAM U4-U7. If the current clock period is qualified for data collection, the RA signal is latched into the buffer. The latching is caused by the negative-going WE- (Write Enable-) pulse received from the Clock Generator (Q-output at flip-flop U10). This data collection address is held by the Collection Address Buffer for the duration of the WE-pulse. Signal WE- is also the write pulse for the Data Collection RAM.

The **Collection Input Buffer** consists of U12 and U16, both 74S374 octal D flip-flops. The 16 outputs of the Probe Input Buffer are applied to the 16 inputs of the Collection Input Buffer. The 16 outputs of the Collection Input Buffer are applied in cascade to the Data Collection RAM and Collection Output Buffer. If the current clock period

is qualified for data collection, signal ACLKINH+ is sent from the State Control Board. This strobes the data at the Probe Input buffer into the Collection Input Buffer. The data is held at the outputs of the Collection Input Buffer for the duration of this pulse.

The two holding buffers (Collection Address & Input Buffers) are provided to compensate for propagation delays. The propagation delay is caused by the Clock Generator and qualification comparison. At high clock rates these delays may result in the next address and data word arriving before the current write has been completed. In this way the holding buffers allow sufficient time to complete the write to the Data Collection RAM.

The **Collection Output Buffer** consists of U13, a 74LS244 octal buffer; and U14, an 8304. The processor uses the Collection Output Buffer to read collected data from the Data Collection RAM and AUX RAM. This is done for purposes of data analysis and display. The eight outputs of each RAM provide the 16 data inputs. The eight output lines are loaded onto the 8-bit Processor Data Bus. Signals 0-7EN and 8-15EN and TRAN/REC received from the Address Decoder enable the buffer outputs to the bus.

8.2.2 CLOCK GENERATOR

Refer to the schematic, sheet 1. The Clock Generator consists of the following components: U1 and U2, both 50 ns delay lines with selectable delay outputs; U9 and U40, 74S04 hex inverters; U11, a 74S02 quad NOR gate (section B is used as a negative input AND gate); and U10A, one-half of a 74S74 dual D flip-flop. A low CLKQUALIN signal signifies that the current input data word is approved for data collection. When a low CLKQUALIN signal is received at U11 pin 6, the delayed data collection clock WE- (Write Enable -) is generated at U10A pin 6. The Clock Generator also provides WE+ (an inverted WE-) and DLYWE- (DeLaYed WE- clock). These signals are present at U11, pin 10 and U9, pin 2, respectively, for use by the State Control Board.

The menu-selected primary external clock, LATCHCLK is received from the State Control Board to clock the Probe Input Buffer. LATCHCLK also is sent via U9F to the delay line U1. After a nominal delay of 40 ns, U1 sends the clock pulse to the clock input of flip-flop U10A via U9D. If the output of U11B is high (by a low CLKQUALIN at the input), the flip-flop is set by the delayed clock. After a nominal 40 ns delay, the clock is reset by the feedback chain via delay line U2. The resulting 40 ns pulses are sent from the Q and Q- outputs of the flip-flop to inverters U11C and U11D. They also are sent as clock signals WE+ and (WE+RDALLMEM)-. The Q output is delayed further by U2 and provided via inverter U9A as clock signal DLYWE- (Delayed Write Enable-).

Generation of all three clock outputs is terminated when CLKINH+ goes high. The CLKINH+ signal is sent to the input of U11A, holding flip-flop U10A reset. This condition occurs when data collection has been completed or when the FORCE DISPLAY keyboard key is depressed.

8.2.3 ADDRESS DECODER

The Address Decoder (sheet 1) consists of the following components: U25, a 74LS138 3-to-8 decoder; U32A, one-half of a 74LS138 3-to-8 decoder; U17, a 6308-1 256-word x 8-bit PROM; and U9E, one section of a 74S04 hex inverter. The processor has access to the State Memory Board via the common Address and Data bus. U32A decodes the upper three bits of the address, enabling the PROM to generate eight control signals. The specific functions of the signals depend on the eight input controls. These controls and their functions are as follows:

a. **A12 and A11** -- determine which of the three memory boards (A, B, or C) is being accessed by the processor.

b. **A10** -- determines whether the upper byte (8-15) or lower byte (0-7) is being accessed by the processor.

c. **CSEL and BSEL** -- identify by ground or voltage, in which of the three

slots (A, B or C) the memory board is inserted. If the A memory is accessed by the processor, no control signals will be generated in the B and C memory slots. The A memory BSEL, CSEL levels combined with the A Memory Address on A15, A14, A13, A12 and A11, control these signals.

d. S1 -- distinguishes between processor read and write commands.

e. I/O/Mem -- distinguishes between I/O and Memory addresses.

f. Main/Aux -- determines whether the collection (main) memory or the Aux memory is being accessed. They both have identical addresses. The Main/Aux signal is received from a State Control Board I/O bit.

The control signals that are generated by the Address Decoder are as follows:

a. 8-15EN (8-15 Enable) -- enables the upper data byte (main memory only) onto the Processor Data Bus via buffer U13.

b. 0-7EN (0-7 Enable) -- enables the lower main memory byte or the Aux Memory byte onto the Processor Data Bus via bi-directional buffer U14. The lower byte can be a read or write.

c. AUX OE -- enables the Aux Memory for a read operation.

d. RDALLMEM- (Read All Memory) -- enables all main memories on all Memory Boards for a read. The proper Memory Board is selected by the 8-15 and 0-7 enables.

e. AUX CS- -- selects the Aux Memory for read or write operation.

f. AUX WE/T/R- -- selects the Aux Memory for a write operation. Also places the U14 processor interface buffer in the write (receive) direction.

g. STBUFEN- (Setup Data Buffer Enable) -- enables decoder U25 to write the Qualifier-Word RAM, the Trigger-Word RAM, or probe outputs U21 and U22.

h. RD STK- (Read Stack Address) -- enables the Trigger Stack Address (trig level) onto the Processor Data Bus.

8.2.4 DATA COLLECTION RAM

The Data Collection RAM (sheet 1) consists of U6, U7, U14 and U15, all 2149H 1k-word x 4-bit static RAMs.

The 10 outputs of the Collection Address Buffer are applied to the 10 address lines of the four 1kx4 RAMs. The 16 output lines of the Collection Input Buffer are cascaded to the four sets of four data-in lines of the RAMs. U6 is at the high order end.

In the collection or write mode, the WE (write enable) sent to the RAMs is held low. The WE- signal sent from the Clock Generator is applied in parallel to the chip select inputs of the RAMs. Therefore, in the write mode, the RAMs act as a single 1024-word x 16-bit RAM. 16-bit data words, sent from the Collection Input Buffer, are written to RAM by the WE- write pulses from the Clock Generator. The Collection Address Counter on the State Control Board provides sequential addresses via the Collection Address Buffer. ACLKINH places the RAMs in the write mode.

In the read mode, ACLKINH is high (no write enable). The RDALLMEM signal received from address decoder U17 is applied to chip select. Then data is transferred to the Processor bus via buffer U13 or U14, depending on the address selection.

8.2.5 AUX RAM

The Auxiliary RAM consists of U15, an HM6116 2048 x 8-bit RAM. The AUX RAM is used to save a data collection from the Main Memory (1024 x 16-bit RAM). The data is saved by reading it out of the main memory and

storing each byte in the AUX memory. The address for a given byte is identical for main memory or Aux memory. The processor makes the Main/Aux selection by setting an I/O bit on the State Control Board. The save routine might consist of the following partial sequence:

Output Main memory select
Read D2CF
Output Aux memory select
Write D2CF
Output Main memory select
Read D2D0
etc.

The data is read from the AUX RAM in the following manner: The 11 address lines (A0-A10) of RAM U15 are received from the Processor Address Bus. Buffer U14 is enabled in the transmit direction when a byte is read out.

Address Decoder outputs AUXWE, AUXCS- and AUXOE- are used as the write-enable, clock-select and output-enable inputs of RAM U15.

8.2.6 QUALIFIER-WORD RAM

The Qualifier-Word RAM (sheet 2) consists of U26, U27, U30, U31 and U29, all 74S289 16-word x 4-bit static RAMs. The RAMs are connected as follows: The 16 data lines from the output of the Probe Input Buffer are divided into four sets of four lines. Four address inputs are sent to each of the four RAMs, U26, U27, U30 and U31. The four most significant bits are applied to the four address inputs of U26. Four qualifier signals Q1, Q2, FT, EXT, are sent from the Probe Input Buffer to the address lines of RAM U29.

Each RAM has 16 possible combinations of four bits on the address lines. These bits address the 16 word locations in the RAM. Thus any given combination of values of the four probe input bits will be unique. This combination will address a unique word location in the specified RAM. Each word location contains four storage bits. These four bits are assigned as follows: Bit 0 to the ARM word; bit 1 to the CQ1 clock-qualifier word; bit 2 to the CQ2 clock-qualifier word; bit 3 to the RESTART word.

NOTE: The ARM word is used only in the Counter Timer/Signature Board. It is the first of the two trigger words shown on the respective menus. The Arm Comparator output is buffered and sent to a rear panel BNC. As an example, assume that a menu has specified, in binary format, the following first clock-qualifier word:

0110 001X XXXX XXXX XXXX XXXX -1XXXXXX XX

The Control Program places the four most significant bits, 0110, on the address inputs of RAM U26. This is accomplished via the Setup Data Buffer. A 1 is written into the CQ1-word bit position (the second bit position). This is done via the D11 input of the RAM using write enable W3- sent from the Address Decoder. The Control Program also writes into the other three bit positions for the ARM, CQ2, and RESTART words.

The 1 that is written into the 0110, bit-1 location means match. The Control Program writes a 0 (no match) into bit 1 of the other 15 words in RAM U26. Thus when the four MSBs of the incoming data are 0110, RAM U26 will output a 1 from D01. For all other bit combinations a 0 will be output from D01.

The next set of four bits, 001X, are used to address RAM U27. The Control Program writes a 1 into bit 1 of the words at addresses 0010 and 0011. This is done because the LSB of this set is a "don't care" X. A 0 is written into bit 1 of the remaining 14 words. For RAMs U30 and U31, the Control Program writes a 1 into bit 1 of all 16 words. This is done since all four address bits are Xs. RAM U29 is addressed by the qualifier-bit group, 1XXX. A 0 is written into bit 1 of the eight word locations addressed by 0000 through 0111. A 1 is written into bit 1 of the eight word locations addressed by 1000 through 1111.

Assume that at run time the data word shown below is clocked into the Probe Input Buffer. The data is clocked by LATCHCLK and placed on the address inputs of the five

RAMs in the Qualifier-Word RAM. Refer to Figure 8-1.

	U26	U27	U30	U31	U29
	====	====	====	====	====
Data Word	0110	0011	1010	0001	000000
Menu Word	0110	0011	XXXX	XXXX	XXXXXX

The Control Program loads a 1 in bit 1 at address 0110, for RAM U26. This provides a match making D01 a 1. Similarly, Output D01 is a 1 for U27, U30, U31, and U29.

The 74S289 RAMs have open collector outputs. All four D01 outputs are tied together and applied to S2-20 as CQ1. This provides a wired AND for the four D01 outputs. For the input data word in the example, signal CQ1 is high (logic 1).

RAM outputs CQ1, CQ2 of U26, U27, U30, U31 (data clock qualifiers) differ from CQ1, CQ2 or U29 (probe clock qualifiers). A data clock qualifier will inhibit collection of an unqualified data word. It will not inhibit the generation of a data trigger signal. A probe clock qualifier will inhibit both data collection and trigger generation.

Now assume that the following data word is received.

	U26	U27	U30	U31	U29
	====	====	====	====	====
Data Word	0110	0010	0000	1111	000000
Menu Word	0110	0011	XXXX	XXXX	XXXXXX

This word produces a 0 at the D01 output U26, and signal CQ1 goes low.

The Qualifier-Word RAM provides four output signals, ARM, CQ1, CQ2 and RESTART. They are sent to connector pins S2-20, 19, 18, and 17, respectively. Signals CQ1 and CQ2 are used by Clock Control on the State Control Board. This is shown on sheet 3 of the schematic. Signal RESTART is used by the RESTART Generator on the State Control Board. The ARM signal is a linkage from the timing analyzer.

8.2.7 TRIGGER-WORD RAM

The Trigger-Word RAM (sheet 2) consists of U34, U35, U38, U39 and U37. These are all Signetics 82S117 256-word x 1-bit static RAMs. The 256 1-bit word locations in each RAM are addressed by eight address inputs, A7-A0.

The Trigger-Word RAM inputs are configured in a similar manner as the Qualifier-Word RAM inputs. The 16 data lines output from the Probe Input Buffer are divided into four sets of four lines. One set is sent to address inputs A3-A0 (Q1,Q2,FT,EXT) of each of the four RAMs, U34, U35, U38 and U39. The four qualifier lines output from the Probe Input Buffer are sent to address inputs A3-A0 of U37. Trigger Stack Address lines TSA3-TSA0 are received from the State Control Board. These signals are applied as address inputs A7-A4 of the five RAMs. These four address bits (TSA3-TSA0) are decoded into 16 blocks of 16 locations each. Each block represents one of the 16 trigger stack levels on the menu.

The Trigger-Word RAM performs the comparison function in much the same way as the Qualifier-Word RAM. The bit organization differs between the two. For example, start at level 0 of the trigger stack. As before, the incoming 20-bit data word is divided into five 4-bit groups. Each group feeds four address inputs of one of the five RAMs. These four bits address 16 locations. As in the Qualifier-Word RAM, each location represents one of 16 possible combinations of 1s and 0s for the four bits.

As with the Qualifier-Word RAM, each location is loaded at set-up time with a 1 or a 0. This provides a "match" or "no match", according to the bit configuration of the trigger word at stack level 0. As before, the five RAM outputs are connected in a wired AND configuration. Thus there must be a match for all five 4-bit groups of the incoming data word. This will produce a TRUE output from the Trigger-Word RAM.

The four search words in the Qualifier-Word RAM are ARM, CQ1, CQ2 and RESTART. All must be compared with the incoming data word

simultaneously. Each search word is assigned a bit in the RAM output word. In the Trigger-Word RAM, the 16 search words are not compared simultaneously. Only the trigger word at the current trigger stack level is compared. Each of the 16 search words is assigned a block of 1-bit RAM words. The proper block is selected by the 4-bit Trigger Stack Address received by the A7-A4 inputs of each RAM.

A comparison is made as the Trigger Stack Address at the A7-A4 inputs of each RAM advances to the next higher stack level. At each advance the four bits at the A3-A0 inputs are shifted to the next block of 16 stored bits. One bit is required for each of the 16 possible combinations of the four input data bits. At any given stack level, the five RAMs appear as a Qualifier-Word RAM having only one qualifier word.

The 82S117 RAMs have open collector outputs. All five single-bit outputs are wire ANDed to produce the output signal TRIG+ (Trigger +) at connector pin S2-16. The TRIG+ signal is used by Stack Management on the State Control Board. The pull-up resistor for the wired AND is on the State Control Board. The RAM output is sent to U33B, translated to ECL level, inverted, and applied to S2-10 as signal ST- (State Trigger -).

8.3 BOARD A, BOARD B AND BOARD C

The differences in function between boards plugged into the A slot, B slot and C slot are discussed in the following paragraphs.

8.3.1 QUALIFIER BITS

There are two qualifier lines received from each of the three probe pods. Those coming from Pod A connect to Board A, Pod B to Board B, and Pod C to Board C. The EXT qualifier and LINK are applied to Boards A, B and C. These four signals are sent to each board at the inputs to U26A in the Probe Input Buffer. The term names of these signals are Q1, Q2, EXT and LINK.

On the menu, the qualifier bits displayed as follows:

-XXXXXX XX

The formatting is shown on the menu Clock Select line as follows:

QUALIFIERS: -AABBCCEL

With additional identification of signal names, the menu format is as follows:

QUALIFIERS: -AQ1,AQ2,BQ1,BQ2,CQ1,CQ2
EXT,LINK

The signals at the Probe Input Buffer, Qualifier-Word RAMs and Trigger-Word RAMs are as shown below:

AQ2,AQ1,EXT,LINK (for Board A)
BQ2,BQ1,EXT,LINK (for Board B)
CQ2,CQ1,EXT,LINK (for Board C)

The input qualifier lines, Q1 and Q2, are distinct from the outputs of the Qualifier-Word RAM, -CQ1 and -CQ2. For either the A or B Board, the -CQ1 output represents the result of the comparison of the following two words: An entire input data word and the entire menu-specified first clock-qualifier word, including both the Q1 and Q2 bits. Similarly, the -CQ2 output represents the result of the comparison of the following two words. An entire input data word and the entire menu-selected second clock-qualifier word, including both the Q1 and Q2 bits.

8.3.2 SIGNAL CLKQUALIN

CLKQUALIN- (Clock Qualifier In -) is the signal that enables the Clock Generator. This is done by enabling Write Enable signal WE- (State Memory Board) and WE+ and DLYWE- clock pulses (State Control Board). Signal WE- is the pulse that causes the current 16-bit data word to be stored in the Data Collection RAM. The CLKQUALIN- signal to State Memory Boards A and B, ACLKQUALIN- and BCLKQUALIN-, are wired to a constant low (true) level. Refer to the Clk Qual Gate at the top of sheet 3, State Control Board

schematic. Thus the State Memory Boards at the A or B sockets will collect a 16-bit data word at every occurrence LATCHCLK. This is true regardless of the outcome of the clock-qualifier comparison. Note that the CWE+ and CDLYWE- clocks that drive State Control are received from Board C. These clocks are generated only when CCLKQUALIN- is low. Signal CCLKQUALIN- is low when either of the two following statements is true. Signals ACQ1, BCQ1, and CCQ1 are high (true); or ACQ2, BCQ2, and CCQ2 are high. ACQ1 is the first clock-qualifier word signal sent from Board A, BCQ1 from Board B, and so forth.

The data words collected by Board A are written one on top of the other into the same address. This continues until the clock qualification requirements set up in the Qualifier-Word RAM on Boards A, B and C are met. At that point, CCLKQUALIN- causes CWE- to be generated. Then the C data word is collected as well as the A and B data words. Signals CWE+ and CDLYWE- are also generated so that the data collection address is advanced. The next A data word (qualified or not) is sent to the new address. This preserves the qualified A data word in the previous address.

8.3.3 SIGNAL CLKINH

The Clock Generator on the State Memory Board can be inhibited from producing the WE family of clocks. This is done using signal CLKINH+ (Clock Inhibit +) received from State Control. State Control generates three such signals described as follows: Signals ACLKINH+ at Board A, BCLKINH+ at Board B, and CCLKINH+ at Board C.

Boards A, B and C finish the collection at the same time. The collection is stopped by concurrent signals ACLKINH+, BCLKINH+ and CCLKINH+ received from State Control. When processing the collected data, the Control Program reads 16-bit words from equivalent addresses in Boards A, B and C. The Control Program then places them side-by-side in main memory as one 48-bit word.

8.3.4 SIGNAL BSELECT-

The Control Program can read from only one State Memory Board at a time. It must write set-up data into the Qualifier-Word RAM and Trigger-Word RAM one board at a time. This ability is provided by signal BSELECT-. This is sent via connector pin S2-15 to Address Decoder pin U2-14, with a pull-up resistor at U3-11. Connector pin S2-15 is hard-wired low at the A and B sockets, but left open at the C socket. This causes BSELECT- to be high at the C Board. The A and B boards are differentiated by inverting address line A11 that is sent to the A board. The Address Decoder responds to Board A and B addresses when the signal is low, and to Board C addresses when the signal is high.

8.4 SCHEMATIC, BOARD LAYOUT AND PARTS LIST

The schematic diagram, board layout and parts list for the State Memory Board are contained on the following pages.

PARENT ITEM 143-0127-0001 | CROSS REF ITEM | DESCRIPTION 1K STATE MEMORY BASIC PC ASSY. ENGR DRAW ECO 610 REV G | BATCH QTY 1 | EFFEC 12/08/82 | ITEM TYPE 0 | UNIT MEAS EA | LOW LEVEL 02 | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	113-0002-0002	I.C. 7402 U11		1.000	EA	4C				8/06/81	
	05	113-0002-0004	I.C. 7404 U9 U40		2.000	EA	4C				3/01/82	
	05	113-0002-0074	I.C. 7474 U10		1.000	EA	4C				8/06/81	
	05	113-0002-0373	I.C. N74S373N U3 U8		2.000	EA	4C				8/06/81	
	04	113-0002-0374	I.C. 74S374 U12 U15 U20 U23 U36		5.000	EA	4C				6/15/82	
	05	113-0003-0138	I.C. 74LS138 U25 U32		2.000	EA	4C				8/06/81	
	05	113-0003-0244	I.C. 74LS244 U13 U19 U24 U29		4.000	EA	4C				6/06/81	
	05	113-0003-0374	I.C. 74LS374 U21 U22		2.000	EA	4C				6/15/82	
	05	113-0014-0002	I.C. DP8304N NSC U14	ECO 462	1.000	EA	4C				2/02/82	
	03	113-0045-0001	I.C. 325117, AM27LS01C 93411 U34 U35 U37 U38 U39		5.000	EA	4C				8/06/81	
	03	113-0053-0001	I.C. 27S02, 74S289 U26 U27 U29 U30 U31		5.000	EA	4C				8/06/81	
	03	113-0066-0001	I.C. 16K RAM HM6116LP-4 200NS U16		1.000	EA	4C				8/07/81	
	03	113-0069-0001	I.C. 2149H RAM U4 U5 U6 U7		4.000	EA	4C				8/07/81	
	03	113-0200-0124	I.C. MC10124 U33		1.000	EA	4C				8/06/81	
	03	143-0127-0000	1K STATE MEMORY PC ASSY O/S	ECO 624 REV F	1.000	EA	1C				8/07/81	

SECTION 8: STATE MEMORY BOARD

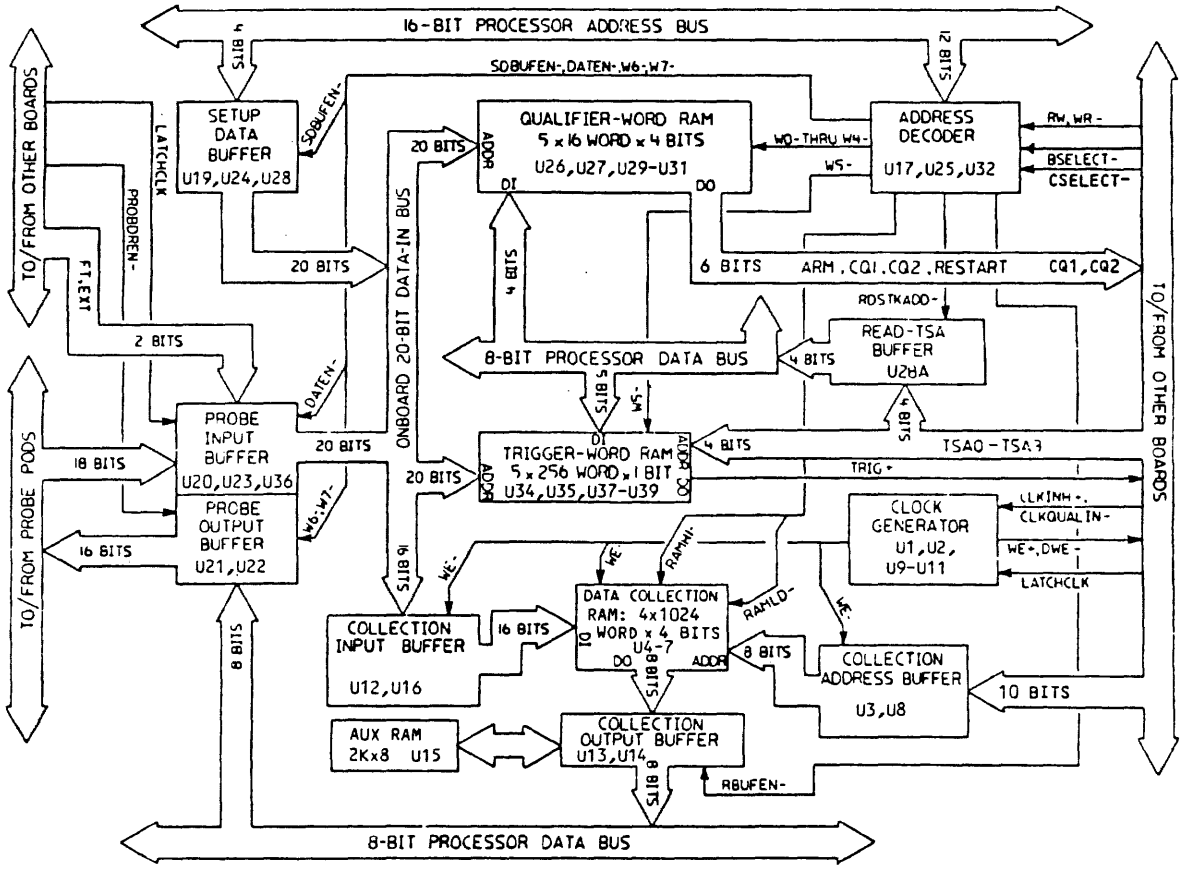
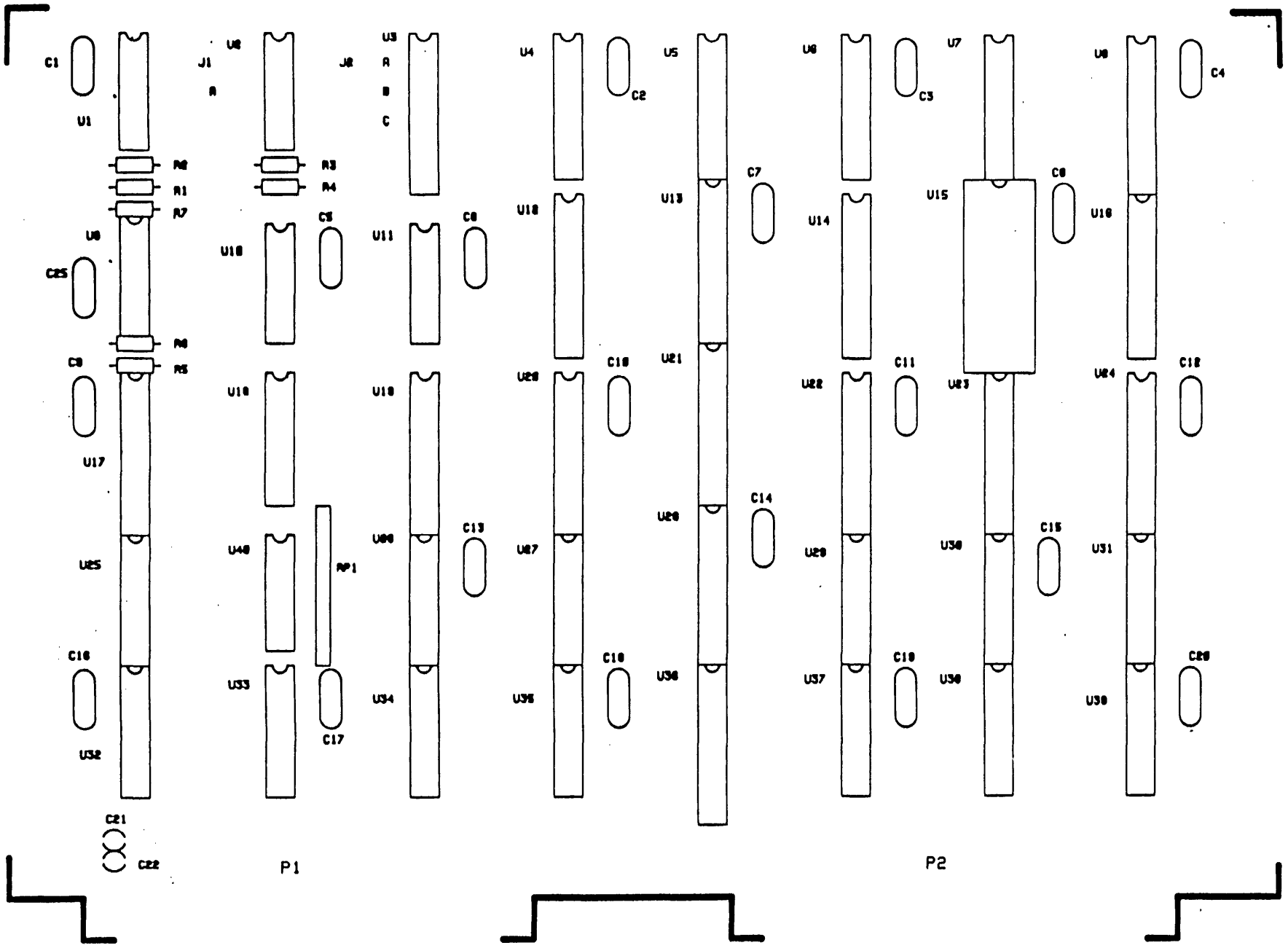


Figure 8-1 State Memory Board Block Diagram

PARENT ITEM 143-0127-0001 | CROSS REF ITEM | DESCRIPTION 1K STATE MEMORY PC ASSY O/S ENGR DRAW ECO 624 REV F | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	36	110-0005-0049	180 OHM 1/4W 5% CF RES R2 R3		2.000	EA	4C				8/06/81	
	37	110-0005-0047	220 OHM 1/4W 5% CF RES R1 R4		2.000	EA	4C				8/06/81	
	37	110-0005-0051	330 OHM 1/4W 5% CF RES R5 R6		2.000	EA	4C				8/06/81	
	38	110-0005-0063	1K OHM 1/4W 5% CF RES R7		1.000	EA	4C				8/06/81	
	05	110-0314-0031	RN 4.7K OHM X9 10 PIN SIP RP1		1.000	EA	4C				5/25/82	
	35	110-0315-0001	RN 2.2K OHM X15 16 PIN DIP U19		1.000	EA	4C				8/07/81	
	39	111-0004-0072	.1 UF 25V CD CAP C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20		20.000	EA	4C				10/07/81	
	36	111-0012-0030	100 PF 1KV CD CAP C29		1.000	EA	4C				8/06/81	
	05	111-0050-0107	33 UF 6V TANT DROP CAP C21 C22		2.000	EA	4C				8/06/81	
	05	113-0046-0001	DELAY LINE 21135 U1 U2		2.000	EA	4C				8/06/81	
	36	115-0303-0001	SOCKET 14PIN U9 U10 U11 U40		4.000	EA	4C				3/03/82	
	38	115-0005-0001	SOCKET 16PIN U25 U26 U27 U29 U30 U31 U32 U33 U34 U35 U37 U38 U39		13.000	EA	4C				11/23/81	
	36	115-0008-0001	SOCKET 18PIN U4 U5 U6 U7		4.000	EA	4C				11/23/81	
	36	115-0009-0001	SOCKET 20PIN U3 U8 U12 U13 U14 U16 U17 U20 U21 U22 U23 U24 U29 U36 U19		15.000	EA	4C				11/23/81	
	36	115-0011-0001	SOCKET 24PIN U15		1.000	EA	4C				11/23/81	
	34	125-0127-0001	1K STATE MEMORY PC FAB	ECO 497 REV 2	1.000	EA	4C					



1K Memory

NICOLET PARATRONICS

TIMING CONTROL BOARD

SECTION 9: TIMING CONTROL BOARD

SECTION IX
TIMING CONTROL BOARD

9.1 INTRODUCTION

Hardware registers, counters, and RAMs on the Timing Control Board are loaded by the Control Program. The loading is done using information entered at the keyboard with the aid of the TIMING menu. The Timing Control Board directs the collection of timing data in the Timing Memories.

9.2 FUNCTIONAL DESCRIPTION

A block diagram of the Timing Control Board is shown in Figure 9-1. Also refer to the schematic diagram, board layout and parts list that are included at the end of this section. Tables of connector pins versus signal names for all motherboard connectors are provided in SIGNAL AND INTERCONNECTION TABLES. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for acronyms or terms that may be unfamiliar.

The functional units of the Timing Control Board are as follows: The Processor Interface, Clock Generator, Clock Control,

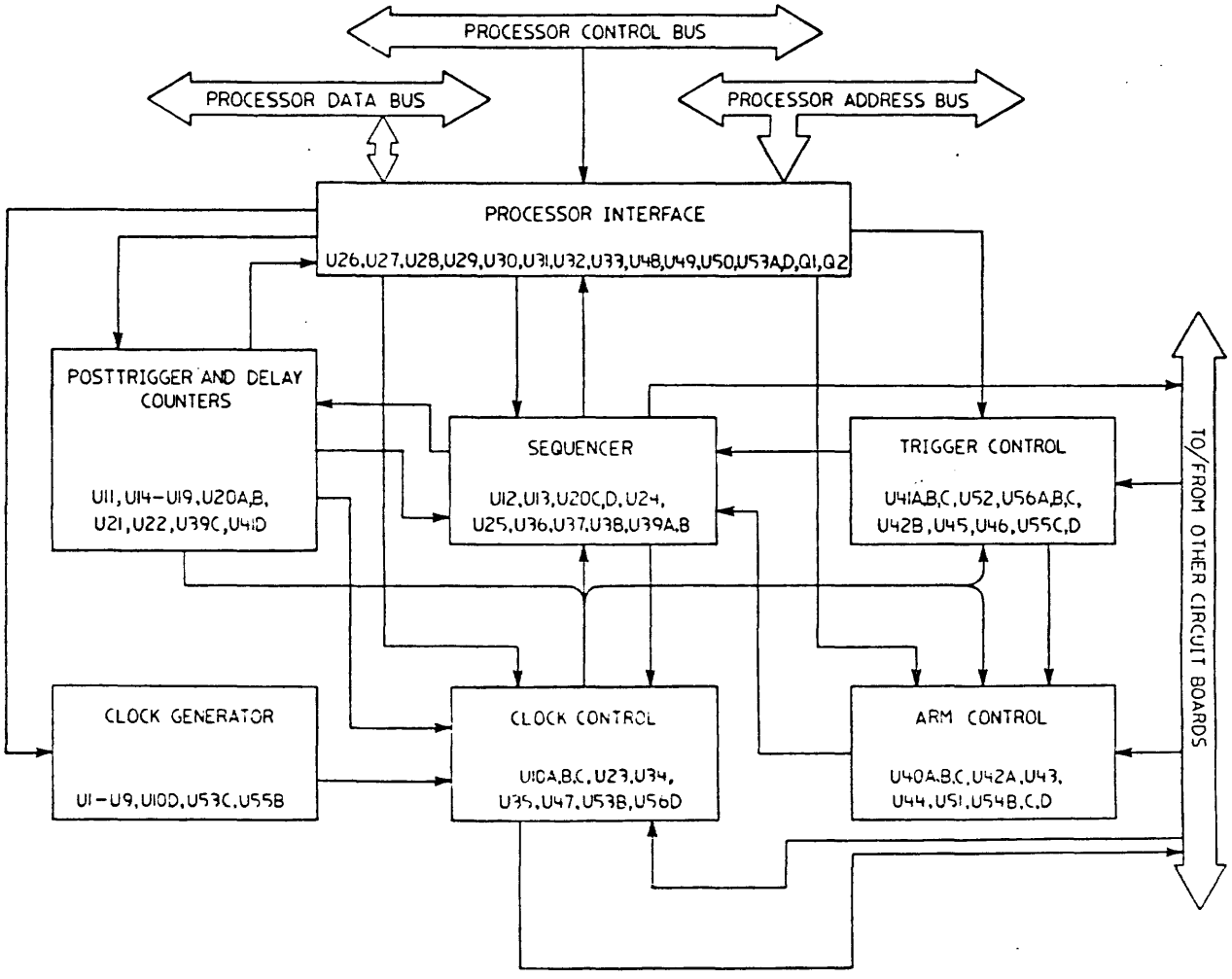


Figure 9-1 Timing Control Board Block Diagram

Trigger Control, Sequencer, Post-trigger Counter and Delay Counters. These units are discussed in detail in the following subsections.

9.2.1 PROCESSOR INTERFACE

Refer to schematic #127-0071-001, sheet 4. The Processor Interface is comprised of the following: The Address Decoder, Master Control Register, Control Shift Register, and Status Port. This circuitry allows the processor to load the register, counters and RAMs on the Timing Control Board with user-supplied information. This prepares the analyzer to execute the intended application. The processor can interrogate various status and signal lines and send control signals.

The **Address Decoder** consists of U50, a 74LS138 3-to-8 decoder. This circuit allows the processor to perform the following operations:

a. Clock the Master Control Register (with signal MCRCLK).

b. Address the Status Port (with signal RDSTAT-)

c. Send write enable signal WRRAM- to the Sequencer RAM

d. Send reset signal RESET- to the Sequencer Latch.

The **Master Control Register** consists of U49, a 74LS374 octal D flip-flop, and Q1 and Q2, both 2N3905 transistors. U49 latches control signals sent from the Processor Data Bus when clocked by MCRCLK from the Address Decoder. These signals include the following:

a. SRCLK, the clock for the Control Shift Register.

b. SRDATA, serial data for the Control Shift Register.

c. SWCLKINH, a clock-inhibit signal that allows the Control Program to stop all clocks from Clock Control when appropriate.

The remaining signals sent from the Master Control Register are high-speed control signals. These high-speed signals are too fast for the Control Shift Register to handle and are sent to the Clock Generator. The shift register data line, U49-5, doubles as a clock-select signal line when the register is not being loaded. Transistors Q1, Q2, shift signal levels from TTL to CMOS on the two signals that feed the Control Shift Register.

The **Control Shift Register** consists of eight CMOS 4015 dual 4-bit static shift registers, U26 through U33. These registers supply 63 software-generated control signals to other circuits on the Timing Control Board. The registers are loaded in series through the SRDATA line from the Master Control Register. The 63 parallel outputs are supplied at ECL-compatible levels. This method saves considerable circuit board space. Otherwise space would have been required for 62 parallel input signals and 62 level-shifting transistor circuits.

The **Status Port** consists of U48, a 74LS373 octal D latch, and U53A,D, sections of a quad ECL-to-TTL translator. Latch U48 acts as an input port that allows the processor to read the status of certain signals. U53A and D translate the levels of two ECL signals feeding the TTL latch.

9.2.2 CLOCK GENERATOR

The Clock Generator (sheet 6) is comprised of the following: The Clock Oscillator, First Stage Divider, First Stage Selector, Second Stage Divider, and Second Stage Selector. This circuitry generates internal clock pulses in discrete clock periods from 20 ns through 10 ms. The 10 ns clock period is obtained by a multiplexing scheme to be described later. These clock periods also provide the means for the Control Program to select the keyboard-specified clock period.

The **Clock Oscillator** consists of U10D, a section of a 10102 quad NOR gate; Y1, L1, C1,

R2, RP1-7, RP11-4; U9, an 10138 biquinary counter; and U53C, a section of a 10125 ECL-to-TTL translator. U10D and the associated components form an oscillator with a 100 MHz output. This 100 MHz signal is fed to both clock inputs of counter U9. U9 produces a 50 MHz signal at pin 15 and a 20 MHz signal at pin 4. The 50 MHz (20 ns) signal is the fastest clock in the complement. This 50 MHz signal is applied directly to Clock Control (sheet 8) as signal INT50 (Internal 50 MHz). The 20 MHz (50 ns) signal is translated to TTL level by U53C and sent to the First Stage Divider. It is also sent directly to the Second Stage Selector for possible selection by the Control Program.

Inductor L1 is adjusted for reliable lock to the crystal frequency of 50 MHz +/- 0.1%, as measured at pin U9-15.

The First Stage Divider consists of U1, a 74LS74 dual D flip-flop; and U8, a 74LS90 biquinary counter. By successively dividing the 50 ns input signal, this circuitry produces four clock signals. The four signals have periods of 100 ns (at U1-5), 200 ns (at U1-9), 500 ns (at U8-8), and 1000 ns (at U8-12). These signals are sent to the First Stage Selector.

The First Stage Selector consists of U2, a 74LS151 1-of-8 data selector. This circuit uses two software-generated clock-select signals CLKSELD and CLKSELE. These two signals are sent from the Processor Interface. They are used to select the pin 6 output from one of the four inputs received from the First Stage Divider. The selected output is sent to the Second Stage Divider for further processing. It is also sent directly to the Second Stage Selector for possible selection by the Control Program.

The Second State Divider consists of four 74LS90 biquinary counters, U4 through U7. Each of these counters is connected to divide-by-10 logic. The four-divider chain provides four output clock signals. The four signals have periods equal to the input period multiplied by 10 (at U4-12), 100 (at U5-12), 1000 (at U6-12) and 10,000 (at U7-12). For example, with 100 ns selected as the input, the output signals would have periods of 1 us, 10 us, 100 us and 1 ms. The four output signals are sent to the Second Stage Selector.

The Second Stage Selector consists of U3, a 74LS151 1-of-8 data selector, and U55B, a section of a 10124 quad TTL-to-ECL translator. Selector U3 receives the software-generated pseudo clock (PSEUDOCLK) on input pin 12. The 50 ns clock is received on input pin 14. The output of the First Stage Selector is received on pin 15. The outputs of the Second Stage Divider are received on pins 1,2,3 and 4. The Processor Interface feeds selector U3 inputs (pins 9, 10 and 11) with the clock-select signals CLKSELA, CLKSELB, and CLKSELC.

The Control Program can select either the pseudo clock or any one of 17 internal clocks. This is achieved by manipulating three select signals and the two signals CLKSELD and CLKSELE. The clock periods range from 50 ns through 10 ms in cascading 1-2-5 ratios. The 20 ns clock is selectable in Clock Control. The selected clock output at pin 6 is sent via U55B to Clock Control as ECL-level signal INT<50 (Internal Less Than 50 MHz).

9.2.3 CLOCK CONTROL

Clock Control (sheet 8) is made up of Qualifier Control, the Final Clock Selector, and A/B Multiplexer (Motherboard). This circuitry and the Control Program implement the clock selection. The following selections may be entered via the keyboard:

a. The choice of internal or external clock.

b. If internal, the choice of a 50 MHz or <50 Mhz. The specified value of the <50 MHz clock having been preselected in the Clock Generator.

c. If external, the choice of the positive or negative-going edge.

d. If external, the choice of 0, 1 or X for clock-qualifier polarity.

Internal to the analyzer, data is always

clocked with a positive-going clock edge. Therefore, any keyboard-entered negative-going edge must be converted to a positive-going edge for the working clock used within the analyzer. This conversion, if required, is performed by Clock Control. Also, Clock Control shuts off all analyzer working clocks at post-trigger terminal count. This is accomplished by using the clock inhibit signals from the Post-trigger Counter.

Qualifier Control consists of U10A,B,C, sections of a 10102 quad NOR gate and U47, a 10130 dual latch. Section C of U10 has an OR output, and sections A and B are used as Negative-input gates. The clock qualifier signal, QCLK+ is received from the A-channel Model 80 Probe. It is connected to one input of gate U10A. The inverted clock qualifier signal, QCLK- is received from the A-channel Model 80 Probe. It is connected to one input of gate U10B. The clock qualifier from the B-channel Model 80 Probe is not used. Gates U10A and U10B are enabled by the software-generated control signals SWQCLK0- (Software Clock Qualifier 0 -) and SWQCLK1-, respectively.

The keyboard-entered selections of 0, 1 or X for clock qualifier polarity determines how these two signals are used. The selections are implemented as described below:

a. If the choice was 0, the Control Program brings SWQCLK0- low. A low level of QCLK+ will produce a high (true) qualifier signal, QUAL, at U10C-14.

b. If the choice was 1, the Control Program brings SWQCLK1- low. A low level of QCLK- will produce a high QUAL signal at U10C-14.

c. If the choice was X, the Control Program brings both SWQCLK0- and SWQCLK1- LOW. Signal QCLK+ will produce a high QUAL at either high or low level.

Signal QUAL is sent to the D inputs of latches U47A and U47B. The common clock input (pin 9) is left unconnected so that it is pulled low internally. This allows the latches to be clocked separately. The two polarities of the external clock signal, CLK+ and CLK- are sent from the Model 80 Probe. CLK+ is sent to pin 6 and CLK- to pin 11. The latches are transparent while these clock inputs are low, and latch on the **positive-going** clock transition. The Q- output of U47A, is clocked by the leading edge of CLK+. This Q- output is used to enable gate U35A. This is the control gate for the working clock that represents an external positive-going clock edge. The Q- output of U47B is clocked by the trailing edge of CLK-. This Q- output is used to enable gate U35B. This is the control gate for the working clock that represents the external negative-going clock edge.

If signal QUAL is high during the positive-going clock edge, a low level is sent from the Q- output of the set latch(s) to the corresponding U35 gate. The level is held low for the duration of the clock period. These enabling levels establish that the corresponding clock edge meets the qualifier conditions and may be further selected by the Final Clock Selector.

The **Final Clock Selector** consists of U34 and U35, both 10211 dual 3-input, 3-output NOR gates. They are used as negative-input AND gates. By means of enabling signals, the Control Program uses these gates to select the data clock for the analyzer in accordance with keyboard entries. The following choices are available:

a. The choice of external or internal clock. The external clock is handled by gates U35A (for CLK-) and U35B (for CLK+). The internal clock is handled by gates U34A (for INT50) and U34B (for INT<50).

b. The choice of the positive going or negative-going edge if the clock is external. This choice is implemented by signals SWPE- (Software Positive Edge -) and SWNE- at gates U35A and U35B, respectively.

c. The choice of a 50 MHz or <50 Mhz clock frequency if the clock is

internal. The specified value of the <50 MHz clock has been preselected in the Clock Generator. This choice is implemented by software generated signals SW50- (Software 50 MHz -) and SW<50- at gates U34A and U34B, respectively.

Note that the analyzer always uses the positive-going edge of the working clock. A negative-going edge entered from the keyboard must be converted to an equivalent positive-going edge. This conversion is made in gate U35B. These 10211 AND gates require negative inputs. Gate U35B is enabled by SWNE- and fed by CLK+, that has a negative-going trailing edge. This produces a working clock with a positive-going **trailing** edge. Similarly, the U35A gate is enabled by SWPE- and fed by CLK- that has a negative-going leading edge. This produces a working clock with the desired positive-going **leading** edge.

Gates U34 and U35 implement clock shutoff at the end of post-trigger data collection. This is done using clock-inhibit signals CLKINHA+, CLKINHB+, and CLKINHC+ received from the Post-trigger Counter. Signals CLKINHA+ at U35A and CLKINHB+ at U35B are wired ORed with respective clock qualifier signals. These clock qualifier signals are received from the Qualifier Control latches. Signal CLKINHC+ is applied to both U34A and U34B. At the time of post-trigger terminal count, all three clock inhibit signals go high simultaneously. Thus the working clock is shut off no matter which of the four gates is active.

A wired OR consisting of one output from each of the four gates in the Final Clock Selector produces the final working clock. This signal is fed to the Clock Delay circuit. Within the logic of the Control Program, the four selecting signals are mutually exclusive. Therefore, only one of the four gates is enabled at any given time. If either SW50- or SW<50- is low, both SWPE- and SWNE- are held high. Or, if either SWPE- or SWNE- is low, both SW50- and SW<50- are held high.

An identical clock from a separate wired-OR set of the gate outputs is sent to pin S2-6 as signal CT (Clock, Timing). This signal is one of the two clocks sent to the Timing Memory Boards. Signal CLKTTL, to be discussed later, is the other. Signal CT is also the clock for the Waveform Control Board. CT is sent to the Clock Conditioning circuit shown on sheet 5 of the Waveform Control Board schematic.

The **Clock Delay** circuit consists of U23, a delay line; U53B, a section of a 10125 quad ECL-to-TTL translator; and U56D, a section of a 10101 quad OR/NOR gate. The 10101 is used as a buffer/driver. This circuitry produces the following two working clocks:

a. **CLKECL**, an ECL-level clock that is identical to the CT clock except that it is delayed by about 2.5 ns.

b. **CLKTTL**, a TTL-level clock that is identical to the CT clock except that it is delayed by about 15 ns.

CLKECL is used throughout the Timing Control Board. **CLKTTL** is used by the Timing Memory Boards. CLKTTL is sent to the Clock Generator shown on sheet 1 of the Timing Memory Board schematic.

The **A/B Multiplexer** circuitry is located on the Motherboard, but is described in this section. Please refer to the Motherboard schematic during the discussion.

The A/B Multiplexer consists of the following:

a. U1, U2, U6 and U7, all 10116 ECL triple differential amplifiers.

b. Section A of U8, a 10125 ECL-to-TTL translator.

c. Sections A and B of U10, a 7406 hex open-collector inverter.

d. U4, a multi-tapped 20 ns delay line.

e. Relays U5 and U9, and various resistors and diodes.

Differential amplifiers U1, U2 and U6, when

active, connect the Probe outputs of A Probe in parallel with that of B Probe. These amplifiers are made active when their Vcc Supply voltage is switched on by relay U5. This is caused in response to signal BPBSNS received from the Processor Board. Signal BPBSNS is enabled by the Control Program when the 2000-word data collection mode is selected from the keyboard. The enabling signal is bit 5 of port C in U40, the 8155.

In the 2000-word mode, amplifiers U1, U2 and U6 are active. Note that in this mode all data is collected from the A Probe. The B Probe should not be connected to the analyzer. An error message will appear on the CRT if the B Probe is connected.

A B-Clock Delay circuit is comprised of Amplifier U7C, the delay line U4, and translator U8. This is identical to the Clock Delay Circuit on the Timing Control Board. Using clock BCT as input, this B Clock Delay circuit generates clock BCLKTTL for the B Memory Board. CLKTTL from Timing Control is sent to the A Memory Board as ACLKTTL. Also, clock CT from Timing Control is sent to the A Memory Board as ACT.

In the 16-bit, 1000-word data collection mode, clock CT (the ECL-level clock) is sent via the contacts of relay U9 to become BCT. A relay is used to avoid the propagation delay of a solid state device. BCLKTTL is essentially identical to ACLKTTL. The A Memory and B Memory collect data in unison as 16-bit words. The A Memory receives data from the A Probe and the B Memory from the B Probe.

Signal 2KWRD causes relay U9 to select an inverted CT clock from U7A as clock BCT. This occurs in the 8-bit 2000-word data collection mode. Clocks BCT and BCLKTTL are 180° out of phase with clocks ACT and ACLKTTL. Together the A Memory and B Memory receive 200 interlaced 8-bit words from the A Probe. Because of the 2-phase clock, the collection interval is half the normal clock interval of CT. The 20 ns CT clock, for example, produces a 10 ns collection interval. The Control Program takes this into account when responding to keyboard entry of the clock interval for the 2000-word mode.

9.2.4 TRIGGER CONTROL

Trigger Control (sheet 3) is comprised of the Trigger Linker and the Trigger Filter. This circuitry allows the Control Program to set up specified trigger linkages with other NPC 764 or 600 Series analyzers, or external trigger signals. It also implements the keyboard-selected degree of trigger filtering. Trigger filtering provides that the trigger signal be true longer than a specified number of clock periods to be considered valid.

The Trigger Linker consists of the following components: U56A,B,C, sections of a 10101 quad OR/NOR gate, used as buffer-inverters; U55C,D, sections of a 10124 quad TTL-to-ECL translator; and U42B, U45 and U46, all 10117 dual 2-wide OR-NAND gates.

The upper OR gates in U45A,B and U46A are not used. The software-generated enabling levels applied to these OR gates are SWTT0-, SWSTA0-, and SWSTB0-. These signals are always held high so the outputs of the three NAND gates are controlled by the lower OR gates.

U56A,B and C are used to provide both true and inverted signals to the OR-NAND gates U45A,B and U46A. However, as noted above, only the inverted outputs are used. U55C,D convert TTL level signals to ECL level. The ECL signals are sent to gates U46B and U42B and to Sheet 2 for gates in the ARM Linker.

The outputs of the five 2-wide OR-NAND gates are connected in a wired AND. All outputs must be low to produce the active-low trigger signal. This signal is sent to the Trigger Filter. The enabling signal SWTT1- is always held low by the Control Program. This insures that the Timing trigger TT- will control the output of the U45A.

Signals STA- and STB- are not used in the NPC 764. The Control Program holds signals SWSTA1- and SWSTB1- high. Thus the outputs of U45B and U46A are held low. These

signals then do not interfere with the wired AND of the remaining three OR-NAND gates.

Gates U46B and U42B implement the trigger linkage function. The keyboard input may specify a trigger link to the External signal. This causes the Control Program to bring SWEXT- low so that EXT controls the output of U46B. Otherwise, SWEXT- is held high and EXT has no effect. Similarly, if a trigger link to another analyzer has been specified, SWFS- is brought low. This brings signal FS low effecting the output of U46B. Signal FS is produced from LINK by circuitry on the Motherboard. If a link to the Waveform trigger has been specified, SWWT- is brought low. This allows signal TRIG+ to control the output of U42B.

All enabled linkages must be true simultaneously with TT- to produce a true (low) trigger output. This is caused because of the wired AND connection of the OR-NAND gate outputs. The true (low) trigger output signal is sent to U41A-4 and U41B-6 as TRIG-.

The **Trigger Filter** consists of U41A,B,C, sections of a 10102 quad NOR gate and U52, a 10137 decade counter. Section A of the 10102 is used as a negative-input AND gate, sections B and C are used as inverters.

U41B inverts TRIG- and feeds it to the U52 decade counter at pin 9. At set-up time, the S1 and S2 inputs to the decade counter are both low. This causes the counter to be in the load mode. The Control Program presets the counter to the keyboard-specified filter value. Signals TF0-TF3 (Trigger Filter 0-3) received from the Processor Interface, are used for this function. This value may range from the default value of 0 to a maximum of 9.

When the trigger signal goes true, S1 goes high, putting the counter in the count down mode. Clocked by CLKECL from Clock Control, the counter counts down from the preset filter value. The counter outputs are connected in wired AND. When the count reaches 0, the pin 5 input to AND gate U41A is brought low. The 0-count low level is inverted by U41C. This signal is sent back to the counter Carry-In input, U52-10, to stop the count. If TRIG- at U41A-4 is still true at 0 count, signal TRIG+ goes true at the output of U41A. TRIG+ is sent to the Sequencer Latch (sheet 5).

9.2.5 ARM CONTROL

Arm Control (sheet 2) is comprised of the Arm Linker and the Arm Filter. This circuitry allows the Control Program to set up keyboard-specified linkages with External, other NPC 764 analyzers or Waveform arm signals. The circuitry also implements the keyboard-selected degree of arm filtering. Arm filtering provides that the arm signal be true for a specified number of clock periods to be considered valid.

The **Arm Linker** consists of the following components: U54B,C,D sections of a 10101 quad OR/NOR gate, used as buffer-inverters; and U42A, U43 and U44, all 10117 dual 2-wide OR-NAND gates. The operation of this circuitry is analogous in every respect to the operation of the Trigger Linker. Note that ECL-level EXT and FS signals are taken from the U55 translators in the Trigger Linker.

The **Arm Filter** consists of U40A,B,C, sections of a 10102 quad NOR gate and U51, a 10137 decade counter. Section A of the 10102 is used as a negative-input AND gate, sections B and C are used as inverters. The operation of this circuitry is analogous in every respect to the operation of the Trigger Filter.

9.2.6 SEQUENCER

The Sequencer (sheet 5) is comprised of Load Control, the Sequencer Latch, the Sequencer RAM, Sequencer Output, and LINK Control. This circuitry allows the Control Program to set up sequences in accordance with the keyboard-entered instructions. The sequence operations pertain to the Delay Counter and Post-trigger Counter in relation to the arm and trigger events.

Load Control consists of U39A,B, sections of a quad TTL-to-ECL translator; and U20C,D,

U38, quad AND gates. Circuits U39A and B provide level translation for the RESET- signal. RESET- is sent to the Sequencer Latch. Level translation is also provided for WRRAM- (Write RAM) write-enable signal sent to the Sequencer RAM. Both of these signals are received from the Address Decoder in the Processor Interface. Gates U20C,D and U38 are enabled by the LDSEQ+ (Load Sequencer +) signal. This signal is received from the Control Shift Register in the Processor Interface. When enabled, these gates feed setup address signals, PTCTR03 (Post-trigger Counter 03) through PTCTR08, to the Sequencer RAM.

The **Sequencer Latch** consists of U12, a 10186 hex D flip-flop. Inputs to the latch are the ARM+ and TRIG+ signals from Arm Control and Trigger Control, the DLYTC- (Delay Terminal Count -) signal from the Delay Counter, and the three state output lines from the Sequencer RAM. The six outputs of the latch are sent to the six address inputs of the Sequencer RAM. Output Q0 also feeds the ARML+ (Arm Latch +) signal to the Count Mode Selector (sheet 7). The outputs Q3,4 and 5 also feed signals S0 (Sequence 0), S1, and S2 to Sequencer Output.

The **Sequencer RAM** consists of U13, U25 and U37, all 10148 64-word x 1-bit static RAMs. The RAM data inputs are sent from the Processor Interface with signals PTCTR00 (Post-trigger Counter 00), PTCTR01 and PTCTR02. The RAM address inputs are wired OR connected. The input signals are sent from Sequencer Latch and Load Control gates.

At set-up time, the processor brings the RAM WE- inputs low with signal WRRAM-. The processor resets the Sequencer Latch so that all latch outputs are low. The RAM address inputs are therefore under processor control through the Load Control gates. This allows the Control Program to load the RAMs with sequencing data in accordance with the keyboard-entered delay mode information. Sequencer Latch output signals S0, S1 and S2 are all low. These signals are applied to the decoder, producing output signals, DLYCNT+/LD- AND PTCNT+/LD- that are in the load state (low). This allows the Control Program to preset the Delay Counter and Post-trigger Counter to appropriate values.

At run time, the Control Program brings the Load Control gate outputs low with a low LDSEQ+. This leaves the RAM address inputs under control of the Sequencer Latch. The Sequencer Latch is clocked by CLKECL. Starting with address 00, the Sequencer Latch steps through the control sequence stored in the RAM. The high-order three bits of each successive RAM address are determined by the three RAM outputs from the previous address. The low-order three address bits change when an arm-word or trigger-word match occurs. The bits also change when the delay terminal count is reached. At the proper point in the delay control sequence, S0, S1 and S2 decode to bring DLYCNT+/LD- high. This starts the delay count. Similarly, at the proper time, PTCNT+/LD- is brought high, thus starting the post-trigger count.

Sequencer Output consists of U36, a 10125 quad ECL-to-TTL translator; and U24, a 10162 1-of-8 decoder. Translators U36B,C and D translate the Sequencer Latch outputs S0, S1 and S2 to TTL level. The TTL level signals are sent to the Status Port in the Processor Interface. Sequencer Latch outputs S0, S1, and S2 also are sent to the three decoder inputs. The decoder produces two output signals, DLYCNT+/LD- (Delay Count + / Load -) and PTCNT+/LD- (Post-trigger Count + / Load -). These signals are sent to the Delay Counter and Post-trigger Counter, respectively. Signal PTCNT+/LD- is also sent through translator U36A as signal FT (Function of Timing). This signal is sent to the Status Port in the Processor Interface. Signal FT is also sent, via connector pin S2E-11, to LINK Control on the Motherboard for possible linking to another NPC 764. Both signals PTCNT+/LD- and FT go high when the NPC 764 arm and trigger conditions have been met.

The **LINK Control** circuitry is located on the Motherboard but will be discussed here (see Motherboard schematic). The circuit con-

sists of sections B,C, and E, sections of U12, a 7406 hex open-collector inverter.

When no link is set in the timing menu, the NPC 764, as timing analyzer, is specified as the master in a linking. Then the LINK Control circuit allows the Control Program to enable signal FT as the outgoing LINK signal.

When the link is set in the timing menu, the NPC 764, as timing analyzer, is the slave in the linking. Then the LINK Control circuit allows the Control Program to enable an incoming LINK signal as signal FS. Signal FS is sent to the Arm Linker and Trigger Linker circuits on the Timing Control Board.

9.2.7 POST-TRIGGER AND DELAY COUNTERS

The Post-trigger and Delay Counters are comprised of the Count Mode Selector, the Delay Counter, and the Post-trigger Counter. These circuits allow the Control Program to implement the selected delay function and specified pre-trigger and post-trigger division of collected data.

The **Count Mode Selector** consists of the following components: U20A,B, sections of a 10104 quad AND gate, and U41D, a section of a 10102 quad NOR gate (used as an inverter). The wired OR outputs of U20A and B produce signal DLYCLK (Delay Clock). This signal occurs either at every ARML+ occurrence or at every CLKECL clock. The controlling signal depends on the polarity of software-generated signal DLYARM+/CLK-. This signal is dependent on a keyboard entry. DLYCLK is used to clock the Delay Counter.

The Delay Counter consists of U17, U18, U19 and U21, all 10137 decade counters; and U22A,B,D, sections of a 10103 quad OR gate. The 10103 gates are used as negative-logic AND gates. The counters are operated in the countdown mode. Using the U22 AND gates, the four counters are connected in cascade. A terminal count of 0000 produces a low signal, DLYTC- (Delay Terminal Count -). This signal is wired AND at the junction of U21 and U22D outputs. The maximum preset count value is 9999.

The **Post-trigger Counter** consists of the following components: U14, U15 and U16, all 10137 decade counters, U22C, a section of a 10103 quad OR gate (used as a negative-logic AND gate); U11, a 10211 dual 3-input, 3-output NOR gate; and U39C, a section of a 10124 quad TTL-to-ECL translator. The counters are operated in the countdown mode. Using AND gate U22C, these counters, on a terminal count of 000, will produce low levels at pins 5, 7 of AND gate U11A. The maximum preset count value is 999.

At set-up time, the counters are placed in the load mode by a low level on signal PTCNT+/LD-. This signal is sent from the Sequencer to the counter S1 mode-select inputs. This allows the Control Program to load the counters with the post-trigger count. To accomplish this, signals PTCTR00 (Post-trigger Counter 00) through PTCTR11 are used. The Post-trigger counter signals are received from the Control Shift Register in the Processor Interface. The Control Program derives the post-trigger count from 1000 minus the specified pre-trigger count.

At run time, if the specified arm, delay and trigger conditions are met, the Sequencer brings PTCNT+/LD- high. This puts the Post-trigger Counter in the countdown mode. Then the preset count is decremented by CLKECL, received from Clock Control. A terminal count of 000 produces high outputs sent from AND gate U11A if signal, ENCLKINH- (Enable Clock Inhibit -), is low. Signal ENCLKINH- is received from the Control Shift Register in the Processor Interface. It is normally brought low by the Control Program at run time. The three outputs of U11A are connected in wired OR with those of U11B. This produces three identical signals, CLKINHA+ (Clock Inhibit A+), CLKINHB+, and CLKINHC+. All are produced either by the post-trigger terminal count at U11A or by SWCLKINH- (Software Clock Inhibit -) at U11B. Signal SWCLKINH- is received from the Master Control Register in the Processor Interface. It is used by the Control Program during set-up.

When the post-trigger terminal count has been reached, the working clocks are turned off. This is done by the three clock inhibit signals that are sent to Clock Control and turn off CT, CLKECL, and CLKTTL. Three identical clock inhibit signals are needed because two are separately wire ORed with the two Qualifier Control latch outputs. These are shown on sheet 8.

9.3 SCHEMATIC, BOARD LAYOUT AND PARTS LIST

The schematic diagram, board layout, and parts list for the Timing Control Board are contained on the following pages.

PARENT ITEM 143-0071-0090 | CROSS REF ITEM | DESCRIPTION TIMING CONTROL PC ASSY-OUTSIDE | ENGR DRAW ECO 427 REV F | BATCH QTY 1 | EFFEC 12/08/82 | ITEM TYPE 1 | UNIT MEAS EA | LOW LEVEL 03 | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0045	180 OHM 1/4W 5% CF RES R3		1.000	EA	4C					
	07	110-0005-0047	220 OHM 1/4W 5% CF RES R13 R14		2.000	EA	4C					
	05	110-0005-0049	270 OHM 1/4W 5% CF RES R7		1.000	EA	4C					
	06	110-0005-0063	1K OHM 1/4W 5% CF RES R10 R11 R12 R4 R5 R9		6.000	EA	4C					
	06	110-0005-0070	2K OHM 1/4W 5% CF RES R2		1.000	EA	4C				3/06/80	
	06	110-0005-0075	3.3K OHM 1/4W 5% CF RES R3 R5		2.000	EA	4C					
	05	110-0306-0001	RN 100 OHM X7 8 PIN SIP RP10		1.000	EA	4C					
	05	110-0307-0001	RN 150 OHM X7 8 PIN SIP RP9		1.000	EA	4C					
	05	110-0308-0001	RN 470 OHM X7 8 PIN SIP RP1 RP11 RP12 RP2 RP3 RP4 RP5 RP6 RP7 RP8		10.000	EA	4C					
	06	111-0004-0072	.1 UF 25V CD CAP C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C4 C5 C6 C7 C8 C9		25.000	EA	4C					
	05	111-0012-0003	2.2 PF 1KV CD CAP C1		1.000	EA	4C					
	06	111-0012-0030	100 PF 1KV CD CAP C29		1.000	EA	4C					
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C2 C3		2.000	EA	4C				8/21/80	
	06	112-0101-0001	TRANSISTOR 2N3905 Q1 Q2		2.000	EA	4C					
	04	112-0305-0001	CRYSTAL 100 MHZ CRYSTEK Y1		1.000	EA	4C				10/21/80	
	04	113-0046-0003	DELAY LINE,LC0202100R,PE21182 U23		1.000	EA	4C				5/05/80	
	06	115-0003-0001	SOCKET 14PIN U1 U4 U5 U6 U7 U8		6.000	EA	4C					
	06	115-0005-0001	SOCKET 16PIN U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U2 U20 U21 U22 U24 U25 U26 U27 U28 U29 U3 U30 U31 U32 U33 U34 U35 U36 U37 U38 U39 U40 U41 U42 U43 U44 U45 U46 U47 U50 U51 U52 U53 U54 U55 U56 U9		47.000	EA	4C					

PARENT ITEM	CROSS REF ITEM	DESCRIPTION TIMING CONTROL PC ASSY-OUTSIDE	BATCH QTY 1	ITEM TYPE 1	LOW LEVEL 03
143-0071-0090		ENGR DRAW ECO 427 REV E	EFFEC 12/08/82	UNIT MEAS EA	PLANNER

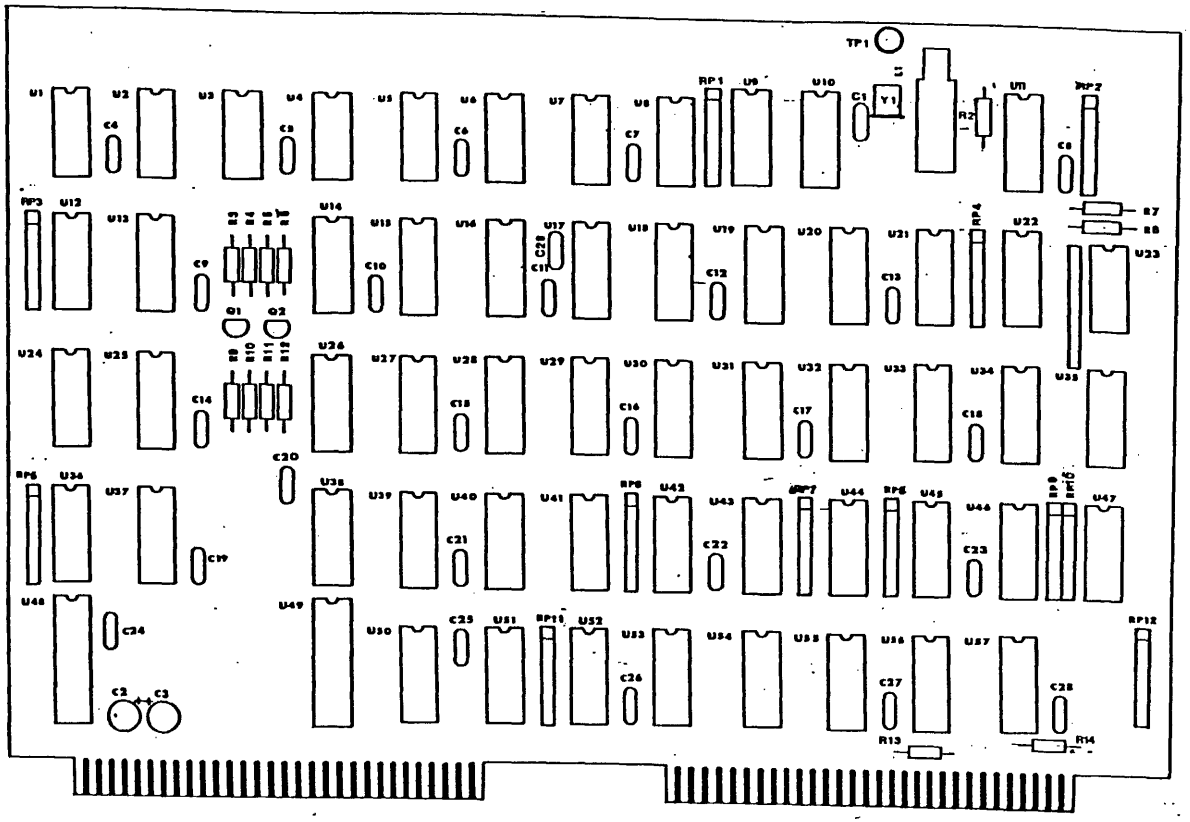
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	115-0009-0001	SOCKET 22PIN U49 U49		2.000	EA	4C					
	04	121-0013-0001	UNICOIL T7-116 4 1/2 TURNS L1		1.000	EA	4C					
	04	126-0071-0001	TIMING CONTROL PC FAB	ECO 227 REV F	1.000	EA	4C					

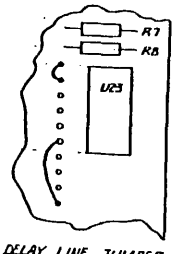
PARENT ITEM	CROSS REF ITEM	DESCRIPTION TIMING CONTROL PC ASSY	BATCH QTY 1	ITEM TYPE 1	LOW LEVEL 02
143-0071-0001		ENGR DRAW ECO 427 REV E	EFFEC 12/08/82	UNIT MEAS EA	PLANNER

REF NBR	LL CO	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	117-0030-0001	TERMINAL 120-1032-04 CAMBION TPL		1.000	EA	4C				10/22/81	
	03	143-0071-0090	TIMING CONTROL PC ASSY-OUTSIDE	ECO 427 REV E	1.000	EA	1C					

PARENT ITEM 143-0071-0001 | CROSS REF ITEM | DESCRIPTION TIMING CONTROL PC ASSY ENGR DRAW ECO 427 REV F | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	03	113-0003-0074	I.C. 74LS74 U1		1.000	EA	4C					
	03	113-0003-0090	I.C. 74LS90 U4 U5 U6 U7 U8		5.000	EA	4C					
	06	113-0003-0138	I.C. 74LS138 U50		1.000	EA	4C					
	04	113-0003-0151	I.C. 74LS151 U2 U3		2.000	EA	4C					
	05	113-0003-0373	I.C. 74LS373 U48		1.000	EA	4C					
	05	113-0003-0374	I.C. 74LS374 U49		1.000	EA	4C					
	04	113-0042-0001	I.C. SCL4015AE U26 U27 U28 U29 U30 U31 U32 U33		8.000	EA	4C					
	03	113-0200-0101	I.C. MC10101 U54 U56		2.000	EA	4C					
	04	113-0200-0102	I.C. MC10102 U10 U40 U41		3.000	EA	4C					
	03	113-0200-0103	I.C. MC10103 U22		1.000	EA	4C					
	03	113-0200-0104	I.C. MC10104 U20 U38		2.000	EA	4C					
	04	113-0200-0117	I.C. MC10117 U42 U43 U44 U45 U46		5.000	EA	4C					
	03	113-0200-0124	I.C. MC10124 U39 U55		2.000	EA	4C					
	05	113-0200-0125	I.C. MC10125 U36 U53		2.000	EA	4C					
	04	113-0200-0130	I.C. MC10130 U47		1.000	EA	4C					
	03	113-0200-0137	I.C. MC10137 U14 U15 U16 U17 U18 U19 U21 U51 U52		9.000	EA	4C					
	03	113-0200-0138	I.C. MC10138 U9		1.000	EA	4C					
	03	113-0200-0148	I.C. MC10148 U13 U25 U37		3.000	EA	4C					
	03	113-0200-0162	I.C. MC10162 U24		1.000	EA	4C					
	03	113-0200-0186	I.C. MC10186 U12		1.000	EA	4C					
	03	113-0200-0211	I.C. MC10211 U31 U34 U35		3.000	EA	4C					





DELAY LINE JUMPER SETTINGS

DETAIL A
SCALE - 2/1

Timing Control

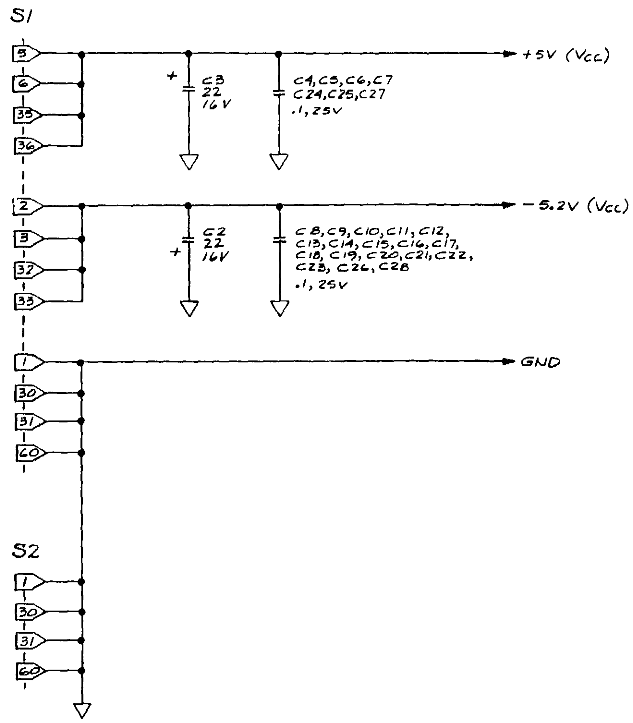
NICOLET PARATRONICS

126-0071-0201 Rev. G

1. ADD DELAY LINE JUMPERS IN ASSEMBLY AS SHOWN IN DETAIL "A". DELAY LINE JUMPERS MAY REQUIRE ADJUSTMENT IN TEST.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	DESCRIPTION	DATE	APPROVED
C	REV PER ECC 106	3/4/80	WO
D	REV PER ECO's 130,133A		
E	REV PER ECO 185	4/16/80	
F	REV PER ECO 227	11/6/80	KRF
G	REV PER ECO 420		MCP
H	REV PER ECO 558	3 31 82	
J	Rev. Per Eco 773	11-11-82	



POWER DISTRIBUTION

"U" NUMBER'S	DEVICE	+5V (VCC)	−5.2V (VCC)	GND	PACKAGE
54,56,	10101	—	8	1, 16	16 DIP
42,43,44,45,46	10117	—	8	1, 16	↑
40, 41, 10	10102	—	8	1, 16	
51,52,16,15,14,21,19,18,17	10137	—	8	1, 16	
55, 39	10124	9	8	16	↓
50	74LS138	16	—	8	16 DIP
49	74LS374	20	—	10	20 DIP
53,36	10125	9	8	16	16 DIP
48	74LS373	20	—	10	20 DIP
26,27,28,30,31,32,33,29	CD4015	—	8	16	16 DIP
20, 38	10104	—	8	1,16	↑
12	10186		8	16	
37,25,13	10148		8	1,16	
24	10162		8	1,16	↓
2, 3	74LS151	16	—	8	16 DIP
4,5,6,7,8	74LS90	5	—	10	14 DIP
1	74LS74	14	—	7	14 DIP
9	10138	—	8	1,16	16 DIP
22	10103	—	8	1,16	↑
11, 35, 34	10211	—	8	1,15,16	↓
47	10130	—	8	1,16	16 DIP

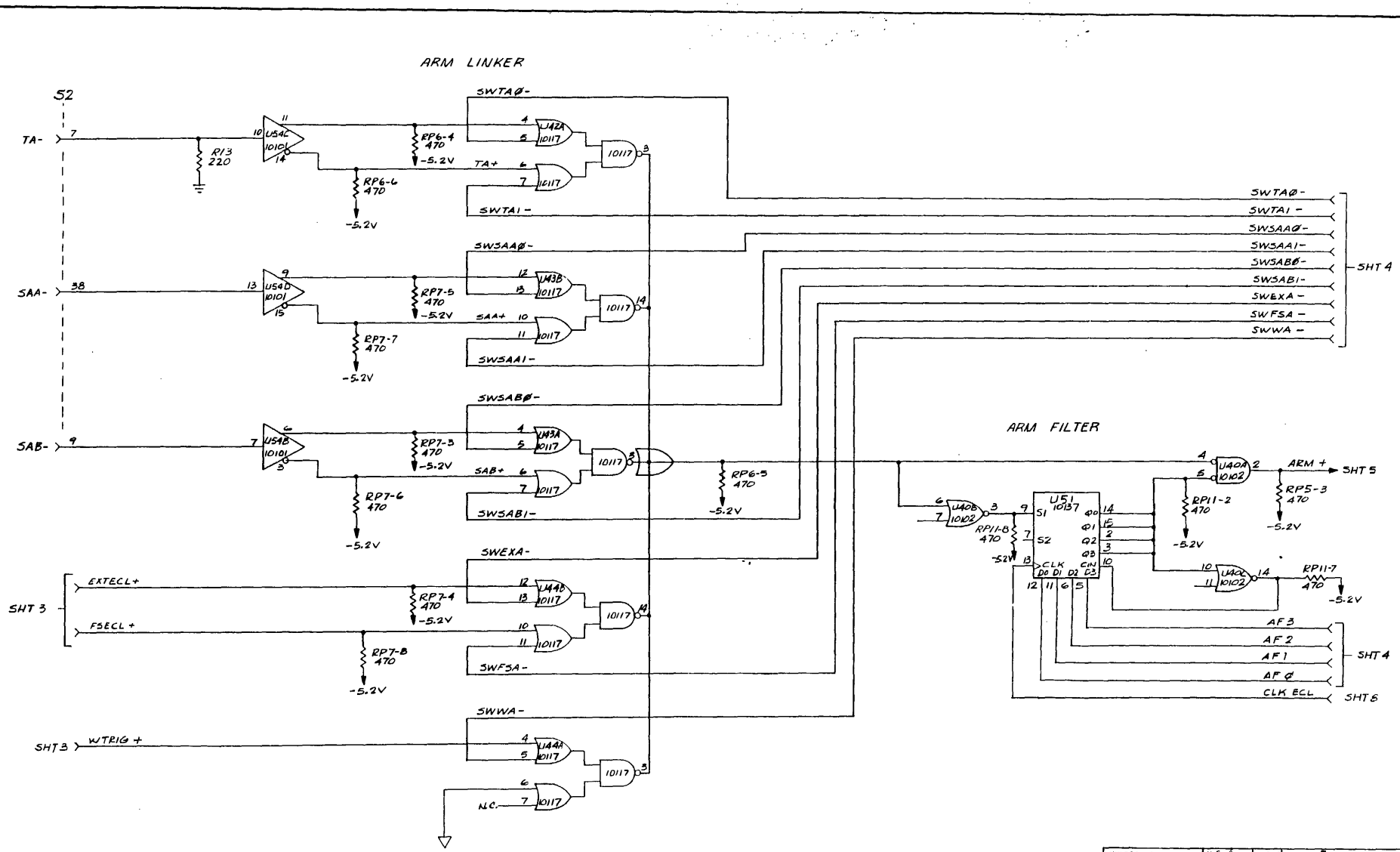
3. THIS SCHEMATIC TO BE USED WITH REV. "F" PCB. FABRICATION
2. ALL CAPACITORS ARE IN MICROFARADS, DISC CERAMIC
1. ALL DISCRETE RESISTORS ARE 1/4W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED:

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

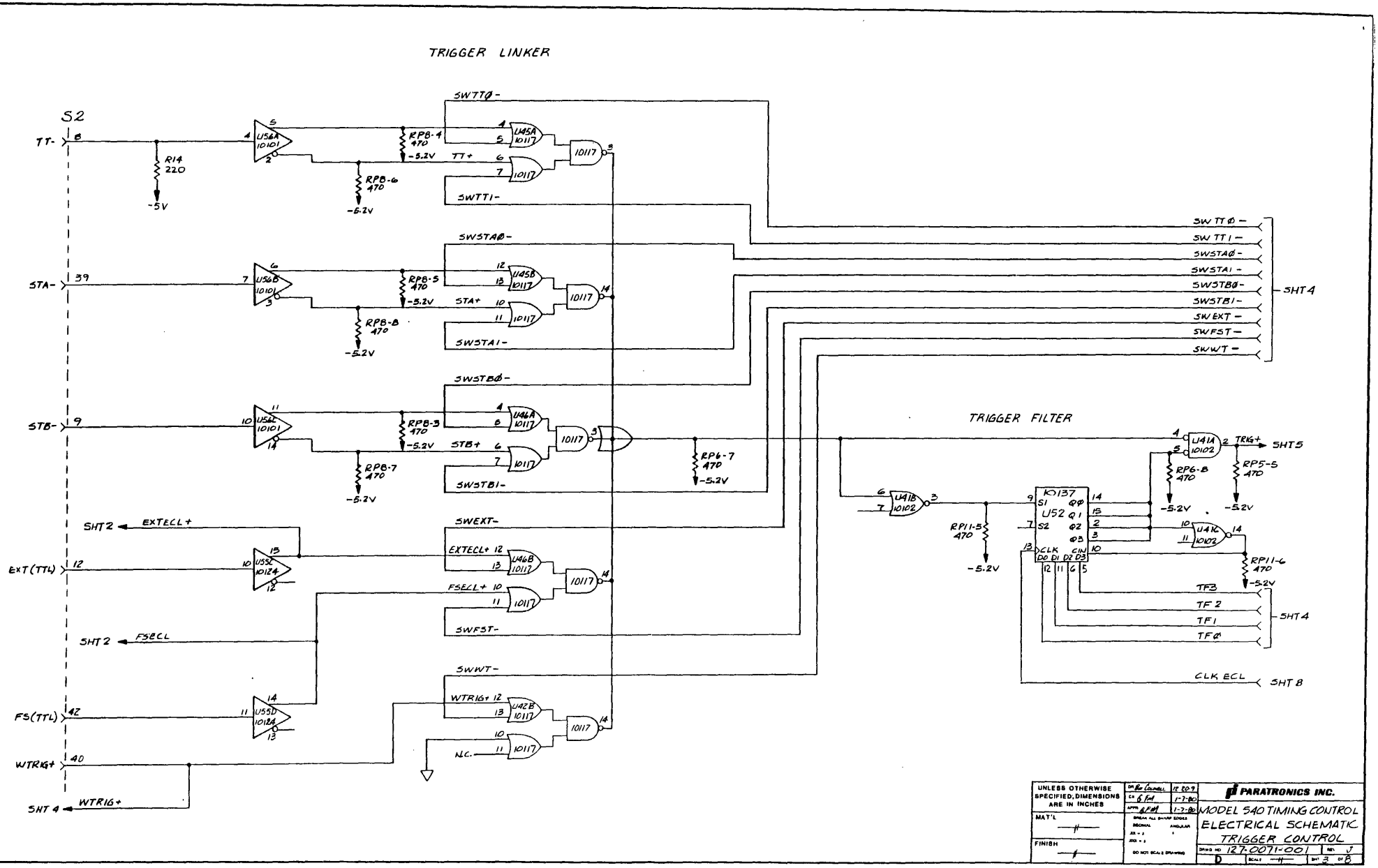
PARATRONICS INC.

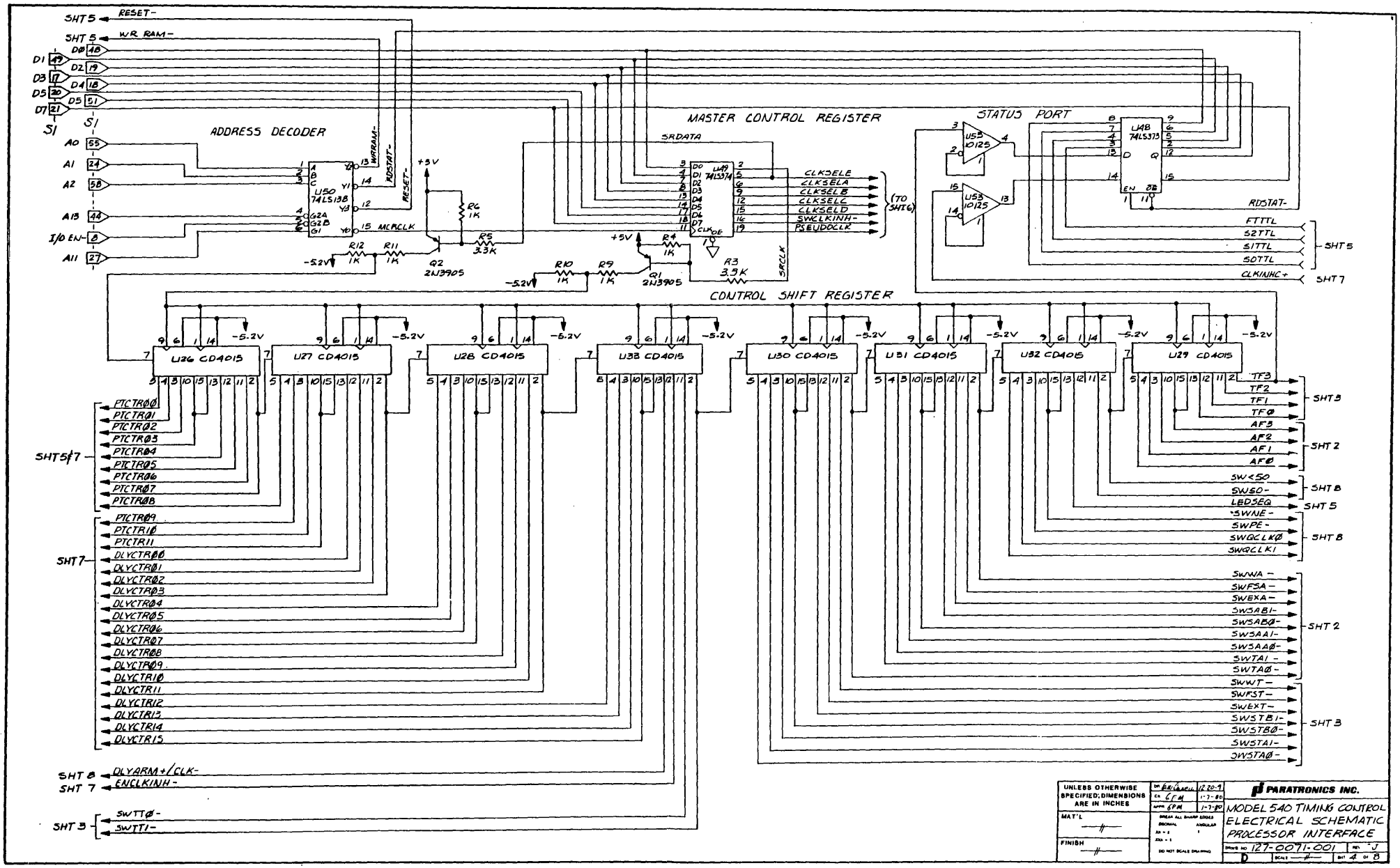
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
PWR & GND DISTRIBUTION

DWG NO 127-0071-001 REV J
D SHT 1 OF 8

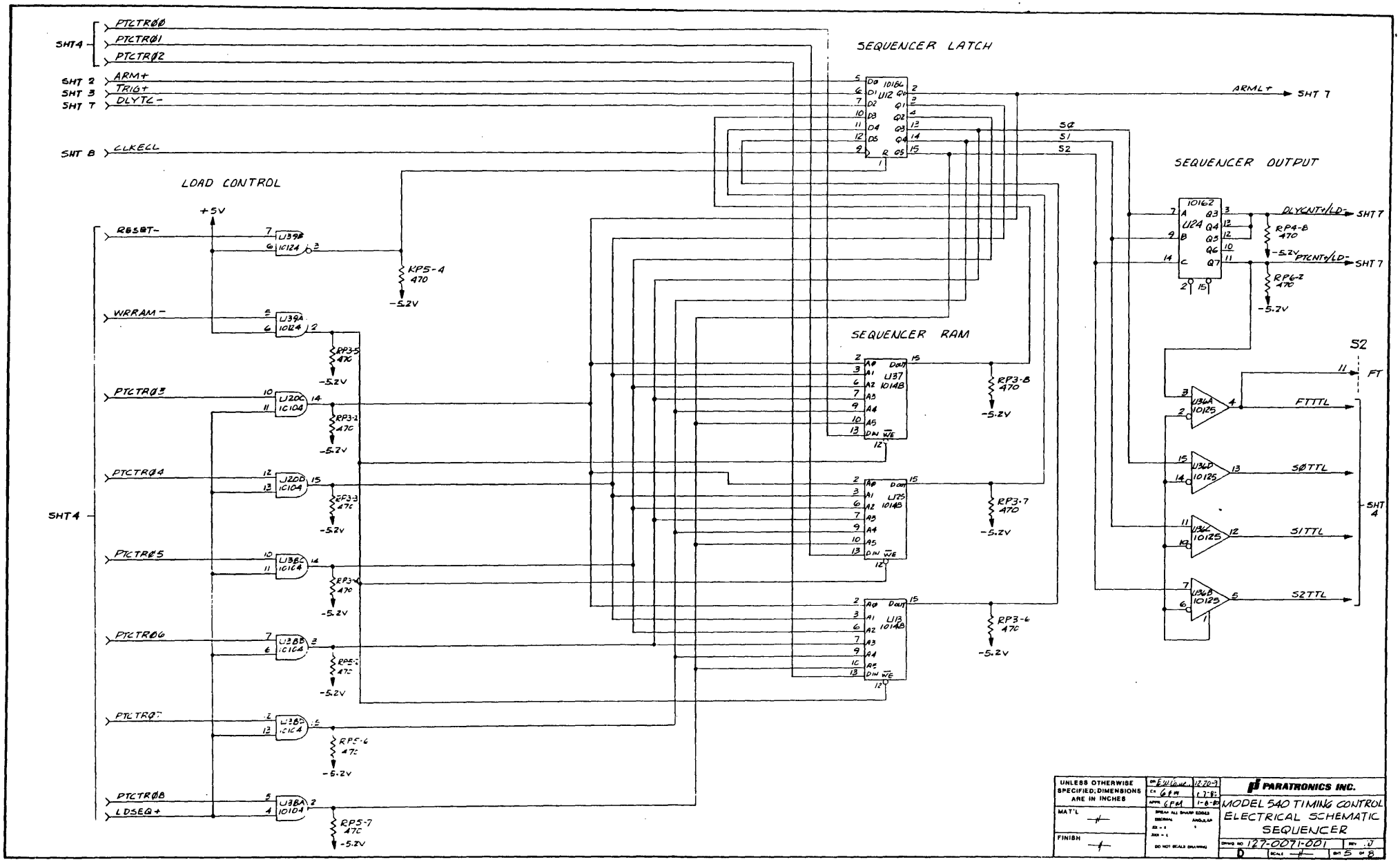


UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR E.W. Daniel	12-20-9	PARATRONICS INC.
	CK [illegible]	1-21-9	MODEL 540 TIMING CONTROL
MAT'L	APPR [illegible]	1/21/89	ELECTRICAL SCHEMATIC
FINISH	BREAK ALL SHARP EDGES		ARM CONTROL
	DO NOT SCALE DRAWING		DWG NO 127-0071-001 REV J
			D SCALE SHT 2 OF 8

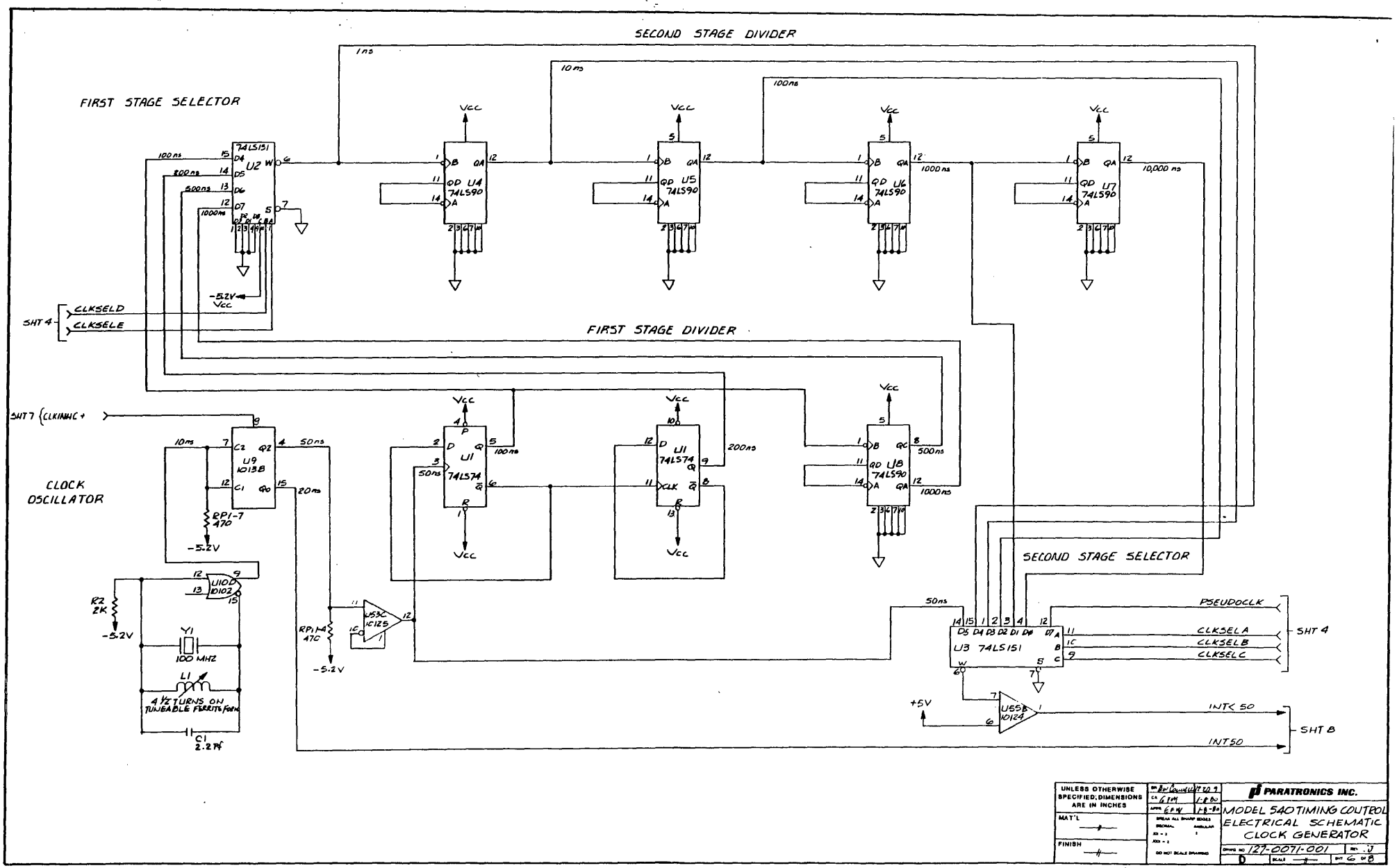

TRIGGER LINKER
S2
TT-
STA-
STB-
EXT(TTL)
FS(TTL)
WTRIG+
SHT 4 WTRIG+
SHT 2 EXTECL+
SHT 2 FSECL
R14 220
-5V
RPB-1 470
RPB-6 470
RPB-5 470
RPB-8 470
RPB-3 470
RPB-7 470
-5.2V
U56A 10101
U56B 10101
U56C 10101
U55C 10124
U55D 10124
U45A 10117
U45B 10117
U46A 10117
U46B 10117
U42B 10117
10117
TT+
STA+
STB+
EXTECL+
FSECL+
WTRIG+
N.C.
SWTTØ-
SWTT1-
SWSTAØ-
SWSTA1-
SWSTBØ-
SWSTB1-
SWEXT-
SWFST-
SWWT-
SW TTØ-
SW TT1-
SWSTAØ-
SWSTA1-
SWSTBØ-
SWSTB1-
SW EXT-
SWFST-
SWWT-
SHT 4
RP6-7 470
TRIGGER FILTER
U41B 10102
RPI1-5 470
10137 U52
S1 S2 CLK CIN
Q0 Q1 Q2 Q3
D0 D1 D2 D3
U41A 10102
U41C 10102
RP6-8 470
RP5-5 470
RPI1-6 470
TRIG+
SHT5
TF3
TF2
TF1
TFØ
SHT 4
CLK ECL
SHT 8
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DR Ric Connell 12 DEC 79
CK G Fink 1-7-80
APPR A Fink 1-7-80
DO NOT SCALE DRAWING
PARATRONICS INC.
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
TRIGGER CONTROL
DRWG NO 127-00071-001
REV J
D
SHT 3 OF 8



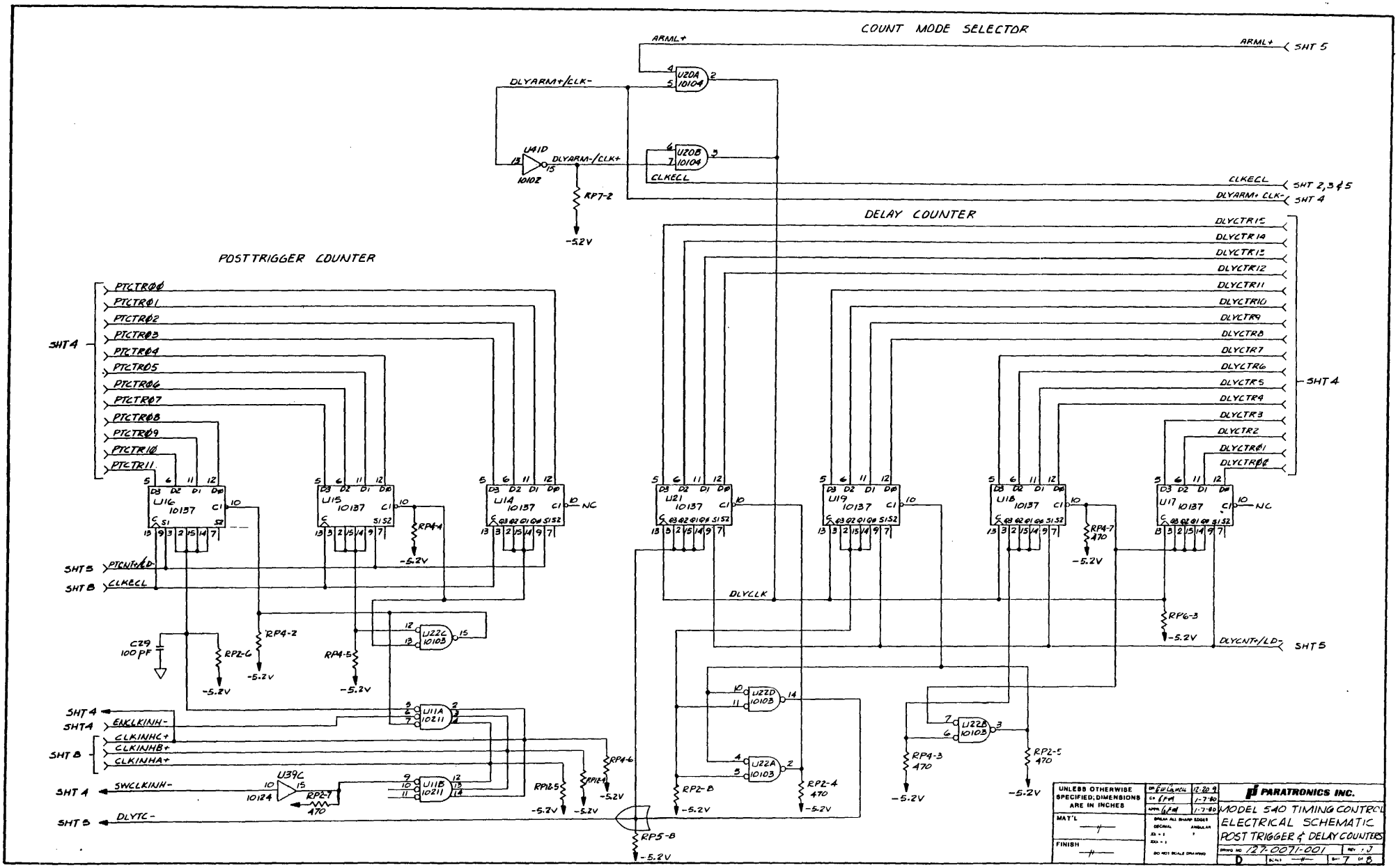
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	PARATRONICS INC.	
MAT'L	MODEL 540 TIMING CONTROL ELECTRICAL SCHEMATIC PROCESSOR INTERFACE	
FINISH	DRWG NO 127-0071-001 REV J	
DO NOT SCALE DRAWING	SCALE — SHT 4 OF 8	

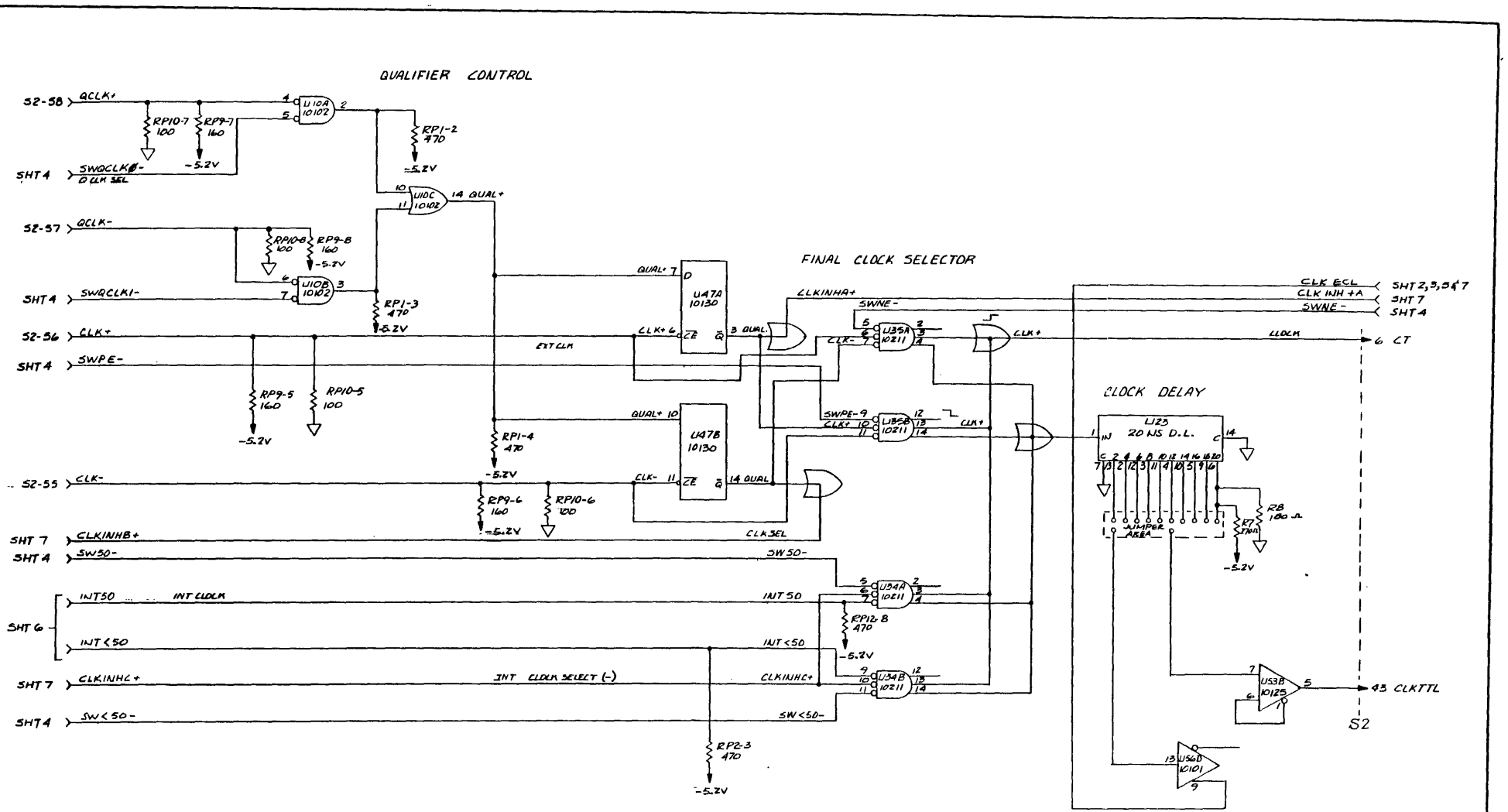


UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES	DR E.W.Lowe	12-20-7	PARATRONICS INC.
	CH G.P.M.	1-7-8	MODEL 540 TIMING CONTROL
MAT'L	APPR G.P.M.	1-16-8	ELECTRICAL SCHEMATIC
FINISH	BREAK ALL SHARP EDGES		SEQUENCER
	DO NOT SCALE DRAWING		DRWG NO 127-0071-001 REV J
			D SCALE SHT 5 OF 8



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR R.W. Carroll 1-7-80	PARATRONICS INC.
MAT'L	CH G.H.M. 1-8-80	MODEL 540 TIMING CONTROL
FINISH	APPR G.H.M. 1-8-80	ELECTRICAL SCHEMATIC
	BREAK ALL SHARP EDGES	CLOCK GENERATOR
	DO NOT SCALE DRAWING	DRAWING NO 127-0071-001 REV J
		D SCALE — SHT 6 OF 8


COUNT MODE SELECTOR
POSTTRIGGER COUNTER
DELAY COUNTER
ARML+
DLYARM+/CLK-
DLYARM-/CLK+
CLKECL
RP7-2
-5.2V
U20A 10104
U20B 10104
U41D
10102
PTCTR00
PTCTR01
PTCTR02
PTCTR03
PTCTR04
PTCTR05
PTCTR06
PTCTR07
PTCTR08
PTCTR09
PTCTR10
PTCTR11
U16 10137
U15 10137
U14 10137
U21 10137
U19 10137
U18 10137
U17 10137
RP4-4
RP4-7 470
RP6-3
DLYCLK
DLYCNT+/LD-
DLYCTR15
DLYCTR14
DLYCTR13
DLYCTR12
DLYCTR11
DLYCTR10
DLYCTR9
DLYCTR8
DLYCTR7
DLYCTR6
DLYCTR5
DLYCTR4
DLYCTR3
DLYCTR2
DLYCTR01
DLYCTR00
C29 100 PF
RP2-6
RP4-2
RP4-5
U22C 10103
U11A 10211
U22D 10103
U22A 10103
U22B 10103
RP4-3 470
RP2-5 470
RP2-8
RP2-4 470
RP5-8
U39C 10124
U11B 10211
RP2-7 470
RP4-6
RP2-3
RP2-2
ENCLKINH-
CLKINHC+
CLKINHB+
CLKINHA+
SWCLKINH-
DLYTC-
SHT 4
SHT 5
SHT 8
SHT 2,3 & 5
DLYARM+ CLK-
PTCNT+/LD-
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
PARATRONICS INC.
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
POST TRIGGER & DELAY COUNTERS
127-0071-001
REV. J
SIZE D
SHT 7 OF 8



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	DR B.W. Gramling 12-26-9	PARATRONICS INC.
MAT'L —	CK [illegible]	MODEL 540 TIMING CONTROL
FINISH —	APPR	ELECTRICAL SCHEMATIC
DO NOT SCALE DRAWING		CLOCK CONTROL
		DRWG NO 127-0071-001 REV J
		D SCALE — SHT 8 OF 8

TIMING MEMORY BOARD

SECTION 10: TIMING MEMORY BOARD

SECTION X
TIMING MEMORY BOARD

10.1 INTRODUCTION

There are two identical Timing Memory Boards in the NPC 764. These Boards store high-speed incoming data in a multiplexed static RAM as directed by the Timing Control Board. Also, using logic-gate comparators, they detect matches of incoming data with keyboard-specified arm and trigger words. When specified from the keyboard, they detect and pulse-stretch data glitches for storage and display.

10.2 FUNCTIONAL DESCRIPTION

A block diagram of the Timing Memory Board is shown in Figure 10-1. Also refer to the schematic diagram, board layout and parts list included at the end of this section. Tables of connector pins versus signal names for all motherboard connectors are provided in SIGNAL AND INTERCONNECTION TABLES. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for acro-

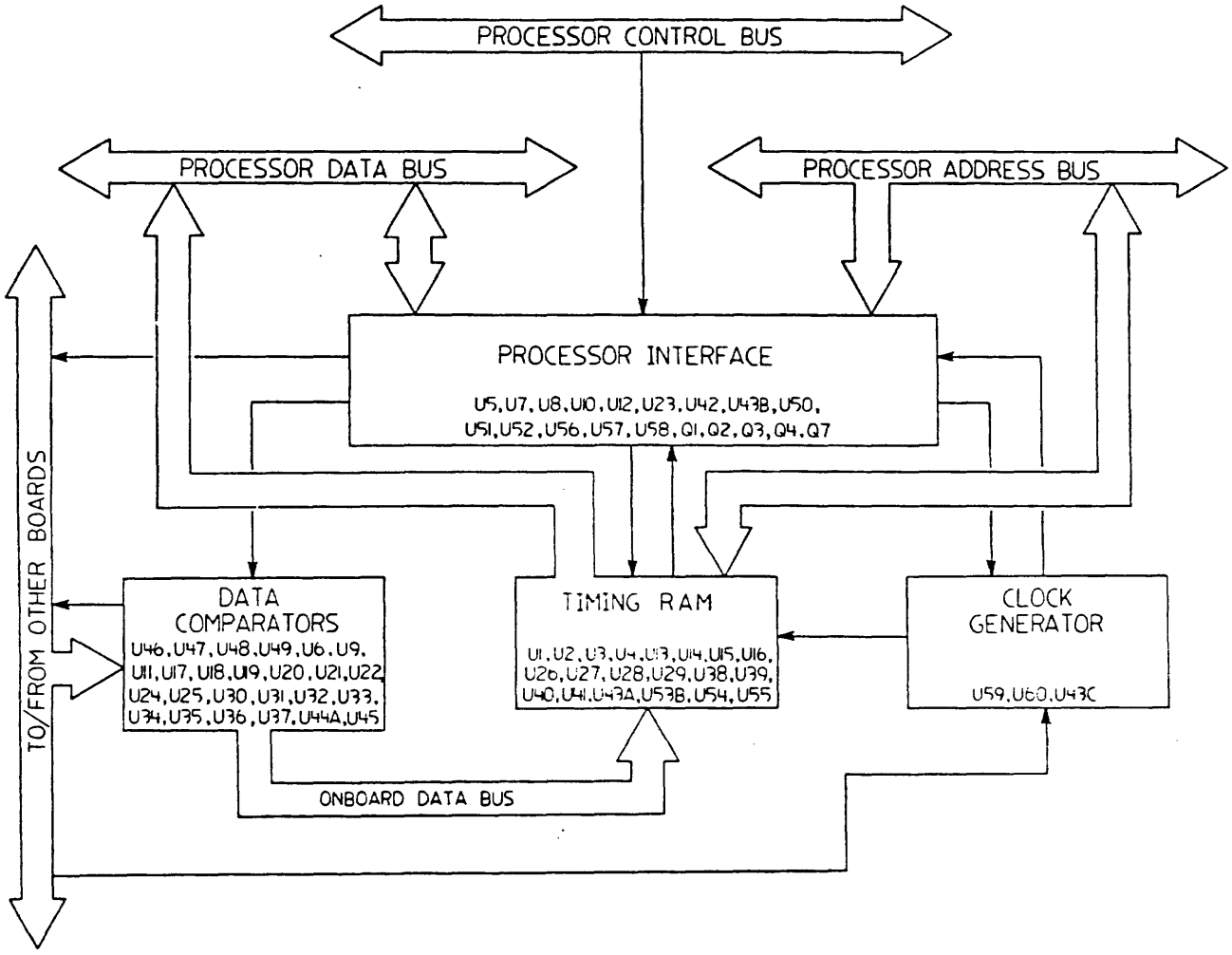


Figure 10-1 Timing Memory Board Block Diagram

nyms or terms that may be unfamiliar.

The functional units of the Timing Memory Board are the Processor Interface, Clock Generator, Timing RAM, and Data Comparators. These units are discussed in detail in the following subsection.

10.2.1 PROCESSOR INTERFACE

Refer to schematic #127-0065-001. The Processor Interface is comprised of the following components: The Address Decoder, A/B Decoder Probe Threshold Control, Control Port, Status Port, Last-Word Address Port (sheet 2), and Control Shift Register (partly on sheet 3, partly on sheet 4). This circuitry allows the Control Program to set up certain Probe parameters according to keyboard-entered instructions. It also causes certain control signals to be sent and to interrogate various status lines as needed.

The **Address Decoder** consists of U52, an MMI 6301-1 256-word x 4-bit PROM; U43B, a section of a 74S10 triple 3-input NAND gate (used as an inverter); and U51, a 74LS138 3-to-8 decoder. PROM U52 is enabled by processor control signal RW- (Read OR Write). The PROM accepts Address Bus signals A10-A15 and control signals S1 (Read) and IO+/M- (I/O + Memory -). These inputs are decoded to produce the following control signals:

a. RDLAST- (Read Last -), enables the Last-Word Address Port, U5 on sheet 2.

b. RDRAM- (Read RAM -), places the RAM Address Counter (U54 and U55 on sheet 2) in the load mode. This enables the processor to preset the counter or address the RAM.

c. EN51- (Enable U51 -), enables the second state address decoder, U51.

Decoder U51 is enabled by EN51-. U51 then accepts Processor Address Bus signals A0 and A1 and processor control signals IO+/M- and RW. It decodes them to produce the following control signals:

d. **EORAM0** (Enable Output, RAM 0), **EORAM1, EORAM2** and **EORAM3**, enable the outputs of RAM sections 0, 1, 2 and 3, respectively.

e. LDTHRESHA- (Load Threshold A -), and LDTHRESHB-, enable the CS- inputs of D/A converters U56, U57 in Threshold Control.

f. ENSTAT- (Enable Status -), enables the Status Port, U50.

g. ENCTRL- (Enable Control -), enables the Control Port, U42.

The A/B Decoder is located on the Motherboard but will be discussed in this section (see Motherboard schematic #127-0123-01). The circuit consists of sections D,E and F of U10, a 7406 hex open-collector inverter.

This circuit inverts some of the address bits sent to the B Memory Board S2 socket. This allows the Control Program to separately address the Timing Memory Boards. They must be plugged into the A and B Memory Board S2 sockets on the Motherboard.

The **Probe Threshold Control** consists of the following components: U56 and U57, AM 6080 8-bit D/A converters; and U58, an LM747 dual operational amplifier. U57 is enabled by LDTHRESHA-, received from the Address Decoder and WR-, received from the processor. D/A converter U57 converts a digital value to an analog voltage. The keyboard-entered digital value is sent from the Processor Data Bus by the Control Program. The analog voltage is applied to operational amplifier U58A that produces THRESHA. This signal is sent to the Model 80 Probe. THRESHA is a threshold reference voltage for the external clock, the qualifier, and data channels 0, 1, 2 and 3. Similarly, U56 and U58B supply THRESHB to the Model 80 Probe for data channels 4, 5, 6 and 7.

Potentiometer R19 is used to set the reference voltage applied to pin 14 of D/A converters U56 and U57. This voltage, as

measured at test point TP1, should be 10.0V, +/- 0.05V.

The **Control Port** consists of U42, a 74LS174 hex D flip-flop; Q3, a 2N3905 transistor; and Q7, a 2N3904 transistor. When flip-flop U42 is enabled by signal ENCTRL-, the following signals are clocked into the flip-flops from the Processor Data Bus:

a. **PRSCLKG-** (Preset Clock Generator), presets the four flip-flops in the Clock Generator.

b. **CLRCLKG-** (Clear Clock Generator), clears the four flip-flops in the Clock Generator.

c. **SRDATA** (Shift Register Data), serial data to be loaded into the Control Shift Register.

d. **CLKSR** (Clock, Shift Register), the clock that loads the Control Shift Register.

e. **HYSTCTRL** (Hysteresis Control), when high, adds hysteresis to the comparators in the Model 80 Probe. Transistors Q3 and Q7 supply signal HYST as a nominal level, measured with Probe connected. When hysteresis is ON it is +1.7V, when hysteresis is OFF it is -5.1V.

f. **DSELT+/W-** (Data Select Timing + / Waveform -), is sent to the Data Comparator circuits. It is used to select either Timing data from the Model 80 Probe or Waveform data from the Waveform Control Board.

The **Status Port** consists of U50, a 74LS367 hex bus driver with 3-state outputs; and Q4, a 2N3904 transistor. When the U50 outputs are enabled by ENSTAT-, this circuitry allows the processor to read the following signals:

a. CLKPH0- through CLKPH3- (Clock, Phase 0-3), when read at clock shutoff time, determines which of the four RAM sections contains the last data word collected.

b. **ROLLOVER**, indicates that the memory has been filled (at least once) and has started overwriting prior collected data with new data.

c. **ENDSRD** (End Shift Register Data), is the last bit in the Control Shift Register chain. This permits the Control Program to determine the status of SRDATA as shifted through the registers. Transistor Q4 converts the level from CMOS to TTL.

The **Last-Word Address Port** (sheet 2) consists of U5, a 74LS244 octal buffer with 3-state outputs. The inputs at U5 are received from the Address Counter. The outputs are sent to the Processor Data Bus. The outputs are enabled by RDLAST-, received from the Address Decoder after clock shutoff. When thus enabled, this port allows the Control Program to read the contents of the Address Counter. This counter still contains the last memory address that stored collected data. This address and the status of the 4-phase clock, provides the orientation point for processing the collected data. For example, counting back from this point by the post-trigger count establishes the location of the stored trigger word.

The **Control Shift Register** consists of U7, U8, and U23 (sheet 4), and U10 and U12 (sheet 3), all CMOS 4015 dual 4-bit static shift registers; and Q1 and Q2 (sheet 3), both 2N3905 transistors. Q1 and Q2 translate Control Port signals CLKSR and SRDATA from TTL level to CMOS level. Shift Register sections U7, U8, U10, and U12 transmit software-generated control signals to the Arm-Bit and Trigger-Bit Comparators. The comparators detect data matches with keyboard-specified arm and trigger words. Shift Register section U23 transmits the software-generated control signals to the Data Selectors. These select either Timing data or Waveform data for storage in the Timing RAM.

10.2.2 CLOCK GENERATOR

The Clock Generator (sheet 1) consists of U59 and U60, both 74S74 dual flip- flops; and

U43C, a section of a 74S10 triple 3-input NAND gate. This circuitry provides a 4-phase clock to the Timing RAM.

The four flip-flops are connected in cascade. All preset inputs are received in parallel by PRSCLKG-. All clear inputs are received in parallel by CLRCLKG-. The preset and clear signals both are received from the Control Port. The flip-flops are all clocked by CLKTTL from the Timing Control Board. The 4-phase clock outputs are sent from the Q-side of the flip-flops.

The Clock Generator is started in the preset condition. The D input of the first flip-flop held low by the output of gate U43C. Feedback around the first flip-flop, U59A, would normally produce a divide-by-two. In this case, the feedback is held off three CLKTTL clock periods. The hold off is accomplished by the 3-input NAND gate, U43C. The delay allows the Q-low pulse to ripple down to the third flip-flop, U60A. Refer to Figure 10-2. The result is an asymmetrical divide-by-four operation for each flip-flop. This produces the set of output clock signals shown in the figure. The clock pulse at the Q- output of each successive flip-flop is delayed from the preceding flip-flop by one CLKTTL period.

The 4-phase clock is sent to the Timing RAM section as CLKPH0-, CLKPH1-, CLKPH2- and CLKPH3-. One clock phase is applied to each of the four sections. An additional clock, CLKPH0+, is produced at the Q output of U59A and sent to the Address Counter. The application of these clocks will be discussed in the next subsection.

10.2.3 TIMING RAM

The Timing RAM (sheet 2) is comprised of the Address Counter, Rollover Detector, and Timing RAM Sections 0, 1, 2 and 3. Each of the four RAM sections stores 256 8-bit words, thus the total storage capacity is 1024 8-bit words. The memory is arranged so that the 45 ns RAMs can store data that is clocked at intervals as short as 10 ns.

The two Timing RAMs (one from each board) are used to store 2000 8-bit words or 1000 16-bit words sent from the Data Comparators. Although the full memory capacity is 2048 words, the post-trigger count is adjusted so that only 2000 or 1000 words are collected. The data received from the Comparators may have been generated by either the Model 80 Probe (as timing data) or the Waveform Control Board (as Waveform data). After collection, data stored in the Timing RAMs may be read by the Control Program for analysis and display.

The **Address Counter** consists of U54 and U55, both 74LS191 4-bit binary counters; and U44A, a section of a 74S10 triple 3-input NAND gate (used as an inverter). The two counters are wired to count up and are connected in cascade (through U43). This will produce an 8-bit output. The 8-bit output is sent to the input of Address Latch U4 (Timing RAM Section 0) and to the Last-Word Address Port.

The counter load-control inputs are controlled by RDRAM- generated by the Address Decoder. When RDRAM- is low, the counter outputs follow the inputs. This mode is used by the Control Program to preset the counter to 000 before data collection starts. This mode is also used to address the Timing RAM when reading data after collection stops. The counter is clocked by CLKPH0+ sent from the Clock Generator. Clocking occurs on the positive-going edge of this signal.

When data collection begins, the Address Counter starts from 000 and advances the address one count with each CLKPH0+ clock. The maximum count is 256 (000-255), the memory capacity of one section of the Timing RAM. If clocking continues beyond this point, the counter overflows and starts over again from 000. Counting stops when the CLKTTL input clock to the Clock Generator is stopped by the Timing Control Board.

The **Rollover Detector** consists of U53B, one-half of a 74LS73 dual J-K flip-flop. This circuit detects the first occurrence of overflow of the Address Counter. The J input of the flip-flop is wired high, and the K input is wired low. Once set, the flip-

flop will not change state again until reset by a low clear signal at pin 6. The flip-flop is clocked by the MSB, RA7, of the Address Counter. Clocking occurs on the negative-going edge of this signal. As maximum address count is approached, the MSB goes low again. This transition clocks the flip-flop. The signal used to clear the flip-flop, PRSCLKG-, is sent from the Control Port. The same signal is used to preset the Clock Generator. Thus, before the start of data collection, the Rollover Detector is cleared at the same time the Clock Generator is initialized.

The flip-flop outputs ROLLOVER that is sent to the Status Port on sheet 1. There it can be accessed by the Control Program. After data collection has stopped, the Rollover Detector state is used to determine the location of the trigger word in the Timing RAM.

Timing RAM Section 0 consists of the following components: U16 and U29, both Fairchild 93422 256-word x 4-bit static RAMs with 3-state outputs; Address Latch U4, a 74S373 octal D latch; and Data Flip-Flop U41, a 74S374 octal D flip-flop. This circuitry stores 256 8-bit words of collected data.

The address inputs of the two RAMs are received in parallel from Address Latch U4. The inputs of the Address Latch are sent from the Address Counter, signals RA0 (RAM Address bit 0) through RA7. The 4-bit data inputs of the two RAMs are connected in cascade to the 8-bit output of Data Flip-Flop U41. The inputs of the Data Flip-Flop are received via the on-board Timing Data Bus. These input signals are TDB0 (Timing Data Bus bit 0) through TDB7. The 4-bit data outputs are sent in cascade to the 8-bit Processor Data Bus. These signals are DB0 (Data Bus bit 0) through DB7.

The output-enable inputs of the two RAMs are controlled in parallel by signal EORAM0- sent from the Address Decoder. The phase-0 clock signal, CLKPH0-, is received from the Clock Generator, and sent to the following points: The two RAM write-enable inputs, U16-20 and U29-20; the Address Latch enable, U4-11; and the Data Flip-Flop clock input, U41-11.

Timing RAM Section 1 consists of RAMs U15 and U28, Address Latch U3, and Data Flip-Flop U40. IC types are the same for all four RAM sections. The address inputs of the two RAMs are received in parallel from Address Latch U3. The inputs of the Address Latch are received from **Address Latch U4** in Section 0. The other operations of this section are similar to those of Section 0. The exceptions are that enable signal EORAM1- is sent from the Address Decoder and clock signal CLKPH1- is sent from the Clock Generator.

Timing RAM Section 2 consists of RAMs U14 and U27, Address Latch U2, and Data Flip-Flop U39. The operations of this section are similar to those of Section 1. The differences are as follows: The inputs of Address Latch U2 are received from Address Latch U3 in Section 1; the enable signal is EORAM2-, and the clock signal is CLKPH2-.

Timing RAM Section 3 consists of RAMs U13 and U26, Address Latch U1, and Data Flip-Flop U38. The operations of this section are similar to those of Section 2. The differences are as follows: The inputs of Address Latch U1 are received from Address Latch U2 in Section 2; the enable signal is EORAM3-, and the clock signal is CLKPH3-.

As described, the address inputs to the RAM sections are configured in an open loop. They are sent as follows: From the Address Counter to the Section 0 Address Latch, from the Section 0 Address Latch to the Section 1 Address Latch, from the Section 1 Address Latch to the Section 2 Address Latch, and from the Section 2 Address Latch to the Section 3 Address Latch. The reason for using this design will become apparent.

A typical data collection cycle is described below. Refer to Figure 10-2, the Clock Generator Timing Diagram. Data word AA on the Timing Data Bus is clocked into U41 Section 0 Data Flip-Flop by the positive-going edge of CLKPH0-. Refer to point A on the timing diagram. This data is held in U41 until the next positive-going clock edge

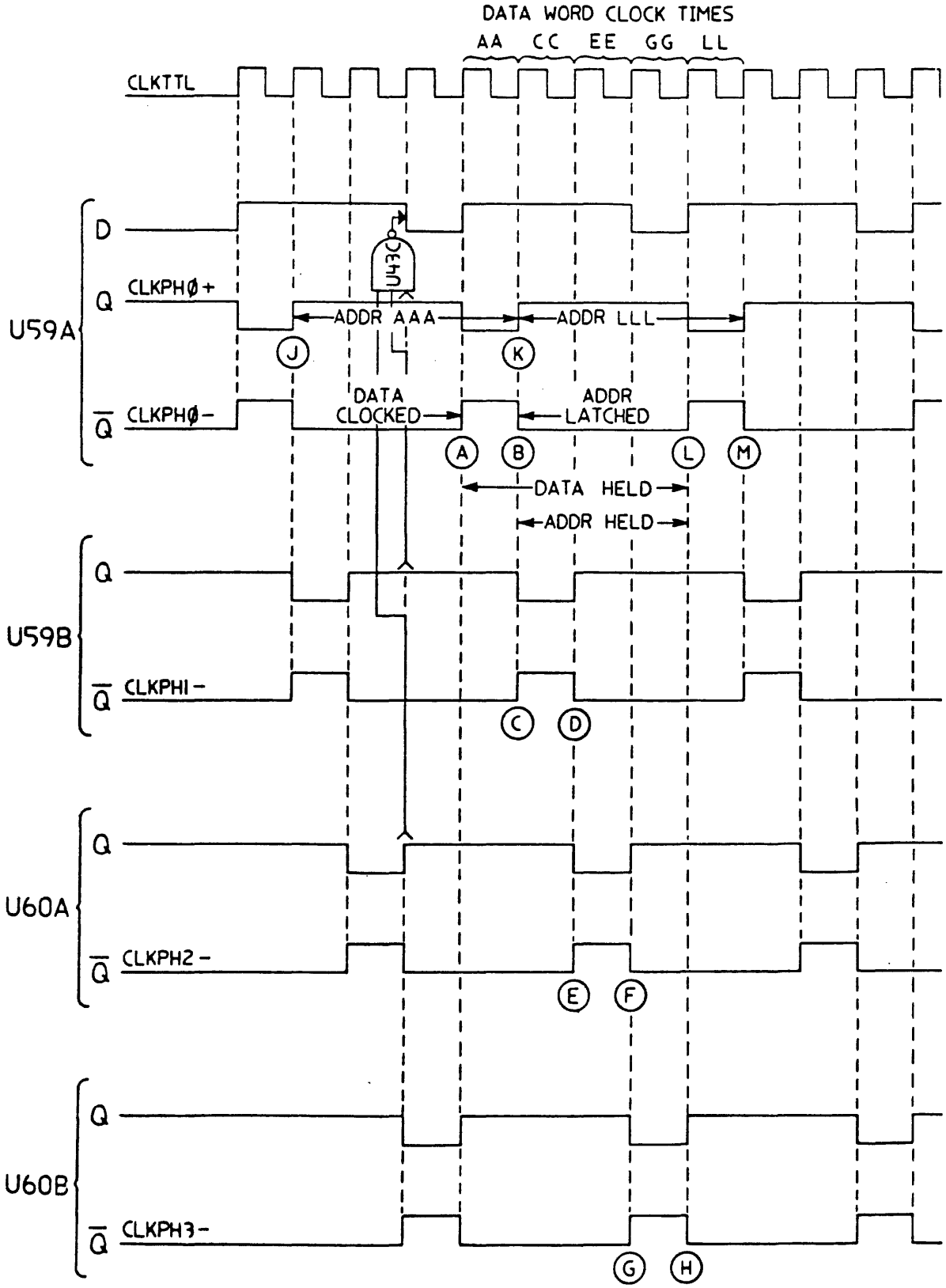


Figure 10-2 Clock Generator Timing Diagram

at point L. Address AAA, the current address count, was set in the Address Counter by CLKPH0+ at point J. This address is latched in the U4 Section 0 Address Latch. The address is latched by the low level at the negative-going transition of CLKPH0-. Refer to point B on the diagram. The address is held latched for the duration of the low level.

The Address Counter is advanced one count by the positive-going edge of CLKPH0+ (point K on the diagram). This point coincides with the address latch point B. However, note that propagation time delays the arrival of the new address at Section 0, until after the current address has been latched. The new address at Section 0 is LLL, the current address is AAA. The write enable inputs of the Section 0 RAMs are also brought low at point B. This write enable pulse is held true until the positive-going transition of CLKPH0- at point L. The data and address inputs are both held stable for the duration of this pulse.

The 93422 RAMs are described in the following paragraphs. The minimum write-pulse length, specified as 30 ns, is always exceeded. Even using the minimum CLKTTL period of 20 ns, the write-pulse width is 3 x 20 ns = 60 ns. The data is clocked into the Data Flip-Flop one CLKTTL period ahead of the write pulse. This provides a data set-up time of at least 20 ns, four times the specified 5 ns minimum. The address is latched in the Address Latch on the same clock transition that starts the write pulse. However, the address has been stable for much longer than the required 10 ns. The total time is approximately 70 ns as follows: The time is 50 ns minimum in the Address Counter for the Section 0 RAMs. In addition, it has been stable for 20 ns minimum in the preceding Address Latch for the RAMs in Sections 1, 2, and 3.

At point C the positive-going edge of CLKPH1- clocks data word CC into the Section 1 Data Flip-Flop U40. Data has changed since point A because the data is being sent to the Data Flip-Flops at the CLKTTL rate. The flip-flops are connected in parallel to the on-board Timing Data Bus.

At point D, the AAA address being held in the Section 0 Address Latch is latched into the Section 1 Address Latch by the low level of CLKPH1-. Note that although a count increment has been started in the Address Counter, address AAA can still be used by Sections 1, 2 and 3. This is because of the series loop connection of the Address Latches. The write-enable inputs of the Section 1 RAMs are also brought low at point D, thus storing word CC.

Data word AA is now written into the Section 0 RAMs at address AAA. Data word CC is written into the Section 1 RAMs at address AAA. Data is clocked at point E and addresses latched at pint F. This operates so that data word EE is written into the Section 2 RAMs at address AAA. Similarly, data word GG is written into the Section 3 RAMS at address AAA.

At the next clock pulse of CLKPH0-, L-M, the next sequential address LLL is stable at the Address Counter output. Address LLL then is latched in the Section 0 Address Latch. The next set of four data words is written into the four RAM sections at address LLL. The first word written is data word LL in the Section 0 RAMs.

Each address stores four consecutive data words, one in each RAM section. Each RAM section stores every fourth data word in consecutive addresses. When the Address Counter has reached maximum count, each RAM section contains 256 data words. This makes a total of 1024 data words interlaced in the four RAM sections.

At the next CLKPH0+, the Address Counter overflows and starts over at address 000. Data collection may end at any address count and on any one of the 4-phase clock pulses.

At the end of data collection (post-trigger terminal count), CLKTTL stops. This stops the Clock Generator that in turn stops the Address Counter. This leaves all Timing RAM Address Latches and Data Flip-Flops in the same state as at the last memory write. The Control Program reads the Last-Word Address Port to find the address of the last

word stored. It also reads, from the Status Port, the state of the four flip-flops in the Clock Generator. This defines which RAM section stored the last word at that last address. The Control Program can then locate the address and RAM section for any desired stored data word.

After the CLKTTL has stopped, the Control Program can read data words from the Timing RAM. This is done by bringing the Address Counter load control lines low with signal RDRAM- received from the Address Decoder. The Address Counter receives addresses from the Processor Address Bus. In this load mode, the incoming addresses are sent straight through the Section 0 Address Latch, U4. The Control Program also clears the Clock Generator flip-flops with CLRCLKG- received from the Control Port. This brings all clock outputs to the RAM Address Latches high. This holds all four Address Latches in the transparent mode.

The sequence of operations is described as follows. The Control Program places an address on the Processor Address Bus. That address is sent by the Address Counter to all four Address Latches in the loop. Note that all four RAM sections are addressed simultaneously. The Control Program can select the RAM section that contains the word to be read. That RAM section is selected by activating the proper RAM output-enable line. This signal is one of EORAM0- through EORAM3-, and is sent via the Address Decoder.

10.2.4 DATA COMPARATORS

There are eight Data Comparators, one for each of the eight parallel incoming data lines. The incoming data may be sent from the Waveform Control Board or from the Model 80 Probe. If sent from the Waveform Control Board, the data is applied only to the Data Selector and the ECL-to-TTL translator. The Data Selector selects either the Waveform or Timing data. If sent from the Model 80 Probe, the data is acted upon by two comparator functions. The first of these detects any glitch in the data. The second detects any match with a corresponding arm or trigger-word bit.

The NPC 764 Logic Analyzer operation defines a glitch as follows: A pulse on a data line that exceeds the selected voltage threshold and is shorter than the selected analyzer clock period. A user definition of a glitch may be as follows: A pulse shorter than the normal data period or target-system clock period. Since the analyzer clock period is usually shorter than the incoming data period, many such user-defined glitches are processed as data. They are therefore displayed to the user without requiring the use of the glitch capture mode.

Selection of glitch-capture or sample mode of input data is made on a line-by-line basis by menu-prompted keyboard entries. The Data Comparators allow the Control Program to turn glitch capturing on or off for each incoming data line.

Data Comparator 0, shown on sheet 4, consists of the following components:

a. U48B,C, sections of a 10102 quad NOR gate.

b. U47A, one-half of a 10130 dual latch.

c. U36B, one-half of a 10131 dual master-slave, positive-edge clocked, type D flip-flop.

d. U19, a 10117 dual 2-3-input OR-AND/OR-NOR gate used as a 2-wide OR-NOR gate.

e. U31B, one-fourth of a 10158 quad 2-input multiplexer.

f. U30A, one-fourth of a 10125 quad ECL-to-TTL translator.

This circuitry performs the data comparator and data selection functions for data bit 0.

Data Comparators 1 through 7 (sheets 3 and

4) operate identically to Data Comparator 0. The IC numbers and signal term names differ.

The following description of the function of Data Comparator 3 can be applied to the other seven Comparators. Refer to Figures 10-3 and 10-4.

Timing data sent from the Model 80 Probe is applied in to the Comparator in differential form. That is, as two signals of opposite polarity, here labeled D3+ and D3- (Figure 10-3). D3+ is sent to the D input of Data Latch U37B. The common clock input for the U37 dual latch, C-, is left unconnected and is pulled low internally. The two latches in U37 are therefore controlled independently by their individual CE- inputs. The CE- input of U37B is received with signal D3G+/S- (Data Bit 3, Glitch + / Sample -). Signal D3G+/S- is sent from the U23 section of the Control Shift Register (sheet 4).

If the **sample mode** has been selected for Data Bit 3, the CE- input of latch U37B is held low with D3G+/S-.

When the CE- input is low, the set and reset inputs of U37B are inhibited. This causes the Q output to follow the D input. Thus in the sample mode Data Latch U37B has essentially no effect. Timing data is sent straight through to the D input of Data Flip-Flop U32A. U32A is a master-slave, type D flip-flop that is clocked by the positive-going edge of the clock signal. The U32A clock input is received with signal CT (Clock, Timing). CT is received, via U44A, from the Clock Control on the Timing Control Board.

The CT clock is keyboard-selected as either external or internal. If the clock is internal, the clock period is also keyboard-selected. For Timing analysis, the clock is usually selected as internal. The clock period is usually selected to be shorter than the data period by a factor of at least 10. This ensures that resolution will be adequate.

When **glitch-capture mode** has been selected for Data Bit 3, the CE- input to U37B is held high with signal D3G+/S-. The latched mode is defined as when the CE- input is high. In this mode the D input has no effect and U37B responds only to the set and reset inputs. The outputs of Comparator Gates U49C and U49D are sent to U37B set and reset inputs, respectively. D3- and the U32A Q output are applied to the inputs of gate U49C. The D3+ and the U32A Q- output are applied to the inputs of gate U49D.

Comparator Gate U49C detects positive-going transitions in D3+ by detecting the negative-going transitions in D3-. Comparator Gate U49D detects any negative-going transitions in D3+. Any positive-going transition in D3+ (whether by data or glitch) sets latch U37B. Any negative-going transition in D3+ resets latch U37B. The U37B Q output is clocked into flip-flop U32A as in the sample mode.

Note that the ECL devices used in the Comparator circuits are fast enough so that any glitch pulses $\geq$5 ns will be detected.

Operation of the **Arm-Bit and Trigger-Bit Comparator Gates** is described as follows. The upper OR gate of Arm-Bit Comparator Gate U9B receives the Q output of U32A and software-generated signal AW3B1-. This is the Arm Word 3-Bit selected as 1 -. The lower OR gate of U9B receives the Q- output of U32A and signal AW3B0-. These AW3B signals are software-generated in accordance with keyboard selection. They are generated by U8 of the Control Shift Register in the Processor Interface. The output of the NAND gate in U9B is ANDed with the outputs of the other seven Arm-Bit Comparator Gates. All seven Comparator Gate outputs must be low in order to produce a low TA- output signal.

If Arm-Word Bit 3 was keyboard-specified as a 1 (high), then signal AW3B1- is held low (true) and signal AW3B0- high. If arm bit 3 was specified as a 0, the Control Program holds AW3B1- high and AW3B0- low. If arm bit 3 was specified as X (don't care), the Control Program holds both AS3B1- and AW3B0- high.

Assume that arm bit 3 was specified as a 1.

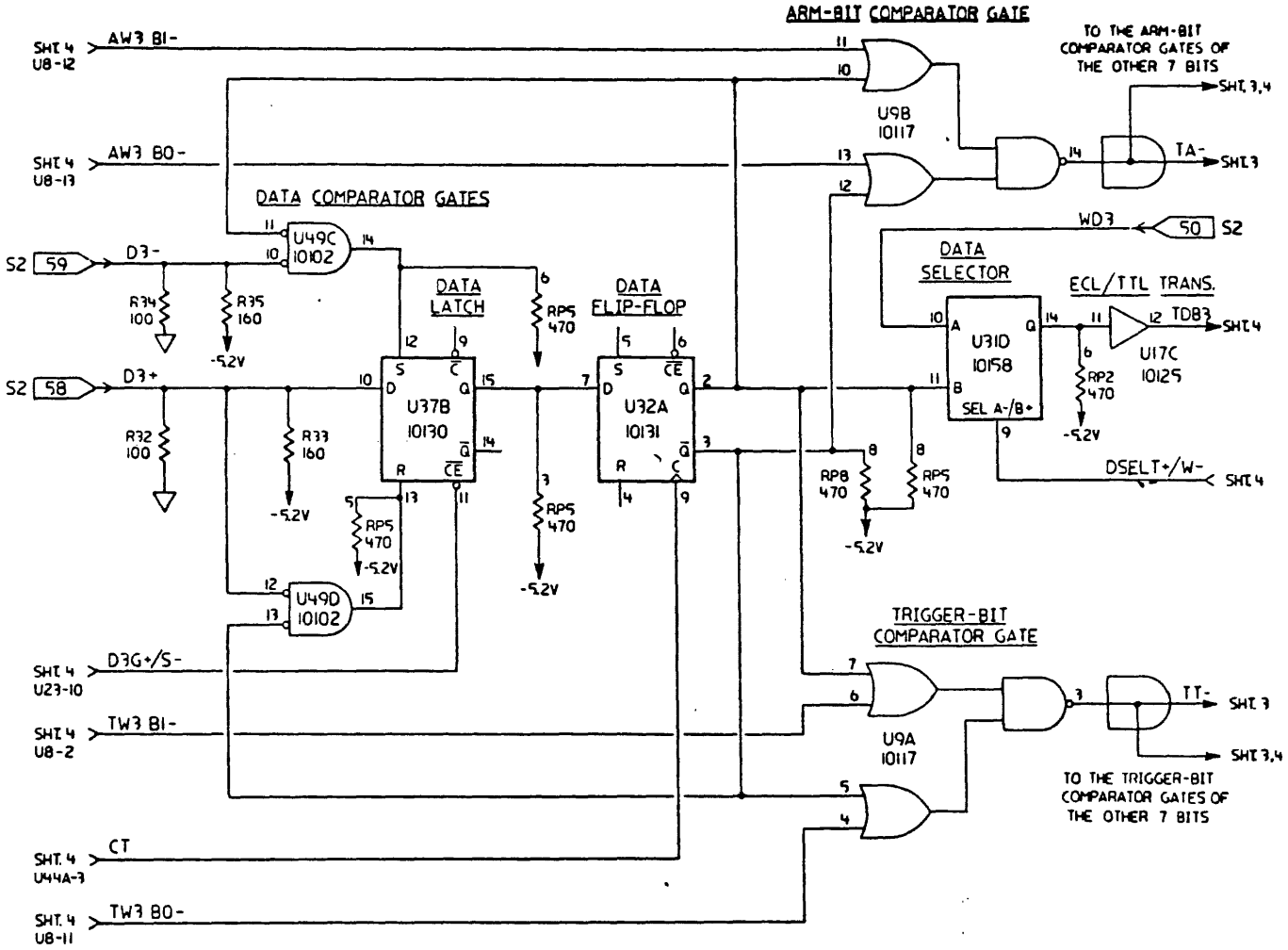
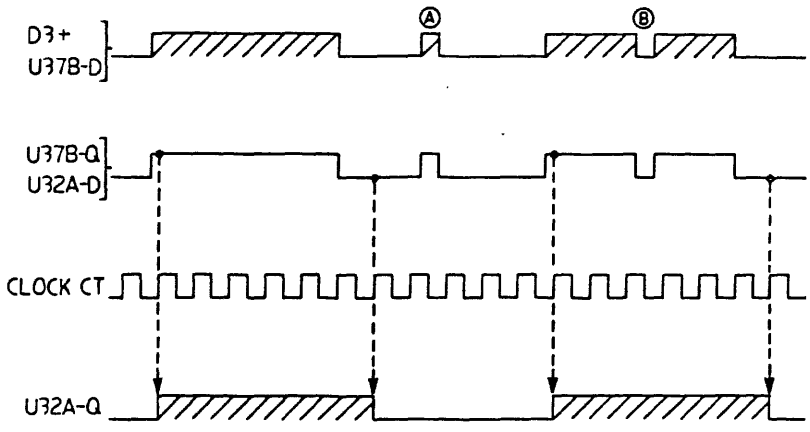


Figure 10-3 Data Comparator Expanded Schematic



SAMPLE MODE

Figure 10-4 Data Comparator Timing Diagram

Signal AW3B0- will be high, and the lower OR gate of U9B will always have a high output. This will be true regardless of the data input. This leaves the upper OR gate in control of the U9B NAND gate output. Signal AW3B1- will be low, and as long as U32A-Q (that reflects D3+) is low. The output of the upper OR gate will be low and U9B-14 will contribute a low to the wired AND output TA-. If the outputs of the other seven Arm-Bit Comparator Gates are also low, TA- will be low. This indicates that an arm-word match has occurred.

If arm bit 3 was specified as a 0, U32A-Q- goes high (indicating that D3+ is low). Signal U39B-14 will contribute a low to the wired AND output TA-.

If arm bit 3 was specified as an X, the output of both OR gates will always be high (because both AW3B1- and AW3B0- are high). Signal U9B-14 will constantly contribute a low to TA-.

In the glitch-capture mode, the captured glitches will have the same effect as data on the operation of the Arm-Bit Comparator Gate. Spurious bit matches can be prevented by a keyboard-specified arm-word filter setting of 2. This designates that the arm-word match must be present at least two clock periods in order to be acted upon. However, filter settings greater than 2 must be used with caution when the signal period is less than 10 times the clock period.

Note that the filtering action affects **only** the arm-word and triggering-word match function. It does **not** affect the storage and display of collected data. Refer to the Trigger Filter circuit shown on Timing Control schematic sheet 3.

The Trigger-Bit Comparator Gate operates in exactly the same way as the Arm-Bit Comparator Gate. The output of U9A (TT-) is connected in a wired AND with the outputs of the other seven Trigger-Bit Comparator Gates.

Data Selector U31D is used by the Control Program to select either Timing data or Waveform data. The selected data will be stored in the Timing RAM. Bit 3 Timing data is sent from U32A-Q to input B of U31D. Bit 3 Waveform data (WE3) is sent from the Waveform Board via pin S2-50 to input A of U31D. Signal DSELT+/W- is the Data Select Timing + / Waveform - signal. DSELT+/W- is used to select one input or the other as output to the level translator U17C. The output of U17C, TDB3 (Timing Data Bus bit 3) is placed on the on-board Timing Data Bus. This signal is applied to the inputs of the Data Latches in the Timing RAM sections.

10.3 SCHEMATIC, BOARD LAYOUT, AND PARTS LIST

The schematic diagram, board layout, and parts list for the Timing Memory Board are contained on the following pages.

PARENT ITEM 143-0065-0001 | CROSS REF ITEM | DESCRIPTION BASIC TIMING MEMORY P.C. ASSY ENGR DRAW ECO 541 REV H | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

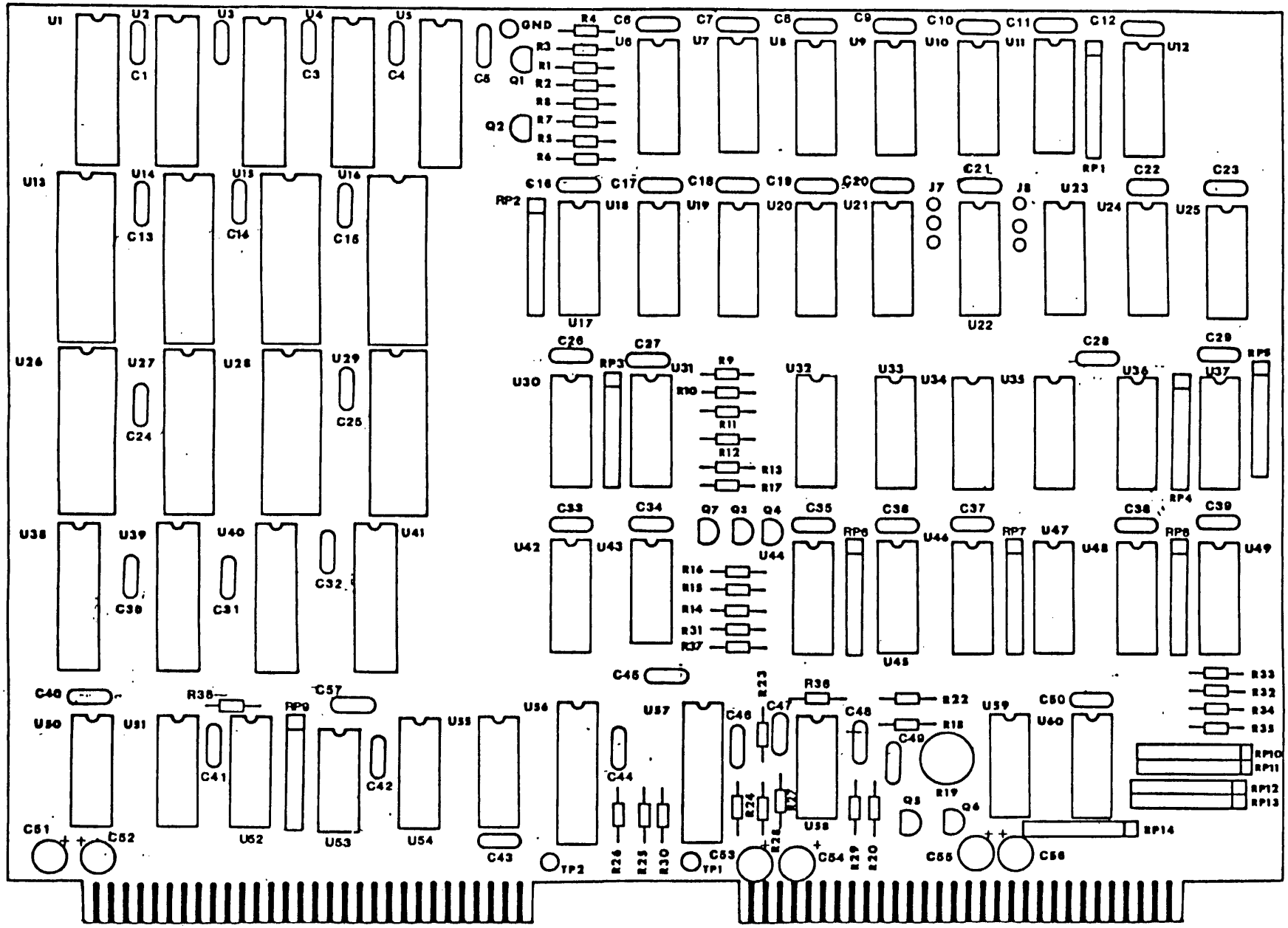
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	112-0113-0001	OP AMP LM747C U58		1.000	EA	4C					
	05	113-0002-0010	I.C. 74S10 U43		1.000	EA	4C					
	05	113-0002-0074	I.C. 74S74 U59 U60		2.000	EA	4C					
	05	113-0002-0373	I.C. N74S373N U1 U2 U3 U4		4.000	EA	4C					
	04	113-0002-0374	I.C. 74S374 U38 U39 U40 U41		4.000	EA	4C					
	04	113-0003-0073	I.C. 74LS73 U53		1.000	EA	4C					
	06	113-0003-0138	I.C. 74LS138 U51		1.000	EA	4C					
	06	113-0003-0174	I.C. 74LS174 U42		1.000	EA	4C					
	05	113-0003-0191	I.C. 74LS191 U54 U55		2.000	EA	4C					
	05	113-0003-0244	I.C. 74LS244 U5		1.000	EA	4C					
	05	113-0003-0367	I.C. 74LS367 U50		1.000	EA	4C					
	05	113-0017-0002	I.C. 93L422 93422 93412 U13 U14 U15 U16 U26 U27 U28 U29		8.000	EA	4C					
	04	113-0042-0001	I.C. SCL4015AE U10 U12 U23 U7 U8		5.000	EA	4C					
	04	113-0043-0001	I.C. AY6060 U56 U57		2.000	EA	4C					
	04	113-0200-0102	I.C. MC10102 U35 U46 U48 U49		4.000	EA	4C					
	05	113-0200-0116	I.C. MC10116 U44		1.000	EA	4C					
	04	113-0200-0117	I.C. MC10117 U11 U19 U20 U21 U24 U25 U6 U9		8.000	EA	4C					
	05	113-0200-0125	I.C. MC10125 U17 U36		2.000	EA	4C					
	04	113-0200-0130	I.C. MC10130 U34 U37 U45 U47		4.000	EA	4C					
	04	113-0200-0131	I.C. MC10131 U22 U32 U33 U39		4.000	EA	4C					
	04	113-0200-0158	I.C. MC10158 U18 U31		2.000	EA	4C					
	04	143-0065-0093	TIMING MEMORY PCB ASSY-OUTSIDE ECO 512 REV I		1.000	EA	1C					

PARENT ITEM 143-0055-0002 CROSS REF ITEM DESCRIPTION TIMING MEMORY PCB ASSY-OUTSIDE FOR DRAW ECO 612 REV I BATCH QTY 1 ITEM TYPE 1 LOW LEVEL 04 EFFEC 12/08/82 UNIT MEAS EA PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	110-0005-0037	82 OHM 1/4W 5% CF RES R13		1.000	EA	4C					
	05	110-0005-0039	100 OHM 1/4W 5% CF RES R22 R29 R32 R34		4.000	EA	4C					
	05	110-0005-0044	150 OHM 1/4W 5% CF RES R33 R35		2.000	EA	4C					
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R39		1.000	EA	4C				7/10/80	
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R20		1.000	EA	4C					
	06	110-0005-0059	680 OHM 1/4W 5% CF RES R9		1.000	EA	4C				9/30/90	
	05	110-0005-0063	1K OHM 1/4W 5% CF RES R1 R12 R3 R31 R4 R5 R7 R8		8.000	EA	4C					
	05	110-0005-0067	1.5K OHM 1/4W 5% CF RES R10 R11		2.000	EA	4C					
	05	110-0005-0071	2K OHM 1/4W 5% CF RES R16 R37		2.000	EA	4C				10/06/81	
	06	110-0005-0075	3.3K OHM 1/4W 5% CF RES R13 R14 R15 R2 R6		5.000	EA	4C					
	05	110-0005-0096	24K OHM 1/4W 5% CF RES R17		1.000	EA	4C					
	05	110-0051-0794	20K 1/4W .5% RES R24 R25 R26 R30		4.000	EA	4C				6/29/82	
	05	110-0051-0850	1.07K 1/4W .5% RES R23 R27 R28 R36		4.000	EA	4C				6/29/82	
	06	110-0205-0001	POT, 50 OHM, TRIM 3329H-50 R18		1.000	EA	4C					
	05	110-0306-0001	RN 100 OHM X7 8 PIN SIP RP11 RP13		2.000	EA	4C					
	05	110-0307-0001	RN 150 OHM X7 8 PIN SIP RP10 RP12		2.000	EA	4C					
	05	110-0308-0001	RN 470 OHM X7 8 PIN SIP RP14 RP2 RP3 RP4 RP5 RP6 RP7 RP8 RP9		9.000	EA	4C					
	05	110-0309-0001	RN 4.7K OHM X7 8 PIN SIP RP1		1.000	EA	4C					
	06	111-0004-0072	.1 UF 25V CD CAP C1 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C4 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C5 C50 C6 C7 C8 C9		50.000	EA	4C					

PARENT ITEM	CROSS REF ITEM	DESCRIPTION	BATCH QTY	ITEM TYPE	LOW LEVEL
143-0065-0090		TIMING MEMORY PCB ASSY-OUTSIDE ENGR DRAW ECO 612 REV I	1 EFFEC 12/08/82	1 UNIT MEAS EA	04 PLANNER

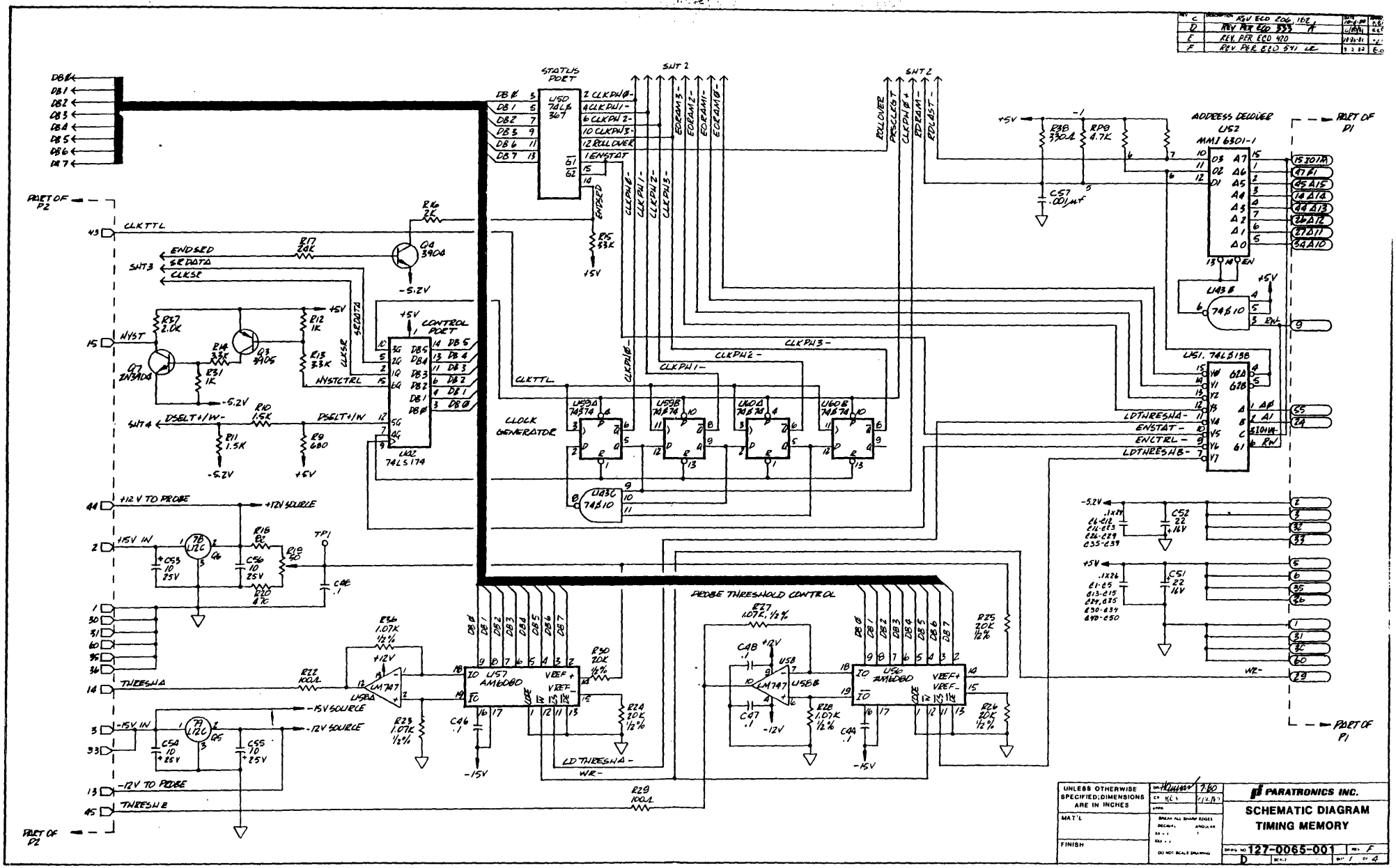
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	111-0012-0050	.001 UF 1KV CD CAP C57		1.000	EA	4C				7/10/80	
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C51 C52		2.000	EA	4C				3/29/82	
	05	111-0209-0096	10 UF 25V ELECT RADIAL CAP C53 C54 C55 C56		4.000	EA	4C				3/29/82	
	06	112-0100-0001	TRANSISTOR 2N3904 Q4 Q7		2.000	EA	4C					
	06	112-0101-0001	TRANSISTOR 2N3905 Q1 Q2 Q3		3.000	EA	4C					
	05	112-0115-0001	V.REG +12V LM78L12ACZ 78L12CP Q6		1.000	EA	4C					
	05	112-0116-0001	V.REG -12V 79L12CPMOT LM320LZN Q5		1.000	EA	4C					
	06	115-0003-0001	SOCKET 14PIN U43 U53 U58 U59 U60		5.000	EA	4C					
	06	115-0005-0001	SOCKET 16PIN U10 U11 U12 U17 U18 U19 U20 U21 U22 U23 U24 U25 U30 U31 U32 U33 U34 U35 U36 U37 U42 U44 U45 U46 U47 U48 U49 U50 U51 U52 U54 U55 U6 U7 U8 U9		36.000	EA	4C					
	06	115-0009-0001	SOCKET 20PIN U1 U2 U3 U38 U39 U4 U40 U41 U5 U56 U57		11.000	EA	4C					
	06	115-0010-0001	SOCKET 22PIN U13 U14 U15 U16 U26 U27 U28 U29		8.000	EA	4C					
	06	117-0030-0001	TERMINAL 120-1032-04 CAMBION TP1 TP2 TP3		3.000	EA	4C					
	05	126-0065-0001	TIMING MEMORY PC FAB	ECO 541 REV F	1.000	EA	4C					

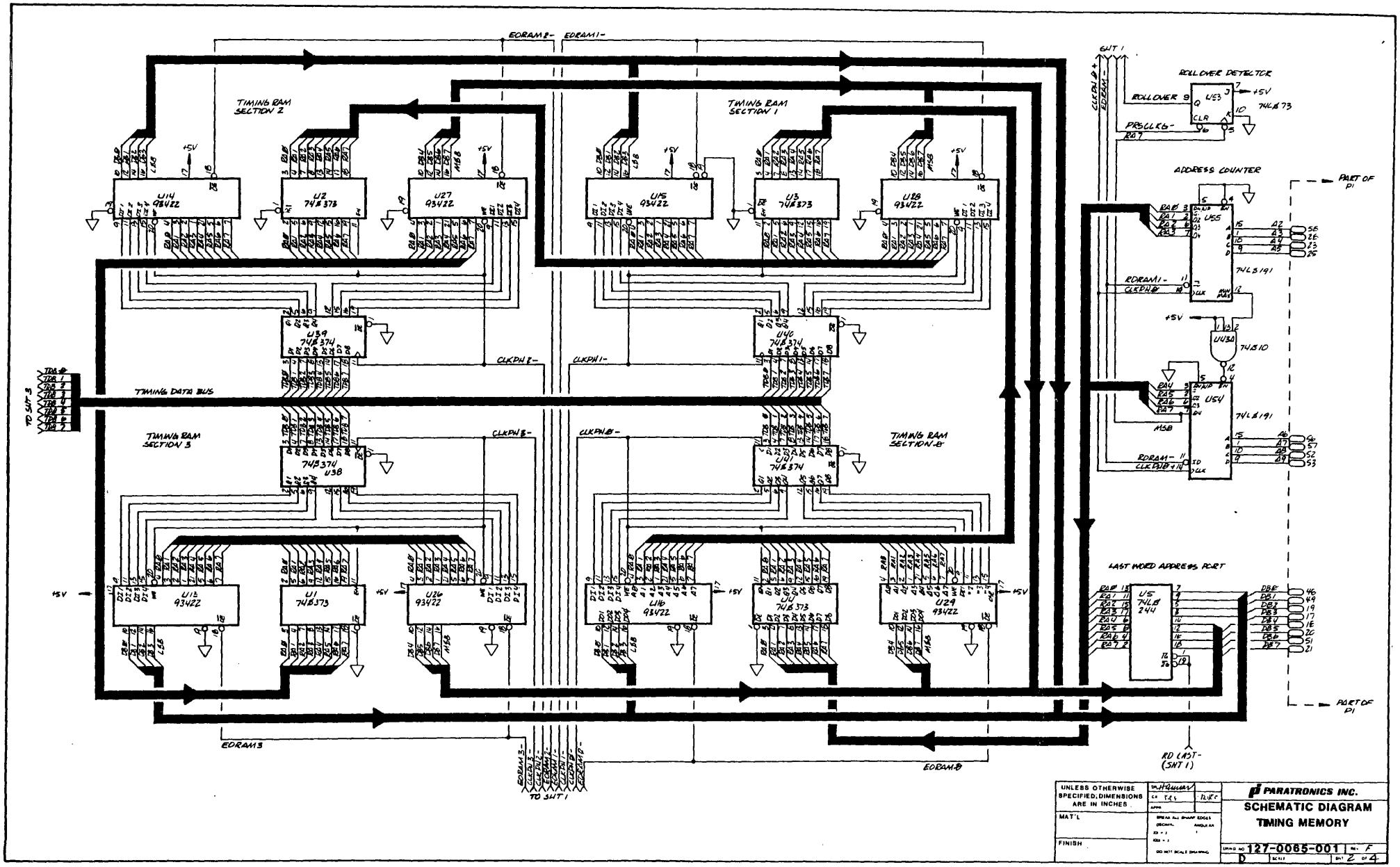


Timing Memory

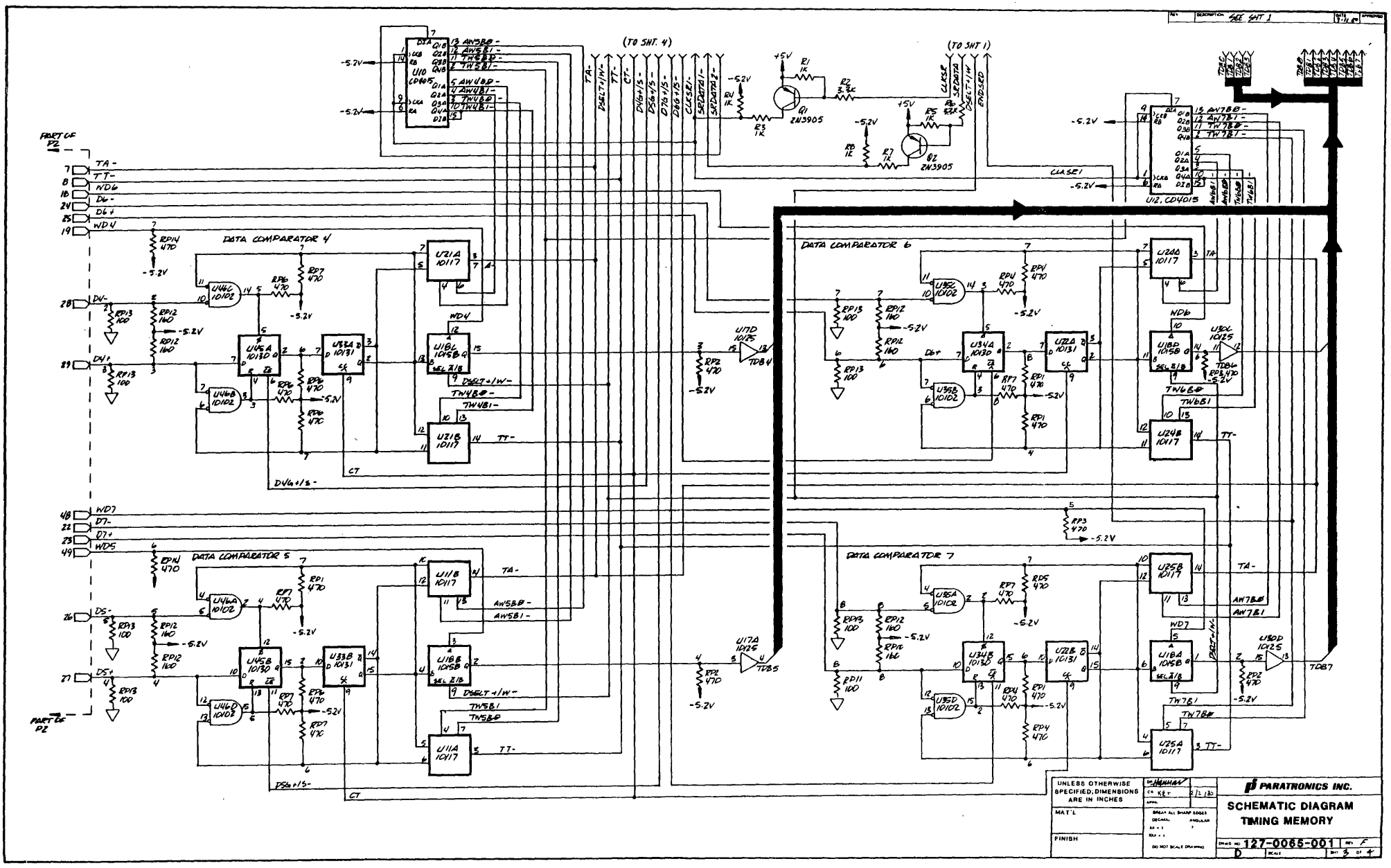
NICOLET PARATRONICS

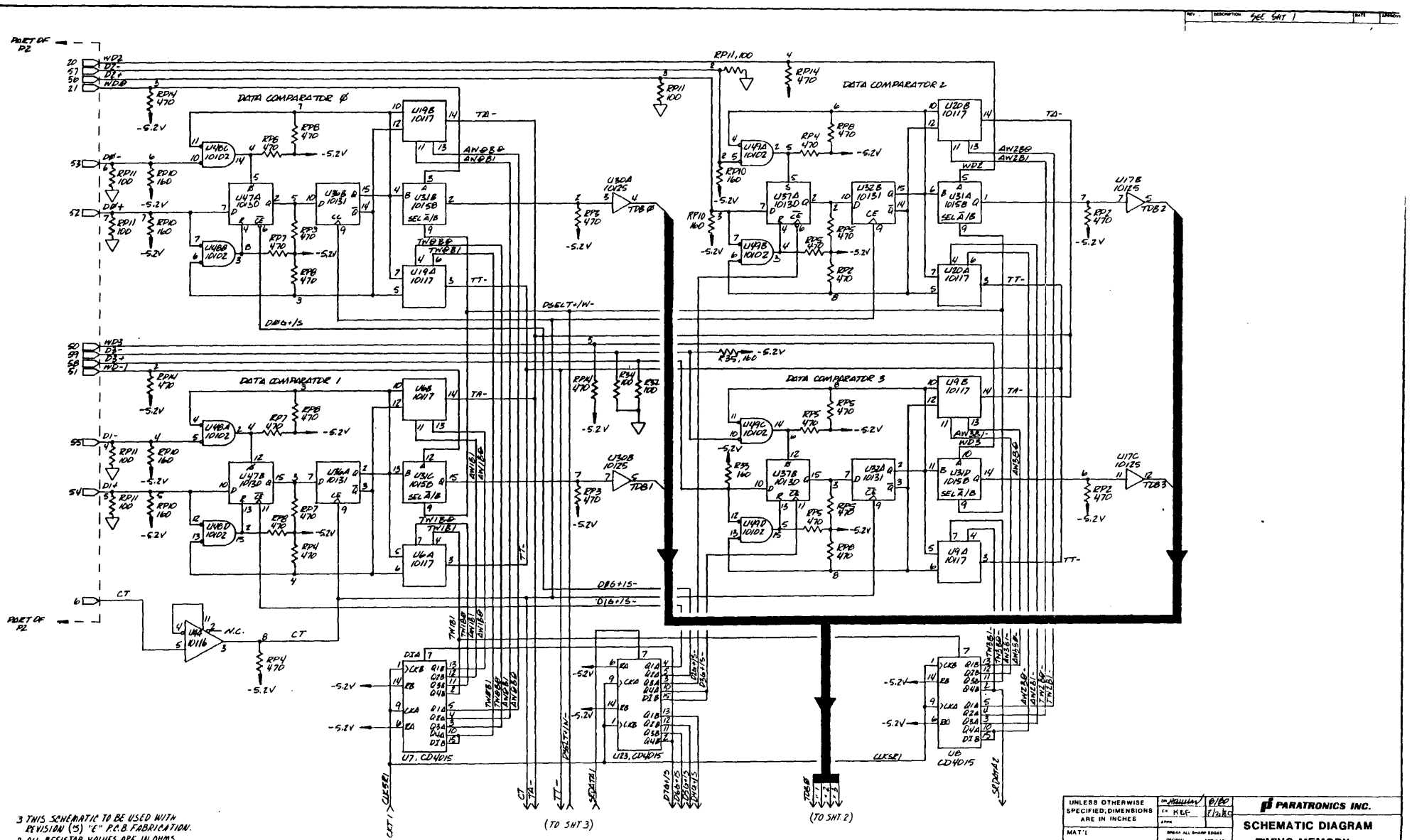
126-0065-0201 Rev. C


PARATRONICS INC.
SCHEMATIC DIAGRAM
TIMING MEMORY
127-0065-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DO NOT SCALE DRAWING
STATUS PORT
CONTROL PORT
ADDRESS DECODER U52 MMI 6301-1
CLOCK GENERATOR
PROBE THRESHOLD CONTROL
U50 74LS367
U52 74LS174
U57 AM6080
U58 LM747
U59A 74S74
U59B 74S74
U60A 74S74
U60B 74S74
U61, 74LS138
U43A 74S10
U43B 74S10
U43C 74S10
CLKTTL
ENDSED
SEDATA
CLKSE
SHT3
SHT4
HYST
HYSTCTRL
DSELT+/W-
DSELT+/W
+12V TO PROBE
+12V SOURCE
-12V SOURCE
-15V SOURCE
+15V IN
-15V IN
-12V TO PROBE
THRESH A
THRESH B
TP1
CLKPH0-
CLKPH1-
CLKPH2-
CLKPH3-
EDRAM3-
EDRAM2-
EDRAM1-
EDRAM0-
ROLLOVER
PRSCLKGT
CLKPH0+
EDRAM+
ROLLST-
LDTHRESHA-
ENSTAT-
ENCTRL-
LDTHRESHB-
WR-
FROM P2
TO P2
FROM P1
TO P1



UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES	DR J. Hauser	PARATRONICS INC.
MAT'L		SCHEMATIC DIAGRAM TIMING MEMORY
FINISH	BREAK ALL SHARP EDGES	
	DO NOT SCALE DRAWING	SIZE D, DWG NO 127-0065-001, REV F, SHT 2 OF 4


SEE SHT 1
(TO SHT. 4)
(TO SHT 1)
PART OF P2
DATA COMPARATOR 4
DATA COMPARATOR 5
DATA COMPARATOR 6
DATA COMPARATOR 7
U12, CD4015
TA-
TT-
WD6
D6-
D6+
WD4
WD7
D7-
D7+
WD5
DV-
DV+
DS-
DS+
CT
DV6+1/8-
DS6+1/8-
DSELT+1/W-
TW4B0-
TW4B1-
TW6B0-
TW6B1
TW7B0-
TW7B1-
AW5B0-
AW5B1-
AW7B0-
AW7B1-
CLKSE1
SRDATA1-
SRDATA2-
ENDSE1
-5.2V
+5V
Q1 2N3905
Q2 2N3905
U110 CD4015
U21A 10117
U21B 10117
U21C 10117
U21D 10125
U22A 10131
U22B 10131
U22C 10125
U22D 10125
U23A 10131
U23B 10131
U23C 10131
U23D 10102
U24A 10102
U24B 10117
U24C 10102
U24D 10102
U25A 10117
U25B 10117
U25C 10102
U25D 10102
U26A 10102
U26B 10102
U26C 10102
U26D 10102
U27A 10125
U27B 10125
U27C 10125
U27D 10125
U28A 10130
U28B 10130
U28C 10130
U28D 10130
U29A 10158
U29B 10158
U29C 10158
U29D 10158
U11A 10117
U11B 10117
U11C 10117
U11D 10125
U12A 10117
U12B 10117
U12C 10117
U12D 10125
U13A 10102
U13B 10102
U13C 10102
U13D 10102
U14A 10102
U14B 10102
U14C 10102
U14D 10102
U15A 10130
U15B 10130
U15C 10130
U15D 10130
U16A 10158
U16B 10158
U16C 10158
U16D 10158
RP1 470
RP2 470
RP3 470
RP4 470
RP5 470
RP6 470
RP7 470
RP11 100
RP12 160
RP13 100
RP14 470
R1 1K
R2 3.3K
R3 1K
R4 1K
R5 1K
R6 22K
R7 1K
R8 1K
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DO NOT SCALE DRAWING
PARATRONICS INC.
SCHEMATIC DIAGRAM
TIMING MEMORY
DWG NO 127-0065-001
REV F
SIZE D
SCALE
SHT 3 OF 4



3 THIS SCHEMATIC TO BE USED WITH REVISION (5) "E" P.C.B. FABRICATION.
2 ALL RESISTOR VALUES ARE IN OHMS
1 ALL CAPACITOR VALUES ARE IN UF
NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR. Mullen 8/80	PARATRONICS INC.
MAT'L	CK K.E.F. 8/20/80	SCHEMATIC DIAGRAM TIMING MEMORY
FINISH	APPR.	DRWG. NO. 127-0065-001 REV. F
	DO NOT SCALE DRAWING	D SCALE SHT 4 OF 4

COUNTER-TIMER/
SIGNATURE ANALYZER

SECTION 11: COUNTER-TIMER/SIGNATURE ANALYZER

SECTION XI
COUNTER-TIMER/SIGNATURE ANALYZER

11.1 INTRODUCTION

The Counter-Timer/Signature Analyzer (C-T/SA) Board contains two independent functions, that share input circuitry and microprocessor interfacing. The Counter-Timer section is a full function frequency counter and interval timer based on the Intersil ICM7226B LSI device. The Signature Analyzer is based on a 16-stage tapped shift register with feedback. This generates a calculated number based on a serial bit stream received via the input probe. It emulates the Hewlett-Packard algorithm for signature analysis. Nicolet Paratronics is under license from Hewlett-Packard to produce the H-P compatible signature analyzer.

11.2 MICROPROCESSOR INTERFACE

Refer to the block diagram, Figure 11-1, and schematic #127-0099-001 (sheet 3). The C-T/SA Board occupies I/O space from 70_{HEX} to 73_{HEX}. The six most significant bits are decoded by U5 (74LS32) and U6 (74LS10). These output signals are used to gate U16, a 74LS138. The most significant select bit is connected to the S1 (pin 47) signal of the processor. This determines if the cycle is a read or write. Consequently, outputs Y4-Y7 are I/O read select lines, and

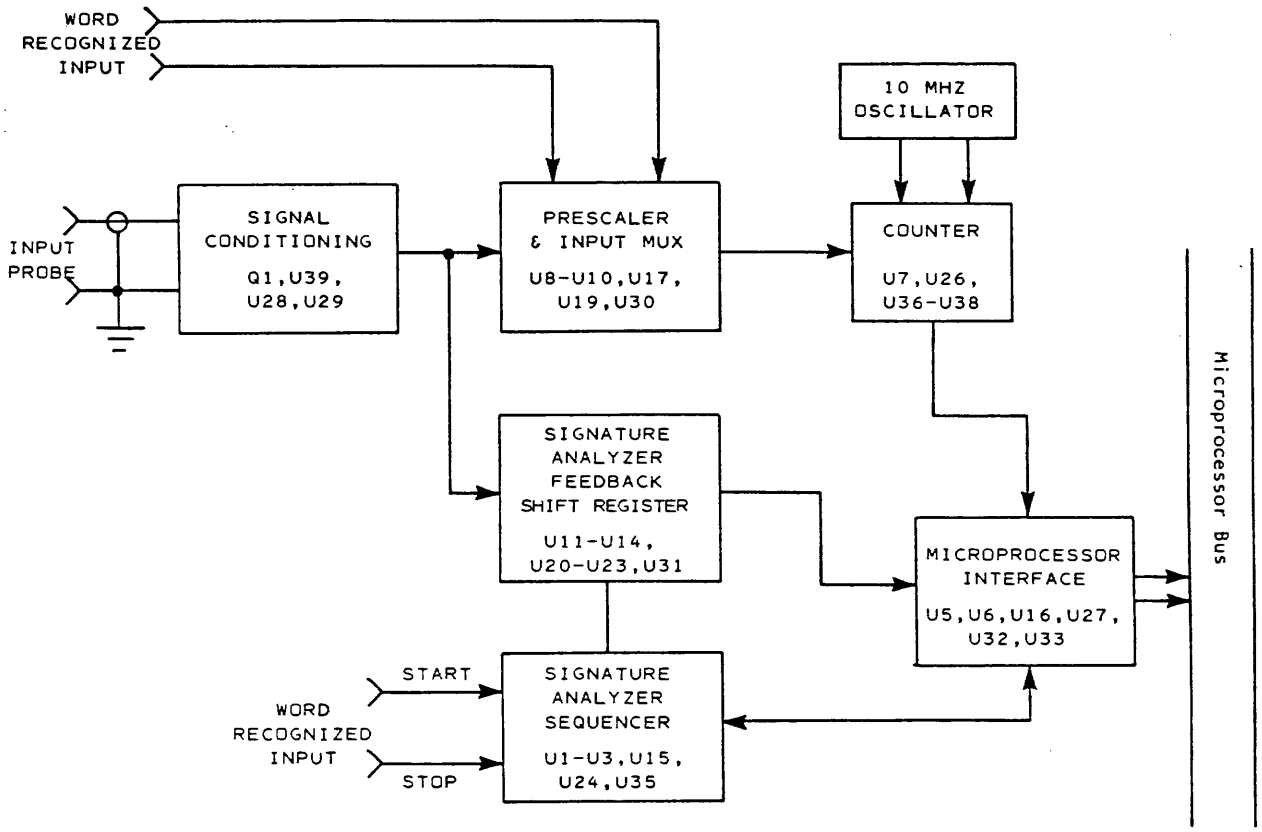


Figure 11-1 CTSA Block Diagram

Y0-Y2 are write select lines for addresses 70-73, respectively. These signals are used for the functions described by their names on the schematic.

11.3 INPUT CIRCUITRY

Refer to sheet 2. The DATA IN signal is applied to Q1A via the input r-c circuitry. The input impedance of this circuit is approximately 1 megohm shunted by 30 pF. Capacitor C36 provides high frequency compensation. Diodes CR1 and CR2 clip the input signal at +/- 2.5V. This protects FET Q1 and U39, the AM687 high speed comparator. Transistor Q1 is set up as a zero-offset source follower to provide d-c coupled current gain. U39 compares the input signal with a threshold voltage generated by the D/A converter U28 and buffer U29.

The ECL level outputs of U39 drive a delay line. The delay line output is used by the Signature Analyzer, and a pre-scaled and input MUX that is used by the Counter-Timer. The delay line is necessary to adjust the timing of the input data with the clock. The clock must go through additional circuitry within the rest of the Logic Analyzer.

Other inputs to the board are the Arm and Trigger signals. These are generated by the state analyzer, and become start/stop signals. The start/stop signals are used by the Signature Analyzer, and the Counter-Timer in interval mode. These are buffered by U10, an MC10116, and synchronized by part of U30, an MC10176.

The clock signals CT and CWE+ are buffered by U10 and U39 respectively. The selection between these two signals is made by half of U19. This is done by grounding of one of two S2 connector pins (28 or 29). The pin grounded indicates the use in a state or timing analyzer.

11.4 COUNTER-TIMER FUNCTIONAL DESCRIPTION

Refer to sheet 2. The Counter-Timer device receives the DATA A input via four-to-one multiplexer U9 and ECL-to-TTL converter U17. The MUX enables the processor to select either the probe input, the probe frequency divided-by-10 via U8, the start (ARM) signal, or the system clock. In addition, the stop (TRIG) signal is buffered by U17 for use in the interval mode.

Refer to sheet 3. The range and function inputs of the U7 (ICM7226B) are driven by U27 and U38, both 8-to-1 multiplexers. These select which of the digit strobe signals are sent to the range and function inputs. The select lines of both multiplexers are driven by U37. U37 is an octal latch that is set up as output port 70_{HEX}.

The Intersil ICM7226B is an LSI device that provides an eight digit output with the following characteristics: Frequency of input A to 10 MHz; period of A from 400 nanoseconds to 10 seconds; frequency ratio of A to B inputs; and interval from A input to B input.

The results of the measurement are presented at the BCD outputs sequentially. That is, one digit at a time, as indicated by the digit strobe outputs. These digit strobes are sent to a priority encoder, U26, that encodes these eight inputs into a 3-bit binary word. The four BCD outputs, the encoded strobe, and a valid strobe signal are buffered onto the processor bus by U36. This is initiated by an I/O read from address 72_{HEX}.

Half of U25 is used to detect an overflow status. This signal, and measurement-in-progress, are buffered by U34. This is the status port and responds to an I/O read from address 73_{HEX}. The Signature Analyzer status is also read from this port.

11.5 SIGNATURE ANALYZER FUNCTIONAL DESCRIPTION

Refer to sheet 1. The Signature Analyzer is based on shift registers U11 through U14 and XOR gate U31. A delay is generated by U30 to compensate for delay in the start and stop signal paths. Input signal SIGDATA is summed with a feedback signal from the 16-stage shift register. The feedback signal

is generated by summing the 7th, 9th, 12th and 16th stage outputs in U31. This yields a signature identical to that of Hewlett-Packard Signature Analyzer when used under the same conditions.

The outputs of the shift registers are converted from ECL to TTL levels by U20 through U23. The TTL level signals are then multiplexed onto the Processor Data Bus by U32 and U33. The signature is read by I/O reads from addresses 70_{HEX} and 71_{HEX}.

The operation of the shift register is controlled by the S1 and S2 inputs. These signals are the outputs of flip-flops U15B and U1A, respectively. These flip-flops, with flip-flop C (U15) and U2 and U3, form a sequencer that operates as shown in Figure 11-2. The state of the sequencer is converted to TTL by U35 and to tri-state by U34. U34 responds to an I/O read from address 73_{HEX}. The sequencer is reset by an I/O write to address 73_{HEX}.

11.6 SCHEMATICS, BOARD LAYOUTS AND PARTS LIST

The schematic diagram, board layout and parts list for the C-T/SA Board are contained at the end of this section.

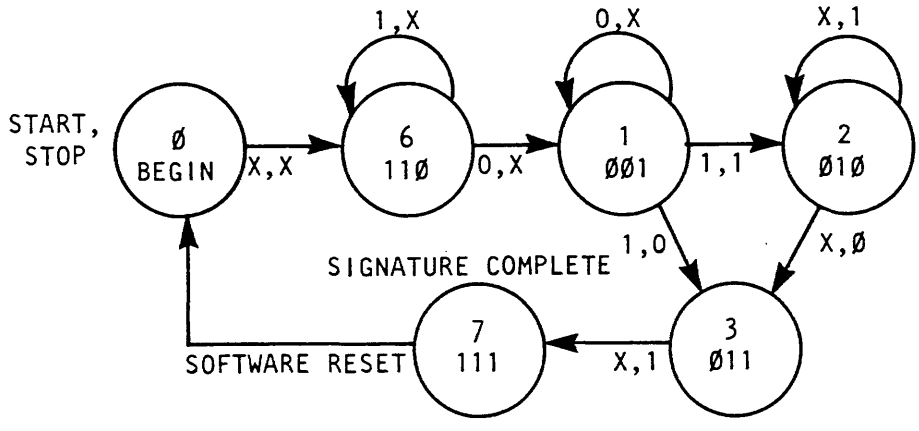


Figure 11-2 Signature Analyzer Sequencer State Diagram

PARENT ITEM 143-0099-0002 | CROSS REF ITEM | DESCRIPTION CT/SA PC ASSY STATE VERSION ENGR DRAW ECO 631 REV E | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 01 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	112-0113-0001	OP AMP LM747C U29		1.000	EA	4C				1/12/81	
	05	113-0003-0000	I.C. 74LS00 U25		1.000	EA	4C				1/12/81	
	04	113-0003-0010	I.C. 74LS10 U6		1.000	EA	4C				1/12/81	
	05	113-0003-0032	I.C. 74LS32 U5		1.000	EA	4C					
	06	113-0003-0138	I.C. 74LS138 U16		1.000	EA	4C				1/12/81	
	02	113-0003-0148	I.C. 74LS148 U26		1.000	EA	4C				1/12/81	
	04	113-0003-0151	I.C. 74LS151 U27 U36		2.000	EA	4C				1/12/81	
	05	113-0003-0244	I.C. 74LS244 U35		1.000	EA	4C				1/12/81	
	06	113-0003-0257	I.C. 74LS257 U32 U33		2.000	EA	4C				1/12/81	
	03	113-0003-0367	I.C. 74LS367 U34		1.000	EA	4C				1/12/81	
	05	113-0003-0374	I.C. 74LS374 U37		1.000	EA	4C				1/12/81	
	04	113-0043-0001	I.C. AM6060 U23		1.000	EA	4C				1/12/81	
	02	113-0046-0004	DELAY LINE 100NS, TYPE 5 U18		1.000	EA	4C				1/12/81	
	05	113-0046-0061	I.C. AM687 U39		1.000	EA	4C				1/12/81	
	02	113-0067-0061	I.C. 72268 INTERSIL U7		1.000	EA	4C				1/12/81	
	03	113-0200-0103	I.C. MC10103 U2		1.000	EA	4C				1/12/81	
	03	113-0200-0104	I.C. MC10104 U3		1.000	EA	4C				1/12/81	
	02	113-0200-0113	I.C. MC10113 U31		1.000	EA	4C				1/12/81	
	05	113-0200-0116	I.C. MC10116 U13		1.000	EA	4C				1/12/81	
	04	113-0200-0117	I.C. MC10117 U19		1.000	EA	4C				1/12/81	
	05	113-0200-0124	I.C. MC10124 U4		1.000	EA	4C				1/12/81	

PARENT ITEM 143-0099-0002 | CROSS REF ITEM | DESCRIPTION CT/SA PC ASSY STATE VERSION ENGR DRAW ECO 631 REV E | BATCH QTY 1 EFFEC 12/08/82 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 01 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEC	LT ADJ	EFFECTIVE DATES FROM	TO
	05	113-0200-0125	I.C. MC10125 U17 U20 U21 U22 U23 U35		6.000	EA	4C				1/12/81	
	02	113-0200-0135	I.C. MC10135 U1 U15		2.000	EA	4C				1/12/81	
	03	113-0200-0138	I.C. MC10138 U8		1.000	EA	4C				1/12/81	
	02	113-0200-0141	I.C. MC10141 U11 U12 U13 U14		4.000	EA	4C				1/12/81	
	02	113-0200-0161	I.C. MC10161 U24		1.000	EA	4C				1/12/81	
	02	113-0200-0164	I.C. MC10164 U9		1.000	EA	4C				1/12/81	
	03	113-0200-0176	I.C. MC10176 U36		1.000	EA	4C				1/12/81	
	02	143-0099-0090	CT/SA PC ASSY OUTSIDE	ECO 612 REV G	1.000	EA	1C				1/12/81	

PARENT ITEM 143-0099-0090 | CROSS REF ITEM | DESCRIPTION CT/SA PC ASSY OUTSIDE ENGR DRAW ECO 612 REV G | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

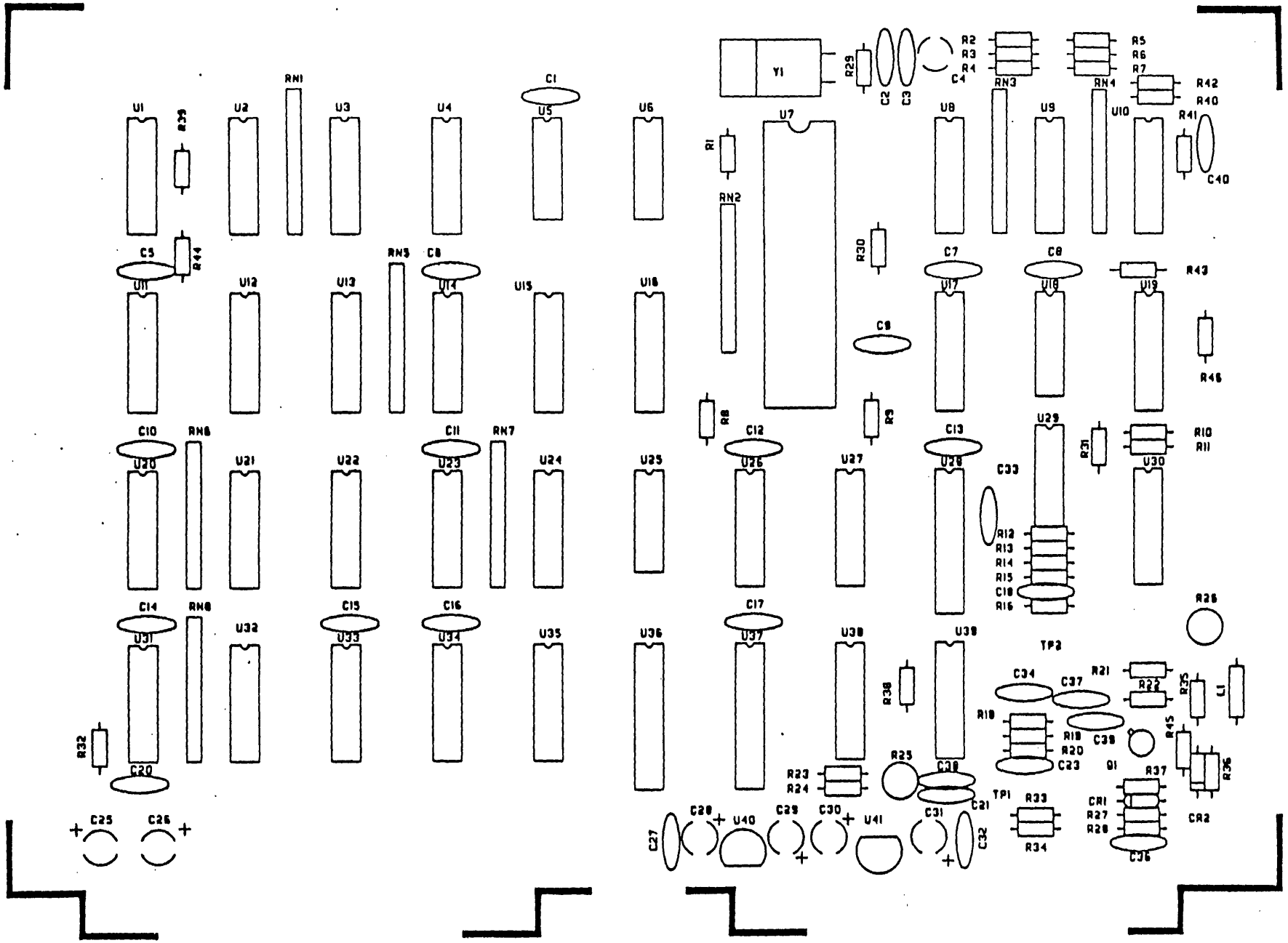
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	110-0003-0094	20K OHM 1/4W 1% MF RES R14 R15		2.000	EA	4C				5/01/80	
	04	110-0003-0135	1 MEG OHM 1/4W 1% MF RES R28		1.000	EA	4C				5/01/80	
	03	110-0003-0356	1.27K 1/4W 1% MF CF RES R12 R13		2.000	EA	4C				6/29/82	
	07	110-0005-0025	27 OHM 1/4W 5% CF RES R16		1.000	EA	4C					
	06	110-0005-0031	47 OHM 1/4W 5% CF RES R21		1.000	EA	4C				5/01/80	
	06	110-0005-0037	82 OHM 1/4W 5% CF RES R22 R24 R45 R47		4.000	EA	4C				6/29/82	
	06	110-0005-0039	100 OHM 1/4W 5% CF RES R18 R35 R36 R37 R42 R43 R46		7.000	EA	4C				6/29/82	
	05	110-0005-0044	160 OHM 1/4W 5% CF RES R41 R40		2.000	EA	4C				7/07/81	
	06	110-0005-0045	180 OHM 1/4W 5% CF RES R11		1.000	EA	4C				5/01/80	
	07	110-0005-0047	220 OHM 1/4W 5% CF RES R39		1.000	EA	4C				1/12/81	
	05	110-0005-0049	270 OHM 1/4W 5% CF RES R10		1.000	EA	4C				5/01/80	
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R44		1.000	EA	4C				1/12/81	
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R23 R30 R31 R32 R38		5.000	EA	4C					
	06	110-0005-0059	680 OHM 1/4W 5% CF RES R2 R5		2.000	EA	4C				11/26/80	
	06	110-0005-0063	1K OHM 1/4W 5% CF RES R34		1.000	EA	4C					
	05	110-0005-0067	1.5K OHM 1/4W 5% CF RES R20 R3 R4 R6 R7		5.000	EA	4C				5/01/80	
	06	110-0005-0075	3.3K OHM 1/4W 5% CF RES R1 R19 R33 R9		4.000	EA	4C				5/01/80	
	05	110-0005-0087	10K OHM 1/4W 5% CF RES R8		1.000	EA	4C				5/01/80	
	05	110-0005-0127	470K OHM 1/4W 5% CF RES R27		1.000	EA	4C				5/01/80	
	03	110-0005-0167	22 MEG OHM 1/4W 5% CF MF RES R29		1.000	EA	4C				5/01/80	
	06	110-0205-0001	POT, 50 OHM, TRIM 3329H-50 R25 R26		2.000	EA	4C				5/01/80	

PARENT ITEM 143-0099-0090 | CROSS REF ITEM | DESCRIPTION CT/SA PC ASSY OUTSIDE ENGR DRAW ECO 612 REV G | BATCH QTY 1 | EFFEC 12/08/82 | ITEM TYPE 1 | UNIT MEAS EA | LOW LEVEL 02 | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FRCM	TC
	03	110-0316-0001	RN 470 OHM X9, 10 PIN SIP RP1 RP3 RP4 RP5 RP6 RP7 RP8		7.000	EA	4C				5/01/80	
	04	110-0319-0001	RN 1K OHM X9, 10 PIN SIP RP2		1.000	EA	4C					
	06	111-0004-0066	.01 UF 25V CD CAP C1 C10 C11 C12 C13 C14 C15 C16 C17 C19 C20 C21 C23 C27 C32 C33 C34 C37 C5 C6 C7 C8 C9		23.000	EA	4C				11/24/81	
	06	111-0006-0050	.001 UF 50V CD CAP C38 C39		2.000	EA	4C				6/28/82	
	06	111-0012-0006	5 PF 1KV CD CAP C3 C40		2.000	EA	4C				6/28/82	
	04	111-0012-0021	39 PF 1KV CD CAP C2		1.000	EA	4C				5/01/80	
	06	111-0012-0030	100 PF 1KV CD CAP C36		1.000	EA	4C				11/26/80	
	06	111-0056-0107	33 UF 6V TANT DROP CAP C25 C26		2.000	EA	4C					
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C28 C31		2.000	EA	4C				11/26/80	
	05	111-0209-0096	10 UF 25V ELECT RADIAL CAP C29 C30		2.000	EA	4C				6/28/82	
	03	111-0906-0004	TRIM CAP 5-30PF JOANSON 9383 C4		1.000	EA	4C				2/01/82	
	05	112-0114-0001	TRANS U440 E420 E421 SILICON Q1		1.000	EA	4C				5/01/80	
	05	112-0115-0001	V.REG +12V LM78L12ACZ 78L12CP U40		1.000	EA	4C					
	05	112-0116-0001	V.REG -12V 79L12CPMOT LM320LZN U41		1.000	EA	4C					
	03	112-0215-0001	DIODE IN916 CR1 CR2		2.000	EA	4C					
	03	112-0312-0001	CRYSTAL 10 MHZ CRYSTEX Y1		1.000	EA	4C				5/01/80	
	06	115-0003-0001	SOCKET 14PIN U25 U29 U5 U6		4.000	EA	4C				5/01/80	
	06	115-0005-0001	SOCKET 16PIN U1 U2 U3 U4 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U19 U20 U21 U22 U23 U24 U26 U27 U30 U31 U32 U33 U34 U35 U38 U39		30.000	EA	4C				5/01/80	

PARENT ITEM	CROSS REF ITEM	DESCRIPTION CT/SA PC ASSY OUTSIDE	BATCH QTY 1	ITEM TYPE 1	LOW LEVEL 02
143-0099-0090		ENGR DRAW ECO 612 REV G	EFFEC 12/08/82	UNIT MEAS EA	PLANNER

REF NBR	LL CO	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	115-0009-0001	SOCKET 20PIN U23 U36 U37		3.000	EA	4C				5/01/80	
	06	115-0013-0001	SOCKET 40PIN U7		1.000	EA	4C				5/01/80	
	06	117-0030-0001	TERMINAL 120-1032-04 CAMBION TP1 TP2		2.000	EA	4C					
	03	126-0099-0001	COUNTER/TIMER/SA PC FAB	ECO 631 REV D	1.000	EA	4C				5/01/80	


U1
U2
RN1
U3
U4
C1
U5
U6
Y1
R29
C2
C3
R2
R3
R4
C4
RN3
R5
R6
R7
RN4
R42
R40
U10
R41
C40
U7
U8
U9
R1
RN2
R30
C7
C8
R43
C5
R44
RN5
C6
U11
U12
U13
U14
U15
U16
U17
U18
U19
C9
R46
R8
R9
C10
RN6
C11
RN7
C12
C13
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R11
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U22
U23
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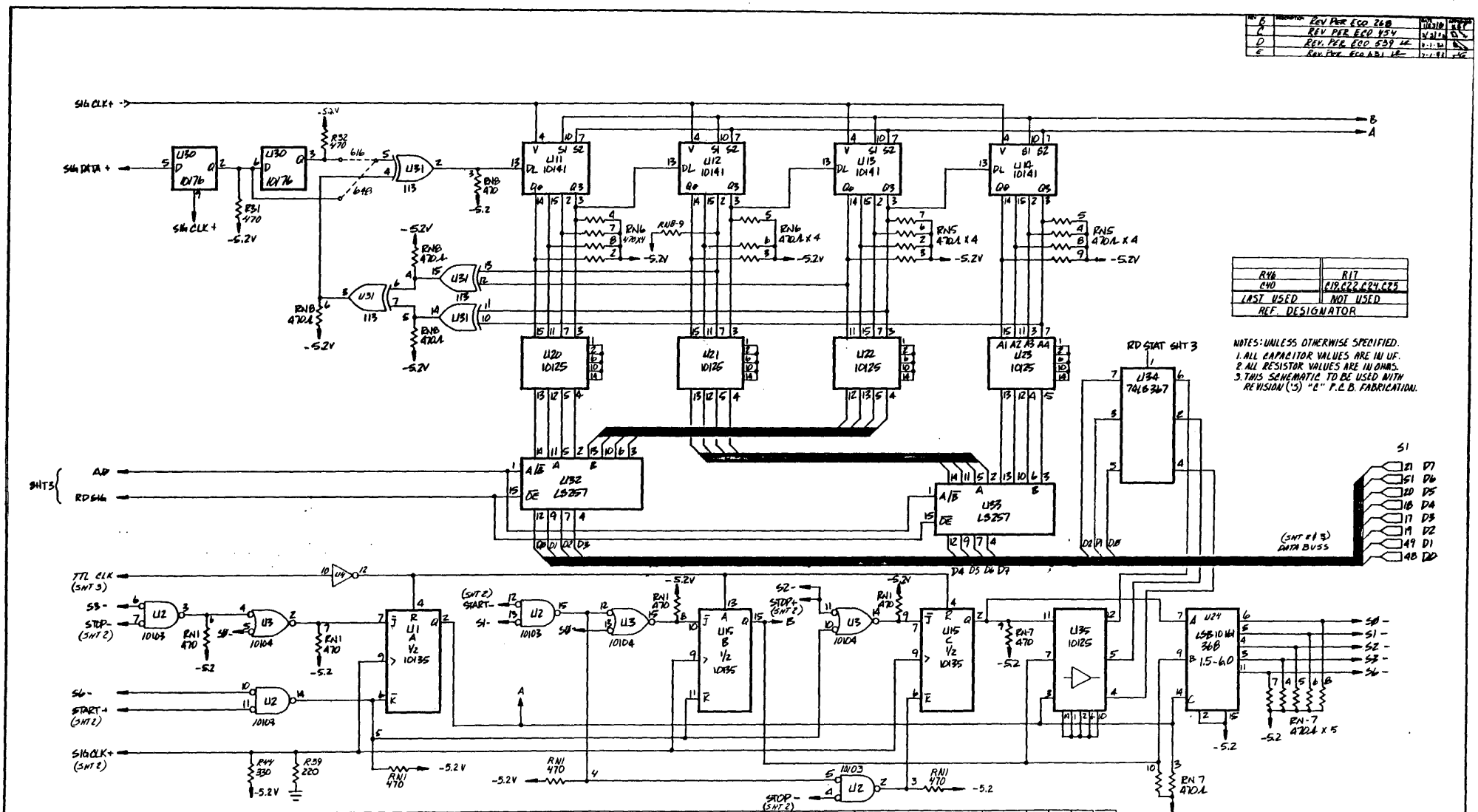
U28
U30
C33
R12
R13
R14
R15
C18
R16
R26
C14
RN8
C15
C16
C17
U31
U32
U33
U34
U35
U36
U37
U38
U39
TP2
R38
C34
C37
R21
R22
R35
L1
R32
C20
R18
R19
R20
C23
C38
R45
R25
C22
Q1
R37
R36
R23
R24
TP1
R33
C21
CR1
R27
R28
CR2
C25
C26
C28
U40
C29
C30
U41
C31
C27
C32
R34
C36



R46	R17
C40	C19, C22, C24, C25
LAST USED	NOT USED
REF. DESIGNATOR	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITOR VALUES ARE IN UF.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. THIS SCHEMATIC TO BE USED WITH REVISION ('5') "E" P.C.B. FABRICATION.

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 268	10/2/78	RET
C	REV PER ECO 454	3/21/79	DV
D	REV. PER ECO 539 LE	9-1-81	LE
E	REV PER ECO 681 LE	2-1-82	LE

POWER AND GROUND LOCATER CHART

REF. DES.	TYPE	GND	+5V	-5V	#PINS
U25	74LS00	7	14		14
U6	74LS10	7	14		14
U5	74LS32	7	14		14
U16	74LS138	8	16		16
U26	74LS148	8	16		16
U27, U38	74LS151	8	16		16
U4	10164	1,16		8	16
U36	74LS244	10	20		20
U32, U33	74LS257	8	16		16
U34	74LS367	8	16		16
U37	74LS374	10	20		20
U18	LC02021008	7,14	—	—	14
U28	AM6080 RP1, RP3, RP4, RP5, RP6, RP7, RP8	10	20	17	20
	470Ω RP			1	10
U39	AN687	3,14	11	6	16
U7	7226B	12	25		40
U2	10103	1,16		8	16
U3	10104	1,16		8	16
U31	10113	1,16		8	16
U10	10116	1,16		8	16
U19	10117	1,16		8	16
RP2	1K RP		1		10
U29	LM747		9	4	14
U4	10124	16	9	8	16
U17, U20, U21, U22, U23, U35	10125	16	9	8	16
U1, U15	10135	1,16		8	16
U8	10138	1,16		8	16
U11, U12, U13, U14	10141	1,16		8	16
U24	10161	1,16		8	16
U30	10176	1,16		8	16

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L N/A

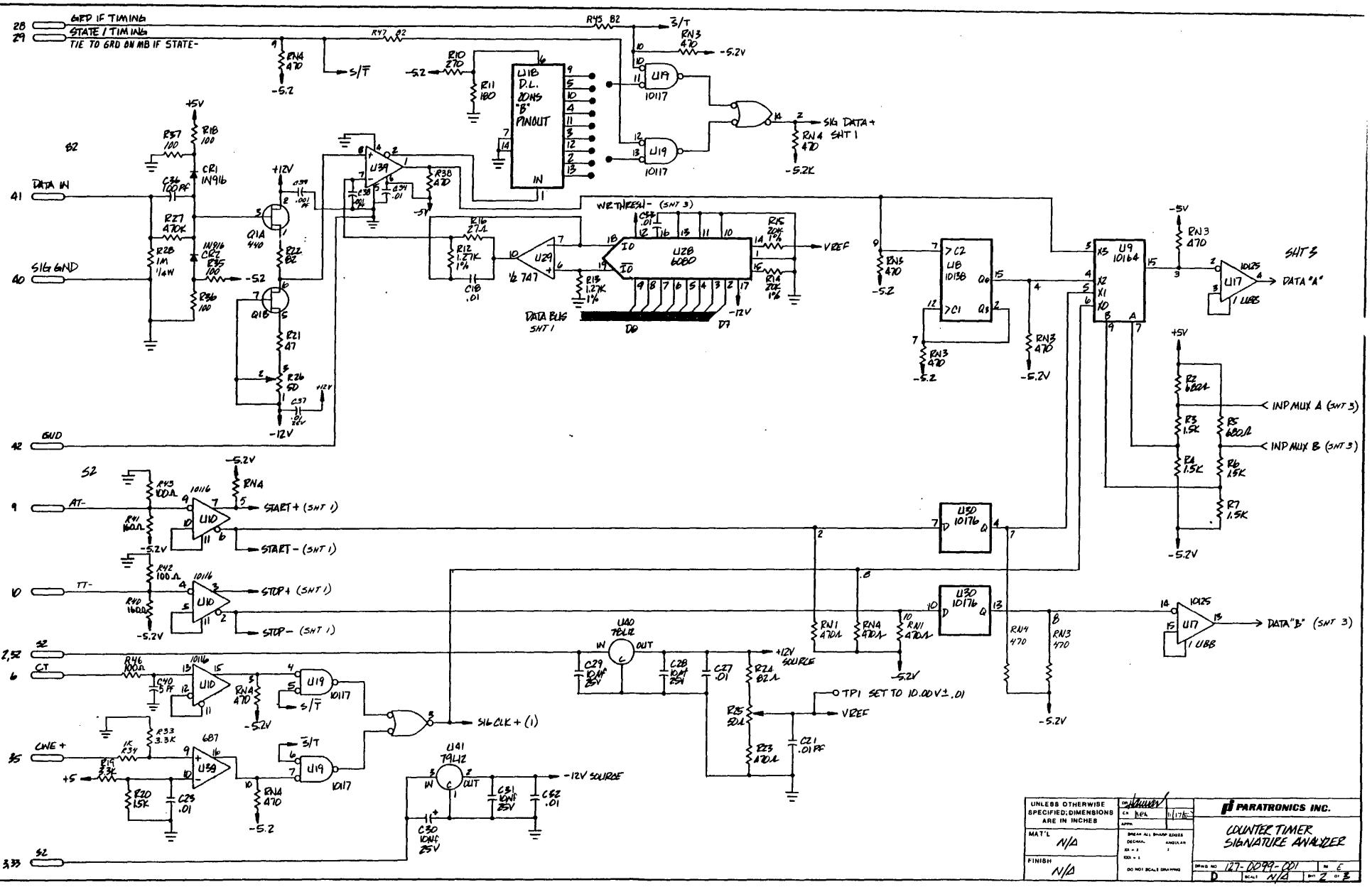
FINISH N/A

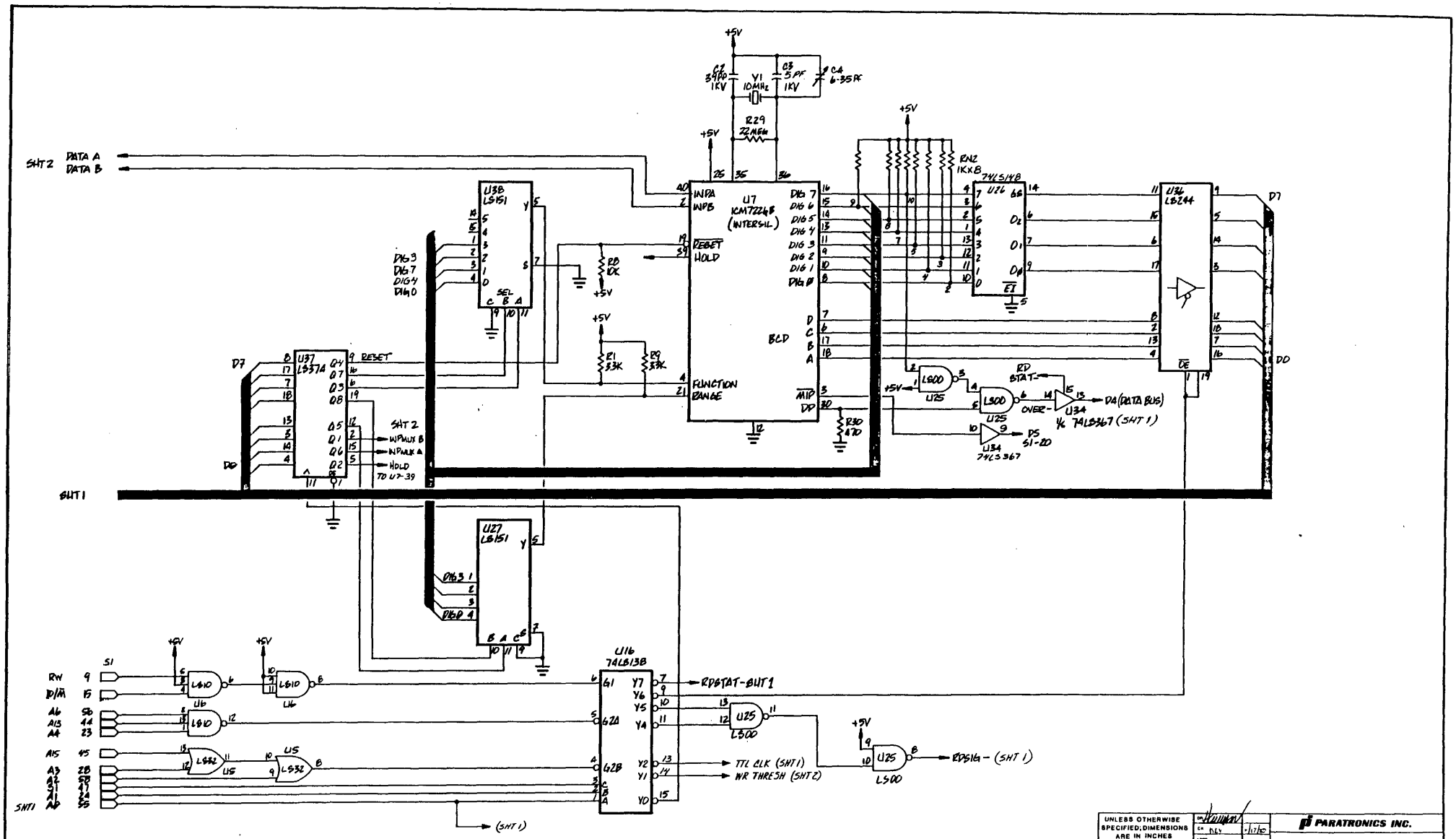
PARATRONICS INC.

COUNTER TIMER SIGNATURE ANALYZER

DWG NO 127-0099-001 REV E

SCALE N/A SHT 1 OF 3


GND IF TIMING
STATE / TIMING
TIE TO GRD ON MB IF STATE-
S/T
SIG DATA + SHT 1
DATA IN
SIG GND
GND
DATA BUS SHT 1
WR THRESH - (SHT 3)
VREF
DATA "A"
DATA "B" (SHT 3)
INP MUX A (SHT 3)
INP MUX B (SHT 3)
START + (SHT 1)
START - (SHT 1)
STOP + (SHT 1)
STOP - (SHT 1)
SIG CLK + (1)
-12V SOURCE
+12V SOURCE
TP1 SET TO 10.00V ± .01
COUNTER TIMER
SIGNATURE ANALYZER
PARATRONICS INC.



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR	PARATRONICS INC.
MAT'L N/A	CH N.L.Y. 1/17/90	COUNTER TIMER SIGNATURE ANALYZER
FINISH N/A	APPR	
BREAK ALL SHARP EDGES .XX ± .1 .XXX ± .1 DO NOT SCALE DRAWING		DRWG NO 127-0049-001 REV E
		D SCALE N/A SHT 5 OF 3

WAVEFORM BOARD

SECTION 12: WAVEFORM BOARD

SECTION XII
WAVEFORM BOARD

12.1 INTRODUCTION

The Waveform Board provides a high speed analog interface and special display hardware used to display the collected analog signal.

12.2 FUNCTIONAL DESCRIPTION

Refer to schematic #127-0072-001, the board layout and parts list at the end of this section. Tables of connector pins versus signal names for all Motherboard connectors are provided in SIGNAL AND INTERCONNECTION TABLES. An alphabetical list of all interboard signals is provided. The GLOSSARY section offers explanations for acronyms or terms that may be unfamiliar.

The input signal is received via edge connector pin S2-29 that is connected to the rear panel BNC connector. Relay K1 selects d-c (closed) or a-c input coupling. Relays K2-K5 and the associated components form a precision attenuator network with division ratios of 1, 10, 100 and 1000. Relay K6 provides a ground reference when closed.

FET Q1 is configured as a zero-offset source follower and is used for buffering and impedance transformation. This signal is applied to a low-pass filter consisting of C16, C17 and L1. This filter limits the bandwidth of the signal to be presented to the A/D converter. U13, an SG592 video amplifier, in conjunction with relays K7 and K8, forms a programmable-gain amplifier. U9, an LH0024 operational amplifier (op-amp), and transistor Q2 provide high speed, low output-impedance buffering. This is used to drive the A/D converters and the triggering circuit. The offset, or vertical position voltage is added at the input of U9. The offset voltage is generated under software by D/A converter U11 and the associated buffer.

The triggering circuit consists of an AM687 high speed comparator, U8. This circuit compares the input signal to a reference generated by D/A U10 under software control. The true or complement outputs of the AM687 are selected by U7 to determine the slope of the triggering signal. This output is sent to trigger latch U20, an MC10131 dual D flip-flop. The other half of the MC10131 is used to hold the trigger latch reset until the clock starts.

U6 is wired as output port D5 (HEX). This allows control of the circuit via relays K1-K8 and the trigger polarity select line.

The A/D converter is two multiplexed TRW TDC1014Js. The A/D converter output is sent to the Timing Memory Board for storage.

After collection in the Timing Memory, the data is sent to a 256-word x 8-bit display memory in the display section of the Waveform board. The display memory occupies address locations 2E00H through 2EFFH. No provision is made for reading this memory. Operation of the display section is described below.

The CRT screen is mapped into the display memory as 256 vertical columns corresponding to 256 X values. Each X value is assigned a memory location. The 8-bit data value in each memory location determines the Y value of the video dot for that X value. The resulting string of 256 dots constitutes the waveform and is sent to the Video Display Board for display on the CRT.

It is possible that a dot in the string will be displaced up or down from the preceding dot more than one raster scan line. If this occurs, the circuit will fill in the gap. This is done by adding a string of vertical dots to the scan line in the new column above or below the preceding dot. The number of dots added may range from one to

many, as required. This preserves the visual continuity of the display.

Note that the line must be allowed to begin and end inside the screen boundaries. Thus, a scale and annotation may be included in the display. The gap-fill feature is inhibited for Y values of 0FFH. The Control Program places an FF-value dot at the beginning and end of the data string. No vertical line is drawn to or from the FF-value dot, and the dot itself is not displayed.

The display may be inhibited by writing a 00 or enabled by writing a 01 to port 0D4H. The display must be inhibited while the memory is being altered.

12.3 SCHEMATIC, BOARD LAYOUT AND PARTS LIST

The schematic diagram, board layout and parts list for the Waveform Board are contained on the following pages.

PARENT ITEM 143-0072-0090 | CROSS REF ITEM | DESCRIPTION WAVEFORM PC ASSY. ENGR DRAW ECO 727 REV T | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0039	100 OHM 1/4W 5% CF RES R45 R55		2.000	EA	4C				1/29/80	
	05	110-0005-0049	270 OHM 1/4W 5% CF RES R217 R59		2.000	EA	4C				8/30/80	
	07	110-0005-0051	330 OHM 1/4W 5% CF RES R16 R50		1.000	EA	4C					
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R13 R18 R56 R57 R60 R70		6.000	EA	4C				1/17/80	
	06	110-0005-0059	680 OHM 1/4W 5% CF RES R25 R39 R42		3.000	EA	4C					
	06	110-0005-0063	1K OHM 1/4W 5% CF RES R1 R27		2.000	EA	4C					
	05	110-0005-0067	1.5K OHM 1/4W 5% CF RES R40 R41 R43 R44		4.000	EA	4C					
	07	110-0005-0079	4.7K OHM 1/4W 5% CF RES R58		1.000	EA	4C					
	06	110-0005-0087	10K OHM 1/4W 5% CF RES R219		1.000	EA	4C					
	05	110-0005-0127	470K OHM 1/4W 5% CF RES R8		1.000	EA	4C					
	04	110-0007-0039	100 OHM 1/2W 5% CF RES R29		1.000	EA	4C				1/17/80	
	06	110-0205-0001	POT, 50 OHM, TRIM 3329H-50 R12 R49		2.000	EA	4C				1/17/80	
	04	110-0205-0004	POT, 500 OHM 3329H-1-501 BOURN R17 R19		2.000	EA	4C				1/17/80	
	05	110-0306-0001	RN 470 OHM X7 8 PIN SIP RP1 RP3		2.000	EA	4C				1/29/80	
	05	110-0314-0001	RN 4.7K OHM X9 10 PIN SIP RP2		1.000	EA	4C				1/29/80	
	06	111-0004-0056	.01 UF 25V CO CAP C47 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C14 C15 C25 C26 C27 C28 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C202		57.000	EA	4C					
	05	111-0004-0074	.1 UF 25V CO CAP C20		1.000	EA	4C					
	06	111-0006-0050	.001 UF 50V CO CAP C17 C213 C214		3.000	EA	4C				8/30/80	

PARENT ITEM 143-0072-0090 | CROSS REF ITEM | DESCRIPTION WAVEFORM PC ASSY. ENGR DRAW ECO 727 REV T | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NEP	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	111-0008-0064	.0068 MF 100V CD CAP C11		1.000	EA	4C				1/17/80	
	04	111-0012-0013	15 PF 1KV CD CAP C24		1.000	EA	4C				1/17/80	
	04	111-0012-0020	33 PF 1KV CD CAP C17 C19 C21 C5		4.000	EA	4C				1/17/80	
	05	111-0012-0022	47 PF 1KV CD CAP C16		1.000	EA	4C				10/12/82	
	06	111-0012-0030	100 PF 1KV CD CAP C215		1.000	EA	4C					
	04	111-0012-0045	560 PF 1KV CD CAP C8		1.000	EA	4C				1/17/80	
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C103 C104 C201 C23 C29 C30 C81 C82 C83 C86		10.000	EA	4C				3/30/82	
	05	111-0209-0096	10 UF 25V ELECT RADIAL CAP C84 C85		2.000	EA	4C				3/30/82	
	04	111-0417-0068	.22 MF 200V MYLAR CAP C1		1.000	EA	4C				1/17/80	
	04	111-0800-0001	TRIM CAP 2.5-10PF JOHN 9611 C3 C6 C9		3.000	EA	4C				11/30/81	
	04	111-0800-0002	TRIM CAP 5-35PF JOANSON 9513 C10 C4 C7		3.000	EA	4C				1/17/80	
	04	112-0070-0001	VOLTAGE REG. L1337MP U39	ECO 550 REV A	1.000	EA	4C				4/10/81	
	06	112-0100-0001	TRANSISTOR 2N3904 Q2		1.000	EA	4C				1/17/80	
	05	112-0114-0001	TRANS U440 E420 E421 SILICON Q1		1.000	EA	4C				1/17/80	
	07	112-0204-0001	DIODE 1N3600 1N4148 4149 4150 CR10 CR11 CR12 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9		11.000	EA	4C				1/17/80	
	04	112-0214-0001	DIODE 1N702 VR1		1.000	EA	4C				1/29/80	
	04	112-0307-0001	REED RELAY 191TE2C1-56 SIGMA K2 K5 K3 K4		4.000	EA	4C				1/17/80	
	04	112-0308-0001	REED RELAY 191TE1A1-56 SIGMA K1 K6 K7 K8		4.000	EA	4C				1/17/80	
	06	115-0003-0001	SOCKET 14PIN U12 U13 U14 U19 U22 U23 U26 U3 U30 U4 U5		11.000	EA	4C				1/17/80	

PARENT ITEM 143-0072-0090 | CROSS REF ITEM | DESCRIPTION WAVEFORM PC ASSY. ENGR DRAW ECO 727 REV T | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/09/82 | UNIT MEAS EA | PLANNER

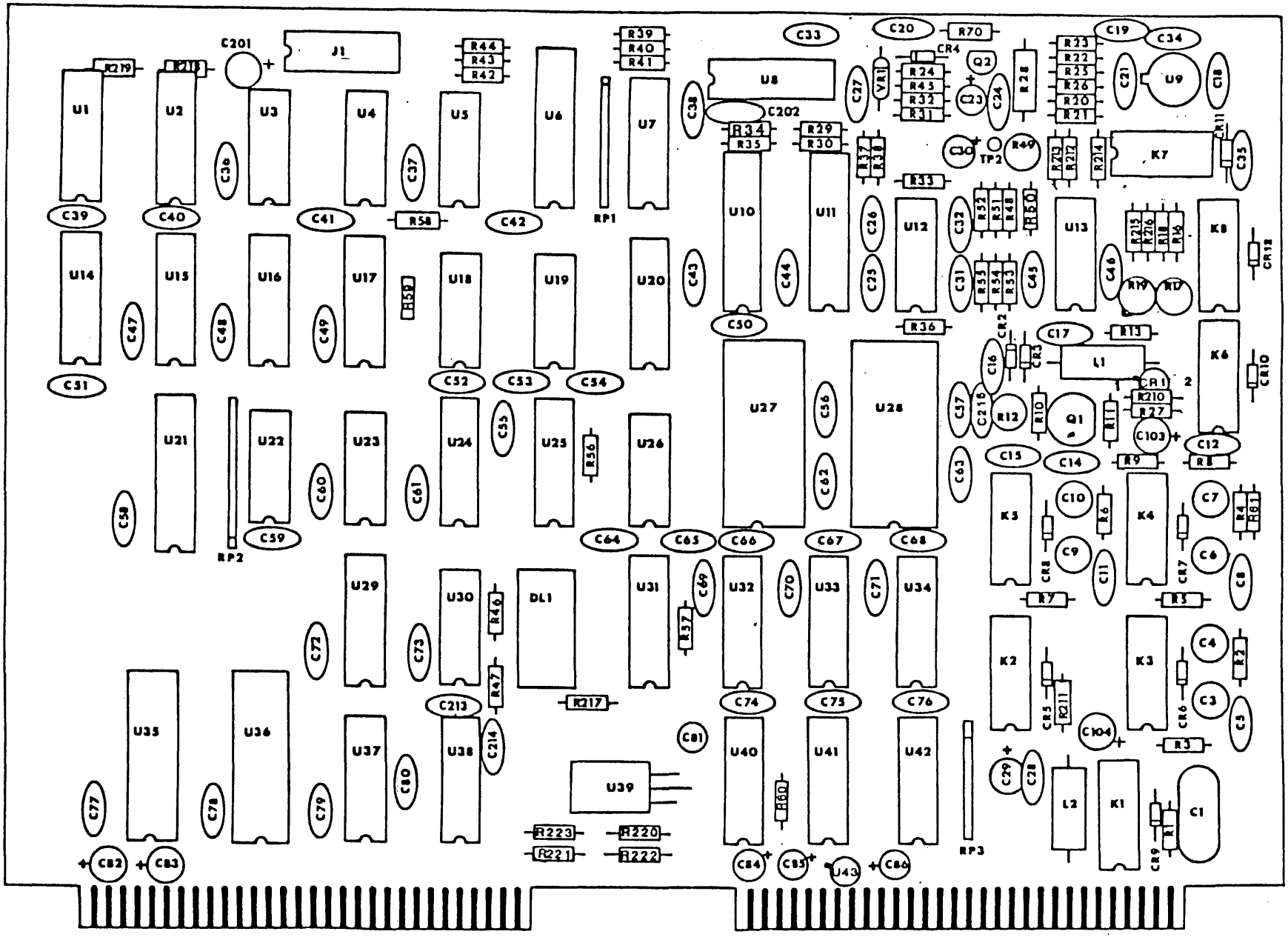
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	04	110-0003-0063	1K OHM 1/4W 1% MF RES R7		1.000	EA	4C				1/17/80	
	04	110-0003-0066	1.3K OHM 1/4W 1% MF RES R22 R25		2.000	EA	4C				1/17/80	
	04	110-0003-0087	10K OHM 1/4W 1% MF RES R29 R30 R34 R35 R5 R52		6.000	EA	4C				1/17/80	
	04	110-0003-0094	20K OHM 1/4W 1% MF RES R54		1.000	EA	4C				1/17/80	
	04	110-0003-0111	100K OHM 1/4W 1% MF RES R51 R53		2.000	EA	4C				10/26/82	
	04	110-0003-0135	1 MEG OHM 1/4W 1% MF RES R6 R9		2.000	EA	4C				10/26/82	
	04	110-0003-0142	2 MEG OHM 1/4W 1% MF RES R61		1.000	EA	4C				1/17/80	
	04	110-0003-0289	237 OHM 1/4W 1% MF RES R220 R221		2.000	EA	4C				6/29/82	
	04	110-0003-0318	475 OHM 1/4W 1% MF RES R20 R21 R212 R213 R214		5.000	EA	4C				6/29/82	
	04	110-0003-0331	649 OHM 1/4W 1% CF RES R31 R33 R36 R37		4.000	EA	4C				6/29/82	
	04	110-0003-0344	909 OHM 1/4W 1% MF RES R222 R223		2.000	EA	4C				6/29/82	
	04	110-0003-0531	113K 1/4W 1% MF RES R3		1.000	EA	4C				6/29/82	
	04	110-0003-0614	909K 1/4W 1% RES R2		1.000	EA	4C				6/29/82	
	04	110-0003-0642	1.96 MEG 1/4W 1% MF RES R4		1.000	EA	4C				6/29/82	
	07	110-0005-0025	27 OHM 1/4W 5% CF RES R11 R210 R211 R32 R39		5.000	EA	4C				1/17/80	
	04	110-0005-0030	43 OHM 1/4W 5% CF RES R48		1.000	EA	4C					
	06	110-0005-0031	47 OHM 1/4W 5% CF RES R23		1.000	EA	4C				8/30/80	
	04	110-0005-0032	51 OHM 1/4W 5% CF RES R10		1.000	EA	4C				1/17/80	
	04	110-0005-0033	56 OHM 1/4W 5% CF RES R24		1.000	EA	4C				1/17/80	
	06	110-0005-0035	68 OHM 1/4W 5% CF RES R219		1.000	EA	4C					
	06	110-0005-0037	82 OHM 1/4W 5% CF RES R215 R216		2.000	EA	4C				1/17/80	

PARENT ITEM 143-0072-0090 | CROSS REF ITEM | DESCRIPTION WAVEFORM PC ASSY. ENGR DRAW ECO 727 REV T | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 03 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	115-0005-0001	SOCKET 16PIN U1 U14 U15 U16 U17 U2 U20 U24 U25 U29 U31 U32 U33 U34 U37 U38 U40 U42 U7 U8		20.000	EA	4C				7/08/81	
	06	115-0009-0001	SOCKET 20PIN U10 U11 U21 U6		4.000	EA	4C				1/17/80	
	06	115-0010-0001	SOCKET 22PIN U35 U36		2.000	EA	4C				1/17/80	
	05	115-0011-0001	SOCKET 24PIN U27 U28		2.000	EA	4C				1/17/80	
	04	115-0017-0001	16 PIN SOCKET 516-AG11D AUG J1		1.000	EA	4C					
	06	117-0030-0001	TERMINAL 120-1032-04 CAMBION TP1 TP2 TP3		3.000	EA	4C				1/17/80	
	04	121-0027-0001	INDUCTOR 1 MH DALE IMS-5 L2		1.000	EA	4C				1/17/80	
	04	121-0027-0002	INDUCTOR 3 UH DALE IM-2 L1		1.000	EA	4C					
	04	126-0072-0001	540 WAVEFORM PC FAB	ECO 637 REV F	1.000	EA	4C				1/17/90	

PARENT ITEM 143-0072-0003 | CROSS REF ITEM | DESCRIPTION M764 WAVEFORM ASSY. ENGR DRAW ECO 538 REV A | BATCH QTY 1 EFFEC 1/04/83 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 01 PLANNER

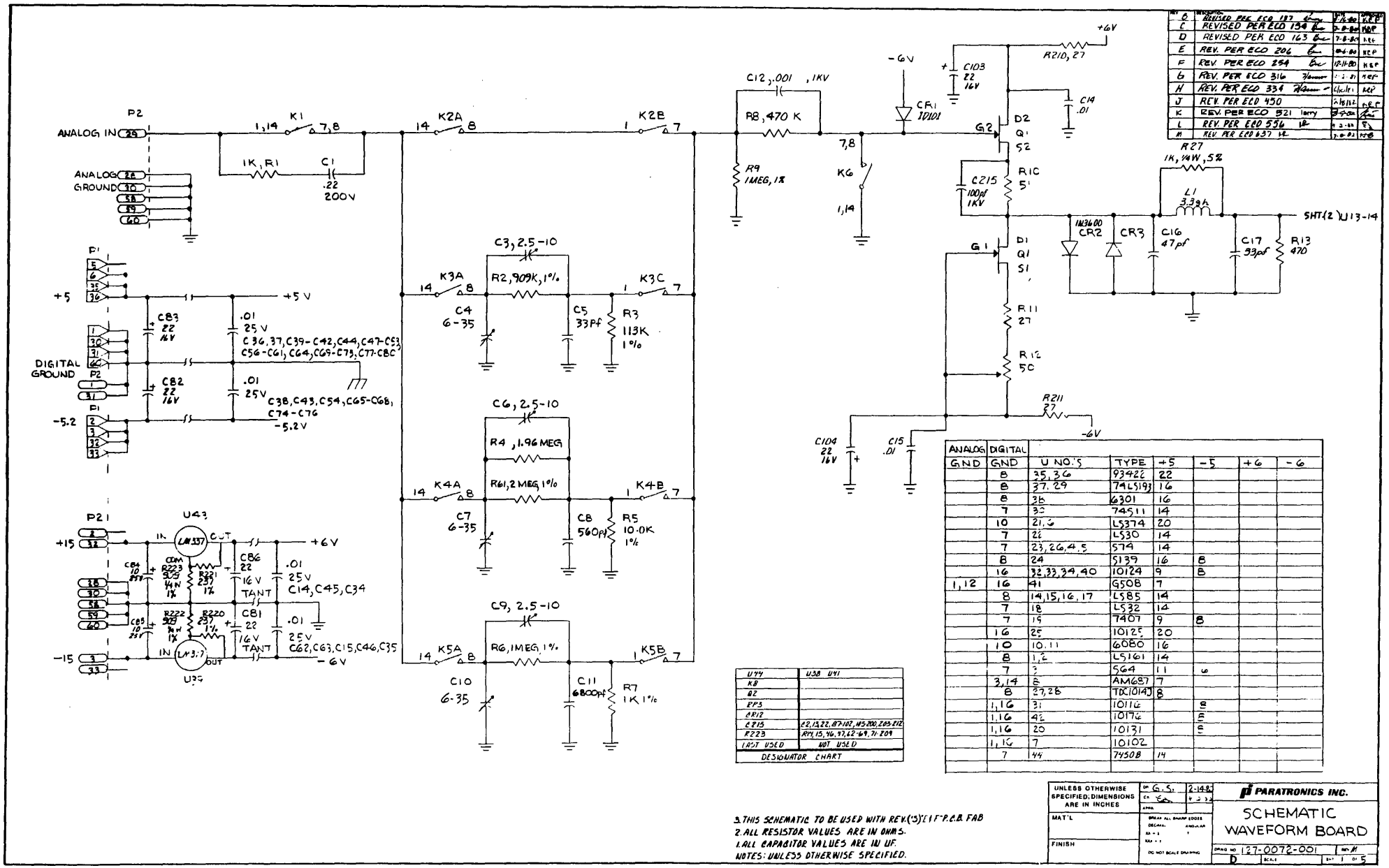
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TC
	02	113-4010-0001	PROM,6301-1 M764 WAVEFORM,U38	ECO 520 REV A	1.000	EA	IC				3/25/82	
	02	143-0072-0001	BASIC WAVEFORM ASSY.	ECO 637 REV C	1.000	EA	IC				3/25/82	



Waveform Bd.

NICOLET PARATRONICS

126-0072-0201 Rev. F



REV	DESCRIPTION	DATE	APPROVED
C	REVISED PER ECO 134	7-8-80	MCP
D	REVISED PER ECO 163	7-8-80	MCP
E	REV. PER ECO 206	8-6-80	MCP
F	REV. PER ECO 254	12-11-80	MCP
G	REV. PER ECO 316	2-2-81	MCP
H	REV. PER ECO 334	4/16/81	MCP
J	REV. PER ECO 450	2/15/82	MCP
K	REV. PER ECO 521	7-7-82	
L	REV. PER ECO 556	1-3-83	
M	REV. PER ECO 637	7-6-83	

ANALOG GND	DIGITAL GND	U NO.'S	TYPE	+5	-5	+6	-6
	8	35, 36	93422	22			
	8	37, 29	74LS193	16			
	8	38	6301	16			
	7	30	74S11	14			
	10	21, 6	LS374	20			
	7	22	LS30	14			
	7	23, 26, 4, 5	S74	14			
	8	24	S139	16	8		
	16	32, 33, 34, 40	10124	9	8		
1, 12	16	41	G508	7			
	8	14, 15, 16, 17	LS85	14			
	7	18	LS32	14			
	7	19	7407	9	8		
	16	25	10125	20			
	10	10, 11	6080	16			
	8	1, 2	LS161	14			
	7	3	SG4	11	6		
	3, 14	5	AM687	7			
	8	27, 28	TDC1014J	8			
	1, 16	31	10116		18		
	1, 16	42	10176		18		
	1, 16	20	10131		18		
	1, 16	7	10102				
	7	44	7450B	14			

U44	U38 U41
K8	
Q2	
RP3	
DR12	
C215	C2, 12, 22, 87-102, 145-200, 205-212
R223	RP1, 15, 16, 17, 42-69, 71-209
LAST USED	NOT USED

DESIGNATOR CHART

3. THIS SCHEMATIC TO BE USED WITH REV. (3) OF P.C.B. FAB
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	DR G.S.	2-14-83
MAT'L	CH	
FINISH	APPR	

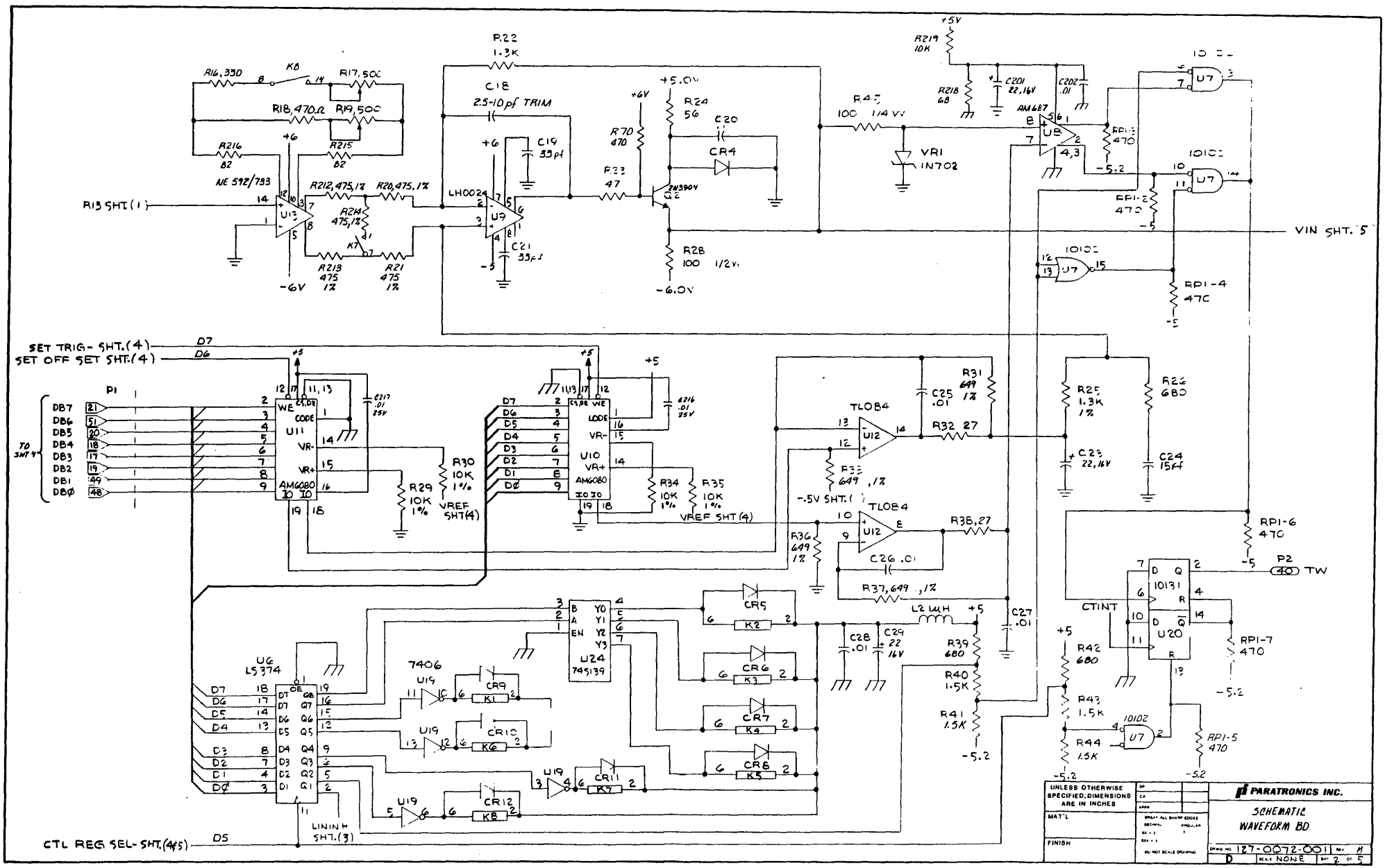
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
XX ± 1 °
XXX ± 1
DO NOT SCALE DRAWING

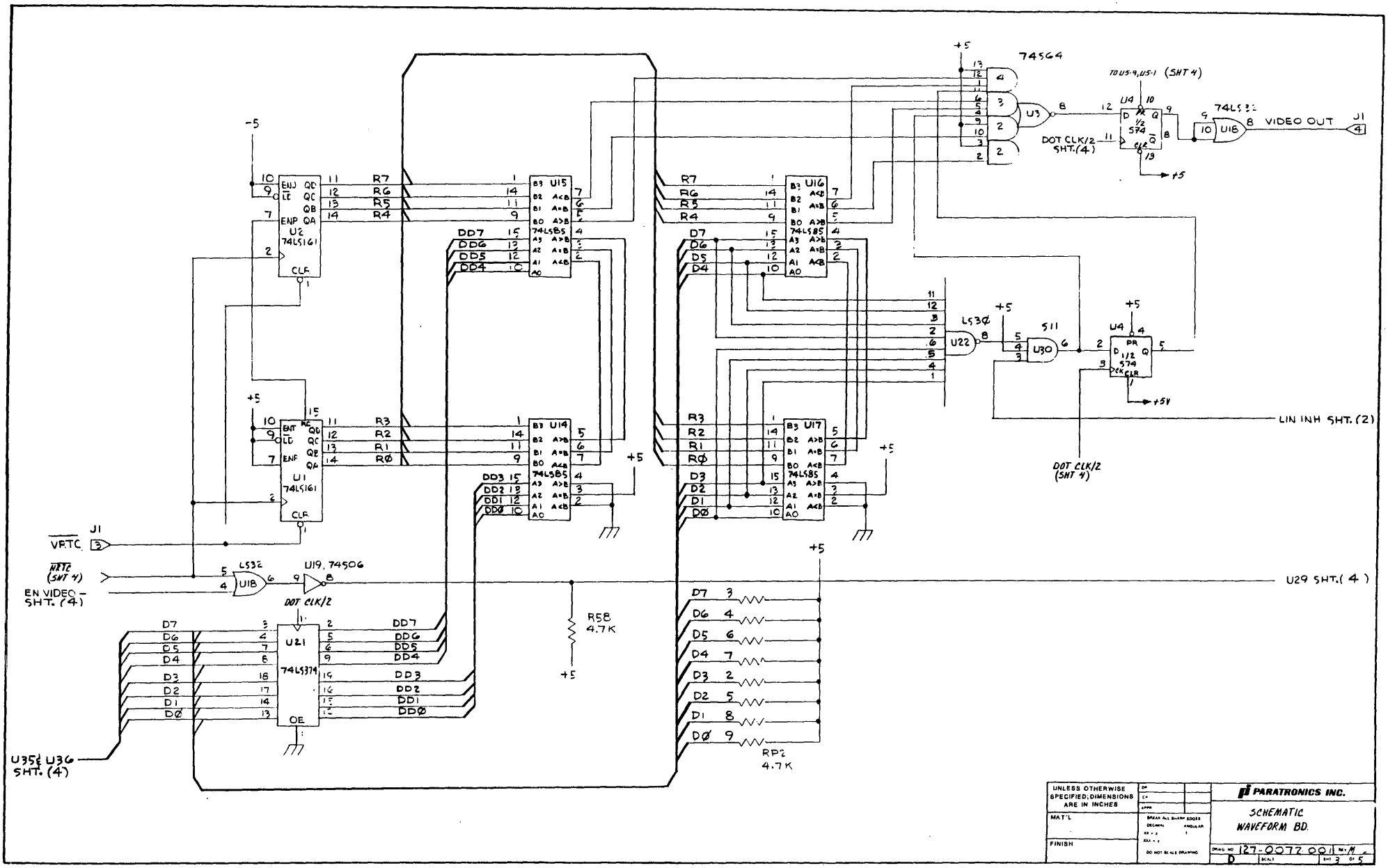
PARATRONICS INC.

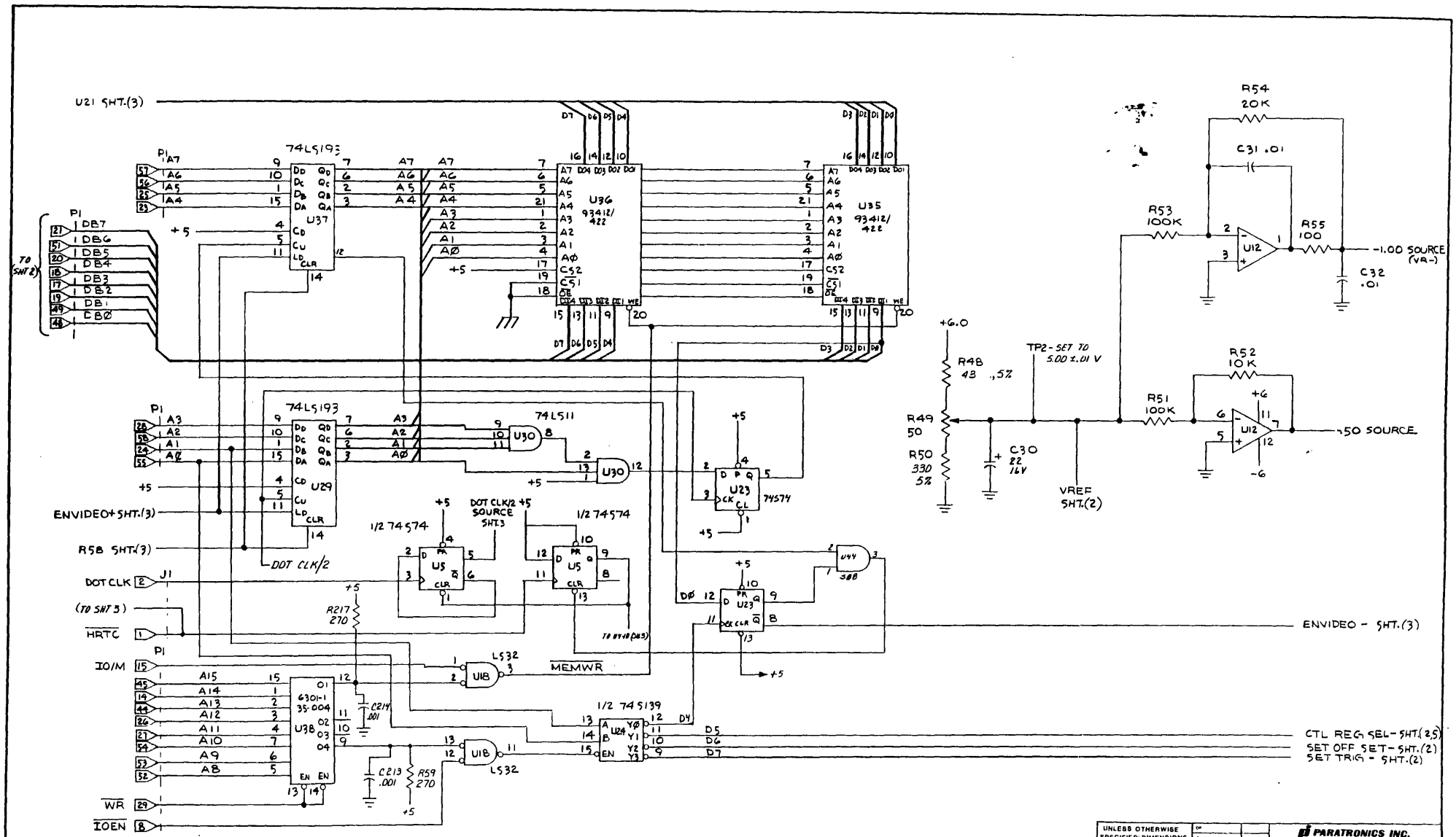
SCHEMATIC WAVEFORM BOARD

DRWG NO 127-0072-001 REV M

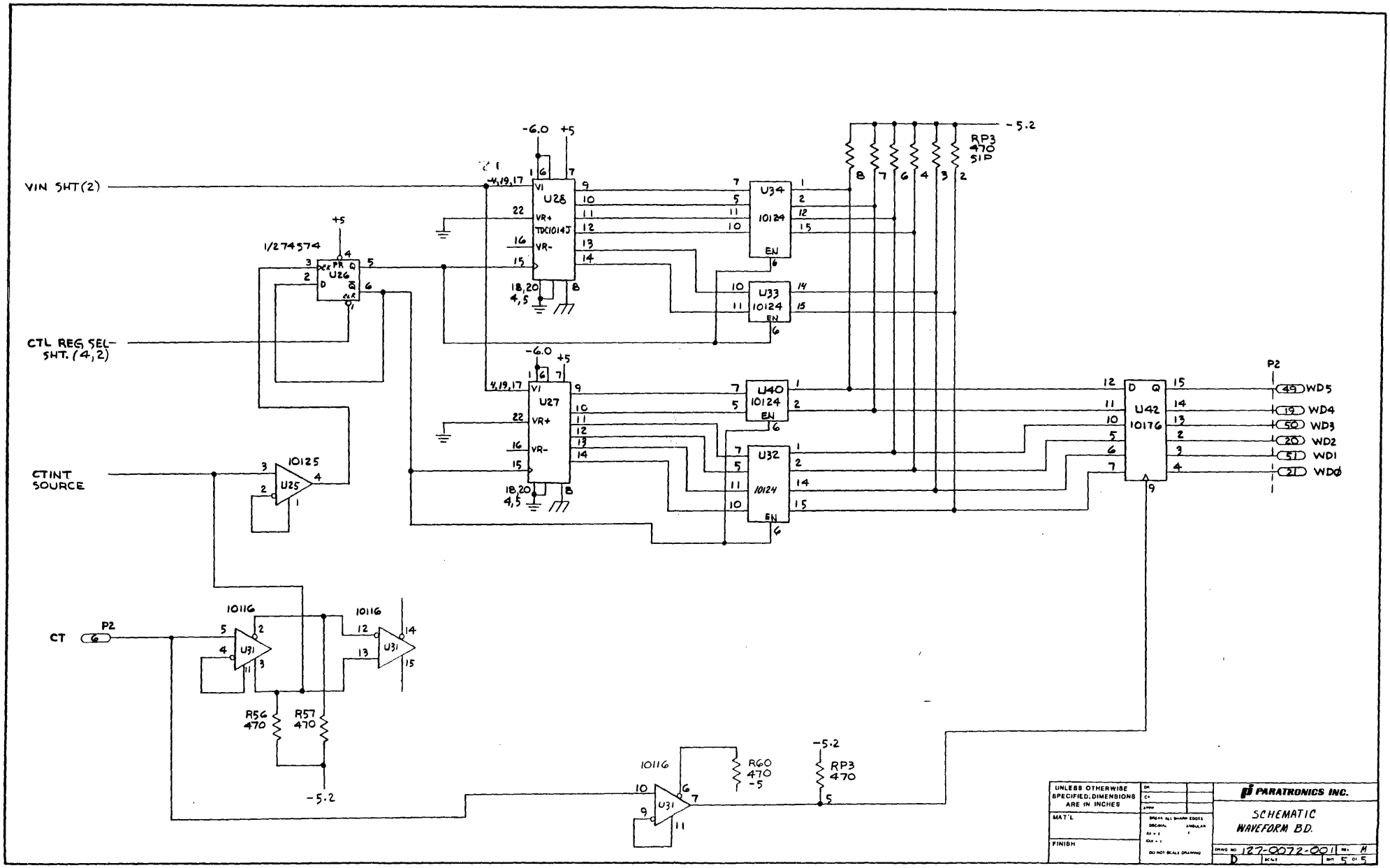
SIZE D SCALE SHT 1 OF 5


R22 1.3K
C18 2.5-10pf TRIM
R16, 330
R17, 50C
R18, 470Ω
R19, 50C
R216 82
R215 82
NE 592/783
R212, 475, 1%
R20, 475, 1%
R214 475, 1%
R213 475 1%
R21 475 1%
-6V
+6V
R70 470
R24 56
C20
CR4
R23 47
2N3904 Q2
R28 100 1/2W
-6.0V
C19 33pf
C21 33pf
LH0024
U9
+5.0V
R45 100 1/4 W
VR1 IN702
R219 10K
R218 68
C201 22,16V
C202 .01
AM687
U8
RP1-2 470
-5.2
U7
RP1-3 470
RP1-4 470
-5
VIN SHT. 5
R13 SHT(1)
SET TRIG- SHT.(4)
SET OFF SET SHT.(4)
D7
D6
P1
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
TO SHT 4
U11
U10
AM6080
R29 10K 1%
R30 10K 1%
VREF SHT(4)
R34 10K 1%
R35 10K 1%
C217 .01 25V
C216 .01 25V
TL084
U12
R31 649 1%
R32 27
R33 649 1%
-.5V SHT.( )
C25 .01
R25 1.3K 1%
R26 680
C23 22,16V
C24 15ff
R36 649 1%
R38, 27
C26 .01
R37, 649 1%
RP1-6 470
P2
40
TW
CTINT
10131
U20
RP1-7 470
R42 680
R43 1.5K
R44 1.5K
RP1-5 470
10102
C27 .01
C28 .01
C29 22 16V
L2 uH
R39 680
R40 1.5K
R41 1.5K
U24
74S139
U6
LS374
7406
U19
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
K1
K2
K3
K4
K5
K6
K7
K8
LININH SHT.(3)
CTL REG SEL- SHT.(4&5)
D5
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
PARATRONICS INC.
SCHEMATIC WAVEFORM BD
127-0072-0011
REV A
D
SCALE NONE
SHT 2 OF 5


74S64
U3
U4
74LS32
VIDEO OUT
J1
DOT CLK/2 SHT.(4)
TO U5-9, U5-1 (SHT 4)
U2
U1
74LS161
U15
U16
U14
U17
74LS85
U22
LS30
S11
LIN INH SHT. (2)
DOT CLK/2 (SHT 4)
VRTC
J1
VRTC (SHT 4)
EN VIDEO - SHT. (4)
LS32
U18
U19, 74S06
DOT CLK/2
U21
74LS374
OE
R58 4.7K
RP2 4.7K
U29 SHT.(4)
U35 & U36 SHT. (4)
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DO NOT SCALE DRAWING
PARATRONICS INC.
SCHEMATIC WAVEFORM BD.
127-0077-001
D
SHT 3 OF 5



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	DR	PARATRONICS INC.
MAT'L		SCHEMATIC WAVEFORM BD.
FINISH	DO NOT SCALE DRAWING	DWG NO 127-0072 001 REV 4
		SIZE D SCALE SHT 4 OF 5


VIN SHT(2)
CTL REG SEL- SHT. (4,2)
CTINT SOURCE
CT
P2
-6.0
+5
-5.2
RP3 470 SIP
1/2 74574
U26
U28
TDC1014J
U27
U34
U33
U40
U32
10124
U42
10176
10125
U25
10116
U31
R56 470
R57 470
R60 470 -5
WD5
WD4
WD3
WD2
WD1
WDØ
PARATRONICS INC.
SCHEMATIC
WAVEFORM B.D.
127-0072-001

DISK CONTROLLER

SECTION XIII
DISK CONTROLLER

13.1 DISK CONTROLLER CIRCUIT DESCRIPTION

Refer to schematic #127-0112-001 (sheet 1). The controller utilizes the Western Digital floppy disk controller chip set. These are U34, U18, and U19 (WD1793, WD1691, and WD2143). Signals received from the drive are buffered by U24 and U21 (7414). Signals sent to the drive are buffered by U22, U23 and U38 (7438). This floppy disk controller is programmed for operation with any industry standard 5 1/4" floppy disk drive at double density. The 1 MHz clock which U34 requires is generated from Y2, a 2 MHz crystal. The bi-directional data bus of U34 is buffered by U46 (DP8304). Circuitry for an RS-232C interface also is contained on this board.

Three potentiometers, R1, R2, R3, are shown in Figure 13-1. They are provided for aligning floppy disk R/W operations as follows:

a. R1 (50K ohm) adjusts the output of VCO U17 (74LS629) to free run at 2 MHz. Resistor network R9, R5, R7 ensures quiescence at approximately 1.5 volts at pins PU, PD of U18.

b. R2 (10K ohm) adjusts the amount of data write pre-compensation for tracks $\geq$44. It is nominally set at 400 ns. The amount of write precompensation can be observed at pin 4 of U18. This is done by putting the disk controller into a continuous write operation.

c. R3 (10K ohm) adjusts the width of RAW DATA-, nominally set at 750 ns.

U34 is selected by address decoder U56 and U35. U44 generates the clock required by latch U45 (LS374) and signal +RDBB. This signal puts the processor into a wait state by pulling RDY low when both INTRQ and DRQ are inactive.

U36 and U37 comprise a time-out circuit. This circuit is used to control the motor ON signal sent to the drive. The time-out circuit causes the motor ON signal to go inactive approximately three seconds after last access. This is done when there is no disk read/write operation, or when U34 has not been selected for more than three seconds. This is accomplished by keeping pin 1 of U36 and U37 high so as to allow the counter U36 to count. The ripple carry output will then cycle to U37 and U37, pin 6 will go low. That will eventually turn U60, pin 6 high. This will ensure that the clear inputs to both U36 and U37 go high allowing the counter to increment.

Refer to sheet 3 of the schematic. The RS-232 interface circuits are depicted on this sheet and are comprised of U47, U57, U58, Y1, VR5, and VR6. Level converters U57 and U58 (1488, 1489), send and receive data, respectively. Crystal Y1 provides the reference for UART U47 (6551). Voltage regulators VR5, VR6 provide +/- 15 volt power for the RS-232 level converters. Additionally, there are two power supply voltage regulators, for +5 volt (VR3) and +12 volt (VR2) shown on this sheet.

13.2 RAM DESCRIPTION

Refer to sheet 2 of the schematic. The system contains 48K bytes of memory (24 chips of 16K x 1 dynamic RAM, U1-U16 and U25-U32). Signals ROW- and COL- respectively strobe in row and column addresses into the RAMs during a read/write operation. U54 and U55 (LS244) buffer the address lines before being strobed into the respective RAM addresses.

Signals RAS, CAS- are generated by the following chips: U39, U49, U50, U40, U41. RAS- has two major constituents: RASA+ provides read or write access and RASR+ increments the refresh address counter U33, whose outputs will be strobed. Note

the row address inputs when ROW- and COL- have both gone inactive. The refresh counter outputs are buffered by U43 (LS244). U52 (LS374) latches the RAM data-out contents during a read operation. This allows the processor to read the RAM data at an appropriate time. U53 is the input data buffer to the RAMs.

13.3 RS-232C SERIAL INTERFACE

An RS-232C Serial Interface is also provided. The interface is bi-directional, and the Control Program can be commanded to transmit what is being displayed on the CRT. A printer with suitable serial input can thus produce hard-copy duplicates of the menu set-ups and data displays.

Timing, control and serialization of data for the interface are accomplished by the Control Program. Refer to sheet 3 of the schematic. The I/O circuitry consists of USART U47 (6251), line driver U57 (1488) and line receiver U56 (1489).

Signals are routed from the RS-232C connector on the rear panel via a 16-pin DIP socket (J2) on the motherboard to the DISK-RAM PCB socket S2B. Signal flow is shown in Table 13-1.

Some parameters required by the Control Program to operate the interface are obtained from the settings of a DIP switch located on the Processor PCB. The function of these switches for the RS-232C interface are shown in Table 13-2. Figure 13-1 depicts location.

13.4 SCHEMATICS, BOARD LAYOUTS AND PARTS LIST

The schematic diagram, board layout and parts list for the DISK-RAM Board are contained at the end of this section.

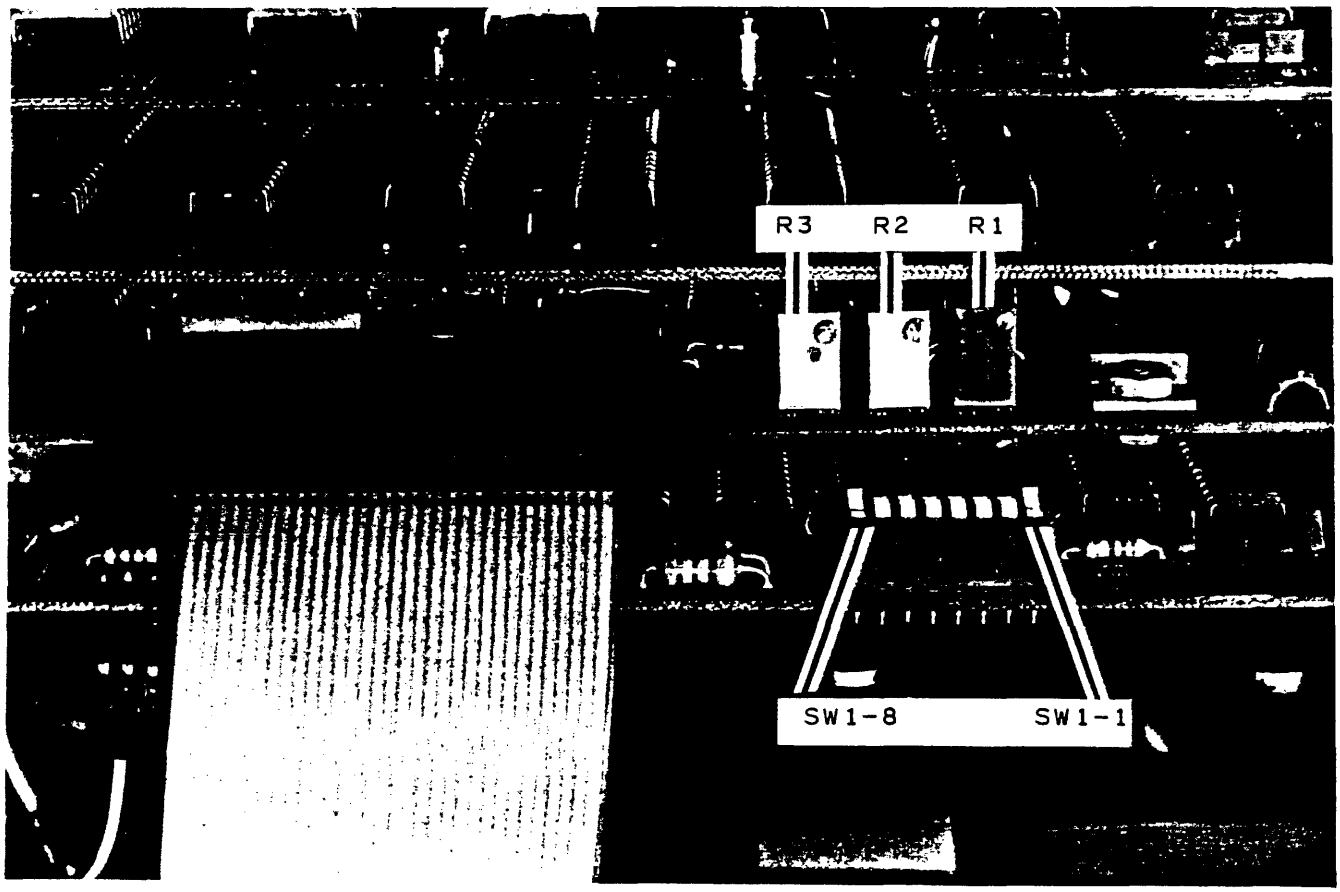


Figure 13-1 Potentiometer and Dip Switch Location

Table 13-1 RS-232C Signal Flow

Signal	U47 Pin	U57 IN	U57 OUT	S2B Pin	J2 Pin	Rear Panel DB-255 Pin
RXD	10	2	3	5	14	2*
RT	8	13	11	6	13	4
DTR	11	10	8	35	7	20
		U58 OUT	U58 IN			
DSR	17	6	4	7	11	6
CTS	9	3	1	37	12	5
DCD	16	11	13	36	9	8
RXD	12	8	10	38		3*

*NOTE: The DISK-RAM Board is provided with the transmit data signal on interface connector pin 2 and receive on pin 3. Jumpers on the board can be rewired to exchange the transmit and receive lines if desired. The jumpers are shown on schematic sheet 3 and on the board layout drawing.

Table 13-2 RS-232C DIP Switch Settings

NOTE: DIP Switch is located on Processor Board.

POWER LINE FREQ
====
50 Hz = OFF
60 Hz = ON

NOT USED

BUSY POLARITY
==========
LOW = OFF
HIGH = ON

SW1 8	7	6	5	4	3	2	1	BAUD RATE
				ON	ON	ON	ON	-
				ON	ON	ON	OFF	50
				ON	ON	OFF	ON	75
				ON	ON	OFF	OFF	110
				ON	OFF	ON	ON	135
				ON	OFF	ON	OFF	150
				ON	OFF	OFF	ON	300
				ON	OFF	OFF	OFF	600
				OFF	ON	ON	ON	1200
				OFF	ON	ON	OFF	1800
				OFF	ON	OFF	ON	2400
				OFF	ON	OFF	OFF	3600
				OFF	OFF	ON	ON	4800
				OFF	OFF	ON	OFF	7200
				OFF	OFF	OFF	ON	9600
				OFF	OFF	OFF	OFF	19200

PARENT ITEM 143-0112-0001 | CROSS REF ITEM | DESCRIPTION RAM/DISK ASSY I/S ENGR DRAW ECO 757 REV H | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 01 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CO	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0005-0091	15K OHM 1/4W 5% CF RES R6		1.000	EA	4C				10/19/81	
	04	110-0005-0103	47K OHM 1/4W 5% CF RES R7		1.000	EA	4C				10/19/81	
	04	111-0052-0103	22 UF 16V TANT DROP CAP C23		1.000	EA	4C				11/29/82	
	05	112-0027-0002	VOLTAGE REG. LM340T-5 VR1	ECO 550 REV A	1.000	EA	4C				2/05/82	
	03	112-0313-0001	CRYSTAL 2.000 MHZ CRYSTEX Y2		1.000	EA	4C				8/04/82	
	03	112-0314-0001	CRYSTAL 1.8432 MHZ CRYSTEX Y1		1.000	EA	4C				8/04/82	
	02	113-0001-0014	I.C. 7414 U21 U24		2.000	EA	4C					
	04	113-0001-0038	I.C. 7438 U22 U23 U38 U60		4.000	EA	4C				2/05/82	
	05	113-0002-0074	I.C. 74S74 U37		1.000	EA	4C				11/29/82	
	05	113-0003-0000	I.C. 74LS00 U50		1.000	EA	4C				9/29/81	
	04	113-0003-0001	I.C. 74LS01 U51		1.000	EA	4C				4/03/81	
	04	113-0003-0002	I.C. 74LS02 U39 U41		2.000	EA	4C				4/03/81	
	05	113-0003-0004	I.C. 74LS04 U48		1.000	EA	4C				4/03/81	
	05	113-0003-0032	I.C. 74LS32 U35		1.000	EA	4C				4/03/81	
	03	113-0003-0074	I.C. 74LS74 U40 U49 U59		3.000	EA	4C				11/29/82	
	06	113-0003-0138	I.C. 74LS138 U44 U56		2.000	EA	4C				4/03/81	
	05	113-0003-0139	I.C. 74LS139 U42		1.000	EA	4C				4/03/81	
	05	113-0003-0161	I.C. 74LS161 U36		1.000	EA	4C				4/03/81	
	03	113-0003-0244	I.C. 74LS244 U43 U53 U54 U55		4.000	EA	4C				4/03/81	
	05	113-0003-0374	I.C. 74LS374 U45 U52		2.000	EA	4C				4/03/81	
	02	113-0003-0393	I.C. 74LS393 U33		1.000	EA	4C					

PARENT ITEM 143-0112-0001 | CROSS REF ITEM | DESCRIPTION RAM/DISK ASSY I/S ENGR DRAW ECO 757 REV H | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 01 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	02	113-0003-0629	I.C. 74LS629 U17	ECO REV	1.000	EA	4C				8/27/81	
	05	113-0014-0002	I.C. DP8304N NSC U46	ECO 462	1.000	EA	4C				2/02/82	
	05	113-0037-0001	I.C. 1488L U59		1.000	EA	4C				4/03/81	
	03	113-0066-0001	I.C. MC1488N SIG U57		1.000	EA	4C				4/03/81	
	03	113-0073-0001	I.C. 9602 FAIRCHILD U25		1.000	EA	4C				4/03/81	
	02	113-0078-0001	I.C. 6551A UART U47		1.000	EA	4C					
	02	113-0079-0001	I.C. 4116 16K RAM U1 U10 U11 U12 U13 U14 U15 U16 U2 U25 U26 U27 U28 U29 U3 U30 U31 U32 U4 U5 U6 U7 U8 U9		24.000	EA	4C					
	02	113-0080-0001	I.C. WD2143 U19		1.000	EA	4C					
	02	113-0081-0001	I.C. WD1691 U18		1.000	EA	4C					
	02	113-0082-0001	I.C. WD1793.1 U34		1.000	EA	4C					
	04	117-0702-0003	4-40 KEP NUT EXT TOOTH STL/CAD 1 EA REGULATOR MTG.		1.000	EA	4C				10/19/81	
	04	117-1202-0003	4-40X1/4 PHILLIPS PH STL/CAD 1 EA REGULATOR MTG.		1.000	EA	4C				10/19/81	
	02	143-0112-0090	RAM/DISK ASSY O/S	ECO 757 REV H	1.000	EA	1C				4/03/81	

PARENT ITEM 143-0112-0090 | CROSS REF ITEM | DESCRIPTION RAM/DISK ASSY O/S ENGR DRAW ECO 757 REV H | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 02 | EFFEC 12/08/82 | UNIT MEAS EA | PLANNER

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	06	110-0005-0035	68 OHM 1/4W 5% CF RES R5		1.000	EA	4C				4/03/81	
	06	110-0005-0039	100 OHM 1/4W 5% CF RES R15		1.000	EA	4C				9/28/81	
	06	110-0005-0063	1K OHM 1/4W 5% CF RES R10 R16 R18		3.000	EA	4C				9/28/81	
	06	110-0005-0070	2K OHM 1/4W 5% CF RES R6 R13 R14		3.000	EA	4C				9/29/81	
	06	110-0005-0087	10K OHM 1/4W 5% CF RES R4 R11 R12		3.000	EA	4C				9/13/82	
	03	110-0005-0109	82K OHM 1/4W 5% CF MF RES R9		1.000	EA	4C				2/05/82	
	03	110-0207-0001	POT 50K OHM 63X R50K BECKMAN R1		1.000	EA	4C					
	03	110-0209-0001	POT 10K OHM 63X R10K BECKMAN R2 R3		2.000	EA	4C					
	05	110-0309-0001	RN 4.7K OHM X7 8 PIN SIP RP2 RP5		2.000	EA	4C				4/03/81	
	04	110-0317-0001	RN 10K OHM X7, 8 PIN SIP RP6		1.000	EA	4C				12/06/82	
	03	110-0321-0001	RN 22 OHM X7, 14 PIN DIP RP3 RP4		2.000	EA	4C					
	03	110-0322-0001	RN 220 OHM X7, 8 PIN SIP RP1		1.000	EA	4C					
	06	111-0004-0066	.01 UF 25V CD CAP C63 C9		2.000	EA	4C				4/03/81	
	06	111-0004-0072	.1 UF 25V CD CAP C1 C12 C13 C14 C15 C16 C17 C18 C19 C2 C25 C26 C27 C28 C29 C3 C30 C31 C33 C34 C35 C36 C37 C38 C39 C4 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C5 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C6 C60 C61 C64 C66 C67 C68 C69 C7 C70 C71 C72 C73 C8		61.000	EA	4C				4/03/81	
	06	111-0012-0030	100 PF 1KV CD CAP C62 C65		2.000	EA	4C				4/03/81	
	06	111-0012-0039	330 PF 1KV CD CAP C74		1.000	EA	4C				9/29/81	
	03	111-0025-0030	100 PF 500V DIPPED MICA CAP C22	ECO REV	1.000	EA	4C				8/27/81	
	03	111-0025-0032	150 PF MICA CAP C24	ECO REV	1.000	EA	4C				8/27/81	

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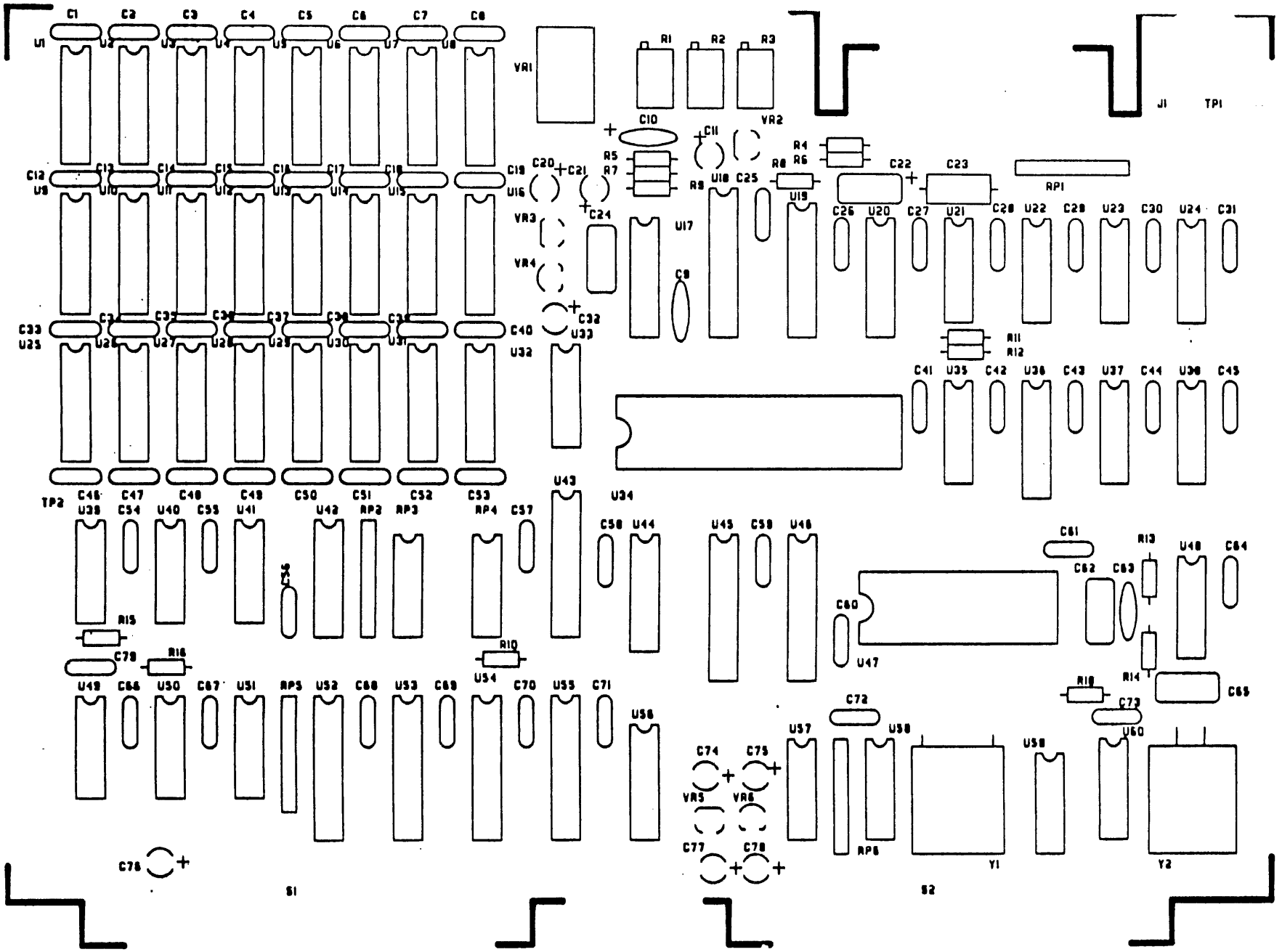
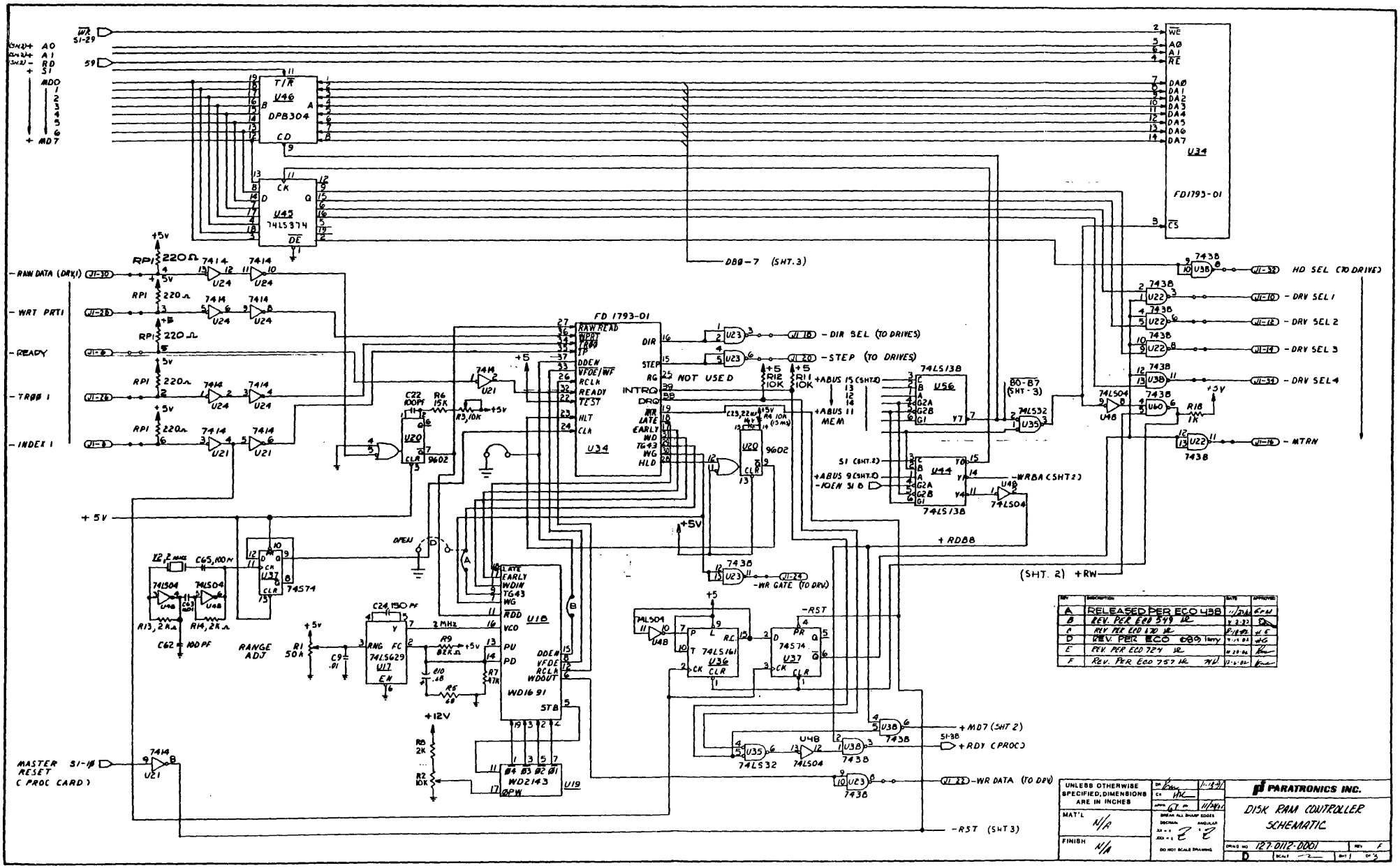
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	03	111-0054-1000	.68 UF 35V TANT DROP RAD CAP C10	ECO REV	1.000	EA	4C				9/24/81	
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C11 C21 C32 C74 C75 C76		6.000	EA	4C				3/29/82	
	05	111-0209-0096	10 UF 25V ELECT RADIAL CAP C20 C77 C78		3.000	EA	4C				3/29/82	
	05	112-0115-0001	V.REG +12V LM78L12ACZ 78L12CP VR2 VR5		2.000	EA	4C				4/03/81	
	05	112-0116-0001	V.REG -12V 79L12CPMOT LM320LZN VR6		1.000	EA	4C				4/03/81	
	03	112-0121-0001	V.REG +5V MC78L05 ACP MOT VR3		1.000	EA	4C					
	03	112-0122-0001	V.REG -5V MC79L05 ACP MOT VR4		1.000	EA	4C					
	06	115-0003-0001	SOCKET 14PIN U21 U22 U23 U24 U33 U35 U37 U38 U39 U40 U41 U48 U49 U50 U51 U57 U58 U59 U60		19.000	EA	4C				9/28/81	
	06	115-0005-0001	SOCKET 16PIN U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U25 U26 U27 U28 U29 U30 U31 U32 U17 U20 U36 U42 U44 U56		30.000	EA	4C				9/28/81	
	06	115-0008-0001	SOCKET 18PIN U19		1.000	EA	4C				9/28/81	
	06	115-0009-0001	SOCKET 20PIN U18 U43 U45 U46 U52 U53 U54 U55		8.000	EA	4C				9/28/81	
	04	115-0012-0001	SOCKET 28PIN U47		1.000	EA	4C				9/28/81	
	06	115-0013-0001	SOCKET 40PIN U34		1.000	EA	4C				9/28/81	
	03	126-0112-0001	RAM DISK P.C. FAB	ECO 757 REV C	1.000	EA	4C					



Ram Disk

NICOLET PARATRONICS

126-0112-0201 Rev. B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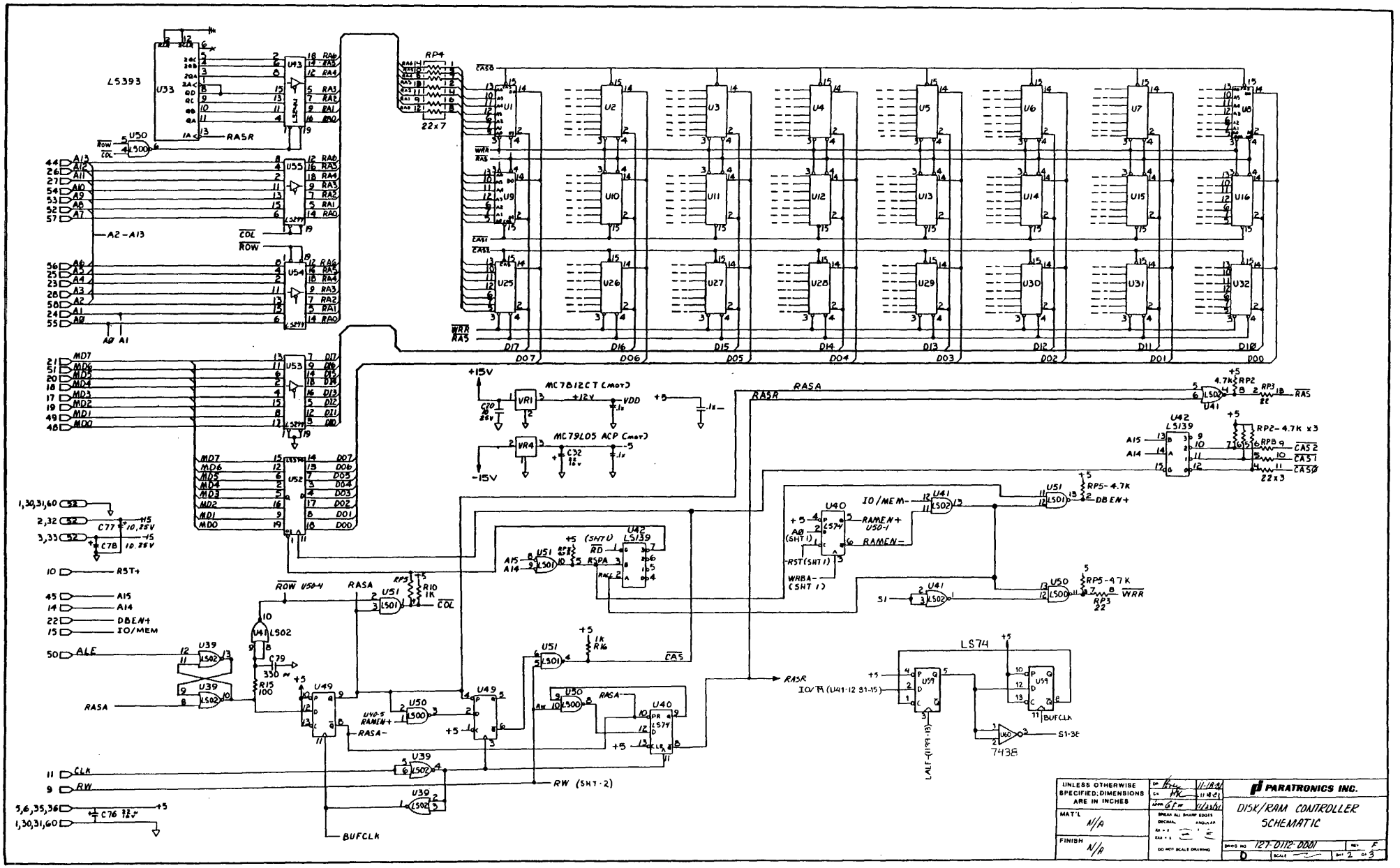
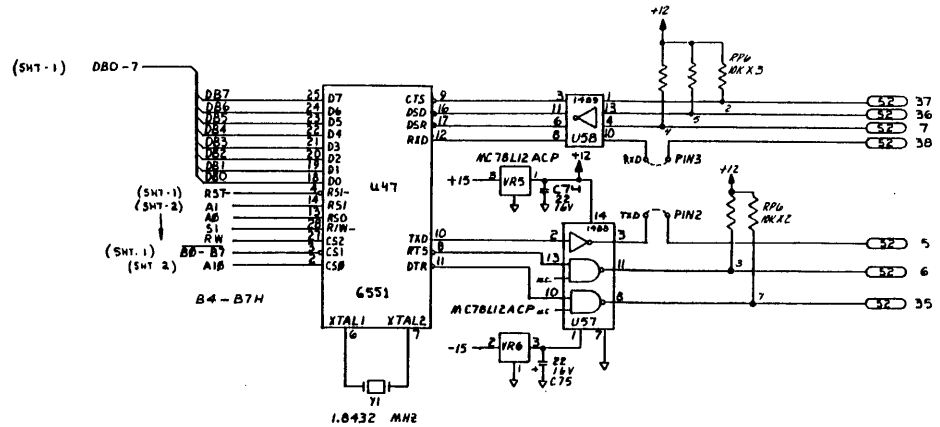
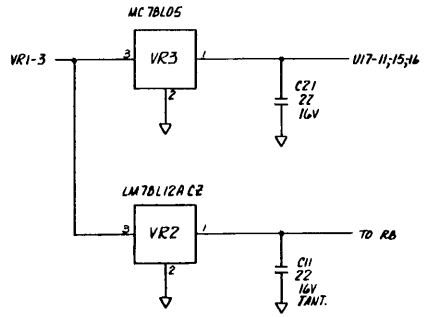
74LS374
FD1793-01
74LS629
WD1691
WD2143
74LS161
74574
74LS32
74LS04
74LS38
9602
DBB-7 (SHT.3)
-DIR SEL (TO DRIVES)
-STEP (TO DRIVES)
NOT USED
HD SEL (TO DRIVE)
-DRV SEL 1
-DRV SEL 2
-DRV SEL 3
-DRV SEL 4
-MTRN
-WR GATE (TO DRV)
-WR DATA (TO DRV)
+RDB8
(SHT. 2) +RW
+MD7 (SHT 2)
+RDY (PROC)
-RST (SHT 3)
MASTER RESET (C PROC CARD)
RANGE ADJ
RELEASED PER ECO 438
REV. PER ECO 549
REV PER ECO 620
REV. PER ECO 689
REV PER ECO 724
REV. PER ECO 757
PARATRONICS INC.
DISK RAM CONTROLLER SCHEMATIC
127.0112-0001

SECTION 13: DISK CONTROLLER



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Kelly 11-18-81	PARATRONICS INC.	
MAT'L N/A	CK MK 11-18-81	DISK/RAM CONTROLLER SCHEMATIC	
FINISH N/A	APPD GF 11/23/81	DRWG NO 127-0112-0001	REV F
BREAK ALL SHARP EDGES. DECIMAL ANGULAR .XX ± .1 .XXX ± .01 DO NOT SCALE DRAWING		D SCALE —	SHT 2 OF 3





V2	
U60	
VR6	
C79	
RP6	
R16	
LAST USED	NOT USED
REF. DESIGNATORS	

POWER AND GROUND LOCATOR CHART						
REF. DESIG.	TYPE	GND	+5V	-5V	+12V	-12V
U17	74LS629	8,5	15,16			
U46	DP8304	10	20			
U20	9602	8	16			
U19	2143-03	9	18			
U18	1691	10	20			
U34	1795-1	20	21		40	
U58	1489	7	14			
U57	1488	7			14	1
U47	6551A	1	15			
U1-U32	16K DRAM	16	9	1	8	
U33	LS393	7	14			
U53-U55	LS244	10	20			
U45,U52	LS374	10	20			
U21, U24	7414	7	14			
U22,U23,U38,U60	7438	7	14			
U50	74LS01	7	14			
U39, U41	74LS02	7	14			
U35	74LS32	7	14			
U40, U49, U59	74LS74	7	14			
U44, U56	74LS138	7	16			
U42	74LS139	7	16			
U36	74LS161	7	16			
U43	74LS04	7	14			
U37	74S74	7	14			

3. THIS SCHEMATIC TO BE USED WITH REVISION (5) "B" P.C.B. FABRICATION.
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DR [illegible] 11/18/81
CK HK
APPR [illegible] 11/23/81
BREAK ALL SHARP EDGES
DECIMAL ± .1 .XX ± .02 .XXX ± .010
ANGULAR ± 2°
DO NOT SCALE DRAWING

PARATRONICS INC.
DISK RAM CONTROLLER SCHEMATIC
DRWG NO 127-0112-0001
REV D
SCALE —
SHT 3

INPUT PROBES

SECTION 14: INPUT PROBES

SECTION XIV
INPUT PROBES

14.1 INTRODUCTION

There are three types of input probes used with the NPC 764 Logic Analyzer as follows: The Model 51A Probe (for the State section), the Model 80 (for the State/Timing section) and the Model 90 Probe (for the Counter-Timer/Signature Analyzer and Waveform sections). These probes provide high impedance signal inputs that can be placed close to the target signals. The probes then can convert the acquired signals to a form suitable for transmission to the NPC 764 for analysis.

The **Model 51A Probe** is used for input to the State analyzer section. The 51A provides inputs for 16 data signals, one clock signal, and two qualifier signals. Three Model 51A Probes are normally used when the analyzer is operated in the 48-bit mode. The qualifier signals may be applied (by keyboard instructions) to the clock signal. At the same time, they may be applied to any or all of the 16 levels of trigger words. The nominal impedance of all inputs is 44K ohms shunted by 15 pF. The probe contains a manual adjustment for setting the logic threshold of the incoming signals. It also contains a switch for pre-setting this threshold to TTL level. The probe also contains a switch for inverting all incoming signals if desired.

The **Model 80 Probe** is used for input to the Timing analyzer section. It provides inputs for eight data signals, a clock signal, and a clock-qualifier signal. The nominal impedance of all inputs is 1 Megohm shunted by 6 pF. The logic threshold voltage for these inputs is variable and is set by keyboard entry. Also, the inputs have a hysteresis function that can be turned on or off from the keyboard.

The **Model 90 Probe** is used for input to the Counter-Timer/Signature Analyzer and to the Waveform Analyzer sections. It provides a single input that can be manually switched between two input impedance levels as follows: 10 Megohms shunted by 12 pF and having a 10:1 attenuation ratio, and 1 Megohm shunted by 70 pF and having a 1:1 attenuation ratio.

These probes are described in greater detail in the following subsections.

14.2 MODEL 51A PROBE

The Model 51A Probe interfaces the State analyzer to the system under test. This probe incorporates comparators for high input impedance and variable threshold selection. Each Probe interfaces 16 data bits, 2 qualifier bits, and a clock input. A switch on the probe is provided to present a fixed threshold of 1.6V for convenience. A monitoring point permits measuring the threshold voltage that can be adjusted over the range of +/- 6V. The voltage at this monitoring point with respect to probe ground is one-half, or 50%, of the actual threshold voltage. The Model 51A also incorporates a data complement (invert) switch for active-low bus conventions. The impedance for all inputs is 44K ohms shunted by 15 pF.

Refer to schematic #127-0015-0021, the board layout and parts list at the end of this section.

Resistors RN1-RN4 form voltage dividers that apply one-half of the input voltage to U1-U5. U1-U5 are high-speed quad comparators, either Motorola MC3430 or National DS3651. The input capacitance of the comparators is compensated by capacitors C1-C19. Resistors R4, R5 and R7 provide approximately 200 mV of hysteresis to the clock input. Comparators U1-U5 accept a threshold reference from the voltage divider formed by R10-R12 or R8,R9. These high-speed comparators convert the variable input voltages to TTL levels. Switch

S1 controls whether buffers U6-U10 operate in a true or complement mode. U10 also selects clock polarity and provides buffering for clock and qualifier signals. The probe receives +/- 5V power from the analyzer through the ribbon cable.

The Model 51A Probe receives a functional check when used in the analyzer self-test with the Logic Analyzer test card.

Although the input resistor divider provides some input protection, voltages higher than +/- 25 V may damage the circuits and should be avoided.

14.3 MODEL 80 PROBE

The Model 80 Probe is used for input to the Timing analyzer section. Refer to schematic #127-0052-001, board layout and parts list at the end of this section. For each of the 10 input channels, the Model 80 Probe contains an Input Buffer and a Comparator. The circuits of all channels are identical. The schematic diagram shows the first two channels in detail and the remaining channels in an abbreviated form.

14.3.1 INPUT BUFFERS

There are 10 Input Buffers. One for each of the eight data inputs, one for the clock input and one for the clock-qualifier input. Because all the buffers are identical, only one will be described. That description can be applied to all the others.

The channel-0 input buffer consists of transistor Q1, a Siliconix E420 dual J-FET; CR1 and CR2, both 1N3600 diodes; and various capacitors and resistors. The major functions of the buffer are to provide signal isolation and high input impedance.

The impedance presented to the incoming signal is essentially determined by the 3:1 passive divider made up of R1, R2, C1, C2 and stray capacity. The high input impedance of Q1A has little effect on the overall circuit impedance. This input impedance is nominally 1 Megohm shunted by 6 Pf. CR1 and CR2 are clamping diodes that provide overvoltage protection for Q1A against input voltage peaks as high as +/-100V. The usable input voltage switch (before clipping by these diodes begins) is +/- 9V. Q1A is connected in cascade with Q1B in a zero-offset source follower circuit. The output of this circuit is fed to the Channel-0 Comparator.

Variable resistor R5 is used to compensate for any mismatch that may exist between Q1A and Q1B. R5 is adjusted so that, with the signal input grounded, the voltage at pin 9 of comparator U1B is 0.0V +/- .005V.

14.3.2 COMPARATORS

As with the Input Buffers, there are 10 identical Comparators and only one will be described.

The Channel-0 Comparator consists solely of U1B, one-half of an AMD AM687 high-speed dual comparator with complementary ECL outputs. The Comparator converts a variety of logic-signal inputs into outputs with pre-established ECL levels and fast transition times.

The comparator positive input, U1B-9, is fed with the low impedance signal from the Channel-0 Buffer. The negative input, U1B-10, is fed with threshold voltage THRESHA (Threshold A) that is compared to the incoming signal. As the input signal crosses this threshold from below, the output of the comparator switches from low to high. As the input signal crosses this threshold from above, the output of the comparator switches from high to logic. THRESHA is received, via connector pin J6-5, from a D/A converter on the Timing Memory Board (sheet 1, TMB schematic). It is keyboard-specified over a range of -6.4V to +6.35V in 0.05V steps. The default value is +1.60V, suitable for TTL logic. Threshold voltage accuracy is +/- 0.05V.

The comparator LE (Latch Enable) input, U1B-13, is grounded. Under this condition, if LE- is held negative (below -100 mV), the comparator operates in a normal manner. If LE- is driven high (above +100 mV), the comparator outputs are latched in their existing logic states. The latched mode is

not used in this application. In the transition region between latched and unlatched modes, there is a small hysteresis range for LE-. This feature is used in the circuit.

When the input hysteresis function has been keyboard-specified as ON, a nominal voltage of +1.7V is sent to the probe. This signal (HYST) appears at connector pin J6-34. This voltage is divided down by R6 and R8 to a nominal +45 mV at the LE- input, U1B-12. There it produces a hysteresis of 67 mV at the probe input (because of the 3:1 input divider, R1-R2). When the input hysteresis function has been keyboard-specified as OFF, signal HYST becomes -5.1V. This divides down to -134 mV at LE- and puts the comparator in the non-hysteresis, non-latch mode. The signal HYST is received from the Control Port on the Timing Memory Board via connector S2-15 (sheet 1, TMB).

Comparators will oscillate if threshold input signals have longer rise or fall times than the propagation time of the comparator (8 ns in this case). However, in this circuit such oscillations are prevented if the hysteresis function is in effect. It is recommended that hysteresis be used normally. The exception would be an application requiring an investigation of the transition region. Accordingly, the default hysteresis condition is ON.

The comparator provides a differential output at ECL levels. The output signals, DO+ and DO-, are fed through pins J6-33, 32 to the Timing Memory Board at pins S2-52, 53 (sheet 3, TMB). The outputs of U1B are open emitters. The necessary pull-down resistors on the Timing Memory Board, provide a 60 ohm termination for each of the signal lines. Both polarities of the data signals are needed by the glitch detecting circuitry on the Timing Memory Board. But the positive signal alone is used when the sample mode, rather than the glitch-capture mode, has been keyboard selected.

The clock channel output signals, CLK+ and CLK-, are fed via J6-3, 2 to Clock Control on the Timing Control Board at S2-56, 55. They may be possible keyboard selected as the operating clock (refer to TCB schematic sheet 8). The clock-qualifier channel output signals, QCLK+ and QCLK-, are fed via J6-9, 8 to Clock Control on the Timing Control Board at S2-58, 57. These signals may be used as a clock qualifier if the probe clock has been selected as the operating clock. Both polarities of the clock and clock-qualifier signals are needed by the logic in the Clock Control circuits.

14.3.3 APPLICATION

The following comments pertain to the internal operation of the Probe-Analyzer system. They are not intended as a discussion of the extensive uses of the instrument in analyzing a target system. Refer to the Operator's Manual for more information on the many uses of the NPC 764).

The Model 80 Probe is designed for use with both timing and state analysis. The discussion will cover both types of analysis. Essentially, the only difference between the two applications is in the use of the clock and clock-qualifier inputs.

In the **timing analysis mode**, the clock will probably be selected as internal. The probe clock and clock-qualifier inputs will not be connected to the system under test. Any signal at the clock-qualifier input has no effect when an internal clock is being used.

In the **16-bit state analysis mode**, the clock will probably be selected as external. The probe clock input will be connected to the system under test in order to provide the external clock. The clock-qualifier input may also be connected if qualification of the clock signal is desired. But the qualifier signal **cannot** be applied to the arm or trigger words.

14.4 MODEL 90 PROBE

The Model 90 Probe interfaces the Counter-Timer/Signature Analyzer or the Waveform Analyzer to the system under test. It is a high-quality oscilloscope probe selected

for suitability to this application.

The Model 90 Probe is a passive probe with a three-position slide switch in the probe body. The three switch positions are X10 (10:1 attenuation), REF (ground reference) and X1 (1:1 attenuation). The probe specifications at the three switch positions are shown below.

The following accessories are supplied as standard equipment:

Insulating Tip
Spring Hook
IC Adapter
BNC Adapter
Trimmer Tool

MODEL 90 PROBE SPECIFICATIONS

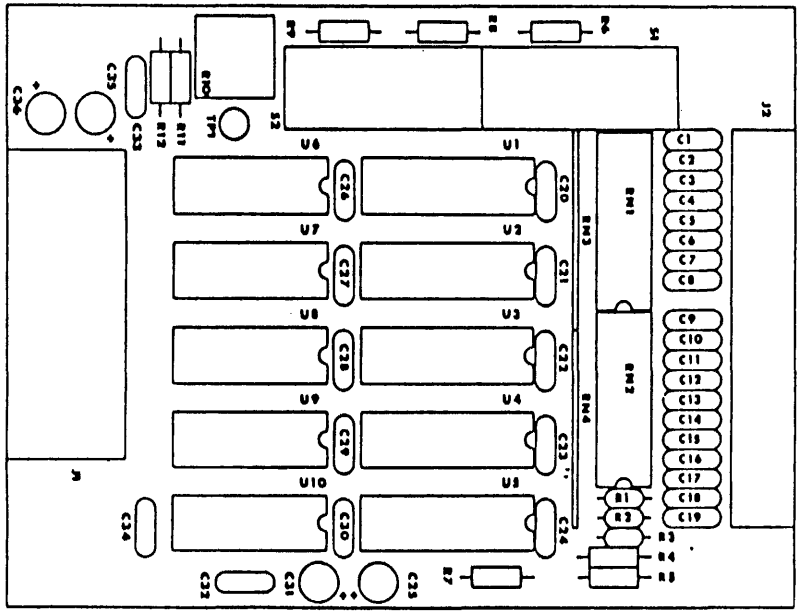
	X10 POSITION	REF POSITION	X1 POSITION
BANDWIDTH	d-c to 100 MHz	---	d-c to 10 MHz
RISE TIME	3.5 ns	---	---
INPUT RESISTANCE	10 Megohm	Probe tip - 90 ohm Analyzer input-grounded	1 Megohm
INPUT CAPACITY	12 pF	---	70 pF
WORKING VOLTAGE	500 Vdc, peak	---	600 Vdc, peak

PARENT ITEM: 143-0015-0002 | CROSS REF ITEM: | DESCRIPTION: M51A P.C.B. I/S ASSY. ENGR DRAW ECO 722 REV D | BATCH QTY: 1 | ITEM TYPE: 1 | LOW LEVEL: 04 | EFFEC: 12/08/82 | UNIT MEAS: EA | PLANNER:

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	113-0001-0006	I.C. 7406 U6 U7 U8 U9		4.000	EA	4C				3/25/80	
	05	113-0002-0006	I.C. 7406 U10		1.000	EA	4C					
	05	113-0021-0001	I.C. MC3430P MOT NSC DS3691N U1 U2 U3 U4 U5		5.000	EA	4C					
	05	114-0003-0001	CONN 20PIN DUAL 6-AA-02-20-1PX J2		1.000	EA	4C					
	05	124-0001-0001	MODEL 50/51 PROBE CABLE ASSY J1	ECO 584 REV F	1.000	EA	4C					
	05	143-0015-0002	M51A PROBE-OUTSIDE ASSY.	332 C	1.000	EA	1C					

PARENT ITEM 143-0015-0092 | CROSS REF ITEM | DESCRIPTION M51A PHONE-OUTSIDE ASSY. ENGR DRAW 332 C | BATCH QTY 1 | ITEM TYPE 1 | LOW LEVEL 05 | EFFEC 1/04/83 | UNIT MEAS EA | PLANNER

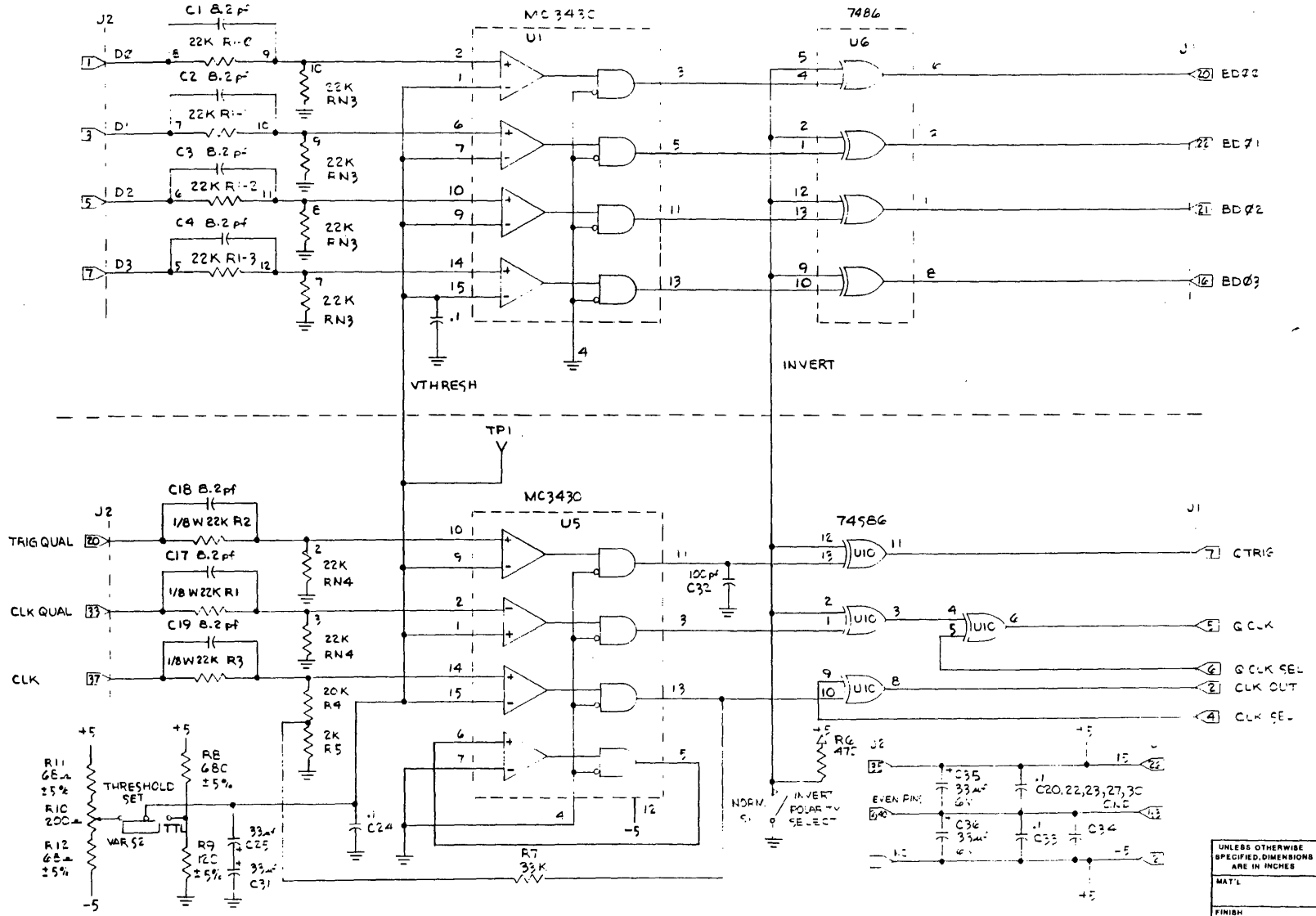
REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0002-0095	22K OHM 1/8W 5% CF RES R1 R2 R3		3.000	EA	4C					
	06	110-0005-0035	68 OHM 1/4W 5% CF RES R11 R12		2.000	EA	4C					
	06	110-0005-0041	120 OHM 1/4W 5% CF RES R9		1.000	EA	4C					
	06	110-0005-0055	470 OHM 1/4W 5% CF RES R6		1.000	EA	4C					
	06	110-0005-0059	680 OHM 1/4W 5% CF RES R8		1.000	EA	4C					
	06	110-0005-0070	2K OHM 1/4W 5% CF RES R5		1.000	EA	4C					
	06	110-0005-0094	20K OHM 1/4W 5% CF RES R4		1.000	EA	4C					
	06	110-0005-0099	33K OHM 1/4W 5% CF RES R7		1.000	EA	4C				1/15/80	
	06	110-0206-0001	POT. 200 OHM 3386P-1-201 BOURN R10		1.000	EA	4C					
	06	110-0311-0001	RN 22K OHM X8 16 PIN DIP RN1 RN2		2.000	EA	4C					
	06	110-0312-0001	RN 22K OHM X9 10 PIN SIP RN3 RN4		2.000	EA	4C					
	06	111-0004-0072	.1 UF 25V CD CAP C20 C21 C22 C23 C24 C26 C27 C28 C29 C30 C33 C34		12.000	EA	4C					
	06	111-0012-0010	8.2 PF 1K CD CAP C1 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C2 C3 C4 C5 C6 C7 C8 C9		19.000	EA	4C				1/15/80	
	06	111-0012-0030	100 PF 1KV CD CAP C32		1.000	EA	4C					
	07	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C25 C31 C35 C36		4.000	EA	4C				8/21/80	
	06	115-0003-0001	SOCKET 14PIN U10 U6 U7 U8 U9		5.000	EA	4C					
	06	115-0005-0001	SOCKET 16PIN U1 U2 U3 U4 U5		5.000	EA	4C				4/23/81	
	07	116-0006-0001	SWITCH DPDT GF-126-0161 CW S1 S2		2.000	EA	4C					
	06	117-0030-0001	TERMINAL 120-1032-04 CAMBION TP1		1.000	EA	4C					
	06	126-0015-0002	M51A PCB FAB	ECO 205 REV C	1.000	EA	4C					



M51A Probe

Nicolet Paratronics
126-0015-0202 Rev C.

REV.	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 104	6-14-77	7-7-77
C	REV. PER ECO 130	9-8-77	9-27-80
			E.S.
D	Rev Per Eco 332	11-8-82	11-9-82



POWER DISTRIBUTION				
U NO.	TYPE	+5	GND	-5
U1-U5	MC3430	16	8	12
U6-U9	7486	14	8	—
U10	74S86	14	8	—
RN3,RN4	9X22K	—	1	—

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES

MAT'L

FINISH

DR G.C. 1-14-77

CK J.P. 1-14-77

APPR.

BREAK ALL SHARP EDGES

DECIMAL ANGULAR

XX ± .1 ±

XXX ± .5

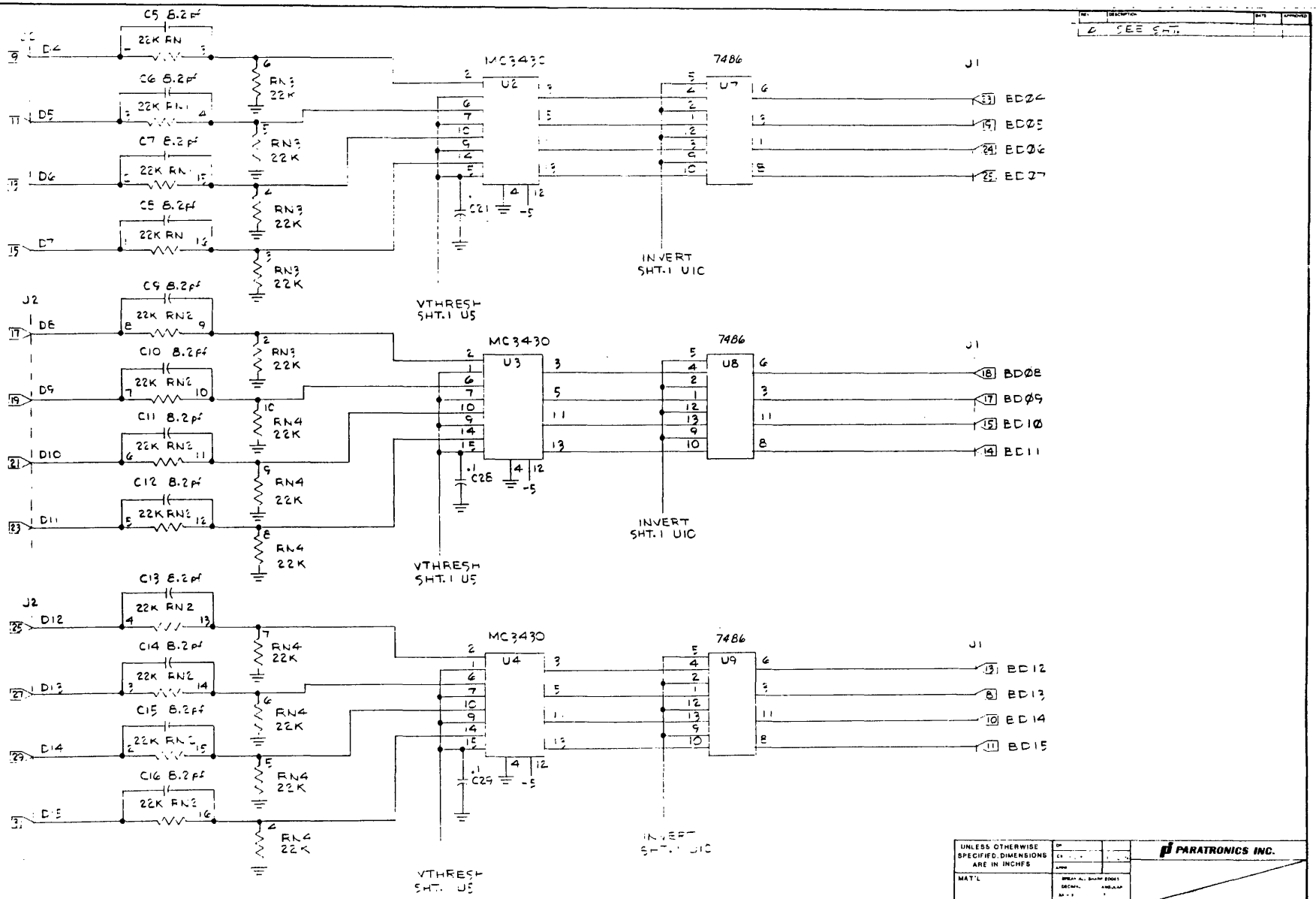
DO NOT SCALE DRAWING

PARATRONICS INC.

SCHEMATIC DIAGRAM
MODEL 51 A PROBE

DWG NO. 51-00-5-002 REV. E

D SCALE SHT 1 OF 2


C5 8.2pf
22K RN
D4
C6 8.2pf
D5
C7 8.2pf
D6
C8 8.2pf
D7
RN3 22K
MC3430
U2
7486
U7
J1
BD04
BD05
BD06
BD07
C21
INVERT SHT.1 U1C
VTHRESH SHT.1 U5
J2
C9 8.2pf
22K RN2
D8
C10 8.2pf
D9
C11 8.2pf
D10
C12 8.2pf
D11
RN4 22K
U3
U8
BD08
BD09
BD10
BD11
C28
C13 8.2pf
D12
C14 8.2pf
D13
C15 8.2pf
D14
C16 8.2pf
D15
U4
U9
BD12
BD13
BD14
BD15
C29
SEE SHT.

PRINT PHANTOM ITEMS
PRINT COMPONENTS OF PHANTOMS
PRINT PHANTOM/COMPONENT COMMENTS

PARENT ITEM 143-0052-0090 CROSS REF ITEM DESCRIPTION MODEL 80 PROBE, OUTSIDE ENGR DRAW ECO 722 REV D BATCH QTY 1 ITEM TYPE 1 UNIT MEAS EA LOW LEVEL 05 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NBR	FIRST CP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	110-0001-0435	332K OHM 1/8W 1% OR 2% MF RES R2-0 R2-1 R2-2 R2-3 R2-4 R2-5 R2-6 R2-7 R2-8 R2-9		10.000	EA	4C				4/10/81	
	06	110-0001-0464	665K OHM 1/8W 1% OR 2% MF RES R1-0 R1-1 R1-2 R1-3 R1-4 R1-5 R1-6 R1-7 R1-8 R1-9		10.000	EA	4C				4/10/81	
	06	110-0002-0025	27 OHM 1/8W 1% CF RES R6		1.000	EA	4C					
	06	110-0002-0036	75 OHM 1/8W 5% CF MF RES R4-1 R4-10R4-2 R4-3 R4-4 R4-5 R4-6 R4-7 R4-8 R4-9		10.000	EA	4C					
	06	110-0002-0039	100 OHM 1/8W 5% MF CF RES R3-1 R3-10R3-2 R3-3 R3-4 R3-5 R3-6 R3-7 R3-8 R3-9		10.000	EA	4C					
	06	110-0002-0063	1K OHM 1/8W 5% CF RES R8		1.000	EA	4C					
	06	110-0005-0031	47 OHM 1/4W 5% CF RES R10 R11 R12 R9		4.000	EA	4C					
	06	110-0205-0001	POT, 50 OHM, TRIM 3329H-50 R5-1 R5-10R5-2 R5-3 R5-4 R5-5 R5-6 R5-7 R5-8 R5-9		10.000	EA	4C					
	06	111-0004-0066	.01 UF 25V CO CAP C3-1 C3-10C3-2 C3-3 C3-4 C3-5 C3-6 C3-7 C3-8 C3-9 C4-1 C4-10C4-2 C4-3 C4-4 C4-5 C4-6 C4-7 C4-8 C4-9 C5-1 C5-2 C5-3 C5-4 C5-5 C6-1 C6-2 C6-3 C6-4 C6-5 C7-1 C7-2 C7-3 C7-4 C7-5 C8-1 C8-2 C8-3 C8-4 C8-5 C9		41.000	EA	4C					
	06	111-0312-0006	5 PF 1KV CO CAP C1-0 C1-1 C1-2 C1-3 C1-4 C1-5 C1-6 C1-7 C1-8 C1-9		10.000	EA	4C				4/10/81	
	17	111-0207-0103	22 UF 16V ELECTRO RADIAL CAP C10 C11		2.000	EA	4C				8/21/80	
	06	112-0114-0001	TRANS 0440 E420 E421 SILICON Q1-1 Q1-10Q1-2 Q1-3 Q1-4 Q1-5 Q1-6 Q1-7 Q1-8 Q1-9		10.000	EA	4C					
	07	112-0204-0001	DIODE 1N3600 1N4148 4149 4150 CR1-1 CR1-2 CR1-3 CR1-4 CR1-5 CR1-6 CR1-7 CR1-8 CR1-9 CR1-10 CR2-1 CR2-2 CR2-3 CR2-4 CR2-5 CR2-6 CR2-7 CR2-8 CR2-9 CR2-10		20.000	EA	4C					
	06	115-0005-0001	SOCKET 16PIN U1 U2 U3 U4 U5		5.000	EA	4C					
	06	117-0010-0001	TERMINAL 120-1032-04 CAMBION TP1		1.000	EA	4C					
	06	126-0052-0001	MODEL 80 PCB FAB	ECO 432 REV C	1.000	EA	4C					

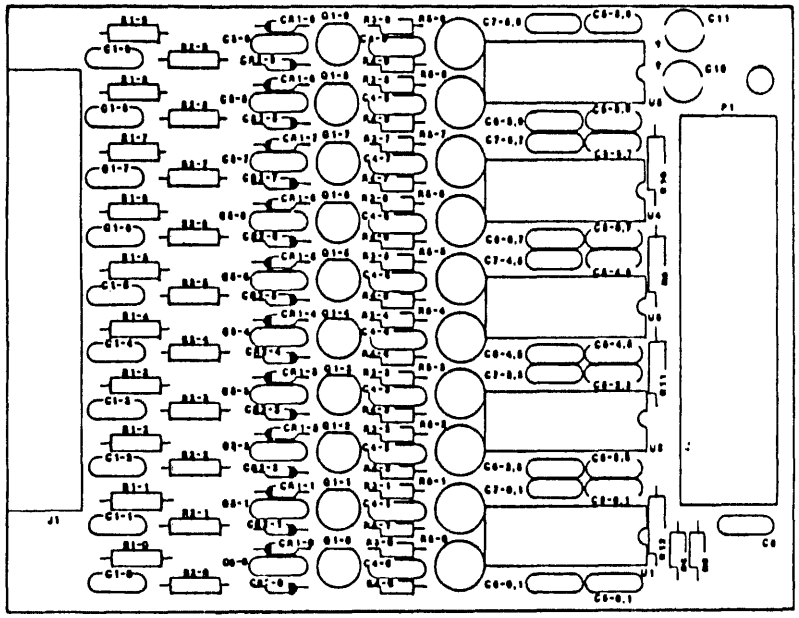
PARENT ITEM 143-0052-0090 | CROSS REF ITEM | DESCRIPTION MODEL 90 PROBE, OUTSIDE ENGR DRAW ECO 722 REV D | BATCH QTY 1 | ITEM TYPE 1 UNIT MEAS EA | LOW LEVEL 05 PLANNER

REF NBR	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	TYP	OPT NBR	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	06	117-0030-0001	TERMINAL 120-1032-04 CAMDION TPL		1.000	EA	4C					
	06	125-0052-0001	MODEL 90 PCB FAB	ECO 432 REV C	1.000	EA	4C					

PRINT PHANTOM ITEMS
PRINT COMPONENTS OF PHANTOMS
PRINT PHANTOM/COMPONENT COMMENTS

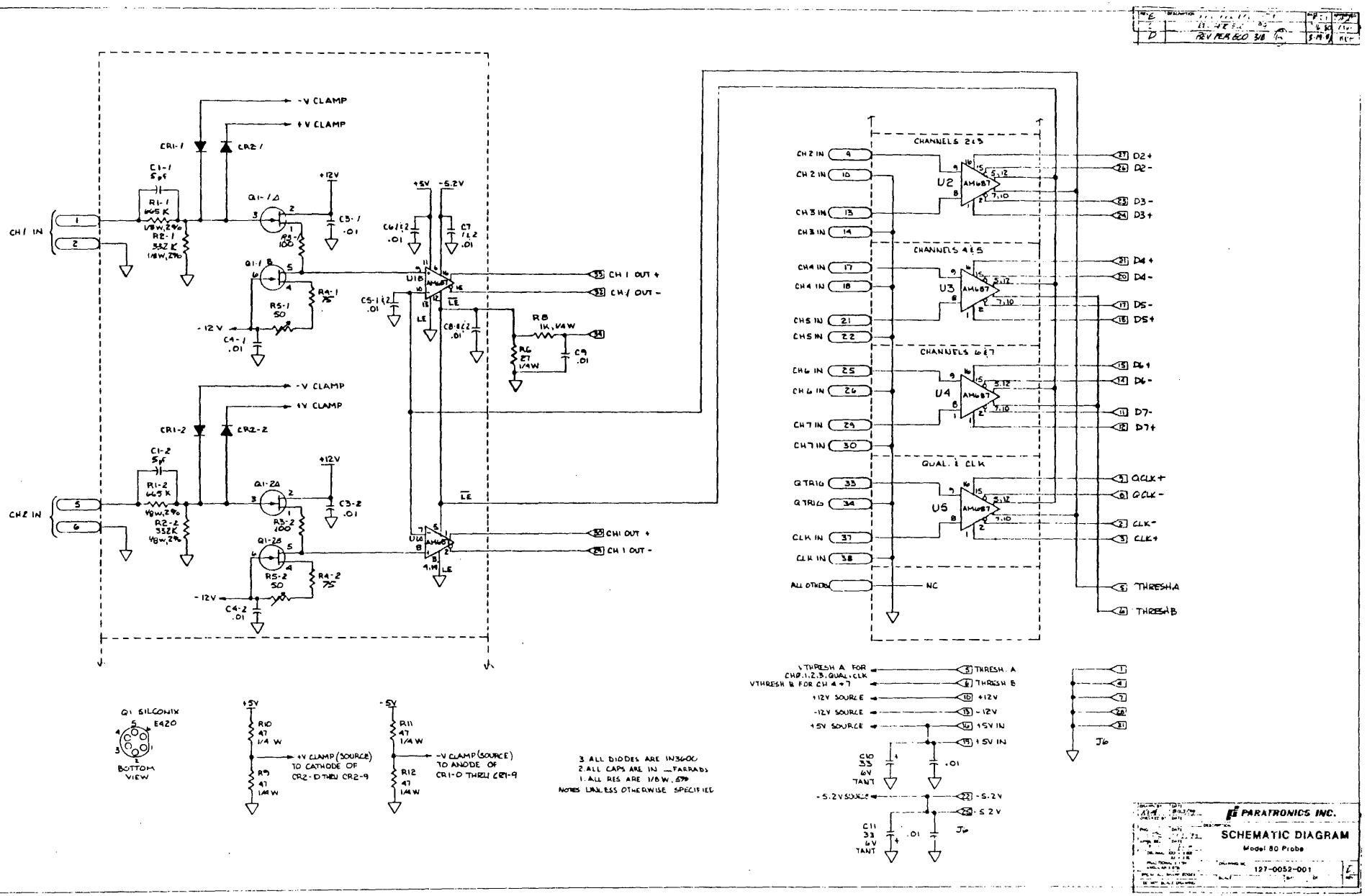
PARENT ITEM 143-0052-0001 CROSS REF ITEM DESCRIPTION MOD P.C.B. I/S ASSY. FROM DRAW ECO 722 REV D BATCH QTY 1 ITEM TYPE 1 UNIT MEAS EA LOW LEVEL 04 PLANNER

REF NUM	LL CD	COMPONENT & CROSS REF.	DESCRIPTION & COMMENT	ENGINEERING DRAWING NUMBER	QUANTITY PER	ITEM UM	ITEM TYP	OPT NEP	FIRST OP SEQ	LT ADJ	EFFECTIVE DATES FROM	TO
	05	113-0046-0001	I.C. AM6N7 U1 U2 U3 U4 U5		5.000	EA	4C					
	05	114-0003-0001	CONN 20PIN DUAL 6-AA-02-20-1PX		1.000	EA	4C					
	05	124-0029-0001	MODEL 80 CABLE ASSY	ECO 584 REV G	1.000	EA	4C					
	05	143-0052-0090	MODEL 90 PROBE, OUTSIDE	ECO 722 REV D	1.000	EA	1C					



Nicolet Paratronics

80 Probe 126-0052-0201 Rev. B


-V CLAMP
+V CLAMP
CR1-1
CR2-1
C1-1 5pf
R1-1 665K 1/8W,2%
R2-1 332K 1/8W,2%
CH 1 IN
Q1-1A
Q1-1B
+12V
C3-1 .01
R3-1 100
R4-1 75
R5-1 50
-12V
C4-1 .01
+5V
-5.2V
C6/12 .01
C7 1/12 .01
C5-1/12 .01
U1B
U1A
LE
R8 1K, 1/4W
R6 27 1/4W
C8-1/12 .01
C9 .01
35 CH 1 OUT +
32 CH 1 OUT -
CR1-2
CR2-2
C1-2 5pf
R1-2 665K 1/8W,2%
R2-2 332K 1/8W,2%
CH 2 IN
Q1-2A
Q1-2B
C3-2 .01
R3-2 100
R4-2 75
R5-2 50
C4-2 .01
U1C
U1D
30 CH 2 OUT +
28 CH 2 OUT -
CHANNELS 2&3
CHANNELS 4&5
CHANNELS 6&7
QUAL. & CLK
U2
U3
U4
U5
AM687
CH2 IN 9
CH2 IN 10
CH3 IN 13
CH3 IN 14
CH4 IN 17
CH4 IN 18
CH5 IN 21
CH5 IN 22
CH6 IN 25
CH6 IN 26
CH7 IN 29
CH7 IN 30
QTRIG 33
QTRIG 34
CLK IN 37
CLK IN 38
ALL OTHERS
NC
27 D2+
26 D2-
23 D3-
24 D3+
21 D4+
20 D4-
17 D5-
16 D5+
15 D6+
14 D6-
11 D7-
12 D7+
5 QCLK+
6 QCLK-
2 CLK-
3 CLK+
5 THRESH A
6 THRESH B
Q1 SILCONIX E420
BOTTOM VIEW
+5V
R10 47 1/4 W
R9 47 1/4 W
+V CLAMP (SOURCE) TO CATHODE OF CR2-0 THRU CR2-9
-5V
R11 47 1/4 W
R12 47 1/4 W
-V CLAMP (SOURCE) TO ANODE OF CR1-0 THRU CR1-9
3 ALL DIODES ARE IN3600
2 ALL CAPS ARE IN _ FARRADS
1 ALL RES ARE 1/8 W, 5%
NOTES UNLESS OTHERWISE SPECIFIED
VTHRESH A FOR CHP.1,2,3,QUAL+CLK
VTHRESH B FOR CH 4+7
+12V SOURCE
-12V SOURCE
+5V SOURCE
THRESH. A
THRESH B
+12V
-12V
+5V IN
+5V IN
C10 33 6V TANT
.01
-5.2V SOURCE
-5.2V
-5.2V
C11 33 6V TANT
.01
J6
J6
PARATRONICS INC.
SCHEMATIC DIAGRAM
Model 80 Probe
127-0052-001

MOTHERBOARD CONNECTIONS

SECTION 15: MOTHERBOARD CONNECTIONS

SECTION XV
MOTHERBOARD CONNECTIONS

15.1 INTRODUCTION

This section contains the motherboard connector allocations. The connectors on the motherboard are denoted from front to rear as A through K. The plug-in PC boards associated with these connectors are as follows:

A. Processor
B. RAM Disk
C. State Control
D. State Memory C (LSB)
E. State Memory A (MSB)
F. State Memory B
G. Timing Control
H. Timing Memory A
I. Timing Memory B
J. Waveform
K. Counter-Timer/SA

Interboard Signals. S1 Connections (Less Power & Ground)

Signal Name	Board and Pin Connections
ALE	S1A-50, S1B-50, S1C-50, S1D-50, S1E-50, S1F-50, S1G-50, S1H-50, S1I-50, S1J-50, S1K-50
A00	S1A-55, S1B-55, S1C-55, S1D-55, S1E-55, S1F-55, S1G-55, S1H-55, S1I-55, S1J-55, S1K-55
A01	S1A-24, S1B-24, S1C-24, S1D-24, S1E-24, S1F-24, S1G-24, S1H-24, S1I-24, S1J-24, S1K-24
A02	S1A-58, S1B-58, S1C-58, S1D-58, S1E-58, S1F-58, S1G-58, S1H-58, S1I-58, S1J-58, S1K-58
A03	S1A-28, S1B-28, S1C-28, S1D-28, S1E-28, S1F-28, S1G-28, S1H-28, S1I-28, S1J-28, S1K-28
A04	S1A-23, S1B-23, S1C-23, S1D-23, S1E-23, S1F-23, S1G-23, S1H-23, S1I-23, S1J-23, S1K-23
A05	S1A-25, S1B-25, S1C-25, S1D-25, S1E-25, S1F-25, S1G-25, S1H-25, S1I-25, S1J-25, S1K-25
A06	S1A-56, S1B-56, S1C-56, S1D-56, S1E-56, S1F-56, S1G-56, S1H-56, S1I-56, S1J-56, S1K-56
A07	S1A-57, S1B-57, S1C-57, S1D-57, S1E-57, S1F-57, S1G-57, S1H-57, S1I-57, S1J-57, S1K-57
A08	S1A-52, S1B-52, S1C-52, S1D-52, S1E-52, S1F-52, S1G-52, S1H-52, S1I-52, S1J-52, S1K-52
A09	S1A-53, S1B-53, S1C-53, S1D-53, S1E-53, S1F-53, S1G-53, S1H-53, S1I-53, S1J-53, S1K-53
A10	S1A-54, S1B-54, S1C-54, S1D-54, S1E-54, S1F-54, S1G-54, S1H-54, S1I-54, S1J-54, S1K-54
A11	S1A-27, S1B-27, S1C-27, S1D-27, S1E-27, S1G-27, S1H-27, S1J-27, S1K-27, U7-9
A12	S1A-26, S1B-26, S1G-26, S1H-26, S1I-26, S1J-26, S1K-26
A13	S1A-44, S1B-44, S1G-44, S1J-44, S1K-44, U7-11
A14	S1A-14, S1B-14, S1G-14, S1H-14, S1I-14, S1J-14, S1K-14
A15	S1A-45, S1B-45, S1G-45, S1K-45, U7-13
A13-	S1C-44, S1D-44, S1E-44, S1F-44, S1H-44, S1I-44, U7-10, RP3-6
A11-	S1F-27, S1I-27, U7-8, RP3-8
A15-	S1C-45, S1D-45, S1E-45, S1F-45, S1H-45, S1I-45, S1J-45, U7-12, RP3-4
A14-	S1C-14, S1D-14, S1E-14, S1F-14
A12-	S1C-26, S1D-26, S1E-26, S1F-26
CLK	S1A-11, S1B-11, S1C-11, S1D-11, S1E-11, S1F-11, S1G-11, S1H-11, S1I-11, S1J-11, S1K-11
DB0	S1A-48, S1B-48, S1C-48, S1D-48, S1E-48, S1F-48, S1G-48, S1H-48, S1I-48, S1J-48, S1K-48, U1-3
DB1	S1A-49, S1B-49, S2C-49, S1D-49, S1E-49, S1F-49, S1G-49, S1H-49, S1I-49, S1J-49, S1K-49, U1-18
DB2	S1A-19, S1B-19, S1C-19, S1D-19, S1E-19, S1F-19, S1G-19, S1H-19, S1I-19, S1J-19, S1K-19, U1-14
DB3	S1A-17, S1B-17, S1C-17, S1D-17, S1E-17, S1F-17, S1G-17, S1H-17, S1I-17, S1J-17, S1K-17, U1-13
DB4	S1A-18, S1B-18, S1C-18, S1D-18, S1E-18, S1F-18, S1G-18, S1H-18, S1I-18, S1J-18, S1K-18, U1-8
DB5	S1A-20, S1B-20, S1C-20, S1D-20, S1E-20, S1F-20, S1G-20, S1H-20, S1I-20, S1J-20, S1K-20, U1-7
DB6	S1A-51, S1B-51, S1C-51, S1D-51, S1E-51, S1F-51, S1G-51, S1H-51, S1I-51, S1J-51, S1K-51, U1-4
DB7	S1A-21, S1B-21, S1C-21, S1D-21, S1E-21, S1F-21, S1G-21, S1H-21, S1I-21, S1J-21, S1K-21, U1-17
DBEN+	S1A-22, S1B-22, S1C-22, S1D-22, S1E-22, S1F-22, S1G-22, S1H-22, S1I-22, S1J-22, S1K-22
HLDA	S1A-7, S1B-7, S1C-7, S1D-7, S1E-7, S1F-7, S1G-7, S1H-7, S1I-7, S1J-7, S1K-7
HOLD	S1A-39, S1B-39, S1C-39, S1D-39, S1E-39, S1F-39, S1G-39, S1H-39, S1I-39, S1J-39, S1K-39

Interboard Signals. S1 Connections (Less Power & Ground)

Signal Name	Board and Pin Connections
INTA-	S1A-37, S1B-37, S1C-37, S1D-37, S1E-37, S1F-37, S1G-37, S1H-37, S1I-37, S1J-37, S1K-37
INTR	S1A-13, S1B-13, S1C-13, S1D-13, S1E-13, S1F-13, S1G-13, S1H-13, S1I-13, S1J-13, S1K-13
IOEN-	S1A-8, S1B-8, S1C-8, S1D-8, S1E-8, S1F-8, S1G-8, S1H-8, S1I-8, S1J-8, S1K-8
IO/M-	S1A-15, S1B-15, S1C-15, S1D-15, S1E-15, S1F-15, S1G-15, S1H-15, S1I-15, S1J-15, S1K-15
RDY	S1A-38, S1B-38, S1C-38, S1D-38, S1E-38, S1F-38, S1G-38, S1H-38, S1I-38, S1J-38, S1K-38
RD-	S1A-59, S1B-59, S1C-59, S1D-59, S1E-59, S1F-59, S1G-59, S1H-59, S1I-59, S1J-59, S1K-59
RST	S1A-10, S1B-10, S1C-10, S1D-10, S1E-10, S1F-10, S1G-10, S1H-10, S1I-10, S1J-10, S1K-10
RST5.5	S1A-43, S1B-43, S1C-43, S1D-43, S1E-43, S1F-43, S1G-43, S1H-43, S1I-43, S1J-43, S1K-43
RST6.5	S1A-12, S1B-12, S1C-12, S1D-12, S1E-12, S1F-12, S1G-12, S1H-12, S1I-12, S1J-12, S1K-12
RST7.5	S1A-42, S1B-42, S1C-42, S1D-42, S1E-42, S1F-42, S1G-42, S1H-42, S1I-42, S1J-42, S1K-42
RW	S1A-9, S1B-9, S1C-9, S1D-9, S1E-9, S1F-9, S1G-9, S1H-9, S1I-9, S1J-9, S1K-9
SID	S1A-40, S1B-40, S1C-40, S1D-40, S1E-40, S1F-40, S1G-40, S1H-40, S1I-40, S1J-40, S1K-40, C6, RP3-2, U7-1, J12-49
SOD	S1A-16, S1B-16, S1C-16, S1D-16, S1E-16, S1F-16, S1G-16, S1H-16, S1I-16, S1J-16, S1K-16
SO	S1A-46, S1B-46, S1C-46, S1D-46, S1E-46, S1F-46, S1G-46, S1H-46, S1I-46, S1J-46, S1K-46
S1	S1A-47, S1B-47, S1C-47, S1D-47, S1E-47, S1F-47, S1G-47, S1H-47, S1I-47, S1J-47, S1K-47
TRAP-	S1A-41, S1B-41, S1C-41, S1D-41, S1E-41, S1F-41, S1G-41, S1H-41, S1I-41, S1J-41, S1K-41, J1-3
WR-	S1A-29, S1B-29, S1C-29, S1D-29, S1E-29, S1F-29, S1G-29, S1H-29, S1I-29, S1J-29, S1K-29, U4-5
SPARE	S1A-34, S1B-34, S1C-34, S1D-34, S1E-34, S1F-34, S1G-34, S1H-34, S1I-34, S1J-34, S1K-34
SPARE	S1A-4, S1B-4, S1C-4, S1D-4, S1E-4, S1F-4, S1G-4, S1H-4, S1I-4, S1J-4, S1K-4

S2 and Power Connections

Signal Name	Board and Pin Connections
ARME-	S2F-9, S2G-38, R7, S2K-9, S2D-9
ARM+	S2D-20, S2E-20, S2F-20, U3-5,6
ARMOUT-	U3-4, J10-5, RP1-4
CLKINH+	S2C-38, S2D-7, S2E-7, S2F-7
CLKSEL2+	U1-2, U4-1, U2-3
CLKSEL2-	U4-2, U2-11, U2-4
CLKSEL3-	U4-4, U2-13
CLKSEL3+	U1-19, U4-3, U2-6
DO1+	S2C-3, S2D-3, S2E-3, S2F-3,
DO2	S2C-33, S2D-33, S2E-33, S2F-33,
EXT	S2D-12, S2E-12, S2F-12, S2G-12, J10-11
EXT1+	U4-10, U3-9
EXT1-	S2A-49, U4-11
FS	S2C-42, U3-3
GND	J2 (4,10) J3-(23,12,14,18,20,22,24,16) J10-(2,4,6,8) J1-(1,2) J10 (10,12,14,16) S1A-(1,30,31,60), S1C-(1,30,31,60), S1D-(1,30,31,60), S1E-(1,30,31,60), S1F-(1,30,31,60), S1K-(1,30,31,60), S2A-(1,19,30,31,60), S2C-(1,30,31,60), S2D-(1,30,31,34,35,36,38,60) S2E-(1,15,30,31,34,35,36,37,38,60) S2F-(1,15,30,31,34,35,36,37,38,60) S1B-(1,30,31,60) S1G-(1,30,31,60) S1H-(1,30,31,60) S1I-(1,30,31,60) S1J-(1,30,31,60) S2G-(1,30,31,60) S2B-(1,30,31,60) S2H-(1,30,31,35,36,60) S2I-(1,30,31,35,36,60) S2J-(1,28,30,31,58,59,60) S2K-(1,30,31,36,40,60) S2K-29 SPK U1-(1,10) U10-(1,16), U11-16

Signal Name	Board and Pin Connections
GND	U7-7, U9-(7,14) U6-(2,3,7,9,10) U2-(7,9,10), U3-7, U4-7, U5-7 R3, R5 J4-(1,7) J12-(1,2,36,72,71,35,107,108) C2, C3, C4, C5, C6, C7, C8, C9
LINK	S2D-11,S1E-11,S2F-11 J10-3, RP1-2, U3-1, U5-(4,11,12,10)
RA0	S2C-16, S2D-46, S2E-46, S2F-46
RA1	S2C-15, S2D-45, S2E-45, S2F-45
RA2	S2C-14, S2D-44, S2E-44, S2F-44
RA3	S2C-13, S2D-43, S2E-43, S2F-43
RA4	S2C-12, S2D-42, S2E-42, S2F-42
RA5	S2C-11, S2D-41, S2E-41, S2F-41
RA6	S2C-10, S2D-40, S2E-40, S2F-40
RA7	S2C-9, S2D-39, S2E-39, S2F-39
RA8	S2D-13, S2E-13, S2F-13, S2C-28
RA9	S2D-32, S2E-32, S2F-32, S2C-29
MAIN/$\overline{\text{AUX}}$	S2D-8, S2E-8, S2F-8, S2C-2
LINK-	RP1-8, S2G-42, S2A-5, U5-13
RDYOUT-	S2A-7, U5-(5,6)
RESTART	S2F-17, S2E-17, S2D-17, S2C-47
SADATAIN	S2K-41, J10-7
TRIG+	S2C-45, S2D-16, S2E-16, S2F-16
TRIGE-	S2F-10, S2G-10, S2K-10, R8, S2D-10
TSA0	S2C-20, S2D-50, S2E-50, S2F-50
TSA1	S2C-19, S2D-49, S2E-49, S2F-49
TSA2	S2C-18, S2D-48, S2E-48, S2F-48
TSA3	S2C-17, S2D-47, S2E-47, S2F-47
WR+	U4-6, U3-8
WR1-	U3-10, U1-11, RP1-5
+15	S2A-(2,32), S2B-(2,32), S2K-(2,32), J2-4 S2H-2, S2H-32 S2I-2, S2I-32, S2J-2, S2J-32 R1 S1G-2, S2G-32, (Optional)
TRIGOUT-	U11-5, J10-1

Signal Name	Board and Pin Connections
+5	C2, C3, C4, C5, C7, C9 J2-(1,2) S1B-(5,6,35,36), S1C-(5,6,35,36), S1D-(5,6,35,36) S1E-(5,6,35,36), S1F-(5,6,35,36), S1K-(5,6,35,36) RP1-1, RP2-1, RP3-1, U1-20, U2-(1,14), U3-14, U4-14, U5-14, U6-(1,14), U7-14 U11-8, J12-(141,142) S1G-(5,6,35,36) S1H-(5,6,35,36) S1I-(5,6,35,36) S1J-(5,6,35,36) S1A-(5,6,35,36), CR1-
+12	S2H-44, S2I-44, J12-24, J12-48
-12	S2I-13, S2H-13, J12-26, J12-4
-15	S2B-(3,33), S2A-3,33, J2-9 S2H-3, S2H-33, S2I-3, S2I-33 S2J-3, S2J-33, S2K-3, S2K-33 (S2G-3, S2G-33 optional)
-5.2	J2-(5,6), C8 S1A-(2,3,32,33) S1B-(2,3,32,33), S1C-(2,3,32,33), S1D-(2,3,32,33), S1E-(2,3,32,33), S1F-(2,3,32,33), S1K-(2,3,32,33) S1J-2, S1J-3, S1J-32, S1J-33 S1I-2, S1I-3, S1I-32, S1I-33 S1G-2, S1G-3, S1G-32, S1G-33 S1H-2, S1H-3, S1H-32, S1H-33 U10-8, U11-8, R6, R7, R8, R4 R2 J12-(143,144)
232TXD	S2B-5, J4-3
232DCD	J4-8, S2B-36
232DSR	S2B-6, J4-4
232DTR	J4-20, S2B-35
232DSR	J4-6, S2B-7
232RXD	J4-2, S2B-38
232CTS	J4-5, S2B-37

Signal Name	Board and Pin Connections
488ATN	J3-21, S2A-29
488DAV	J3-11, S2A-28
488D1	J3-1, S2A-42
488D2	J3-3, S2A-11
488D3	J3-5, S2A-41
488D4	J3-7, S2A-10
488D5	J3-2, S2A-40
488D6	J3-4, S2A-9
488D7	J3-6, S2A-39
488D8	J3-8, S2A-38
488EOI	J3-9, S2A-58
488IFC	S2A-(5,6), J3-17
488NDAC	J3-15, S2A-27
488NRFD	J3-13, S2A-57
488REN	S2A-26, J3-10
488SRQ	J3-19, S2A-59
ACLKSEL	S2C-24, J12-121
ACQ1	S2E-19, U6-12, RP2-6
ACQ2	S2E-18, U6-5, RP2-5
ACTL	S2C-27, J12-119
ADO	S2E-56, J12-89
AD1	S2E-54, J12-91
AD2	S2E-55, J12-90
AD3	S2E-29, J12-84
AD4	S2E-53, J12-92
AD5	S2E-57, J12-88
AD6	S2E-52, J12-93
AD7	S2E-51, J12-94
AD8	S2E-58, J12-87
AD9	S2E-59, J12-86
AD10	S2E-28, J12-85
AD11	S2E-27, J12-83
AD12	S2E-26, J12-82
AD13	S2E-23, J12-79
AD14	S2E-24, J12-80
AD15	S2E-25, J12-81
ALATCHCLK	S2C-4, S2E-4
APROBCLK	S2C-23, J12-122, U2-12
APROBDREN-	S2C-43, S2E-14
AQCLKSEL	S2C-26, J12-120
AQ1 (C)	S2C-25, S2E-21, J12-77
AQ2 (T)	S2E-22, J12-78
BPBSNS+	J12-127, U7-2
BCLKSEL	S2C-56, J12-124
BCQ1	S2F-19, U6-11, RP2-8
BCQ2	S2F-18, U6-6, RP2-7
BCTL	S2C-53, J12-126
BDO	S2F-56, J12-69

Signal Name	Board and Pin Connections
BD1	S2F-54, J12-74
BD2	S2F-55, J12-70
BD3	S2F-29, J12-62
BD4	S2F-53, J12-65
BD5	S2F-57, J12-68
BD6	S2F-52, J12-64
BD7	S2F-51, J12-63
BD8	S2F-58, J12-67
BD9	S2F-59, J12-66
BD10	S2F-28, J12-61
BD11	S2F-27, J12-60
BD12	S2F-26, J12-59
BD13	S2F-23, J12-56
BD14	S2F-24, J12-57
BD15	S2F-25, J12-58
BLATCHCLK	S2C-34, S2F-4
BPROBCLK	S2C-57, U2-5, J12-123
BPROBDREN-	S2C-44, S2F-14
BDCLKSEL	S2C-54, J12-125
BD1 (C)	S2C-55, S2F-21, J12-54
BD2 (T)	S2F-22, J12-55
CCLKDUALIN-	S2D-37, U6-8
CCLKSEL	J12-117, U1-5
CCD1	S2D-19, U6-13, RP2-4
CCD2	S2D-18, U6-4, RP2-3
CCTL	J12-116, U1-15
CD0	S2D-56, J12-109
CD1	S2D-54, J12-111
CD2	S2D-55, J12-110
CD3	S2D-29, J12-100
CD4	S2D-53, J12-112
CD5	S2D-57, J12-106
CD6	S2D-52, J12-113
CD7	S2D-51, J12-114
CD8	S2D-58, J12-105
CD9	S2D-59, J12-104
CD10	S2D-28, J12-101
CD11	S2D-27, J12-102
CD12	SD2-26, J12-103
CD13	S2D-23, J12-97
CD14	S2D-24, J12-98
CD15	S2D-25, J12-99

Signal Name	Board and Pin Connections
CLATCHCLK	U2-8, S2D-4
CPROBCLK	J12-118, U2-2
CPROBDREN-	S2D-14, U1-16
COCLKSEL	J12-115, U1-9
CQ1 (C)	S2D-21, J12-95, U3-(11,12)
CQ1-	RP1-3, U3-13 (Optional)
CQ2 (T)	S2D-22, J12-96
CTAPCLK-	S2D-6, S2C-37
CWE+	S2D-5, S2C-35, S2K-35
AT-	S2H-7, S2G-7, S2I-7,
ACH0+	S2H-52, J12-44
ACH0-	S2H-53, J12-43
ACH1+	S2H-54, J12-42
ACH1-	S2H-55, J12-41
ACH2+	S2H-56, J12-40
ACH2-	S2H-57, J12-39
ACH3+	S2H-58, J12-38
ACH3-	S2H-59, J12-37
ACH4+	S2H-29, J12-34
ACH4-	S2H-28, J12-33
ACH5+	S2H-27, J12-32
ACH5-	S2H-26, J12-31
ACH6+	S2H-25, J12-30
ACH6-	S2H-24, J12-29
ACH7+	S2H-23, J12-28
ACH7-	S2H-22, J12-27
ACLK+	S2G-56, J12-51
ACLK-	S2G-55, J12-50
ACT	S2H-6, S2G-6, S2J-6, S2K-6, S2C-36, U8-1, U10-5, R6, R5
ACLKTTL	S2H-43, S2G-43
HYSTERYSIS A	S2H-15, J12-46
A THRESHOLD A	S2H-14, J12-45
A THRESHOLD B	S2H-45, J12-47
HYSTERYSIS B	S2I-15, J12-7
B THRESHOLD A	S2I-14, J12-5
B THRESHOLD B	S2I-45, J12-6
AOCLK+	S2G-58, J12-53
AOCLK-	S2G-57, J12-52
BCH0+	S2I-52, J12-23
BCH0-	S2I-53, J12-22
BCH1+	S2I-54, J12-21

Signal Name	Board and Pin Connections
BCH1-	S2I-55, J12-20
FT+	S2G-11, U5-8
BCH2+	S2I-56, J12-16
BCH2-	S2I-57, J12-17
BCH3+	S2I-58, J12-18
BCH3-	S2I-59, J12-19
BCH4+	S2I-29, J12-15
BCH4-	S2I-28, J12-14
BCH5+	S2I-27, J12-13
BCH5-	S2I-26, J12-12
BCH6+	S2I-25, J12-11
BCH6-	S2I-24, J12-10
BCH7+	S2I-23, J12-9
BCH7-	S2I-22, J12-8
100 MHz	S2A-35, U7-5
BCLKTTL	S2I-43, U11-4
BCT	S2I-6, U7-13, U8-14, U10-13
TT-	S2H-8, S2G-8, S2I-8, U11-7
WD0	S2H-21, S2J-21
WD1	S2H-51, S2J-51
WD2	S2H-20, S2J-20
WD3	S2H-50, S2J-50
WD4	S2H-19, S2J-19
WD5	S2H-49, S2J-49
WD6	S2H-18, S2J-18
WD7	S2H-48, S2J-48
WFIN	S2J-29, J10-13
WTRIG	S2G-40, S2J-40
-T/S	NC On S2K-28
KD6	S2A-17, J1-6
KD5	S2A-47, J1-7
KD4	S2A-16, J1-8
KD3	S2A-46, J1-9
KD2	S2A-15, J1-10
KD1	S2A-45, J1-11
KD0	S2A-14, J1-12
DAAP	S2A-44, J1-4
STRB	S2A-48, J1-13
BEEP+	S2A-6, U7-3
REBOOT	S2A-51, J1-3

Circuit Connections

1. U2-11, U2-4
2. U4-10, U3-9
3. U4-6, U3-8
4. U3-10, U1-11, RP1-5
5. U9-1, U10-15
6. U1-2, U4-1
7. U1-19, U4-3
8. U11-1, U11-6
9. U9-6, R3, R4
10. U1-6, U3-2
11. U1-12, U5-9
12. C1+, R1-2
13. U7-4, R1-1
14. U11-2, U11-1
15. U10-2, U8-8
16. U10-12, U10-9, U10-11, U10-4
17. U10-5, R6, R5
18. U7-2, J12-127

GLOSSARY

SECTION 16: GLOSSARY