SmartMC ™ II Modem Codec

Host-Processed, V.90/K56flex™ Modem Codec (MC) Device Set with Host Side Device (11246) and SmartDAA™ (20463) for AC-link (AC'97 2.1) Applications

The Conexant™ SmartMC II V.90/K56flex™ Modem Codec (MC) Device Set with SmartDAA technology supports analog data up to 56 kbps, analog fax to 14.4 kbps, voice/telephone answering machine (TAM), and AC-link (AC'97) interface operation. The modem operates with PSTN telephone lines in the U.S. and world-wide. Table 1 lists the available models.

The SmartMC II™ MC with AC-link interface supports Audio/Modem Riser (AMR), Mobile Daughter Card (MDC), and Mini PCI interfaces for applications such as embedded/plug-in modems.

Conexant's SmartDAA technology (patent pending) eliminates the need for a costly line transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations. The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling world-wide homologation of a single modem board design.

The SmartDAA system side powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost for world-wide support.

For over a decade, Conexant has assisted customers with DAA technology and homologation. This expertise and system level approach has been leveraged in this product.

The SmartMC II device set, consisting of an 11246 Host Side Device (HSD) in a 48-pin TQFP and a 20463 Line Side Device (LSD) (SmartDAA device) in a 32-pin TQFP, supports data/fax/voice/TAM and DAA (Digital Access Arrangement)/telephone line interface functions (Figure 1). Figure 2 identifies the major hardware signal interfaces. Figure 3 identifies typical supported MC configurations.

Audio recording and playback over the telephone line interface using A-Law, μ-Law, or linear coding at 8 kHz sample rate supports applications such as remote digital telephone answering machine (TAM).

Distinguishing Features

- V.90 data/V.17 fax soft modem, MMX optimized
- SmartDAA technology
  - Eliminates many costly traditional DAA discrete components
  - Reduces modem and DAA board footprint
  - Allows a single modem board design to be approved for world-wide shipments
  - Line-in-use detection
  - Remote hangup detection
  - Extension off-hook detection
  - Wake-up on ring for primary/secondary codec
- Telephony/voice/TAM
- Supports Conexant RipTide D7400/D7300 controllers and selected AC'97-compliant core logic
- Supports soft speakerphone using WDM drivers
- Data/Fax/Voice call discrimination
- World-class operation (optional)
- Industry standard communication commands
- AC-link (AC'97 2.1 compatible) host interface
  - Single line Data/Fax/Voice/TAM modem codec
  - Operable as a primary or a secondary codec
  - Supports AMR, MDC, and Mini PCI host interface
  - Sleep current less than 1 mA
- System compatibilities
  - Windows Driver Model (WDM)
  - Windows 95/98, Windows NT 4.0, Windows 2000
  - Microsoft PC 98 and PC 99 compliant
  - Advanced Power Management (APM and ACPI)
- V.80 synchronous access
- +3.3V operation with +5V tolerant digital inputs

Applications

- Primary or secondary modem AMR and MDC card
- Speakerphone using Conexant audio products
- Embedded/plug-in Mini PCI modems

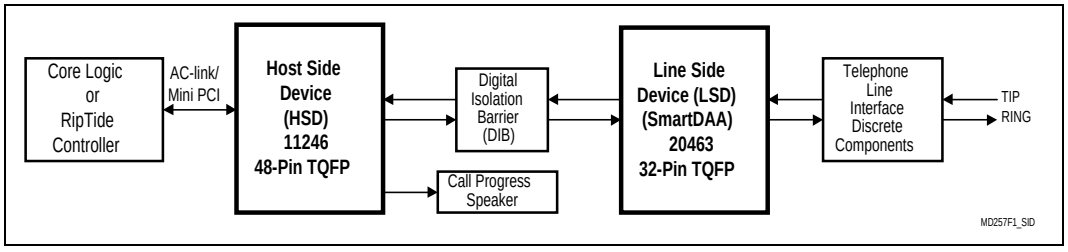


Figure 1. SmartMC II Devices and Major Signal Interfaces

Table 1. SmartMC II Models and Functions

Model/Order/Part Numbers				Supported Functions		
Marketing No.*	Device Set Order No.	Host Side Device (HSD) [48-Pin TQFP] Part No.	Line Side Device (LSD) (SmartDAA) [32-Pin TQFP] Part No.	Ultra-Low Power Operation	V.90/K56flex Data, V.17 Fax, Voice/TAM, Basic Audio Software	World-wide
SmartMC II/L	DSAC-L200-001	11246-12	20463-12	Y	Y	—
SmartMC II/WL	DSAC-L300-201	11246-12	20463-11	Y	Y	Y

Notes:
1. Model options:
   - W World-wide
   - L Ultra low power
2. Supported functions (Y = Supported; – = Not supported):
   - Voice/TAM Telephone answering machine (Voice playback and record through telephone line)

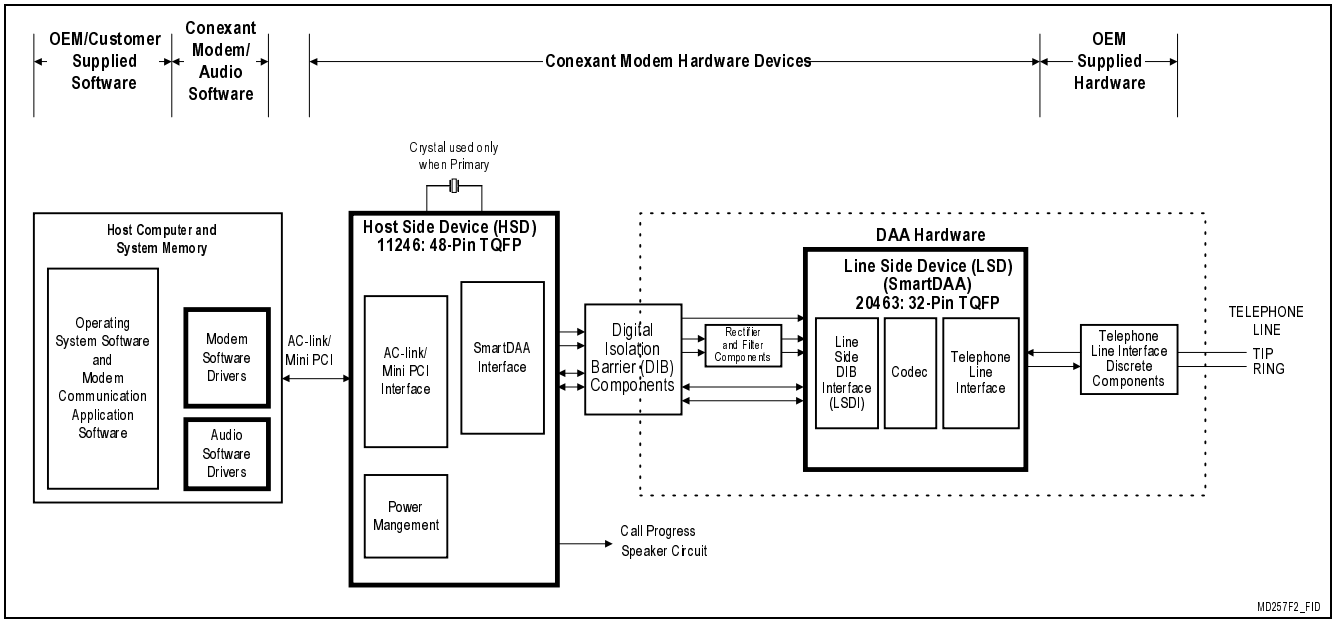


Figure 2. SmartMC II Major Interfaces

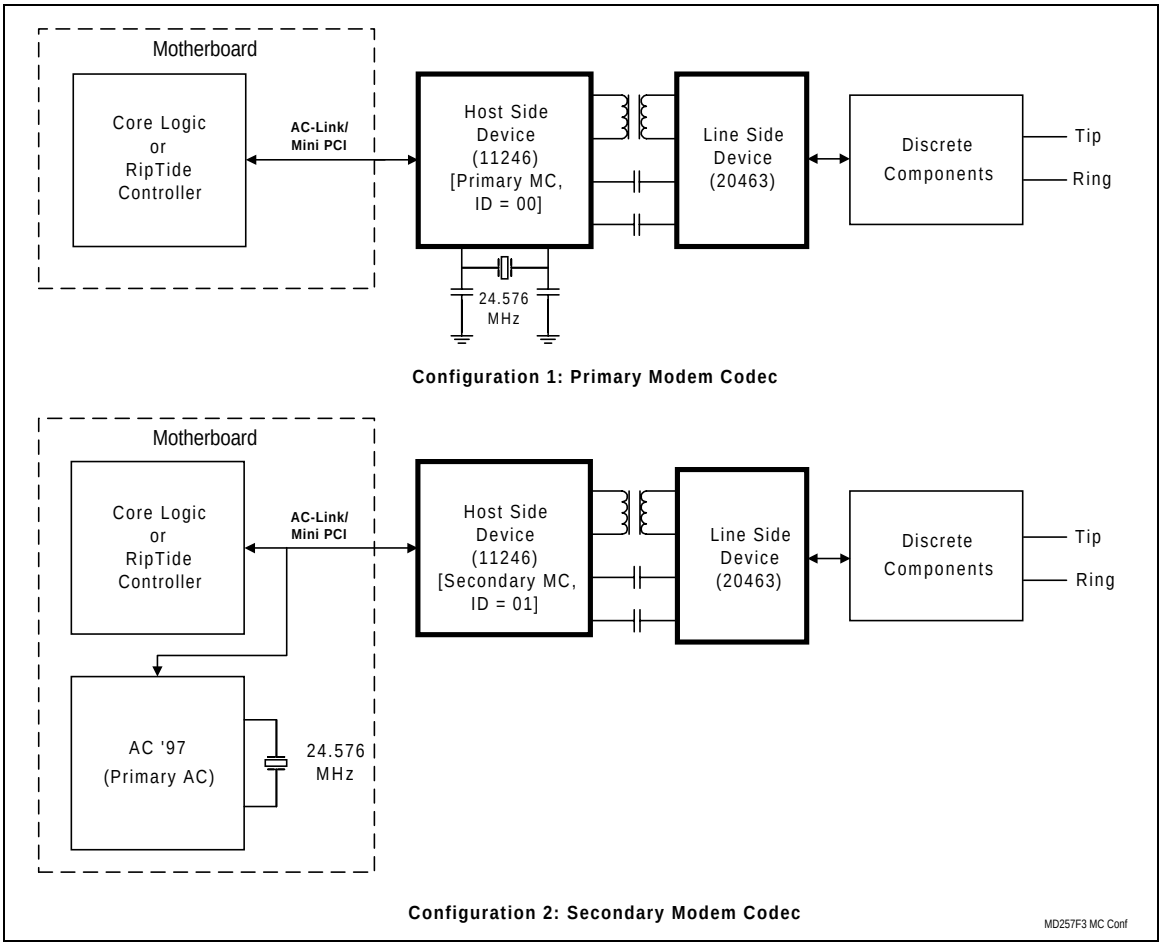


Figure 3. Typical Supported MC Configurations

Detailed Features

General Modem Features

- V.90 data modem with receive rates up to 56 kbps and send rates up to V.34 rates
  - ITU-T V.90, K56flex, V.34 (33.6 kbps), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - V.250 (ex V.25 ter) and V.251 (ex V.25 ter Annex A) commands
- V.17 fax modem with send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 ch 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0 commands
- Telephony/Voice/TAM
  - V.253 commands
  - 8-bit μ-Law/A-Law coding (G.711)
  - 8-bit/16-bit linear coding
  - 8 kHz sample rate
  - Concurrent DTMF detect, ring detect and caller ID
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- V.8/V.8bis and V.251 (ex V.25 ter Annex A) commands
- Data/Fax/Voice call discrimination
- Host software-based signal processing
- Single configuration profile stored in host
- World-Class (W model)
  - Complies to TBR21 and other country requirements
  - Caller ID detection
- System compatibilities
  - Windows Driver Model (WDM)
  - Windows 95/98 operating system
  - Windows NT 4.0, Windows 2000 operating systems
  - Microsoft PC 98 and PC 99 Design Initiative compliant
  - Advanced Power Management (APM and ACPI)
  - Unimodem/V compliant
  - Pentium 166 MMX MHz-compatible or greater
  - 32 Mbyte RAM or more
- Thin packages support low profile designs (1.6 mm max. height)
  - HSD (11246): 48-pin TQFP
  - LSD (20463): 32-pin TQFP
- +3.3V operation with +5V tolerant digital inputs

AC-link (AC'97) Host Interface Features

- Operates as a single-line Data/Fax/Voice/TAM modem
- AC'97 rev 2.1 compatible codec with the LSD and DIB (uses protocol slot 5 and 12)
- Uses +3.3VSB for power management mode
- Wake-on-ring in primary and secondary codec
- Sleep current: 1 mA typical
- Supports Conexant RipTide D7400/D7300 controllers and selected AC'97-compliant core logic
- Supports soft speakerphone using WDM drivers
- Operable as either a primary or a secondary codec selected by external pin configuration.
  - BIT_CLK is the input bit clock input in secondary codec operation
  - BIT_CLK is the output bit clock (derived from external crystal) in primary codec operation
- Supports Power Management
  - ACPI Power Management Registers
  - APM support
  - Wake-on ring in D3cold

SmartDAA Features

- System side powered DAA operates under poor line current supply conditions
- Wake-on-ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Pulse dialing
- Line-in-use detection – detects even while on-hook
- Remote hang-up detect – for efficient call termination
- Extension pickup detect
- Handset exclusion (patent pending)
- Call waiting detection
- Digital PBX line protection
- Meets world-wide DC VI Masks requirements (W model)

Description

General

Modem operation, including dialing, call progress, telephone line interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host processor via an AC-link interface. The OEM adds a 24.576 MHz crystal circuit if Primary MC operation is required, optional digital speaker circuit, DIB components, LSD power rectifier and filter components, telephone line interface components, control straps, and other supporting discrete components as required and supported by the model to complete the system.

Host Modem Software

The host modem software performs the following tasks:

1. General modem control, which includes command sets, fax Class 1, voice/TAM, speakerphone through Conexant WDM driver or RipTide configuration, error correction, data compression, and operating system interface functions.
2. Modem data pump signal processing, which includes data and facsimile modulation and demodulation, as well as voice/TAM sample formatting.
3. SmartDAA control, which includes HSD SmartDAA Interface control, LSD configuration and control, telephone interface parameter control, and telephone line impedance control.

Configurations of the modem software are provided to support modem models listed in Table 1.

Data/Fax Modes

As a V.90/K56flex data modem, the modem can receive data from a digitally connected central site modem (CSM) at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data up to V.34 rates. This mode can fallback to full-duplex V.34 mode, and to lower rates as dictated by line conditions.

As a V.34 data modem, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the fax EIA/TIA-578 Class 1 and T.31 Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

Synchronous Access Mode (SAM) - Video Conferencing

V.80 synchronous access mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

Voice/TAM Mode

Voice/TAM Mode features include 8-bit μ-Law, A-Law, and linear coding at 8 kHz sample rates. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

Voice/TAM Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or, for speakerphone configuration, to a microphone/speaker.
2. Voice Receive Mode supports recording voice or audio data input from the telephone line or, for speakerphone configuration, from a microphone.
3. Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for speakerphone configuration, to a speaker.
4. Full-duplex voice supports concurrent voice receive and transmit.

Reference Design

An AMR data/fax/voice/TAM/handset exclusion reference design card and an MDC data/fax/voice/TAM reference design card are available to minimize application design time and costs.

The card is pretested to pass FCC Part 15, Part 68, and TBR 21.

A design package is available in electronic form. The design package includes schematics, bill of materials (BOM), vendor parts list (VPL), board layout files in Gerber format, and complete documentation.

The reference designs are production ready for immediate manufacturing. The design can also be used for the basis of a custom design by the OEM to accelerate design completion for rapid market entry.

Hardware Description

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in world-wide markets by eliminating the need for country-specific components.

Host Side Device (HSD)

The HSD serves as an AC'97 2.1 -compatible modem codec (MC) packaged in a 48-pin TQFP. It can function as a primary or secondary AC-link codec as selected by the ID0#, ID1#, and PRIMARY_DN pins. As a primary codec, it uses an attached 24.576 MHz crystal to generate internal clocks and produce the 12.288 MHz AC-link bit clock (BIT_CLK). As a secondary codec, it uses an incoming 12.288 MHz BIT_CLK signal to generate its internal clocks.

Internal functions include an AC-link (AC'97) Interface, Power Management Interface, Caller ID Detection, and a SmartDAA Interface.

The AC-link Interface connects directly to core logic or a PCI-based controller, typically through an AMR, MDC, or Mini PCI connector.

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

Digital Isolation Barrier (DIB) (OEM Supplied)

The DIB electrically DC isolates the HSD from the LSD and telephone line. The HSD is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB power and clock transformer (PCXFMR) couples power and clock from the HSD to the LSD.

The DIB data channel supports bidirectional serial transfer of data, control, and status information between the HSD and the LSD.

Line Side Device (LSD)

The LSD includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the HSD through the DIB.

LSD power is received from the DIB PCXFMR secondary winding through a half-wave rectifying diode and capacitive power filter circuit. The CLK input is also accepted from the PCXFMR secondary winding through a capacitor and a resistor in series. The LSD DGND is referenced to the bottom of the PCXFMR secondary winding.

Information is transferred between the LSD and the HSD through the DIB_P and DIB_N pins. These pins connect to the HSD DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and world-wide regulations and to actively control the DAA power dissipation.

HSD (11246) Hardware Pins and Signals

General

AC-link Host Interface

The AC-link host interface conforms to AC'97 rev 2.1 compatible for a single line Data/Fax/Voice/TAM only modem codec.

The supported AC-link signals are:

- Bit Clock (BIT_CLK), input/output
- Frame Sync (SYNC), input
- Serial Data Output (SDATA_OUT), input
- Serial Data Input 0 (SDATA_IN0), input/output
- Serial Data Input 1 (SDATA_IN1), output
- AC '97 Master Hardware Reset (AC_RESET#), input

Control Signals

Control signals from straps or the host are:

- Primary Down (PRIMARY_DN), input
- Mux Enable (MUX_EN), input
- Codec ID (ID0# and ID1#); input
- Sub Assembly ID (SUBID[3:0]); input

LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Plus (PWRCLKP); output
- Clock and Power Minus (PWRCLKN); output
- Data Plus (DIB_DATAP); input/output
- Data Minus (DIB_DATAN); input/output

Digital Speaker Interface

The digital speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode which can be optionally connected to an AC'97 audio device to enable playback of call progress through the analog mixer in the AC'97 device. The DSPKOUT output can be also be connected to a low-cost on-board speaker, e.g., a sounducer, without the use of an external op-amp.

Pin Assignments and Signal Definitions

The HSD (11246) 48-pin TQFP hardware interface signals are shown by major interface in Figure 4, are shown by pin number in Figure 5, and are listed by pin number in Table 2.

The HSD (11246) hardware interface signals are defined in Table 3.

The HSD (11246) digital characteristics are defined in Table 4.

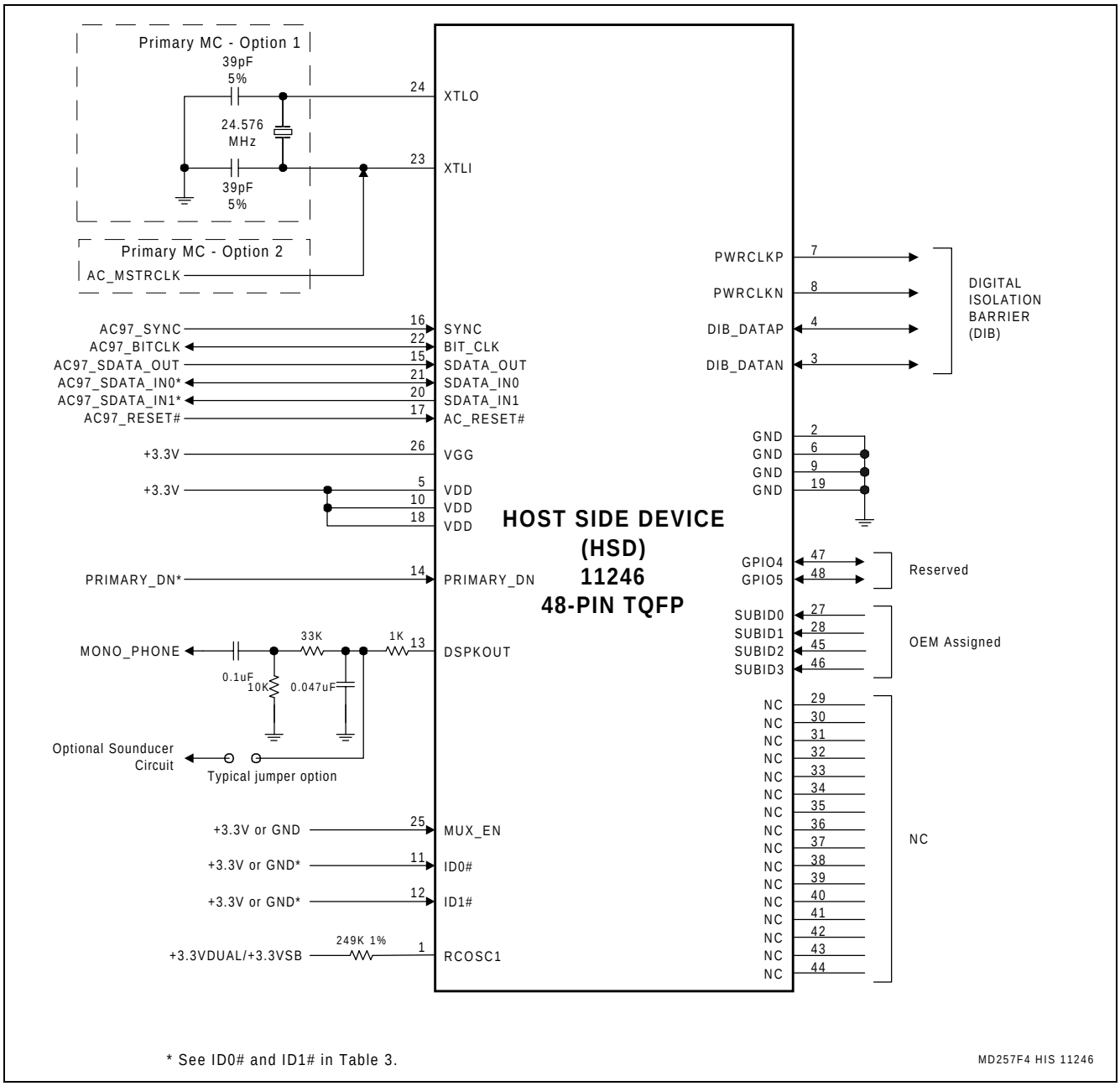


Figure 4. HSD (11246) 48-Pin TQFP Hardware Interface Signals

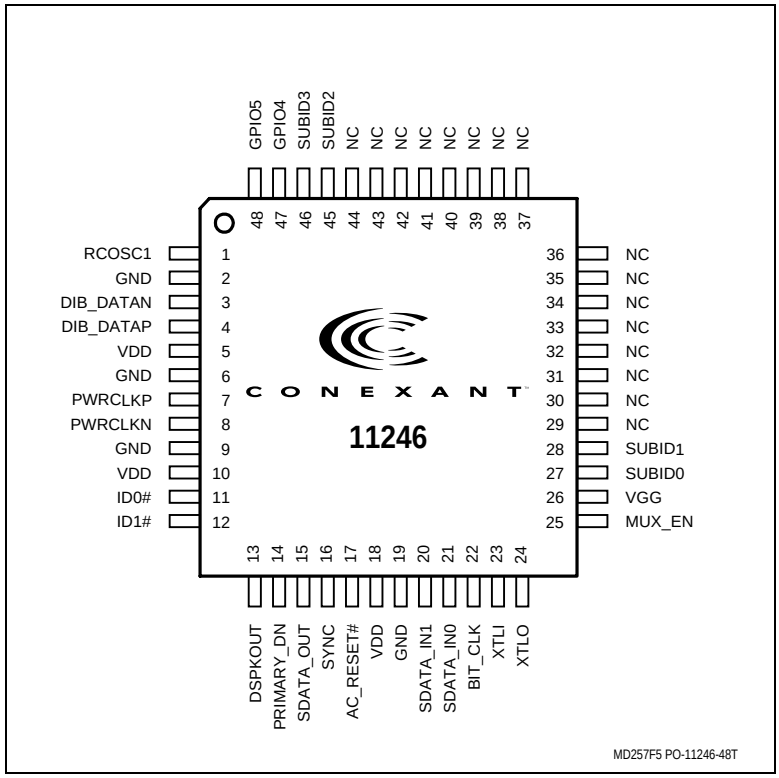


Figure 5. HSD (11246) 48-Pin TQFP Pin Signals

Table 2. HSD (11246) 48-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	RCOSC1		+3.3Vdual through 249 KΩ, 1%	25	MUX_EN	It	GND
2	GND	GND	GND	26	VGG	REF	+3.3V
3	DIB_DATAN	Idd/Odd	DIB: Data Negative Channel capacitor	27	SUBID0	It	Sub Assembly ID 0
4	DIB_DATAP	Idd/Odd	DIB: Data Positive Channel capacitor	28	SUBID1	It	Sub Assembly ID 1
5	VDD	PWR	+3.3V	29	NC		NC
6	GND	GND	GND	30	NC		NC
7	PWRCLKP	Odpc	DIB: PCXFMR Primary Top Winding	31	NC		NC
8	PWRCLKN	Odpc	DIB: PCXFMR Primary Bottom Winding	32	NC		NC
9	GND	GND	GND	33	NC		NC
10	VDD	PWR	+3.3V	34	NC		NC
11	ID0#	It	See ID0# and ID1# in Table 3	35	NC		NC
12	ID1#	It	See ID0# and ID1# in Table 3	36	NC		NC
13	DSPKOUT	Ot2	AI: Digital Speaker	37	NC		NC
14	PRIMARY_DN	It	See ID0# and ID1# in Table 3	38	NC		NC
15	SDATA_OUT	Iac	AC-link: AC97_SDATA_OUT	39	NC		NC
16	SYNC	Iac	AC-link: AC97_SYNC	40	NC		NC
17	AC_RESET#	Iac	AC-link: AC97_RESET	41	NC		NC
18	VDD	PWR	+3.3V	42	NC		NC
19	GND	GND	GND	43	NC		NC
20	SDATA_IN1	Oac	See ID0# and ID1# in Table 3	44	NC		NC
21	SDATA_IN0	Iac/Oac	See ID0# and ID1# in Table 3	45	SUBID2	It	Sub Assembly ID 2
22	BIT_CLK	Iac/Oac	AC-link: AC97_BITCLK	46	SUBID3	It	Sub Assembly ID 3
23	XTLI	Ix	For Primary MC, 24.576 MHz crystal circuit or clock oscillator circuit (AC_MSTRCLK). For Secondary MC, can be NC.	47	GPIO4	It/Ot12	NC
24	XTLO	Ox	For Primary MC, 24.576 MHz crystal circuit, or leave open if XTLI is connected to clock circuit. For Secondary MC, can be NC.	48	GPIO5	It/Ot12	NC

1. I/O types:

Iac	Digital input, AC-link-compatible, C_{IN} = 50 pF (see Table 4)
Iac/Oac	Digital input, AC-link-compatible, C_{IN} = 50 pF/Digital output, AC-link-compatible (see Table 4)
Idd/Odd	DIB data input/DIB data output
It	Digital input, TTL-compatible
Ix	Crystal input
Oac	Digital output, AC-link-compatible (see Table 4)
Odpc	DIB power and clock output
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ox	Crystal input

2. Interface Legend:

DIB	Digital Interface Barrier
NC	No external connection

Table 3. HSD (11246) 48-pin TQFP Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
System			
VDD	5, 10, 18	PWR	**Digital Supply Voltage.** Connect to +3.3V.
GND	2, 6, 9, 19	GND	**Digital Ground.** Connect to digital ground.
XTLI	23	Ix	**Crystal In/Clock In.** For Primary MC, connect to 24.576 MHz crystal circuit or clock oscillator circuit (AC_MSTRCLK). For Secondary MC, pins can be left open.
XTLO	24	Ox	**Crystal Out.** For Primary MC, connect to 24.576 MHz crystal circuit, or leave open if XTLI is connected to clock circuit. For Secondary MC, pins can be left open.
VGG	26	REF	**Reference Voltage.** Connect to +3.3V.
MUX_EN	25	It	**Mux Enable.** Connect to +3.3V (High) or GND (Low). High defines SDATA_IN0 as an input for use when the SmartMC is a Secondary MC. In this case, the Smart MC multiplexes the AC'97 audio input data on SDATA_IN0 with the internal modem data, then outputs the data on SDATA_IN1.
ID0# ID1#	11 12	It It	**Codec ID.** Used in conjunction with PRIMARY_DN to select modem codec operation as a primary or secondary codec, as follows and shown in Figure 6: **For a Modem-Only Riser Card:** 1. Connect PRIMARY_DN to GND. 2. Connect SDATA_IN0 to AC-link AC97_SDATA_IN0 through 33 Ω. 3. Connect SDATA_IN1 to AC-link AC97_SDATA_IN1 through 33 Ω. 4. Connect ID0# to AMR PRIMARY_DN. 5. Leave ID1# open. If PRIMARY_DN is low (codec is present on the motherboard), the ID is internally set to 01 for secondary codec operation and SDATA-IN1 is used. If PRIMARY_DN is high (codec is not present on the motherboard), the ID is internally set to set to 00 for primary codec operation and SDATA-IN0 is used. **For an MDC Board:** 1. Connect PRIMARY_DN to MDC PRIMARY_DN. 2. Connect SDATA_IN0 to SDATA_IN1. 3. Connect SDATA_IN0 or SDATA_IN1 to motherboard SDATA_IN through 33 Ω. 4. Leave ID0# open. 5. Leave ID1# open. The MDC SDATA_INA signal should be used whether or not there is a primary codec. PRIMARY_DN is high when audio codec is on the motherboard. **For a Modem-Only Mini PCI Board:** 1. Connect PRIMARY_DN to GND. 2. Connect SDATA_IN0 to SDATA_IN1. 3. Connect SDATA_IN0 to SDATA_IN1 to motherboard SDATA_IN through 33 Ω. 4. Connect ID0# to Mini PCI Codec_ID0#. 5. Connect ID1# to Mini PCI Codec_ID1#.
SUBID0 SUBID1 SUBID2 SUBID3	27 28 45 46	It It It It	**Sub Assembly ID 0.** Connect to GND or +3.3V as defined by the OEM. **Sub Assembly ID 1.** Connect to GND or +3.3V as defined by the OEM. **Sub Assembly ID 2.** Connect to GND or +3.3V as defined by the OEM. **Sub Assembly ID 3.** Connect to GND or +3.3V as defined by the OEM.
RCOSC1	1		**RC Circuit 1.** Connect to +3.3VDUAL/+3.3VSB through 249 KΩ 1%.
GPIO4 GPIO5	47 48	It/Ot12	**General Purpose I/O.** Reserved. If unused, connect to GND or +3.3V.

Table 3. HSD (11246) 48-pin TQFP Pin Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
PWRCLKP	7	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD**.** Connect to the top of the DIB power and clock transformer (PCXFMR) primary winding.
PWRCLKN	8	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD**.** Connect to the bottom of the DIB power and clock transformer (PCXFMR) primary winding.
DIB_DATAP	4	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the HSD and LSD**.** Connect to the LSD through DIB data positive channel components.
DIB_DATAN	3	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the HSD and LSD. Connect to the LSD through DIB data negative channel components.
AC-link and AMR/MCD Interface			
BIT_CLK	22	Iac/Oac	**Bit Clock**. 12.288 MHz serial data output bit clock derived from a 24.576 MHz external crystal circuit when the MC is configured as a primary codec. 12.288 MHz serial data input bit clock when the MC is configured as a secondary codec. Connect to AC97_BITCLK.
SYNC	16	Iac	**Frame Sync.** 48 kHz fixed rate sample AC-link sync input. Synchronization pulse from an AC'97 compliant controller to all of the AC'97 compliant codecs on the link. This signal is nominally 1.3 µs wide pulse that is used to synchronize the AC-link. Reset state = low. Standard load = 50 pF. Connect to AC97_SYNC.
SDATA_OUT	15	Iac	**Serial Data Output.** Serial, time division multiplexed, input data stream from an AC'97 controller. Reset state = low. Standard load = 50 pF. Connect to AC97_SDATA_OUT through 33 Ω.
SDATA_IN0	21	Iac/Oac	**Serial Data Input 0.** Serial, time division multiplexed, input/output data stream. Output data stream to an AC'97 controller when the SmartMC II is a Primary MC. Input data stream from an AC'97 controller when the SmartMC II is a Secondary MC. See ID0# and ID1# description in this table and Figure 6. Connect to AC97_SDATA_ IN0 through 33 Ω.
SDATA_IN1	20	Oac	**Serial Data Input 1.** Serial, time division multiplexed, output data stream to an AC'97 controller when the SmartMC II is a Secondary MC. See ID0# and ID1# description in this table and Figure 6. Connect to AC97_SDATA IN1 through 33 Ω.
AC_RESET#	17	Iacl	**AC '97 Master Hardware Reset.** Active low reset. Reset state = low. Standard load = 50 pF. Connect to AC97_RESET.
PRIMARY_DN	14	It	**Primary Down**. Used in conjunction with ID0# and ID1# to select modem codec operation as a primary or secondary codec. See ID0# and ID1# description in this table and Figure 6.
DSPKOUT	13	Ot12	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator. Connect to the MONO_PHONE signal through a filter circuit and optionally to an on-board speaker circuit, e.g., sounducer. The DSPKOUT output is used for call progress monitoring.
Not Used			
NC	29-47		**No Connect**. No internal connection.

Notes:

1. I/O types:
   - Iac — Digital input, AC-link-compatible, C_{IN} = 50 pF (see Table 4)
   - Iac/Oac — Digital input, AC-link-compatible, C_{IN} = 50 pF/Digital output, AC-link-compatible (see Table 4)
   - Idd/Odd — DIB data input/DIB data output
   - It — Digital input, TTL-compatible
   - Ix — Crystal input
   - Oac — Digital output, AC-link-compatible (see Table 4)
   - Odpc — DIB power and clock output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - Ox — Crystal input
2. Interface Legend:
   - DIB — Digital Interface Barrier
   - NC — No external connection

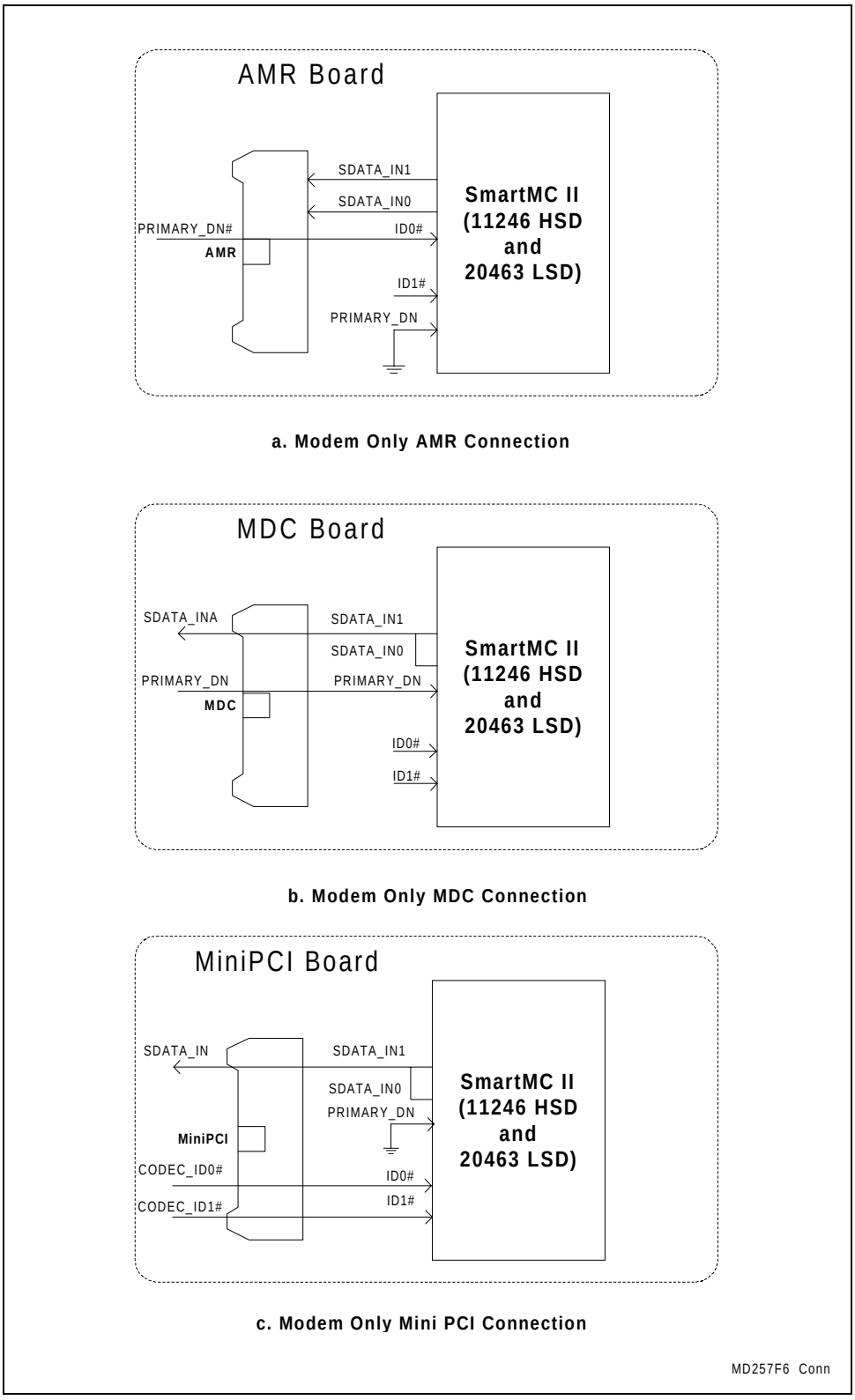


Figure 6. Modem Codec Primary/Secondary Codec Connections

Table 4. HSD (11246) Digital Electrical Characteristics - AC-link

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage	V_{IN}	-0.30	–	3.60	VDC	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	VDC	
Input Voltage High	V_{IH}	1.6	–	–	VDC	
Output Voltage Low	V_{OL}	0	–	0.33	VDC	
Output Voltage High	V_{OH}	2.97	–	–	VDC	
Input Leakage Current (AC-link inputs)	–	-10	–	10	µA	
Output Leakage Current (High-Z AC-link outputs)	–	-10	–	10	µA	

Notes:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.

Table 5. HSD (11246) Digital Electrical Characteristics –TTL - Compatible

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IL}	-0.3	–	0.8	VDC	
Input Voltage High	V_{IH}	2.0	–	3.6	VDC	
Input Current Low (See Note 2)	I_{IL}	–	–	-10	µA	V_{IN} = 0
Input Current High (See Note 2)	I_{IH}	–	–	+10	µA	V_{IN} = +3.6V

Notes:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C.
2. Current flow out of the device is shown as minus.

AC Timing Characteristics

AC Link Clocks

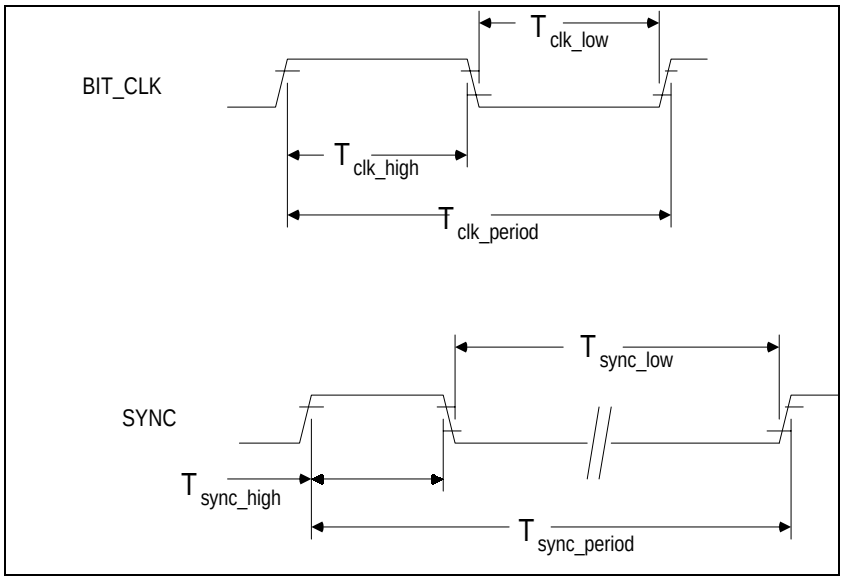


Figure 7. BIT_CLK and SYNC Timing Waveforms

Table 6. BIT_CLK and SYNC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (Note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs

Note 1: Worst case duty cycle restricted to 45/55.
Note 2: 47.5-70 pF external load.

Data Output and Input

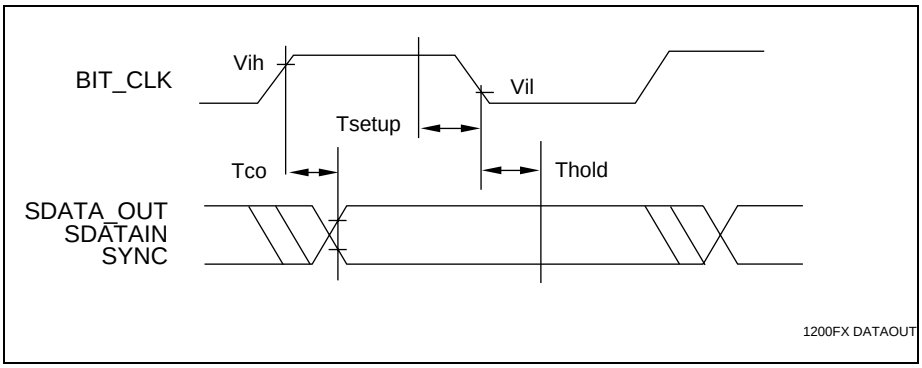


Figure 8. Data Output and Input Timing Waveforms

Table 7. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	Tco	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. **Note 2:** 50 pF external load.					

Table 8. AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	T_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	T_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC inputs with respect to BIT_CLK at the device latching the input.					

Table 9. AC-link BIT_CLK and SDATA Rise and Fall Time Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note: Maximum combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					

Signal Rise and Fall Times

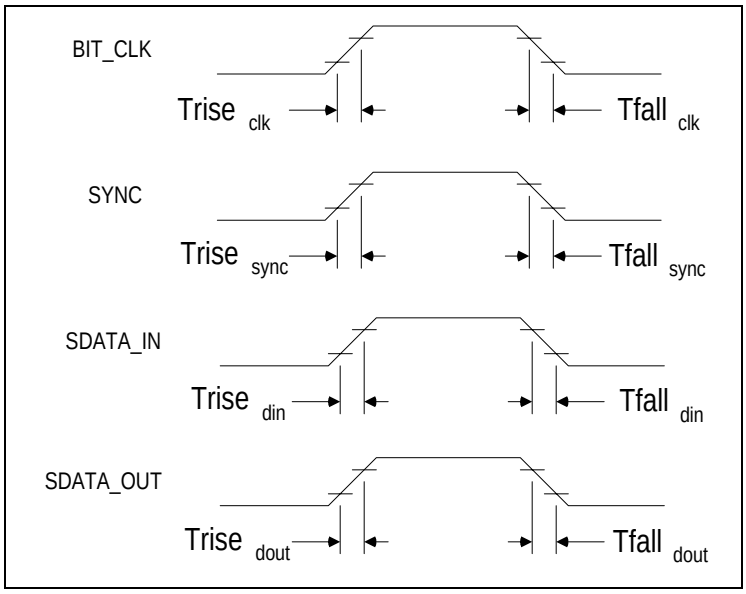


Figure 9. Signal Rise and Fall Time Timing Waveforms

Table 10. Signal Rise and Fall Time Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns

Note1: 50pF external load; from 10% to 90% of VDD.
Note 2: rise is from 10% to 90% of VDD (Vol to Voh).
Note 3: fall is from 90% to 10% of VDD (Voh to Vol).

RESET# (Cold Reset)

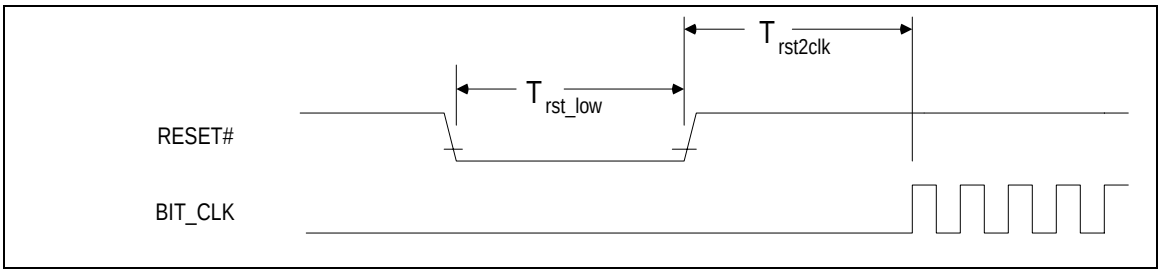


Figure 10. Cold Reset Timing Waveforms

Table 11. Cold Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

RESET# (Warm Reset)

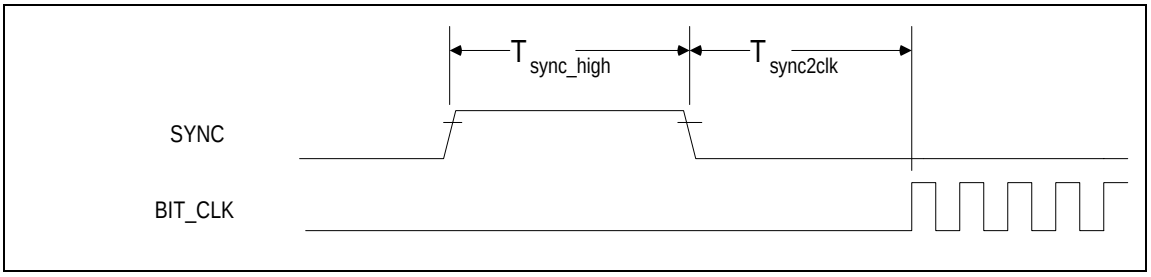


Figure 11. Warm Reset Timing Waveforms

Table 12. Warm Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns
Note: The minimum SYNC pulse width pertains to warm reset only, during normal operation, SYNC is asserted for the entire tag phase (16 BIT_CLK times).					

AC-link Low Power Mode Timing

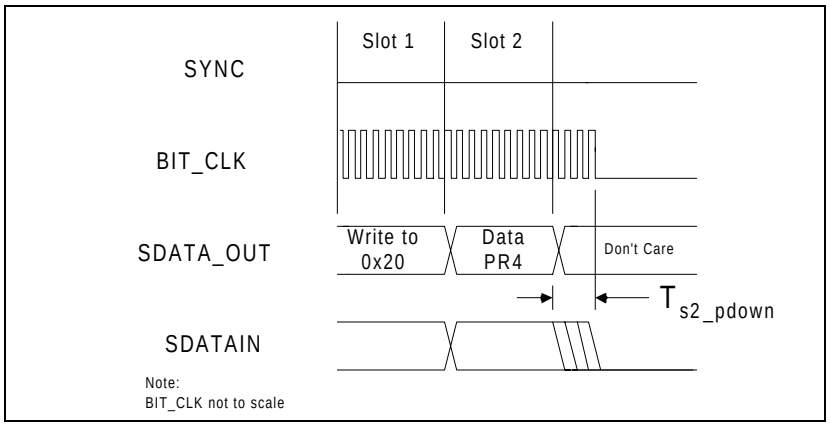


Figure 12. AC-link Low Power Mode Timing Waveforms

Table 13. AC-link Low Power Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

ATE Test Mode Timing

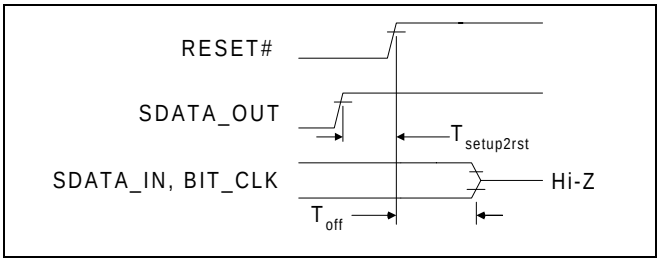


Figure 13. ATE Test Mode Timing Waveforms

Table 14. ATE Test Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

AC-link IO Pin Capacitance and Loading

In multiple Codec implementations, the AC '97 2.1 Controller can drive SYNC and SDATA_OUT to two or more destinations. The Controller's SYNC and SDATA_OUT output pin drivers must meet AC-link timing requirements when loaded by the total capacitance on each of these outputs.

In multiple Codec implementations, the SmartMC II can drive BIT_CLK to 1 or 2 destinations. The Codec's BIT_CLK output pin driver meets AC-link timing requirements when loaded by the total capacitance on this output.

The following factors contribute to total capacitance:

- Controller or Codec output pin capacitance (internal device characteristic)
- Codec or Controller input pin capacitance (7.5 pF max per AC '97 2.1, see Table 15)
- Total trace length capacitance on motherboard plus riser (estimated 2.5 pF per inch). Note that motherboard plus riser trace lengths, especially in multiple Codec implementations such as AC down (motherboard) and MC up (riser), could exceed ~15 inches, particularly in NLX form factor designs.
- IO connectors, such as motherboard to riser (estimated 2.5 pF)

AC '97 2.1 compatibility recommends that the following Controller and Codec input pins have a maximum of 7.5 pF capacitance:

- Controller BIT_CLK and SDATA_IN[0-3] inputs
- Primary and Secondary Codec SYNC and SDATA_OUT inputs
- Secondary Codec BIT_CLK input

AC '97 2.1 compatibility recommends the Controller and Codec AC-link output pin drivers identified in Table 15 be of sufficient strength to meet AC-link timing requirements for the following specified external capacitive loads in 1-4 Codec implementations. In addition to these external capacitive loads, additional allowance must be made for the particular Controller or Codec output pin capacitance (internal device characteristic).

Table 15. AC-link Pin IO Driver Loading

Output pin	Capacitance: 1 Codec	Capacitance: 2 Codecs
Controller: SYNC, SDATA_OUT	47.5 pF	55 pF
Codec: BIT_CLK (can support 2 codecs)	55 pF	55 pF
Codec: SDATA_IN (point to point)	47.5 pF	47.5 pF
Notes: 47.5 pF load comprehends 1 input, 1 connector, and ~15 inches of trace length. 55 pF load comprehends 2 inputs, 1 connector, and ~15 inches of trace length.		

Crystal Specification

Table 16 lists the required crystal parameters.

Table 16. Crystal Specification

Parameter	Range
Frequency	24.576 MHz
Oscillation Mode	Fundamental
Resonance	Parallel
Load Capacitance	39 pF
Frequency Tolerance	± 40 ppm @ 25 °C
Temperature Stability	± 45 ppm, 0-70 °C
Operating Temperature	0 -70 °C
Shunt Capacitance	< 7 pF
Equivalent Series Resistance	< 35 ohms @ 20 nW Drive Level
Drive Level	100 µW Correlation, 300 µW Max
Aging	± 15 ppm over 5 years
Storage Temperature Range	-40 to +85 °C

MC Interface Registers

Table 17 identifies the MC registers and bits.

Table 17. Modem Codec (MC) Registers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0	CID2	CID1	HSET	LIN 2	LIN1	xxx9h
40h	Modem Line 1 ADC/DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
56h	Misc. Modem Status/Control	x	CID1	CIDR	MLNK	x	x	x	x	x	x	x	x	x	x	x	x	4000h
66h	Miscellaneous Control	Res	Res	Res	Res	x	x	x	x	x	x	x	CIDBSY	x	x	PDXTAL	LINSEL	0000h
68h	Cold Reset Mask	COS15	COS14	COS13	COS12	COS11	COS10	COS9	COS8	COS7	COS6	COS5	COS4	COS3	COS2	COS1	COS0	xxxxh
6Ah	XTAL to BITCLK Timer	x	x	x	x	x	x	x	x	TIM7	TIM6	TIM5	TIM4	TIM3	TIM2	TIM1	TIM0	0040h
78h	Reserved	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	xxxxh
7Ah	Reserved	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	80xxh
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4358h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5421h

Register Definitions

Extended Modem ID Register (Index 3Ch)

The extended modem ID is a read/write register that primarily identifies the codec's modem capabilities.

Depending upon which line is selected by bit 66:0, bits 0, 1, 3, 4 will change accordingly. In other words, bit 3 should equal bit 0 and bit 4 should equal bit 1. This register is defaulted on power-on to line 1, meaning the default value for this register will be x009h.

ID0# and ID1# will reflect the state of the external codec ID pins as well as the detection of the PRIMARY_DN signal. See ID0# and ID1# in Table 3 for more details.

Even though the bits are listed as read only, the register is actually a read/write register. Writing any value to this register performs a register reset, which causes all registers to revert to their default values.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0	CID2	CID1	HSET	LIN 2	LIN1	xxx9h

Bit	Label	R/W	Description
15:14	ID[1:0]	R/W	**Codec Configuration Identifier.** This 2-bit field identifies the codec configuration: 00 = Primary codec configuration 01, 10, or 11 = Secondary codec configuration
13			**Reserved.**
12:9	SB[7:4]	R	**Sub-Assembly ID.** Fixed to 0 (default).
8:5	SB[3:0]	R	**Sub-Assembly ID.** Mapped to SUBID[3:0] pins, respectively.
4	CID2	R	**Caller ID Decode for Line 2 Supported.** 0 = Default.
3	CID1	R	**Caller ID Decode for Line 1 Supported.** 1 = Supported.
2	HSET	R	**Handset DAC.** 0 = Not supported.
1	LIN2	R	**Line 2 Supported.** 0 = Default.
0	LIN1	R	**Line 1 Supported.** 1 = Supported.

Modem Line 1 ADC/DAC Rate Control Register (Index 40h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Modem Line 1 ADC/DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**Modem Line 1 ADC/DAC Sample Rate.** 16-bit unsigned value between 0 and 65535 as follows representing the rate of operation in Hz: **D[15-0] (hex) — Sample Rate** 1F40 — 8 kHz 2580 — 9.6 kHz (48000/5) 3592 — 13.71428 kHz (96000/7) 3E80 — 16 kHz 4B00 — 19.2 kHz 5DC0 — 24 kHz BB80 — 48 kHz (Default.)

Miscellaneous Modem Register (Index 56h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Misc. Modem Status/Control	x	CID1	CIDR	MLNK	x	x	x	x	x	x	x	x	x	x	x	x	4000h

Bit	Label	R/W	Description
15			**Reserved.**
14	CID1	R	**Caller ID for Line 1 Captured.** 0 = Caller ID for Line 1 has not been captured. (Default.) 1 = Caller ID for Line 1 has been captured and stored.
13	CIDR	R	**Caller ID Data is Raw.** 0 = Caller ID data is not raw. (Default.) 1 = Caller ID is raw (demodulated but not decoded; includes seizure, marks, etc.).
12	MLNK	R/W	**MC '97 Link.** Controls MC '97 AC-link status. 0 = AC-link is on. (Default.) 1 = AC-link is off (sleep).
11:0			**Reserved.**

Miscellaneous Control (Index 66h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	Miscellaneous Control	Res	Res	Res	Res	x	x	x	x	x	x	x	CIDBSY	x	x	PDXTAL	LINSEL	0000h

Bit	Label	R/W	Description
15:5	Reserved		Reserved
4	CIDBSY	W	**Caller ID Busy** 0 = (Default.) 1 = Counter in register 6A that switches from RC oscillator to BIT_CLK is being decremented and the SSD registers are not accessible through the AC-link. Reset by the device automatically.
3:2	Reserved		Reserved
1	PDXTAL	W	**Crystal Circuit Power Down Enable.** 0 = Crystal Circuit power-down is not enabled. (Default.) 1 = Crystal Circuit power-down is not enabled.
0	LINSEL	W	**Line Select.** 0 = MC functions as Line 1 (Default.) 1 = MC functions as Line 2 (not supported).

Cold Reset Mask (Index 68h)

Written to before going into sleep mode, the cold reset mask allows certain sections to NOT be reset. The caller ID may have information store in its RAM and should not be cleared with a reset. Register banks are also preserved with their original values. E8B4h is the 16-bit decode value that needs to be written in order for cold reset masking to be enabled.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	Cold Reset Mask	COS15	COS14	COS13	COS12	COS11	COS10	COS9	COS8	COS7	COS6	COS5	COS4	COS3	COS2	COS1	COS0	xxxxh

XTAL to BITCLK Timer (Index 6Ah)

Contains a timer which determines when to switch from using the crystal to BIT_CLK after caller ID is completed while in secondary mode. The count value is in the lower eight bits of this register. Each count is defaulted to 0040h. It does not need to be re-programmed again unless a cold reset occurs. The indicator bit, CIDBSY, that tells the software the caller ID engine remains busy, is located at 66:4.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	XTAL to BITCLK Timer	x	x	x	x	x	x	x	x	TIM7	TIM6	TIM5	TIM4	TIM3	TIM2	TIM1	TIM0	0040h

Reserved Register (Index 78h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
78h	Reserved	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	xxxxh

Reserved Register (Index 7Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	Indexed 1 Register	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	xxxxh

Vendor ID Registers 1 and 2 (Indexes 7Ch and 7Eh)

This register contains the vendor identification code and revision numbers.

The vendor identification code is reported in the F[7:0], S[7:0], and T[7:0] fields. The ID method is Microsoft's Plug and Play Vendor ID code.

The vendor revision number is reported in the REV[7:0] field.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4358h

Bit	Label	R/W	Description
15:8	F[7:0]	R	**Vendor ID Code Character 1.** Conexant ID code character 1: ASCII "C" (43h).
7:0	S[7:0]	R	**Vendor ID Code Character 2.** Conexant ID code character 2: ASCII "X" (58h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5421h

Bit	Label	R/W	Description
15:8	T[7:0]	R	**Vendor ID Code Character 3.** Conexant ID code character 3: ASCII "T" (54h).
7:0	REV[7:0]	R	**Vendor Revision Number**. Revision number. The initial number is 21h (ACSII "1").

Digital Interface

The codec communicates with the controller via a digital serial link (AC-link). All digital audio streams, modem line codec stream, handset, GPIO, and command/status information is transferred between the controller and the codec over this point to point serial channel. The AC-link interface signals are shown in Figure 14 and are described in Table 18.

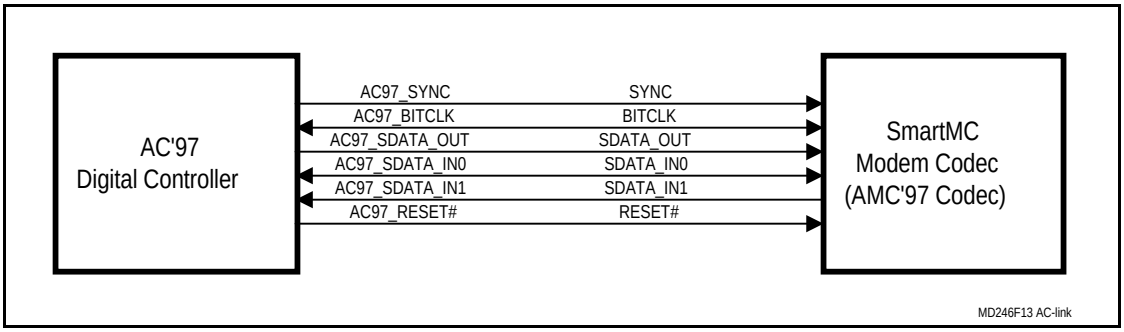


Figure 14. AMC '97 Codec Connection to AC '97 Controller

Table 18. AC-link Serial Interface Signals

Signal Name	MC I/O	Description
SYNC	I	48 kHz fixed rate sample synchronization from the controller to the codec.
BIT_CLK	I O	12.288 MHz serial data clock to the codec (Secondary MC). 12.288 MHz serial data clock from the codec (Primary MC).
SDATA_IN0	I O	Serial data stream from the controller to the codec (Secondary MC) Serial data stream from the codec to the controller (Primary MC)
SDATA_IN1	O	Serial data stream from the codec to the controller.
SDATA_OUT	I	Serial data stream from the controller to the codec.
RESET#	I	Master hardware reset from the controller

The control and status slots allow writing and reading of registers internal to the SmartMC II. These registers are defined as 16 bit and are addressed at word aligned byte addresses 0x00, 0x02, 0x04, …, 0x7e. Registers 0x00 - 0x58 are predefined, 0x5a - 0x7a are reserved for the vendor, 0x7c and 0x7e are for the vendor ID.

Because provisions exist for the modem and other sample rates to be less than 48 kHz, the TAG slot contains bits which indicate the validity of each slot in the serial stream.

The AC '97 specification also defines slot request bits that allow the codec to request samples from the controller. These bit definitions (active low) are implemented as defined in that specification.

When a slot is valid for the outgoing stream, the controller places a one in the corresponding bit position in the TAG slot. For all slots other than the PCM left and right slots, the codec ignores the data present in the slot when the slot's tag bit is a 0 for that particular data phase. This allows the controller to simply repeat the current sample if desired. However, the controller must respond properly to the SLOTREQ bits. For the PCM left and right slots, the codec assumes every slot is valid. If the slot is invalid, the controller must send 0's for the data.

When a slot is valid for the incoming stream, the codec places a one in the corresponding bit position in the TAG slot. The controller must ignore the data present in the slot when the slot's tag bit is a 0 for that particular data phase. The Codec puts zeros in the slot when the slot is invalid.

The AC-link request for status always returns in the next frame. The request is, therefore, always delayed by one frame time. A write request in the current frame will not affect the status that is returned in that particular write frame. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the controller.

The time slots supported by the SmartMC II are listed in Table 19.

Table 19. SmartMC II Supported Slot Assignments

Slot Number	SDATAOUT (Controller to MC)	SDATAIN (MC to Controller)
0	TAG	TAG
1	Command Address Port	Status Address Port
2	Command Data Port	Status Data Port
3	Not Supported	PCM Record Left Channel*
4	Not Supported	PCM Record Right Channel*
5	Modem Line 1 DAC Input Data	Modem Line 1 ADC Output Data
6	Not Supported	Mic ADC Output Data
7	Not Supported	Not Supported
8	Not Supported	Not Supported
9	Not Supported	Not Supported
10	Not Supported	Not Supported
11	Handset DAC Input Data	Handset ADC Output Data
12	GPIO Control	GPIO Status
* Pass through when Secondary MC.		

SDATA_IN (Codec to Controller) Slot Definitions

Input Slot 1: Status Address Port / SLOTREQ Bits

Slot 1, the Status Address Port, delivers codec control register read address slot request flags for all output slots. Bits 11 to 2 are defined as data request flags for output Slots 3-12.

Input Slot 1: Status Address Port	
Bit	**Description**
19	**Reserved.** Set to 0 by the codec.
18:12	**Control Register Index.** Echo of register index for which data is being returned. Set to 0s if tagged "invalid" by the controller.
11:2	**"On Demand" Data Request Flags (next output frame).** 0 = Send data, 1 = Do not send data.
11	**Slot 3 Request.** PCM Left Channel.
10	**Slot 4 Request.** PCM Right Channel.
9	**Slot 5 Request.** Modem Line 1.
8	**Slot 6 Request.** Not used. Set to 0 by the codec.
7	**Slot 7 Request.** Not used. Set to 0 by the codec.
6	**Slot 8 Request.** Not used. Set to 0 by the codec.
5	**Slot 9 Request.** Not used. Set to 0 by the codec.
4	**Slot 10 Request.** Modem Line 2.
3	**Slot 11 Request.** Handset.
2	**Slot 12 Request.** GPIO.
1:0	**Reserved.** Set to 0 by the codec.

The Slot 1 tag bit is independent of the bit 11:2 slot request field, and **only** indicates valid Status Address Port data (Control Register Index). The MC sets SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to "1" when returning valid data from a previous register read. They are otherwise set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots are driven with 0s for maximum compatibility with the original AC '97 Component Specification. Output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit is forced to "1" in the interval between when the powerdown bit for its associated channel is turned off and when its channel is ready to accept samples. The controller can take advantage of this scheme to eliminate the need to poll the MC status registers.

To power down a channel, the controller needs only to:

1. Disable the source of DAC samples in controller.
2. Set the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.

To power up a channel, the controller needs only to:

1. Clear the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.
2. Enable the source of DAC samples in controller.

Input Slot 2: Status Data Port

Input Slot 2, the Status Data Port, port delivers 16-bit control register read data.

Input Slot 2: Status Data Port	
Bit	**Description**
19:4	**Control Register Read Data.** Stuffed with 0's if tagged "invalid" by the codec.
11:0	**Reserved.** Stuffed with 0's by the codec.

Input Slot 5: Modem Line 1 ADC Output Data

Input Slot 5 contains the 16-bit Modem Line 1 ADC output data.

Operates as a single line Data/Fax/Voice/TAM only modem only AC'97 rev 2.1 compatible codec with the Line Side Device and DIB (uses slot 5 and 12).

Input Slot 5: Modem Line 1 ADC Output Data	
Bit	**Description**
19:4	**Modem Line 1 ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 11: Handset ADC Output Data

Input Slot 11 contains the 16-bit Handset ADC output data.

Input Slot 11: Handset ADC Output Data	
Bit	**Description**
19:4	**Handset ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 12: GPIO Control

Input Slot 12 contains the GPIO status bits. The codec constantly updates the status slot based upon the logic level detected at each GPIO configured for input. The controller must debounce the reported states as required for the 48 kHz sample rate.

Input Slot 12: GPIO Status	
Bit	**Description**
19:4	**GPIO[15:0] Status.** 1 = High level detected at input pin; 0 = Low level detected at input pin. Bits corresponding to GPIO outputs reflect the command level.
19	**GPIO15 Status.** Application assigned. Not supported.
18	**GPIO14 Status.** Application assigned. Not supported.
17	**GPIO13 Status.** Application assigned. Not supported.
16	**GPIO12 Status.** Application assigned. Not supported.
15	**GPIO11 Status.** Application assigned. Not supported.
14	**GPIO10 Status.** Application assigned. Not supported.
13	**GPIO9 Status.** Application assigned. Not supported.
12	**GPIO8 Status.** Application assigned. Not supported.
11	**GPIO7 Status.** Internal LSD function (GPI7 = Reserved).
10	**GPIO6 Status.** External LSD function (GPIO6 = Pin 1, labeled GPIO2).
9	**GPIO5 Status.** External LSD function (GPIO5 = Pin 32, labeled GPIO1).
8	**GPIO4 Status.** External LSD function (GPIO4 = Pin 31, labeled GPIO0).
7	**GPIO3 Status.** Internal LSD function (GPI3 = VCR, Monitor VDD voltage).
6	**GPIO2 Status.** Internal LSD function (GPI2 = RINGB, Ring Detect BAR for detecting line polarity reversal).
5	**GPIO1 Status.** Internal LSD function (GPI1 = RING, Ring Detect input).
4	**GPIO0 Status.** Internal LSD function (GPI0 = LCL, Line Current Loss).
3:0	**Not Used.** Stuffed to 0's by the codec.

SDATA_OUT (Controller to Codec) Slot Definitions

Output Slot 1: Command Address Port

Output Slot 1, the Command Address Port, is used to control features and monitor status (see Input Slots 1 and 2) for codec functions such as mixer settings and power management.

Output Slot 1: Command Address Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 2: Command Data Port

Output Slot 2, the Command Data Port, is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19). If the current command port operation is a read, then the entire slot time must be stuffed with 0's by the controller.

Output Slot 2: Command Data Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 5: Modem Line 1 DAC Input Data

Output Slot 5 contains the 16-bit Modem Line 1 DAC input data.

Output Slot 5: Modem Line 1 DAC Input Data	
Bit	**Description**
19:4	**Modem Line 1 DAC Input Data.** 16-bit sample (bit 19 = MSD; bit 4 = LSD)
3:0	**Not Used.** Stuffed to 0's by the controller.

Output put Slots 6-10: Reserved

Output Slots 6-10 are reserved.

Output Slot 6-9: Reserved	
Bit	**Description**
19:0	**Reserved.** Stuffed to 0's by the controller.

Output Slot 11: Handset DAC Input Data

Output Slot 11 contains the 16-bit Handset DAC input data.

Output Slot 11: Handset DAC Input Data	
Bit	**Description**
19:4	**Handset DAC Input Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 12: GPIO Status

Output Slot 12 contains the GPIO control bits. The codec constantly sets the GPIOs that are configured for output based upon the value of the corresponding bit position of the control slot.

Output Slot 12: GPIO Control	
Bit	**Description**
19:4	**GPIO[15:0] Control.** 1 = High level at the codec output pin.; 0 = Low level at the codec output pin. Bits corresponding to GPIO inputs are set to 0 by the controller.
19	**GPIO15 Control.** Application assigned. Not supported.
18	**GPIO14 Control.** Application assigned. Not supported.
17	**GPIO13 Control.** Application assigned. Not supported.
16	**GPIO12 Control.** Application assigned. Not supported.
15	**GPIO11 Control.** Application assigned. Not supported.
14	**GPIO10 Control.** Application assigned. Not supported.
13	**GPIO9 Control.** Application assigned. Not supported.
12	**GPIO8 Control.** Application assigned. Not supported.
11	**GPIO7 Control.** Internal LSD function (GPI7 = Reserved).
10	**GPIO6 Control.** External LSD function (GPIO6 = Pin 1, labeled GPIO2).
9	**GPIO5 Control.** External LSD function (GPIO5 = Pin 32, labeled GPIO1).
8	**GPIO4 Control.** External LSD function (GPIO4 = Pin 31, labeled GPIO0).
7	**GPIO3 Control.** Internal LSD function (GPI3 = VCR, Monitor VDD voltage).
6	**GPIO2 Control.** Internal LSD function (GPI2 = RINGB, Ring Detect BAR for detecting line polarity reversal).
5	**GPIO1 Control.** Internal LSD function (GPI1 = RING, Ring Detect input).
4	**GPIO0 Control.** Internal LSD function (GPI0 = LCL, Line Current Loss).
3:0	**Not Used.** Stuffed to 0's by the controller.

SmartDAA LSD (20463) Hardware Pins and Signals

General

HSD Interface (Through DIB)

The DIB interface signals are:

- Clock (CLK); input
- Digital Power (PWR+); input power
- Digital Ground (DGND); digital ground
- Data Positive (DIB_P); input
- Data Negative (DIB_N); input

Telephone Line Interface

The telephone line interface signals are:

- RING AC Coupled (RAC1); input
- TIP AC Coupled (TAC1); input
- RING AC Coupled (RAC2); input
- TIP AC Coupled (TAC2); input
- Electronic Inductor Resistor (EIR); output
- TIP and RING DC Measurement (TRDC); input
- DAC Output Voltage (DAC); output
- Electronic Inductor Capacitor (EIC)
- Electronic Inductor Output (EIO)
- Electronic Inductor Feedback (EIF)
- Resistive Divider Midpoint (DCF)
- Transmit Analog Output (TXA); output
- Receive Analog Input (RXI); input
- Receiver Gain (RXG); output
- MOV Enable (MOVEN); output
- World-wide Impedance 0 (ZW0); input
- US Impedance 0 (ZUS0); input
- Transmit Feedback (TXF); input
- Transmit Output (TXO); output

SmartDAA LSD (20463) Interface Signals and Pin Assignments

The LSD (20463) 32-pin TQFP hardware interface signals are shown by major interface in Figure 15, are shown by pin number in Figure 16, and are listed by pin number in Table 20.

The LSD (20463) hardware interface signals are defined in Table 21.

The LSD (20463) digital characteristics are specified in Table 22.

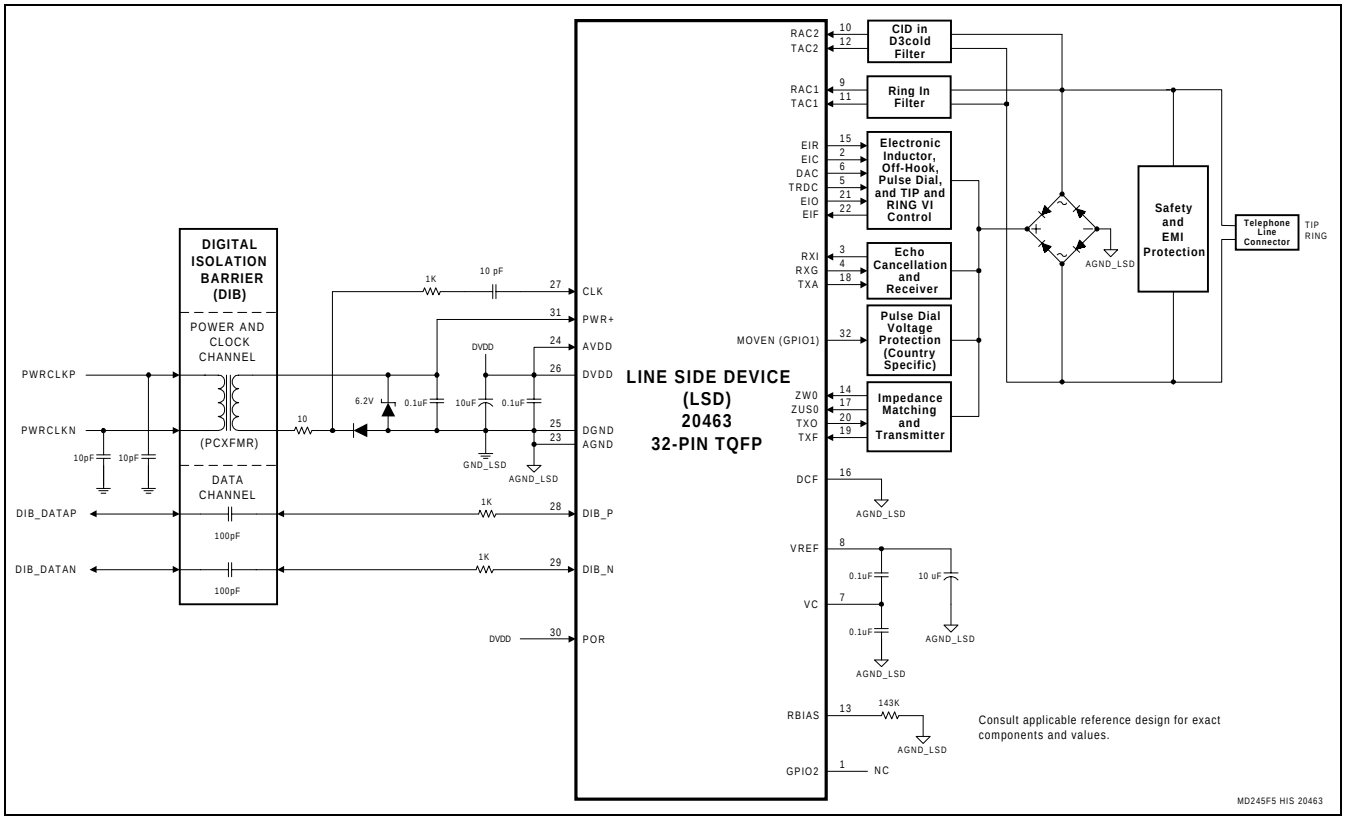


Figure 15. LSD (20463) 32-Pin TQFP Hardware Interface Signals

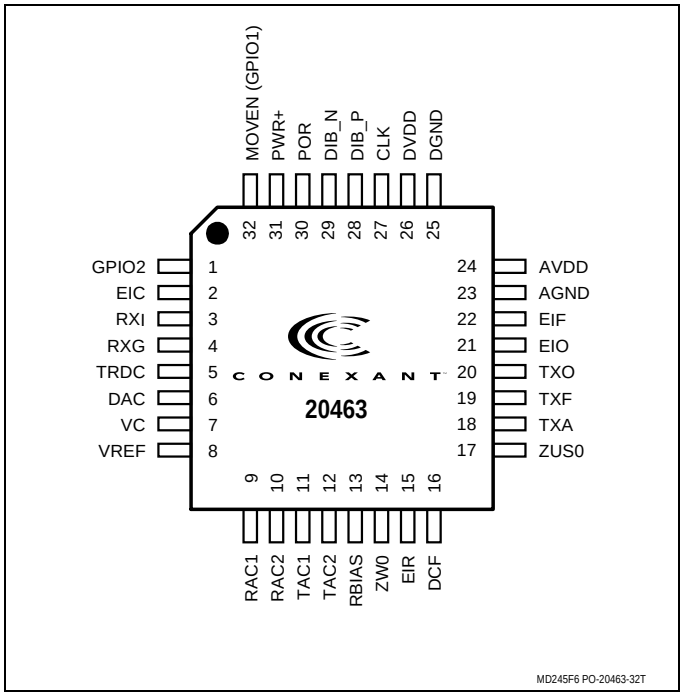


Figure 16. LSD (20463) 32-Pin TQFP Pin Signals

Table 20. LSD (20463) 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface
1	GPIO2	It/Ot12	NC
2	EIC	Oa	Telephone Line Interface Components
3	RXI	Ia	Telephone Line Interface Components
4	RXG	Oa	Telephone Line Interface Components
5	TRDC	Oa	Telephone Line Interface Components
6	DAC	Oa	Telephone Line Interface Components
7	VC	REF	VREF through 0.1 µF and to AGND_LSD through 0.1 µF
8	VREF	REF	VC through 0.1 µF and to AGND_LSD through 10 µF
9	RAC1	Ia	RING through 1 MΩ and 0.033 µF
10	RAC2	Ia	RING through 330 KΩ and 0.001 µF (optional for CID from D3cold)
11	TAC1	Ia	TIP through 1 MΩ and 0.033 µF
12	TAC2	Ia	TIP through 330 KΩ and 0.001 µF (optional for CID from D3cold)
13	RBIAS	Ia	AGND_LSD through 143 KΩ
14	ZW0	Ia	Telephone Line Interface Components
15	EIR	Ot12	Telephone Line Interface Components
16	DCF	Ia	AGND_LSD
17	ZUS0	Ia	Telephone Line Interface Components
18	TXA	Oa	Telephone Line Interface Components
19	TXF	Ia	Telephone Line Interface Components
20	TXO	Oa	Telephone Line Interface Components
21	EIO	Oa	Telephone Line Interface Components
22	EIF	Ia	Telephone Line Interface Components
23	AGND	AGND_LSD	AGND_LSD
24	AVDD	PWR	LSD DVDD pin
25	DGND	GND_LSD	DIB PCXFMR secondary winding bottom through diode and 10 Ω in series and to GND_LSD
26	DVDD	PWR	LSD AVDD pin and to GND_LSD through 10 µF and 0.1 µF in parallel
27	CLK	I	DIB PCXFMR secondary winding bottom through 10 pF and 1 KΩ in series and through 10 Ω shared with LSD DGND pin through diode
28	DIB_P	I/O	DIB line side Data Positive capacitor through 1 KΩ
29	DIB_N	I/O	DIB line side Data Negative capacitor through 1 KΩ
30	POR	It	LSD DVDD pin
31	PWR+	PWR	DIB PCXFMR secondary winding top and to GND_LSD through 6.2 V zener diode and 0.1 µF in parallel
32	MOVEN (GPIO1)	Ot12	Telephone Line Interface Components

Notes:

1. I/O types*:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground
   - *See LSD (20463) Digital Electrical Characteristics (Table 22).
2. Interface Legend:
   - HSD — Host Side Device

Table 21. LSD (20463) 32-Pin TQFP Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
AVDD	24	PWR	**Analog Power Supply.** Connect to the LSD DVDD pin. See Layout Guidelines section.
AGND	23	AGND_LSD	**LSD Analog Ground. LSD Analog Ground.** Connect to AGND_LSD at the GND_LSD/AGND_LSD tie point and to the analog ground plane. See Layout Guidelines section.
POR	30	It	**Power-On Reset.** Connect to LSD DVDD pin.
VREF	8	REF	**Output Reference Voltage.** Connect to VC through 0.1 µF and to AGND_LSD through 10 µF. Ensure a very close proximity between this capacitor and the VREF pin.
VC	7	REF	**Output Middle Reference Voltage.** Connect to AGND_LSD through 0.1 µF. Ensure a very close proximity between this capacitor and the VC pin. Use a short path and a wide trace to AGND_LSD pin.
DIB INTERFACE SIGNALS			
CLK	27	I	**Clock.** Provides input clock, AC coupled, to the LSD**.** Connect to DIB PCXFMR secondary winding bottom through 1 KΩ and 10 pF in series and through 10 Ω shared with LSD DGND pin through diode.
PWR+	31	PWR	**Digital Power Input**. Provides input digital power to the LSD. Connect to DIB PCXFMR secondary winding top, and to GND_LSD though a 6.2 V zener diode and 0.1 µF in parallel.
DVDD	26	PWR	**Digital Power**. Connect to pin 24 (AVDD) and to GND_LSD through 10 µF and 0.1 µF in parallel.
DGND	25	GND_LSD	**LSD Digital Ground.** Connect to DIB PCXFMR secondary winding bottom through diode in series with 10 Ω, and to GND_LSD at the GND_LSD/AGND_LSD tie point.
DIB_P, DIB_N	28, 29	I/O, I/O	**Data and Control Positive and Negative.** Connect to HSD DIB_DATAP and HSD DIB_DATAN, respectively, each line serially through 1 KΩ on LSD side and 100 pF in DIB. Signals are differential, and ping pong between DIB and HSD (half duplex).
TIP AND RING INTERFACE			
RAC1, TAC1	9, 11	Ia, Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC coupled voltage from telephone line used to detect ring. Connect RAC1 to the top of the diode bridge through 1 MΩ and 0.033 µF (200V). Connect TAC1 to the of the diode bridge through 1 MΩ and 0.033 µF (200V).
RAC2 TAC2	10, 12	Ia, Ia	**RING2 AC Coupled and TIP2 AC Coupled for Caller ID from D3cold.** AC coupled voltage from telephone line used to detect ring for Caller ID from D3cold. Connect RAC2 to the top of the diode bridge through 330 KΩ and 0.001 µF (200V). Connect TAC2 to the bottom of the diode bridge through 330 KΩ and 0.001 µF (200V). Optional; leave open if not used.
EIR	15	Oa	**Electronic Inductor Resistor.** Electronic inductor resistor switch.
EIC	2	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to no connect when pulse dialing and to ground all other times. This is needed to eliminate pulse dial interference from the electronic inductor AC filter capacitor.
DAC	6	Oa	**DAC Output Voltage.** Output voltage of the reference DAC.
TRDC	5	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information.
EIO	21	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control offhook, pulse dial, and DC IV mask operation.
EIF	22	Ia	**Electronic Inductor Feedback.** Electronic inductor feedback.
RXG	4	Oa	**Receiver Gain.** Receiver gain output.
RXI	3	Ia	**Receive Analog Input.** Receive signal input.
TXA	18	Oa	**Transmit Analog Output.** Transmit signal used for canceling echo in the receive path.
MOVEN (GPIO1)	32	Ot12	**MOV Enable**. Connect to pulse dial voltage protection circuit for Australia/Poland/Italy use. Leave open if not required.
RBIAS	13	Ia	**Receiver Bias.** Connect to GND through 143 KΩ.
DCF	16	Ia	**Resistive Divider Midpoint.** Connect to LSD analog ground.

Table 22. LSD (20463) 32-Pin TQFP Pin Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
TELEPHONE LINE INTERFACE (CONTINUED)			
ZW0	14	Ia	**World-Wide Impedance 0.** Input signal used to provide line complex impedance matching for world-wide countries.
ZUS0	17	Ia	**US Impedance 0.** Input signal used to provide line impedance matching for U.S.
TXO	20	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to transmitter transistor.
TXF	19	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor.
NOT USED			
GPIO2	1	It/Ot12	**General Purpose I/O 2**. Leave open if not used.

Notes:

1. I/O types*:

Ia	Analog input
It	Digital input, TTL-compatible
Oa	Analog output
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
AGND_LSD	Isolated LSD Analog Ground
GND_LSD	Isolated LSD Digital Ground

*See LSD (20463) Digital Electrical Characteristics (Table 22).

2. Interface Legend:

HSD	Host Side Device

Table 22. LSD (20463) Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	3.60	V	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.4 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF

Electrical and Environmental Specifications

The operating conditions are specified in Table 23.

The absolute maximum ratings are listed in Table 24.

The current and power requirements are listed in Table 25.

Table 23. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	+3.0 to +3.6	VDC
Operating Temperature Range	T_A	0 to +70	°C

Table 24. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.0	V
Input Voltage	V_{IN}	-0.5 to (VIO +0.5)*	V
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VIO +0.5)*	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VIO = +3.3V ± 0.3V or +5V ± 5%.			

Table 25. Current and Power Requirements

Device State (Dx)	Conditions			Current		Power	
	AC-link	HSD Crystal**	DIB Clocks*	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)
HSD (11246) + LSD (20463)							
D0—Port Closed	On	On	On	3.5	—	11.5	—
D0—Port Open	On	On	On	8.0	—	26.4	—
D0—On-Line	On	On	On	33	—	110	—
D3—Suspend	Off	Off	On	3.0	—	9.9	—
D3—Suspend	Off	Off	Off*	0.47*	—	1.6	—

Notes:

Operating voltage: VDD = +3.3V Dual/Standby.

Definitions:

Device State: D0 = Full power state; D3 = Low power state.

AC-link: The AC-link is considered off upon removal of the BIT_CLK.

*DIB Clocks: On = The DIB clocks must be on (i.e., digital interface between the system-side and line-side is operating) to wake from ring or to capture Caller ID.

** HSD Crystal control applies to Primary operation only. For Secondary operation, the AC-link provides the device clock.

Layout Guidelines

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the modem and voice codec devices. This is especially important for high performance modem operation with high bit rate data and fax. Suppression of noise is essential to the proper operation and performance of the modem and DAA circuitry.

Two major aspects of noise in an OEM board design containing the modem device set must be considered:

- On-board generated noise and off-board generated noise that is coupled on-board can affect analog signal levels (especially low levels) and quality as well as affecting analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC) operation. Of particular concern is noise in frequency ranges affecting modem and audio circuit performance.
- On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce EMI to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to obtain EMI certification.

A board design should also comply with a host interface specification addressing electrical, physical, and environmental requirements.

The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars covering noise suppression techniques are routinely offered by technical and professional associations as well as component suppliers.

These guidelines are offered to help achieve good modem performance, minimize audible noise for audio circuit use, and to minimize EMI generation.

EMI Considerations

General

1. Because EMI always takes the easiest path to earth ground, ensure that EMI has a good planned path to earth ground. Provide ground paths to the bracket. The best ground is provided by the bracket, not by the ground pins on the bus (while the ground pins provide effective signal returns to the motherboard, at high frequencies these traces become inductors that acquire higher impedance with increasing frequency). The bracket ground connected to the PC chassis is quite effective in dealing with unwanted EMI. This includes using both bracket screws with as much contact surface area as possible to ground (including under the screw head), and pin 1 on any audio jacks (which tie to the bracket via the connector chassis and screw). On the bracket edge of the board, place a ground strip on both sides of the board. The bracket ground (chassis ground) depends on the PC's case, so choose a system for FCC testing with good EMI shielding. Experience has shown different PC brands can have quite different EMI characteristics of their own.
2. Surround noisy signals, especially clocks, with a wide GND guard band. Pay special attention to where the guard bands are grounded, as the effectiveness of this technique will be greatly diminished with increased physical distance from a good ground point.
3. Use multiple vias rather than a single via with power/ground distribution when changing layers on the board. The more vias that are on the board, the lower the impedance.
4. Avoid vias on traces carrying fast signals.
5. If radiated emissions move 6 or more dBuV just by slightly moving connected cables, the grounding technique used in design should be improved. At this point, maximize dumping EMI energy directly to the bracket ground without dumping too much EMI energy to scattered ground traces on the board.
6. In a design needing EMI filtering, define an additional "chassis" section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be placed in this section. Fill the unused space with a chassis ground plane where possible, and connect it to the metal card bracket and any connector shields/grounds.
7. Keep the current paths of separate board functional areas isolated from each other, thereby limiting the propagation of EMI to all areas of the board. Separate board functional areas include: Digital, DAA, and Analog.
8. Place a series terminating resistor as close as possible to the signal source on clock lines or fast edge rate signals.

Filtering

1. A general rule of thumb is to filter every connector on the board. On modem/audio boards, these filters take the form of ferrite beads and capacitors. Place a ferrite bead in series with the signal and a capacitor between the signal and ground. After the signal is filtered, it must not be exposed to any board noise. Therefore, the filter must be as close to the connector as possible and filtered signals kept away from the digital ground and power.

Decoupling

1. Another way to minimize EMI is to short it to ground through proper decoupling capacitors (caps). Because traces and component leads become inductors at high frequencies, use surface mount caps if possible, and place them close to the device being decoupled. Decouple power pins of a device directly to associated ground pins of the device as close to the device as possible - not to a remote ground plane. If you have power and ground planes, connect capacitors to the planes with more than one via. This will decrease the lead inductance and increase the effectiveness of the capacitors.
2. Capacitors can reduce EMI by shorting high frequencies to ground. This is good if the ground plane is properly grounded (i.e., short path to chassis ground). However, if the ground plane isn't properly grounded, then the decoupling caps need to be used to source as much noise to the ground plane as it can handle. Also note that the desired value of the decoupling cap depends on the frequency to be eliminated. With higher system clock rates it is necessary to have a mixture of values for decoupling caps (e.g., 0.001 uF, 0.01 uF and 0.1 uF).
3. Sourcing too much energy to ground can be just as harmful to EMI performance as not sourcing enough EMI to ground, if the path to ground is poor. The capacitor value chosen for an offending frequency can be mathematically correct but also cause excessive EMI ripple on the ground. Unless the impedance of ground traces can be reduced, the solution is to reduce the capacitor value. As an example, if the board is excessively radiating at 100 MHz with a 0.01 uF cap, try a 0.047 uF. The idea is to only source as much energy to ground as the ground can handle and no more, or the EMI will radiate.

Capacitor Value	Frequency of Reduced EMI
0.1 uF	10 MHz
0.01 uF	30 MHz
0.001 uF	100 MHz

4. There is some overlap, as these values will change as inductance of the board comes into effect, and the fact you rarely have just one problem frequency. Another rule of thumb, derived from experience, is 0.1 uF for <80 MHz, 0.01 uF for 60-500 MHz, and 0.001 uF for >400 MHz. The designer should provide several different values for de-coupling capacitors. These should be spread evenly around the power pins of devices on the board. A few capacitors can be placed in open areas of the board to stabilize the power and ground.
5. Separate analog power/ground from digital power/ground with inductors or ferrite beads. The side effect of this separation is that the analog circuit cannot dump their high frequency noise to the chassis ground. The EMI characteristic of boards can be improved by using adequate decoupling and by limiting the areas of analog power/ground.

Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another case. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in TIP and RING lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. Developing two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

General Layout Guidelines for a 2-Layer SmartMC II Board

Follow the guidelines in this section unless otherwise specified by a AMR specification, a local government regulation, or by a specific guideline mentioned in Section 0.

Placing Components

1. From the system circuit schematic, identify the digital, analog, and DAA circuits and their components, as well as external signal and power connections. Note the location of pins for power, ground, digital signals, and analog signals for each device.
2. Roughly place digital, DAA, and analog sections on the board.
   a) Place the digital section near the AMR connector.
   b) Place the DAA section near the telephone line RJ-11 connector.
3. Place the components starting with the connectors and jacks, then the modem devices (mixed signal devices), and finally the supporting components. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
   d) Orient components so pins carrying digital signals extend onto the digital portion of each section and pins carrying analog signals extend onto the analog portion section as much as possible.
   e) Place digital components close together in order to minimize signal trace length.
4. Place digital section components (see specific layout guidelines).
   a) Place the Host Side Device (HSD) near the AC-Link and immediately next to the Digital Isolation Barrier (DIB) with digital signal pins toward host interface connector and power, clock and data pins toward the DIB.
   b) Place AC-Link interface components close to the AMR connector in accordance with the applicable bus interface standard or specification.
   c) Place crystal circuits as close as possible to the HSD.
5. Place DAA section components (see specific layout guidelines).
   a) Place the LSD as close to the DIB as possible with analog signal pins toward the RJ-11 jack and power, clock and data pins toward the DIB.
   b) Place the DIB interface components between the LSD and the DIB.
   c) Place the analog telephone interface components between the LSD and the RJ-11 jack.
6. Place analog section components (see specific layout guidelines).
   a) Place the VC with analog signal pins toward the DAA section and digital signals toward the HSD.
   b) Place mixed-signal components to straddle the border between analog and digital sections.
   c) Place the analog components close to and on the side of card containing the analog signals.
   d) Avoid placing noisy components and traces near these analog signal traces.
7. Place decoupling (bypass) capacitors close to the pins (usually power and ground) of the device or connector they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI. Evenly distribute the decoupling capacitors around the associated device or connector.
8. Provide a "connector" component, usually a zero ohm resistor or a ferrite bead at one point on the PCB to connect one section's ground to another. Allow other points for grounds to be connected together if necessary for EMI suppression.

Power

1. Identify digital power (VDD) and analog power (AVDD) supply connections.
2. Place a **10 µF electrolytic or tantalum capacitor** in parallel with a ceramic 0.1µF capacitor between power and ground at a few points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power enters the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. Generally, route all power traces before signal traces.

Grounds

1. Provide a digital ground plane.
   a) Provide a digital ground plane on the board bottom everywhere except under the DAA section and where the analog ground plane is provided.
   b) Connect the digital ground plane to the board bracket (chassis ground).
   c) Provide digital ground fill, or islands, in unused space in the digital sections on top the board.
   d) Connect digital ground fill to the digital ground plane using multiple vias and to the bracket via multiple traces if possible.
   a) Provide digital ground guard bands around critical traces.
   a) Connect digital ground guard bands to the digital ground plane by one or more vias.
2. Provide separate and isolated DAA digital and DAA analog ground planes in the DAA section.
   a) Provide a DAA analog ground (AGND_LSD) on the board bottom under the DAA analog components.
   b) Provide a DAA digital ground (GND_LSD) on the board bottom side under the DAA digital components.
   c) Provide DAA digital ground fill in unused space around digital components in the DAA section on the top the board. **Ensure that this fill is at least 40 mils from any "hot" DAA signal coming from the phone jack.**
   d) Connect DAA analog ground (AGND_LSD) and DAA digital ground (LSD_GND) together at one point within the DAA, i.e., near the LSD AGND (pin 23) and power capacitor.
3. Provide an analog ground plane in the analog section.
   a) Provide analog ground plane on the board bottom under the analog section.
   b) Provide analog ground fill in unused space around analog components in the analog section on top the board. **Ensure that this fill is at least 40 mils from any "hot" DAA signal coming from the phone jack.**
   c) Connect the analog and digital ground planes together at a single point, preferably near a bracket.

Trace Widths

1. Minimize trace width variation on a given trace.
2. Provide 25 mil minimum width for power, ground, and critical signal traces.
3. Provide 15 mil minimum width for crystal traces.
4. Provide 10 mil (preferably 12 - 15 mil) minimum width for analog signal traces (e.g., the M_MIC_IN, M_LINE_OUT, M_LINE_IN, M_SPKR_OUT, VC, and VREF).
5. Provide 5 mil (preferably 10 mil) minimum width for all other traces.

Trace Spacing

1. Provide 15 to 40 mil minimum spacing between analog and digital ground traces.
2. Provide 40 mil minimum spacing around TIP and RING signal traces from the RJ-11 plug to the first resistor, then normal spacing after the resistor.
3. Provide 40 mil minimum spacing from BR1+ to the first resistor, then normal spacing after the resistor.
4. Provide 10 mil minimum spacing for all analog signals.
5. Provide 8 mil minimum spacing for all digital signals.

Trace Routing

1. Provide consistent trace routing. EMI radiation will occur every time a trace changes impedance, so avoid vias and try to keep a constant trace width for any given signal.
2. Keep high-speed digital traces as short as possible.
3. Keep sensitive analog traces as short as possible.
4. Provide maximum isolation between traces carrying noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, separate noise source traces and noise sensitive traces with traces carrying neutral signals.
5. Keep digital signals within the digital section and analog signals within the analog section (placement of isolation traces should prevent these traces from straying outside their respective sections).
6. Route digital traces perpendicular to analog traces to minimize signal cross coupling.
7. Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.
    a. Route an analog isolation ground trace or fill, at least 50 mil to 100 mil wide, around the border of the analog section; put on both sides of the PCB.
    b. Route a digital isolation ground trace or fill, at least 50 mil to 100 mil wide, and 200 mil wide on one side of the PCB edge, around the border of the digital section.
8. Route the traces between components by the shortest possible path (the components should have been previously placed to allow this).
9. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
10. Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.
11. Provide rounded or 45 degree corners. Avoid right angle (90 degree) turns on high frequency traces.
12. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
13. Keep all signal traces away from crystal circuits.
14. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
15. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes in the DAA circuit.
16. Eliminate ground loops, which are unexpected current return paths to the power source.

Specific Layout Guidelines for a 2-Layer SmartMC II Board

This section describes layout guidelines specifically for a 2-layer SmartMC II data/fax board.

Digital Section

Crystal Circuit

1. Place the two bypass capacitors, the series output resistor and the amplifier feedback resistor as close as possible to the HSD crystal pins to reduce induced noise levels and minimize any parasitic inductance and capacitance which could affect the crystal oscillator (Figure 17).

    Note: PCB layout of the crystal circuit is extremely critical; undesired parasitics due to poor layout may cause circuit instability preventing proper crystal circuit startup.

2. Keep the traces to the HSD crystal pins, XTLI (pin 23) and XTLO (pin 24), extremely short with no bend greater than 45 degrees and containing no vias (Figure 17).
3. Place digital ground fill under the crystal on top the board extending approximately 40 mils beyond the crystal case area. Do not put digital ground under the crystal case in the digital ground plane on the bottom of the board.
4. Connect the bypass capacitors directly to the digital ground fill.

DIB Interface

1. Place and rotate the HSD close to the AMR connector and to the DIB to minimize trace length of AC-Link and DIB signals.
2. Place the DIB transformer and DIB capacitors over the 110-mil (minimum gap = 2.7 mm = 106.3 mil) DAA isolation gap with the transformer closest to the HSD such that the PWRCLKP, PWRCLKN, DIB_DATAP, and DIB_DATAN traces can be routed with no more than one 90° turn rounded at no more than 45° angle, and without vias.

   Note: The PWRCLKP and PWRCLKN signals generate noise and the trace routing is extremely critical. The PWRCLKP and PWRCLKN traces must be extremely short, at least 10 mil wide, and be surrounded by GND guard band. Minimize the area used by the PWRCLKP and PWRCLKN traces.

AC-Link Signal Routing

1. Route the AC-Link interface signals directly to the AMR connector. The HSD pinouts are arranged such that signals can be routed to the AMR connector easily. The essential rules are: consistent trace aperture, minimum number of vias, trace bends at 45 degree angle maximum.
2. Provide 15-mil minimum trace width for the BIT_CLK clock signal. Keep the trace width as consistent as possible to minimize impedance change. The clocks should always be routed on the top of the board.

DAA Section

Note: A DAA is governed by local government regulations covering subjects such as component spacing, high voltage suppression, and current limiting.

DAA Isolation Gap

1. Provide a 110-mil gap (no traces within the gap) around the DAA section on the top and bottom of the board with the gap positioned directly under the DIB transformer and DIB capacitors.

DAA Section Grounding

1. Provide separate and isolated digital and analog areas in the DAA section.
2. Provide an isolated DAA analog ground plane (AGND_LSD) on the bottom of the board underneath the analog circuits and extending to the 110-mil gap on three sides and to midway underneath the LSD. **Do not provide a AGND_LSD plane on top of the board due to space restrictions. Leave analog components on top separated by gaps.**
3. Provide an isolated DAA digital ground plane (LSD_GND) on the bottom of the board underneath the digital components and extending to the 110-mil gap on three sides and to midway underneath the LSD. Place an LSD_GND plane on the top of the board, i.e., LSD_GND islands around components, and extending to the 110-mil gap on three sides and to midway underneath the LSD. Connect the top and bottom LSD_GND planes in several places with vias.
4. Connect to AGND_LSD and GND_LSD planes together at one tie point (U1) near AGND (pin 23) and GND (DGND).
5. Route separate traces from C28 to AVDD (pin 24) and from C28 to DVDD (Pin 26) to minimize noise coupling.
6. Route a single trace from C28 to C30.
7. Route a single trace from C28 to U1 (Ground Tie) then to AGND (pin 23).
8. All component connections to AGND_LSD should be through a via.

DIB Interface

1. Place the LSD within the DAA section such that the LSD side with analog signals (pins 9-16) is oriented toward the analog circuits, and the LSD side with digital signals (pins 25-32) is oriented toward the DIB. This should allow the DIB signals traces to be routed to components and to the LSD without vias.
2. Route the DIB power and clock signals from the DIB to the connecting diode and capacitors and then to the LSD with **extremely** short traces without vias. Try to keep all the components in the path of a straight trace. Route the DIB data signals from the DIB to the connecting resistors and then to the LSD with short traces without vias.

DC Hold and Impedance Match Interface

1. Place the components connecting to RXI (pin 3) extremely close to the RXI pin
2. Place Q6 close to TXF (pin 19) and TXO (pin 20), with TXF (pin 19) having priority.

3. Provide isolated heat sink planes on the top and bottom of the board for Q4 collector. Each plane area should be as large as possible (at least the width and twice the length of Q4). Connect the heat sink planes with no less than nine vias. Solder the Q4 tab (collector) to the top plane.

Diode Bridge

1. Route a 40-mil minimum trace directly from BR 1+ to the Q4 collector.
2. Route a 14-mil trace from thick trace to R6, C10 and C12.
3. Provide 40-mil spacing around the trace from BR1+ to the first resistor, then normal spacing after the resistor.

VC and VREF Circuit

1. Place C42 extremely close to VREF (pin 8) and VC (pin 7) and place C44 immediately next to C42.
2. Route a single extremely short trace from C42 to VREF (pin 8).
3. Route a single, short, straight trace from VC (pin 7) to the common nodes of C42 and C44.
4. Route an extremely short trace from C44 to a via connected to AGND_LSD.

Telephone Line Interface

1. Connect the 1000 pF 2 KV capacitor to Telephone Line TIP to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
2. Connect the 1000 pF 2 KV capacitor to Telephone Line RING to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
3. Provide 25-30 mil traces for the TIP and RING traces.
4. Provide 40-mil spacing around traces from TIP and RING at the RJ-11 plug to BR1 and the first resistor, then normal spacing after the resistor.
5. Provide 10 mil spacing minimum for other analog signal traces.
6. Minimize the number of signal traces on the bottom of the board.

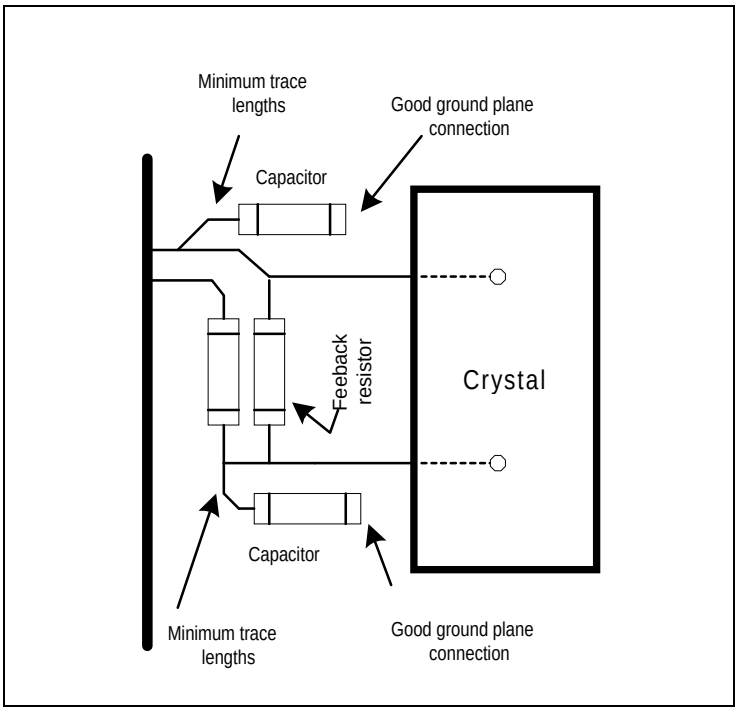
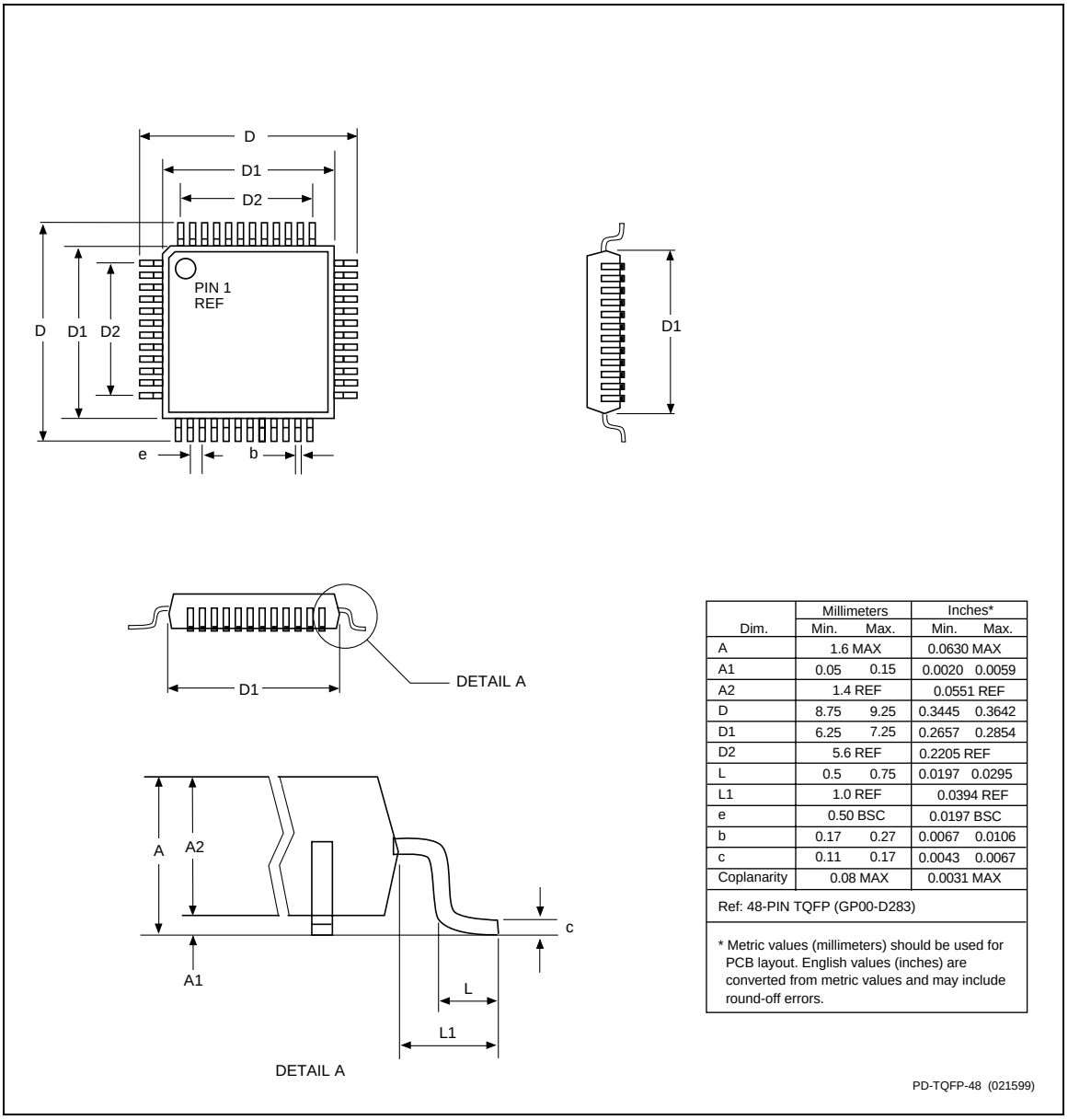


Figure 17. Crystal Solution

Package Dimensions

The package dimensions are shown in Figure 18 (48-pin TQFP) and Figure 19 (32-pin TQFP).

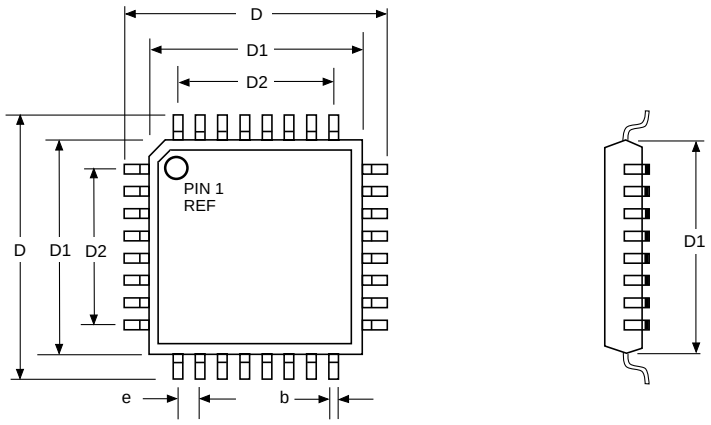


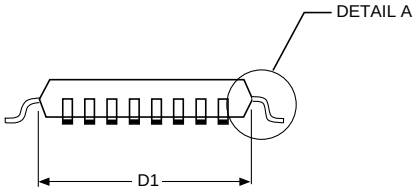
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	8.75	9.25	0.3445	0.3642
D1	6.25	7.25	0.2657	0.2854
D2		5.6 REF		0.2205 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

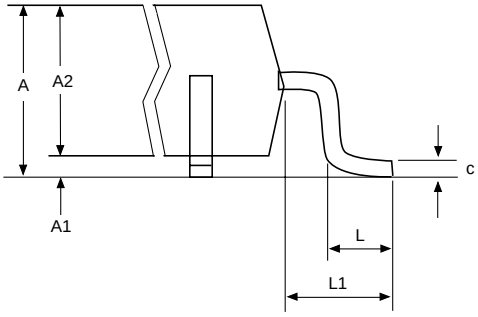
Ref: 48-PIN TQFP (GP00-D283)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 18. Package Dimensions - 48-Pin TQFP







Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	8.75	9.25	0.3445	0.3642
D1		7.0 REF		0.2756 REF
D2		5.6 REF		0.2205 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.80 BSC		0.0315 BSC
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-32 (040395)

Figure 19. Package Dimensions - 32-Pin TQF

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