CONFIDENTIAL

ENVY24HT

PCI Multi-Channel Audio Controller

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Ordering Information

- ICE1724 - 128PQFP

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Section 1: Introduction

The Envy24*HT*™ is a versatile PCI 24bit multi-channel audio controller that brings your computer at par with the fidelity of state-of-the-art home audio electronics, such as 24bit/192kHz DVD-Audio. It allows up to 10 outbound streams and 4 simultaneous inbound channels. All paths pass 24bit audio, “as is”, unaltered, bit per bit accurate. Some of the typical applications for this part are computer based high fidelity multi-channel audio, home theater and entertainment, cost effective multi-track audio, PC-based data acquisition, waveform generation. To maintain a full digital path for PCM or compressed audio formatc, the Envy24*HT* integrates a complete S/PDIF transmitter. All 5 output and 2 input pairs can be combined with professional grade I²S converters, S/PDIF receivers or multi-channel out AC-link codecs, such as the VT1616™.

The Envy24*HT* supplies a master I²C interface providing connection to an E²PROM to store and retrieve PCI Subsystem and Subsystem vendor IDs, specific board configurations and custom features identification.

The Envy24*HT* integrates an independent MPU-401 MIDI UART.

Direct access GPIOs brings flexibility for multi-purpose use.

The Envy24*HT* is ACPI compliant making it suitable for platforms designed to be instantly on.

Depending on the sampling rates that need to be supported by the target solution, one or two crystals are sufficient to operate the whole system. For more detail on the part, please refer to the system block diagram Figure 4-1 in Section 4.

1.1 Features

- PCI 2.2 I/F with bus mastering and burst modes
- 24-bit resolution audio format support
- Bit accurate transfers
- Sampling rates up to 192kHz
- 5 synchronous I²S/AC-link ouput data stream pairs
- 2 synchronous I²S/AC-link input data stream pairs
- Multi-channel AC-link supported alternatively
- Integrated S/PDIF transmitter with IEC958 line driver
- Digital loopback and stream routing mechanism
- Peak meters on all streams
- MPU-401 MIDI UART port
- ACPI and PCI PMI support
- I²C subset I/F for E²PROM (configuration and ID storage) and peripherals control
- 23-pin, direct access GPIO port
- Windows® WDM drivers
- 49.152/24.576 and 22.5792 MHz crystal operation
- 3.3V operating supply (5V tolerant I/O)
- 128-pin PQFP (14mm x 20mm body)

1.2 Applications

- “Pro-sumer” audio
- High Fidelity audio reproduction
- PC-based Home Theater
- PC-based multi-channel audio like DVD-Audio
- PC-based multi-track audio recording
- General purpose multi-channel I/O
- PC-based data acquisition
- PC-based waveform generation
- PC-based instrumentation

Section 2: Pins

The following section includes the pinout diagram of the chip that is housed in a standard 128-PQFP. Also, three lists of pin assignments are provided for your convenience. They are logically sorted by functionality and description, alphabetically and numerically sorted in ascending order. These list are provided to assist hardware development, test, debugging and quality assurance. The mechanical data about the part can be found in Section 6.

2.1 Pinout Diagram

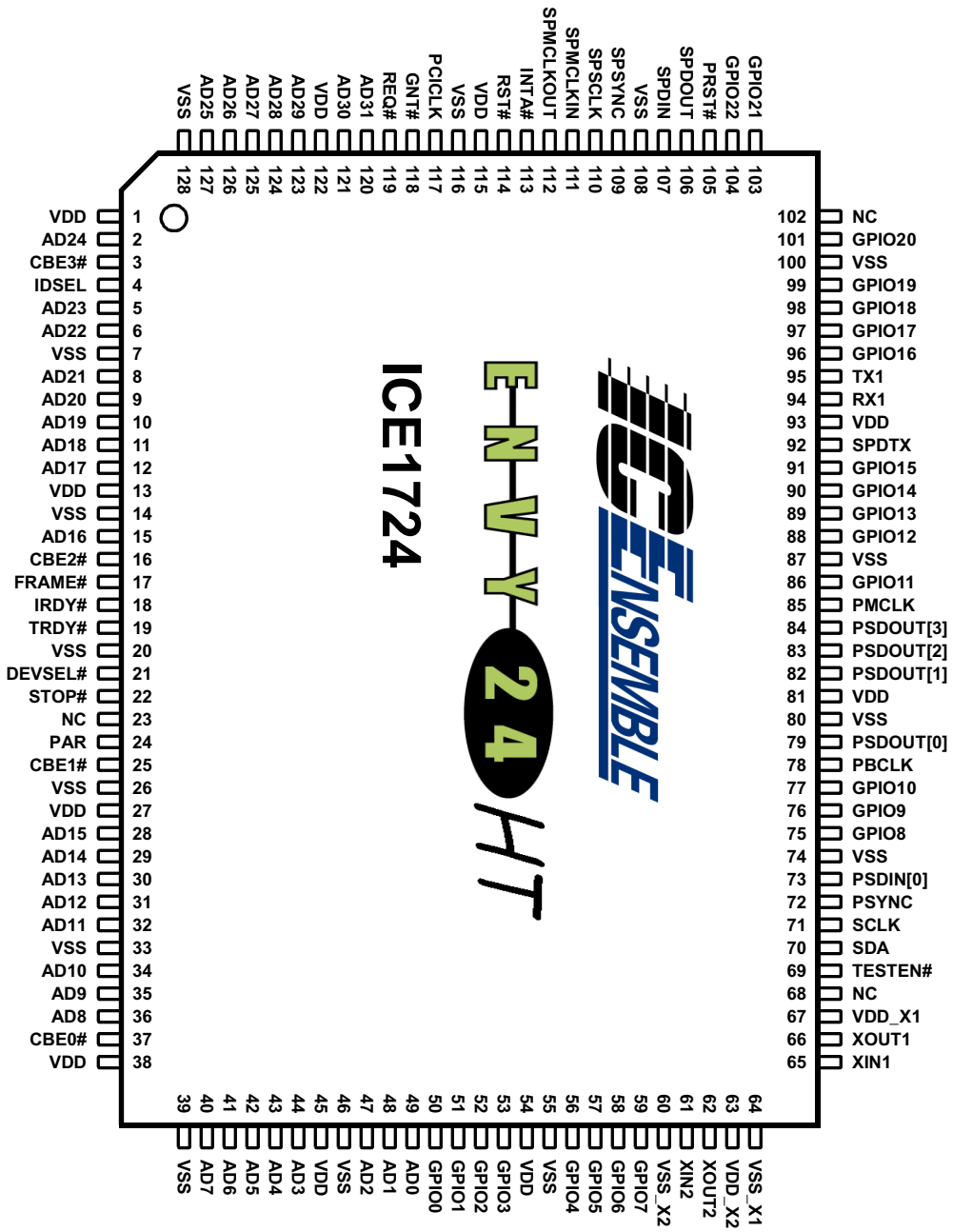

Figure 2-1. 128-pin PQFP Package

2.2 Pin Descriptions

The following table provides a brief description of each pin of the ICE1712. Pins with dual usage may be listed twice for consistency. Please note that all the PCI bus pins are 5V tolerant. The following abbreviations are used to identify the pin types.

I - Input Signal

O - Output Signal

B - Bidirectional Signal

OD - Open Drain

A - Analog Signal

PU - Pull-up. 50kΩ nominal

Table 2-1. Pin Descriptions

Symbol	Type	Description
PCI BUS INTERFACE		
AD[31:0]	B	Multiplexed PCI Address/Data Bus.
CBE#[3:0]	B	Bus command/Byte Lane Enable. These signals are bus commands during the address phase and byte lane enable during the data phase. These signals are output during a bus master cycle.
PCICLK	I	PCI Bus Clock.
DEVSEL#	B	Device Select. The ICE1724 drives this signal active when it decodes its address as the current target of the current acces.
FRAME#	B	PCI Cycle Frame. When asserted by the bus mster, this signal indicates the beginning of a bus transaction.During the final data phase of a bus transaction it is deasserted.
GNT#	I	When active it indicates bus master is granted to ICE1724.
IDSEL	I	Initialization Device Select. This is the chip select during the PCI configuration register accesses
INTA#	OD	PCI Interrupt Request.
IRDY#	B	Initiator Ready.
PAR	B	Parity Signal.
REQ#	O	Bus master control request
RST#	I	System Reset. All ICE1724 registers and state machines are at default when this signal is asserted.
STOP#	B	Target disconnect signal.
TRDY#	B	Target Ready.
I^2C PORT		
SDA	B	Serial bidirectional dat.
SCLK	O	Serial bit shift clock

Table 2-1. Pin Descriptions (continued)

Symbol	Type	Description
MPU-401 UART		
TX1	O, PU	MPU-401 Transmit data
RX1	I, PU	MPU-401 Receive data
PROFESSIONAL MULTI-TRACK AC-LINK / I²S INTERFACE		
PSYNC	O	AC'97: 48kHz fixed rate sync pulse for up to 4 codecs, or 8 I²S type converters: Left/Right Clock
PBCLK	I/O	Serial Bit Clock. It can be master or slave configured
PSDIN[1:0]	I	2 separate incoming stereo stream pairs
PSDOUT[3:0]	O	4 separate outbound stereo stream pairs
PMCLK	O	Master Clock for AC'97 codecs or I²S converters
PRST#	O	Cold reset for I²S/AC-link converters
CLOCKS		
XOUT1	A	Clock Out 1
XIN1	A	49.152 (256*192kHz)/24.576MHz (512*48kHz). Runs the core blocks.
XOUT2	A	Clock Out 2
XIN2	A	22.5792MHz (512*44.1kHz)
S/PDIF (SONY/PHILIPS DIGITAL INTERFACE)		
SPMCLKIN	I	S/PDIF Master Clock Input or other 256X clock for salve operation
SPMCLKOUT	O	S/PDIF Master Clock Output is PMCLK/2 or /4, 128X PSYNC
SPSCLK	O	S/PDIF Serial Bit Clock
SPDIN	I	Incoming S/PDIF Serial Data
SPDOUT	O	Copy of Outbound S/PDIF Serial Data present on SPDTX
SPDTX	A, PU	S/PDIF out IEC958 line driver output. The voltage divider implemented on the board will pull down signaling that the digital audio transmitter is implemented via bit CCS07_0.
SPSYNC	O	S/PDIF Frame Sync
GENERAL PURPOSE I/O		
GPIO[22:4]	B, PU	General Purpose I/O. Capable of driving 8mA.
GPIO3 / E²PROM	B, PU	General Purpose I/O. E²PROM presence indicator during power-up (default). The state is reflected on CCS13_7 bit. Capable of driving 8mA.
GPIO[2:1]	B, PU	General Purpose I/O. Capable of driving 8mA.
GPIO0 / I²S#	B, PU	General Purpose I/O. Sets AC-link interface for professional section during power-up (default). The state is reflected on PCI61_7 bit in reverse polarity. Capable of driving 8mA.
TEST MODE		
TESTEN#	I, PU	Test mode enable. Do not connect for normal operation.

Table 2-1. Pin Descriptions (continued)

Symbol	Type	Description
POWER AND GROUND		
VDD		3.3V digital supply
VSS		Ground

2.3 Pin Lists

Table 2-2 lists all the pins alphabetically. **Table 2-3** lists all the pins in numerical order.

Table 2-2. Alphabetical Pin Listing

Symbol	Pin(s)
AD[31:0]	2, 5-6, 8-12, 15, 28-32, 34-36, 40-44, 47-49, 120-121, 123-127,
CBCLK	90
CBE#[3:0]	3, 16, 25, 37
CMCLK	92
CRST#	86
CSDIN	89
CSDOUT	91
CSYNC	88
DEVSEL#	21
FRAME#	17
GNT#	118
GPIO[0]/I²S#	50
GPIO[1]	51
GPIO[2]	52
GPIO[3]/E²PROM	53
GPIO[22:4]	56-59, 75-77, 86, 88-91, 96-99, 101, 103-104
IDSEL	4
INTA#	113
IRDY#	19
NC	23, 68, 102
PAR	24
PBCLK	78
PCICLK	117
PMCLK	85
PRST#	105
PSDIN0	73
PSDOUT[3:0]	79, 82-84
PSYNC	72
REQ#	119
RST#	114

Table 2-2. Alphabetical Pin Listing (continued)

Symbol	Pin(s)
RX1	94
SCLK	71
SDA	70
SPDIN	107
SPDOUT	106
SPDTX	92
SPMCLKIN	111
SPMCLKOUT	112
SPSCLK	110
SPSYNC	109
STOP#	22
TESTEN#	69
TRDY#	19
TX1	95
VDD	1, 13, 27, 38, 45, 54, 81, 93, 115, 122
VDD_X1	67
VDD_X2	63
VSS	7, 14, 20, 26, 33, 39, 46, 55, 74, 80, 87, 100, 108, 116, 128
VSS_X1	64
VSS_X2	60
XIN[2:1]	61, 65
XOUT[2:1]	62, 66

Table 2-3. Numerical Pin Listing

Pin #	Symbol		Pin #	Symbol
1	VDD		65	XOUT1
2	AD24		66	VDD_X1
3	CBE3#		67	VDD
4	IDSEL		68	VSS
5	AD23		69	TESTEN#
6	AD22		70	SDA
7	VSS		71	SCLK
8	AD21		72	PSYNC
9	AD20		73	PSDIN[0]
10	AD19		74	VSS
11	AD18		75	GPIO8
12	AD17		76	GPIO9
13	VDD		77	GPIO10
14	VSS		78	PBCLK
15	AD16		79	PSDOUT[0]
16	CBE2#		80	VSS
17	FRAME#		81	VDD
18	IRDY#		82	PSDOUT[1]
19	TRDY#		83	PSDOUT[2]
20	VSS		84	PSDOUT[3]
21	DEVSEL#		85	PMCLK
22	STOP#		86	GPIO11
23	NC		87	VSS
24	PAR		88	GPIO12
25	CBE1#		89	GPIO13
26	VSS		90	GPIO14
27	VDD		91	GPIO15
28	AD15		92	SPDTX
29	AD14		93	VDD
30	AD13		94	RX1
31	AD12		95	TX1
32	AD11		96	GPIO16
33	VSS		97	GPIO17

Table 2-3. Numerical Pin Listing (continued)

Pin #	Symbol		Pin #	Symbol
34	AD10		98	GPIO18
35	AD9		99	GPIO19
36	AD8		100	VSS
37	CBE0#		101	GPIO20
38	VDD		102	NC
39	VSS		103	GPIO21
40	AD7		104	GPIO22
41	AD6		105	TX2
42	AD5		106	SPDOUT
43	AD4		107	SPDIN
44	AD3		108	VDD
45	VDD		109	SPSYNC
46	VSS		110	SPSCLK
47	AD2		111	SPMCLKIN
48	AD1		112	SPMCLKOUT
49	AD0		113	INTA#
50	GPIO[0]		114	RST#
51	GPIO[1]		115	VDD
52	GPIO[2]		116	VSS
53	GPIO[3]		117	PCICLK
54	VDD		118	GNT#
55	GPIO[4]		119	REQ#
56	GPIO[5]		120	AD31
57	GPIO[6]		121	AD30
58	GPIO[7]		122	VDD
59	VSS_X2		123	AD29
60	XIN2		124	AD28
61	XOUT2		125	AD27
62	VDD_X2		126	AD26
63	VSS_X1		127	AD25
64	XIN1		128	VSS

Section 3: PCI Interface and Configuration

Table 3-1. PCI Host Interface Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
Device Identification		Vendor Identification		00
PCI Device Status		PCI Command		04
Class Code		Reserved. Read as 0	Revision ID	08
BIST	Header Type	Latency Timer	Reserved. Read as 0	0C
Controller I/O Base Address				10
Multi-Channel I/O Base Address				14
-				18
-				1C
Subsystem ID		Subsystem Vendor ID		2C
Reserved. Read as 0				30
Capability Pointer				34
Reserved. Read as 0				38
Minimum Latency and Maximum Grant		Interrupt Pin and Line		3C
	SVID Mask			40
Hardware Configuration Control				60
Power Management Capability		Next Item Pointer	Capability ID	80
PMCSR Support Extensions and Data		Power Management Control and Status		84

3.1 Envy24*HT* PCI Configuration Registers

PCI00: Vendor Identification Register

Address Offset: 00 - 01h

Default Value: 1412h

Bit	Attribute	Description
15:0	RO	Vendor Identification Number. This is the 16-bit value assigned to IC Ensemble, Inc.

PCI02: Device Identification Register

Address Offset: 02 - 03h

Default Value: 1724h

Bit	Attribute	Description
15:0	RO	Device Identification Number. 1724 reflects the part number.

PCI04: PCI Command Register

Address Offset: 04 - 05h

Default Value: 0000h

Bit	Attribute	Description
15:10	R0b	Reserved. Read as 0s.
9	R0b	Fast Back-to-Back Enable. This bit is hardwired to 0 (Not Implemented).
8	R/W	SERR# enable. Hardwired to 0 (Not Implemented).
7	R0b	A/D stepping enable. This bit is hardwired to 0 (Not Implemented).
6	R0b	Parity error detect enable. Hardwired to 0 (Not Implemented).
5	R0b	VGA palette snoop enable. Hardwired to 0 (Not Implemented).
4	R0b	Memory write and invalidate enable. Hardwired to 0 (Not Implemented).
3	R0b	Special Cycle Enable (SCE). Hardwired to 0 (Not Implemented).
2	R/W	Bus master enable. 1=enable. 0=disable (default).
1	R0b	Memory Access. Hardwired to 0 (Not Implemented).
0	R/W	I/O Space accesses enable. 1=enable. 0=disable (default).

PCI06: PCI Status Register

Address Offset: 06 - 07h

Default Value: 0210h

Bit	Attribute	Description
15	R/W/C	PAR status. Parity error detected (even when parity not enabled).
14	R/W/C	SERR# status. Read as 0 (Not Implemented).
13	R/W/C	Master abort status. This bit is set to 1 when master aborts and cleared by writing "1" to it.
12	R/W/C	Received target abort status. This bit is set to 1 when target abort is received and cleared by writing a 1 to it.
11	R0b	Signaled target abort status. This bit is set when target abort generated and cleared by writing a 1 to it. Hardwired to 0 (never abort).
10:9	R10b	DEVSEL# timing status. Envy24 always asserts DEVSEL# with medium timing.
8	R0b	PERR# response. Read as 0 (Not Implemented).
7	R0b	Fast back to back. Read as 0 (Not implemented).
6	R0b	User Define Function (UDF). Read as 0 (Not implemented).
5	R0b	Reserved. Read as 0. 33MHz only.
4	R1b	Hardwired to 1 to indicate the support for PCI power management capability.
3:0	R0000b	Reserved. Read as 0s.

PCI08: Revision ID Register

Address Offset: 08h - 09h

Default Value: 000Xh

Bit	Attribute	Description
15:0	R00h	-
7:0	RO	Revision ID

PCI0A: Class Code Register

Address Offset: 0Ah - 0Bh

Default Value: 0401h

Bit	Attribute	Description
15:8	RO	Base Class. Reflects Multimedia
7:0	RO	Sub class. Reflects Audio.

PCI0C: Cache Size Register

Address Offset: 0Ch

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0. Not supported

PCI0D: Latency Timer Register

Address Offset: 0Dh

Default Value: 00h

Bit	Attribute	Description
7:3	R/W	Latency timer
2:0	RO	Read as 0

PCI0E: Header Type Register

Address Offset: 0Eh

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0

PCI0F: BIST Register

Address Offset: 0Fh

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0. Not supported

PCI10: Envy24HT I/O Base

Address Offset: 10h - 13h

Default Value: 00000001h

Bit	Attribute	Description
31:5	RW	Controller I/O Base Address for CCSxx registers described in chapter 4
4:1	R0h	Hardwired to 0 to have 32 bytes I/O space. This includes UARTs and game port.
0	R1b	Hardwired to 1 to indicate registers map to I/O space

PCI14: Multi-Channel I/O Base

Address Offset: 14h -17h

Default Value: 00000001h

Bit	Attribute	Description
31:7	R/W	Multi-Channel I/O Base Address for MTxx registers described in chapter 4
6:1	R0	Hardwired to 0 to have 128 bytes I/O space
0	R1b	Hardwired to 1 to indicate registers map to I/O space

PCI2C: Sub-Vendor ID

Address Offset: 2Ch - 2Fh

Default Value: 17241412h

Bit	Attribute	Description
31:0	RO	Sub-vendor ID: Read it from external E²PROM after reset if it exists, otherwise, same as vendor ID. It can also be written by disabling write protection bit defined in PCI42_7.

PCI34: Capability Pointer

Address Offset: 34h

Default Value: 80h

Bit	Attribute	Description
7:0	RO	CP7-CP0: Capability data structure pointer for PCI power management. Hardwired to 80h.

PCI34: Interrupt Pin and Line

Address Offset: 3Ch - 3Dh

Default Value: 01FFh

Bit	Attribute	Description
15:8	RO	01h read from this register indicates the interrupt pin used is INTA# and cannot be modified.
7:0	R/W	Interrupt line routing information set by POST during power-up initialization. Default FFh indicates no connection to the PIC yet.

PCI3E: Latency and Grant

Address Offset: 3Eh - 3Fh

Default Value: 0000h

Bit	Attribute	Description
15:8	RO	Maximum latency
7:0	RO	Minimum grant

PCI42: Subsystem ID Mask

Address Offset: 42h

Default Value: 0000h

Bit	Attribute	Description
		Reserved
7	R/W	0: SVID read only. (default) 1: SVID read/write enable.

PCI80: Capability ID

Address Offset: 80h

Default Value: 01h

Bit	Attribute	Description
7:0	RO	Capability ID

PCI81: Next Item Pointer

Address Offset: 81h

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Hardwired to 0 to indicate the end of list

PCI82: Power Management Capabilities

Address Offset: 82h - 83h

Default Value: 0401h

Bit	Attribute	Description
15:11	RO	PME not supported. Hardwired to 0.
10	R1	D2 state support. Hardwire to 1.
9	R0	D1 state not support. Hardwired to 0.
8:6	R000	Reserved.
5	R0	DSI. Hardwired to 0.
4	R0	Aux. Power. Hardwired to 0
3	R0	PMC clock for generation of PME#. Hardwired to 0.
2:0	R001b	Hardwired to 001 to indicate PPMI 1.0 compliance

PCI84: Power Management Control and Status

Address Offset: 84h - 85h

Default Value: 0000h

Bit	Attribute	Description
15	R0b	PME status. Read as 0.
14:13	R00b	Data scale. Not supported.
12:9	R0h	Data select: Not supported.
8	R0b	PME assertion. Hardwired to 0
7:2	RO	Hardwired to 000000
1:0	R/W	Power state. To determine the current state of power state. 00 : D0 01 : D1 (not supported) 10 : D2 11 : D3_hot

There are four power states defined in the PCI bus power management spec.

States	Description
D0	Normal operation state after system power up or internal reset
D1	not supported.
D2	Power down all the blocks defined in the power down registers.
D3(hot)	Same as D2 state, except a transition to D0 will generate an internal reset (incl. PCI config. space)

PCI86: PMCSR_Base and Data

Address Offset: 86h - 87h

Default Value: 0000h

Bit	Attribute	Description
15:0	R0000h	-

Section 4: Hardware Interfaces

In the previous section PCI host interface and configuration registers were discussed. In this section description of the major blocks, their respective hardware interfaces and associated registers will be discussed.

The first figure in this section, **Figure 4-1**, is a chip level block diagram with typical external interface usage. It is a very good overview of the whole chip, but should not be regarded as the most detailed diagram. As appropriate, the databook will resort to sub-block diagrams to further detail the functionality. These are the multi-track DMA transfer mechanism, data stream routing capabilities and the digital mixer block diagram.

The following descriptive summary can be considered along with **Figure 4-1**. In its default state, the ICE1724 has an 8 interleaved DMA and an independent, concurrent stereo pair which is tied to the integrated SPDIF transmitter but the same data is simultaneously available at the corresponding I²S data output pin. The ganged channels can be disengaged to form independent stereo pairs while leaving the remainder tightly coupled in even quantity of channels, i.e. 8, 6, 4 or 2 ganged. This means that the part can output 5 simultaneous, independent stereo pairs that are not tightly time correlated as if it would be in the interleaved mode. See register MT19 for the various setting if you want to depart from the default mode.

The incoming data stream, i.e. the Record DMA channels are always set as 2 independent and simultanous pairs.

The above description about the flexiblity of the ICE1724 leads to effective use of bus bandwidth yet does not abandon the time correlation of multichannel streams or independent stereo operation without disturbing other stream that may start, stop or pause at random times, independent from one another.

Since there is always a single master clock to run the system, regardless whether in master or slave mode, even in the independent stereo mode, all streams must be at the same sampling rate, including the S/PDIF output path and the record channels.

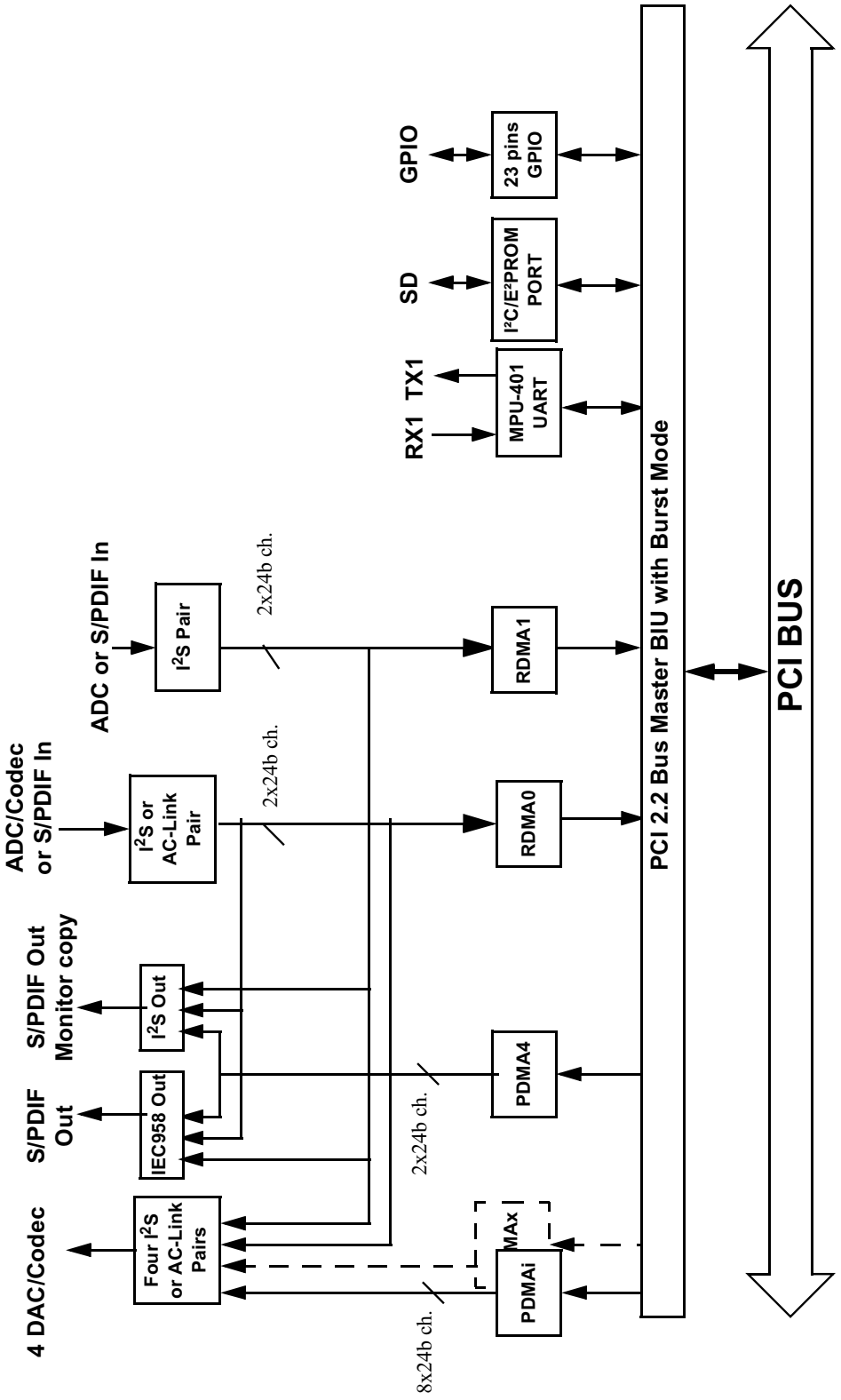

Figure 4-1. Functional Block Diagram

4.1 Controller Registers

The following registers are offset from base address set by PCI10. The 32 bytes I/O space includes main control/status registers, I^2C interface, MPU-401 MIDI UARTs and game port control as well. Each CCSxx register is physically located at the address determined by [PCI10]+xx and accessed directly. The registers can be accessed as a byte, word or dword register.

Table 4-1. CCSxx Controller Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
-	Envy24HT Status	Interrupt Mask	Global	00
S/PDIF Configuration	I²S Configuration	AC-link Configuration	System Configuration	04
RX UART queue	TX UART queue	-		08
-	UART Setting	UART Comm./Status	MIDI UART Data	0C
I²C Port Control/Status	I²C Port R/W Data	I²C Port Byte Address	I²C Port Dev. Address	10
GPIO[15:0] Write Mask Register		GPIO[15:0] Data Register		14
-	GPIO[22:0] Direction Register			18
GPIO[22:16] W. Mask	GPIO[22:16] Data Reg.	-	Power Down	1C

CCS00: Control/Status Register

Address Offset: 00h

Default Value: 00h

Bit	Attribute	Description
7	R/W	Entire Chip soft reset
6:0	R/W	Reserved

CCS01: Interrupt Mask Register

Address Offset: 01h

Default Value: FEh

Bit	Attribute	Description
7	R/W	MPU-401 MIDI UART receive interrupt mask. See CCS0E for high watermark setting.
6	R/W	Reserved
5	R/W	MPU-401 MIDI UART transmit interrupt mask. See CCS0E for low watermark setting.
4	R/W	Multi-channel playback and record. This is the macro interrupt mask for any P and RDMAx.
3:0	R/W	Reserved

CCS02: Interrupt Status Register

Address Offset: 02h

Default Value: 00h.

These bits are sticky and only writing a 1 to that bit location will clear itself.

Bit	Attribute	Description
7	R/W/C	MPU-401 MIDI UART receiver FIFO
6	R/W	Reserved
5	R/W/C	MPU-401 MIDI UART transmit FIFO
4	RO	Multi-channel playback or record. This is the macro interrupt status for any PDMAx and RDMAx. To clear individual status bit, write a 1 to the associated bit location defined in section 4.2, MT00.
3:0	R/W	Reserved

CCS04: System Configuration Register

Address Offset: 04h

Default Value: 0Fh

The following four bytes (04h-07h) have to be read from E^2PROM by driver and then written to setup the codec configuration, unless otherwise noted.

Bit	Attribute	Description
7:6	R/W	XIN1 Clock Source Configuration. Refer to register MT01. 00: XIN1: 24.576MHz crystal (96kHz*256) 01: XIN1: 49.152MHz crystal (192kHz*256) 1x: - Reserved
5	R/W	1: MPU-401 UART implemented 0: MPU-401 UART not implemented.
4	R/W	-Reserved
3:2	R/W	00: one stereo ADC connected 01: two stereo ADCs connected 10: one stereo ADC and a S/PDIF receiver connected 11: No physical inputs
1:0	R/W	Must have at least one stereo pair DAC. 00: one stereo DAC connected 01: two stereo DACs connected 10: three stereo DACs connected 11: four stereo DACs connected

CCS05: AC-Link Configuration Register

Address Offset: 05h

Default Value: 00h

Except for bit 7, the four bytes at CCS04 should be read from E^{2}PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	Multi-channel converter type: 0: AC'97 1: I²S. Reflects power-up status of pin 50 during reset cycle in reverse polarity. Can be overwritten.
6:2	R/W	Reserved.
1	R/W	If bit 7 is 0, i.e. AC'97 mode, it may affect the DMA to pin mappings where the audio streams are transferred to. See description in MT05[1:0] and **Table 4-3**. 0: split mode: AC'97 codec SDATA_OUT split to different pin outputs, PSDOUT[3:0]. The individual stereo AC'97 codecs like VT1611A should be properly IDed. 1: AC-link packed mode: AC'97 codec SDATA_OUT packed in slots per AC'97 2.2 spec only on PSDOUT0 (pin79). See VT1616 spec as the codec to be used in this mode.
0	R/W	Reserved.

CCS06: I^{2}S Converters Features Register

Address Offset: 06h

Default Value: 01h

This byte is valid only when CCS05_7 is 1. The four bytes at CCS04 should be read from E^{2}PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	For I²S codec Volume and mute 0: I²S codec has no volume/mute control feature. 1: I²S codec has volume/mute control capability and need to be program through GPIO (e.g., CS4222)
6	R/W	I²S converter 96kHz sampling rate support. 0: does not; 1 : supports
5:4	R/W	Converter resolution: 00: 16-bit 01: 18-bit 10: 20-bit 11: 24-bit
3	R/W	I²S converter 192kHz sampling rate support. 0: does not; 1 : supports
2:0	R/W	Other I²S IDs

CCS07: S/PDIF Configuration Register

Address Offset: 07h

Default Value: 01h

The four bytes at CCS04 should be read from E^2PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	1: Enable integrated S/PDIF transmitter. Valid only when bit 6 of this register is '1'. Must be disabled to change mode via MT3C.
6	R/O	1: Internal S/PDIF Out implemented. Reflects the state of pin 92, SPDTX during reset. If '0', the transmitter is not implemented on the board. Note that it is reverse polarity of pin 92 reset state.
5:2	R/W	S/PDIF chip IDs
1	R/W	1: S/PDIF Stereo In is present.
0	R/W	1: External S/PDIF Out implemented.

CCS0A: UART TX FIFO Queue Status Register

Address Offset: 0Ah

Default Value: 00h

Description: This read-only register reflects the number of valid bytes in hex form, ready to be transmitted on TX1 (pin95) from the TX FIFO. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:5	RO	Reserved.
4:0	RO	Valid MPU-401 data bytes in TX FIFO.

CCS0B: UART RX FIFO Queue Status Register

Address Offset: 0Bh

Default Value: 00h

Description: This read-only register reflects the number of valid bytes hex form, to be read by the host from the RX FIFO. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:5	RO	Reserved.
4:0	RO	Valid MPU-401 data bytes in RX FIFO.

CCS0C: MIDI UART Data Register

Address Offset: 0Ch

Default Value: 00h

Bit	Attribute	Description
7:0	R/W	MIDI UART data register

CCS0D: MIDI UART Command/Status Register

Address Offset: 0Dh

Default Value: 00h

Bit	Attribute	Description
7:0	R/W	MIDI UART command and status register

CCS0E: UART Setting Register

Address Offset: 0Eh

Default Value: 00h

Description: This register allows setting high/low watermarks for RX/TX FIFO interrupts to avoid polling or constant interruption during heavy system activity. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:6	R/W	Reserved.
5	R/W	1: Receive FIFO high watermark setting. 0: Transmit FIFO low watermark setting.
4:0	R/W	Enter the watermark value, between 0 and 31 (00h to 1Fh). Both RX and TX FIFO are 32-bytes. The default watermark level is 0 for both TX and RX.

CCS10: I^2C Port Device Address Register

Address Offset: 10h

Default Value: 00h

Each write to this register will trigger to start the read/write cycle. So, before write to this I/O address, driver needs to check to make sure that the status bit is idle as defined in the I²C status register CCS13. The controller is always the only master and does not support multi-byte data burst mode.

Bit	Attribute	Description
7:1	R/W	I^2C device address. Device address "1010000" is reserved for the external I²C E2PROM such as 24C02 for sub-vendor ID and configuration data.
0	R/W	0: read 1: write

CCS11: I²C Port Byte Address Register

Address Offset: 11h

Default Value: 00h

Bit	Attribute	Description
7:0	R/W	Byte address to read or write

CCS12: I²C Port Read/Write Data Register

Address Offset: 12h

Default Value: 00h

Bit	Attribute	Description
7:0	RW	Read or write data

CCS13: I²C Port Control and Status Register

Address Offset: 13h

Default Value: 00h

When bit 0 is 0 (meaning the I²C port is idle), SCLK (pin 71) will be tri-stated. Envy24HT is providing the serial clock only when it reads/writes through I²C bus at a nominal rate of 31.25kHz.

Bit	Attribute	Description
7	RO	Reflects the power strapping on GPIO3 (pin 53). A 1 (default) indicates external E²PROM exists. A 0 (pull down by a resistor) means, no external E²PROM connected.
6:2	0	-
1	R/W	Reserved. Keep at 0 state.
0	RO	I²C port read/write status. 0: idle 1: busy

CCS14: GPIO Data Register

Index: 14 -15h

Default Value: 0000h

The direction is set up in CCS18, the GPIO direction control register (see CCS1E for MSB GPIO Data Register). These register bits can be writable only when the corresponding mask bit is zero in the mask register, CCS16. If the direction is output, it reads back the last data written. The use of these will depend upon board configuration as defined by the E²PROM settings content. See CCS04 register description for more details.

Bit	Attribute	Description
15:0	R/W	GPIO data (Warning: few GPIO pins may be shared with other functions)

CCS16: GPIO Write Mask Register

Index: 16 - 17h

Default Value: FFFFh

Bit	Attribute	Description
15:0	R/W	GPIO15 through GIO0 write mask 0: Corresponding CCS14 register bit can be written. 1: Can NOT be written.

CCS18: GPIO Direction Control Register

Index: 18h - 1Ah

Default Value: 000000h

Bit	Attribute	Description
22:4	R/W	GPIO22 through GPIO4 direction.
3	R/W	GPIO3 direction. During reset, this pin is used for E²PROM power-on strapping.
2	R/W	GPIO2 direction. If TESTEN# pin is active, this pin is always input.
1:0	R/W	GPIO1 and GPIO0 direction.

For all bits 0: input; 1: output.

CCS1C: Power Down Register

Index: 1Ch

Default Value: 00h

Bit	Attribute	Description
7	R/W	1: Crystal clock generation power down for XTAL_1
6	R/W	Reserved
5	R/W	1: Crystal clock generation power down for XTAL_2
4	R/W	1: Stop I²C port clock
3	R/W	1: Stop MIDI clock
2	R/W	1: Stop S/PDIF clock
1	R/W	Reserved.
0	R/W	1: Stop Multi-channel I²S serial interface clock

CCS1E: GPIO Data Register

Index: 1Eh

Default Value: 00h

The direction is set up in CCS18, the GPIO direction control register (see CCS14 for LSW GPIO Data Register). These register bits can be writable only when the corresponding mask bit is zero in the mask register CCS1F. Also, if the direction is output, it reads back the last data written.

Bit	Attribute	Description
6:0	R/W	GPIO22 through GPIO16 data

CCS1F: GPIO Write Mask Register

Index: 1Fh

Default Value: FFh

Bit	Attribute	Description
6:0	R/W	GPIO22 through GIO16 write mask 0: Corresponding CCS1E register bit can be written. 1: Can NOT be written.

4.2 Multi-Channel Control Registers

The following registers are offset from base address set by PCI14. The MTxx registers are located at [PCI14]+xx. The 128 bytes I/O space controls the multi-channel record and playback, audio stream routing, digital mixer and related output capability. The Playback DMA default organization is 8 interleaved and a concurrent, independent stereo pair tied to the SPDIF out linedriver and a copy to the respective I²S data out pin. Refer to the introduction of this chapter for a concise description of the DMA channels involved.

Table 4-2. MTxx Controller Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
DMA Interrupt Mask	I²S data format	Sampling Rate Select.	DMA Interrupt Status	00
AC '97 Data Port		AC '97 Comm./Stat.	AC '97 Index	04
-				08
-				0C
Interleaved Playback DMA (PDMAi) Current/Base Address				10
-	PDMAi Current/Base Count			14
Global DMA Pause/R.	Underrun/Overrun	PDMAi Burst Size	Global DMA Start/Stop	18
-	PDMAi Current/Base Terminal Count			1C
Record DMA 0 (RDMA0) Current/Base Address				20
Record DMA 0 Current/Base Terminal Count		Record DMA 0 Current/Base Count		24
-				28
Routing control to PSDOUT[3:0] and SPDOUT				2C
Record DMA 1 Current/Base Address				30
Record DMA 1 Current/Base Terminal Count		Record DMA 1 Current/Base Count		34
-				38
Peak meter data	Peak meter index	S/PDIF IEC958 Control Register		3C
Playback DMA 4 (PDMA4)/ S/PDIF output Current/Base Address				40
PDMA4 Current/Base Terminal Count		PDMA4 Current/Base Count		44
Playback DMA 3 (PDMA3) output Current/Base Address				50
PDMA3 Current/Base Terminal Count		PDMA3 Current/Base Count		54
Playback DMA 2 (PDMA2) output Current/Base Address				60
PDMA2 Current/Base Terminal Count		PDMA2 Current/Base Count		64
Playback DMA 1 (PDMA1) output Current/Base Address				70
PDMA1 Current/Base Terminal Count		PDMA1 Current/Base Count		74

4.2.1 Multi-Channel Mode Registers

MT00: DMA Interrupt Status Register:

Address Offset: 00h

Default Value: 00h

This register relates to both all DMA operation modes. When DMAs are stopped, the last latched value is retained. This "DC" value may affect the converters state.

Bit	Attribute	Description
7	R/W/C	SPDIF Out/PDMA4 pair playback interrupt status. Write a 1 to clear.
6	R/W/C	PDMA3 pair playback interrupt status. Write a 1 to clear.
5	R/W/C	PDMA2 pair playback interrupt status. Write a 1 to clear.
4	R/W/C	PDMA1 pair playback interrupt status. Write a 1 to clear.
3	R/W/C	DMA FIFO underrun/overrun condition. See MT1A for status.
2	R/W/C	RDMA1 (typically S/PDIF input) pair record interrupt status. Write a 1 to clear.
1	R/W/C	RDMA0 pair (typically ADC) record interrupt status. Write a 1 to clear.
0	R/W/C	Multi-channel interleaved/PDMA0 pair playback interrupt status. Write a 1 to clear.

MT01: Sampling Rate Select Register:

Address Offset: 01h

Default Value: 00h.

This register applies to . When in slave mode, e.g. S/PDIF input, 256X master clock alone selects the sampling rate. See **Figure 4-3** and **Figure 4-4** on page 15 and page 16 respectively, in this chapter

Bit	Attribute	Description
7:5	R000b	-
4	R/W	S/PDIF input clock as the master. 0: disabled 1: enabled (Envy24HT slave mode) S/PDIF receiver chip or other source provides the master clock through SPMCLKIN (pin 111) Note that in this mode, 256X is the highest master clock available while the AC'97 MCLK requires 512X. AC'97 codecs, such as the VT1611A are designed based on BCLK which uses MCLK/2, i.e. 256X. When S/PDIF provides the master clock, if VIA AC'97 codecs are used, before setting S/PDIF as the master clock, proceed to switching the primary codec into slave mode (refer to the VT1611A datasheet). In this mode PBCLK will be output from Envy24HT.

Bit	Attribute	Description
3:0	R/W	Codec and S/PDIF sampling rate select. The entire system runs synchronously, based on the same master clock and sampling rate. All channels are set to the same rate. These bits are ignored if S/PDIF input is master. See bit 4 of this register. 0000: 48kHz (default) 0001: 24kHz 0010: 12kHz 0011: 9.6kHz 0100: 32kHz 0101: 16kHz 0110: 8kHz 0111: 96kHz 1110: 192kHz only for CCS04_6=1 (X1=49.152MHz) or MT02_3=1 (128X) & CCS04_6=0 1111: 64kHz 1000: 44.1kHz 1001: 22.05kHz 1010: 11.025kHz 1011: 88.2kHz 1100: 176.4kHz (forces to 128X mode only) others: reserved

MT02: I²S Data Format Register:

Address Offset: 02h

Default Value: 00h

Bit	Attribute	Description
7:4	R0	-
3	R/W	MCLK/LRCLK ratio, except for 176.4kHz where 128X is the only choice 0: 256x (default) 1: 128x
2	R/W	
1:0	R/W	Data format: 00: I²S (timing diagram provided below) others: Reserved

See **Figure 4-2** below for a timing diagram for bits [1:0]. See **Figure 4-3** and **Figure 4-4** on page 15 and page 16 respectively for the visual description of other bits.

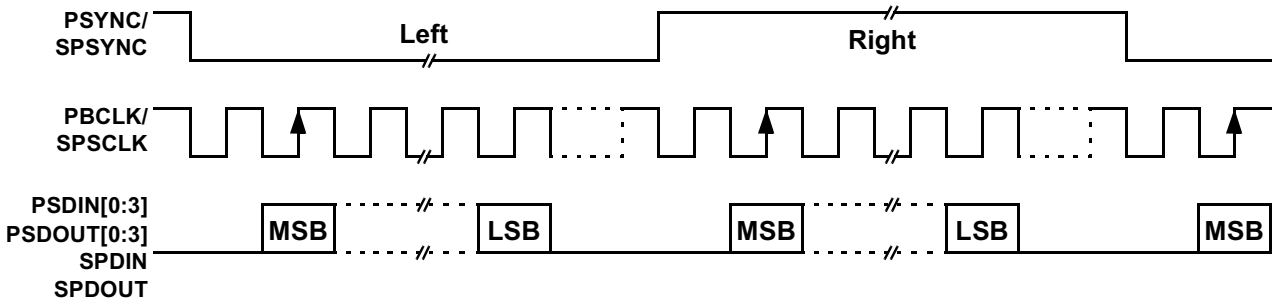

Figure 4-2. I²S Format Timing Diagram

MT03: DMA Interrupt Mask Register:

Address Offset: 03h

Default Value: FFh

This register relates to all DMA channels. By default all interrupts are off (‘1’), i.e. masked. When enabled (set to ‘0’), MT00 interrupt status reflects each DMA channels interrupt state.

Bit	Attribute	Description
7	R/W	SPDIF Out/PDMA4 pair playback interrupt mask. Always valid.
6	R/W	PDMA3 pair playback interrupt mask. Valid only when MT19>00b
5	R/W	PDMA2 pair playback interrupt mask. Valid only when MT19>01b
4	R/W	PDMA1 pair playback interrupt mask. Valid only when MT19=11b
3	R/W	DMA FIFO underrun/overrun condition interrupt mask. MT1A reports the offending channel.
2	R/W	RDMA1 (typically S/PDIF input) pair record interrupt mask. Always valid.
1	R/W	RDMA0 pair (typically ADC) record interrupt mask. Always valid.
0	R/W	Multi-channel interleaved/PDMA0 pair playback interrupt mask. Always valid.

MT04: Index Register for AC’97 Codecs

Address Offset: 04h

Default Value: 00h

This register is valid when AC-link interface (CCS05_7 = 0) is used. It has no validity when the converter interface is set to I²S mode (CCS05_7 = 1).

Bit	Attribute	Description
7	R0	-
6:0	R/W	AC’97 registers Index. Refer to the AC’97 specification for register descriptions.

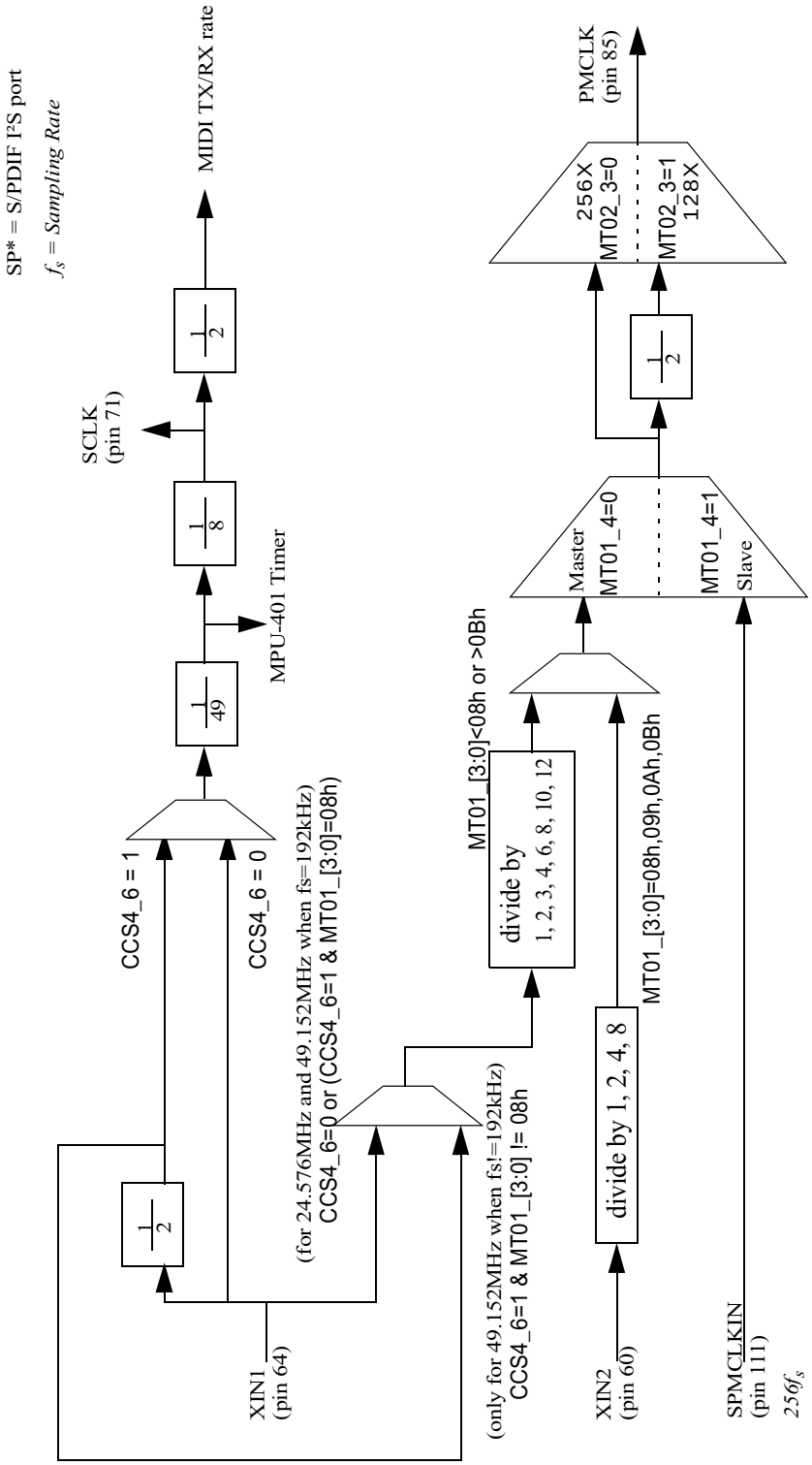

Figure 4-3. Crystals to Master Clocks clock generation tree

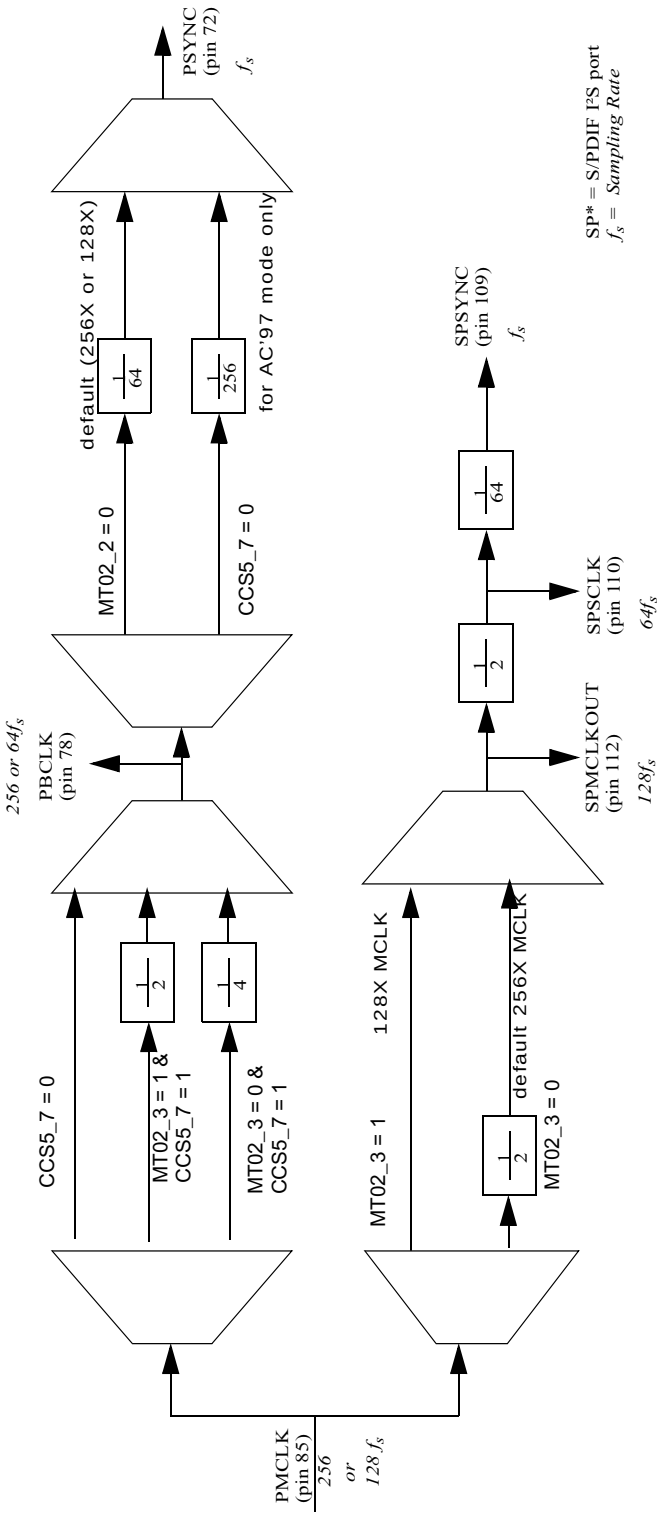

Figure 4-4. Master Clocks to Bit Clocks, L/R Clocks and Sync generation

MT05: Command and Status Register for AC'97 Codecs

Address Offset: 05h

Default Value: 00h

This register is valid when AC-link interface (CCS05_7 = 0) is used. It has no meaning when the converter interface is set to I²S mode (CCS05_7 = 1)..

Bit	Attribute	Description
7	R/W	Cold reset. Write 1 to assert PRST# (pin105) active. Write back 0 to remove reset condition from all professional section codecs.
6	R/W	Warm reset. Write 1 to have warm reset by asserting PSYNC (pin 72). This bit together with PRST# (pin 105) active (MT05_7=1) can be used to set the external VIA primary AC'97 codec to slave mode (such as the VT1611A). This must be done when S/PDIF input is the master. Apply Cold reset to restore codec master mode.
5	R/W	Write 1 to write to AC'97 codec register Reading a 1 indicates the write cycle is still in progress, cleared when write cycle complete.
4	R/W	Write 1 to read AC'97 CODEC register Reading a 1 indicates the read cycle is still in progress, cleared when there is valid data.
3	RO	AC'97 codec ready status bit. After power-on, check that this bit is 1 before accessing codec registers.
2	R0b	-
1:0	R/W	ID for external AC'97 registers read/write when split mode (CCS05_1 = 0) is used. When a 6-channel AC'97 like the VT1616 is used (CCS05_1 = 1), the multichannel PCM data is transmitted on the default slots but on the same data out pin, PSDOUT0, pin 79. 00: select primary AC'97 codec. PCM transmitted on time slots 3,4. 01: select second slave AC'97 codec.PCM transmitted on time slots 3,4. 10: select third slave AC'97 codec. PCM transmitted on time slots 7,8. 11: select fourth slave AC'97 codec. PCM transmitted on time slots 6,9.

MT06: Data Port Register for AC'97 codecs on Professional section

Address Offset: 06h - 07h

Default Value: 00h

This register is valid when AC-link interface (CCS05_7 = 0) is used. It has no meaning when the converter interface is set to I²S mode (CCS05_7 = 1).

Bit	Attribute	Description
15:8	R/W	AC'97 codec register data high byte (index 07h) Refer to the AC'97 specification for register descriptions..
7:0	R/W	AC'97 codec register data low byte (index 06h). Refer to the AC'97 specification for register descriptions.

4.2.2 Multi-Channel Interleaved DMA Playback Registers

The following **Figure 4-5** represents the manner the data is sequenced and interleaved for efficient transfer of multi-channel data over PCI bus. A total of 12 layers (or sample times t_0 through t_{11}) deep buffer structure is implemented for a seamless flow of each stream, i.e. a maximum of 12*8chs*24bit data can be buffered before the physical output pins. Each burst cycle fills 4 layers (or sample time t_x to t_{x+4}) for each channel. If empty time slots (or layers) remain, a new bus request is issued until all layers are full. An initial buffer fill therefore, generates 3 consecutive bus requests. 32-bit unpacked data transfers are used across the PCI bus regardless of the audio data resolution. All transfer data are left (MSB) justified. Each transfer request results into a PCI bus master burst cycle. The maximum and default burst size is 4*8chs.=32 PCI data cycles. The burst size can be reduced to 6, 4 or 2 channels (see MT19), i.e. shrink to 24, 16 or 8 PCI data cycles transferred. This improves PCI bus efficiency when only a limited amount of channels are used and frees up the DMA FIFO for independent stereo pair operation where each channel has independent control over the data flow.

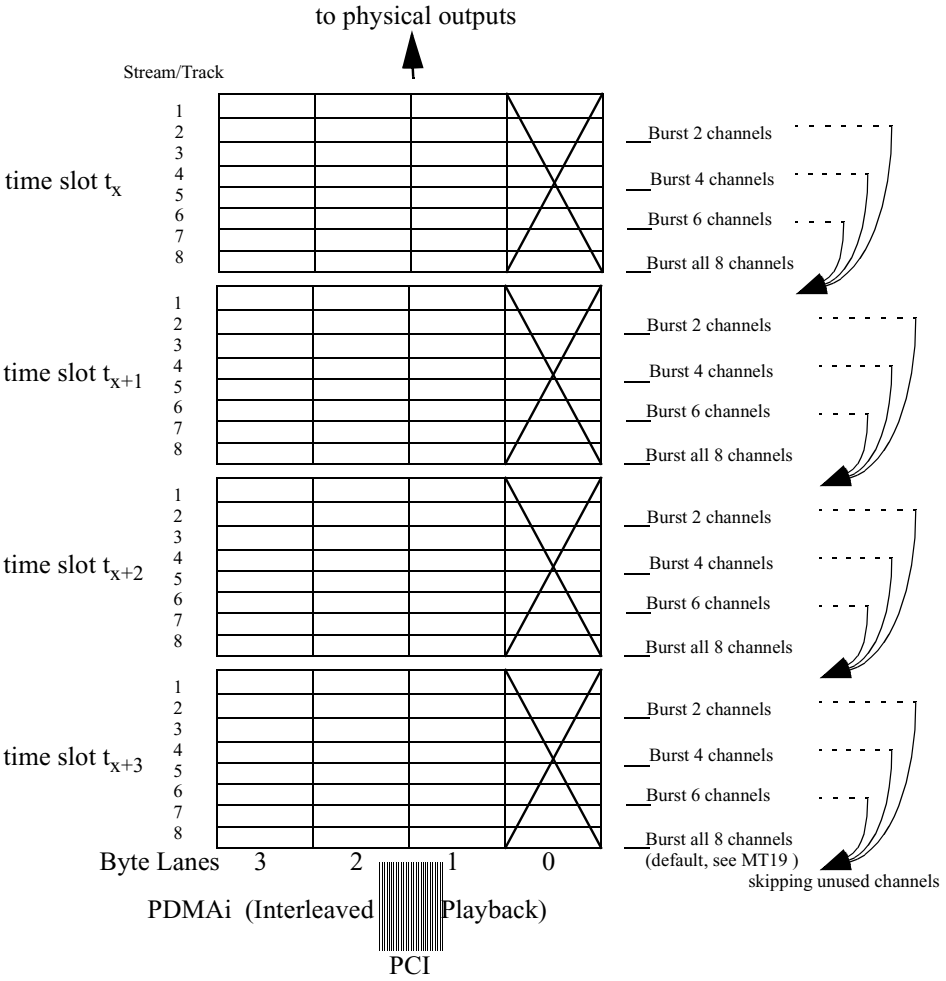

Figure 4-5. Multi-channel Interleaved DMA Playback diagram

The usage of I²S converters (see CCS05_7) or AC-link (split and or packed mode, see CCS05_1) determines which DMA slots map into which physical pin. The table below shows the DMA FIFO mapping into I²S or AC-link time slots. Refer to **Figure 4-5** above for DMA stream/track information or **Figure 4-7** on page 29 of this chapter. The ID in AC'97 mode is the value read at the standard location 28h, along with the AMAP bit. The mapping of proper DMA FIFO track into corresponfing time slots is done to eliminate the need for manipulation of streaming data by the software drivers per Microsoft WAVEFORMATEXTENSIBLE format and the definition of predetermined multichannel speaker location.

DMA FIFO track	I²S mode (CCS05_7=1)	split AC-link mode (CCS05_1=0)	packed AC-link (CCS05_1=1)
PDMAi 1,2 or PDMA0	PSDOUT0 L/R	PSDOUT0 3,4, IDx 00 (primary)	PSDOUT0 3,4 (Front L/R)
PDMAi 3,4 or PDMA1	PSDOUT1 L/R	PSDOUT1 6,9 IDx 11 (secondary 3)	PSDOUT0 6,9 (Center/LFE)
PDMAi 5,6 or PDMA2	PSDOUT2 L/R	PSDOUT2 7,8 IDx 10 (secondary 2)	PSDOUT0 7,8 (Surr. L/R)
PDMAi 7,8 or PDMA3	PSDOUT3 L/R	PSDOUT3 3,4, IDx 01 (secondary 1)	PSDOUT0 10,11(AC'97 S/PDIF)

Table 4-3. DMA to I²S/AC-link time slots mapping

For more information on the AC-link time slots definition, codec IDing, AMAP and similar topics, please, refer to the industry standard AC'97 specification Rev 2.2 and can be found at

http://developer.intel.com/ial/scalableplatforms/audio/index.htm

MT10: Interleaved Playback DMA Current/Base Address Register

Index: 10h - 13h

Default Value: 00000000h. PDMAi interleaves 8 outbound data slots, each with 32-bit from the system memory to physical outputs.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT14: Interleaved Playback DMA Current/Base Count Register

Index: 14h - 16h

Default Value: 0000h

Bit	Attribute	Description
18:0	R/W	Write the Interleaved Playback DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT18: Global Playback and Record DMA Start/Stop Register

Index: 18h

Default Value: 00h.

Software should always resort to RMW (read modifiy write) to guarantee unintended interference with other channels that may be simultaneously active.

Bit	Attribute	Description
7	R/W	1: SPDIFout/PDMA4 start; 0: SPDIFout/PDMA4 stop
6	R/W	1: PDMA3 start; 0: PDMA3 stop. Valid only when MT19>00b
5	R/W	1: PDMA2 start; 0: PDMA2 stop. Valid only when MT19>01b
4	R/W	1: PDMA1 start; 0: PDMA1 stop. Valid only when MT19=11b
3	R0	-
2	R/W	1: RDMA1 start; 0: RDMA1 stop
1	R/W	1: RDMA0 start; 0: RDMA0 stop
0	R/W	1: PDMAi/PDMA0 start; 0: PDMAi/PDMA0 stop

MT19: Interleaved Playback DMA Active Streams/PCI Burst Size Register

Index: 19h

Default Value: 00h.

Bit	Attribute	Description
7:2	R0	Reserved
1:0	R/W	00 (default): Burst all 8chs.*4=32 data slots interleaved on PDMAi 01: Burst first 6chs.*4=24 data slots on PDMAi. PDMA3 is available independently. 10: Burst first 4chs*4=16. data slots on PDMAi. PDMA3 and PDMA2 are available independently. 11: Burst only first stereo pair, i.e. PDMA0 as 8 data slots. This is the mode for having 4 independent pairs, each with its own request/grant mechanism.

MT1A: Global Playback and Record DMA FIFO Underrun/Overrun Register

Index: 1Ah

Default Value: 00h.

This register alerts software of a DMA underrun/overrun condition by raising a "1" flag. Any flag triggers an interrupt. The status can be checked by reading

Bit	Attribute	Description
7	R/W/C	1: SPDIFout/PDMA4 underrun; 0: SPDIFout/PDMA4 normal. Write a 1 to clear.
6	R/W/C	1: PDMA3 underrun; 0: PDMA3 normal. Valid only when MT19>00b. Write a 1 to clear.
5	R/W/C	1: PDMA2 underrun; 0: PDMA2 normal. Valid only when MT19>01b. Write a 1 to clear.
4	R/W/C	1: PDMA1 underrun; 0: PDMA1 normal. Valid only when MT19=11b. Write a 1 to clear.
3	R0	-
2	R/W/C	1: RDMA1 overrun; 0: RDMA1 normal. Write a 1 to clear.
1	R/W/C	1: RDMA0 overrun; 0: RDMA0 normal. Write a 1 to clear.
0	R/W/C	1: PDMAi/PDMA0 underrun; 0: PDMAi/PDMA0 normal. Write a 1 to clear.

MT1B: Global Playback and Record DMA Pause/Resume Register

Index: 1Bh

Default Value: 00h.

Software should always resort to RMW (read modifiy write) to guarantee unintended interference with other channels that may be simultaneously active.

Bit	Attribute	Description
7	R/W	1: SPDIFout/PDMA4 pause; 0: SPDIFout/PDMA4 resume
6	R/W	1: PDMA3 pause; 0: PDMA3 resume. Valid only when MT19>00b
5	R/W	1: PDMA2 pause; 0: PDMA2 resume. Valid only when MT19>01b
4	R/W	1: PDMA1 pause; 0: PDMA1 resume. Valid only when MT19=11b
3	R0	-
2	R/W	1: RDMA1 pause; 0: RDMA1 resume
1	R/W	1: RDMA0 pause; 0: RDMA0 resume
0	R/W	1: PDMAi/PDMA0 pause; 0: PDMAi/PDMA0 resume

MT1C: Interleaved Playback DMACurrent/Base Terminal Count Register

Index: 1C - 1Dh

Default Value: 0000h

Bit	Attribute	Description
18:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

4.2.3 Record DMA Stereo Pairs Registers

MT20: Record DMA 0 Current/Base Address Register

Index: 20h - 23h

Default Value: 00000000h. RDMA0 interleaves 2 slots, each with 32-bit data to the system memory.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT24: Record DMA 0 Current/Base Count Register

Index: 24 - 25h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the Record DMA 0 initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Record DMA pointer after having allowed at least 2 sample frames.

MT26: Record DMA 0 Current/Base Terminal Count Register

Index: 26h - 27h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

MT30: Record DMA 1 Current/Base Address Register

Index: 30h - 33h

Default Value: 00000000h. RDMA1 stereo, each with 32-bit to the system memory from physical inputs of PSDOUT1 in I²S form. Typically S/PDIF in but nothing precludes it from being an ADC data.

Bit	Attribute	Description
31:2	R/W	Write the stereo pair 1 Record DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT34: Record DMA 1 Current/Base Count Register

Index: 34h - 35h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 1 Record DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT36: Record DMA1 Current/Base Terminal Count Register

Index: 36 - 37h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

4.2.4 Digital Loopback

The Envy24HT provides an extensive routing capability of the data streams, avoiding host loading if data transfer across the bus is not requested by the user. The routing is possible only in the I²S mode, i.e. CCS05_7=1. Since the xDMAx may not be mapped into AC-link time slots consecutively, the digital loopback is not available when CCS05_7=0. The following registers control the routing from numerous sources to various destination. Insertion of the stream routing functionality adds a maximum of a single sample cycle delay with respect to the original data. The switch matrix being so complex, careful register setting is crucial to avoid undesirable effects. For simplicity of the register description only pin names are used. Refer to the pin list for pin numbers and location.
The diagram below is a visual representation of possible connection. If a dot is missing on an intersection, it reflects the lack of routing capabitlity. The output DMA can only be routed to its intended physical output. However, any input can be looped back to any of the output. This is useful for digitizing an analog source and outputting on S/PDIF Out or the reverse, taking an S/PDIF input PCM stream and converting it to analog directly on the fly, swapping Left/Right channels, routing signals to different output pairs, .

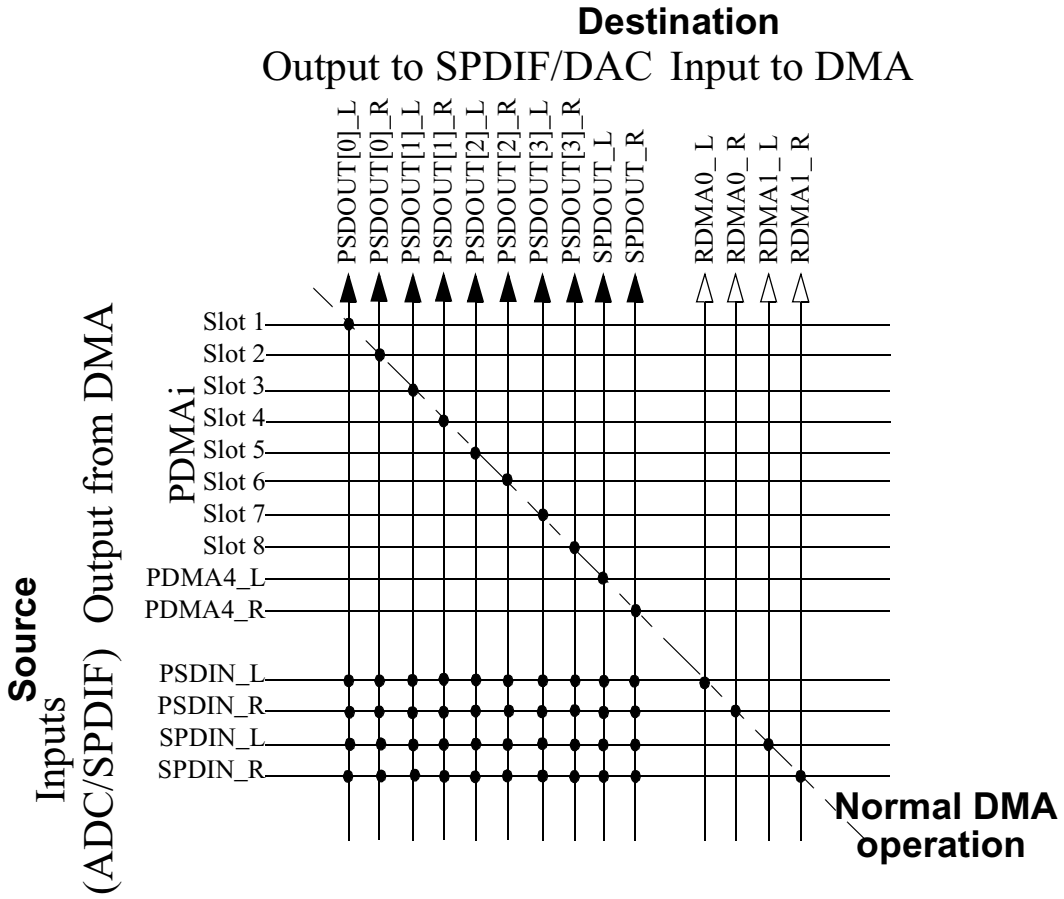

Figure 4-6. Data stream routing capabilities

MT2C: Routing Control Register for Data to PSDOUT[0:3] and SPDOUT

Default Value: 00h

Bit	Attribute	Description
31:29	R/W	PSDOUT[3] Right source 000: from PDMAi slot 8 or PDMA3 Right 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
28:26	R/W	PSDOUT[2] Right source 000: from PDMAi slot 6 or PDMA2 Right 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
25:23	R/W	PSDOUT[1] Right source 000: from PDMAi slot 4 or PDMA1 Right 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
22:20	R/W	PSDOUT[0] Right source 000: from PDMAi slot 2. 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
19:17	R/W	PSDOUT[3] Left source 000: from PDMAi slot 7 or PDMA3 Left 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
16:14	R/W	PSDOUT[2] Left source 000: from PDMAi slot 5 or PDMA2 Left 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved

Bit	Attribute	Description
13:11	R/W	PSDOUT[1] Left source 000: from PDMAi slot 3 or PDMA1 Left 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
10:8	R/W	PSDOUT[0] Left source 000: from PDMAi slot 1 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
7:6	R/W	Reserved
5:3	R/W	SPDOUT Right source 000: from PDMA4 Right (2nd) slot 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
2:0	R/W	SPDOUT Left source 000: from PDMA4 Left (1st) slot 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved

4.2.5 Integrated S/PDIF Transmitter Register

MT3C: S/PDIF IEC958 Transmitter Control Register

Address Offset: 3Ch - 3Dh

Default Value: x000h

Description: This read/write register controls the S/PDIF functionality when bit CCS07_0 reports that S/PDIF is implemented. It will return 0000h when SPDTX, pin 92 left floating or pulled high. If S/PDIF is implemented for the final product, it will read 2000h at power-up. The register manages the bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written when the S/PDIF transmitter is disabled (S/PDIF Enable/Disable bit CCS07_7 = 0). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

Bit	Attribute	Description
15	R/W	Validity: This bit affects the “Validity flag”, bit 28 transmitted in each subframe and enables the S/PDIF transmitter to maintain connection during error or mute conditions. 1: Tags both samples as invalid by setting bit 28, “Validity flag” to “1” 0: If a valid Left/Right pair was transmitted through S/PDIF, the Validity bit should be reset.
14 : 12	R/W	These bits declare the S/PDIF transmitter clock rate (64*fs) in the Channel Status Byte 3, low nibble if Consumer mode (MT3C_0 = 0) and Byte 0 (bits 7-6) and Byte 4 (bits 6-3) if Professional mode (MT3C_0 = 1). It will be set automatically by MT01 low nibble if master. In slave mode (MT01_4 = 1), to display the correct sampling rate, it must be written to reflect the external clock recovered. 000: 44.1kHz 001: Reserved 010: 48kHz (default) 011: 32kHz 100: 88.2kHz 101: 96kHz 110: 192kHz 111: 176.4kHz
11	RW	Generation Level: Programmed according to IEC standards.
10:4	RW	Category Code. Programmed according to IEC standards.
3	R/Wh	Preemphasis. “1” : Indicates filter preemphasis is 50/15µs. “0” : Default is no Preemphasis.
2	R/W	Copyright “1” : Indicates copyright is not asserted. “0” : Copyright is asserted (default).
1	R/W	/PCM: Non-Audio Samples “1” : Set this bit for transmitting non-PCM audio samples such as AC-3. “0” : Indicates samples are linear PCM suitable for direct conversion to audio playback.
0	R/W	Professional “1” : Set Professional mode. Set this bit in conjunction with /PCM bit (above) for AC-3. “0” : Indicates Consumer mode (default).

4.2.6 VU Peak Meter Registers

MT3E: Peak Meter Index Register

Address Offset: 3Eh

Default Value: 00h

Bits	Attribute	Description
7:5	R000b	-
4:0	R/W	Peak meter stream index 00000: Playback stream 1 (PDMAi slot 1) 00001: Playback stream 2 (PDMAi slot 2) 00010: Playback stream 3 (PDMAi slot 3) 00011: Playback stream 4 (PDMAi slot 4) 00100: Playback stream 5 (PDMAi slot 5) 00101: Playback stream 6 (PDMAi slot 6) 00110: Playback stream 7 (PDMAi slot 7) 00111: Playback stream 8 (PDMAi slot 8) 01000: S/PDIF Left stream (PDMA4 slot 1) 01001: S/PDIF Right stream (PDMA4 slot 2) 01010: Record0 Left stream (RDMA0 slot 1) 01011: Record0 Right stream (RDMA0 slot 2) 01100: ignored. 01101: ignored. 01110: ignored. 01111: ignored. 10000: ignored. 10001: ignored. 10010: Record1 Left stream (RDMA1 slot 1, typ. S/PDIF Right input stream) 10011: Record1 Right stream (RDMA1 slot 2, typ. S/PDIF Right input stream) 10100: ignored. 10101: ignored. others: ignored.

MT3F: Peak Meter Data Register

Address Offset: 3Fh

Default Value: 00h

Bits	Attribute	Description
7:0	R	Peak data derived from the absolute value of 9 msb. 00h min - FFh max volume. Reading the register resets the meter to 00h.

4.2.7 Concurrent Stereo Pairs Playback DMA Registers

The following figure is a visual representation of the stereo pairs data transfer mechanism. This is an alternative to the default interleaved DMA method. In this mode the data is not packed tightly for time correlation. It allows independent stereo pair operation. A 12 layers deep buffer structure is implemented for a seamless flow of each stream. If the PDMAi burst size is left at 8, no stereo pair DMA is available except for SPDIFout/PDMA4 and Record DMAs which are always independently controllable. As the burst size of PDMAi is decreased by writing to MT19, independently controllable playback stereo pair DMAs become available. 32-bit data transfers are used regardless of the audio data resolution. All transfer data are left (MSB) justified. Each transfer request results into a PCI bus master burst cycle. The burst size is always 8 PCI data cycles long, i.e. Left and Right for 4 consecutive sampling times. All stereo DMA pairs behave similarly.

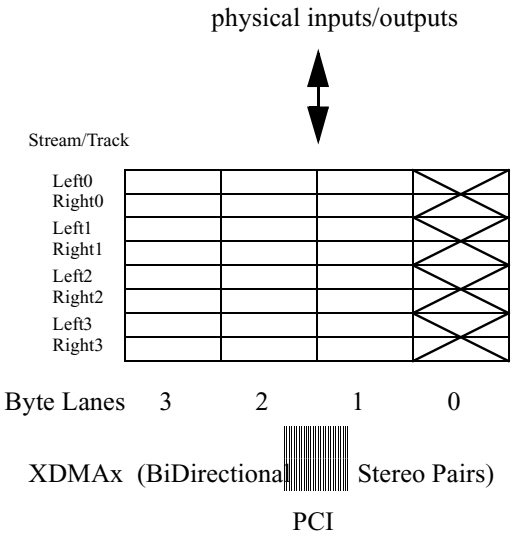

Figure 4-7. Stereo Pairs DMA Playback diagram

MT40: SPDIFout/PDMA4 Playback DMA Current/Base Address Register

Index: 40h - 43h

Default Value: 00000000h. SPDIFout/PDMA4 stereo, each with 32-bit from the system memory to physical outputs of IEC958 line driver and a copy toPSDOUT4 in I²S form.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT44: SPDIFout/PDMA4 Playback DMA Current/Base Count Register

Index: 44h - 45h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 4/SPDIF out DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT46: SPDIFout/PDMA4 Playback DMACurrent/Base Terminal Count Register

Index: 46 - 47h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

MT50: PDMA3 Playback DMA Current/Base Address Register

Index: 50h - 53h

Default Value: 00000000h. PDMA3 stereo, each with 32-bit from the system memory to physical outputs of PSDOUT3 in I²S form.

Bit	Attribute	Description
31:2	R/W	Write the stereo pair 3 Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT54: PDMA3 Playback DMA Current/Base Count Register

Index: 54h - 55h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 3 Playback DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT56: PDMA3 Playback DMACurrent/Base Terminal Count Register

Index: 56 - 57h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

MT60: PDMA2 Playback DMA Current/Base Address Register

Index: 60h - 63h

Default Value: 00000000h. PDMA2 stereo, each with 32-bit from the system memory to physical outputs of PSDOUT2 in I²S form.

Bit	Attribute	Description
31:2	R/W	Write the stereo pair 2 Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT64: PDMA2 Playback DMA Current/Base Count Register

Index: 64h - 65h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 2 Playback DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT66: PDMA2 Playback DMACurrent/Base Terminal Count Register

Index: 66 - 67h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

MT70: PDMA1 Playback DMA Current/Base Address Register

Index: 70h - 73h

Default Value: 00000000h. PDMA1 stereo, each with 32-bit from the system memory to physical outputs of PSDOUT1 in I²S form.

Bit	Attribute	Description
31:2	R/W	Write the stereo pair 1 Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT74: PDMA1 Playback DMA Current/Base Count Register

Index: 74h - 75h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 1 Playback DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT76: PDMA1 Playback DMACurrent/Base Terminal Count Register

Index: 76 - 77h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

Section 5: Electrical Characteristics

5.1 Maximum Ratings

Table 5-1. Maximum Ratings

Parameter	Min	Typ	Max	Unit
Storage Temperature	-55		150	°C
Operating Ambient Temperature	0	25	70	°C
DC Supply Voltage (Analog and Digital)	3.0	3.3	4.0	V
I/O Pin Voltage	GND - 0.5		VDD	V
Power Dissipation			TBD	W

5.2 Electrical Specifications

Table 5-2. DC Characteristics

(T_A=25°C, VDD = 3.3V ± 5%; GND = 0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	-0.3		V_{DD}+0.3	V
V_{IL}	Input Low Voltage			0.3 x V_{DD}	V
V_{IH}	Input High Voltage	0.7 x V_{DD}			V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
–	Input Leakage Current	-10		10	µA
–	Output Leakage Current	-10		10	µA
–	Output Buffer Drive Current		TBD		mA

Table 5-3. Power Consumption

(T_A=25°C, VDD = 3.3V ± 5%; GND = 0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
I_{VDD}	Supply Current: Power Up		TBD		mA
I_{VDD}	Supply Current: Partial Power Up		TBD		mA
I_{VDD}	Supply Current: Partial Power Down		TBD		mA
I_{VDD}	Supply Current: Power Down		TBD		mA

5.3 AC Timing Characteristics

(Test Conditions: T_A=25°C, VDD = 3.3V ± 5%; GND = 0V; 50pF Load)

Table 5-4. Cold Reset

Symbol	Parameter	Min	Typ	Max	Unit
T_{RST_LOW}	CRST#/PRST# Active Low Pulse Width	1			µs
$T_{RST2CLK}$	CRST#/PRST# Inactive to CBLK/PBCLK/SPSCLK Startup Delay	162.8			ns

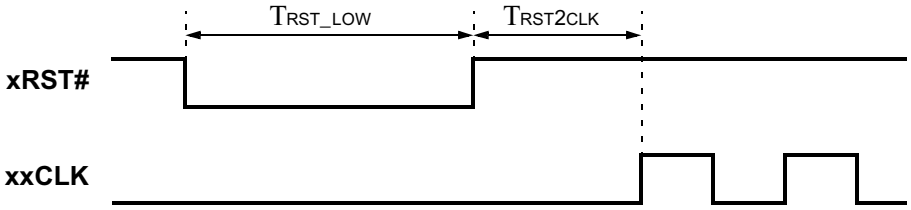

Figure 5-1. Cold Reset Timing

Table 5-5. Warm Reset

Symbol	Parameter	Min	Typ	Max	Unit
TSYNC_HIGH	CSYNC/PSYNC Active High Pulse Width		1.3		µs
TSYNC2CLK	CSYNC/PSYNC Inactive to CBLK/PBCLK Startup Delay	162.8			ns

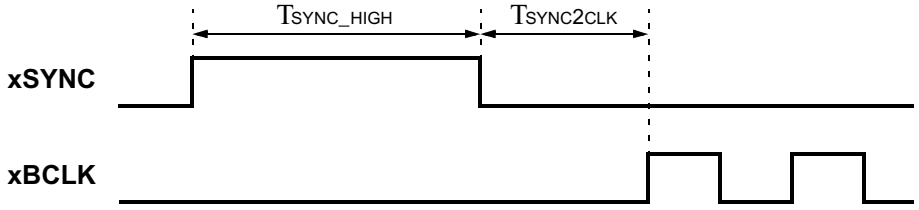

Figure 5-2. Warm Reset Timing

Table 5-6. Slave Mode Master clock delay

Symbol	Parameter	Min	Typ	Max	Unit
TSPI2MCK	SPMCLKIN to PMCLK Delay		4		ns
TSPI2SPO	SPMCLKIN to SPMCLKOUT Delay		5.5		ns

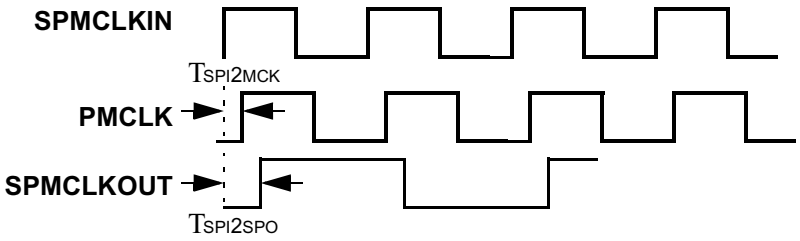

Figure 5-3. Master Clock Delay

Table 5-7. xBCLK / xxSYNC Timing

Symbol	Parameter	Min	Typ	Max	Unit
	xBCLK Frequency		see Appendix		MHz
TCLK_PERIOD	xBCLK Period		see Appendix		ns
	xBCLK Output Jitter		TBD	750	ps
TCLK_HIGH	xBCLK Pulse Width (high)		see Appendix		ns
TCLK_LOW	xBCLK Pulse Width (low)		see Appendix		ns
TCLK_DC	xBCLK Duty Cycle		see Appendix		%
	xxSYNC Frequency		see Appendix		kHz
TSYNC_PERIOD	xxSYNC Period		see Appendix		µs
TSYNC_HIGH	xxSYNC Pulse Width (high)		see Appendix		µs
TSYNC_LOW	xxSYNC Pulse Width (low)		see Appendix		µs

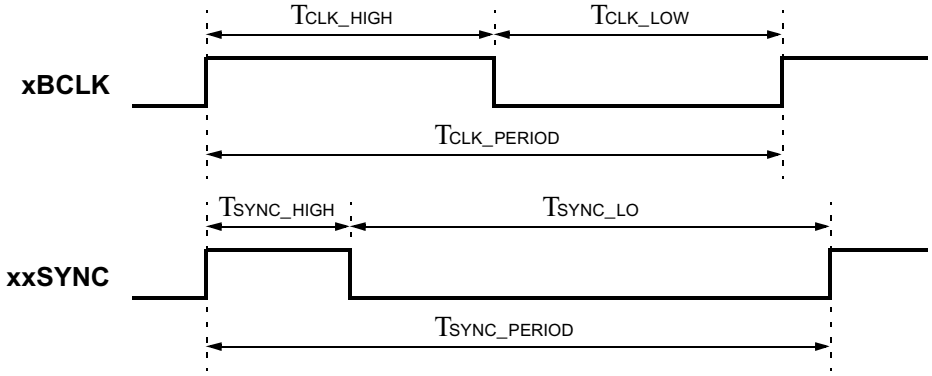

Figure 5-4. xBCLK to xxSYNC Timing

Table 5-8. Setup and Hold

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP1	xSDOUT Setup to falling edge of xBCLK	15			ns
THOLD1	xSDOUT Hold from falling edge of xBCLK	5			ns
TSETUP2	xSYNC Setup to rising edge of xBCLK	15			ns
THOLD2	xSYNC Hold to rising edge of xBCLK	5			ns

Note: SDATA_IN seup and hold calculations determined by AC'97 controller propagation delay.

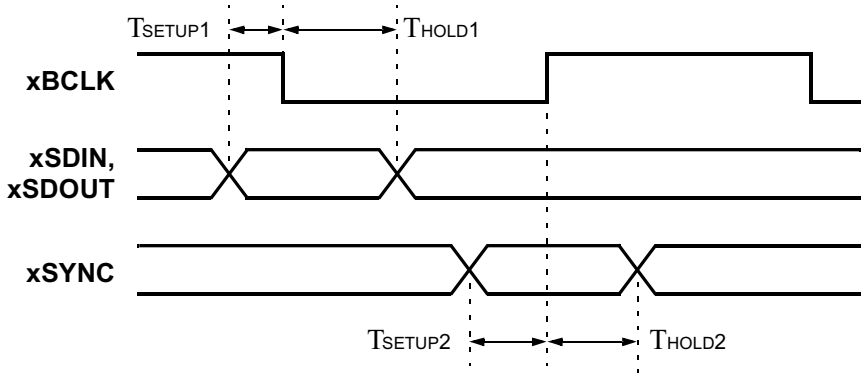

Figure 5-5. Setup and Hold Time

Table 5-9. Rise and Fall Time

Symbol	Parameter	Min	Typ	Max	Unit
TRISE	xBCLK rise time	2		6	ns
TFALL	xBCLK fall time	2		6	ns
TRISE	xxSYNC rise time	2		6	ns
TFALL	xxSYNC fall time	2		6	ns
TRISE	xSDIN rise time	2		6	ns
TFALL	xSDIN fall time	2		6	ns
TRISE	xSDOUT rise time	2		6	ns
TFALL	xSDOUT fall time	2		6	ns

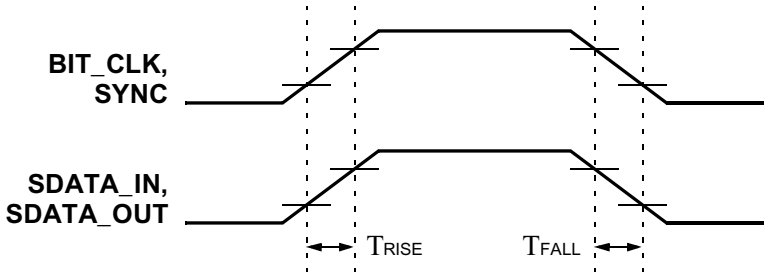

Figure 5-6. Rise Time and Fall Time

Table 5-10. AC-link Low Power Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{S2_PDOWN}	End of Slot 2 to CBCLK/PBCLK to CSDIN/PSDIN low			1	µs

Note: CBCLK/PBCLK not to scale.

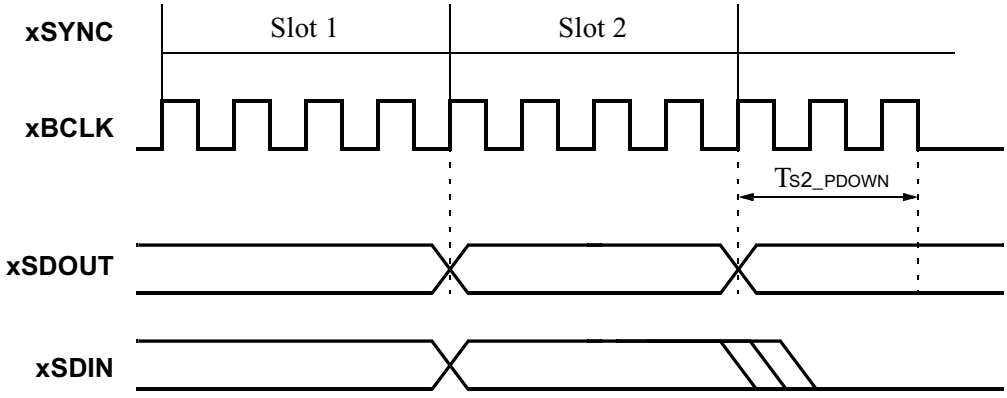

Figure 5-7. AC-link Power Mode Timing.

Section 6: Mechanical Data

6.1 Thermal Specifications

Parameter	Min	Typ	Max	Unit
Thermal Resistenace θ_{JA} (Still Air)		TBD		°C/W
Junction Temperature		TBD		°C

6.2 Package Dimensions

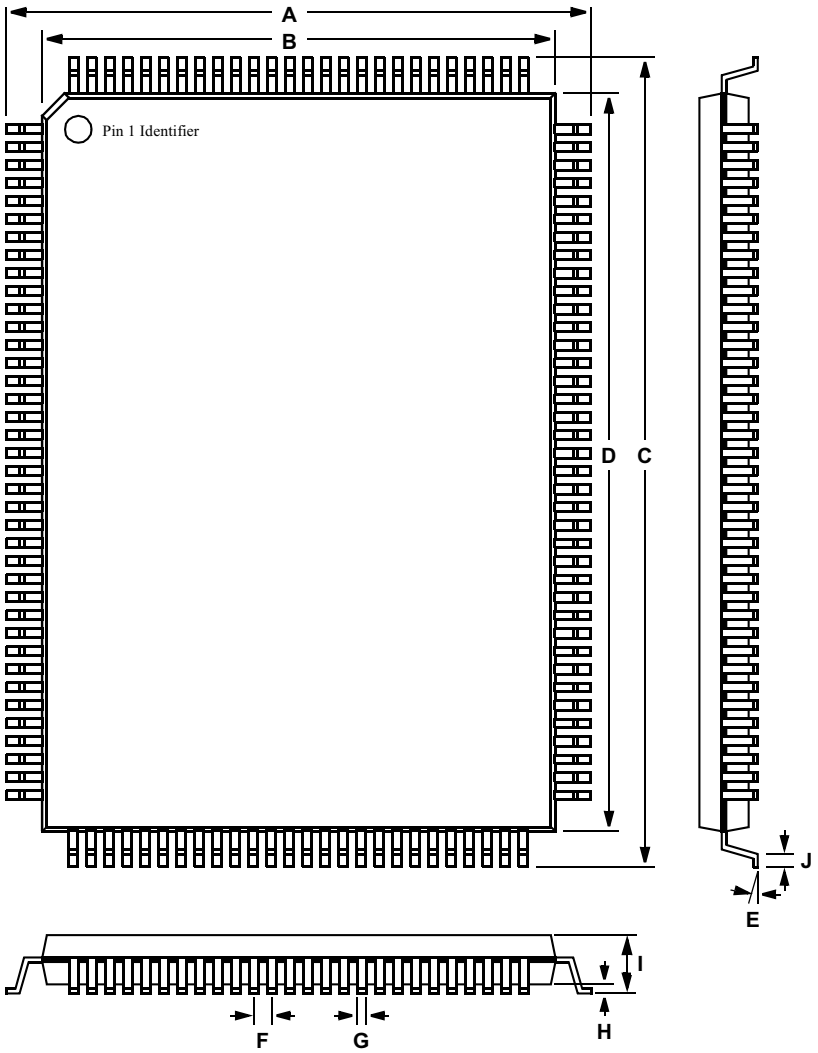

Table 6-1. Mechanical Dimensions (millimeters, unless otherwise stated)

Symbol	A	B	C	D	E	F	G	H	I	J
minimum	17.0	13.9	23.0	19.9	0°	0.5	0.17	0.25	–	0.65
maximum	17.4	14.1	23.4	20.1	7°		0.23	-	3.4	0.95