

MB85341A-60/-70/-80

CMOS 1M x 32 Fast Page Mode DRAM Module

CMOS 1,048,576 x 32 Bit Fast Page Mode DRAM Module

The Fujitsu MB85341A is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB814400A devices. The MB85341A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85341A are the same as the MB814400A which features fast page mode operation. For ease of memory expansion, the MB85341A is offered in a 72-pad Single In-line Memory Module package (SIMM).

PRODUCT LINE & FEATURES

| Parameter | MB85341A-60 | MB85341A-70 | MB85341A-80 |
|---------------------------|--|-------------|-------------|
| RAS Access Time | 60ns max. | 70ns max. | 80ns max. |
| Random Cycle Time | 110ns min. | 125ns min. | 140ns min. |
| Address Access Time | 30ns max. | 35ns max. | 40ns max. |
| CAS Access Time | 15ns max. | 20ns max. | 20ns max. |
| Fast Page Mode Cycle Time | 40ns min. | 45ns min. | 45ns min. |
| Power Dissipation | 4840mW max. | 4400mW max. | 3960mW max. |
| • Operating mode | 88mW max. (TTL level) / 44mW max. (CMOS level) | | |
| • Standby mode | | | |

- Organization : 1,048,576 words x 32 bits
- Memory : MB814400A, 8 pcs
- Decoupling Capacitor : 0.22 μ F, 8 pcs
- Package and Ordering Information: 72-pad SIMM, order as MB85341A-xxPJPBK (PJPBK = Gold Pad) MB85341A-xxPJPB (PJPB = Solder Pad)

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

| Parameter | Symbol | Value | Unit |
|------------------------------|--------|--------------|------|
| Supply Voltage | VCC | -1.0 to +7.0 | V |
| Input Voltage | VIN | -1.0 to +7.0 | V |
| Output Voltage | VOUT | -1.0 to +7.0 | V |
| Short Circuit Output Current | IOUT | 50 | mA |
| Power Dissipation | PD | 8.0 | W |
| Storage Temperature | TSTG | -55 to +125 | °C |

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

See page 6

MSS-72P-P29

See page 7

MSS-72P-P48

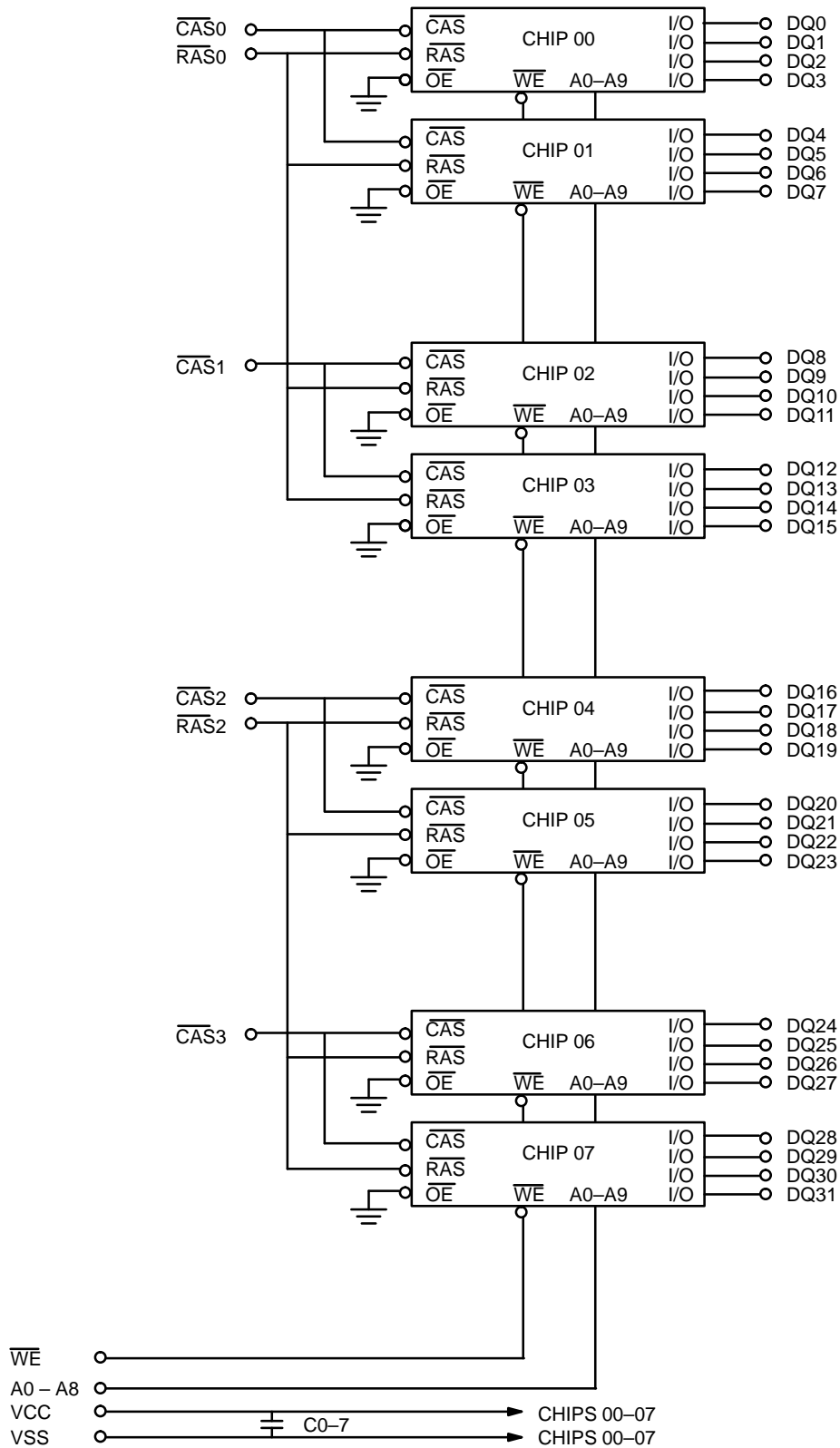
| | | | |
|------|----|----|------|
| DQ0 | 2 | 1 | VSS |
| DQ1 | 4 | 3 | DQ16 |
| DQ2 | 6 | 5 | DQ17 |
| DQ3 | 8 | 7 | DQ18 |
| VCC | 10 | 9 | DQ19 |
| A0 | 12 | 11 | NC |
| A2 | 14 | 13 | A1 |
| A4 | 16 | 15 | A3 |
| A6 | 18 | 17 | A5 |
| DQ4 | 20 | 19 | NC |
| DQ5 | 22 | 21 | DQ20 |
| DQ6 | 24 | 23 | DQ21 |
| DQ7 | 26 | 25 | DQ22 |
| A7 | 28 | 27 | DQ23 |
| VCC | 30 | 29 | NC |
| A9 | 32 | 31 | A8 |
| RAS2 | 34 | 33 | NC |
| NC | 36 | 35 | NC |
| NC | 38 | 37 | NC |
| CAS0 | 40 | 39 | VSS |
| CAS3 | 42 | 41 | CAS2 |
| RAS0 | 44 | 43 | CAS1 |
| NC | 46 | 45 | NC |
| NC | 48 | 47 | WE |
| DQ24 | 50 | 49 | DQ8 |
| DQ25 | 52 | 51 | DQ9 |
| DQ26 | 54 | 53 | DQ10 |
| DQ27 | 56 | 55 | DQ11 |
| DQ28 | 58 | 57 | DQ12 |
| DQ29 | 60 | 59 | VCC |
| DQ30 | 62 | 61 | DQ13 |
| DQ31 | 64 | 63 | DQ14 |
| NC | 66 | 65 | DQ15 |
| PD2 | 68 | 67 | PD1 |
| PD4 | 70 | 69 | PD3 |
| VSS | 72 | 71 | NC |

| Pin # | Symbol | -60 | -70 | -80 |
|-------|--------|-----|-----|-----|
| 67 | PD1 | Vss | Vss | Vss |
| 68 | PD2 | Vss | Vss | Vss |
| 69 | PD3 | NC | Vss | NC |
| 70 | PD4 | NC | NC | Vss |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85341A-60
MB85341A-70
MB85341A-80

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Value | | | Unit | Ambient Operating Temp. |
|--------------------------------|-------|--------|-------|-----|-----|------|-------------------------|
| | | | Min | Typ | Max | | |
| Supply Voltage | 1 | VCC | 4.5 | 5.0 | 5.5 | V | 0 °C to 70 °C |
| | | VSS | 0 | 0 | 0 | | |
| Input High Voltage, all inputs | 1 | VIH | 2.4 | — | 6.5 | V | |
| Input Low Voltage, all inputs | 1 | VIL | −2.0 | — | 0.8 | V | |
| Input Low Voltage, DQ(*) | 1 | VILD | −1.0 | — | 0.8 | V | |

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

| Parameter | Notes | Symbol | Conditions | Values | | | Unit |
|---|-------------|--------|---|--------|-----|-----|------|
| | | | | Min | Typ | Max | |
| Output High Voltage | 1 | VOH | IOH = −5mA | 2.4 | — | — | V |
| Output Low Voltage | 1 | VOL | IOL = 4.2mA | — | — | 0.4 | V |
| Input Leakage Current | RAS | II(L) | 0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V; all other pins not under test = 0V | −30 | — | 30 | μA |
| | CAS | | | −20 | — | 20 | |
| | ADD, WE | | | −60 | — | 60 | |
| Output Leakage Current | | IO(L) | 0V ≤ VOUT ≤ 5.5V; Data out disabled | −10 | — | 10 | μA |
| Operating Current (Average power supply current) 2 | MB85341A-60 | ICC1 | RAS & CAS cycling; tRC = min. | — | — | 880 | mA |
| | MB85341A-70 | | | | | 800 | |
| | MB85341A-80 | | | | | 720 | |
| Standby Current (Power supply current) | TTL Level | ICC2 | RAS = CAS = VIH | — | — | 16 | mA |
| | CMOS Level | | RAS = CAS ≥ VCC−0.2V | | | 8 | |
| Refresh Current #1 (Average power supply current) 2 | MB85341A-60 | ICC3 | CAS = VIH; RAS = cycling; tRC = min. | — | — | 880 | mA |
| | MB85341A-70 | | | | | 800 | |
| | MB85341A-80 | | | | | 720 | |
| Fast Page Mode Current 2 | MB85341A-60 | ICC4 | RAS = VIL; CAS = cycling; tPC = min. | — | — | 440 | mA |
| | MB85341A-70 | | | | | 400 | |
| | MB85341A-80 | | | | | 360 | |
| Refresh Current #2 (Average power supply current) 2 | MB85341A-60 | ICC5 | RAS = cycling; CAS—before—RAS tRC = min. | — | — | 720 | mA |
| | MB85341A-70 | | | | | 640 | |
| | MB85341A-80 | | | | | 560 | |

CAPACITANCE (TA = 25°C, f = 1MHz)

| Parameter | Symbol | Typ | Max | Unit |
|----------------------------------|--------|-----|-----|------|
| Input Capacitance, A0 to A8 | CIN1 | — | 70 | pF |
| Input Capacitance, RAS0 and RAS2 | CIN2 | — | 36 | pF |
| Input Capacitance, CAS0 to CAS3 | CIN3 | — | 25 | pF |
| Input Capacitance, WE | CIN4 | — | 59 | pF |
| I/O Capacitance, (DQ0-31) | CDQ | — | 11 | pF |

MB85341A-60

MB85341A-70

MB85341A-80

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

| No. | Parameter | Notes | Symbol | MB85341A-60 | | MB85341A-70 | | MB85341A-80 | | Unit |
|-----|--|-------|-----------|-------------|--------|-------------|--------|-------------|--------|------|
| | | | | Min | Max | Min | Max | Min | Max | |
| 1 | Time Between Refresh | | t_{REF} | — | 16.4 | — | 16.4 | — | 16.4 | ms |
| 2 | Random Read/Write Cycle Time | | t_{RC} | 110 | — | 125 | — | 140 | — | ns |
| 3 | Access Time from \overline{RAS} | 6,9 | t_{RAC} | — | 60 | — | 70 | — | 80 | ns |
| 4 | Access Time from \overline{CAS} | 7,9 | t_{CAC} | — | 15 | — | 20 | — | 20 | ns |
| 5 | Column Address Access Time | 8,9 | t_{AA} | — | 30 | — | 35 | — | 40 | ns |
| 6 | Output Hold Time | | t_{OH} | 0 | — | 0 | — | 0 | — | ns |
| 7 | Output Buffer Turn On Delay Time | | t_{ON} | 0 | — | 0 | — | 0 | — | ns |
| 8 | Output Buffer Turn off Delay Time | 10 | t_{OFF} | — | 15 | — | 15 | — | 20 | ns |
| 9 | Transition Time | | t_T | 2 | 50 | 2 | 50 | 2 | 50 | ns |
| 10 | \overline{RAS} Precharge Time | | t_{RP} | 40 | — | 45 | — | 50 | — | ns |
| 11 | \overline{RAS} Pulse Width | | t_{RAS} | 60 | 100000 | 70 | 100000 | 80 | 100000 | ns |
| 12 | \overline{RAS} Hold Time | | t_{RSH} | 15 | — | 20 | — | 20 | — | ns |
| 13 | \overline{CAS} to \overline{RAS} Precharge Time | | t_{CRP} | 5 | — | 5 | — | 5 | — | ns |
| 14 | \overline{RAS} to \overline{CAS} Delay Time | 11,12 | t_{RCD} | 20 | 45 | 20 | 50 | 20 | 60 | ns |
| 15 | \overline{CAS} Pulse Width | | t_{CAS} | 15 | — | 20 | — | 20 | — | ns |
| 16 | \overline{CAS} Hold Time | | t_{CSH} | 60 | — | 70 | — | 80 | — | ns |
| 17 | \overline{CAS} Precharge Time (Normal) | 17 | t_{CPN} | 10 | — | 10 | — | 10 | — | ns |
| 18 | Row Address Set Up Time | | t_{ASR} | 0 | — | 0 | — | 0 | — | ns |
| 19 | Row Address Hold Time | | t_{RAH} | 10 | — | 10 | — | 10 | — | ns |
| 20 | Column Address Set Up Time | | t_{ASC} | 0 | — | 0 | — | 0 | — | ns |
| 21 | Column Address Hold Time | | t_{CAH} | 12 | — | 12 | — | 15 | — | ns |
| 22 | \overline{RAS} to Column Address Delay Time | 13 | t_{RAD} | 15 | 30 | 15 | 35 | 15 | 40 | ns |
| 23 | Column Address to \overline{RAS} Lead Time | | t_{RAL} | 30 | — | 35 | — | 40 | — | ns |
| 24 | Column Address to \overline{CAS} Lead Time | | t_{CAL} | 30 | — | 35 | — | 40 | — | ns |
| 25 | Read Command Set Up Time | | t_{RCS} | 0 | — | 0 | — | 0 | — | ns |
| 26 | Read Command Hold Time Referenced to \overline{RAS} | 14 | t_{RRH} | 0 | — | 0 | — | 0 | — | ns |
| 27 | Read Command Hold Time Referenced to \overline{CAS} | 14 | t_{RCH} | 0 | — | 0 | — | 0 | — | ns |
| 28 | Write Command Set Up Time | 15 | t_{WCS} | 0 | — | 0 | — | 0 | — | ns |
| 29 | Write Command Hold Time | | t_{WCH} | 10 | — | 10 | — | 12 | — | ns |
| 30 | \overline{WE} Pulse Width | | t_{WP} | 10 | — | 10 | — | 12 | — | ns |
| 31 | Write Command to \overline{RAS} Lead Time | | t_{RWL} | 15 | — | 20 | — | 20 | — | ns |
| 32 | Write Command to \overline{CAS} Lead Time | | t_{CWL} | 15 | — | 18 | — | 20 | — | ns |
| 33 | DIN set Up Time | | t_{DS} | 0 | — | 0 | — | 0 | — | ns |
| 34 | DIN Hold Time | | t_{DH} | 10 | — | 10 | — | 12 | — | ns |
| 35 | \overline{RAS} Precharge time to \overline{CAS} Active Time (Refresh cycles) | | t_{RPC} | 0 | — | 0 | — | 0 | — | ns |

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

| No. | Parameter | Notes | Symbol | MB85341A-60 | | MB85341A-70 | | MB85341A-80 | | Unit |
|-----|--|-------|-------------------|-------------|--------|-------------|--------|-------------|--------|------|
| | | | | Min | Max | Min | Max | Min | Max | |
| 36 | $\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh | | t_{CSR} | 0 | — | 0 | — | 0 | — | ns |
| 37 | $\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh | | t_{CHR} | 10 | — | 10 | — | 12 | — | ns |
| 38 | $\overline{\text{WE}}$ Set Up Time from $\overline{\text{RAS}}$ | 18 | t_{WSR} | 0 | — | 0 | — | 0 | — | ns |
| 39 | $\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ | 18 | t_{WHR} | 10 | — | 10 | — | 10 | — | ns |
| 40 | DIN to $\overline{\text{CAS}}$ Delay Time | | t_{DZC} | 0 | — | 0 | — | 0 | — | ns |
| 41 | Fast Page Mode $\overline{\text{RAS}}$ Pulse width | | t_{RASP} | — | 200000 | — | 200000 | — | 200000 | ns |
| 42 | Fast Page Mode Read/Write Cycle Time | | t_{PC} | 40 | — | 45 | — | 45 | — | ns |
| 43 | Access Time from $\overline{\text{CAS}}$ Precharge | 9,16 | t_{CPA} | — | 35 | — | 40 | — | 40 | ns |
| 44 | Fast Page Mode $\overline{\text{CAS}}$ Precharge Time | | t_{CP} | 10 | — | 10 | — | 10 | — | ns |
| 45 | Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | | t_{RHCP} | 35 | — | 40 | — | 40 | — | ns |

Notes:

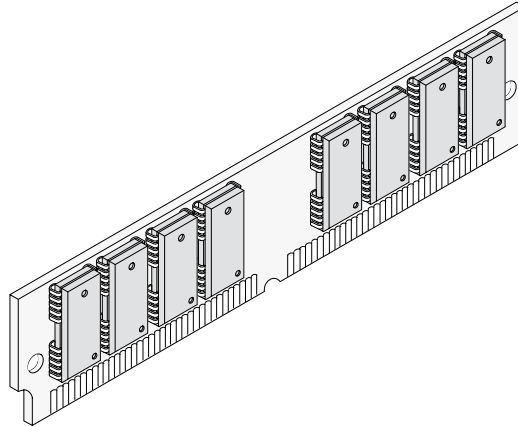
- Referenced to VSS.
- ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
ICC depends on the number of address change as $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VIH}$, $\text{VIL} > -0.5\text{V}$.
ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VIH}$.
ICC4 is specified at one time of address change during one Page cycle.
- An initial pause ($\overline{\text{RAS}} = \overline{\text{CAS}} = \text{VIH}$) of 200 μs is required after power-up followed by any eight $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- AC characteristics assume $t_{\text{T}} = 5\text{ns}$.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
- If $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$, and $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{CAC} .
- If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{AA} .
- Measured with a load equivalent to two TTL loads and 100 pF.
- t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
- Operation within the $t_{\text{RCD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2t_{\text{T}} + t_{\text{ASC}}(\text{min})$.
- Operation within the $t_{\text{RAD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the data output pin will remain High-Z state through entire cycle.
- t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{\text{CAS}}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than $t_{\text{CPA}}(\text{max})$.
- Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh.
- Assumes that Test mode function.

* Source: See MB814400A Data Sheet for details on the electricals.

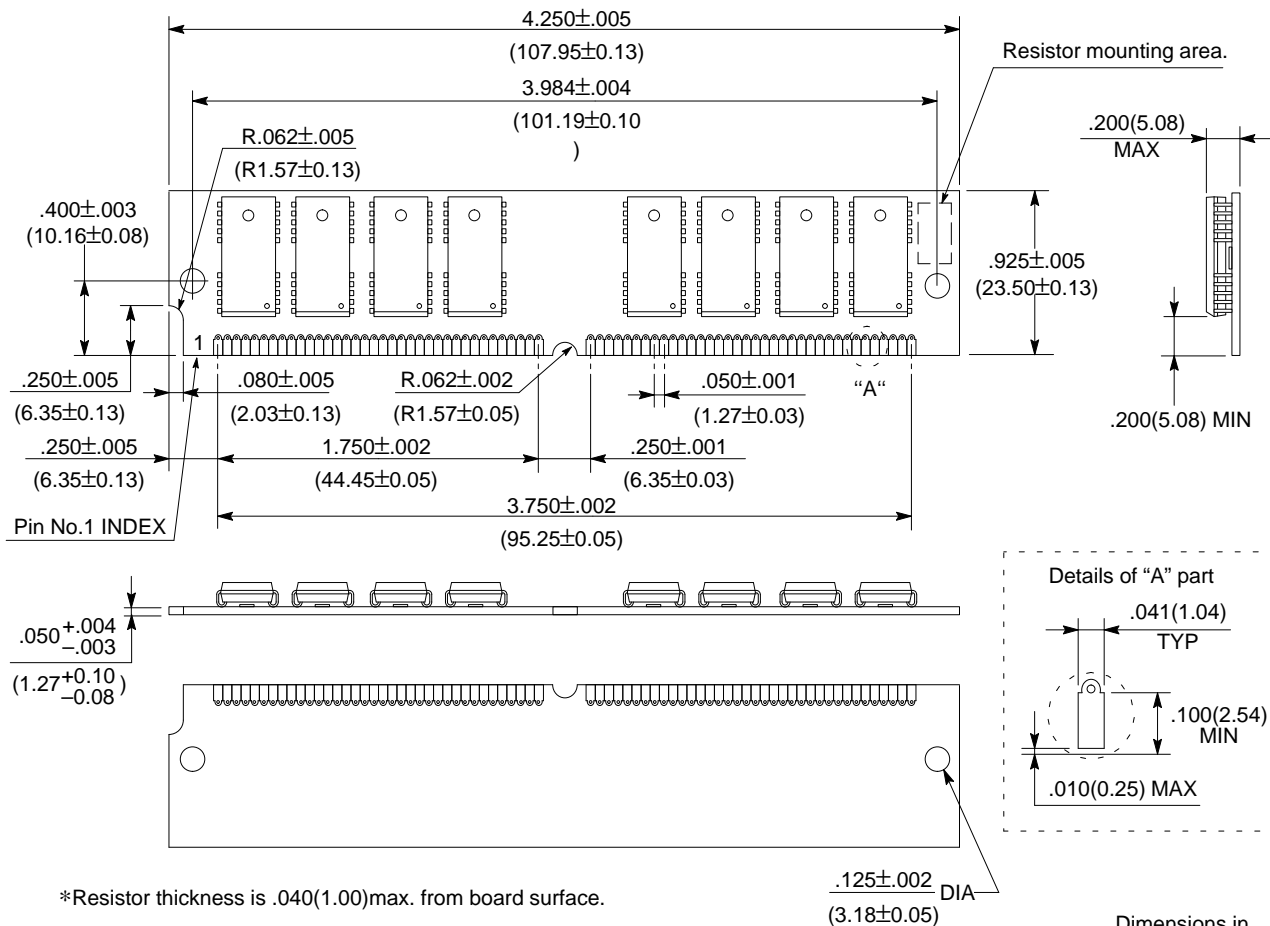
MB85341A-60
MB85341A-70
MB85341A-80

PACKAGE DIMENSIONS

(Suffix: PJPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P29)

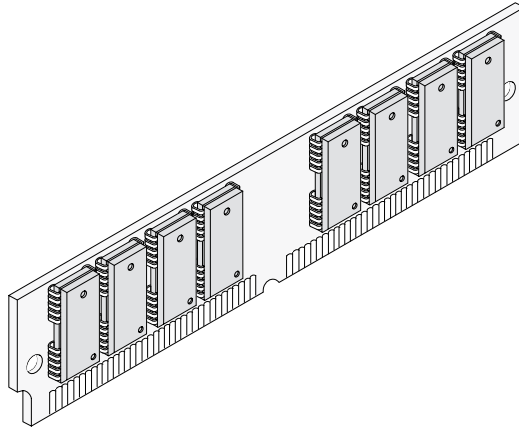


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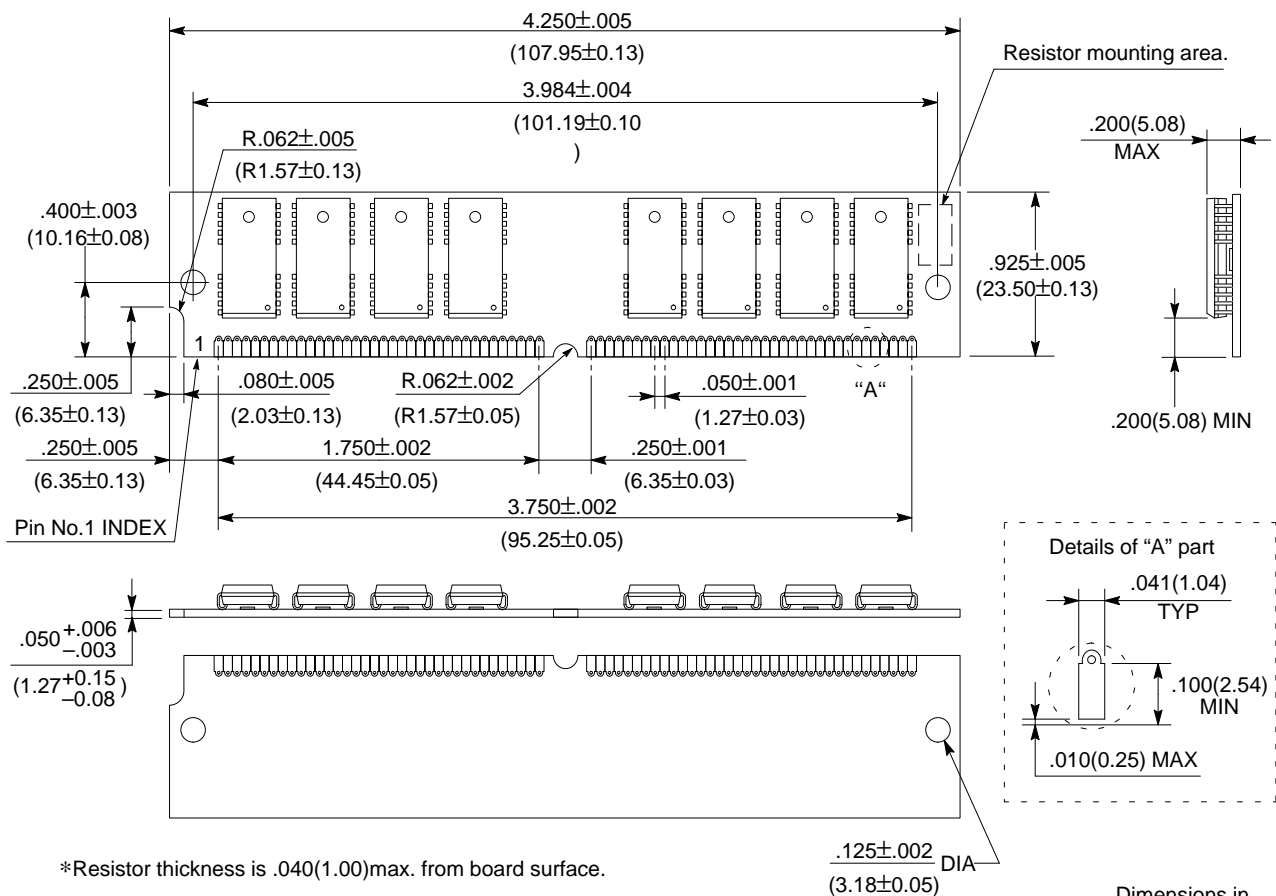
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PJPB)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P48)



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Dimensions in
inches (millimeters)

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