

Fujitsu

16M Bit

Synchronous

DRAM

Target Spec

MB81116421A/MB81116422A 16M BIT SYNCHRONOUS DRAM

Organization 2 banks x 2,097,152 words x 4 bit

Clock Frequency 125/100/83/67 MHz max.

Refresh Cycle 65.6ms/4,096cycles

Power Supply 3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series-Terminated Transceiver Logic
MB81116421A Only

2 Banks Interleave Operation
With Bank Select (A11)

Programmable Burst Type
(Sequential/Interleave)

Programmable Burst Length
(1, 2, 4, 8, or Full Column)

Programmable CAS latency
(1, 2, or 3)

Burst Stop Function

Burst Read/Single Write Capability

Auto-refresh & Self-refresh

Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

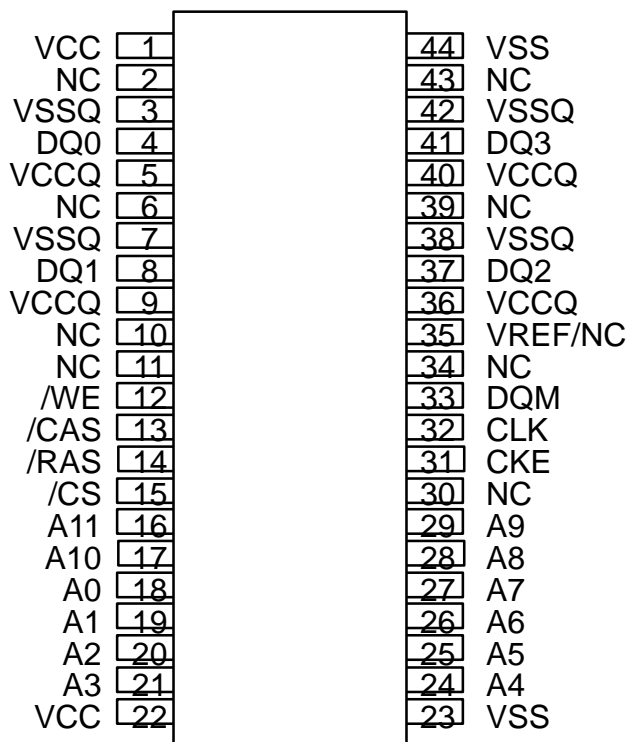
Address

Row Address A0–A10

Column Address A0–A9

Bank Select A11

Package : 44pin TSOP Type-II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

DYNAMIC RAM

MB81116821A/MB81116822A 16M BIT SYNCHRONOUS DRAM

Organization 2 banks x 1,048,576 words x 8 bit

Clock Frequency 125/100/83/67 MHz max.

Refresh Cycle 65.6ms/4,096cycles

Power Supply 3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series-Terminated Transceiver Logic
MB81116821A Only

2 Banks Interleave Operation
With Bank Select (A11)

Programmable Burst Type
(Sequential/Interleave)

Programmable Burst Length
(1, 2, 4, 8, or Full Column)

Programmable CAS latency
(1, 2, or 3)

Burst Stop Function

Burst Read/Single Write Capability

Auto-refresh & Self-refresh

Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

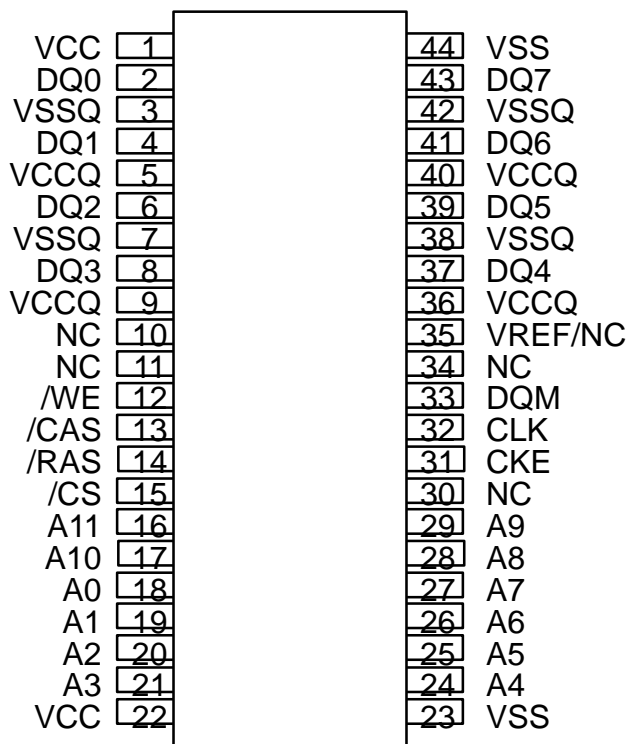
Address

Row Address A0–A10

Column Address A0–A8

Bank Select A11

Package : 44pin TSOP Type-II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

DYNAMIC RAM

MB811161621A/MB811161622A 16M BIT SYNCHRONOUS DRAM

Organization 2 banks x 524,288 words x 16 bit

Clock Frequency 125/100/83/67 MHz max.

Refresh Cycle 65.6ms/4,096cycles

Power Supply 3.3 ± 0.3 V

Fully Synchronous Operation
Referred To The Positive Clock Edge

LVTTL & SSTL* I/O Interface

* : Stub Series-Terminated Transceiver Logic
MB811161621A Only

2 Banks Interleave Operation
With Bank Select (A11)

Programmable Burst Type
(Sequential/Interleave)

Programmable Burst Length
(1, 2, 4, 8, or Full Column)

Programmable CAS latency
(1, 2, or 3)

Burst Stop Function

Burst Read/Single Write Capability

Auto-refresh & Self-refresh

Clock Enable For Timing
Synchronization And Power Down

Input Data And Output Mask Option

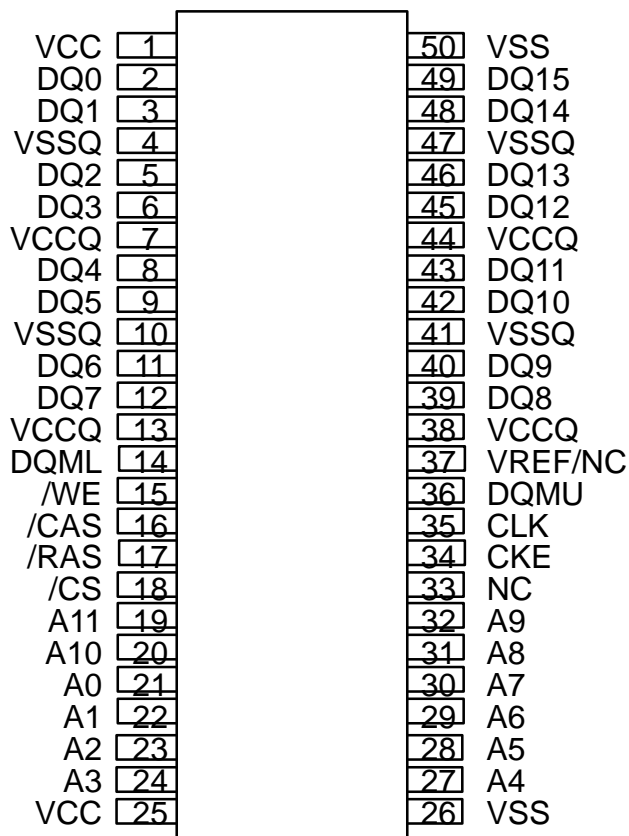
Address

Row Address A0–A10

Column Address A0–A7

Bank Select A11

Package : 50pin TSOP Type-II Package
(400mil, 0.8mm Lead Pitch)



Pin Assignment
(Top View)

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