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Two-dimensional Mathematical Analysis of a Planar Type Junction Field-effect Transistor*

Abstract: A two-dimensional mathematical analysis is presented of the steady-state mechanisms of operation within a planar type junction field-effect transistor (JFET). This analysis shows that the potential distribution within the source-drain channel follows from solutions of Poisson's equation rather than from Laplace's equation. In particular, velocity-limited carrier transport produces a region of carrier accumulation in a region of the source-drain channel previously assumed to be depleted of carriers by the gate junction space-charge layers. The results of this two-dimensional mathematical analysis are presented in graphic form.

Introduction

In previous publications[1,2] a phenomenological discussion was presented describing the mechanisms of operation within the semiconductor device of Fig. 1. In these publications a field-effect device was proposed in which the source and drain contacts are electrically isolated by the space-charge layers of two planar gate junctions, even at potential equilibrium. Therefore, little source-drain electric current is possible until a forward biasing voltage is applied to the gate junctions. In this mode of operation (forward-biased gate junctions), the gate junction biasing voltage is not sufficient to produce a significant gate junction electric current, although this biasing voltage is sufficient to produce gate junction space-charge layer contraction. In this fashion, it was proposed that a small forward biasing voltage upon the gate junctions would produce a significant increase of source-drain electric current.

This phenomenological model is based upon a depletion layer concept of p-n junction operation. From the depletion layer theory,[3] the gate junction space-charge layers are assumed to be ideally depleted of mobile charge carriers (holes and electrons). For this reason immobile ionized impurity atoms constitute the only source of electrostatic charge. Therefore, no source-drain electric current is considered possible when the source-drain channel is completely obstructed by an ideally depleted gate junction space-charge layer. It can be shown, however, that the gate junction space-charge layer is never completely depleted of mobile charge carriers[4]; many questions therefore arise concerning the mechanisms by which the source-drain electric current is influenced by a gate junction biasing voltage.

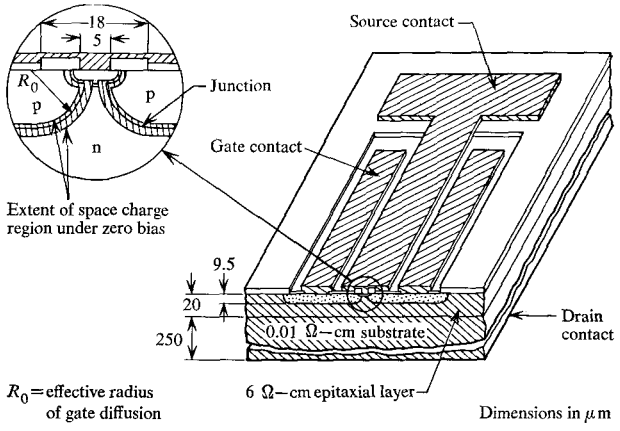

Figure 1 Illustration of the field-effect device model considered in this investigation (from Ref. 2).

Additional questions arise concerning the forward-bias mode of gate junction operation. From an extension of the depletion layer theory, space-charge layer contraction is frequently considered a fundamental consequence resulting from the forward biasing of any p-n junction. In contrast, a rigorous mathematical treatment of the p-n junction problem shows that space-charge layer contraction cannot always be taken for granted. For example,

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asymmetrical abrupt p-n junctions do indeed exhibit space-charge layer contraction,[4] although space-charge layer expansion is sometimes encountered in a forward-biased linearly graded p-n junction.[5,6] Because the characteristics of a diffused p-n junction lie somewhere between those of an abrupt and those of a linearly graded type of structure[7,8] (depending upon design), it is particularly difficult to determine qualitatively the predominating mechanisms within the gate junctions of this field-effect device.

These important questions of field-effect device theory are answerable only through a rigorous mathematical treatment of the problem. For this reason, a computer program has been developed for the two-dimensional solution of a boundary value problem closely approximating the structure shown in Fig. 1. The computer program provides a detailed two-dimensional calculation of the impurity atom distribution introduced during device fabrication. Thereafter, the computer program provides a two-dimensional solution of the ambipolar diffusion equations for holes and electrons; the solution is subject to constraints imposed by the calculated impurity atom distribution, and also by the geometrical structure of the particular semiconductor device.

From this method of analysis, detailed information is obtained concerning the mechanisms of operation within a junction field-effect transistor. For example, it is mathematically verified that, when the gate junctions are electrically connected to either the source or drain contact (no external gate biasing voltage), electric-current saturation arises from a reverse biasing of the gate junctions by the applied source-drain biasing voltage. In this particular structure (Fig. 1), it is shown that current saturation occurs after the gate junction space-charge layers have extended across the entire source-drain channel; the source-drain electric current is therefore a consequence of charge carrier transport through the gate junction space-charge layers. For this reason, by forward biasing the gate junction a reduction of reverse bias is obtained in those regions of the gate junction that bound the source-drain channel. This situation indicates that many similarities exist between the device shown in Fig. 1 and the more conventional field-effect devices.

The present analysis also shows that the process of electrical conduction within a source-drain channel follows from solutions of Poisson's equation, rather than from Laplace's equation (Ohm's Law). The potential distribution within a source-drain channel is influenced by an electrostatic charge distribution induced by the gate junction space-charge layers.

Mathematical methods

This analysis is composed of two different calculations: first, a calculation of the impurity atom distribution within the semiconductor device; second, a calculation of the hole and electron distributions arising from a given set of applied biasing voltages. This series of calculations is conducted for a mathematical model (Fig. 2) approximating the cross section of the device shown in Fig. 1. This analysis gives detailed information concerning the space-charge distribution, the hole and electron distributions, the electrostatic potential distribution, and the electric current distribution within the structure under consideration.

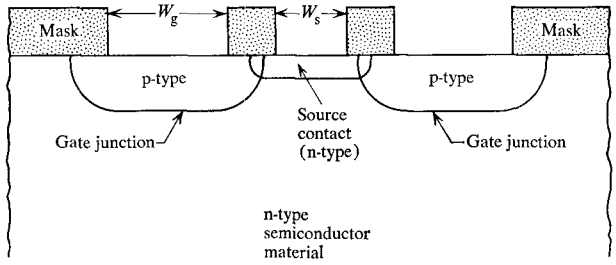


Figure 2 Two-dimensional mathematical model for Fig. 1.

• *Impurity atom distribution calculations*

In Fig. 2 the entire semiconductor surface is assumed to be covered by a diffusion mask, with the exception of those regions of the surface from which diffusion is to take place. It is emphasized that this analysis is based upon an idealization of the oxide masking technique. For purposes of analysis, the diffusion mask is assumed to be an impenetrable barrier for impurity atoms, thereby reducing to zero the impurity atom flux normal to the semiconductor surface. Furthermore, it is presumed that a path of easy diffusion does not exist along the mask-semiconductor boundary.

From the elementary theory of diffusion,[9] the distribution of impurity atoms within this device can be approximated by a solution of the differential equation,

$$\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} = \frac{1}{D}\frac{\partial C}{\partial t}, \tag{1}$$

where $C(x, y, t)$ is the impurity atom distribution and D is the diffusion constant for these impurities in silicon. In addition to satisfying Eq. (1), this solution must also satisfy all the boundary conditions imposed during device fabrication.

There is no known analytical solution for Eq. (1) that is consistent with the boundary conditions shown in Fig. 2. In fact, this particular type of mixed boundary value problem is one of recognized mathematical difficulty.[10] For this reason, relaxation methods[11] have been used to obtain the required impurity atom distribution. The entire two-dimensional analytical model (Fig. 2) is approximated by an array of about eight thousand spatial locations. Boundary conditions are approximated

by maintaining a specified impurity atom density at locations representing the semiconductor surface. Thereafter, the impurity atom density within this array is relaxed in a manner consistent with a finite difference approximation for Laplace's equation; thereby the diffusion process is synthesized.[11e] After a prescribed number of relaxation cycles through this matrix array, the resulting impurity atom distribution is taken to be the required solution for this boundary value problem.

In this fashion, an impurity atom density is calculated at each location within the approximating array. Thereafter the impurity atom distribution is used in calculations relating to the electrical properties of the field-effect device under consideration.

• *Semiconductor calculations*

In a semiconductor, the distribution of mobile holes and electrons is described by the mathematical equations[12]

$$\text{(a)}\quad \text{div grad } \Psi = -\frac{q}{\kappa\epsilon_0}(C - n + p),$$

$$\text{(b)}\quad \mathbf{J}_p = -qD_p \text{ grad } p - q\mu_p p \text{ grad } \Psi,$$

$$\text{(c)}\quad \mathbf{J}_n = qD_n \text{ grad } n - q\mu_n n \text{ grad } \Psi,$$

$$\text{(d)}\quad \text{div } \mathbf{J}_p = q\mathcal{R}_p,$$

$$\text{(e)}\quad \text{div } \mathbf{J}_n = q\mathcal{R}_n, \text{ and}$$

$$\text{(f)}\quad \mathbf{J}_T = \mathbf{J}_n + \mathbf{J}_p, \qquad (2)$$

by assuming no trapping mechanisms within the structure under consideration.

Equation (2a) is Poisson's equation, and it relates the divergence of the electric field ($\mathbf{E} = -\text{grad } \Psi$) to the electrostatic charge distribution arising from mobile charge carriers (holes and electrons) and immobile ionized impurity atoms within the semiconductor lattice. In Eq. (2a), the ionized impurity atom distribution C is obtained from the previously described solution of Eq. (1), by assuming that all impurity atoms within the semiconductor material are ionized.

Equations (2b) and (2c) describe the electric current distribution in a semiconductor arising from the transport of mobile holes and electrons. These equations express the dependence of each electric current component ($\mathbf{J}_n$ and $\mathbf{J}_p$) upon the concentration gradients of holes and electrons, the mobility of these charge carriers, and the electrostatic potential gradient (electric field) within the semiconductor material.

For simplicity, the hole and electron mobilities (μ_p, μ_n) are often assumed to be invariant within a given sample of semiconductor material. This is sometimes an unreasonable simplification. Experiment shows that the mobility for holes and electrons alike undergoes large changes.[5,13] Such changes arise from large values of electric field and from large values of impurity atom density within the semiconductor material. For this reason, the present analysis takes into consideration the influence of both electric field and impurity atom density upon the mobility of holes and electrons. The large-electric-field properties of mobile carriers were taken directly from the publication of Ryder[13a] on this subject. The small-electric-field mobility of holes and electrons (due to variations of impurity atom density) has been taken directly from the publication of Wolfstirn.[13f]

Equations (2d) and (2e) are the continuity equations for holes and electrons; in these equations the mechanisms of carrier generation and recombination remain unspecified. As in other mathematical investigations of junction field-effect transistor operation, carrier generation/recombination is assumed to be zero within the structure under investigation. This assumption has little (or no) influence upon the mechanisms of operation to be presented here.

Equation (2f) states that the total electric current density ($\mathbf{J}_T$) is the vector sum of the electric currents due to holes ($\mathbf{J}_p$) and to electrons ($\mathbf{J}_n$).

The six equations (2) have been combined into three simultaneous nonlinear differential equations in three variables: electrostatic potential, mobile-hole concentration and mobile-electron concentration. A rigorous mathematical analysis of this semiconductor device requires the solution of these three simultaneous equations. Such a solution is a difficult task; in fact, any attempt to solve this problem by traditional analytical means will probably fail and it appears reasonable to assume that there exists no rigorous analytical solution. For this reason, numerical techniques have been used throughout the present investigation.

The calculations presented in this paper result from two-dimensional simultaneous numerical solutions of the equations (2). Three two-dimensional nodal arrays are used to represent the device under consideration (Fig. 2). Boundary conditions for each independent variable, in addition to the calculated impurity atom distribution, are introduced as constraints upon the solutions obtained for each array. Thereafter, using a finite-difference form for these differential equations, relaxation techniques[11] are applied sequentially to the three arrays; this method provides detailed information concerning the mechanisms of operation within this semiconductor device.

Impurity atom distribution calculations

Figure 3 illustrates a calculated profile for the metallurgical p-n junctions within this semiconductor device. The calculation is based upon the impurity atom diffusion process used in device fabrication. Figure 3 shows the junction profile within a structure assumed to have an ideal geometrical configuration (perfect diffusion mask alignment).

In the present series of calculations (Fig. 3), the gate junctions and the source contact are assumed to be formed by two independent diffusions. The gate junctions are formed by a two-step diffusion process[14]; boron is initially diffused for 5 minutes into the semiconductor from a constant surface concentration of 2×10^{20} atoms/cm^3. Thereafter, the impurity atom source is removed and the gate junction diffusion process is continued for 40 minutes. During this 40-minute diffusion, oxide growth takes place within the gate junction diffusion mask openings.

For purposes of mathematical simplification, the mechanism of oxide growth is neglected in this analytical investigation. Oxide growth represents a motion of the semiconductor surface during diffusion, and thereby numerous additional complications arise in an already complex two-dimensional diffusion problem. Because the gate junction depth is approximately 10 μm from the semiconductor surface, it is believed that oxide growth during gate junction diffusion has a negligible influence upon the final impurity atom distribution.

After the completion of this gate junction fabrication, a new diffusion mask opening is introduced (W_s in Fig. 2), and phosphorus (n-type) is diffused into the semiconductor from a constant-C_0 source (5×10^{21} atoms/cm^3). The phosphorus diffusion provides a source contact for the device being fabricated.

Although Fig. 3 provides a pictorial view of the junction locations within this device, such information is of little practical value in the present investigation. Instead, a calculation of the electrical properties attributable to this device requires detailed information concerning the impurity atom distribution throughout the entire structure under consideration. Such information is available within the computer memory, after concluding the calculations for Fig. 3.

Equilibrium space-charge layer calculations

These numerical methods have been used to calculate the electrostatic charge distribution within the source-drain channel of the structure shown in Fig. 3, by assuming potential and thermal equilibrium. Such calculations uncover important inadequacies in a one-dimensional analysis of this problem. In particular, a one-dimensional analysis cannot take into consideration modifications of the gate junction space-charge layers that arise from changes in impurity atom density along the length of the source-drain channel. These changes of impurity atom density have a significant influence upon the equilibrium gate junction space-charge layers, and hence upon the ultimate electrical properties of this device.

In one dimension, the gate junction space-charge layers are assumed to penetrate into a source-drain channel of constant impurity atom density. Contrasting with this

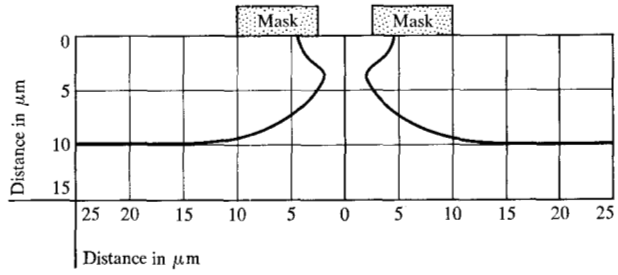


Figure 3 Calculated p-n junction profile within the device considered in this investigation.

one-dimensional concept, the source-contact diffusion introduces a region of large impurity atom gradient, and this gradient terminates near the point of minimum source-drain channel width. Therefore, the channel is bounded by a high-low type of semiconductor junction, and this junction also contains a space-charge region.[15] The close proximity of the high-low junction to these gate junctions implies that the gate junction space-charge layers could penetrate into semiconductor material already containing a significant electrostatic charge. This proposal is confirmed in Fig. 4.

Figure 4 illustrates the calculated electrostatic charge distribution within the source-drain channel for structures containing minimum channel widths of approximately 3.0, 2.0 and 1.0 μm. In this illustration, the metallurgical gate junctions are represented by heavy solid lines; the lighter solid lines describe contours of positive electrostatic charge on the channel side of the metallurgical junctions. These regions of positive electrostatic charge arise from electron depletion within the n-type material.

In a similar fashion the dashed contours lying within this source-drain channel (Fig. 4) describe a region of negative electrostatic charge arising from electron accumulation. This region of negative charge is one-half the electrostatic double-layer attributable to the high-low junction formed during source contact diffusion. Unlike a p-n junction, the high-low junction (n-n$^+$) acquires an electrostatic double-layer by redistributing majority carriers (electrons) within both sides of the structure. A region of negative electrostatic charge results from electron accumulation on the low conductivity side of the junction in Fig. 4, while a positive electrostatic charge arises from electron depletion within the source contact region.

Although the positive half of this double-layer is not shown in Fig. 4, it nonetheless exists within these calculated charge distributions. In Fig. 4, a positive electrostatic charge of small density exists throughout the entire source contact region.

These calculations (Fig. 4) show that when the metallurgical channel width is in excess of 2.0 μm, a path of large electrical conductivity exists between the source and

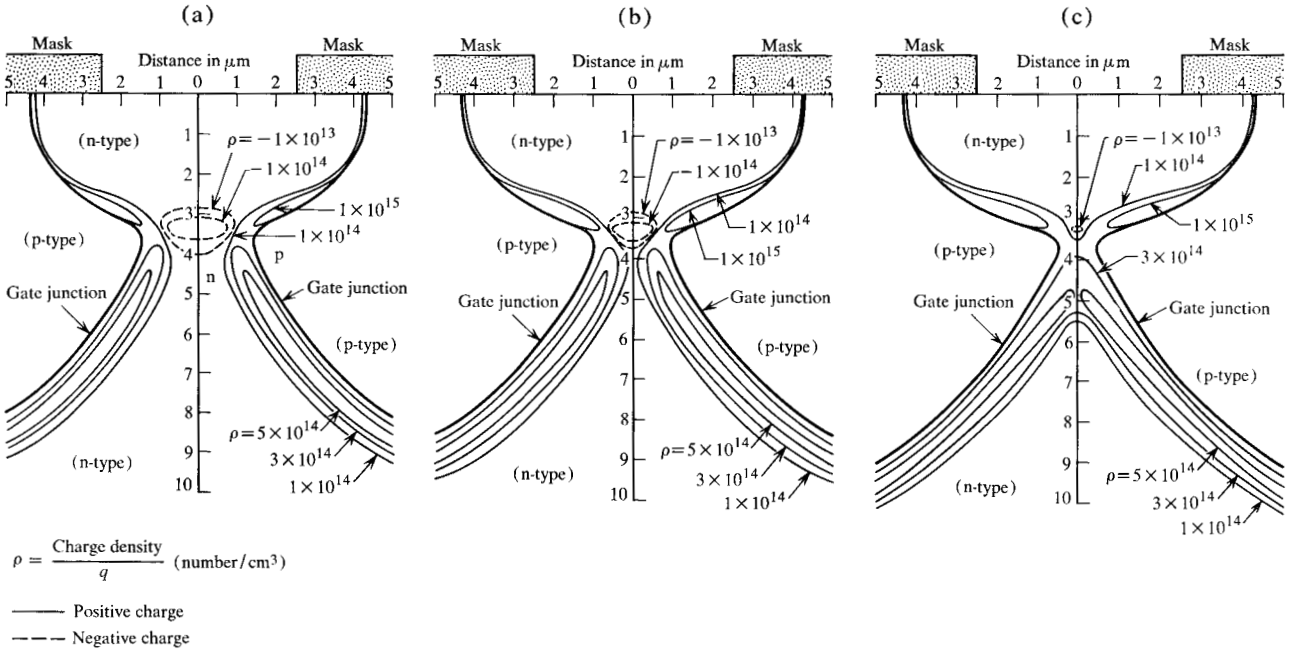
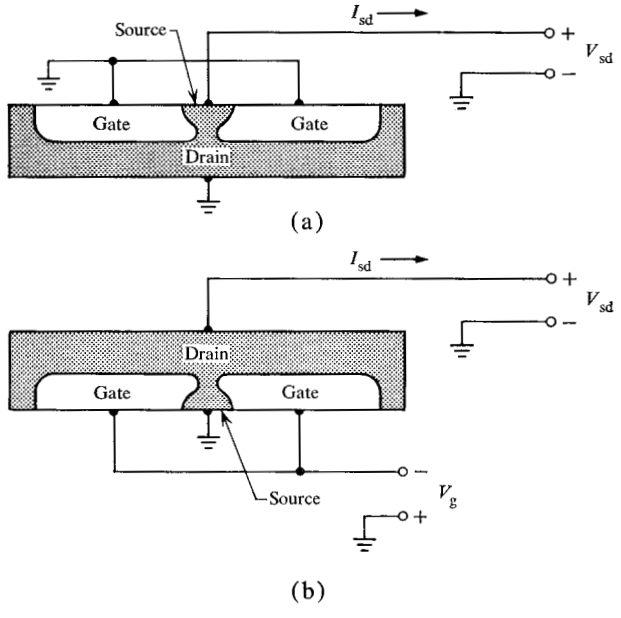


Figure 4 Calculated electrostatic charge distribution within the source-drain channel for three different values of minimum channel width: (a) 30 μm; (b) 2.0 μm; (c) 1.0 μm.

Figure 5 Schematic diagram of the circuit configurations in which electric current saturation is observed. (a) Grounded drain; (b) grounded source.



drain contacts of the device. In contrast, a metallurgical channel width of 1.0 μm results in a substantial degree of source-drain channel pinch-off, even at potential equilibrium. In this narrow channel structure (1.0 μm), the equilibrium gate junction space-charge layers remove many mobile charge carriers from the source-drain channel. Electrical conduction within this channel therefore must always take place through a region depleted of mobile charge carriers.

Electric current saturation

In the absence of a gate junction biasing voltage the source-drain electrical characteristics of this semiconductor device exhibit current saturation. Figure 5 illustrates two substantially different circuit configurations in which current saturation is observed. In Fig. 5(a), the gate junctions and the drain contact are grounded, and an external biasing voltage V_{sd} is applied to the source contact. In Fig. 5(b) the source contact is grounded, and an external biasing voltage V_{sd} is applied to the drain contact. Although the illustration, Fig. 5(b), contains an external gate junction biasing voltage V_g, the present discussion is directed toward device operation with no external biasing voltage applied to the gate junctions.

Throughout this paper the circuit configuration shown in Fig. 5(a) is called a grounded drain circuit. Similarly, Fig. 5(b) is called a grounded source circuit.*

At small values of biasing voltage (for example, up to about $V_{sd} = 0.75$ V), the source-drain electric current

* It is recognized that the source and drain contacts are traditionally selected to designate the direction of majority carrier flux within the channel of an FET. This convention is used in the initial publications[1,2] describing the device shown in Fig. 1; in these publications the direction of applied bias maintains the source contact at the semiconductor surface. Throughout the present investigation we have retained the terminology adopted by Roosild et al (Fig. 1): One contact to the source-drain channel is located at the semiconductor surface, and this is called the source contact, regardless of the direction of majority carrier flux within this channel.

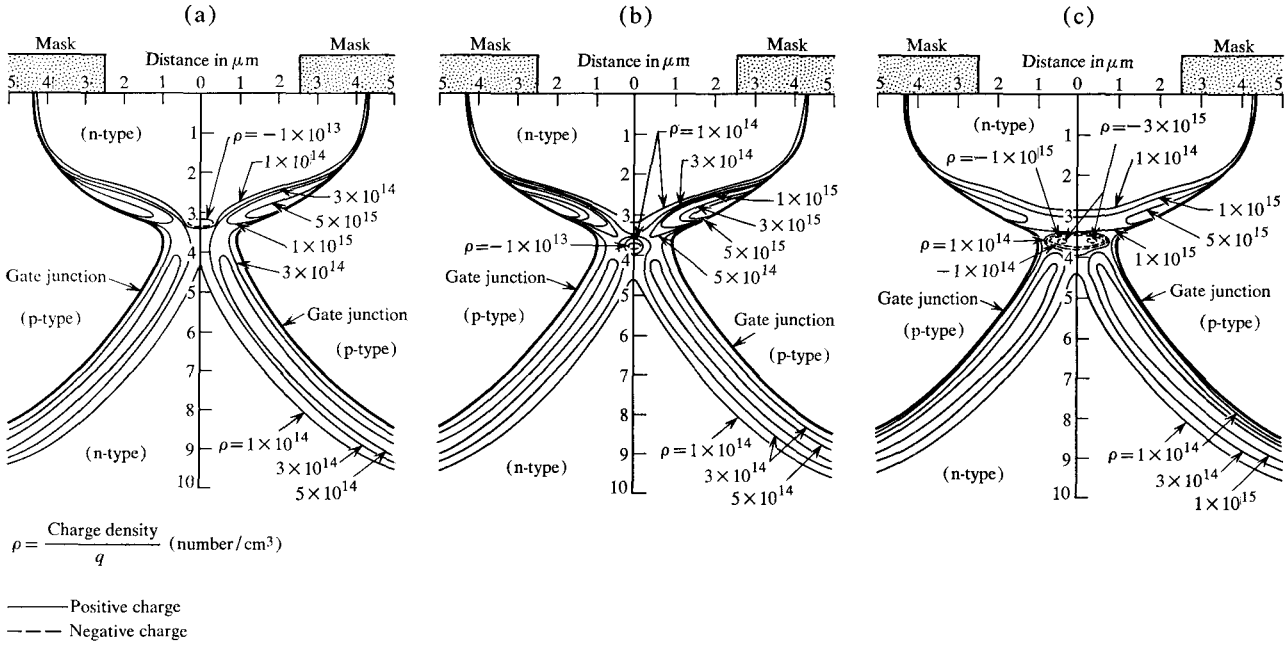


Figure 6 Calculated electrostatic charge distribution within the source-drain channel, grounded drain operation. $V_g = 0$. (a) $V_{sd} = 0.5$V; (b) $V_{sd} = 0.75$V; (c) $V_{sd} = 1.0$V.

I_{sd} exhibits a substantial increase with an increase of applied voltage. When this source-drain voltage V_{sd} has a magnitude in excess of some critical value (depending upon the specific device), it has been reported[16] that the electric current I_{sd} is nearly constant and independent of the biasing voltage; this situation is called current saturation.

The present discussion outlines the results of a mathematical investigation into the mechanisms of current saturation within this semiconductor device. Two different methods of operation are considered: the grounded drain circuit shown in Fig. 5(a), and the grounded source circuit shown in Fig. 5(b).

• *Grounded drain operation*

In the grounded drain circuit, Fig. 5(a), each gate junction is electrically connected to the drain contact; this connection assures that the distributed source-drain channel voltage appears as a reverse bias upon the gate junctions. In this fashion, gate junction space-charge layer widening eliminates mobile electrons from the n-type source-drain channel, and a modification is obtained in the electrostatic charge distribution within this channel. For purposes of comparison Fig. 6 illustrates the calculated space-charge distribution within the source-drain channel for three different assumed values of source-drain biasing voltage, $V_{sd} = 0.5$, 0.75 and 1.0 volts.

In grounded drain operation, little or no biasing voltage appears across those regions of the gate junctions that are far removed from the source-drain channel. In contrast, almost the entire source-drain voltage appears as a reverse bias across those parts of the gate junctions bounding the source contact region. In between the source contact region and the drain contact region (through the source-drain channel) the distribution of source-drain voltage determines the distribution of reverse bias upon the gate junctions. A detailed computation of the voltage distribution within this device is illustrated in Fig. 7, for two values of applied voltage, $V_{sd} = 0.5$ and 1.0 volts.

A comparison of Figs. 4 and 6 shows that an applied biasing voltage produces little space-charge layer widening within the source contact region. This situation is a result of the large impurity atom density introduced during source contact diffusion; a negligibly small charge is therefore required in the gate junction space-charge layer width to support the reverse biasing voltage applied to this part of each gate junction.

The application of a biasing voltage introduced some unexpected modifications in the calculated electrostatic charge distribution within the source-drain channel (see Fig. 6). At a bias of 0.5 volts, the gate junction space-charge layers extend across the source-drain channel within a region lying on the drain contact side of the electron accumulation layer. Furthermore, this extension of the gate junction space-charge layers decreases both the geometrical size and the density of accumulated electrons arising from the high-low junction. Figure 6 shows that an increase in the applied biasing voltage

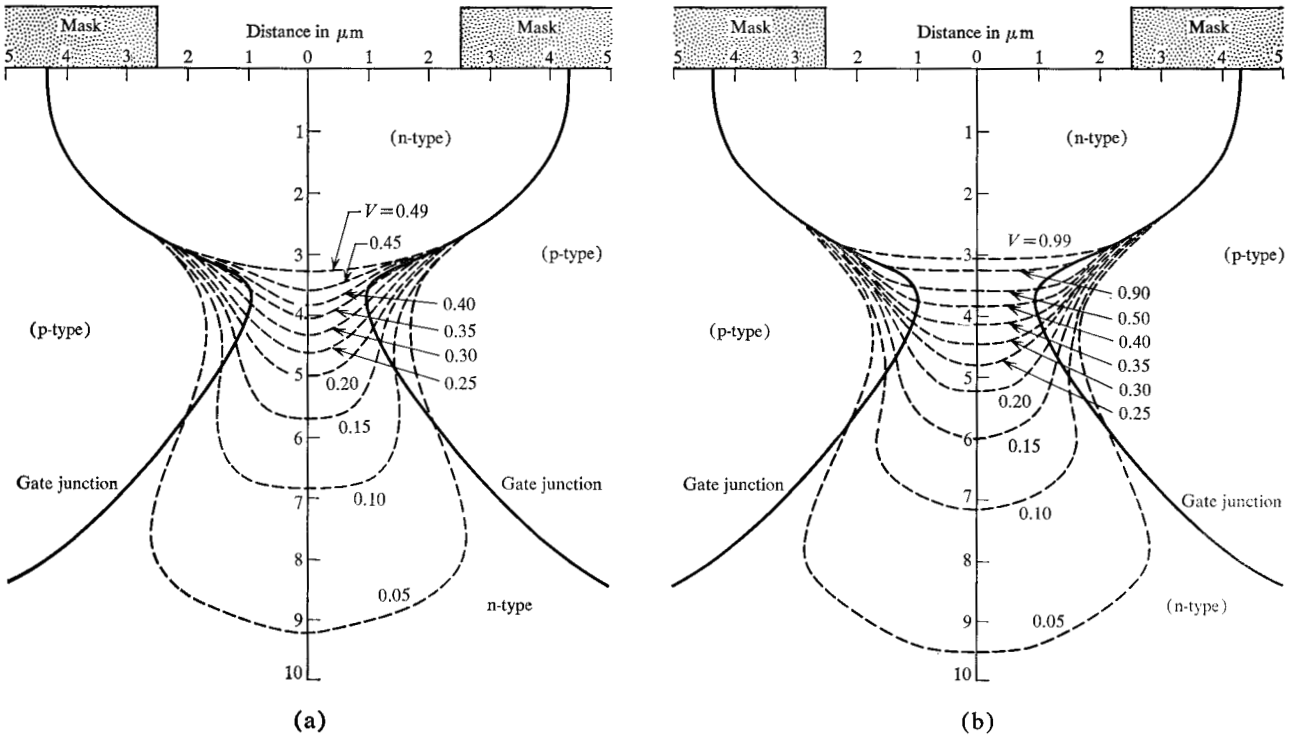
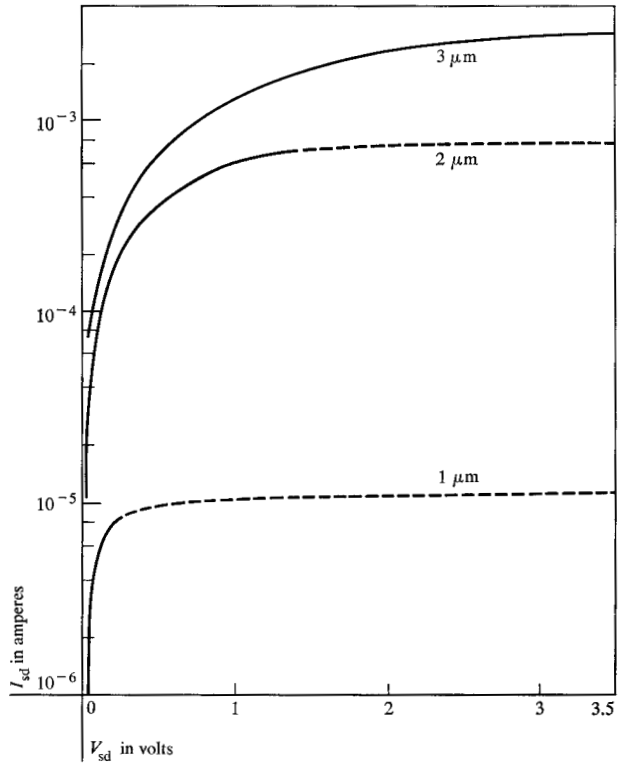


Figure 7 Calculated voltage distribution within the source-drain channel, grounded drain operation. $V_g = 0$. (a) $V_{sd} = 0.5$; (b) $V_{sd} = 1.0$ (all V in volts; this stipulation is implicit in subsequent Figures).

Figure 8 Calculated volt-ampere characteristics for three values of source-drain channel width, grounded drain operation.



(to 0.75 volts) introduces a further decrease in electron accumulation, accompanied by a physical displacement of the accumulation region to a location lying deeper within the source-drain channel. Although this modification may initially appear to be a minor deviation from the mechanisms of operation suggested by elementary theory, Fig. 6 also shows that a further increase of the applied biasing voltage (to 1.0 volts) accentuates this process of electron accumulation within the source-drain channel.

At a bias of 1.0 volts, an increase is observed in the calculated density of the accumulated electrons residing within the source-drain channel; this increase in accumulated electrons is observed as an increase in negative electrostatic charge (Fig. 6). It is emphasized that this region of electron accumulation resides within the source-drain channel at a location where elementary theory would predict an extensive degree of mobile carrier depletion.

An important conclusion from this series of calculations (Fig. 6) is that, at voltages substantially below electric current saturation (saturation is encountered at a source-drain bias of 0.75 to 1.0 volts), the gate junction space-charge layers extend across the entire source-drain channel. Implied by this situation is that electric current saturation in this device cannot be viewed as the simple constriction of an ohmic conduction path between the

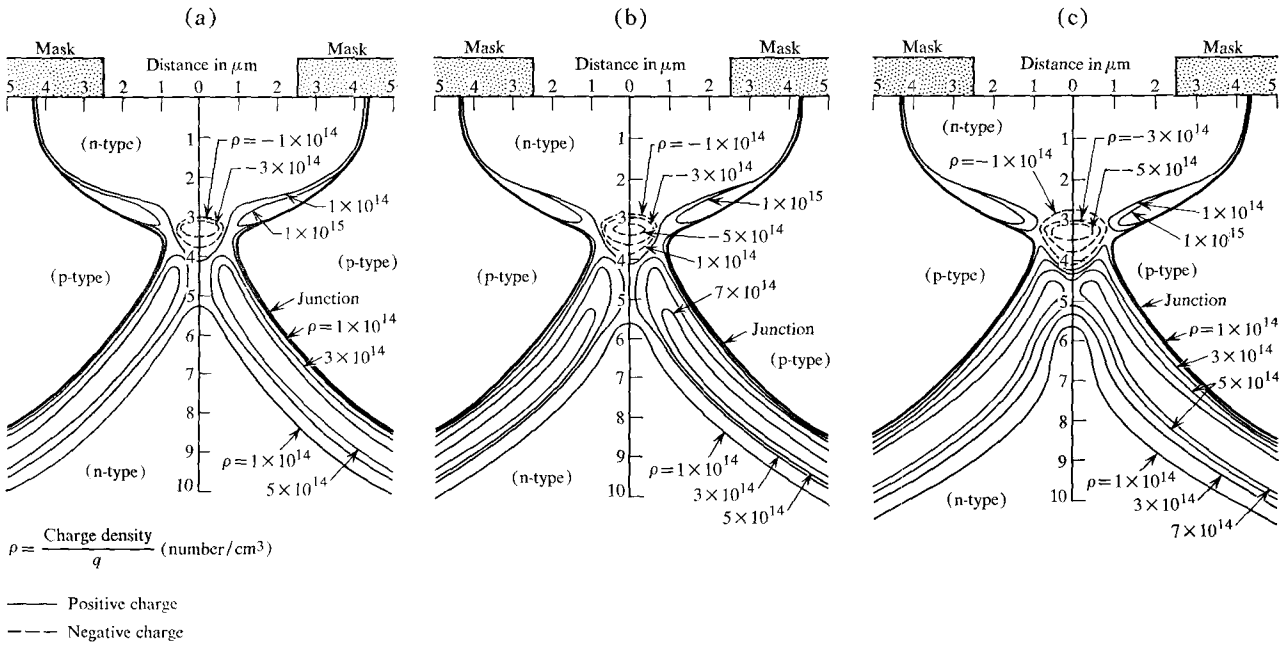


Figure 9 Calculated electrostatic charge distribution within the source drain channel, grounded-source operation. $V_g = 0$. (a) $V_{sd} = 0.5$; (b) $V_{sd} = 1.0$; (c) $V_{sd} = 2.0$.

source and drain contacts. Instead, the source-drain electric current arises from charge carrier transport through a region of substantial electrostatic charge; this region cannot be viewed as a simple ohmic conductor.[16] The voltage distribution within the source-drain channel is mathematically determined from solutions of Poisson's equation, which takes into consideration the influence of electrostatic charges residing within the path of electrical conduction.

Figure 8 illustrates the calculated volt-ampere characteristics of this device as used in a grounded drain circuit configuration. In Fig. 8, the solid lines represent calculated results while the dashed lines are extrapolations of these calculated results into a region of questionable computational accuracy. The questionable accuracy of this region has two sources: first, the unexpected space-charge distribution encountered within this source-drain channel; second, an inadequacy in the computer program used to solve this particular problem.

The computational difficulty illustrated in Fig. 8 arises from an inadequate nodal point density within the relaxation matrix used to approximate the source-drain channel. In this grounded drain circuit, current saturation results in substantial mobile carrier depletion from a narrow layer (estimated to be 0.125 μm in width) residing on the source contact side of the channel. For this reason, an exceedingly large nodal point density would be required in this computer program to accurately determine the free carrier density lying within this narrow layer; such information is necessary to accurately establish the source-drain electric current. A computer program containing this nodal point density is not now available.

From Fig. 8, an increase in source-drain channel width results in an increase in the biasing voltage required to obtain electric current saturation. In addition, this series of calculations indicates that an increase in channel width results in an increase in source-drain electric current when the device is biased into saturation. These changes in the volt-ampere characteristics with channel width are in qualitative agreement with experiments on devices containing a channel width of 2.0 μm or less.[17]

• *Grounded source operation*

Many differences are observed in the calculated electrostatic charge distribution between grounded drain and grounded source operation of this semiconductor device. In grounded source operation, the applied source-drain voltage reverse biases almost the entire gate junction, in fact all of it except that portion bounding the source contact region. Therefore, in grounded source operation, the gate junction space-charge layers introduce mobile carrier depletion throughout a comparatively large region lying between the point of minimum source-drain channel width and the drain contact. This increase in the size of the depleted region eliminates the computational difficulty discussed above in connection with grounded drain operation.

Figure 9 illustrates the calculated electrostatic charge distribution (grounded source operation) for three different values of source-drain biasing voltage: $V_{sd} = 0.5$, 1.0 and 2.0 volts. From this series of calculations, an

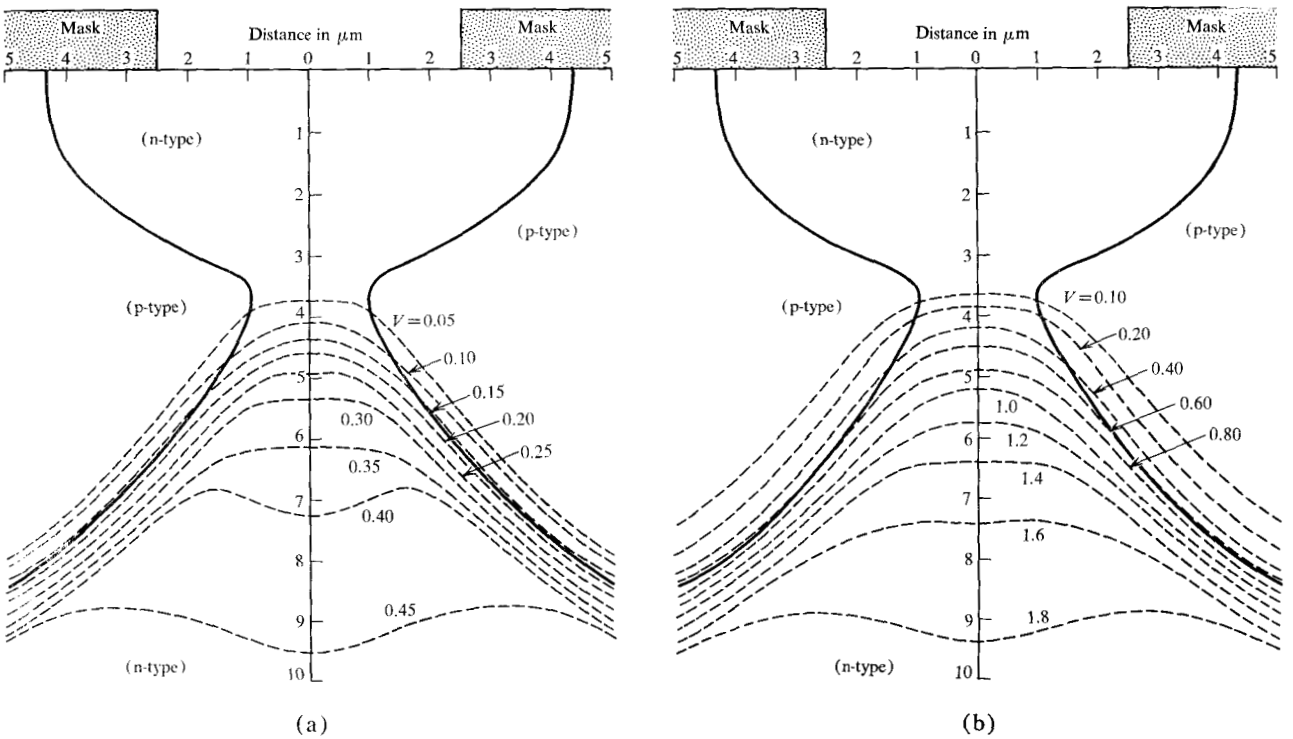
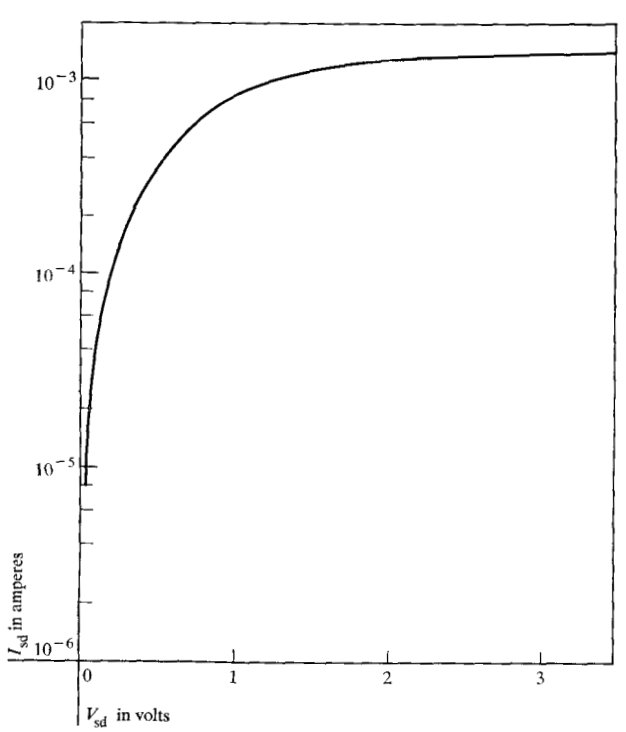


Figure 10 Calculated voltage distribution within the source-drain channel, grounded source operation. $V_g = 0$. (a) $V_{sd} = 0.5$; (b) $V_{sd} = 2.0$.

Figure 11 Calculated volt-ampere characteristic for a source-drain channel width of 2.0 μm, grounded source operation.



applied bias of 0.5 volts results in an extension of the gate junction space-charge layers across the source-drain channel, although this extension does not take place at the point of minimum channel width. Depletion of mobile carriers (electrons) is confined to a region adjacent to this point of minimum channel width, on the side nearest the drain contact. It is emphasized that the gate junctions introduce only partial depletion of mobile carriers from the source-drain channel; therefore substantial electric current results from this applied biasing voltage.

The calculated voltage distribution within this source-drain channel (Fig. 10) is plotted for two different values of biasing voltage: $V_{sd} = 0.5$ and 2.0 volts. The results of these calculations are consistent with the qualitative concepts of grounded source operation. That part of the gate junctions bounding the source contact region can be considered unbiased, and the remaining part of each gate junction is reverse biased. At a given location, the magnitude of gate junction biasing voltage is dependent upon the relative position of this location within the structure. Little reverse biasing voltage is found across the gate junctions near the point of minimum source-drain channel width. In contrast, gate junction regions far removed from the source-drain channel (on the drain contact side of the channel) are reverse biased by almost the total applied source-drain voltage.

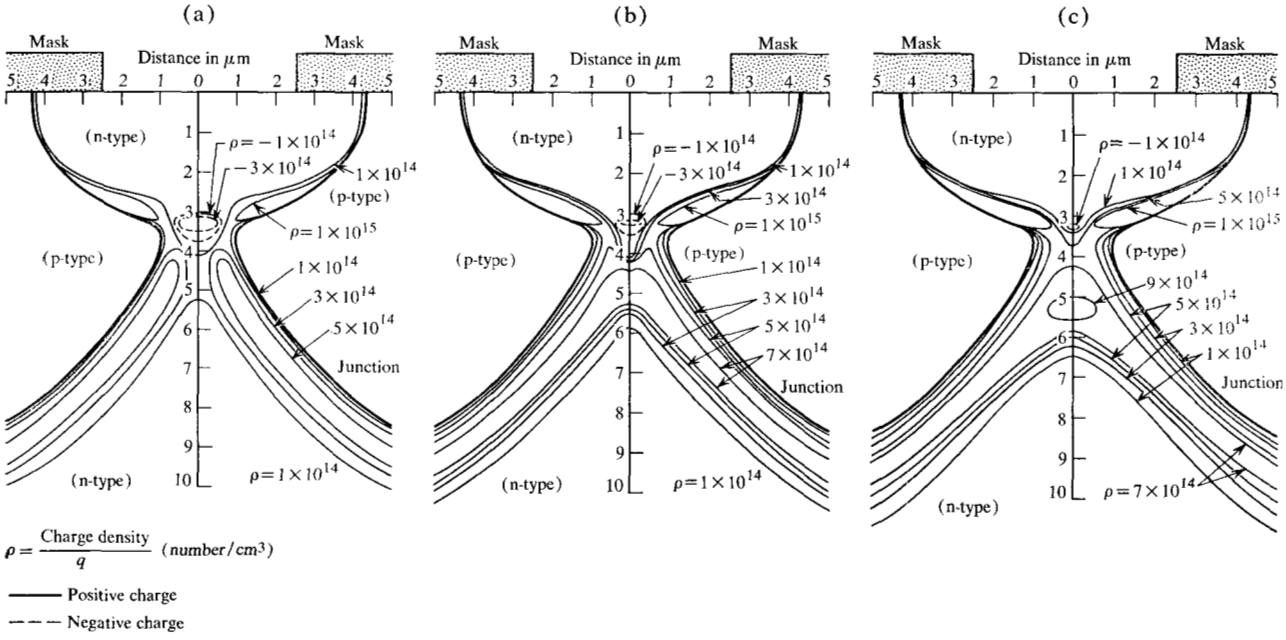


Figure 12 Calculated electrostatic charge distribution within the source-drain channel, grounded source operation. $V_{sd} = 0.5$. (a) $V_g = 0$; (b) $V_g = 1.0$; (c) $V_g = 2.0$.

An important observation from these calculations is the influence of an applied source-drain biasing voltage upon the region of electron accumulation. From Fig. 9, an increase in the applied voltage introduces a substantial increase in the density of accumulated electrons within the source-drain channel, and these electrons penetrate well into the narrowest part of the channel. In fact, these calculations show that the region of electron accumulation has almost completely eliminated the gate junction space-charge layers throughout a region where elementary theory would predict almost total channel "pinch-off."

The grounded source volt-ampere characteristic of this semiconductor device (Fig. 11) exhibits an electric current saturation. A comparison of this theoretical volt-ampere characteristic (Fig. 11) with the previously described characteristics for grounded drain operation (Fig. 8) indicates only small differences between the two types of operation. In a grounded drain circuit, saturation takes place at a slightly smaller source-drain biasing voltage, and the magnitude of source-drain electric current is slightly smaller.

Grounded source operation: reverse biased gate junctions

Figure 5(b) illustrates the circuit configuration assumed in this series of calculations; at all times the source-drain bias V_{sd} is maintained at 0.5 volts. In addition, it is assumed that an external biasing voltage V_g is applied to the gate junctions. In this circuit configuration, a distribution of reverse biasing voltage appears across the gate junctions (due to the source-drain channel voltage distribution), in addition to the biasing voltage applied from an external source. For comparison Fig. 12 illustrates the calculated electrostatic charge distribution within the source-drain channel for a gate junction bias V_g of zero, 1.0, and 2.0 volts.

Figure 12 also shows that an increase in gate junction biasing voltage produces a general increase in the gate junction space-charge layer width. Therefore, an overall decrease is observed in the mobile carrier density (electrons) within the source-drain channel. A substantial decrease is obtained in both the electron accumulation layer associated with the high-low junction, and in the electron density throughout a region of the channel lying on the drain contact side of this electron accumulation layer.

The voltage distribution associated with Fig. 12 implies an important property of this field-effect device. This voltage distribution is illustrated in Fig. 13 for a source-drain bias V_{sd} of 0.5 volts and a gate junction bias V_g of 2.0 volts. From Fig. 13, little voltage drop is observed within the region of minimum channel width. Instead (as shown in Fig. 13) almost all of the source-drain biasing voltage appears across a region of the source-drain channel lying on the drain contact side of the structure. This voltage distribution (in combination with the results shown in Fig. 12) indicates the existence of a region within the source-drain channel that is partially depleted of electrons, yet contains a negligible electric field component parallel to the direction of source-drain electric

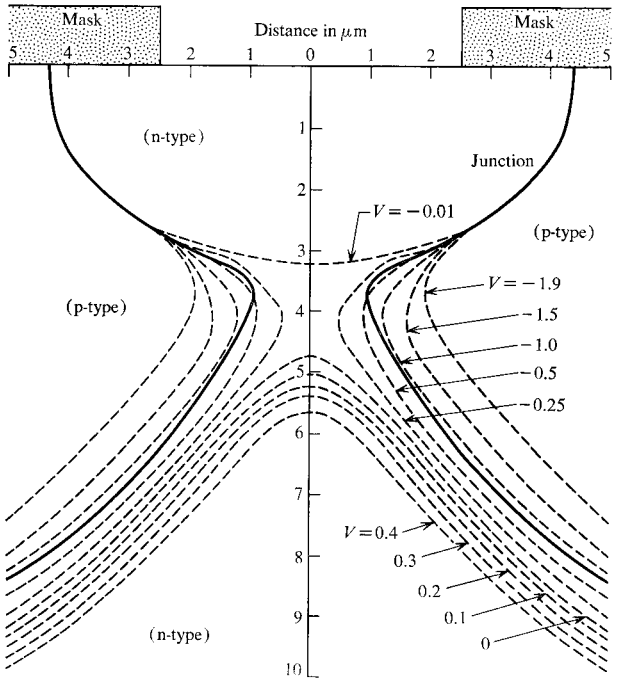
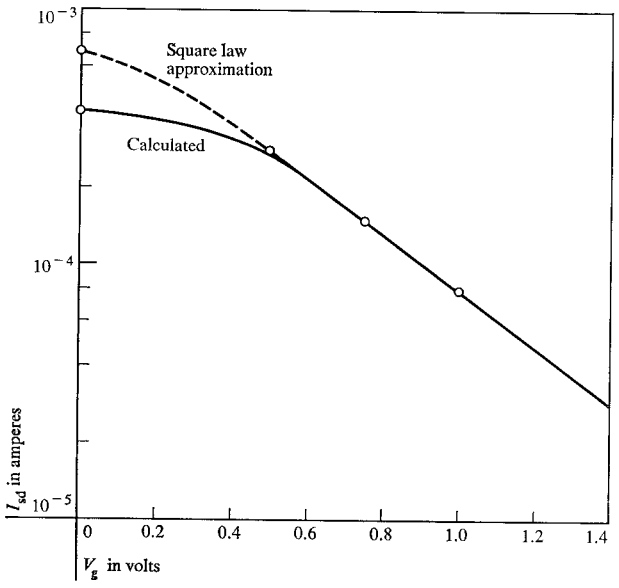


Figure 13 Calculated voltage distribution within the source-drain channel, grounded source operation. $V_{sd} = 0.5$; $V_g = 2.0$.

Figure 14 Calculated volt-ampere characteristics; grounded source operation. $V_{sd} = 0.5$.



current. Because an electric current is present within this analytical model, mechanisms other than drift must be considered important in the transport of electrons within the source-drain channel.

For completeness, Fig. 14 presents the calculated volt-ampere characteristics for this mode of device operation.

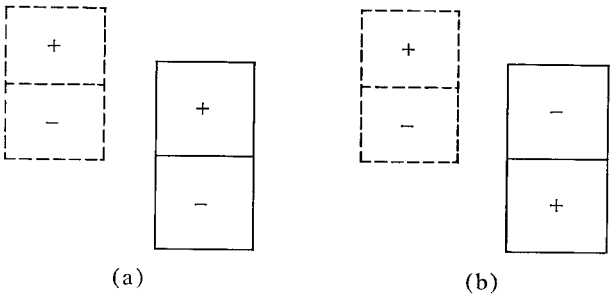


Figure 15 Illustration of electrostatic double-layer interaction within this field-effect device. (a) Grounded drain; (b) grounded source.

This figure illustrates the calculated source-drain electric current throughout a range of applied gate junction biasing voltage. Also illustrated is a comparison between these computer-calculated characteristics and a square-law approximation arising from the elementary theory of field-effect devices.[18]

It is emphasized that the comparison shown in Fig. 14 is not a straightforward application of the square-law equation found in the literature. The square-law equation was derived from a junction field-effect device containing an abrupt type of gate junction; therefore, the entire gate junction biasing voltage is assumed to be supported across a gate junction space-charge layer that resides on the channel side of the metallurgical junction. For this reason, the square-law relation shown in Fig. 14 is based upon calculations of that portion of the applied biasing voltage V_g supported on the channel side of the gate junction space-charge layer.

This comparison (Fig. 14) also shows that agreement is obtained between the two different computational methods at values of gate biasing voltage (V_g) in excess of the source-drain biasing voltage (V_{sd}). The square-law equation was derived for a model in which the applied source-drain voltage produces electric current saturation; 0.5 volts is insufficient to produce current saturation in this particular device. It is believed that the lack of current saturation accounts for the absence of a square-law characteristic when $V_g < V_{sd}$.

Conclusions and discussion

The results of this investigation suggest mechanisms of operation heretofore unreported in the technical literature on junction field-effect devices. In particular, when the source-drain voltage is sufficient to produce electric current saturation, this analysis implies that an electrostatic double-layer is induced into the channel of a junction field-effect device. In an n-type channel, the negative part of this double-layer arises from majority carrier (electron) accumulation, and the positive half from electron depletion. Furthermore, the magnitude and polarization

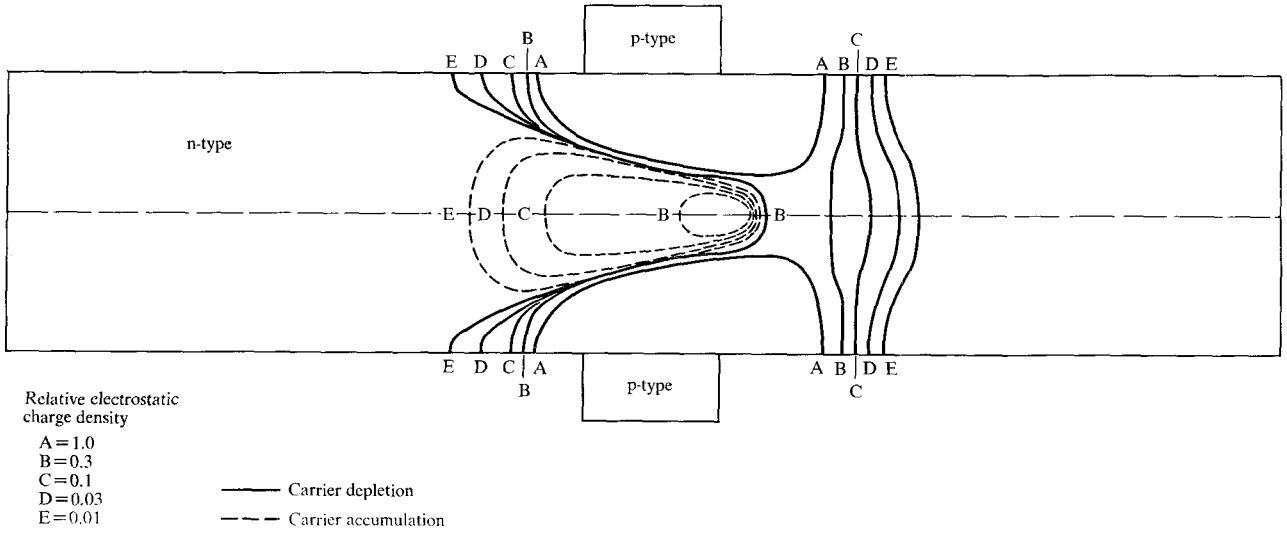


Figure 16 Calculated electrostatic charge distribution in a narrow gate JFET biased into electric current saturation.

of this double-layer are consistent with the magnitude and polarization of the applied source-drain biasing voltage.

From this proposal, the electrostatic charge distributions shown in Figs. 6 and 9 are easily explained. The charge distribution within the source-drain channel is composed of two electrostatic double-layers: The first is a "built-in" double-layer arising from the high-low junction and the second is associated with the mechanism of source-drain channel pinch-off. This second double-layer has a magnitude proportional to the applied source-drain voltage, and a polarization that differs in grounded source and grounded drain operation. This situation is schematically illustrated in Fig. 15. The total electrostatic charge distribution within the source-drain channel (Figs. 6 and 9) can be qualitatively explained in terms of the addition of two such double layers.

At equilibrium, the region of carrier accumulation within the source-drain channel is attributable to a high-low junction formed by the source contact impurity atom distribution (Fig. 4). This region of negative charge represents one-half of the electrostatic double-layer associated with this semiconductor structure; the positive half is dispersed throughout the source contact region. The density of this positive electrostatic charge is small.

In grounded drain operation, the double-layer associated with the high-low junction is in an opposite direction to the double-layer induced by gate junction pinch-off. The double-layer associated with the high-low junction (dashed line in Fig. 15) has a magnitude and direction determined by the impurity atom distribution; the region of carrier depletion (positive charge) is nearest the source contact. The gate-induced double-layer (solid line in Fig. 15) has a magnitude proportional to the applied source-drain voltage, and it is located so that its region of carrier depletion (positive charge) is nearly coincident with the region of carrier accumulation (negative charge), due to the high-low junction. At small values of applied voltage the gate-induced double-layer removes accumulated carriers from the source-drain channel (Fig. 6). At large values of applied voltage, accumulated carriers arising from the high-low junction are removed by the gate-induced double-layer, and the electron accumulation region of this induced double-layer becomes evident.

In grounded source operation, the electrostatic double-layer induced by the gate junctions is reversed in direction (Fig. 15); the negative side is facing the source contact. Furthermore, in this mode of operation the negative side of the induced double-layer is nearly coincident with the negative side of the "built-in" double-layer (formed by the high-low junction). For this reason, an increase in biasing voltage results in an apparent increase of the "built-in" electron accumulation region (Fig. 9), and a further depletion of electrons from the drain side of the channel.

It is recognized that this paper proposes a mechanism of JFET operation heretofore unreported in the literature: the formation of an electrostatic double-layer in the source-drain channel of this semiconductor device. Furthermore, because the structure used in this investigation is rather complex, these calculated results might well be an artifice due to the complicated geometry and impurity atom distribution. For this reason, similar calculations have been performed upon a junction field-effect transistor device of a more conventional type (Fig. 16).

Figure 16 illustrates the calculated electrostatic charge distribution within a conventional JFET, when the structure is biased well into electric current saturation. As proposed from calculations for the planar type device,

substantial carrier accumulation takes place within the source-drain channel. From Fig. 16 and other calculations of a similar nature, it has been found that an electrostatic double-layer is induced into the source-drain channel of junction field-effect transistors that are biased into electric current saturation. Furthermore, this induced double-layer is particularly pronounced in a narrow-gate JFET.

Numerous calculations similar to Fig. 16 have been conducted throughout a wide range of applied source-drain biasing voltage, and upon structures of substantially varying gate junction width. A result of these calculations is an understanding of the mechanisms whereby this electrostatic double-layer is induced into a source-drain channel by the gate junction space-charge layers. Specifically, carrier accumulation (and the associated region of carrier depletion) is a consequence of velocity-limited carrier transport in the source-drain channel,[19] in conjunction with the requirement of electric current continuity within this semiconductor device. Velocity-saturated carrier transport produces a situation for which an increase of electric field in the constricted region of a source-drain channel has little (or no) influence upon the electric current density. As a consequence, carriers accumulate within this constricted region until electric current continuity is established. The electrostatic charge associated with this region of carrier accumulation produces an increase of electron flux at the drain end of the gate junctions; thereby a region of electron depletion is also formed within the channel.

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